Gate-First AlGaN/GaN HEMT Technology for High-Frequency Applications

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***Abstract*—This letter describes a gate-first AlGaN/GaN high-electron mobility transistor (HEMT) with a W/high-k dielectric gate stack. In this new fabrication technology, the gate stack is deposited before the ohmic contacts, and it is optimized to stand the 870 °C ohmic contact annealing. The deposition of the W/high-k dielectric protects the intrinsic transistor early in the fabrication process. Three different gate stacks were studied: W/HfO_2, W/Al_2O_3, and $W/HfO_2/Ga_2O_3$. DC characterization showed transconductances of up to 215 mS/mm, maximum drain current densities of up to 960 mA/mm, and more than five orders of magnitude lower gate leakage current than in the conventional gate-last Ni/Au/Ni gate HEMTs. Capacitance–voltage measurements and pulsed-IV characterization show no hysteresis for the $W/HfO_2/Ga_2O_3$ capacitors and low interface traps. These W/high-k dielectric gates are an enabling technology for self-aligned AlGaN/GaN HEMTs, where the gate contact acts as a hard mask to the ohmic deposition.**

***Index Terms*—GaN, high-k dielectric, high-electron mobility transistor (HEMT), self-aligned.**

I. Introduction

ATTRACTING great interest for high-frequency and high-power amplifiers are AlGaN/GaN high-electron mobility transistors (HEMTs). During the last few years, the frequency performance of GaN HEMTs has increased steadily. Recently, Higashiwaki *et al.* reported an f_T of 181 GHz in unpassivated devices with $L_g = 30$ nm and thin AlGaN barrier [1]. Palacios *et al.* demonstrated an f_T of 153 GHz and an $f_{\max}$ of 230 GHz in HEMTs with $L_g = 100$ nm and an InGaN back barrier [2].

To further improve the frequency performance of AlGaN/GaN HEMTs, it is necessary to reduce the source and drain access resistances in addition to reducing the gate length [3], [4]. In 2007, Endoh *et al.* demonstrated a maximum f_T of 194 GHz in an $L_g = 45$ nm HEMT by cooling down the devices to 16 K [5], which significantly increased the electron mobility and reduced the access resistances [4].

Conventional fabrication techniques involve patterning and annealing the source and drain contacts before lithographically aligning the Schottky gate contact. This approach limits the minimum source-to-gate distance to around 500 nm, which makes very difficult to get source access resistances below $0.4\ \Omega \cdot$ mm. To reduce the source and drain access resistance further, it is necessary to self-align the ohmic source and drain to the gate electrode. There are different approaches for fabricating self-aligned devices, like using n^+ cap layers [6], regrowing the ohmic contacts [7], and using the T-shaped gate as a hard mask for the ohmic evaporation [8]. In the latter approach, a gate stack that can stand the ohmic anneal temperatures (> 800 °C) is necessary for fabricating self-aligned HEMTs with minimum contact resistance. However, the traditional gate metallization formed by Ni/Au or Ti/Pt/Au does not survive these ohmic anneal temperatures.

In this letter, we report AlGaN/GaN HEMTs fabricated by using a gate-first process, where a tungsten/high-k dielectric gate is deposited before the ohmic contacts and then survives the 870 °C anneal necessary to form ohmic contacts. Devices were fabricated with Al_2O_3 and HfO_2 gate dielectrics of different thicknesses, along with a combination of a Ga_2O_3/HfO_2 dielectric stack. These gate-first HEMTs are not only very useful for future self-aligned transistor structures but they also exhibit superior drain current density and transconductance compared to a reference HEMT with a standard Ni/Au/Ni gate stack.

II. Device Fabrication

The AlGaN/GaN transistor structure used in this letter was grown in Si (111) substrates by metal–organic chemical vapor deposition by Nitronex Corporation. The $Al_{0.26}Ga_{0.74}N$ barrier had a thickness of 17 nm, and it is capped by a 2-nm unintentionally doped GaN layer. Further details about the growth technology can be found in [9].

AlGaN/GaN transistors and metal–insulator–semiconductor (MIS) capacitors were fabricated on these wafers. First, mesa isolation was performed by electron cyclotron resonance etching with a 100-W BCl_3/Cl_2 plasma. Then, the high-k dielectrics were deposited on the entire sample. Al_2O_3 and HfO_2 films were deposited by a Cambridge Nanotech Savannah atomic layer deposition reactor, and Ga_2O_3 was grown by oxidizing the GaN cap layer with an O_2 plasma, as described in [10]. A summary of the different dielectrics used in this letter is shown in Table I.

After depositing the gate dielectric, a 60-nm-thick tungsten gate with $L_g = 3\ \mu$m was deposited by e-beam evaporation and patterned by a liftoff process. After the ohmic contact lithography, the dielectric was removed from the contact regions

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TABLE I
SUMMARY OF GATE DIELECTRICS AND FABRICATED DEVICES

Al_2O_3	HfO_2	Ga_2O_3 + HfO_2
15 nm	15 nm	3 nm + 12 nm
20 nm	20 nm	
25 nm	25 nm	

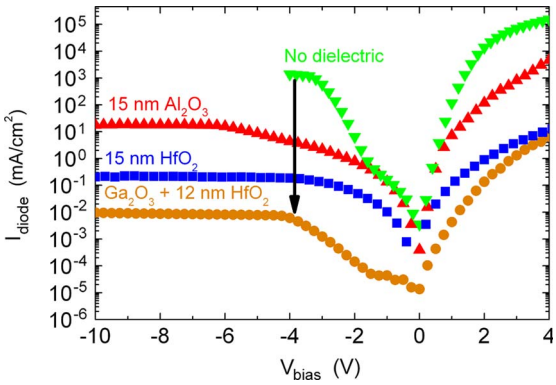

Fig. 1. Current–voltage characteristics for diode structures. The use of high-k dielectrics reduces the leakage current by a factor of up to 100 000.

by a buffered oxide etch (HF). Then, Ti–Al–Ni–Au source and drain contacts, with a source–drain separation of 6 μm, were deposited by e-beam evaporation. After the ohmic metal deposition and liftoff, the contacts (including the gate metal) were annealed at 870 °C for 30 s in a N_2 environment.

III. RESULTS AND DISCUSSION

The as-grown AlGaN/GaN wafers show a sheet charge density of 1.5×10^{13} cm^{-2} and a sheet resistance of 380 $\Omega/\square$. The deposition of the high-k dielectrics on the wafer surface increased the charge density by 20% and decreased the sheet resistance by 15%, as measured by the Hall and transmission line measurements. It has been proposed that dielectric layers increase the mobile charge density by reducing the fixed polarization charge [11].

Circular MIS capacitors with a diameter of 180 μm were fabricated on these samples. Fig. 1 shows the leakage current–voltage (I–V) characteristics of devices with different gate dielectric materials. All the MIS devices studied in this letter showed an important reduction of the reverse and forward leakage currents by up to 100 000 times with respect to the standard Schottky contacts, even though the MIS devices underwent the 870 °C ohmic annealing. Capacitance measurements showed that the dielectric constants for Al_2O_3 and HfO_2 were 10.8 and 18.1, respectively.

Capacitance–voltage hysteresis was measured in these capacitors by sweeping from -10 to 0 V and back to -10 V. The amount of hysteresis is an indicator of slow traps in the oxide and in the interface between the oxide and the semiconductor [12]. The use of a thin Ga_2O_3 layer between the HfO_2 and the GaN epilayer significantly improves the quality of the interface and reduces hysteresis, as shown in Fig. 2. In addition, the conductance method was used to measure the density of interface traps in the different dielectrics between the oxide and semiconductor by sweeping the small signal frequency from

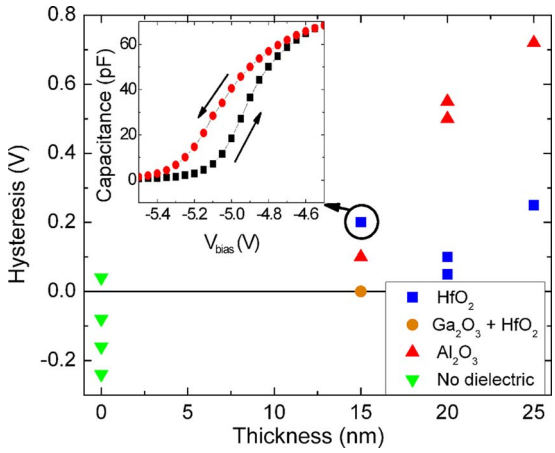

Fig. 2. Hysteresis for different capacitors versus dielectric thickness. The inset shows an example of hysteresis measurement.

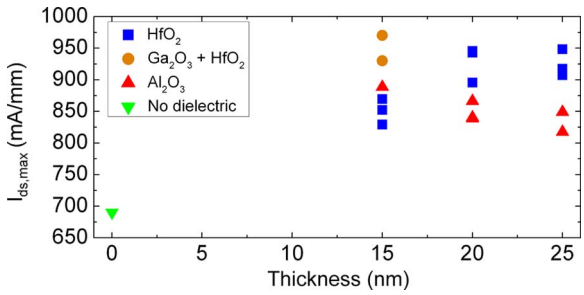

Fig. 3. Maximum drain current densities versus dielectric thickness. Currents measured at the highest $V_{\rm gs}$, where $I_g < 0.1$ mA/mm.

500 Hz to 1 MHz while biasing the capacitors around the depletion point [13]. The capacitors with the HfO_2 dielectric (with and without the Ga_2O_3) and Al_2O_3 had maximum interface trap densities of around 1×10^{12} and 3×10^{13} cm$^{-2} \cdot$ eV^{-1}, respectively, and the characteristic frequencies of the HfO_2 and Al_2O_3 interface traps were between 500 kHz and 1 MHz and less than 500 Hz, respectively. The predominance of slow traps in Al_2O_3 interface accounts for the greater hysteresis in the C–V measurements of the W/Al_2O_3 capacitors than in the W/HfO_2 capacitors.

The $I_{\rm ds}$–$V_{\rm ds}$ output characteristics were measured for the HEMTs with different dielectrics. The gate voltage of each transistor was swept to the highest possible gate voltage ($V_{\rm gs,max}$) without the gate leakage exceeding 0.1 mA/mm. The use of gate dielectric allows for 30%–40% higher $I_{\rm ds,max}$ than in standard devices. As shown in Fig. 3, the $I_{\rm ds,max}$ for the HfO_2 HEMTs increases with the dielectric thickness, and in the Al_2O_3 devices, $I_{\rm ds,max}$ decreases with the dielectric thickness. These trends are currently under investigation and will be the subject of a future publication.

As shown in Fig. 4, the transconductance of the MIS devices is higher than what would be expected considering the lower gate capacitance, even after taking the decrease in sheet resistance into account. There needs to be a relative increase in the saturation velocity or the mobility in order to account for this increase in transconductance. We believe that the presence of an insulator, particularly Al_2O_3, prevents mobility degradation due to the Schottky gate metal, which can explain the increase

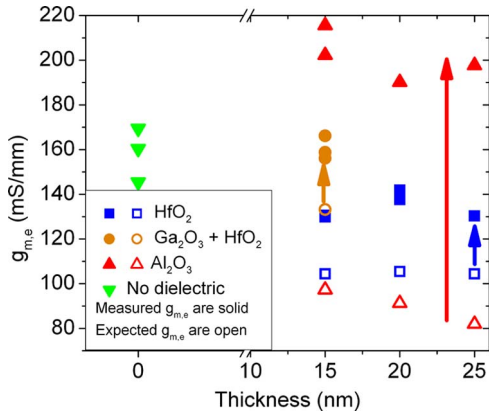

Fig. 4. Maximum extrinsic transconductances versus thickness with $V_{\rm ds} = 5$ V. The measured $g_{m,e}$ for the MIS HEMTs is much higher than what can be expected when taking the reduction in gate capacitance into account.

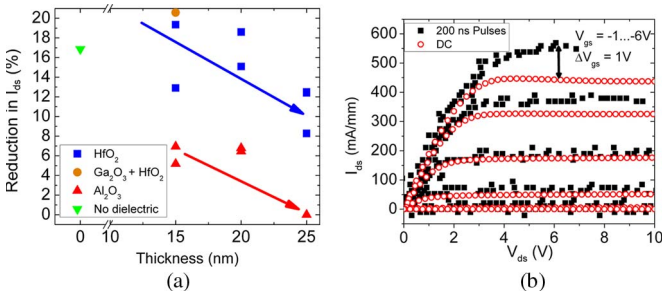

Fig. 5. (a) Reduction in drain current densities, resulting from the change in gate voltage pulse times from 1 ms to 200 ns. (b) Output characteristics of 15-nm Al_2O_3 HEMT for both 200-ns pulsed gate bias and dc gate bias.

in transconductance and electron velocity, as also reported by other groups [14]–[16].

Current collapse in the fabricated devices was characterized by pulsed-IV measurements with pulsewidths of 1 ms, 80 μs, and 200 ns and a load resistance of 100 Ω. Fig. 5(a) shows the reduction in $I_{\rm ds}$ when the gate pulsewidth was changed from 1 ms to 200 ns. For all dielectrics, dispersion reduces with an increase in dielectric thickness, as also demonstrated for Si_3N_4 [17]. The output characteristics shown in Fig. 5(b) show that the Al_2O_3 dielectric passivates the AlGaN surface [16]. The predominance of slow traps in Al_2O_3 may explain why Al_2O_3 passivates the semiconductor better than the HfO_2 despite having a higher interface density than HfO_2, but this is still under investigation.

IV. Conclusion

A new W/high-k dielectric gate stack has been developed, where Al_2O_3, HfO_2, and $Ga_2O_3 + HfO_2$ dielectrics have been evaluated. Devices with the W/dielectric gate stack were annealed at 870 °C and showed no reduction in performance compared to the reference HEMT. While the W/Al_2O_3 HEMTs show the best transconductance and dispersion performance, the $Ga_2O_3 + HfO_2$ combination has the best maximum drain current density, low interface traps, and negligible hysteresis along with transconductance that is comparable to that of standard Ni/Au/Ni gate HEMTs. Regardless of the dielectric used, these W/ high-k dielectric gates show great promise for self-aligned HEMTs in very high frequency applications.

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