XII. NEUROPHYSIOLOGY*

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A. OPERATIONAL AMPLIFIER

In recording through fine pipettes, a biologist needs a wideband amplifier of high input resistance, low noise, and good linearity. Probably the most critical component is the input element. For many years this element was either an electrometer triode or a good tube of higher transconductance compensated so as to behave like an electrometer. Now, with junction field-effect transistors (J-FET's) and insulated-gate field-effect transistors (IG-FET's or MOS-FET's), semiconductors have about the same high input resistance as thermionic devices. The IG-FET rivals the electrometer tube in its characteristics; although its noise is higher than that of a good J-FET, it has an input resistance of 10^{13}-10^{14} Ω. But the IG-FET has a fatal defect; the insulation of the gate is punctured by electrostatic transients of relatively low voltage. This fragility is no hazard for a circuit that is fixed into a rigid setup where protection can be built into the system. But the amplifiers used by physiologists are moved about, the inputs are coupled to electrodes that break occasionally, are repositioned, and replaced often. Protection of the input gate either compromises the input resistance or imposes a ritual for handling that is too easily violated.

If one studies the requirements of a physiologist, one finds very few instances in which there is a real need for an input resistance greater than 10^{12} Ω (and this is larger by an order of magnitude than the strictest experimental conditions warrant). Alternatively, one can specify that the leakage of the input to the rest of the amplifier never exceeds $|10^{-12}|$ A for a dynamic range of 1 V. Thus, if one had an amplifier whose minimum input resistance was 10^{13} Ω, and whose gate current did not exceed $|10^{-13}|$ A over a 1-V dynamic range of the input, the device would more than meet the requirements. A J-FET quite fulfills these conditions, given that it is properly bootstrapped, and it has the additional advantage that it is not fragile like the IG-FET.

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The simplest model for a device that shows constant gate-leakage current is illustrated in Fig. XII-1, a source follower (T_1) that is clamped in its drain current, I_{DS}, and in its drain-source voltage, V_{DS}.

An alternative, however, is shown in Fig. XII-2 wherein T_3 "cascodes" T_1. Provided the drain voltage is high enough, the V_{GS} of T_3 is reasonably constant over a wide

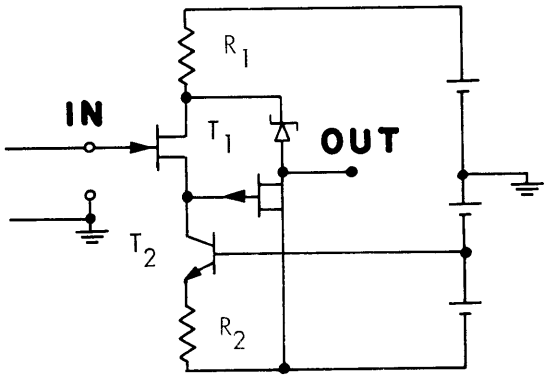


Fig. XII-1.

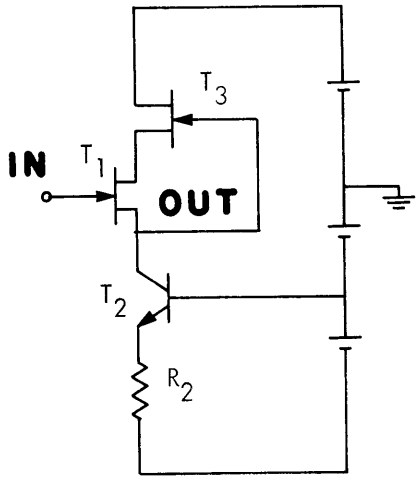


Fig. XII-2.

range of V_{DG} at a constant I_{DS}. Thus T_1 has an almost constant I_{DS} set by T_2 and R_2 and an almost constant V_{DS} set by T_3. T_3 ought to have so large a V_{GS} at the I_{DS} set for T_1 that the V_{DS} of T_1 is well past the knee on the I_{DS}/V_{DS} curve for T_1 at $V_{GS} = 0$. Practically, this stipulates that the I_{DSS} of T_1 at $V_{GS} = 0$ is low and that of T_3 is high.

The gate-leakage current (I_{GSS}) of an N-type J-FET is positive and related to the V_{DG}. But if the source is held slightly negative to the gate at a fixed V_{DG}, the gate-leakage current (which can be regarded as the backleakage of a drain/gate diode) can be balanced by an equal forward current through the gate-source diode. At this V_{DG} and I_{DS} there is no net gate current. If both the I_{DS} and the V_{DS} of a J-FET can be clamped, then this implies not only an increase of the input resistance of the J-FET (through bootstrapping), but also the possibility of cancelling the gate current. In practice the gate current cannot be held stable at a cancellation to better than 1/1000 that of the specified gate leakage. A device of specified 10^{-8} A leakage cannot be held stable to a net leakage of less than 10^{-11} A in a compensatory circuit. Thus T_1 ought be a species of J-FET whose maximum substrate gate leakage is 10^{-10} A. Incidentally, the cancellation of gate leakage is good even with a slight shift in temperature, since the drain-gate diode and gate-source diode have the same substrate and the same characteristics.

An additional requirement, however, is now brought forth by the physiologist. He

is interested in the exact temporal variations in voltage of, say, a nerve spike and is willing to tolerate increased noise to recover high-frequency components. His electrodes, high in resistance, are shunted by a capacitative loss across the wall, and the electrode optimally acts as a simple single-RC, lowpass filter. (In the worst cases the electrode acts as a transmission line.) If there are both little delay time in the input amplifier and a voltage gain, the output can be fed back in phase to the input through a small capacitor and so restore the high-frequency components at the expense of increasing the high-frequency noise. This method is sometimes called "negative capacitance." Thus the amplifier can be redesigned so as to clamp the characteristics of the input J-FET (T_1) and provide in-phase gain with respect to the input signal. One such design is sketched in Fig. XII-3, where the comparator amplifier has high gain so as to

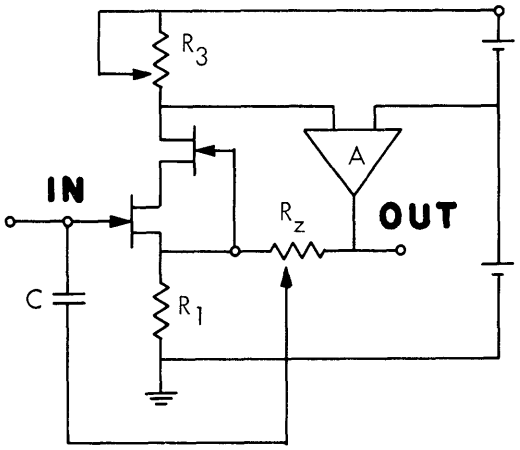


Fig. XII-3.

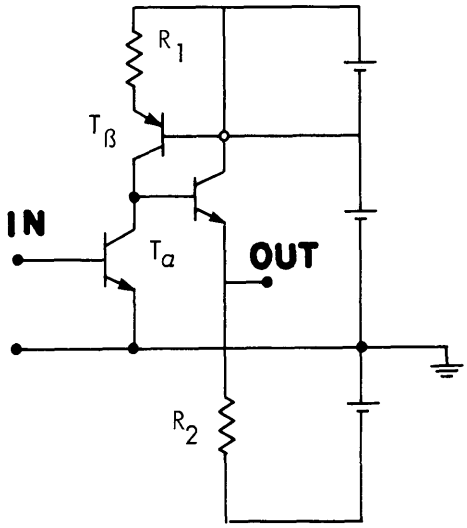
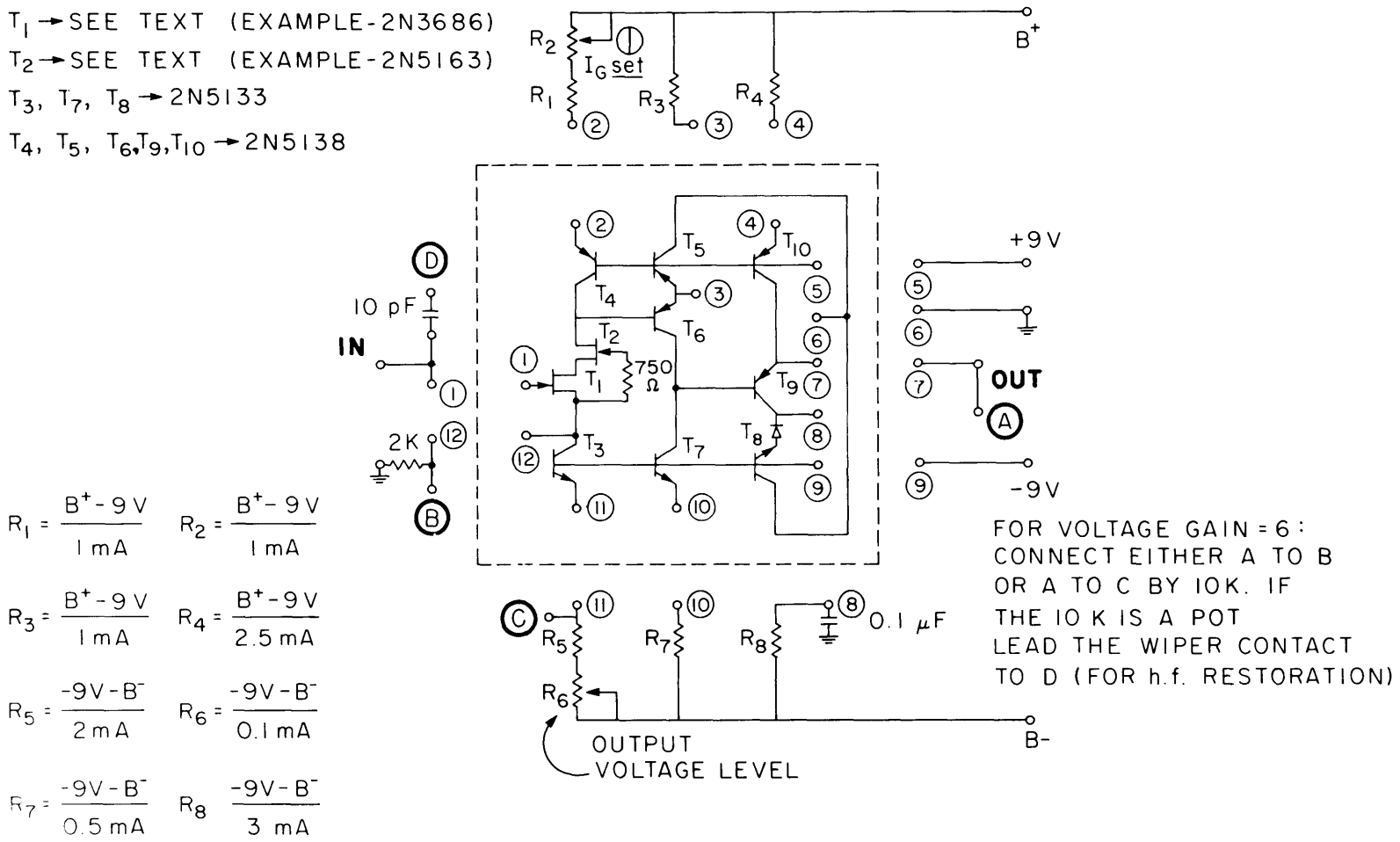


Fig. XII-4.

keep the voltage drop across R_3 very close to constant. At the same time the output then has an in-phase voltage gain, with respect to the input, of $\frac{R_1 + R_2}{R_1}$. R_2 can be a potentiometer, and the wiper arm is connected by C to the input. Thus, the signal used for regenerating the high frequency can be varied from a gain of 1 (with respect to the input signal) to $\left(1 + \frac{R_2}{R_1}\right)$.

Before exhibiting the final design, consider the voltage gain of the amplifier in Fig. XII-4.

Clearly, T_β and R_1 are operating as a "current source," but one for which there is a very high resistance in parallel. That resistance is always positive and will depend as much on the characteristics of the individual transistor as on those of the species.



$R_1 = \frac{B^+ - 9\,V}{1\,mA}$ $R_2 = \frac{B^+ - 9\,V}{1\,mA}$

$R_3 = \frac{B^+ - 9\,V}{1\,mA}$ $R_4 = \frac{B^+ - 9\,V}{2.5\,mA}$

$R_5 = \frac{-9V - B^-}{2\,mA}$ $R_6 = \frac{-9V - B^-}{0.1\,mA}$

$R_7 = \frac{-9V - B^-}{0.5\,mA}$ $R_8 = \frac{-9V - B^-}{3\,mA}$

Fig. XII-5.

Such a loading of the collector is not much used, because of great individual variation in transistors and because the Miller effect at such a high gain, as well as the effects of capacitance to ground, degenerate the high frequencies. This characteristic, however, makes the "current source" loaded collector an almost ideal device for an operational amplifier. Since the voltage gain that we are seeking is relatively low, the greater open-loop gain we have, the better we can clamp the operating conditions of T_1; hence, the design such as shown in the circuit for the single unit in Fig. XII-5. T_1 is a 2N3686, or 2N3088, picked for $V_{PO} \leq 1$ V and $I_{GSS} \leq 0.1$ nA. Its I_{DDS} ought to lie between 0.5 and 1 mA. T_2 is a 2N5163, or 2N3086, of $I_{DSS} \sim 3$ mA.

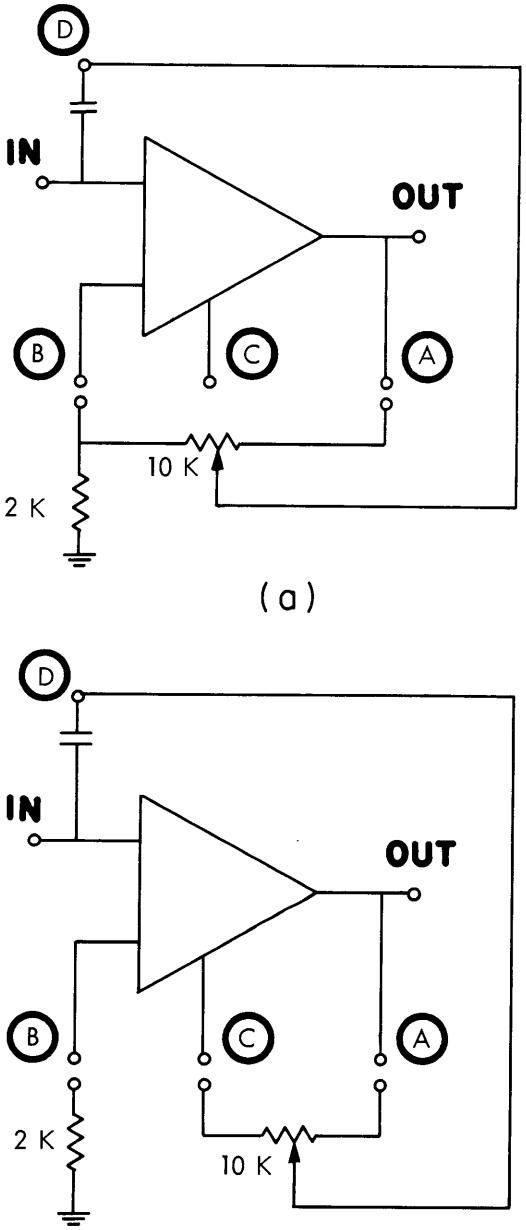


Fig. XII-6.

The open-loop voltage gain of this circuit is $\geq 20,000$ with the transistors shown. The closed loop voltage gain is 6 when it is connected as in Fig. XII-6a. Adjustment of R_2 in Fig. XII-5 sets I_{DS} and so I_{GSS} of T_1. Adjustment of R_6 in Fig. XII-5 sets the output voltage level relative to the input, but affects the I_{DS} only by a small factor.

Transistor T_{10} is not absolutely necessary – but, as a constant-current source, it ensures that the high positive voltage supply, as well as the high negative voltage supply, is drained at constant current. Such a drain allows those supplies to operate at higher internal impedance than if the current drains were variable with input signal.

Notice that no current is drawn from the two 9-V batteries. Indeed, if anything, the base currents of the transistors act to charge rather than to discharge the cells, and it might almost be necessary to put a leakage resistor across the cells to ground to balance out the small charging current. At any rate, the 9-V cells last as long as their shelf-life in the circuit.

An alternative version of the circuit is shown in Fig. XII-6b. It has the same voltage gain, noise, and stability as in Fig. XII-6a, which is the idealization of Fig. XII-5. For the single unit, Fig. XII-6a is the preferable configuration, for it allows slightly greater loading of T_9 at large positive voltages. This is an academic point, however, since these amplifiers are designed to feed into recording devices of moderate-to-high input impedance. But the configuration in Fig. XII-6b allows two of these circuits to be joined to give a push-pull amplifier with high rejection ratio as in Fig. XII-7, a schematized twinning of Fig. XII-5. If B_1 and B_2 are connected as shown, the voltage difference in outputs A_1 and A_2 shows a 12-fold voltage amplification of the voltage difference in inputs, and the rejection ratio of common mode signal is several thousand at least. This rejection ratio does not vary much with nonzero differences at the input. The conversion from two independent units to a single push-pull amplifier is no more complex than replacing the two separate 2K resistors that connect B_1 and B_2 independently to ground by a single 2K resistor that connects B_1 and B_2. Furthermore, in this configuration of push-pull, the noise of the grounded input is equal to or less than 15 μV rms. Thus, by grounding B, one has a single-ended device in which the restoration of high frequency to

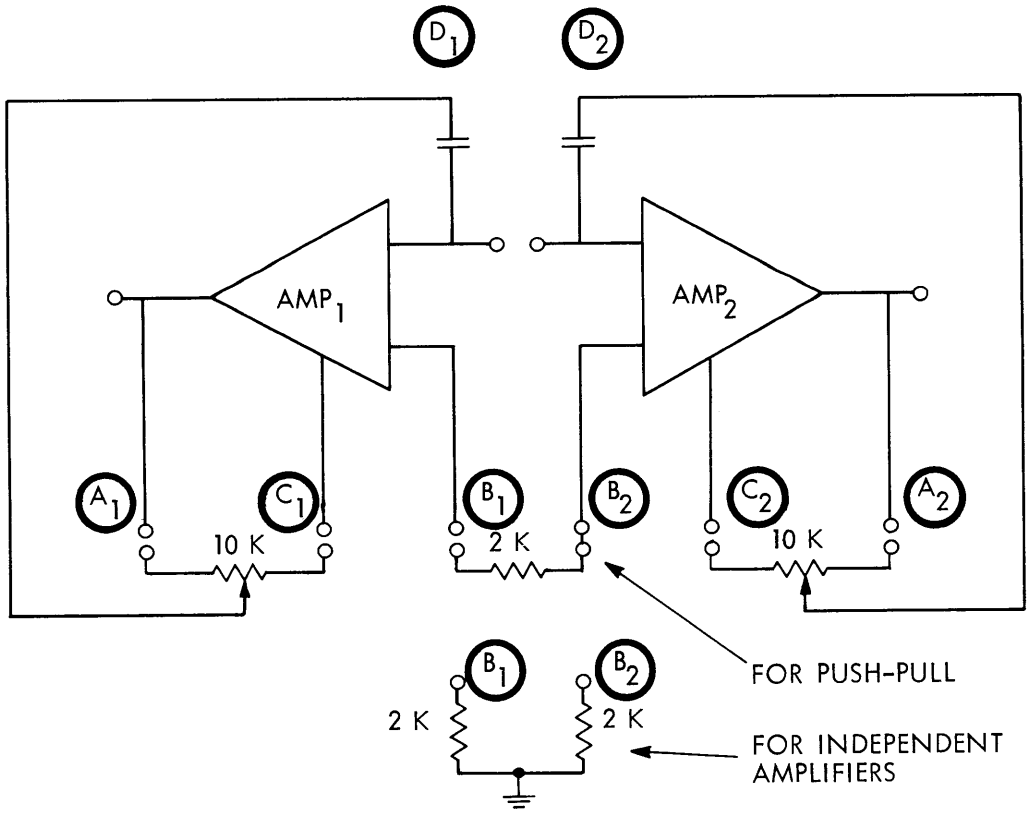


Fig. XII-7.

the input is not compromised by noise significantly above that which occurs in the single unit. But the advantage to such operation is that the push-pull amplifier drifts far less than the single unit with change in B^+, B^-, or temperature.

There are a few caveats in construction.

1. On no account use wire-wound potentiometers. Use instead type J 2-Watt potentiometers and ground the cases.
2. Keep the intercollector lead between T_6 and T_7 relatively short.
3. Drift is relatively low in the single device, and is related more to drift of batteries than to the usual fluctuations of temperature in the laboratory. It is best, therefore, to use a simple power supply for B^+ and for B^-. The best 9-V bias supplies are Hg cells.

Method of adjustment and testing.

1. Initially R_2 and R_6 are sliding adjustments. Ground the input and set R_2 in middle range; set the 10K feedback potentiometer (between A and B or C) with wiper at lowest gain point and adjust R_6 until output is about ground level.
2. Place a 10-pF capacitor between input and ground and transiently short the input to ground every 10 sec.
3. Adjust R_2 until the net tendency of the gate to drift positive is minimum at no more than 0.01 V/sec. But do not adjust so that the gate drifts slowly negative.
4. Now reset R_6 so that the output again sits at ground level. Thereafter, R_2 needs little, if any, adjustment. It can be checked occasionally. The gate current can be adjusted to 10^{-14} A for short periods, but cannot be held reliably to better than 10^{-13} A.
5. Test the noise in the DC to 100 kHz band with the input grounded. Noise referred to input is usually around 10-15 μV rms. It should not exceed 20 μV rms unless the input transistor is noisy.
6. Now attach a 20-MΩ resistor (1/2 W) through a very short lead (1 inch or less) to the input and feed through it a square wave, variable in amplitude from 1 mV to 1 V. The signal will show a high-frequency loss. Advance the wiper arm on R_5 to restore high frequency until a slight overshoot appears at the steps of the square wave. Check the rise time. It ought to be between 3 and 5 μsec. Check the noise of this compensation. For this rise time one cannot have, at room temperature, less than ~350 μV rms for the DC-50 kHz band. The observed noise ought not to exceed 350 μV rms.
7. Overcompensate the feedback from the feedback potentiometer until damped ringing occurs at each step of the square wave. The ringing ought to be symmetrical for upward and downward steps in voltage.

8. Now check drift in the usual way. Ground the input and record fluctuations in output. At constant T (varying no more than 1 °C) and with constant supply voltages (varying no more than a few millivolts), the net drift ought to be ~20 μV/h and show no short fluctuations larger than the net drift. The dual device, run in push-pull mode, will, obviously, be more stable over changes in temperature and drift in power supply.

Specifications for circuit described in this report. (Other gains may be used.)

Gain (voltage) = 6

Dynamic Range of Input = ±1 V with respect to ground

Output Level adjustable ±0.5 V with respect to ground

Input Resistance $\geq 10^{13}\ \Omega$

Gate Current (after adjustment) stable at $10^{-12}\ \text{A} \geq I_{G*} \geq 10^{-13}\ \text{A}$

Noise (DC-100 kHz) $\leq$ 20 μV (with input grounded)

Noise for HF Restoration (DC-100 kHz) $\leq$ 400 μV rms

(using $\frac{1}{2}$-W 20-MΩ resistor in series with input capacitative shunt to ground <10 pF additional to capacitative shunt in the circuit itself and adjusting for rise time of square wave τ, such that 3 μsec $< \tau <$ 5 μsec)

Drift (at constant B^+, B^- and bias voltages and at a constant room temperature) $\leq$ 20 μV/h.

Printed circuits are available for the 4" × 4" × 2" box.

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