MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 ELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 9

Issued: October 31, 2003 **Due:** November 12, 2003

Reading Assignments:

Lecture 18 (11/4/03) - Chap. 11 (11.3 to end)
Lecture 19 (11/6/03) - Chap. 12 (12.1, 12.2)
Lecture 20 (11/13/03) - Chap. 12(12.3 to end); Chap. 13 (13.1)
Lecture 21 (11/18/03) - Chap. 12 (12.4)
Lecture 22 (11/20/03) - Chap. 14 (14.1, 14.2)
Lecture 23 (11/25/03) - Chap. 13 (13.2 to end)

Announcements:

The **second hour exam** is scheduled for Wednesday night, November 5, from 7:30 to 9:30 pm in Room 10-250. The exam is closed book and will cover the material through 10/29/03 and Problem Set #8, including BJT operation and large signal modeling; the MOS capacitor; MOSFET operation and large signal modeling; incremental models for diodes, BJTs, and MOSFETs; and MOSFET inverters. There will be no weblab or HSPICE questions on the exam.

The **design problem** will be distrubuted on Friday, Nov. 7 and will be due on Wednesday, November 26. **Problem Set 9** (this one) is not due until Nov. 12, but you should try to finish it early so you can begin work on the design problem right away.

Problem 1 - Both parts of this problem deal with current mirrors for current source biasing:

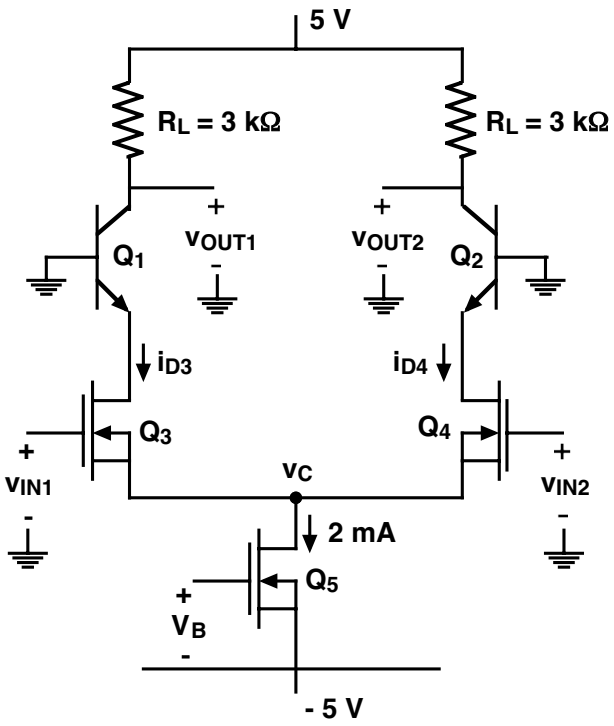
a) Do Problem 11.1 in the course text.
b) Do Problem 12.6 in the course text.

Problem 2 - Do Problem 11.6 in the course text.

Problem 3 - Do Problem 11.10 in the course text.

Problem 4 - The circuit on the next page uses three identical n-channel MOSFETs and two identical npn BJTs in a differential amplifier. Note that each side of the differential amplifier is a cascode circuit. The transistors have the following properties:

n-channel MOSFETs: $K = 2 \times 10^{-3}\ A/V^2$, $V_T = 1\ V$, $|V_a| = 20\ V$
npn BJTs: $\beta = 100$, $v_{BE} \cong 0.6\ V$, $|V_a| = 100\ V$



a) With both inputs zero (i.e, $v_{IN1} = v_{IN2} = 0$) determine the indicated quiescent currents and voltages. Specify units:

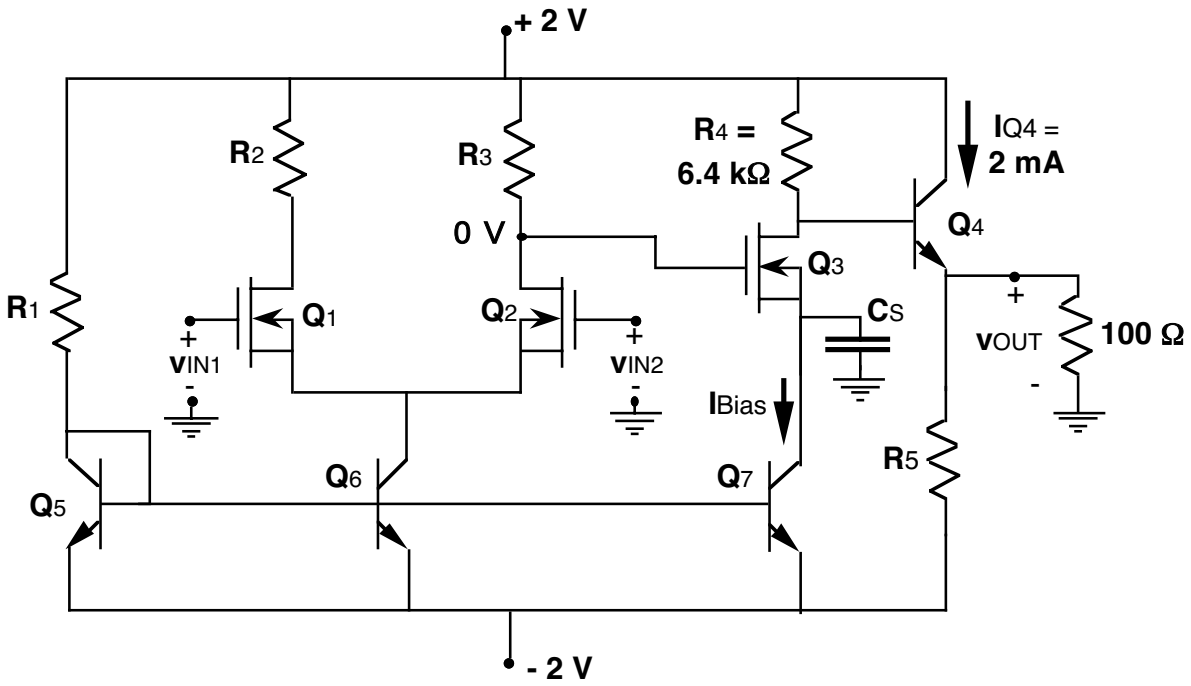
i) I_{D3} (= I_{D4}) ii) V_{OUT1} (= V_{OUT2})
iii) V_C iv) V_{CE1} (= V_{CE2})
v) V_{DS3} (= V_{DS4})

b) Draw two mid-band linear equivalent half circuits (LEHCs) for this differential amplifier, one for common-mode inputs and one for difference-mode inputs. Label all of the elements in your schematics.

c) Derive literal expressions for the common-mode and difference-mode voltage gains, A_{vc} and A_{vd}, respectively, of this differential amplifier. The output conductances of Q_1, Q_2, Q_3, and Q_4 are of insignificant effect and should be neglected in these derivations.

Problem 5 - Consider the differential amplifier circuit illustrated on the next page. In this circuit the three n-channel MOSFETs are identical; they have a threshold voltage, V_T, of 1 V, a drain current in saturation of $2.5(v_{GS} - V_T)^2$ mA, and an Early voltage of 10 V. The MOSFETS do not operate properly if $(v_{GS} - V_T)$ is less than 0.2 V. The npn bipolar junction transistors (BJTs) all have forward betas, β_F, of 100, reverse betas, β_R, of 5, and an Early voltage of 50 V. The BJT sizes have been adjusted to that to a good approximation you may use $|V_{BE,ON}| = 0.6$ V; $|V_{CE,SAT}| = 0.2$ V. Assume C_S is a short at mid-band frequencies, and R_2 and R_3 are identical.

Note: The value of the resistor R_4, the quiescent collector current on Q_4, and minimum quiescent voltage on the gate of Q_3 are indicated on the schematic, as are the supply voltages.



a) What must the bias level (I_{Bias}) on Q_3 be to have a quiescent output voltage of approximately 0 V? (Assume that the quiescent collector current of Q_4 is 2 mA, as indicated, and do not forget its base current.)

b) Select R_5 be to be consistent with a quiescent collector current in Q_4 of 2 mA, and a quiescent output voltage of approximately 0 V.

c) Select R_1 to give a bias current through Q_5 of 1 mA. You may ignor the base currents of Q_5, Q_6, and Q_7.

d) i) Draw a small signal linear equivalent <u>half</u> circuit one could use to calculate the signal voltage on the gate of Q_3 due to the difference-mode input signal, $v_{in1} - v_{in2}$. Find an expression for this voltage in terms of incremental linear equivalent circuit model parameters.

ii) Write an expression for the differential-mode voltage gain of the differential stage (Q_1, Q_2) in terms of the resistors, the MOSFET K-factors, and the quiescent bias levels of Q_1 and Q_2. Select R_2 (= R_3) and the drain current of Q_1 and Q_2 to maximize this voltage gain (magnitude).

e) Suppose you can replace R_2 and R_3 with a current mirror made with p-channel MOSFETs with $|V_T| = 1$ V and $|V_A| = 20$ V. Draw the schematic of such a current mirror, and calculate what inpact this would have on the voltage gain.

f) Looking at the output stage, what are the most positive and negative values of v_{out} possible? Explain your answers.