MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.012 ELECTRONIC DEVICES AND CIRCUITS

Problem Set No. 10

Issued: November 26, 2003 **Due:** December 5, 2003

Reading Assignments:

Lecture 24 (12/2/03) - Chap. 14 (14.3; you can skip the derivation of the gate capacitance expressions, jumping from Eq. 14.30b to Eq. 14.48, and what follows)
Lecture 25 (12/4/03) - Chap. 16 (16.3.1, 16.3.3)
Lecture 26 (12/9/03) - No more reading assignments, but if you want something useful to read, check out Chap. 15 (15.3, 15.4) and Chap. 16 (16.1, 16.2.1a).

The **final exam** will be held between 9 a.m. and Noon on Monday, December 15. It will be closed book with a formula sheet provided and a two-page crib sheet permitted.

Problem 1 - (a) Do Problem 14.4 in the course text.

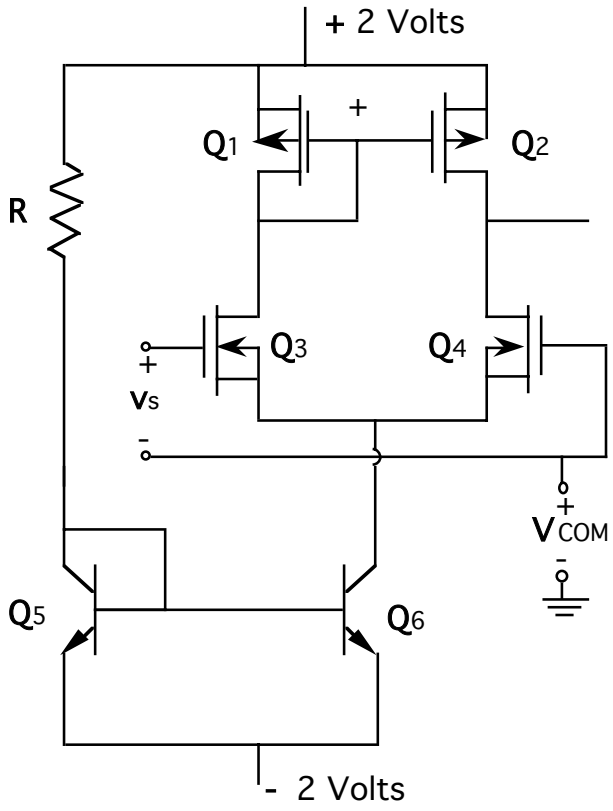
(b) Do Problem 14.9, Parts a, b, d, and e, in the course text.

Problem 2 - Do Problem 14.8 in the course text. In working this problem, ignor the output resistances of the transistors, assume that the source resistance, R_T, is much less than r_1 and R_{B1}' (= $R_{B11} \| R_{B12}$), and assume that the two transistors are biased at the same collector current level. Also, consider the effect of letting R_{C1} be zero on the gain of the circuit and on the high frequency response.

Problem 3 - Calculate the small signal input and output resistance of the amplifier used in Problem 2 (i.e. the amplifier in Figure 13.10 of the course text). Calculate the input resistance looking in at the base of Q_1 to the right of R_{B11} and R_{B12} (that is, do not include R_{B11} and R_{B12} in your answer), and calculate the output resistance looking in at the collector of Q_2 (that is, do not include R_{C2} in your answer); do not ignor the output resistances of the transistors when calculating the output resistance. Compare your answers with the input and output resistances of a cascode stage like that discussed in Lecture 23 (see Foil 6).

Problem 4 - In the differential amplifier shown at the top of the next page Q_1 and Q_2 are identical p-channel MOSFETs with K = 1.0 mA/V^2, V_T = - 0.5 V, and $|V_A|$ = 10 V; Q_3 and Q_4 are identical n-channel MOSFETs with K = 2.0 mA/V^2, V_T = 0.5 V, and $|V_A|$ = 20 V; and Q_5 and Q_6 are identical npn BJTs with β_F = 150, $|V_A|$ = 50 V, and $V_{BE,ON}$ = 0.6 V. The BJTs are in saturation when V_{CE} is less than 0.2 V (i.e., when the base-collector junction is forward biased 0.4 V, or more). The MOSFETs must be operated with $|V_{GS} - V_T| > 0.2$ V, and the BJTs with $I_C > 10$ μA.

(a) Select R so the quiescent drain currents in Q_3 and Q_4 are 0.5 mA.



(b) What is the quiescent value of the gate-to-source voltage, V_{GS}, on the MOSFET, Q_3? Recall that the quiescent drain current in Q_3 is 0.5 mA.

(c) The voltage v_{COM} is applied to both inputs; the voltage v_s has no DC level and is only a small signal voltage. With $v_s = 0$, over what range of values for v_{COM} will all the transistors in this circuit stay biased in their forward active regions?

(d) With $v_s = 0$, and v_{COM} within the range you found in Part (c), what is value of the output voltage, v_{OUT}?

(e) What is the quiescent (DC) power dissipation in this circuit?

(f) This part of the problem concerns the small signal behavior of this amplifier.

(i) In terms of v_{COM} and v_s, what are the differential- and common-mode input voltages, v_{ID} and v_{IC}, respectively?

(ii) What is the small-signal, mid-band voltage gain of this circuit for the input v_s, i.e., what is $A_v = v_{out}/v_s$?

(iii) Is it possible to increase the voltage gain, $|A_v|$, by changing the bias level, I_{C6}? If yes, indicate whether I_{C6} should be increased or decreased, why, and how large $|A_v|$ can be. If no, explain why not.