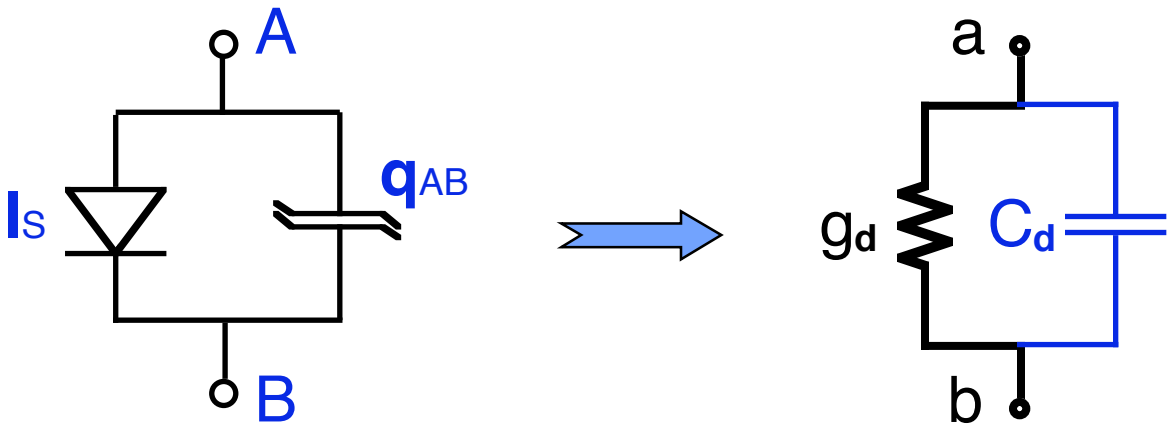
Lecture 15 - Digital Circuits: Inverter Basics - Outline

- **Announcements**
  - Handout - Lecture Outline and Summary
  - The MOSFET alpha factor - use definition in lecture, not text
    ["+1" is missing in Eq. 10.23]
- **Review - Linear equivalent circuits**
  - Notation: $i_D = I_D + i_d(t)$ where i_D = total current; I_D = bias; $i_d(t)$ = increment
  - LECs: the same for npn and pnp; the same for n-MOS and p-MOS;
    all parameters depend on bias, so maintaining a stable bias is critical
- **Digital building blocks - inverters**
  - A generic inverter
  - MOS inverter options
- **Digital inverter performance metrics**
  - Transfer characteristic: logic levels and noise margins
  - Power dissipation
  - Switching speed
  - Fan-out, fan-in
  - Manufacturability
- **Comparing the MOS options**
  - And the winner is….

- **LEC for the p-n junction diode:**



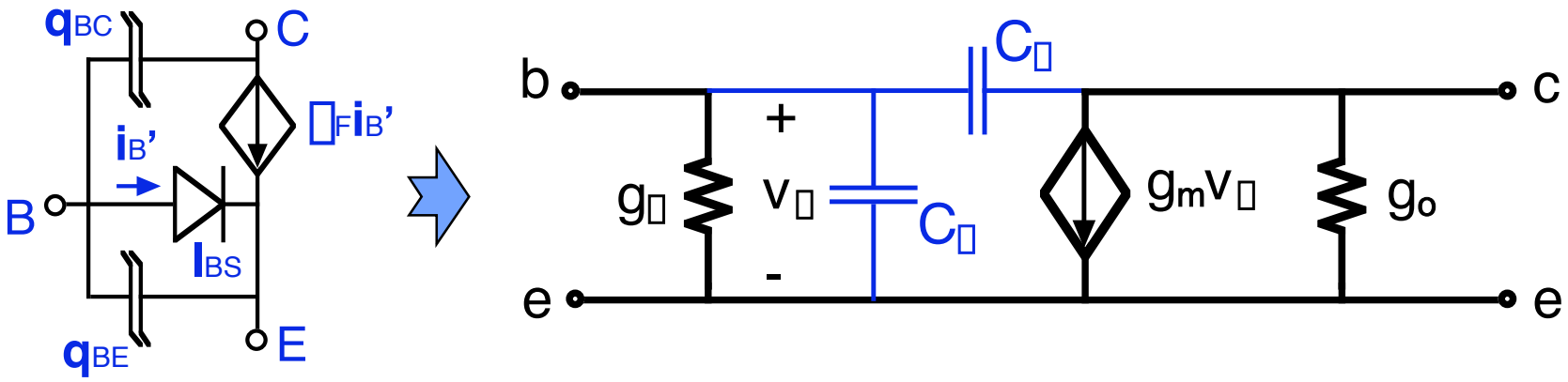
$$g_d = \frac{q}{kT} I_{BS} e^{qV_{AB}/kT} \quad \frac{qI_D}{kT}$$

$$C_d = C_{dp} + C_{df}, \text{ where } \quad C_{dp}(V_{AB}) = A\sqrt{\frac{q\varepsilon_{Si}N_{Ap}}{2(\phi_b - V_{AB})}} \quad \text{and}$$

$$C_{df}(V_{AB}) = \frac{qI_D}{kT}\frac{\left[w_p - x_p\right]^2}{2D_e} = g_d\tau_d \quad \text{with} \quad \tau_d \equiv \frac{\left[w_p - x_p\right]^2}{2D_e}$$

(Note: The capacitance expressions assume an n^+-p diode)

- **Linear equivalent circuit for the <u>BJT</u> in F.A.R:**



$$g_m = \frac{q|I_C|}{kT} \qquad g_\pi = \frac{g_m}{\beta_o}$$

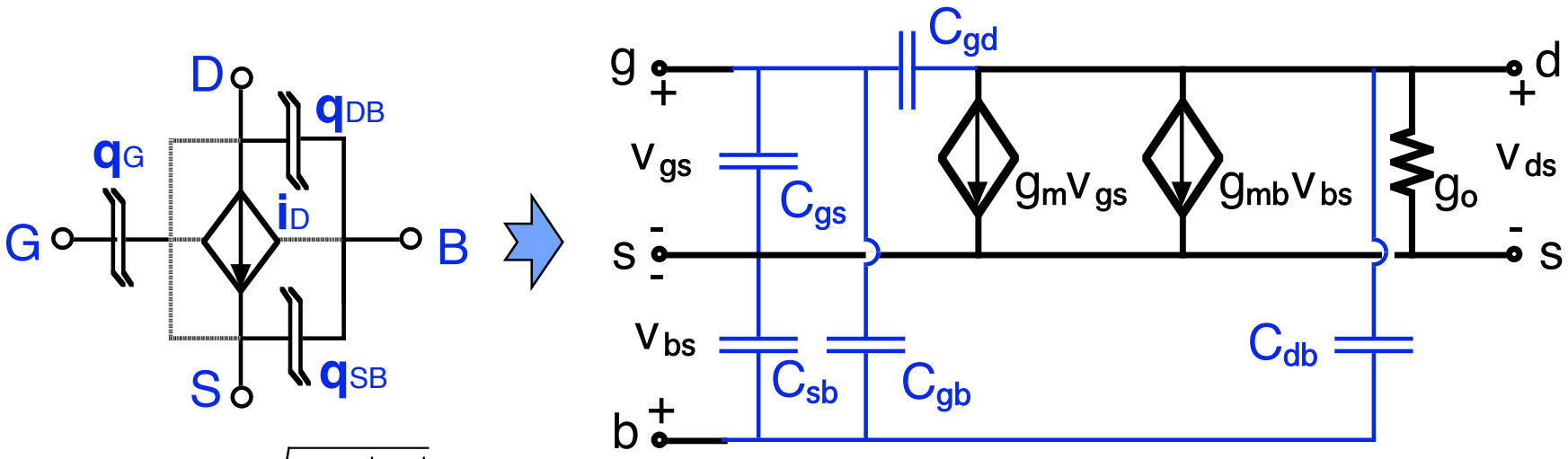
$$g_o = |I_C| \quad \text{or} \quad \left|\frac{I_C}{V_A}\right|$$

$C_\pi = g_m \tau_b +$ B - E depletion capacitance, where $\tau_b = \dfrac{w_B^2}{2 D_{\substack{minority \\ .in\ base}}}$

$C_\mu =$ B - C depletion capacitance

(Note: The LEC is the same for npn and pnp BJTs.

- **Linear equivalent circuit for the MOSFET in saturation:**



$$g_m = \sqrt{2K\,|I_D|}$$

$$g_o = \lambda |I_D| \quad \text{or} \quad = \left|\frac{I_D}{V_A}\right|$$

$$g_{mb} = \chi g_m = \chi\sqrt{2K\,|I_D|} \qquad \text{with} \qquad \chi = \frac{1}{C_{ox}^*}\sqrt{\frac{\varepsilon_{si} q N_A}{|q\phi_p| + V_{BS}}}$$

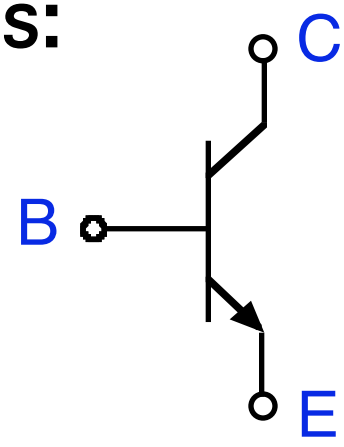
$$C_{gs} = \frac{2}{3} W L C_{ox}^* \qquad C_{sb}, C_{gb}, C_{db}: \text{ depletion region capacitances}$$

$$C_{gd} = W C_{gd}^* \quad \text{where } C_{gd}^* \text{ is the gate-to-drain fringing and overlap capacitance per unit gate width}$$

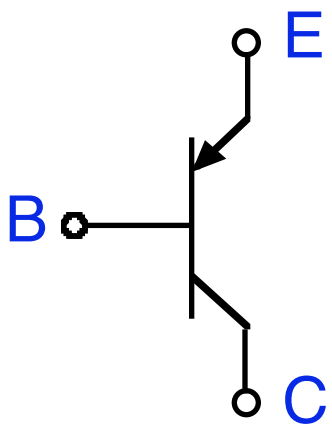
(Note: The LEC is the same for n- and p-channel MOSFETs.

Circuit symbols:

BJT:

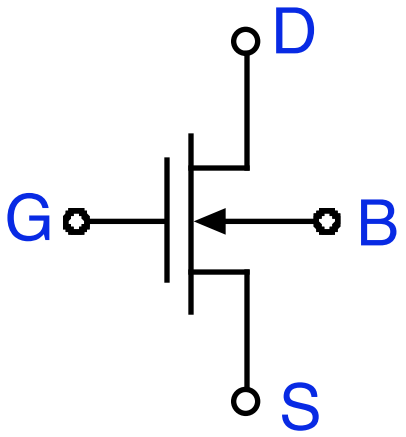


npn

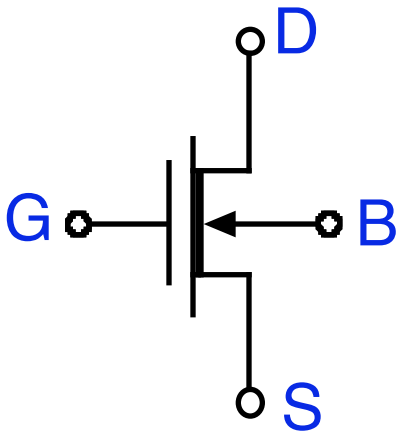


pnp (usual circuit orientation)

MOSFET:

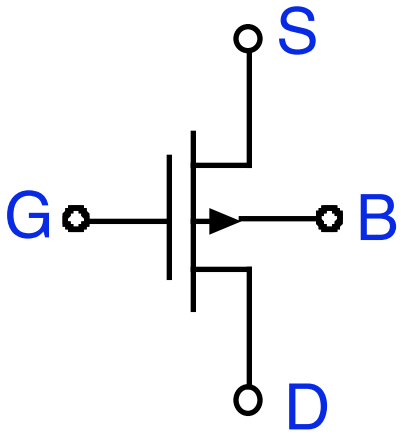


Enhancement mode

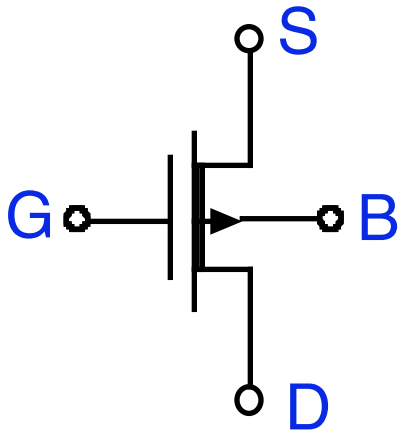


Depletion mode

n-channel



Enhancement mode



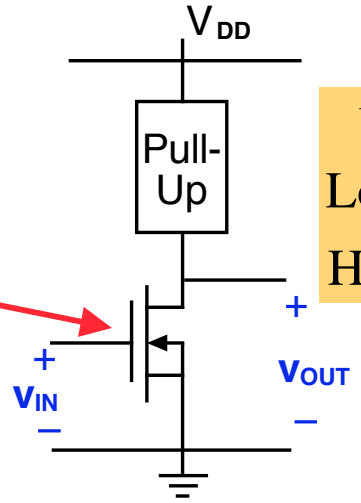
Depletion mode

p-channel (usual circuit orientation)

- **Building Blocks for Digital Circuits: inverters**

A basic inverter

Switch: on or off



v_{IN}	v_{OUT}
Lo (0)	Hi (1)
Hi (1)	Lo (0)

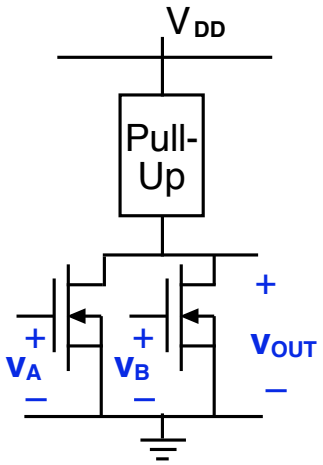
Performance metrics

- Transfer characteristic
- Logic levels
- Noise margins
- Power dissipation
- Switching speed
- Fan-in/Fan-out
- Manufacturability

Logic gates

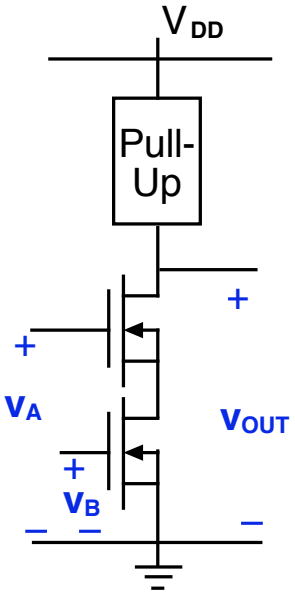
NOR:

v_A	v_B	v_{OUT}
0	0	1
0	1	0
1	0	0
1	1	0

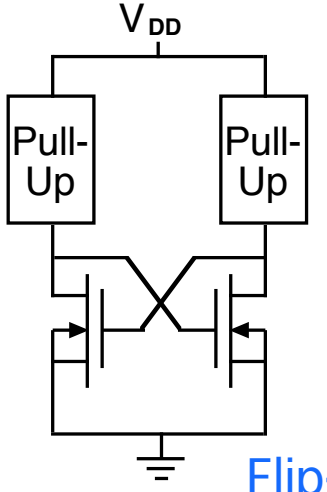


NAND:

v_A	v_B	v_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0



Memory cell



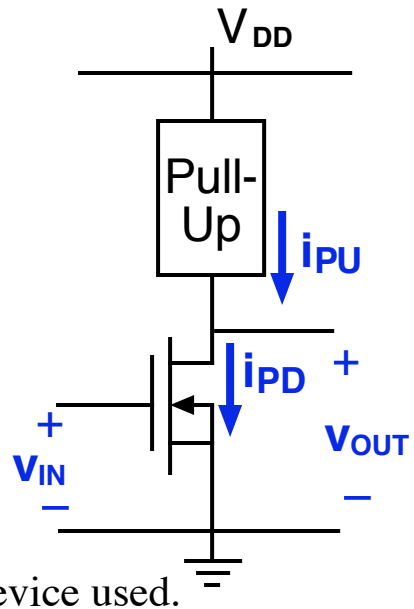
Flip-flop

Transfer characteristic

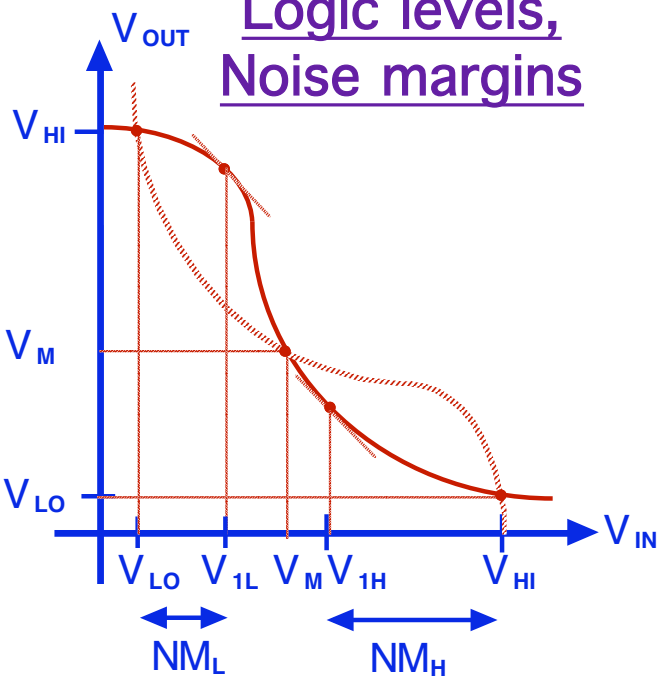
Node equation: $i_{PD} = i_{PU}$

$$i_{PD} = \begin{cases} 0 & \text{when} \quad v_{IN} < V_{T,PD} \\ K_{PD}\left(v_{IN} - V_{T,PD}\right)^2/2 & \text{when} \quad 0 < \left[v_{IN} - V_{T,PD}\right] < v_{OUT} \\ K_{PD}\left(v_{IN} - V_{T,PD} - v_{OUT}/2\right)v_{OUT} & \text{when} \quad 0 < v_{OUT} < \left[v_{IN} - V_{T,PD}\right] \end{cases}$$

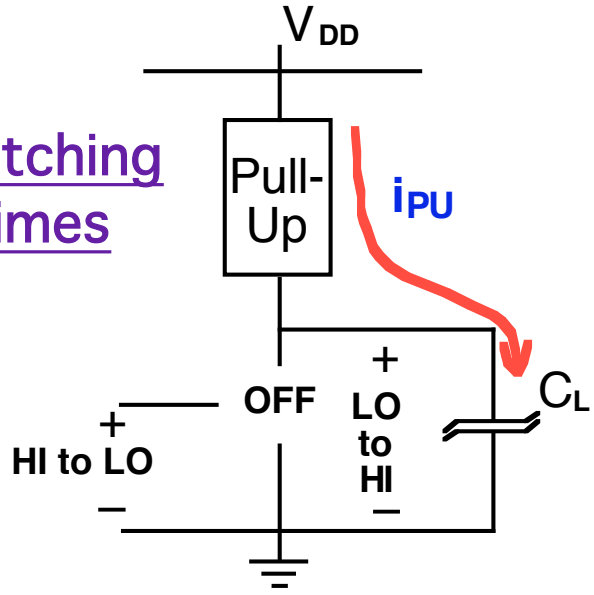
i_{PU} : Depends on the specific pull-up device used.



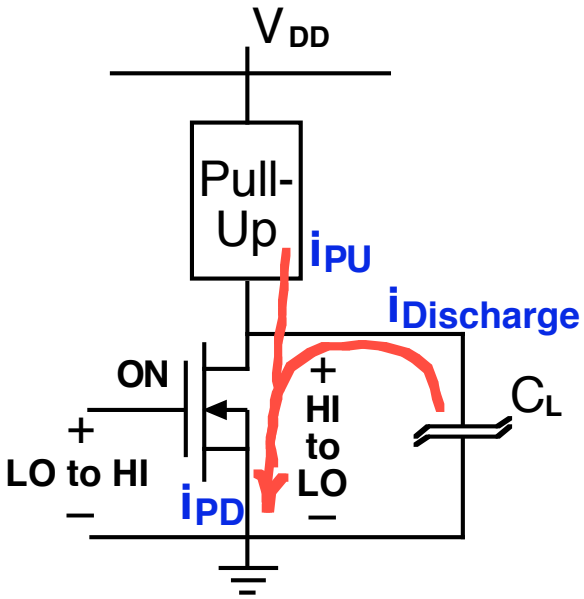
Logic levels, Noise margins



Switching times



Charging cycle: $i_{Charge} = i_{PU}$



Discharging cycle:

$i_{Discharge} = i_{PD} - i_{PU}$

Power

$$P_{Total} = P_{Static} + P_{Dynamic}$$

Static:

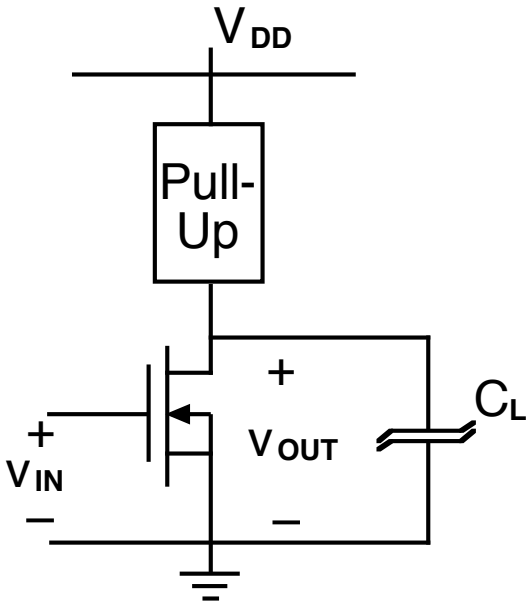
$$P_{Static} = \frac{1}{2} i_{PU,on} V_{DD}$$

Dynamic:

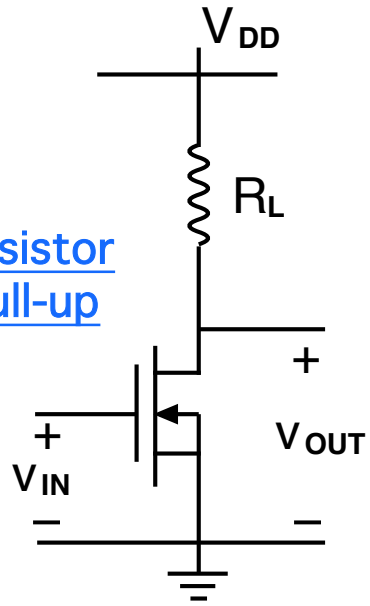
$$P_{Dynamic} = C_L V_{DD}^2 \cdot f$$

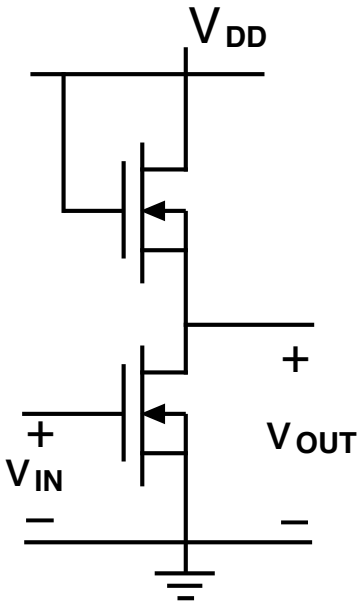
MOS inverters

Generic inverter



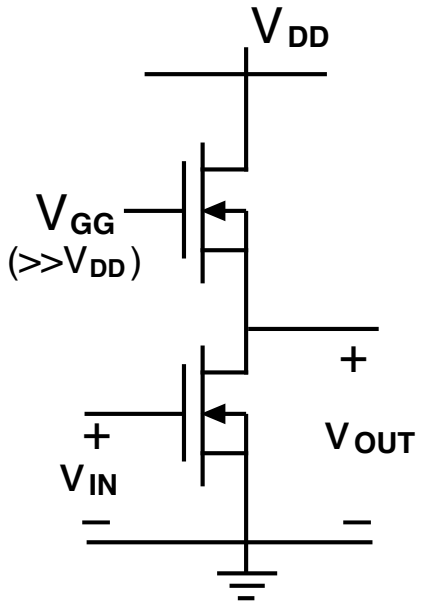
Resistor pull-up



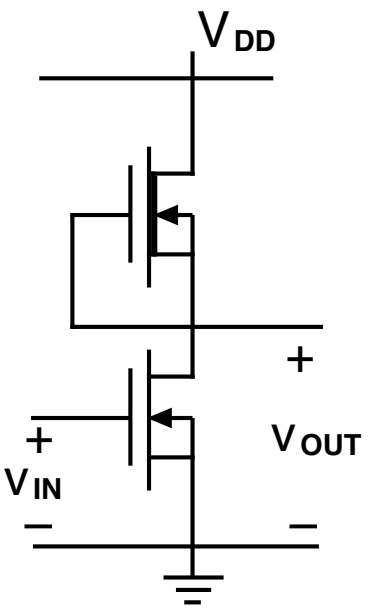


n-channel, e-mode pull-up

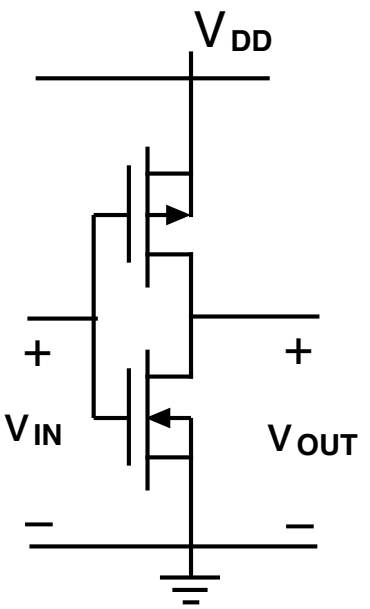
V_{DD} on gate



V_{GG} on gate

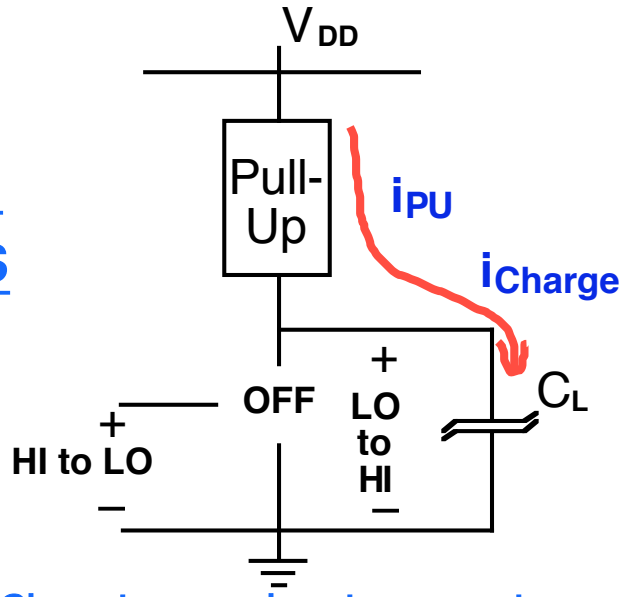


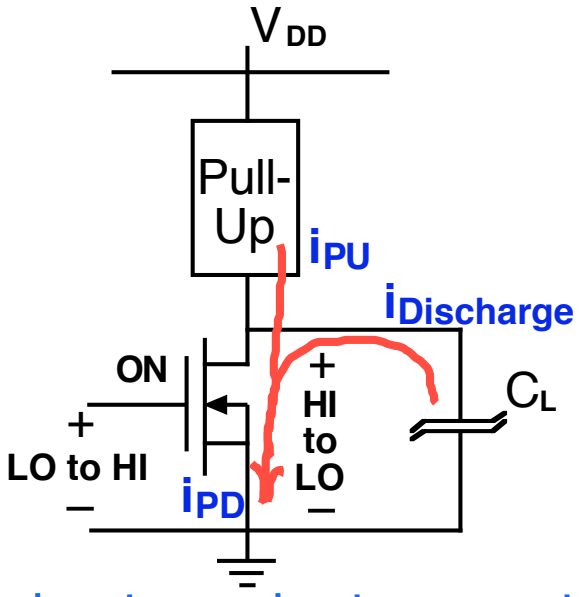
n-channel, d-mode pull-up



p-channel, e-mode pull-up (CMOS)

Switching transients

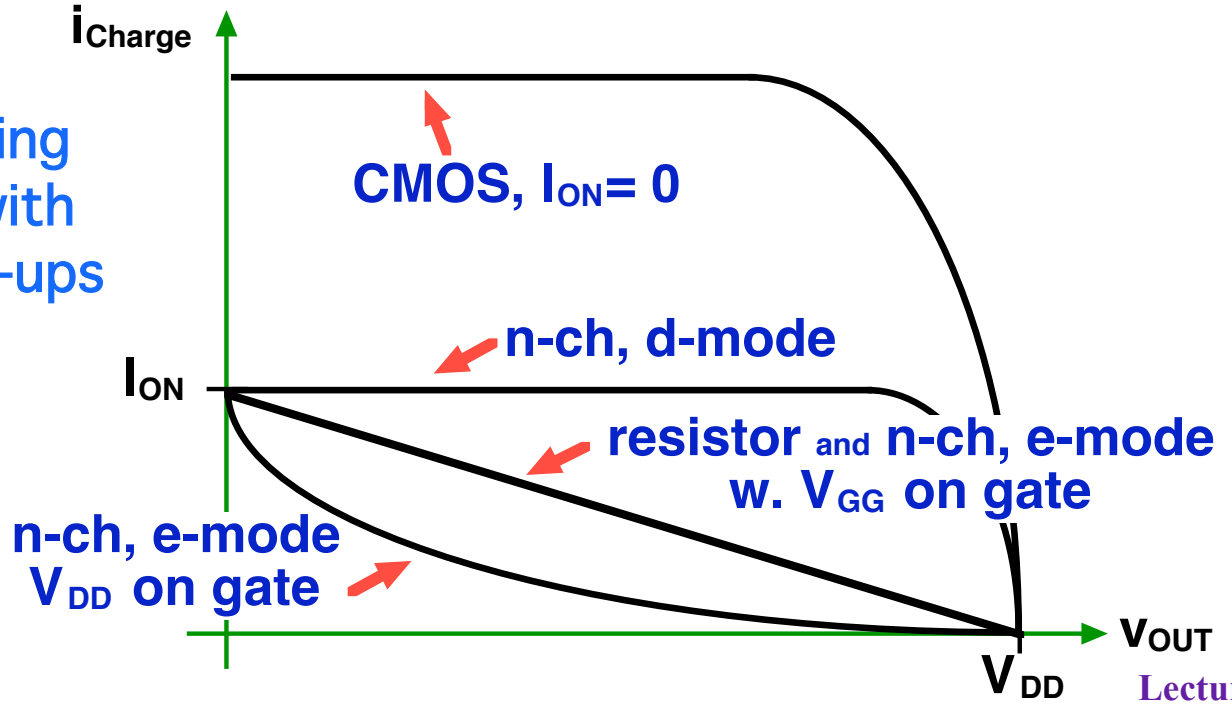




Charging cycle: $i_{Charge} = i_{PU}$

Discharging cycle: $i_{Discharge} = i_{PD} - i_{PU}$

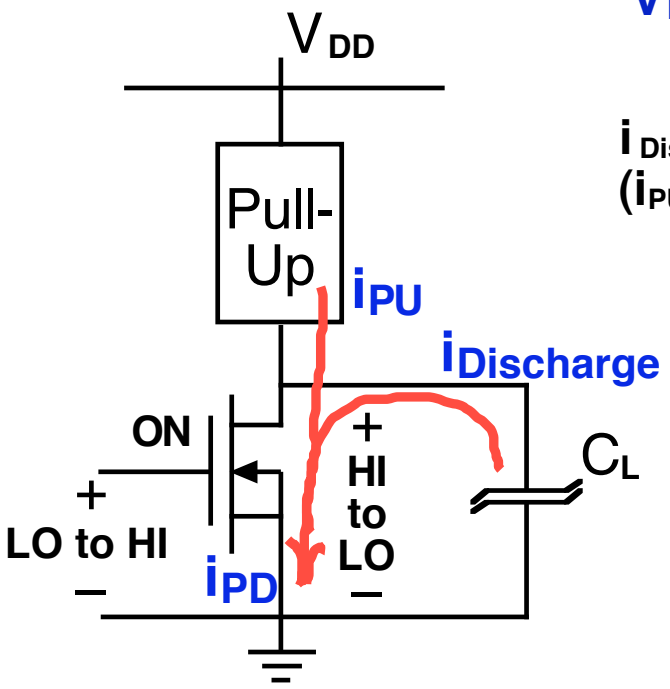
The charging currents with various pull-ups

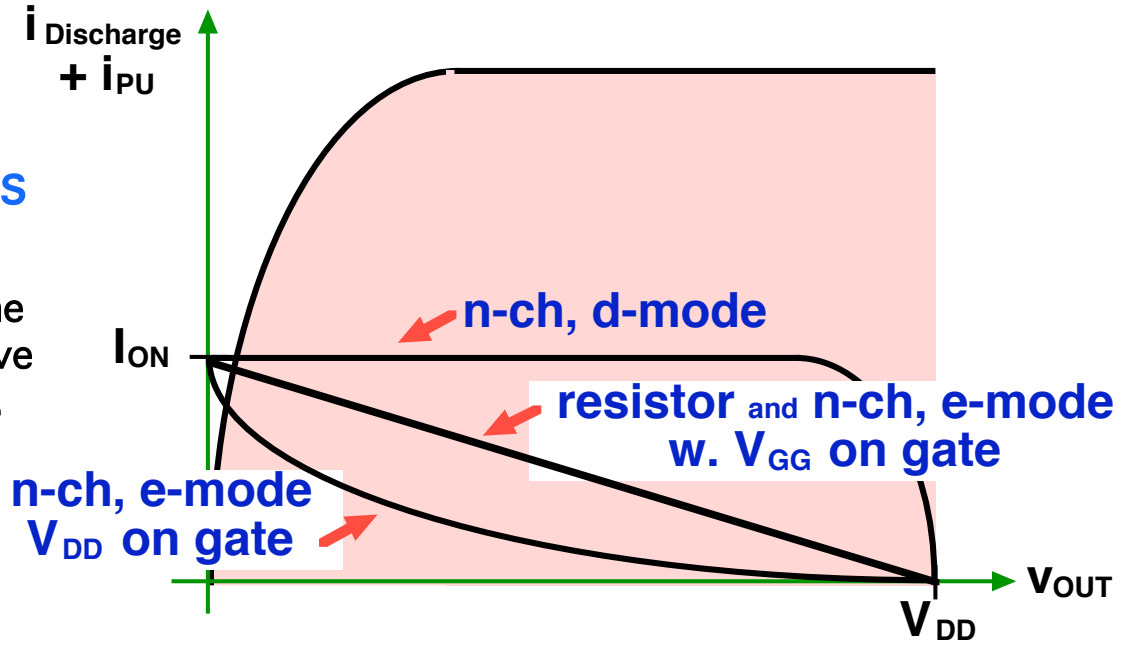


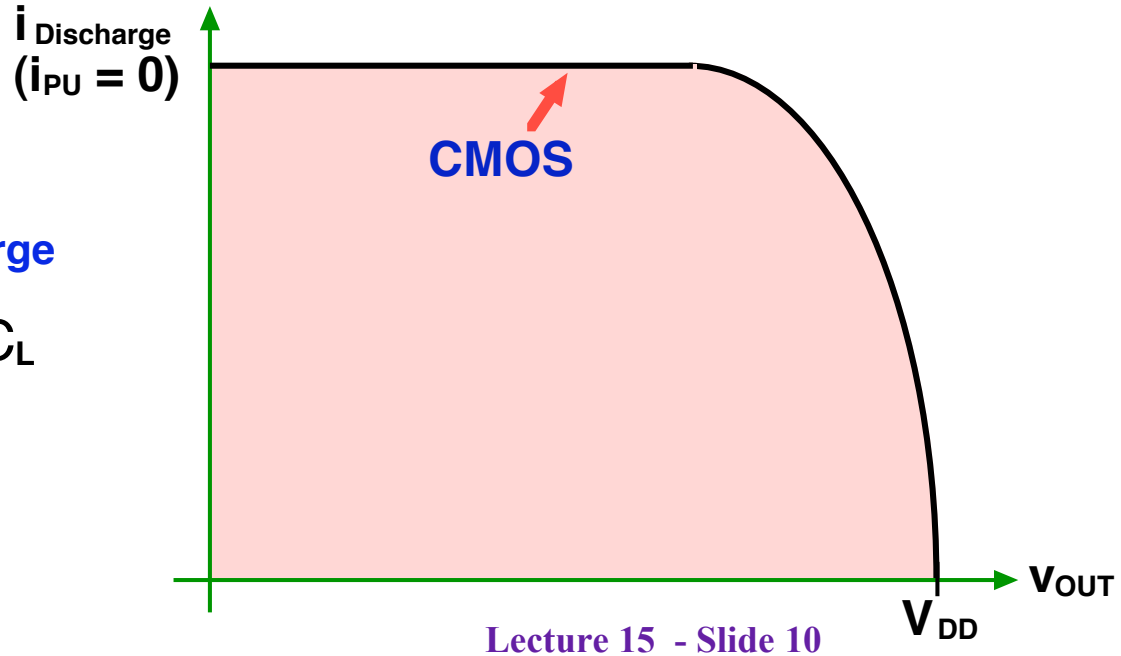
Switching transients

The discharging currents with various pull-ups

Note: The discharge current is the difference between the upper curve and the appropriate lower curve.

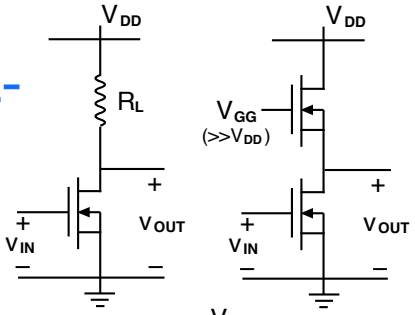


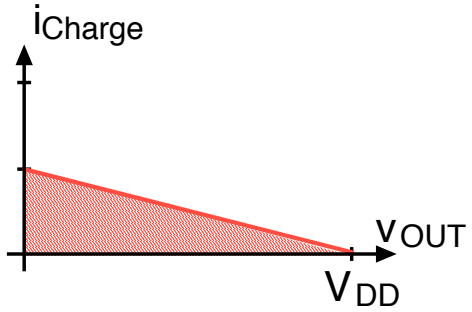


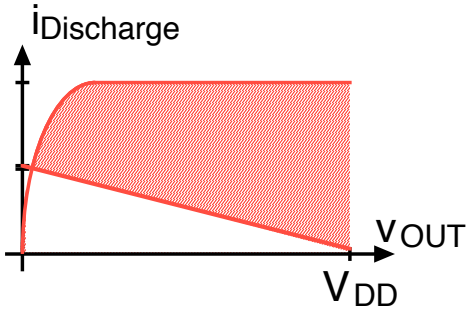


Switching transients: summary of charge/discharge currents

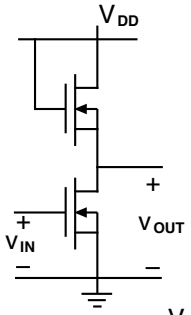
Resistor and E-mode pull-up (V_{GG} on gate)

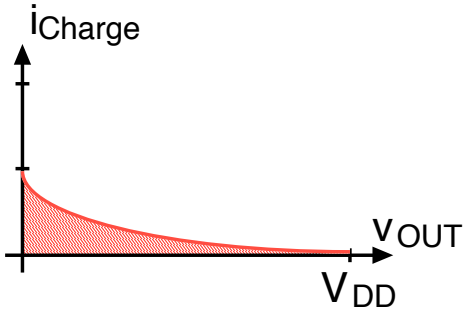


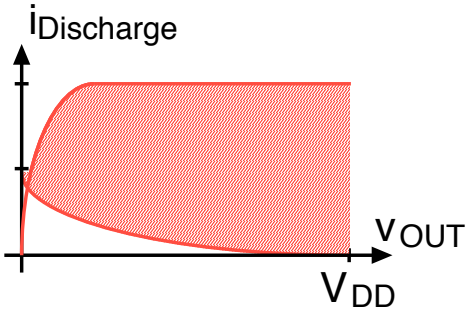




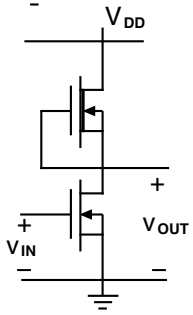
E-mode pull-up (V_{DD} on gate)

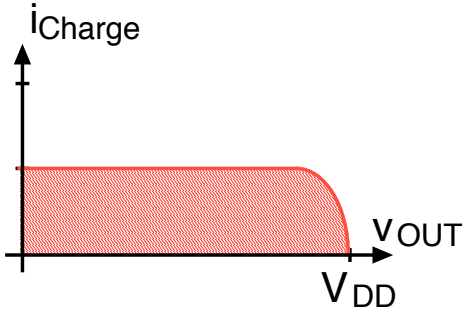


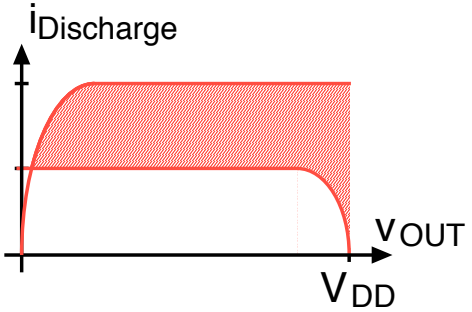




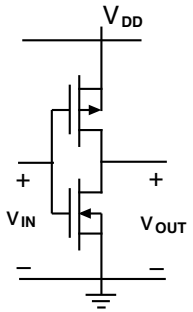
D-mode pull-up (called "n-MOS")

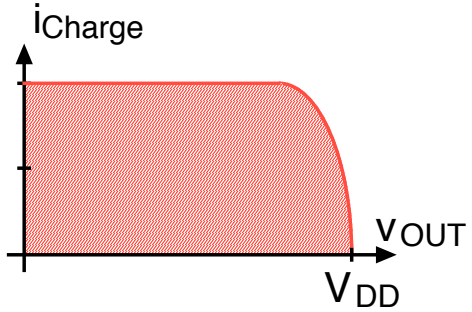


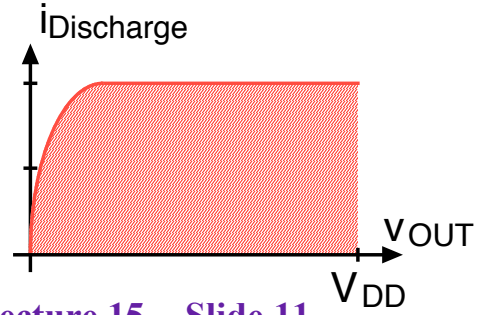




CMOS







Lecture 15 - Digital Circuits: Inverter Basics - Summary

- **Digital building blocks - inverters**
  - A generic inverter - Switch = pull-down device, Load = pull-up device
  - MOS inverter options - Pull-down: n-channel, e-mode (faster than p-channel)
    - Pull-up: 1. resistor; 2. n-channel, e-mode w. and w.o. gate bias;
      3. n-channel, d-mode; 4. p-channel, e-mode (CMOS)
- **Digtial inverter performance metrics**
  - Transfer characteristic
    - Logic levels: V_{HI}, V_{LO}
    - Noise margins: NM_{HI} (high), and NM_{LO} (low)
    - Design variables: choice of pull-up device
      pull-up and pull-down thresholds
      device sizes (absolute and relative)
  - Power dissipation: stand-by power and switching dissipation
  - Switching speed: capacitive load
    charge and discharge currents critical
  - Fan-out, fan-in: minimal issue in MOS; more so with BJT logic
  - Manufacturability: small, fast, low-power, reliable, and cheap
- **Comparing the MOS options**
  - And the winner is….CMOS