

XXVI. CUSTOM INTEGRATED CIRCUITS

Academic and Research Staff

Prof. J. Allen	Prof. R.L. Rivest	Dr. G.S. Miranker
Prof. L.A. Glasser	Prof. G.J. Sussman	Dr. H. Shrobe
Prof. P. Penfield, Jr.		J.T. Holloway

Graduate Students

A. LaPaugh
G.L. Steele

1. CONVERSION OF ALGORITHMS TO CUSTOM INTEGRATED CIRCUITS

U.S. Air Force – Office of Scientific Research (Grant AFOSR-78-3593)

Jonathan Allen, Lance A. Glasser, Paul Penfield, Jr., Ronald L. Rivest,
Gerald J. Sussman, Howard Shrobe, John T. Holloway

In this project, the objective is to determine a set of computational transformations which can convert an initial algorithmic specification to a final mask specification suitable for implementation of NMOS circuits. Techniques for manipulating architectures stated in hardware design languages along space/time trade-offs have been developed, and we are currently creating a language for expressing algorithmic constraints so that the performance of an algorithm can be separated from its competence. This form of algorithmic specification makes performance choices clear, and permits the exploration of architectural alternatives.

A variety of artwork analysis and synthesis programs have been written. These include a layout language, a PLA generator, a design rule checker, a logic simulator, and a router, as well as theoretical results for the optimal placement and routing of interconnect among rectangular modules. Using a high-performance LISP machine with a color monitor, a system for interactive editing of cells has been constructed, which automatically retains constraints due to design rules. These facilities have been used to design a number of interesting chips, including a basic LISP interpreter and an encryption coder.

