

1.0 Submicron Structures Technology and Research

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1.1 Submicron Structures Laboratory

The Submicron Structures Laboratory at MIT develops techniques for fabricating surface structures with linewidths in the range from nanometers to micrometers, and uses these structures in a variety of research projects. These projects of the laboratory, which are described briefly below, fall into four major categories: development of submicron and nanometer fabrication technology; deep-submicron electronics and quantum-effect electronics; crystalline films on amorphous substrates; and periodic structures for x-ray optics and spectroscopy.

1.2 Microfabrication at Linewidths of 100nm and Below

Joint Services Electronics Program (Contract DAAL03-86-K-0002)
National Science Foundation (Grant ECS 87-09806)

Erik H. Anderson, James M. Carter, William Chu, Hui M. Quek, Irving Plotnik, Mark L. Schattenburg, Anthony T. Yen, Henry I. Smith

A variety of techniques for fabricating structures with characteristic dimensions of 0.1 μm (100 nm) and below are investigated. These include: x-ray nanolithography, holographic lithography, achromatic holographic lithography, electron-beam lithography, reactive-ion etching, electroplating and liftoff. Development of such techniques is essential if we are to explore the rich field of research applications in the deep-submicron and nanometer domains. X-ray nanolithography is of special interest

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because it promises to provide high throughput and broad process latitude at linewidths of $0.1 \mu\text{m}$ and below, something that cannot be achieved with scanning- electron-beam lithography. We are developing a new generation of x-ray masks made from inorganic membranes (Si, Si_3N_4 , and SiC) and are investigating means for precisely controlling mask-wafer gap, and achieving nanometer alignment. Phase shifting and transform x-ray masks (i.e., in-line x-ray holography) may permit us to achieve sub-50 nm linewidths at finite gaps. In this year we showed that if the absorber introduces a pi-phase shift in addition to about 10db attenuation the intensity profile at the edge of a feature is steeper than with conventional masks. This is because low levels of radiation that diffract into the shadow region behind an absorber are partially cancelled by the phase shifted radiation transmitted by the absorber. This enables either an increase in the allowable mask-sample gap at a given linewidth or improves the process latitude at a given gap.

A new tri-level technique for making, by electron-beam lithography, x-ray masks with linewidths of 50 nm was developed in collaboration with IBM. This technique allows us to fabricate x-ray masks with patterns of arbitrary geometry and replicate them in our own laboratory, as illustrated in figure 1.1.

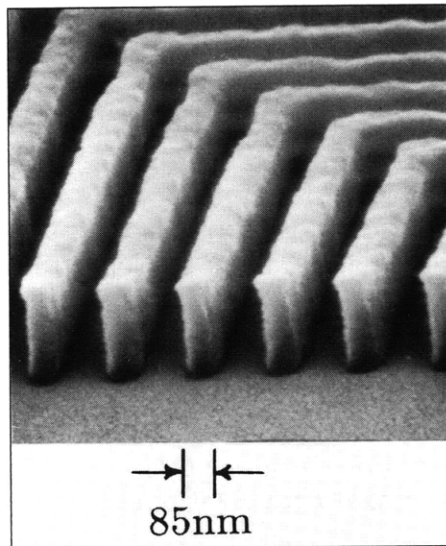


Figure 1.1 X-ray nanolithographic replication of 85 nm-linewidth patterns created on the x-ray mask by scanning e-beam lithography.

Techniques for making x-ray masks from crystallographic templates are being improved. We hope to achieve x-ray replication in PMMA with nanometer scale line-edge smoothness.

An achromatic holographic lithography configuration was developed which allows us to produce periodic structures with linewidths ~ 50 nm over large areas, using deep-UV sources that have poor temporal and spatial coherence, such as the ArF laser. We have also developed a means of feedback stabilizing the fringe pattern against vibrations and other disturbances. Although holographic techniques can be used to

prepare experimental samples, there are important advantages to using them only for preparing x-ray masks. These masks are then replicated using x-ray nanolithography. With C_K and Cu_L x-ray lithography high-aspect-ratio (almost 8:1) structures with linewidths less than 50 nm have been produced in PMMA.

1.3 Improved Mask Technology for X-Ray Lithography

Semiconductor Research Corporation (Contract 87-SP-080)

Yao-C. Ku, Irving Plotnik, Henry I. Smith

In order to utilize x-ray lithography in the fabrication of submicron integrated electronics, distortion in the x-ray mask must be eliminated. Distortion can arise from stress in the absorber, which is usually gold or tungsten. Tungsten is preferred because it is a closer match in thermal expansion to Si, and other materials used as mask membranes. However, W is usually under high stress when deposited by evaporation or sputtering. We have demonstrated that tensile stress in W can be compensated by ion implantation. Strain-induced deflection of Si_3N_4 or Si membranes is measured in a Linnik interferometer. Membrane deflection due to stresses $\sim 7 \times 10^9$ dynes/cm² are reduced to zero by implantation of 1×10^{16} Si atoms/cm² at 25 keV. Stress compensation occurs because the implantation into the top 10nm of the W film causes a compressive stress which in turn produces a torque to compensate the torque produced by the native tensile stress. In the future we will develop a capacitive method of measuring membrane deflection so that stress correction can be done in situ, during film deposition, or in real time during ion implantation.

1.4 Theoretical Analysis of the Lithography Process

Semiconductor Research Corporation (Contract 87-SP-080)

Henry I. Smith

In an earlier theoretical analysis of lithography we studied the effects of statistical fluctuations on linewidth control, and compared the pixel transfer rates of the various lithographic techniques. This analysis has been expanded to include the effects of nonuniform illumination and other non-ideal factors. We have also derived a method for quantifying process-latitude in lithography, a critically important figure-of-merit in manufacturing. The normalized-process-latitude-parameter was evaluated, as a function of minimum linewidth, for several UV and deep UV projection system, and for an x-ray system based on a laser-produced plasma source. As expected, the x-ray system showed a significantly larger process latitude in the important linewidth range between 0.1 and 1 μ m.

1.5 Studies of Electronic Conduction in One-Dimensional Semiconductor Devices

Joint Services Electronics Program (Contract DAAL03-86-K-0002)
National Science Foundation (Grant ECS 85-03443)

S.B. Field, Jerome C. Licini, Udi Meirav, Samuel L. Park, John Scott-Thomas, Dimitri A. Antoniadis, Marc A. Kastner, Henry I. Smith

At low temperatures, Si inversion layers of two-dimensional-electron-gas, with widths less than 100 nm in Si, and less than 1 μm in GaAs, become quasi-one-dimensional. This happens when inelastic scattering is sufficiently reduced that the electronic wave functions have phase coherence over distances larger than the device width.

Three techniques are being employed to fabricate one-dimensional devices. In the first, field-effect transistors are fabricated in Si with widths as narrow as 50 nm. The narrow gate of these MOSFET's is created by glancing-angle evaporation of tungsten onto a 50-nm high step etched in a 100-nm thick oxide on a Si (100) surface. In a second technique, the inversion layer is created under a narrow slot in a wide metal gate by applying a potential to an upper metal gate separated from the first by a layer of SiO_2 . The lower gate with the narrow slot is fabricated using x-ray lithography and lift-off. To create one-dimensional devices in GaAs we are exploring the possibility of using p-implants to confine the two-dimensional electron gas created by modulation doping or by a gate.

Recently, using devices fabricated by the first and second techniques, a new collective state of the electron gas in high magnetic fields was discovered. Initial experiments were done on quasi-one dimensional Si inversion layers, about 100 nm wide and 7 μm long. At 100 mK and low magnetic fields the usual small negative magnetoresistance, and the universal conductance fluctuations associated with localization in one dimension, were observed. In a larger magnetic field of about 4T, however, there is a magnetic-field-induced transition to a new state, with conductance almost ten times larger than in zero field. This giant negative magnetoresistance is astonishing. The conductance per square of the Q1D device, once the new state is formed, is ten times larger than its 2D counterpart. Figure 1.2 shows that in high magnetic fields the conductance rises sharply at certain gate voltages and has plateaus in between. This is reminiscent of the quantum-Hall effect, and it is likely that the high-field state in the Q1D inversion layer is related to the quantum-Hall state in the 2D electron gas. However, the pattern of the plateaus and the temperature dependence of the structure in the conductance-versus-gate voltage provides strong evidence that new many-body effects are important.

There is no model that predicts these phenomena in detail. However, it has been suggested that 1D confinement of the 2D gas might lead to a charge or spin density wave instability when the width is comparable to, but somewhat larger than, the magnetic length (i.e., the radius of the Landau orbit). Such instabilities lead to a gap which remains at the Fermi energy over a wider range of filling factors than for the quantum-Hall state. The plateaus would then reflect plateaus in p_{xy} because p_{xx} would be zero. Experiments are underway to explore how the properties of the high-field state depend on the channel width and mobility. The split, dual-gate configuration produces an inversion layer ~ 30 nm wide. The high-field state has been observed in this structure as well, but at much higher magnetic fields, as expected.

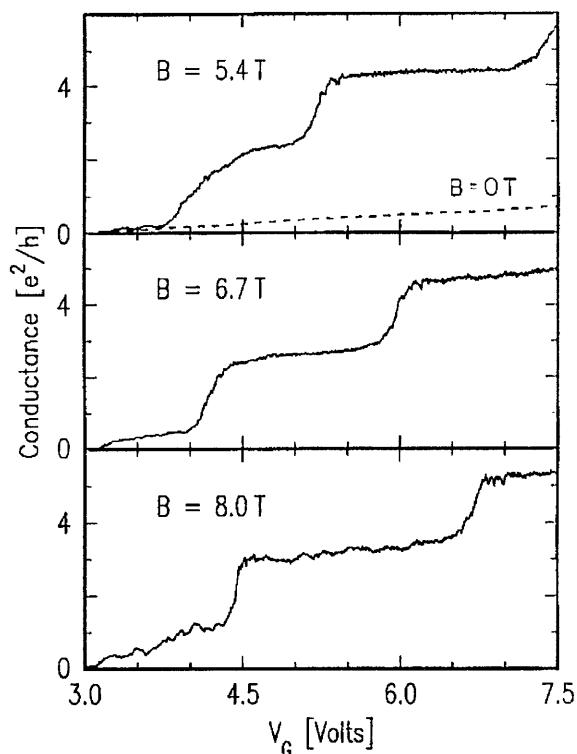


Figure 1.2 Conductance as a function of carrier density (V_G) at three magnetic fields and $T=100$ mK. Note that, although the values are not integral multiples of e^2/h , the largest steps have $2e^2/h$. The risers shift linearly in magnetic field. The dashed curve in the top panel is the conductance at $B=0$.

1.6 Surface Superlattice Formation in Silicon Inversion Layers using $200 \mu\text{m}$ Period Grating-Gate Field-Effect Transistors

*Joint Services Electronics Program (Contract DAAL03-86-K-0002)
U.S. Air Force - Office of Scientific Research (Grant AFOSR 85-0376)*

Phillip F. Bagwell, Anthony T. Yen, Dimitri A. Antoniadis, Marc A. Kastner, Terry P. Orlando, Henry I. Smith

We have been investigating electronic conduction and distinctly quantum-mechanical effects in a surface superlattice (SSL) device. The device is a Si MOSFET with a dual stacked gate configuration. The lower gate is a tungsten grating of 200 nm period (100 nm nominal linewidth), and the upper gate is a uniform metal pad separated from the grating by 200 nm of deposited SiO_2 . We call these devices grating-gate-field-effect transistors (GGFET's). The grating gate is fabricated using x-ray nanolithography and grating contact pads are made with deep-UV lithography. Drain-to-source current in the SSL device runs perpendicular to the grating wires. A distinguishing feature of our GGFET's is that the strength of the periodic modulation in the channel, and the inversion-layer electron density, can be independently controlled by external voltage supplies. At low temperatures we observe a modulation of the inver-

sion layer conductance with gate voltage that is about one hundred times larger than the universal fluctuations predicted by the theory of Lee and Stone. This is consistent with electron back diffraction from the imposed periodic potential.

The first generation of devices had low fabrication yields due to poor gate contacts, adhesion problems, metallization problems and shorts to the substrate. Devices also had low mobility due to radiation damage. These problems have been resolved and second generation devices have been fabricated and tested. The first set suffered from unfavorable line-to-space ratio in the grating gate, making it impossible for us to invert regions in between grating lines. A third set of devices is being fabricated with proper line-to-space ratio.

We have also developed a semiclassical algorithm to calculate the effects of free electron motion perpendicular to the superlattice, elastic impurity scattering, inelastic scattering between electrons and by phonons, and finite temperature on the conductance of these devices. The observability criterion arising from this model is that energy averaging $\sim \kappa t$ from finite temperature and $\sim h/\tau$ from a random impurity configuration must be smaller than the energy gaps at each mini-Brillouin zone boundary. Elastic scattering, by itself, does not lead to energy averaging but, coupled with inelastic scattering, sets the scale of the energy averaging. If no inelastic scattering is present in the device, elastic scattering leads to fluctuations in conductance of size e^2/h . In this regime, the observability criterion is that we must impose an average conductance modulation larger than e^2/h . We are currently implementing this semi-classical algorithm to calculate the conductance of GaAs superlattice devices, described in the next section.

1.7 Study of Surface Superlattice Formation in GaAs/GaAlAs Modulation Doped Field-Effect Transistors

U.S. Air Force - Office of Scientific Research (Grant AFOSR 85-0376)

William Chu, Khalid Ismail, Dimitri A. Antoniadis, Marc A. Kastner, Terry P. Orlando, Henry I. Smith

We have used the modulation-doped field-effect transistor (MODFET) as a test vehicle for studying electron back diffraction in a GaAs/GaAlAs material system. In a regular MODFET the current transport is modulated by a continuous gate positioned between source and drain. In our device, the grating-gate MODFET, shown in figure 1.3, we have combined x-ray nanolithography and liftoff to achieve a $0.2 \mu\text{m}$ -period grating-gate (100nm linewidth). By biasing this gate we can introduce a periodic modulation of the charge concentration in the 2D-gas residing at the GaAlAs/GaAs interface. As a result an electron traveling from source to drain sees a periodic array of barriers. The height of these barriers and the electron concentration can be altered by changing the bias condition on the gate. Theory predicts that such a structure would result in energy gaps opening up in the energy band. This should be manifest as a drop in conductance whenever the Fermi energy is swept across any of those gaps. In our first batch of working devices current we observed plateaus while sweeping the grating-gate voltage. This effect was repeatable from one device to another. In com-

parison, regular MODFET's, which were fabricated on the same sample, had a smooth current increase. This gives evidence that the observed plateaus are a manifestation of electron back diffraction caused by the periodic modulation. Differentiating our results, the effect is more pronounced, as shown in figure 1.4, and had distinct features which were quadratically spaced, as expected for a parabolic energy band.

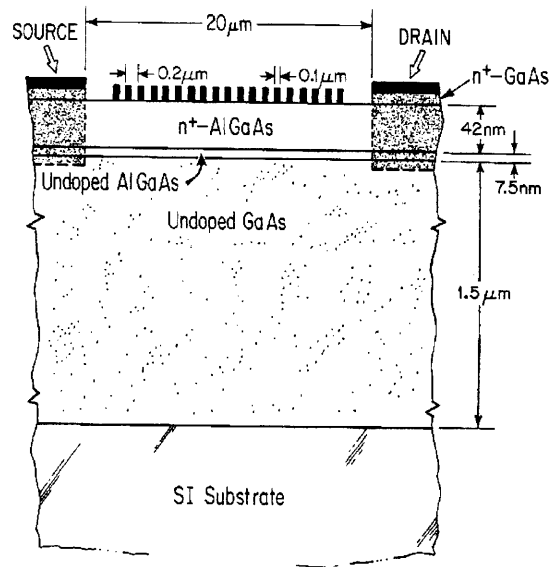


Figure 1.3 Schematic cross section of a grating-gate MODFET device. The channel width and length are both $20 \mu\text{m}$. An undoped GaAs/GaAlAs superlattice (not shown) was used to trap impurities diffusing out of the substrate.

Because this sample had a mobility of $250,000 \text{ cm}^2/\text{V sec}$ at 4 K the calculated mean free path of electrons is $\sim 1.2 \mu\text{m}$. We believe that due to the high material purity, universal conductance fluctuations have been suppressed, since in this regime both the elastic and the inelastic scattering times are comparable. Preliminary magnetoresistance measurements confirm this idea.

We are planning to fabricate devices with grid-gates (figure 1.5) to confine the electron motion in two dimensions. We also intend to exploit our lithographic capabilities to push our grating-gate periodicity down by a factor of two to 100nm period (50nm linewidth). Under those conditions the superlattice effects should become more pronounced at 4 K, and might also become observable at much higher temperatures.

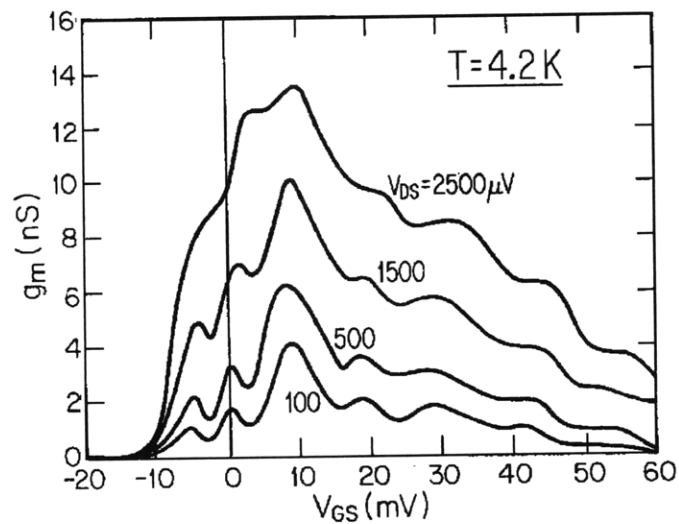


Figure 1.4 Plots of transconductance, g_m , versus gate-to-source voltage, V_{GS} , for several values of the source-drain voltage, V_{DS} .

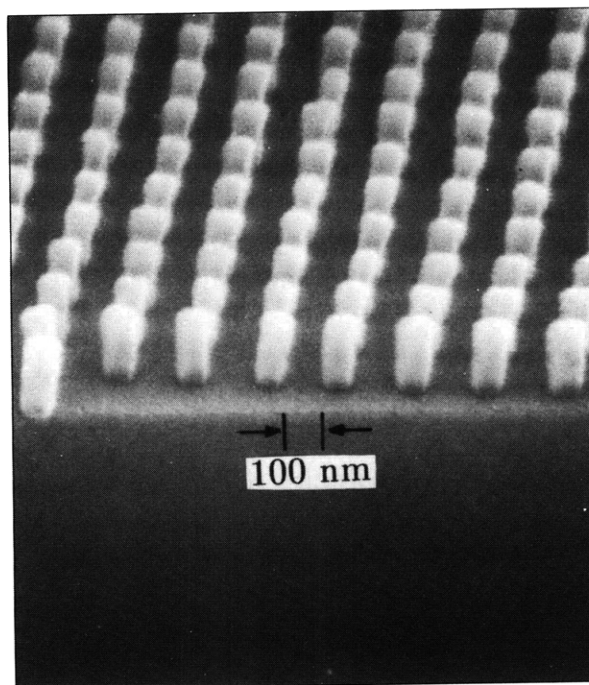


Figure 1.5 X-ray lithographic replication of a grid pattern in PMMA.

1.8 Investigation of One-Dimensional Conductivity in Multiple, Parallel Inversion Lines

*Joint Services Electronics Program (Contract DAAL03-86-K-0002)
U.S. Air Force - Office of Scientific Research (Grant AFOSR 85-0376)*

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In order to study one-dimensional conductivity without the statistical fluctuations normally associated with small systems, field-effect devices have been fabricated which use a submicron-period grating-gate structure to produce 250 narrow inversion lines in parallel. The device is fabricated on the same substrate and by the same procedures as the Si GGFET's discussed in section 1.6. In fact, the major difference is that the grating lines are now parallel to the electron flow. Others have reported a variety of devices which produce a single narrow "micro-channel," but the expected quasi-one-dimensional density of states has generally been obscured by large random fluctuations inherent in small systems. Here, the parallel measurement of many such one-dimensional conductors results in an improved signal-to-noise ratio in the density-of-states sampling. This is due to the incoherence of random fluctuations in different micro-channels in the same device. Proper independent biasing of the two gate electrodes results in the formation of a parallel array of 50 to 100-nm-wide lines of inversion charge connecting the source and drain. Transconductance measurements demonstrate a weak, regular modulation that is consistent with the expected quasi-one-dimensional density-of-state. These experiments are being repeated with a new generation of devices.

We understand the conductance modulation in a quasi-one-dimensional wire as arising from scattering between subbands. As the Fermi level passes into a new subband, we expect a large decrease in conductance. Inelastic scattering at finite temperature will tend to destroy this effect. The same semi-classical modeling techniques used for the surface-superlattice devices have been used to model conductance in single-wire, and multiple wire arrays. We have developed an analytic formula showing that conductance in the wire array closely approximates a quasi-1D wire for a Fermi energy small compared to the scale of the confining potential.

1.9 Study of Electron Transport in MOSFET's in Si with Deep-Submicron Channel Lengths

Joint Services Electronics Program (Contract DAAL03-86-K-0002)

Ghavam Shahidi, Dimitri A. Antoniadis, Henry I. Smith

Electron conduction in sub-100-nm channel length, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET's) in Si is investigated. The devices were fabricated with a combination of x-ray nanolithography and optical projection lithography. The x-ray mask, which defined the minimum lithographic features, was fabricated with conventional photolithography, anisotropic etching of a Si template, and oblique shadowing of the absorber. The gate oxide thickness for these devices was typically

7.5 nm, but in some cases as thin as 2.5 nm. Electron velocity overshoot, to values exceeding bulk saturation values of 10^7 cm sec⁻¹ at room temperature and 1.5×10^7 cm sec⁻¹ at liquid nitrogen temperature, was observed. A non-uniform channel doping was employed to achieve high electron mobility in the inversion layer, while at the same time preventing punchthrough. The doping in the inversion layer is about 10^{16} cm⁻³. Control of punchthrough is achieved by a boron implant in the channel of 4×10^{12} cm⁻² at 50 keV. After oxidation at 900°C for 10 min in O₂, to grow the gate oxide, the boron profile remains abrupt with a peak concentration of about 2.2×10^{17} cm⁻² at 0.19 μm depth. The low-field mobility was estimated from long channel MOSFET's on the same substrate to be about 450 cm²/Vsec.

In addition to velocity overshoot we have also investigated hot electron effects, specifically channel-hot-electron-generated substrate currents. For channel lengths in the range $0.15 \mu\text{m} < L < 0.5 \mu\text{m}$ the normalized substrate current at constant ($V_{\text{DS}} - V_{\text{DSAT}}$) increases with decreasing channel length, presumably because of an increase in the maximum field near the drain. However, as the channel length is decreased below 0.15 μm, a decrease of the normalized substrate current is observed. We believe that this effect accompanies the onset of electron velocity overshoot over a large portion of the channel, and is due to either a decrease of carrier temperature or a relative decrease of the carrier population in the channel, or both.

We have also used indium as an alternative channel implant. Because of higher atomic number one can achieve lower surface doping, and bring the implant peak very close to the surface, thus resulting in higher threshold voltages and a reduction in short-channel effects. Short-channel MOSFET's with indium as the channel implant and gate oxide thickness of 2.5 nm gave transconductances of 720 mS/mm, and reduced short-channel and hot-electron effects. Further work in characterization of devices with indium implants is continuing.

1.10 Crystalline Films on Amorphous Substrates

National Science Foundation (Grant ECS 85-06565)

U.S. Air Force - Office of Scientific Research (Grant AFOSR 85-0154)

Sergio Ajuria, Harry A. Atwater, Jerrold A. Floro, Hui Meng Quek, Henry I. Smith, Carl V. Thompson

We are investigating methods for producing crystalline films on amorphous substrates. This is motivated by the belief that the integration of future electronic and electrooptical systems will be facilitated by an ability to combine, on the same substrate, a broad range of materials (Si, III-V's, piezoelectrics, light guides, etc.). Zone melting recrystallization (ZMR) of Si on amorphous SiO₂ has been highly successful, but device-quality films are obtained only at the expense of high processing temperatures since the Si must be melted. Other materials, such as Ge and InSb, have also been successfully zone melted. ZMR has been an important testing ground for materials combination, and for a number of novel concepts based on the use of lithography to control in-plane orientation and the location of defects (so-called defect entainment).

The most promising approach in the long-term to crystalline films on amorphous substrates is, in our view, based on surface-energy-driven secondary grain growth

(SEDSGG). In this approach, no melting or phase change occurs. Instead, we take advantage of the very large surface energies inherent in ultrathin (20 nm) films to drive the growth of large secondary grains having specific crystallographic planes parallel to the surface. This phenomenon has been demonstrated, as has the use of very fine gratings (~100 nm linewidths) to control the in-plane orientation (i.e., graphoepitaxy in combination with SEDSGG). Currently, research is focused on basic studies of grain growth and coarsening phenomena in ultra-thin films of model materials such as Ge, Si, Ag and Au. We also investigate means of promoting grain growth at temperatures many hundreds of degrees below the melting point. These include ion-bombardment-enhanced grain growth (IBEGG), laser illumination, and use of selective dopants. Theoretical models for surface-energy-driven secondary grain growth were developed and have, for the most part, been confirmed by experiments on Si, Ge and Au films. If our basic studies prove fruitful we may be able to develop a low temperature method, applicable to all crystalline film materials, for producing device-quality films on amorphous substrates. By means of lithography, defects in the films, such as dislocations and stacking faults, would be localized at predetermined positions, out of the way of devices.

1.11 Ion-Bombardment-Enhanced Grain Growth in Thin Films

National Science Foundation (Grant ECS 85-06565)

U.S. Air Force - Office of Scientific Research (Grant AFOSR 85-0154)

Harry A. Atwater, Jerrold A. Floro, Henry I. Smith, Carl V. Thompson

Grain growth in polycrystalline films can lead to formation of low-defect-density or single-crystal film. We have been investigating the effect of ion bombardment on the motion of grain boundaries in normal and secondary grain growth, so called ion-beam-enhanced grain growth (IBEGG). The scientific objective is to better understand how grain boundaries move. The technological objective is to develop a low temperature process for obtaining crystalline films on amorphous substrates. IBEGG has been studied experimentally in thin (i.e., < 1000 Å) Ge, Au and Si films. Ion beams in the 40 - 100 keV range have been employed, resulting in an ion damage profile whose peak is approximately in the center of the thin film. Concurrent with ion bombardment, samples were annealed at 500 and 1050°C for Ge and Si, and at room temperature for Au. The temperature is chosen so that ion damage is annealed dynamically. IBEGG has been characterized by varying the ion dose, ion energy, ion flux, ion species, temperature, and thin film deposition conditions. The effect of these parameters on grain size and microstructure has been analyzed both qualitatively and quantitatively using transmission electron microscopy (TEM). A transition state model has been developed to describe the motion of grain boundaries during ion bombardment. The model accounts for the dependence of IBEGG on experimental parameters. An atomistic picture of the jump rate at grain boundaries during IBEGG has been proposed. Monte-Carlo simulation of ion range and defect production was performed using the TRIM code and a modified Kinchin Pease formula. The calculated defect yield per incident ion was correlated with enhanced grain growth, and used to estimate the number of atomic jumps at the grain boundary per defect generated at the boundary for a given driving force, a quantity which is approximately constant for a given film material. The IBEGG and thermal growth rates have been related to their respective point defect populations.

That is, grain growth rate appears to depend only on the concentration of vacancies and interstitials, irrespective of whether they are created thermally or by ion bombardment.

Recently, we have extended the study of IBEGG to the low energy range (≤ 1 keV). Experiments are done in an ultrahigh vacuum system so that material lost through sputtering can be replaced by deposition from a separate source.

1.12 Epitaxy via Surface-Energy-Driven Grain Growth

U.S. Air Force - Office of Scientific Research (Grant AFOSR 85-0154)

Jerrold A. Floro, Joyce E. Palmer, Carl V. Thompson, Henry I. Smith

Grain growth in polycrystalline films on single-crystal substrates can lead to formation of low-defect-density or single-crystal films. This process is expected to minimize the production of extended defects in large misfit systems, a problem difficult to avoid in conventional heteroepitaxy. We are investigating surface-energy-driven secondary grain growth in semiconductor and metal films on single crystal substrates. We are also further developing the theory of epitaxy by surface-energy-driven secondary grain growth, including effects due to grain boundary motion and due to coarsening via surface diffusion.

1.13 Submicrometer-Period Gold Transmission Gratings for X-Ray Spectroscopy

Lawrence Livermore National Laboratory (Subcontract 2069209)

Erik H. Anderson, Mark L. Schattenburg, Henry I. Smith

Gold transmission gratings with periods of 0.1 to 0.2 μm , and thickness ranging from 0.5 to 1 μm are fabricated using x-ray lithography and electroplating. The x-ray masks are made either with holographic lithography or scanning-electron-beam lithography. Transmission gratings are either supported on polyimide membranes or are made self-supporting by the addition of crossing struts. They are used for spectroscopy of the x-ray emission from plasmas produced by high-power lasers. Gratings fabricated in our lab by these techniques are used in key diagnostic instruments associated with the soft x-ray laser research at Lawrence Livermore National Laboratory.

1.14 High-Dispersion, High-Efficiency Transmission Gratings for Astrophysical X-Ray Spectroscopy

National Aeronautics and Space Administration (Grant NGL22-009-683)

Erik H. Anderson, Mark L. Schattenburg, Claude R. Canizares, Henry I. Smith

Gold gratings with spatial periods of 0.1 - 1.0 μm make excellent dispersers for high resolution x-ray spectroscopy of astrophysical sources in the 100 eV to 10 KeV band.

These gratings are planned for use in the Advanced X-ray Astrophysics Facility (AXAF) which will be launched in the mid 1990's. In the region above 3 KeV, the requirements of high dispersion and high efficiency dictate the use of the finest period gratings with aspect ratios approaching 10:1. To achieve this we first expose a grating pattern in 1.5 μm -thick PMMA over a gold plating base using x-ray nanolithography. To date, we have worked with gratings having periods of 0.3 or 0.2 μm (linewidth 0.15 - 0.1 μm). Gold is then electroplated into the spaces of the PMMA to a thickness of 1 μm . Flight prototype gratings have been fabricated and are undergoing space worthiness tests. In the initial stage of this program we used the carbon K x-ray ($\lambda=4.5\text{nm}$) which required that the mask and substrate be in contact to avoid diffraction. This, in turn, caused distortion of the grating. To avoid this problem we are developing a new technology of microgap x-ray nanolithography using the copper L x-ray ($\lambda=1.33\text{nm}$).

1.15 Soft X-Ray Interferometer Gratings

Collaboration with KMS Fusion, Inc.

Erik H. Anderson, Henry I. Smith

In the soft x-ray region of the electromagnetic spectrum (1-10 nm) reliable optical constant data is scarce or non-existent. In order to fill this gap, an achromatic interferometer instrument is under construction at KMS Fusion Inc. The critical optical components of this instrument are a set of matched, 200-nm-period transmission gratings which will be fabricated at MIT. Because these gratings will be used in an interferometer, the phase-front quality must be extremely good and, at the same time, the lines must be free-standing, i.e.; have no support structure that would attenuate the x-rays. The fabrication process uses a thin membrane of silicon oxynitride which is then etched to make free-standing lines. Gold lines were found to have too much distortion for this application.

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