High Mobility Germanium MOSFETs: Study of Ozone Surface Passivation and n-type Dopant Channel Implants Combined with ALD Dielectrics

by

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B.E. The Cooper Union for the Advancement of Science and Art (2002)

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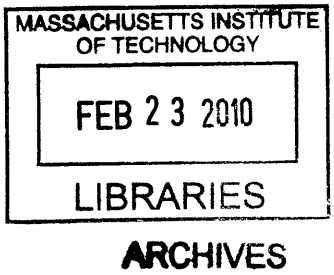

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ABSRACT

Germanium offers higher electron and hole mobility than silicon, making it an attractive option for future high-performance MOSFET applications. To date, Ge p-channel device behavior has shown promise, with many reports of measured hole mobilities exceeding that of Si. However, Ge n-channel devices have shown poor performance due to an asymmetric distribution of interface state density (D_{it}) that degrades electrostatic behavior and carrier mobility.

In this work, two methods are investigated for improving the performance of Ge MOSFETs. First, the formation of an interfacial passivation layer via in-situ ozone oxidation is explored. Long channel Ge p- and n-MOSFETs are fabricated with Al_2O_3 and HfO_2 gate dielectrics deposited by atomic layer deposition (ALD). The ozone surface passivation is observed to result in significant mobility enhancement for all devices, with particularly dramatic improvement in the n-FETs compared to devices with no passivation layer. Measurements of interface state density show a reduction across the entire Ge bandgap.

Further improvement of the interface quality has been observed to occur in the presence of n-type channel implants in Ge n-FETs and this effect is studied. All n-type species investigated in this work (P, As, Sb) are seen to result in significant electron mobility enhancement, particularly at low inversion densities. Ge n-FETs receiving channel implants of As or Sb along with the ozone surface passivation exhibit effective electron mobilities higher than Si electron mobility under some conditions of surface electric field for the first time. Substrate bias measurements and low temperature characterization both suggest a reduction in D_{it}, primarily of acceptor-like trap states near the conduction band.

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Chapter 1 - Introduction

1.1 Germanium MOSFETs

The first transistor, a point-contact bipolar device, was fabricated by Bardeen and Brattain in 1947 from a sample of polycrystalline germanium [1]. The earliest junction bipolar transistors were also fabricated on Ge samples [2], and research in the early 50's primarily focused on Ge devices. Even at that time it was recognized that surface states could dominate the electrical behavior of metal-semiconductor contacts [3], or simple field-effect devices [4] on Ge substrates. The work of Atalla et al. [5] showed that the Si-SiO_2 system could produce an interface that was relatively free from the effects of surface states, leading to the development of the Si MOSFET. The subsequent development of a planar device structure and the integrated circuit (IC) led to the rapid growth of the IC industry from the 1970's onward.

This growth was fueled in part by the continual improvement in intrinsic device performance realized by MOSFET scaling. Generally speaking, MOSFET scaling refers to the continual reduction in device dimensions; this results in increased circuit density (transistors per unit area) and also improvement in the switching delay of the MOSFET itself. Until recently, the continual improvement in intrinsic device performance has progressed without change to the channel material itself. However, it has been recognized that the parasitic components of the MOSFET structure do not follow the same scaling trend as the device size shrinks [6]. In order to maintain the historical performance trends, new channel engineering solutions have been required, such as the industry's introduction of strain-engineered Si devices [7]. As noted by Khakifirooz [8], future scaling

requirements will almost certainly require the replacement of the Si channel with higher mobility materials if that historical performance trend is to be matched.

This makes Ge an appealing option because it possesses higher electron and hole mobilities than Si [9]. Of course, the same issue that plagued early work on Ge MOSFETs still exists today, the lack of a high quality gate interface. Early Ge MOSFETs [10] avoided thermally grown gate oxides due to their inherent instability. The hexagonal GeO_2 phase of the native oxide tends to decompose at elevated temperature and is water-soluble [11]. The GeO_x sub-oxide phases are volatile at elevated temperature [12] and tend to sublime during the oxidation process making thickness and stoichiometry control very challenging for thick films.

Early work on nitrided native oxide gates suggested that germanium oxynitrides could provide more a more stable interface with reasonable device behavior [13][14]. Indeed, more recent work by Shang et al. [15] demonstrated Ge p-MOSFETs with a thin oxynitride gate (~9 nm total thickness) that exhibited hole mobility 40% greater than Si. However, similar n-channel devices showed a peak mobility of only 100 $cm^2V^{-1}s^{-1}$ [16], far below Si. The majority of recent research for a variety of gate stack approaches has also shown similar behavior. Ritenour et al. demonstrated Ge p-FETs with a HfO_2 gate showing near-Si hole mobility, however similar n-FETs showed only single-digit electron mobilities [17]. Similarly, Nicholas et al. reported Ge FETs with a CeO_2/HfO_2 gate stack; n-FET devices showed drive currents nearly two orders of magnitude below similarly processed p-FETs [18].

Generally, the best Ge p-FET results have been obtained using some method of Si surface passivation. In principle, this simplifies the problem of Ge surface passivation to

the better-understood case of Si surface passivation. However, this approach has not proven effective in realizing a well-behaved n-channel device. This asymmetry between hole and electron behavior can at first sight be attributed to the asymmetry of the valence and conduction band discontinuities between the superficial Si and the underlying Ge: holes tend to be confined in the Ge away from the interface while electron layers form at the interface. Brunco et al. reported Si-passivated p-FET devices with peak hole mobilities ranging from 250-300 $cm^2V^{-1}s^{-1}$ depending on the thickness of the passivation layer; the equivalent n-FET devices showed electron mobilities from 1.2-35 $cm^2V^{-1}s^{-1}$ [19]. Other groups have also reported similar observations [20][21].

1.2 GeO_2 Passivation Approaches

The best recent reports on Ge surface passivation have involved some type of GeO_2 interfacial layer. It has long been speculated that the high interface state density (D_{it}) of native oxides on Ge was the result of contamination from sub-oxide species other than GeO_2 [22]. As discussed in the previous section, it is difficult to grow a thick native oxide layer on Ge without significant contribution from GeO_x sub-species. However, a variety of techniques have emerged that employ a GeO_2-Ge interface, often as an interfacial layer that is part of a high-k gate stack. Takahashi et al. deposited GeO_2 layers by RF sputtering onto nitrided Ge substrates [23]. Xie et al. formed a GeO_2 interfacial layer by thermal oxidation at 400 °C prior to HfO_2 deposition and CF_4 plasma treatment [24]. Kuzum et al. used thermal oxidation in ozone ambient at 400 °C prior to Al_2O_3 deposition [25]. Lee et al. reported on GeO_2 gate oxides formed by high-pressure oxidation at 550 °C [26]. All reports show significant reduction in D_{it}, both at midgap and

near the band edges. Carrier transport for both holes and electrons is also greatly improved, with several claims of record p-FET and n-FET mobilities in the references above.

1.3 Goals of Thesis

There are several key challenges facing the incorporation of Ge as a channel material in high-performance MOSFETs. These include junction leakage from band-to-band tunneling [27], the diffusion and activation of n-type dopants for low source/drain resistance [28]. This work focuses on another critical challenge, improving the interface quality between Ge and the gate dielectric. This is primarily accomplished by exploring the impact of novel passivation methods on the performance of long-channel, unstrained MOSFETs on (100) Ge substrates with gate dielectrics deposited via the Atomic Layer Deposition method (ALD). This impact is quantitatively gauged through the reduction of interface state density, improvement in carrier mobility, and improved device electrostatics. Additionally the phosphorus implantation method observed by Ritenour [29] will be expanded to investigate other n-type species, and the impact of this method on p-channel devices will be studied.

1.4 Organization of Thesis

Chapter 2 describes the investigation of various ALD dielectric materials and their electrical behavior on Ge. The choice of wet clean prior to gate deposition is also briefly discussed, revealing that native oxide surfaces can provide superior interface properties on Ge. This is explored in the context of p- and n-FET mobility enhancement as well as improvement in electrostatic behavior. Chapter 3 presents the development and optimization of a novel ozone surface passivation technique. MOSFET results are presented along with more detailed measurement of D_{it}. Chapter 4 discusses the impact of n-type dopant channel implants on Ge FET characteristics, with particular emphasis on the observed mobility improvement in n-FET devices. Results from Ge p-FETs receiving n-type implants are also presented, suggesting that the improvement in behavior is largely confined to electron transport. Chapter 5 investigates the nature of this observed electron mobility enhancement, and results are presented indicating that the implant improves D_{it} through a reduction in acceptor-like trap states near the conduction band of Ge. Chapter 6 summarizes the key contributions of this thesis, and discusses the possibilities for future work on this topic.

Chapter 2 - ALD Gate Dielectrics on Germanium

2.1 ALD Material Capabilities

The ALD gate stacks in this work were deposited using a Cambridge NanoTech Savannah^{TM} 200 reactor. This is a nitrogen-assisted, lateral flow type reactor designed primarily for use with the alkyl-amide class metalorganic ALD precursors summarized in Table 2.1. Secondary ALD precursors utilized include de-ionized H_2O, purified NH_3, and ozone generated by electrical discharge.

Table 2.1. Material capabilities of the ALD system used in this work along with the typical chamber temperature.

ALD Precursor	*Films*	*Temperature (°C)*
tris(dimethylamido) aluminum	Al_2O_3, AlN	200
tetrakis(ethylmethylamido) zirconium [30][31]	ZrO_2, Zr_3N_4	200
tetrakis(ethylmethylamido) hafnium *~or~* tetrakis(dimethylamido) hafnium [30],[31]	HfO_2, Hf_3N_4	200
bis(tert-butylimido)-bis(dimethylamido) tungsten [32]	WN	350

An initial experiment investigated the use of all available dielectrics as interfacial layers on Ge in order to evaluate their suitability with respect to interface state density. The details of the recipe used for each material can be found in Appendix B. MOS capacitors were fabricated on (100) Ge substrates that received an HCl-based wet clean prior to dielectric deposition as detailed in Table 2.2. This clean will be referred to in the

rest of this thesis as the 'standard wet clean'. In every case 25 cycles of each material was first deposited as an interfacial layer, followed by 75 cycles of Al_2O_3 in order to eliminate the impact of the chosen contact metal on the capacitance-voltage (C-V) behavior. No intermediate WN metal was deposited in this case, and all capacitors received a 350 °C final furnace anneal for 30 min in N_2. C-V characteristics were qualitatively evaluated for stretch-out, hysteresis, and frequency dispersion. The interface state density near the middle of the bandgap was calculated by the conductance method [33].

Table 2.2. General process flow for Ge MOS capacitor fabrication.

Step	*Process*	*Description*
1	Ge Standard Wet Clean	5:1 H_2O:HCl 5 min, 5:1:1 H_2O:NH_4OH:H_2O_2 30 s, 5:1 H_2O:HCl 10 min
2	ALD Various Dielectric	Various Thickness (nominal temp 200 °C)
3	ALD Gate Metal (WN) [optional]	20 – 40 nm (350 °C)
4	Sputter Front/Back Metal Contacts	Front: 250nm Al Back: 50 nm Ti / 1μm Al
5	Pattern/Etch Al	Contact Lithography, Aluminum Etchant
6	Dry Etch ALD Gate Metal	CF_4 RIE
7	Post-Deposition Anneal	350 – 500 °C (Furnace or RTA in N_2)

Figure 2.1 and Figure 2.2 and show the resulting MOS capacitor behavior on p-type Ge for all oxide and nitride interfacial layers, respectively. The behavior of all materials on n-type Ge is presented in Appendix A. In both cases the Al-based interfacial layers display more ideal C-V behavior as well as lower calculated values of D_{it}. Although the Zr- and Hf-based films are more desirable from the perspective of reduced EOT scaling, due to their higher dielectric constant, they display significantly poorer C-V behavior on both p-type and n-type Ge, suggesting higher interface density across the

entire bandgap. For this reason the majority of the gate stacks used in this work involve the Al-based materials.

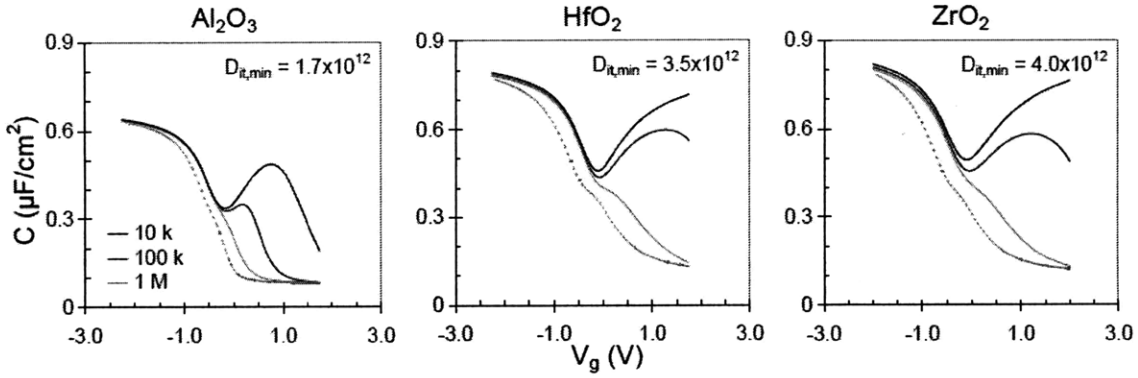

Figure 2.1. Forward C-V characteristics at f = 1 kHz, 10 kHz, and 1 MHz, and reverse (dashed) at f = 1 MHz for p-type Ge capacitors with various ALD oxide interfacial layers (all capped with ALD Al_2O_3). Indicated D_{it} values were calculated with the conductance method.

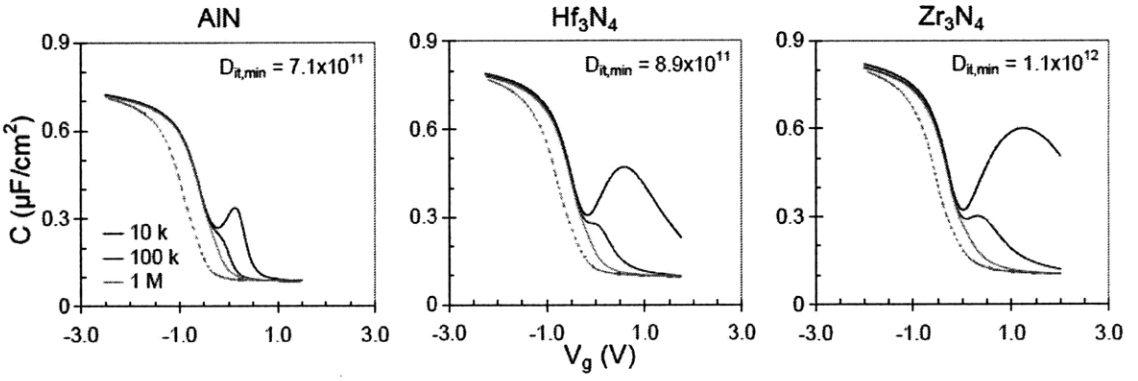

Figure 2.2. Forward C-V characteristics at f = 1 kHz, 10 kHz, and 1 MHz, and reverse (dashed) at f = 1 MHz for p-type Ge capacitors with various ALD nitride interfacial layers (all capped with ALD Al_2O_3). Indicated D_{it} values were calculated with the conductance method.

2.2 Influence of Wet Chemistry on Germanium MOS Capacitor

MOS capacitors were fabricated on (100) p-type Ge substrates (Ga: 0.16-0.47 Ω-cm). Substrates were cleaned in a variety of wet chemistries as indicated in Figure 2.3. In each case the wafer was exposed to the indicated chemistry for 20 min, followed by a 1 min rinse in DI water and then blown dry in N_2. The wafers proceeded directly to ALD gate deposition, in this case receiving a 25 cycle interfacial layer of AlN and a 35 cycle capping layer of Al_2O_3. Sputtered Al was used as the top and backside contact metal.

High frequency C-V characteristics were evaluated for frequency dispersion, stretch-out, hysteresis, and the relative size of the weak-inversion 'bump'. As Figure 2.3 illustrates, the choice of wet chemistry has negligible impact on any of these parameters, suggesting that the interface quality for all choices is nearly identical. Because most chemically formed and native germanium oxides are water soluble, it is likely that any unique surface configuration provided by a specific choice of wet chemistry is ultimately removed during a final water rinse [34].

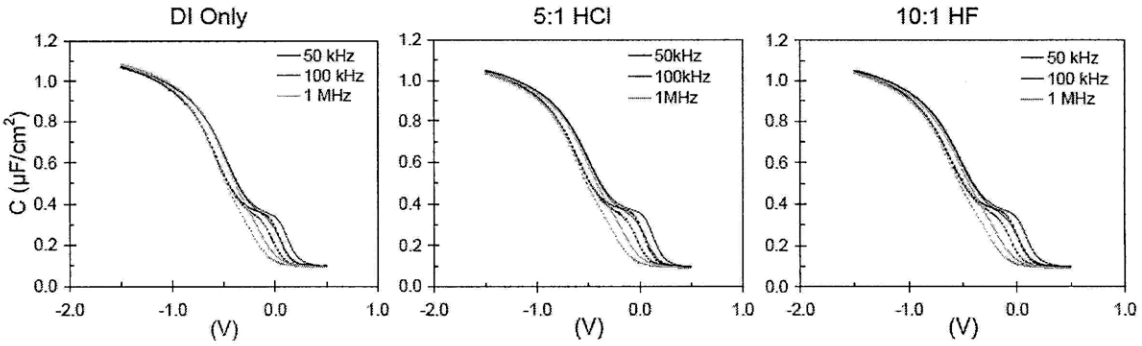

Figure 2.3. Forward and reverse C-V characteristics of ALD AlN/Al_2O_3 on p-type Ge for various choices of wet chemistry prior to gate deposition.

However, even better C-V behavior was noted in a similar experiment that investigated the impact of using no wet clean at all prior to ALD gate deposition. Figure 2.4 shows that the C-V characteristics of two ALD materials on Ge can be dramatically improved when no clean is used, compared to the use of a standard HCl-last wet clean. In the case of the AlN interfacial layer shown in Figure 2.4, the minimum D_{it} near mid-gap as measured by the conductance method was reduced from $2.0x10^{12}$ $cm^{-2}eV^{-1}$ for the wet-cleaned capacitor to $3.6x10^{11}$ $cm^{-2}eV^{-1}$ for the no-clean capacitor.

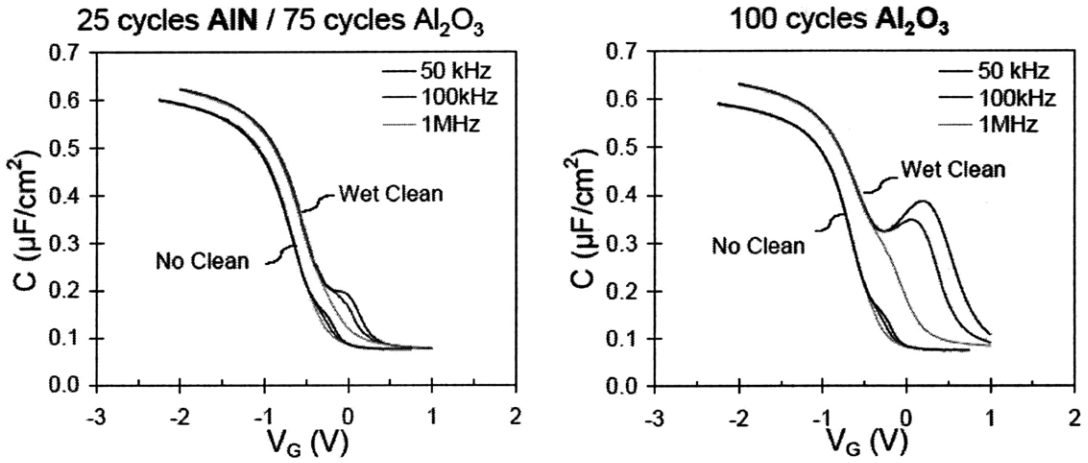

Figure 2.4. C-V characteristics of ALD AlN and ALD Al_2O_3 on p-type Ge for substrates receiving no clean and substrates receiving an HCl-last wet clean prior to deposition.

2.3 'Epi-ready' Ge Surface

The manufacturer (Umicore) of the substrates used in this work markets their material as 'epi-ready' indicating that they are suitable for epitaxial growth directly from the package without an intermediate wet chemical clean. The preparation of the 'epi-ready' surface

involves a proprietary thermal treatment and wet clean, with the final substrate packed in an N_2 environment before shipping.

A simple experiment was performed in order to compare the 'epi-ready' surface to the native oxide of Ge. ALD Al_2O_3 was deposited on p-type Ge substrates that received either no clean, or the standard wet clean followed by 60 hours exposure to air (68 °F, 45% RH). Both devices received a 350 °C furnace anneal for 30 min following sputtering of Al metal contacts. Figure 2.5 shows that the high-frequency C-V characteristics of both samples are remarkably similar, with only slight differences in D-factor, hysteresis, and maximum accumulation capacitance. This result suggests that the 'epi-ready' surface is chemically similar to the native oxide surface.

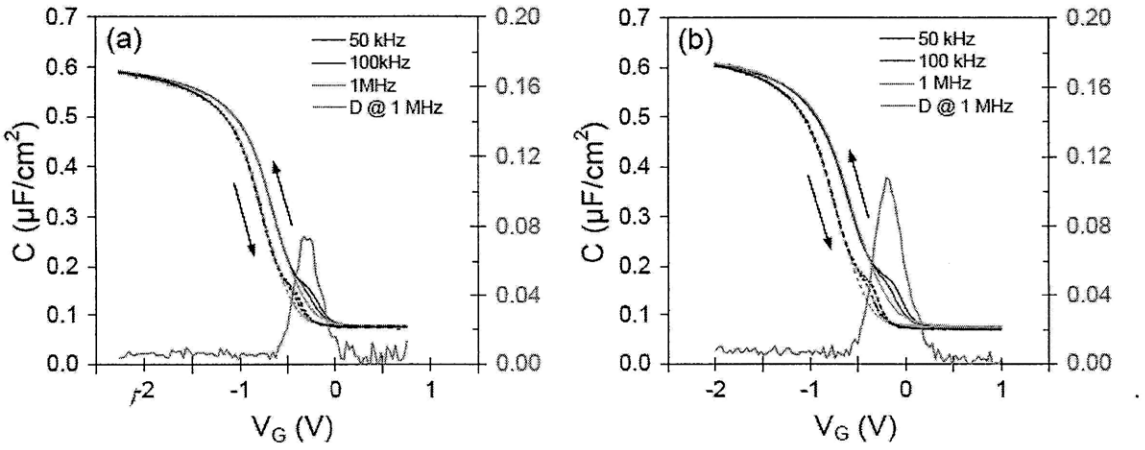

Figure 2.5. Comparison of C-V characteristics for 10 nm ALD Al2O3 on (a) a substrate receiving no wet clean and (b) a substrate receiving the standard wet clean plus 60 hours exposure to air.

This observation was confirmed by performing x-ray photoelectron spectroscopy (XPS) on Ge samples that were prepared as above. Figure 2.6 shows a broad survey comparison of the spectra measured for both samples, and again suggests the two

surfaces are chemically similar. No additional peaks are observable for the 'epi-ready' scan, such as peaks typically observed for Cl- [35] or S-terminated [36] surfaces, two common approaches to Ge monolayer surface passivation. More detailed studies on the interface chemistry of native Ge oxides [37][38] indicate that the 4+ oxidation state is the dominant component. This oxidation state is attributed to the GeO_2 phase of germanium oxide. Figure 2.7 shows a higher resolution scan of the Ge2p peak for each sample, and confirms that the 'epi-ready' surface and native oxide surface are nearly identical in terms of interfacial oxide composition, and also that interface oxide layer is primarily GeO_2.

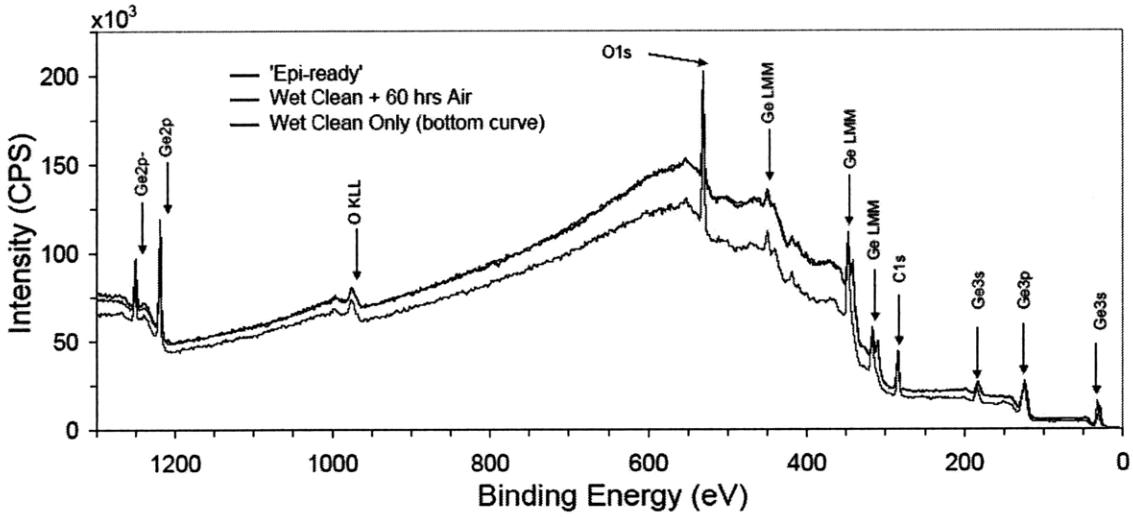

Figure 2.6. XPS survey scan showing a comparison of Ge substrates receiving: standard wet clean, standard wet clean followed by 60 hrs exposure to air, and no clean directly from the package. [Analysis performed at MIT CMSE]

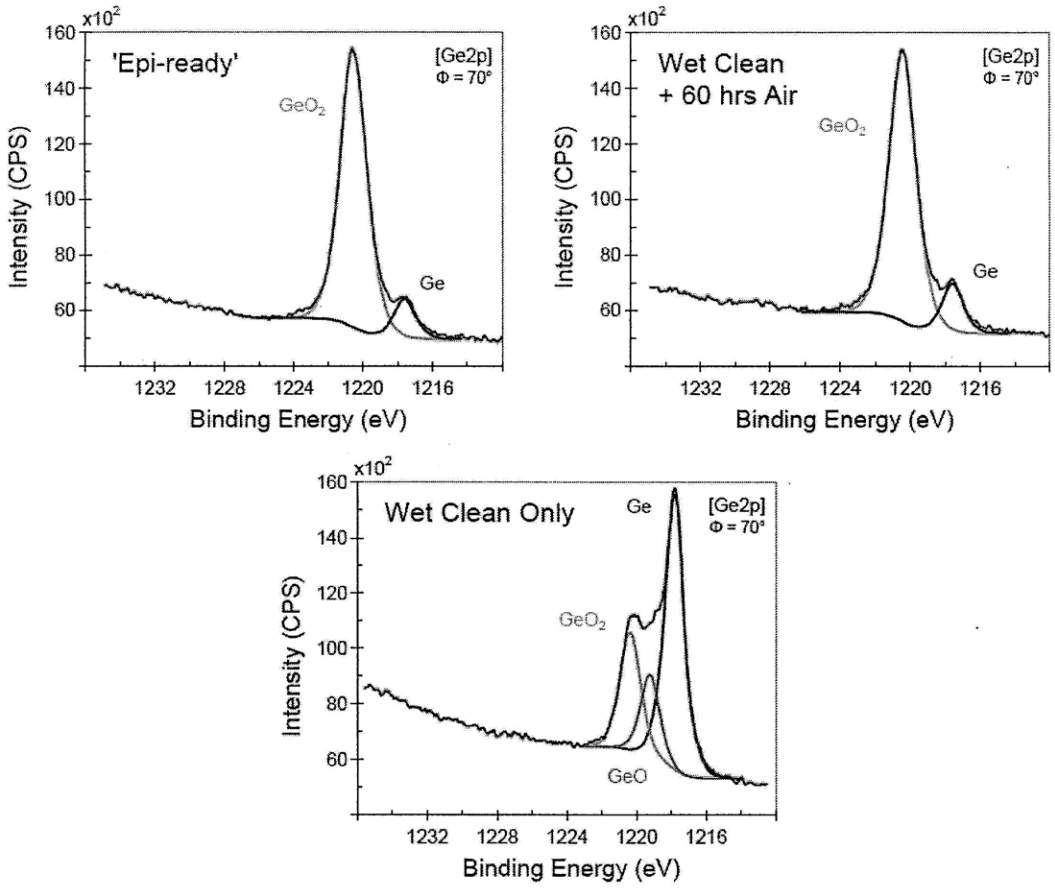

Figure 2.7. Detailed view of Ge2p XPS spectra for substrates with the 'epi-ready' passivation layer compared to a sample receiving the standard wet clean followed by 60 hrs exposure to air and to a sample that received the standard wet clean only immediately prior to analysis.

Table 2.3. General long-channel ring-FET process flow.

Step	*Process*	*Description*
1	Ge Standard Wet Clean [skipped for 'epi-ready' devices]	5:1 H_2O:HCl 5 min, 5:1:1 H_2O:NH_4OH:H_2O_2 30 s, 5:1 H_2O:HCl 10 min
2	ALD Passivation/Dielectric	Various Thickness (nominal temp 200 °C)
3	ALD Gate Metal (WN)	~ 40 nm (350 °C)
4	Gate Pattern/Etch	Contact Lithography, CF_4 RIE
5	S/D Ion Implant	BF_2, 40 keV, $1x10^{15}$ cm^{-2} (p-FET) P, 25 keV, $1x10^{15}$ cm^{-2} (n-FET)
6	Interlayer Dielectric Deposition	200 nm PECVD SiO_2
7	S/D Activation Anneal	450 °C 30 min Furnace N_2 (p-FET) 500 °C 1 min RTA N_2 (n-FET)
8	Via Pattern/Etch	Contact Lithography, 3:1 H_2O:BOE
9	Contact Metal	Front: 500 nm Al Back: 50 nm Ti / 2μm Al
10	Contact Metal Pattern/Etch	Contact Lithography, Aluminum Etchant

Long channel ring-MOSFETs with ALD 40 nm WN / 7 nm Al_2O_3 gate stacks were fabricated in order to evaluate the impact of the native oxide passivation layer on carrier mobility. The full MOSFET process flow is summarized in Table 2.3. Effective hole and electron mobilities as calculated by the split-CV technique [39][40] are shown in Figure 2.8. In this figure, and elsewhere in this thesis, the Si universal mobility for holes or electrons is obtained from universal data plotted versus vertical effective field (E_{eff}) [41]. The number of inversion carriers, N_{inv}, is calculated assuming a constant doping profile equal to that of the Ge substrates used in this work ($N_{A,D} \approx 1x10^{16}$ cm-3).

Nearly a 2x improvement in hole mobility is observed for devices receiving no clean compared to the standard clean devices. Even more dramatic improvement is observed in the electron mobility of n-FET devices receiving no clean. As indicated in Figure 2.9, the typical I_s-V_g curves for n-FET devices receiving the standard wet clean show very poor subthreshold behavior and suppressed drive current, resulting in single digit electron mobility. The 'epi-ready' n-FET devices show significant improvement in

subthreshold behavior, with a subthreshold swing of 92 mV/dec that is among the lowest reported for an n-channel Ge MOSFET. However, this swing is not as low as the equivalent p-FET device (82 mV/dec), and while the measured hole mobility is higher than that of Si, the measured electron mobility remains below.

It is noted from Figure 2.10 that the contribution of the 'epi-ready' passivation layer to the total capacitance equivalent thickness (CET) of the gate stack is greater than 1 nm for both p-FET and n-FET devices. Here CET is defined as the SiO_2 equivalent thickness based on the measured capacitance in inversion, defined as:

$$CET = \frac{\varepsilon_{ox,Si}}{C_{inv}} \tag{1}$$

where $\varepsilon_{ox,Si}$ is the permittivity of SiO_2, 3.5×10^{-13} F cm^{-1}, and C_{inv} is the maximum measured capacitance from the inversion-side split-CV. This differs from the equivalent oxide thickness (EOT), which is also a SiO_2 equivalent thickness, but includes the impact of quantum effects on the measured capacitance (see Section 5.2). The physical thickness of the passivation layer is unknown, however values of the dielectric constant of GeO_2 have been reported ranging from 5 to 6 [42][43]. Using the CET contribution of the native oxide layer indicated in Figure 2.10, the physical thickness is estimated to be between 1.4 and 2.3 nm. The CET values obtained for the 'epi-ready' MOSFETs suggest that the passivation layer on p-type substrates (n-FET) is thicker than the n-type substrates, perhaps as the result of an additional thermal step performed by the manufacturer. This thickness difference was confirmed by XPS. A more subtle discrepancy in CET was observed in the wet-cleaned devices, where the n-FET displays a 0.5 nm higher CET than the p-FET device despite receiving an identical 7 nm Al_2O_3 gate dielectric. This offset is attributed in part to the more severe stretch-out observed the

measured C_{inv} in the n-FET device, which will lead to an underestimation of the true oxide capacitance at an equivalent gate voltage.

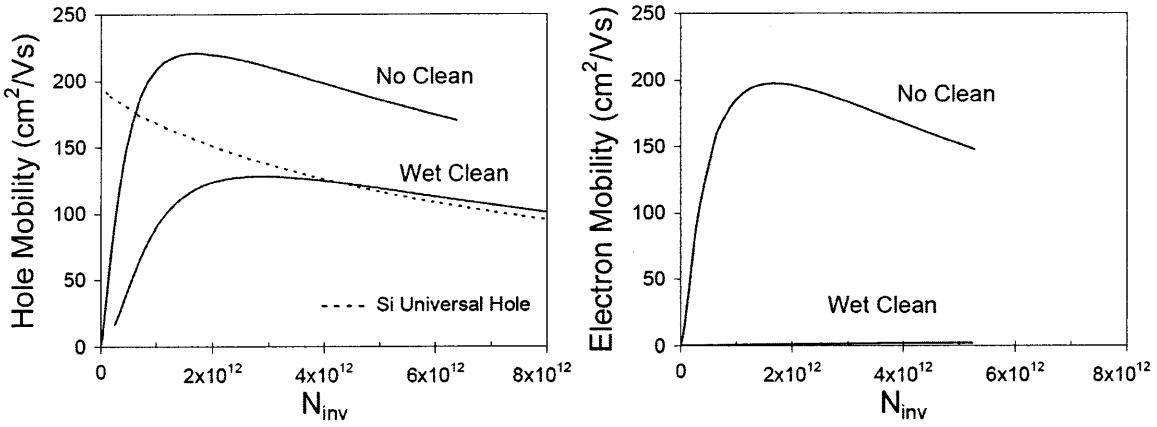

Figure 2.8. Effective carrier mobility for Ge p- and n-MOSFETs with and without standard wet clean prior to deposition of ALD 7 nm Al_2O_3 and 40 nm WN gate stack.

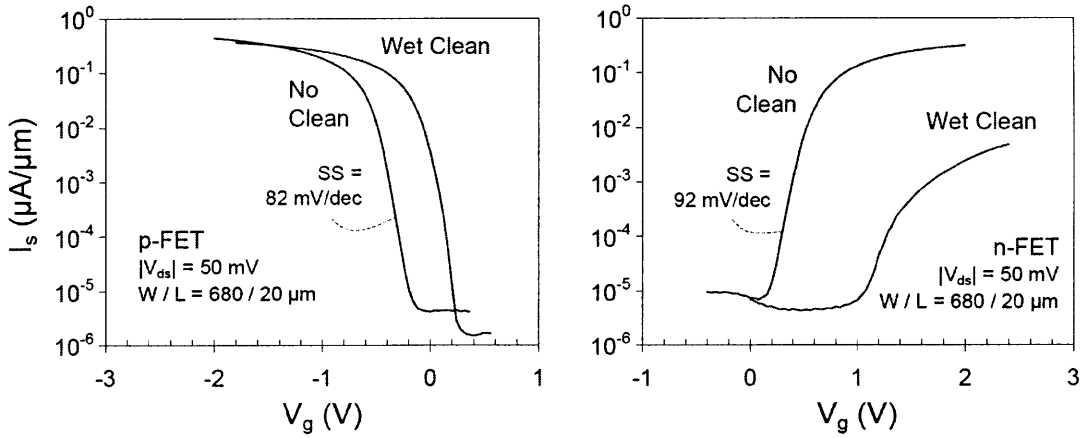

Figure 2.9. Typical I_s-V_g characteristics for Ge p- and n-MOSFETs with and without standard wet clean.

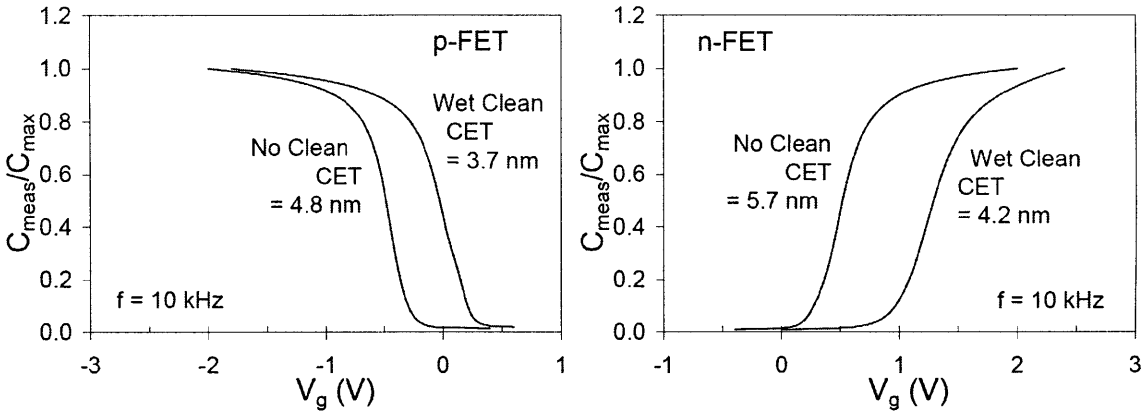

Figure 2.10. Inversion side split-CV characteristics for Ge p- and n-MOSFETs fabricated with and without the standard wet clean. The measured C_{gsd} has been normalized to the maximum measured value for each device.

2.4 Chapter Summary

ALD gate dielectrics deposited directly on wet-cleaned Ge substrates show significant non-idealities in C-V behavior as result of high interface state density. Al-based dielectric films show more promising as-deposited behavior than Hf and Zr based films. The choice of wet chemistry prior to gate deposition was observed to have little impact on measured C-V characteristics, although un-cleaned substrates showed dramatic improvement in C-V behavior as a result of reduced D_{it}. This reduction in D_{it} is the result of the presence of the 'epi-ready' passivation layer that behaves very similarly to a simple native oxide.

As discussed in Chapter 1, thick Ge oxides are difficult to grow without large contributions from non-GeO_2 sub-oxide components that are less desirable from a D_{it} standpoint. Thin native oxides formed at room temperature are primarily GeO_2, but have often been avoided due to their solubility in aqueous solutions and apparent thermal instability. It is speculated that the native oxide passivation layer investigated in this chapter is not degraded during the low temperature ALD process (initially 200 °C),

whereas its instability may be apparent had a higher temperature CVD process been used to complete the gate stack formation. It is also speculated that this ALD capping layer protects the stability of the native oxide layer during subsequent high temperature source/drain annealing.

MOSFETs fabricated with this passivation layer and receiving activation anneals as high as 500 °C show improvement in carrier mobility and subthreshold swing over devices receiving only a standard wet clean. The 'epi-ready' p-FET devices show a 2x hole mobility improvement over the wet cleaned devices, and even more dramatic improvement was observed in the n-FET devices.

Chapter 3 - Ozone Surface Passivation

3.1 Introduction

From a practical standpoint, the surface treatment of 'epi-ready' substrates discussed in the previous chapter is undesirable. As evidenced by the poor characteristics of the wet cleaned devices, the native oxide of Ge is extremely unstable in aqueous solutions, thus limiting its use to pure gate-first processing. Also, as indicated in Figure 2.10, the contribution of the native oxide layer to the total equivalent thickness of the gate is greater than 1 nm, which would preclude its use for aggressively scaled gate stacks.

Ozone is typically used as an alternate oxidizing precursor in a standard ALD process [44][45]. In this work it was investigated for its effectiveness at creating an oxide interfacial layer prior to the deposition of an ALD gate dielectric. Ozone was generated using an MKS O_3Mega electrical-discharge type generator. O_3 is created by introducing high purity O_2 through an electrical-discharge cell that decomposes the molecule into monatomic intermediates that then react with other O_2 molecules to form O_3 at concentrations up to 20% by weight. The addition of a dopant gas, in this case N_2, is usually required to help catalyze the formation of O_3 and stabilize its output.

Figure 3.1 shows that significant improvement in C-V behavior can be obtained for a sample that received the standard wet clean, followed by in-situ (in the ALD chamber) exposure to high-concentration O_3 immediately prior to ALD Al_2O_3/WN gate stack deposition.

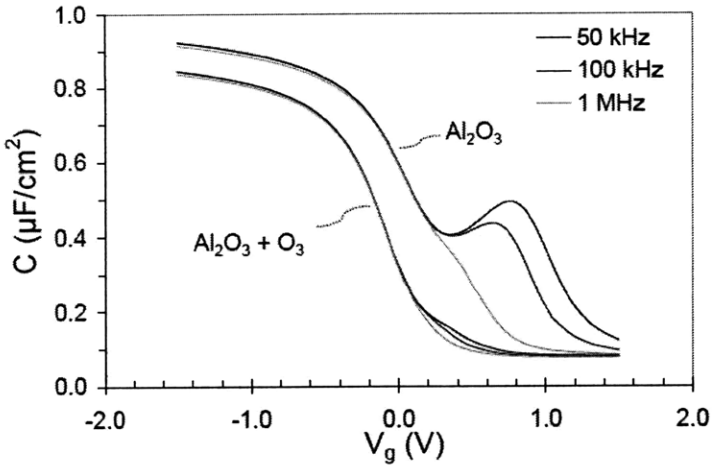

Figure 3.1. C-V characteristics for ALD Al_2O_3 on p-type Ge for samples receiving a wet clean only and a wet clean plus in-situ exposure to O_3. These samples received a 500 °C RTA in N_2 for 1 min.

3.2 Ge MOS Capacitor and Interface State Density

In order to quantify the observed improvement in the C-V behavior of O_3-treated Ge, the interface state density (D_{it}) was extracted on both p- and n-type samples. MOS capacitors were fabricated on (100) Ge substrates that received the standard wet clean described in Chapter 2. The untreated sample proceeded directly to ALD of 6 nm of Al_2O_3, while the O_3-treated sample was first exposed to 10 min of high concentration ozone followed by the same dielectric deposition. The process parameters of the ozone generator used in this initial experiment are described in more detail in Section 3.4.

In Figure 3.2a, D_{it} was calculated near the center of the bandgap by the conductance method [36] at both room temperature and at 250 K. It has been noted [46] that at room temperature the use of the conductance method with Ge may tend to over-estimate the true D_{it} at midgap due the influence of a minority-carrier weak inversion response on the value of the measured conductance. The smaller bandgap of Ge

compared to Si leads to higher intrinsic carrier concentration and therefore a higher density of minority carriers at room temperature. The response from these thermally generated minority carriers in a Ge MOS capacitor can mask the measured conductance, particularly at low frequencies.

This is evident in the discrepancy observed between the D_{it} values calculated on the wet-cleaned p-type samples at room temperature and 250 K where the concentration of minority electrons has been reduced. This discrepancy is not as severe for the O_3-treated and n-type samples because the weak-inversion response (apparent as the 'bump' in the measured C-Vs) is comparatively smaller. The response itself can be trap-assisted, so a reduction in trap density leads to less weak-inversion response and less tendency to overestimate D_{it}. The calculated values of D_{it} on both p- and n-type samples indicate that the O_3 treatment reduces D_{it} near the middle of the gap by nearly an order of magnitude to a minimum value of nearly $2x10^{11}$ $cm^{-2}eV^{-1}$.

In Figure 3.2b, D_{it} was calculated closer to the band edges using the Gray-Brown method [47] at temperatures down to 80 K. This method compares the observed flatband voltage shift as a function of temperature to the ideal shift expected. Any additional observed shift in the measured data can be attributed to interface states that lie within the energy range of the corresponding change in Fermi level.

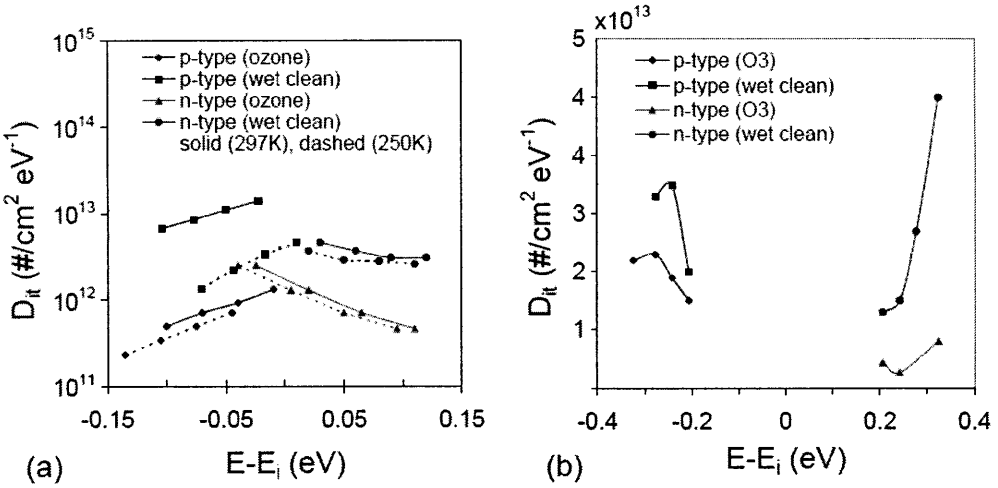

Figure 3.2. Interface state density for ozone-treated and untreated Ge MOS capacitors with 6 nm ALD Al_2O_3. D_{it} values were calculated by (a) the conductance method and (b) the Gray-Brown method.

3.3 Ozone Passivated Ge MOSFETs

In an experiment similar to that described in Section 2.3, long channel ring MOSFETs were fabricated on p-type and n-type Ge (100) substrates (Sb: 0.13-0.16 Ω-cm, Ga: 0.16-0.47 Ω-cm). Devices were fabricated with the clean and general process flow described in Table 2.3. All devices received an ALD 40 nm WN / 6 nm Al_2O_3 gate stack, the O_3-treated devices received a 10 min in-situ exposure immediately prior to this deposition.

The calculated effective hole and electron mobilities and the corresponding I_s-V_g and inversion C-V characteristics are shown in Figure 3.3, Figure 3.4, and Figure 3.5, respectively. Once again, significant mobility enhancement is observed for both p-FET and n-FET devices, with particularly dramatic improvement in electron mobility. The

improvement in mobility and subthreshold swing is similar to that observed for the 'epi-ready' MOSFETs, illustrating the effectiveness of the O_3 treatment in emulating the characteristics of the native oxide surface. However, as indicated in Figure 3.5, the contribution of the O_3 treatment to the total EOT of the gate stack in considerably less than that added by the native oxide. The p-FET devices show an increase in EOT of only 0.3 nm compared to untreated devices.

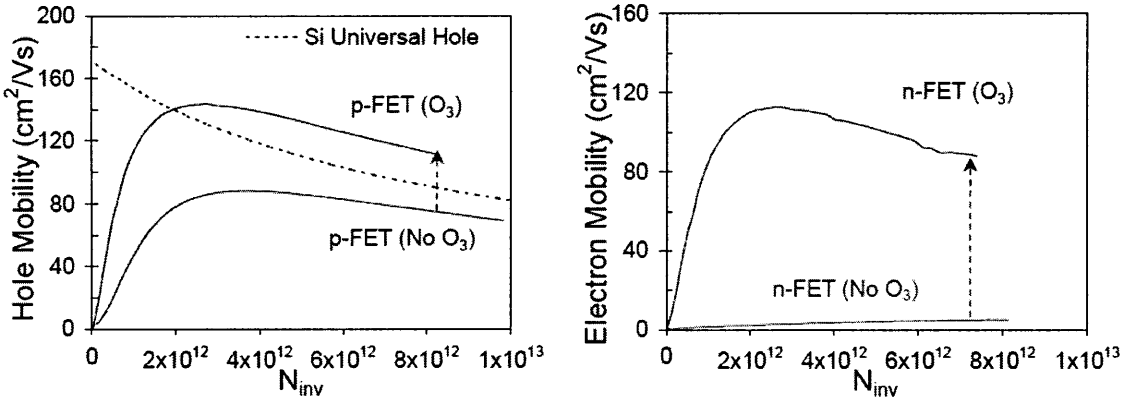

Figure 3.3. Observed mobility improvement for Ge p-and n-FETs receiving the in-situ O_3 surface treatment prior to gate deposition of ALD Al_2O_3.

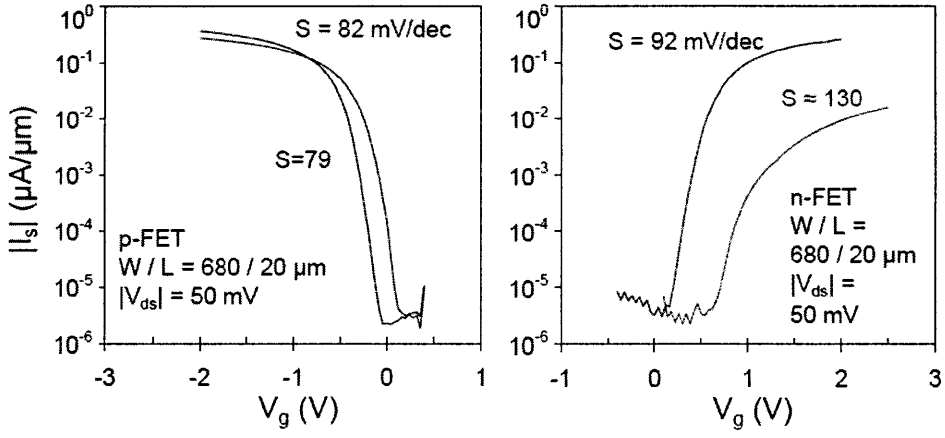

Figure 3.4. Typical I_s-V_g characteristics for Ge p- and n-MOSFETs with and without exposure to the O_3 surface treatment.

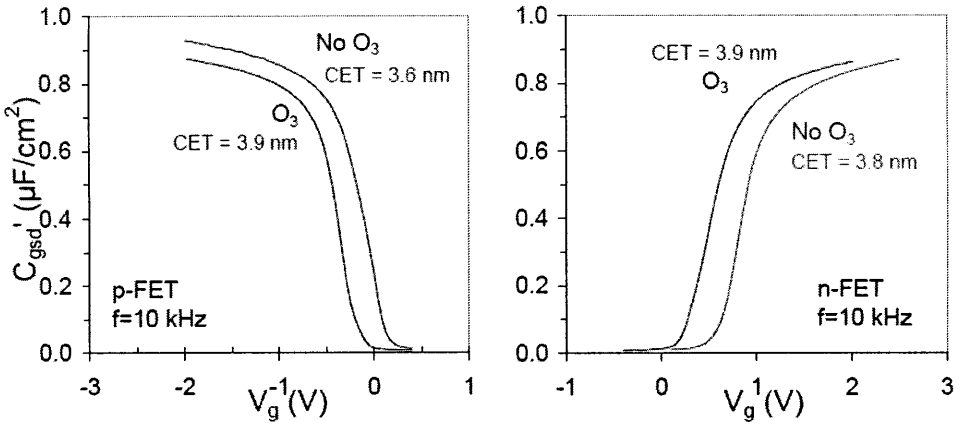

Figure 3.5. Inversion side split-CV characteristics for Ge p- and n-MOSFETs fabricated with and without exposure to the O_3 surface treatment.

3.4 Ozone Surface Treatment Optimization

The results in the previous sections of this chapter were obtained with the parameters of the ozone generator set for the maximum stable ozone concentration of the system. These parameters include:

1. *80% cell power*, a higher setting is possible but O_3 concentration may become unstable due to cell heating and circuit limitations, a lower setting will reduce O_3 concentration
2. *500 sccm O_2 flow*, minimum setpoint, a higher setting will reduce O_3 concentration
3. *0.05 sccm N_2 flow*, O_3 concentration becomes unstable at lower settings, higher settings result in decreased O_3 concentration and increased NO_x byproducts

At these settings the O_3 output concentration as measured by the tool's internal sensor was approximately 19% (by weight in O_2). The initial work was performed with a 10 min

exposure prior to gate deposition, shorter times resulted in notably higher D_{it}, while longer times yielded negligible change in D_{it} or EOT contribution. The exposure was performed at an ALD chamber temperature of 200 °C, the same temperature as the Al_2O_3 deposition.

A more detailed capacitor study was performed in order to investigate and quantify C-V behavior for three main parameters: exposure time, N_2 dopant flow, and exposure temperature. MOS capacitors were fabricated on n- and p-type Ge (Sb: 0.13-0.16 Ω-cm, Ga: 0.16-0.47 Ω-cm) with a 20nm WN / 6 nm Al_2O_3 ALD gate stack. Metallic Al and Ti/Al front and backside contacts were sputter deposited. The Al front contacts were wet etched, followed by RIE etching of the WN gate metal in CF_4. All capacitors received a final rapid thermal anneal in N_2 for 1 min at 500 °C, in order to approximate the typical thermal budget of the full MOSFET process flow.

High-frequency C-V measurements were performed with an Agilent 4924 impedance analyzer at frequencies from 1 kHz – 1 MHz. The highest bandwidth setting was used in order to minimize noise at low frequencies. The same total voltage range was swept for each device with the flatband voltage roughly centered in this range. The measured characteristics were then evaluated for:

1. Minimum D_{it}, the minimum G_p/ω for the voltage curve displaying a clear peak in G_p/ω (see Figure 3.6). The interface state density can then be approximated as [48]:

$$D_{it} \approx \frac{2.5}{q}\left[\frac{G_p}{\omega}\right]_{\max} \tag{2}$$

2. Hysteresis, measured at 100 kHz at a capacitance of $C_{max}/2$.

3. Frequency dispersion in C_{max}, defined as the percent change in C_{max} from 1 kHz to 1 MHz. At low frequencies interface traps respond to the AC signal and contribute to the measured capacitance, at higher frequency some traps may no longer be able to respond, resulting in a reduced measured capacitance.
4. Weak-inversion 'bump', defined as the difference in area between the 20 kHz curve and 1 MHz curve integrated from the starting voltage to $C_{max}/2$. In Ge, thermally generated minority carriers become trapped by midgap states and are able to contribute an additional capacitance to the measured low-frequency C-V curve.
5. C-V steepness, defined as the maximum slope of normalized capacitance (C/C_{max}) at 1 MHz, at high frequency interface traps may not respond to the AC signal but will respond to the slow sweep of the DC bias resulting in stretch-out along the gate bias axis. This comparison is only valid for devices fabricated on substrates with identical doping concentrations.

This summary provides an interesting illustration of the difference in behavior between Ge p-type and n-type capacitors. At midgap, the measured D_{it} and the resulting C-V behavior are similar on both substrates. However, the C-V behavior for holes and electrons is markedly different when biased in strong accumulation (near the majority carrier band edge). As indicated in Table 3.1, all n-type capacitors show significantly more dispersion in C_{max} and more than two times the hysteresis of the equivalent p-type capacitor, even for ozone-treated devices.

The resulting analysis is summarized in Table 3.1 along with values for both p- and n-type capacitors that received no O_3 treatment at all. All ozone-treated devices show

significant improvement over untreated devices specifically with respect to the measured interface state density. Variations in exposure time and temperature from the nominal conditions (devices p2 and n2 in Table 3.1) described above generally resulted in poorer C-V behavior. However, as highlighted in Table 3.1, increases in the dopant flow rate produced the most noticeable improvements across the majority of metrics for both p-type and n-type capacitors. The optimized C-V characteristics are shown in Figure 3.7 and Figure 3.8. For comparison, the C-V characteristics of the untreated p-type and n-type capacitors are shown in Figure 3.9 and Figure 3.10, respectively. The improvement is most evident in the reduction of the weak inversion 'bump', and also the reduction in C_{max} dispersion for the n-type capacitor. For each substrate type the overall steepness of the C-V curve has also been significantly improved. Although measurable, the impact on C-V hysteresis is minor on both substrates despite the large reduction in D_{it}.

Table 3.1. Experimental investigation of ozone operating parameters. Bolded parameters are variations from the nominal devices p2 and n2. Shaded entries represent the best result for both p- and n-type capacitors.

(p/n-type) + ID#, Time (min), Temperature (°C), N_2 flow (sccm)	*Minimum D_{it} ($x10^{11}$ $cm^{-2}eV^{-1}$)*	*Hysteresis (mV)*	*C_{max} Change (%)*	*C-V slope (V^{-1})*	*'Bump' Area ($x10^{-8}$ C/cm^2)*
p1, **1**, 200, 0.05	4.7	110	1.77	1.17	3.8
p2, 10, 200, 0.05	3.7	105	1.16	1.20	2.5
p3, 10, 200, **5.0**	3.4	97	1.07	1.21	2.2
p5, 10, 200, **0.01**	5.0	116	1.32	1.16	4.3
p6, **30**, 200, 0.05	4.0	105	1.16	1.20	2.4
p7, 10, **100**, 0.05	5.7	114	1.25	1.17	6.8
p8, 10, **300**, 0.05	9.4	109	1.09	1.31	7.6
pX, **No O_3**	14.5	110	1.26	0.93	16.7
n1, **1**, 200, 0.05	6.5	243	6.87	1.10	3.1
n2, 10, 200, 0.05	4.7	237	4.58	1.20	2.4
n3, 10, 200, **5.0**	3.8	235	4.88	1.30	2.3
n5, 10, 200, **0.01**	6.1	259	5.61	1.12	3.1
n6, **30**, 200, 0.05	5.8	248	5.52	1.22	3.0
n7, 10, **100**, 0.05	8.4	240	6.03	1.08	3.7
n8, 10, **300**, 0.05	4.2	240	5.37	1.33	2.5
nX, **No O_3**	24.5	246	7.62	0.82	9.8

Interestingly, the ozone concentration is actually lowered to approximately 6% for the optimal N_2 flow rate of 5.0 sccm. Adding N_2 as a dopant gas at low concentration increases the generated O_3 concentration by a catalytic effect [49]. At larger N_2 concentrations the O_3 concentration decreases as the formation of NO_x species becomes more prevalent [50]. Subsequent tests verified that the interface improvement was not the

result of the lower O_3 concentration by fabricating similar capacitors using reduced cell power or higher O_2 flow rates (both of which would also reduce the generation efficiency). In both cases, D_{it} was observed to increase again, suggesting that moderate O_3 concentration plus the additional NO_x species are both needed for optimal D_{it}.

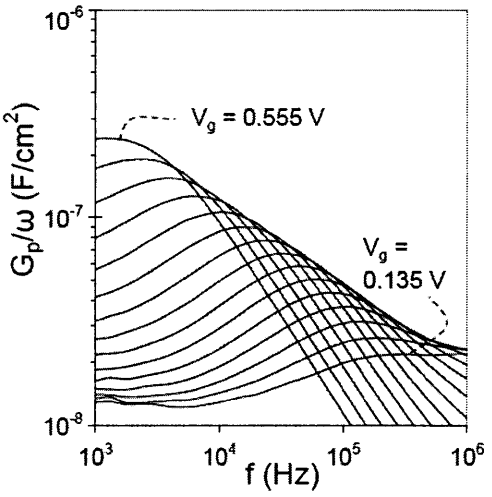

Figure 3.6. Family of G_p/ω curves with applied voltage as a parameter for optimized ozone process on p-type Ge with ALD Al_2O_3 (sample p3).

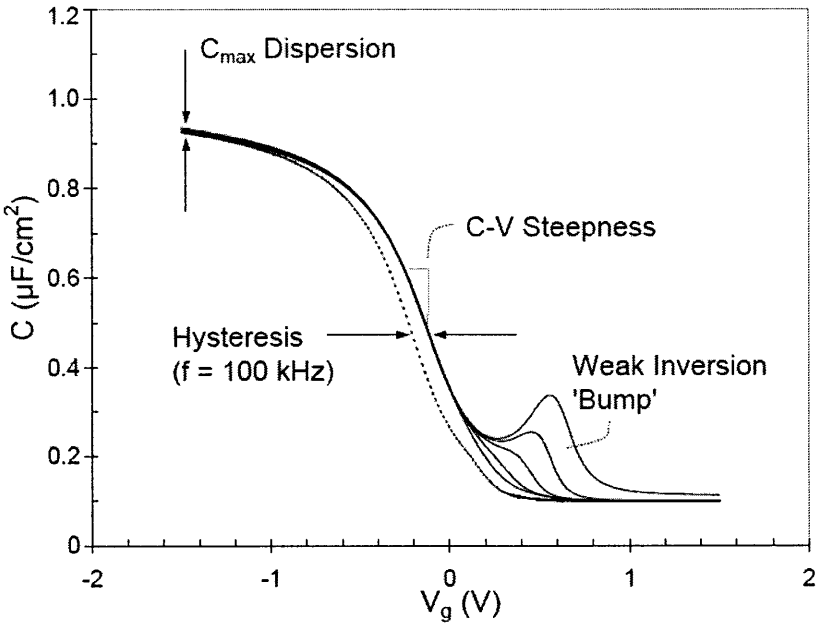

Figure 3.7. Forward C-V characteristics at f = 1, 4, 20, 100, 1000 kHz, and reverse curve (dashed) at f = 100 kHz for optimized ozone process on p-type Ge (sample p3). Labels indicate the characteristics investigated in this optimization.

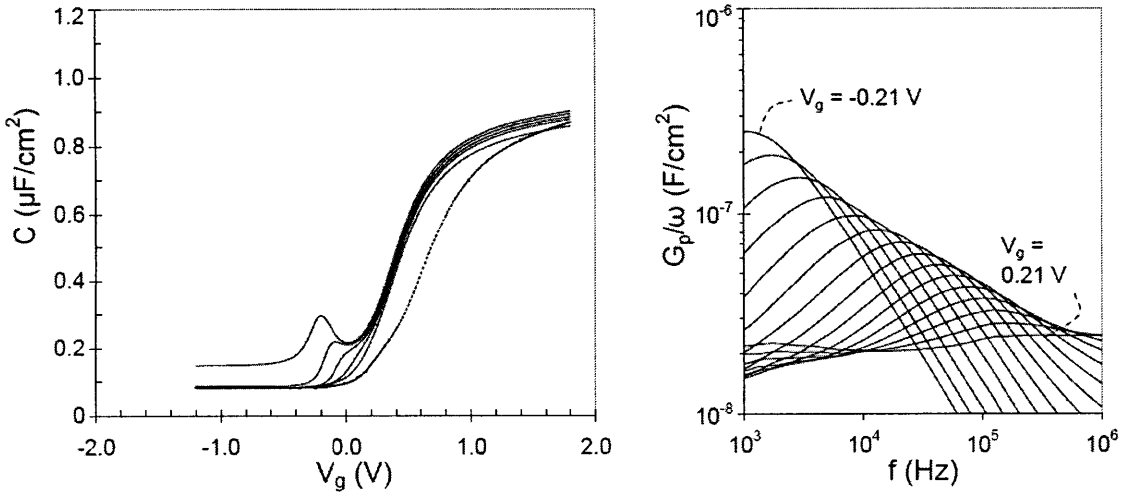

Figure 3.8. Forward C-V characteristics at f = 1, 4, 20, 100, 1000 kHz, and reverse (dashed) at f = 100 kHz for the optimized ozone process on n-type Ge (sample n3), and the family of G_p/ω curves with applied voltage as a parameter for the same device.

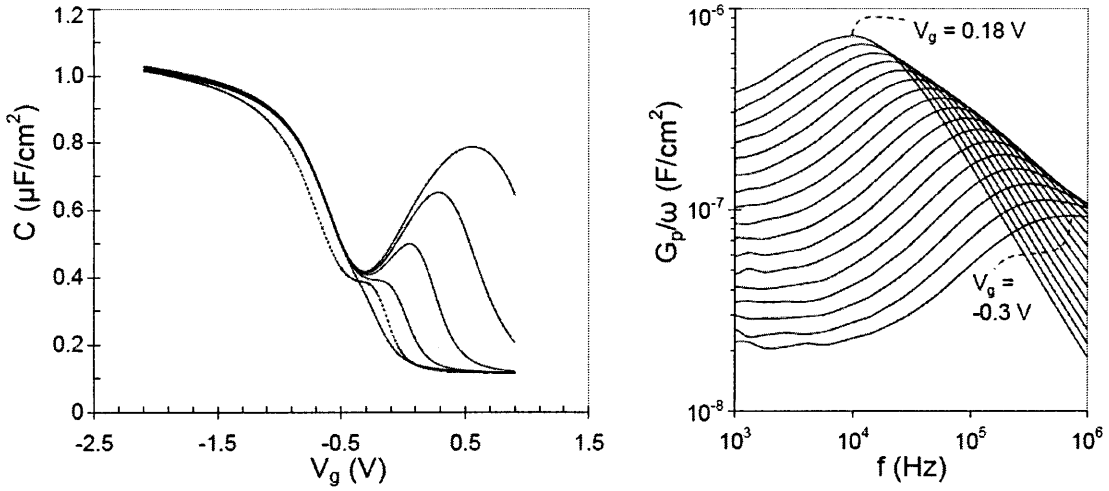

Figure 3.9. Forward C-V characteristics at f = 1, 4, 20, 100, 1000 kHz, and reverse (dashed) at f = 100 kHz for a p-type capacitor receiving no ozone (sample pX), and the family of G_p/ω curves with applied voltage as a parameter for the same device.

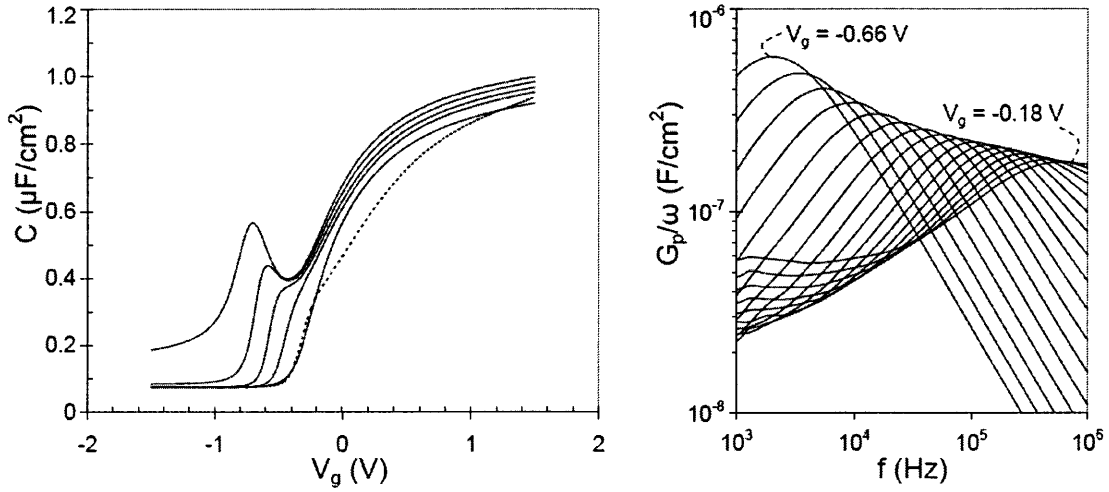

Figure 3.10. Forward C-V characteristics at f = 1, 4, 20, 100, 1000 kHz, and reverse (dashed) at f = 100 kHz for a n-type capacitor receiving no ozone (sample nX), and the family of G_p/ω curves with applied voltage as a parameter for the same device.

A subsequent experiment investigated the impact of the optimized O_3 process on Ge MOSFET performance. Long channel ring-FETs were fabricated on p- and n-type Ge substrates (Sb: 0.16-0.22 Ω-cm, Ga: 0.42-0.46 Ω-cm). The devices were fabricated with same process flow and 6 nm ALD Al_2O_3 gate dielectric as the devices described in

Section 3.3, with the exception of using the optimized O_3 surface treatment discussed above. Figure 3.11 shows the effective hole and electron mobilities for the 'epi-ready' and nominal O_3 processes described earlier, compared to the optimized O_3 process described above. The optimized devices show additional increases in both hole and electron mobility, with equivalent subthreshold slope and EOT when compared to the nominal O_3 process. In fact, the extracted mobility is very similar to that of the 'epi-ready' devices (7 nm Al_2O_3 gate). However, as discussed earlier in this chapter, the O_3 surface passivation layer has far less EOT impact than the native oxide layer.

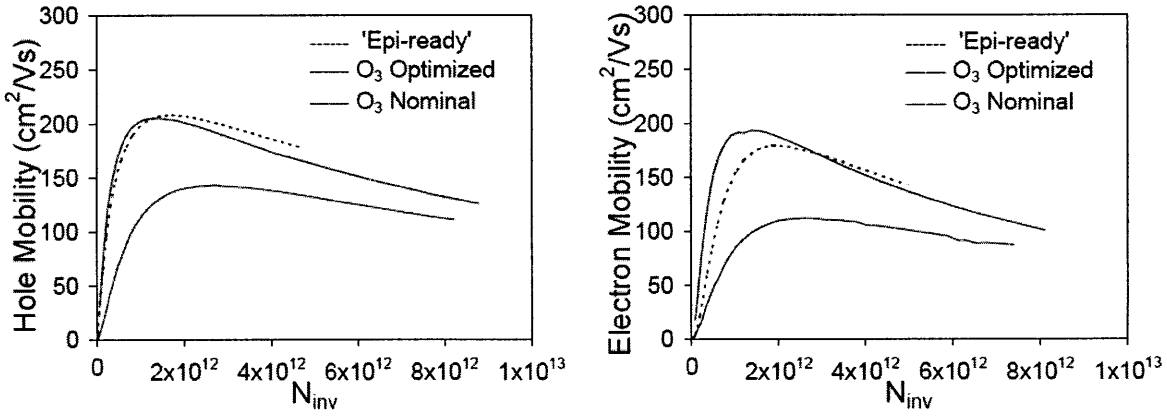

Figure 3.11. Effective carrier mobility (split-CV) for Ge p- and n-MOSFETs receiving the optimized O_3 surface treatment. For comparison the 'epi-ready' devices of Figure 2.8 and the nominal O_3-treated devices of Figure 3.3 are also shown.

XPS analysis was performed on Ge substrates receiving the optimized O_3 treatment in order to gain more understanding about the chemical nature of the resulting interfacial layer. Samples were capped with 1 nm Al_2O_3 in order to protect the surface configuration during ex-situ analysis, but still allow for a strong enough signal from the interface. The samples also received a 500 °C RTA in N_2 for 1 min in order to approximate the thermal budget of the full MOSFET process flow. The resulting

Ge-related spectra are shown in Figure 3.12 for untreated (standard wet clean only) and O_3-treated samples. Decomposition of the Ge3d and Ge2p (more surface sensitive) peaks reveals that the O_3 treatment results in an interfacial layer that contains a higher relative concentration of GeO_2 to other sub-oxides. It is noted that the total contribution from other sub-oxides (compared to the Ge substrate signature) appears relatively unchanged by the O_3 treatment; the dominant effect is an increase in GeO_2. As discussed in Chapter 1, this is consistent with the observations of other groups on the beneficial nature of GeO_2 with respect to D_{it} reduction.

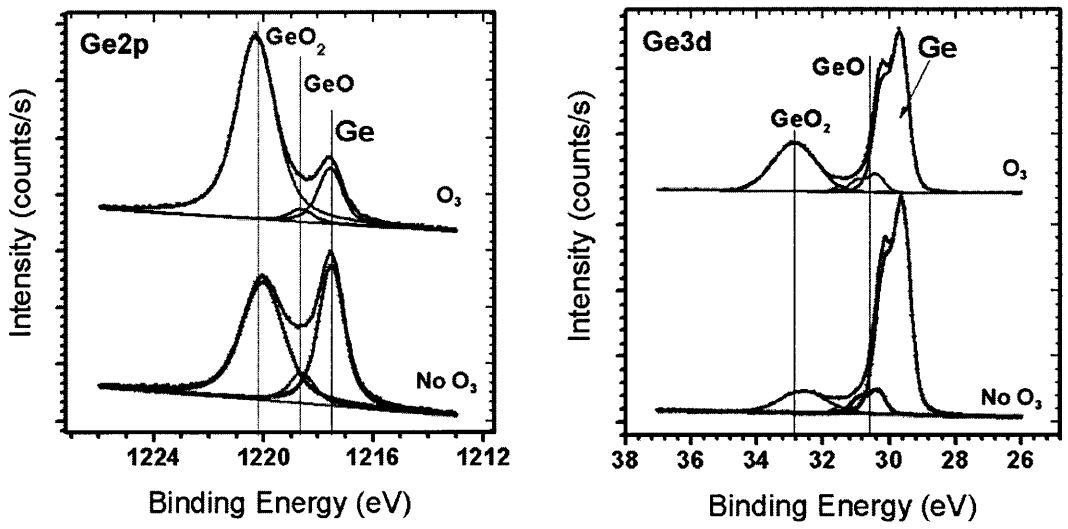

Figure 3.12. Germanium XPS spectra for untreated and O_3-treated substrates. [R. Contreras, M. Milojevic and R.M. Wallace (UT Dallas)]

3.5 Alternate Gate Dielectrics

As discussed in Section 2.1, the majority of the devices investigated in this thesis involve the use of Al_2O_3 gate dielectrics due to the superiority of their as-deposited behavior on

Ge. However, the use of materials with a higher dielectric constant, such as HfO_2, is more desirable from the standpoint of aggressively scaled equivalent oxide thickness (EOT). As illustrated in Figure 3.13, the C-V characteristics of HfO_2 on p-type Ge can be greatly improved using the O_3 treatment discussed in this chapter. Qualitative inspection of the C-V, as well as calculations of midgap D_{it} compare favorably to the results of O_3-treated substrates with Al_2O_3 gates.

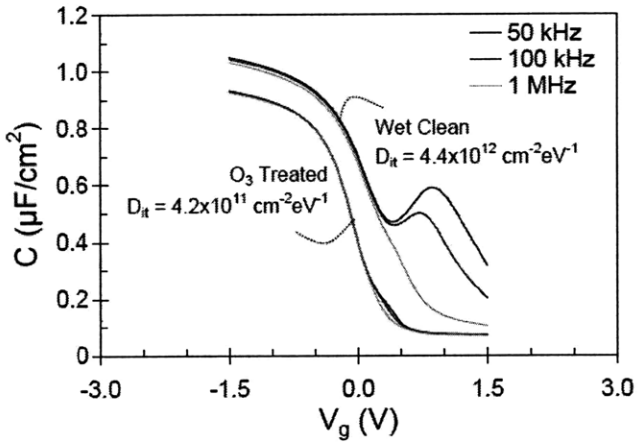

Figure 3.13. C-V characteristics of ALD HfO_2 on O_3-treated p-type Ge substrates and the corresponding minimum midgap D_{it} as calculated by the conductance method. These samples were fabricated with WN gate metal and a final 400 °C furnace anneal in N_2 for 30 min.

Long channel p- and n-MOSFETs were fabricated with the optimized O_3 surface treatment process described in the previous section, and an ALD WN/HfO_2 gate stack. The HfO_2 was deposited with tetrakis(ethylmethylamido)hafnium and water as the ALD precursors at a chamber temperature of 200 °C. The details of the ALD recipe can be found in Appendix B. Figure 3.14 shows the calculated carrier mobilities for the devices in this study. Once again, O_3-treated devices show substantial mobility enhancement over untreated devices with dramatic improvement observed in the n-channel devices. The

O_3-treated devices were fabricated with two different physical thickness of HfO_2, and show little corresponding thickness dependence on either hole or electron mobility.

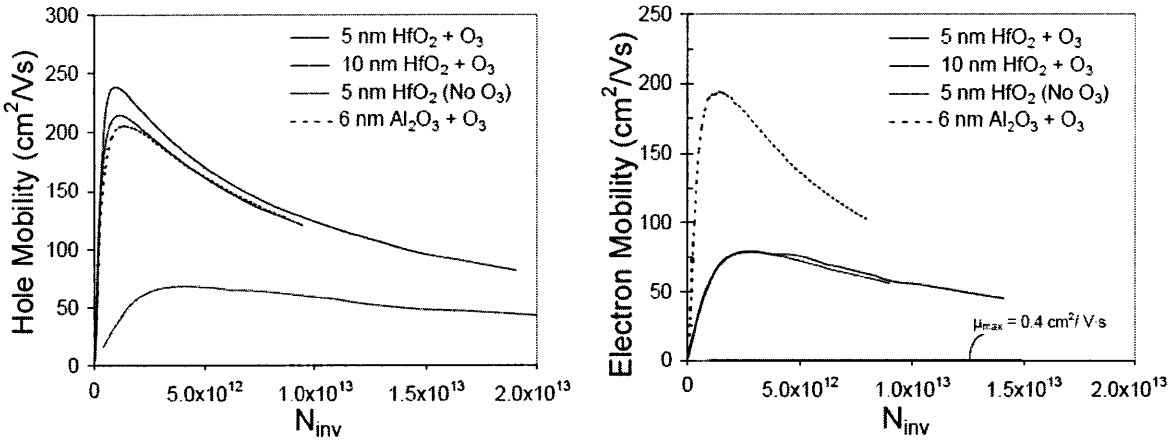

Figure 3.14. Effective hole and electron mobility for ALD WN / HfO_2 gate stacks on O_3-treated Ge. For comparison the dashed lines show the effective mobilities for the Al_2O_3 MOSFETs of Figure 3.11.

The untreated HfO_2 p-FET device is observed to have a lower mobility than an untreated Al_2O_3 device (see Figure 3.3), which one may expect based on the D_{it} calculations made in Chapter 2. However, the O_3-treated HfO_2 p-FET shows a mobility as good or better than the O_3-treated Al_2O_3 p-FET. This suggests that for the case of hole transport, the O_3 passivation layer is able to dominate the interface characteristics relatively independent of the choice of dielectric. A similar comparison of HfO_2 and Al_2O_3 n-FET devices is not as favorable, showing lower electron mobilities for both the untreated and O_3-treated devices. As indicated in Figure 3.15, a similar trend is observed when comparing the subthreshold swing of the HfO_2 and Al_2O_3 devices. The p-FET devices show similar values for both dielectrics, while the n-FET HfO_2 devices have slightly worse swing.

Nonetheless, HfO_2 is a better option for reduced EOT gate stacks because of its higher dielectric constant ($\kappa \sim 20$ vs. ~11 for Al_2O_3). Figure 3.16 shows the inversion side split-CV for the untreated and O_3-treated p-FETs that have a 5 nm physical thickness, along with best-fit ideal C-V curves. The ideal curves were calculated with Schred [51], a Schrodinger-Poisson solver that was modified with the band parameters and physical constants of germanium. The fits suggest an EOT of 0.8 and 1.1 nm for the untreated and O_3-treated devices, respectively. This is consistent with the observed EOT offset in the Al_2O_3 devices discussed earlier in this chapter. Gate leakage measurements were made on these devices in order to assess the possibility of further t_{ox} scaling. As shown in Figure 3.17, gate leakage currents lower than 50 $\mu A/cm^2$ at $|V_t + 1\ V|$ were observed in the 5 nm devices, the lowest reported value for a similar EOT gate stack on Ge [24].

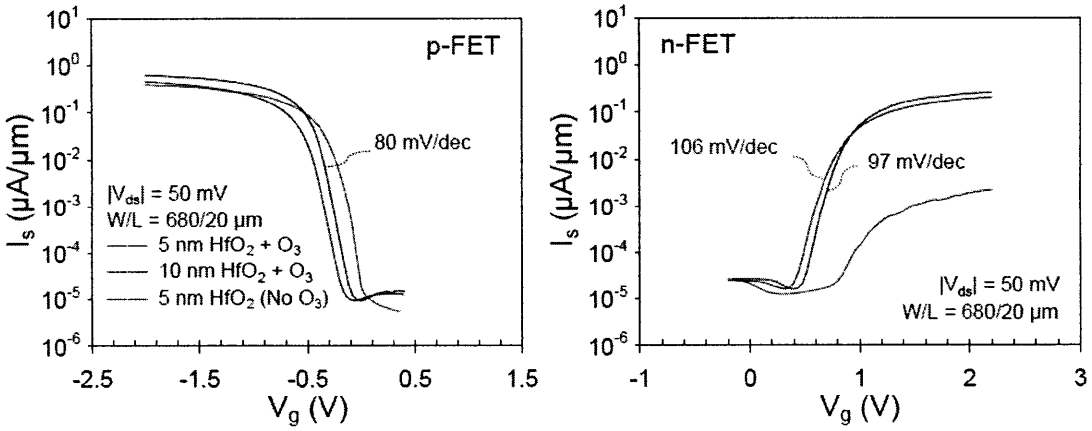

Figure 3.15. I_s-V_g characteristics for Ge p- and n-MOSFETs with ALD HfO_2 gate dielectrics.

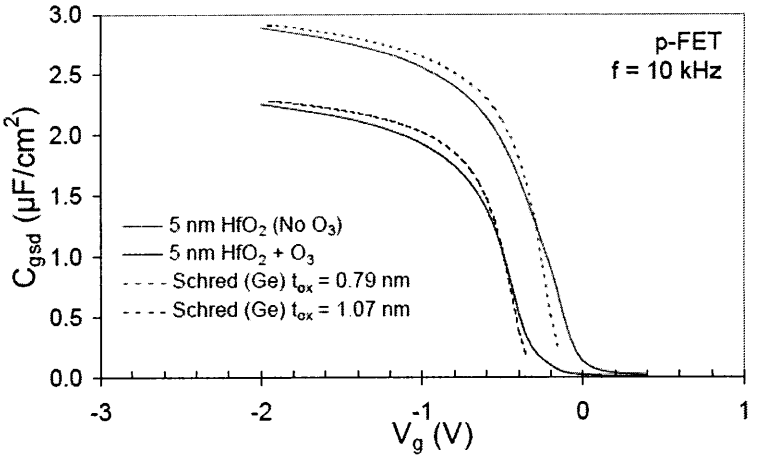

Figure 3.16. Inversion side split-CV measurements on the 5nm HfO_2 p-FETs and the corresponding Schrodinger-Poisson fit.

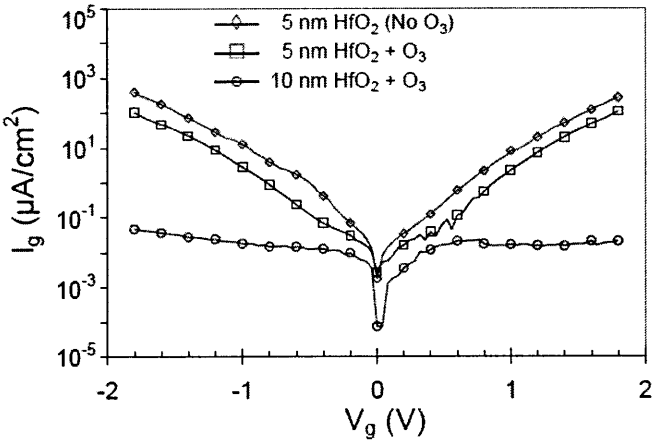

Figure 3.17. Typical gate leakage for Ge p-FETs receiving the O_3 surface treatment with 5 nm or 10 nm ALD HfO_2 gate dielectric.

3.6 Chapter Summary

Ozone surface passivation was observed to result in D_{it} reductions and increased carrier mobility, much like the 'epi-ready devices discussed in Chapter 2. A thorough optimization of the O_3 treatment resulted in additional mobility gains, with a performance that closely matches the best 'epi-ready' devices, but with less impact on the total EOT of

the gate stack. XPS measurements on O_3-treated substrates show that the dominant component of the passivation layer is GeO_2. Similar to claims presented in Chapter 2 regarding the native oxide passivation layer, it is speculated that the thermal stability of the O_3 passivation layer is protected by its formation and subsequent in-situ capping at low temperature. Additional analysis of the thermal stability of this surface treatment is presented in Appendix B, and suggests that the O_3 passivation layer is more stable at typical source/drain annealing temperatures than other reported techniques for forming GeO_2.

The optimization of the O_3 process seems to suggest that the addition of NO_x species (which reduces the O_3 concentration) is beneficial in terms of further reductions in D_{it}. The experimental evidence also implies that this D_{it} reduction is not due to the reduced O_3 concentration, and that some combination of O_3 and NO_x is most desirable.

Additionally, this O_3 passivation technique is observed to be effective for two ALD materials. MOSFETs fabricated with HfO_2 gates and the O_3 surface treatment exhibit hole mobility that is very similar to the Al_2O_3 devices but with slightly degraded electron mobility. Devices are demonstrated with near 1 nm EOT and low gate leakage.

Chapter 4 - Effect of n-type Channel Implants

4.1 Introduction

Previous work at MIT has demonstrated that phosphorus implanted n-FET devices exhibit enhanced mobility and improved subthreshold swing for increasing P dose [52]. The goal of this previous experiment was to fabricate buried-channel like devices in order to demonstrate that high electron mobilities could be obtained if the inversion layer centroid was moved away from the gate interface. Devices in this study receiving a $1x10^{13}$ cm^{-2} dose implant of phosphorus do show significant buried channel behavior, but also dramatic improvement in carrier mobility as shown in Figure 4.1. Interestingly, the devices receiving lower doses show no buried channel characteristics or evidence of reduced effective field operation, but still show substantial mobility enhancement as highlighted in the inset of Figure 4.1. This enhancement suggested that phosphorus may be accumulating at the gate interface and passivating interface states [29].

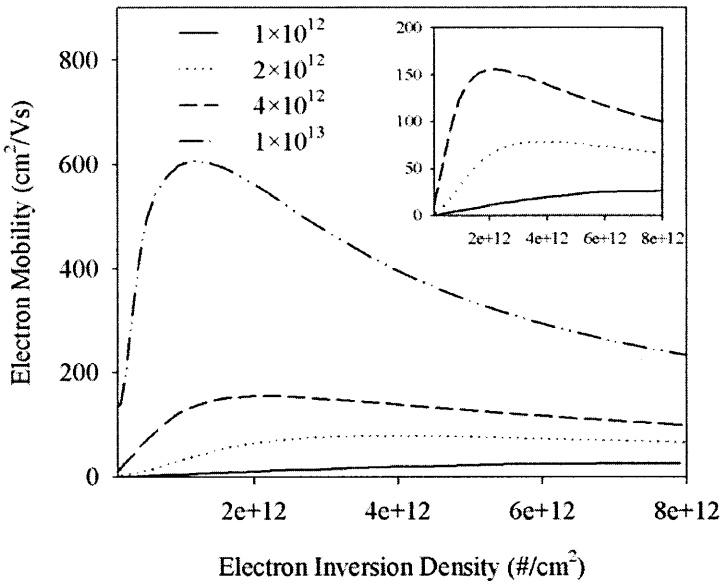

Figure 4.1. Effective electron mobility for phosphorus implanted Ge n-FETs [52].

In this chapter the impact of phosphorus implantation in combination with the ozone surface treatment will be investigated first. Subsequent experiments also investigated the impact of arsenic and antimony channel implants. The initial process flow for these experiments is summarized in Table 4.1. Although the target screen oxide thickness was 11 nm, there was significant variation in the final thickness due to difficulty in controlling the deposition rate on the small diameter wafers used in this work. The primary impact of this variation is expected to be in modulation of the relative dose of the implant, as more of the implanted dose will be stopped in the screen oxide if the screen oxide itself is thicker. Figure 4.2 indicates that this variation is likely mitigated for the As and Sb implanted device lots as their larger mass and higher implant energy results in less straggle and less as-implanted dose in the screen oxide.

Table 4.1. Initial process flow for n-type channel implanted MOSFETs. Following step 5, the MOSFET is completed as in Table 2.3.

Step	Process	Description
1	Pre-LTO clean	5:1 H_2O:HCl 5 min, 5:1:1 H_2O:NH_4OH:H_2O_2 30 s, 5:1 H_2O:HCl 10 min
2	Screen Oxide Deposition	11 nm (target) LPCVD SiO_2
3	Ion-implant	Various n-type species
4	Implant activation	600 °C N_2 RTA 60 s
5	Screen removal and pre-gate clean	50:1 H_2O:HF, 5:1 HCl 5 min

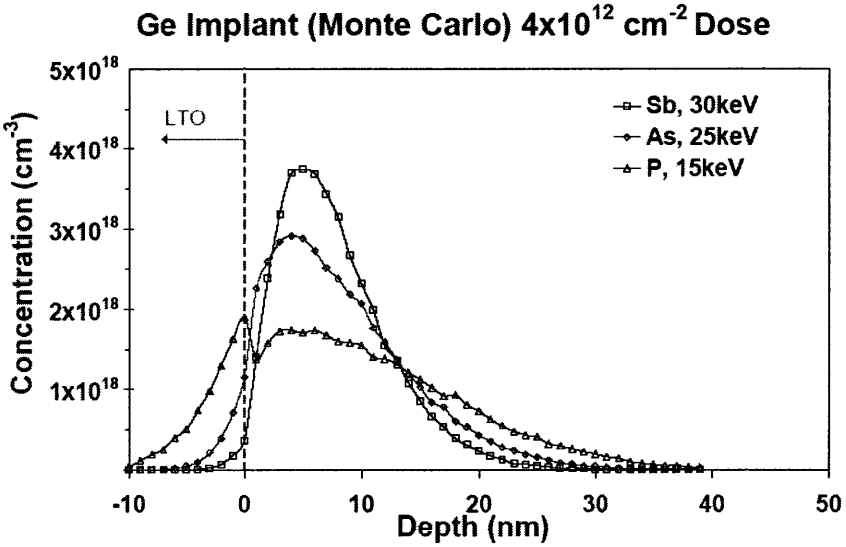

Figure 4.2. Monte Carlo simulation (TRIM [53]) of the as-implanted concentrations of the n-type species investigated in this work.

Table 4.2. Experimental summary for the study of n-type channel implants in Ge MOSFETs.

LOT ID	*Screen Oxide Thickness*	*Species, Dose, Energy*	*Primary Experimental Goals*
A	22 nm, 14 nm (thin)	P, $1x10^{12}$ cm^{-2}, 10 keV P, $4x10^{12}$ cm^{-2}, 15 keV	Impact of phosphorus + ozone for Ge n-FET, phosphorus impact on p-FET [nominal O_3 process]
B	11 nm	As, $1x10^{12}$ cm^{-2}, 25 keV As, $4x10^{12}$ cm^{-2}, 25 keV Sb, $1x10^{12}$ cm^{-2}, 30 keV Sb, $4x10^{12}$ cm^{-2}, 30 keV	Impact of other n-type species on Ge n-FET [nominal O_3 process]
C	13 nm	Sb, $1x10^{12}$ cm^{-2}, 30 keV Sb, $2x10^{12}$ cm^{-2}, 30 keV Sb, $4x10^{12}$ cm^{-2}, 30 keV	Re-investigation of p-FET phenomena, impact of implant activation temperature [optimal O_3 process]

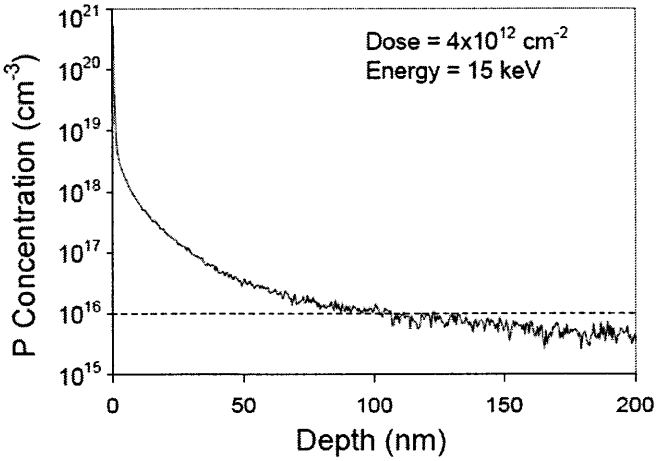

Figure 4.3. Secondary ion mass spectroscopy (SIMS) profile of ion-implanted P in Ge, dashed line indicates approximate substrate doping (p-type, Ga). The implant was performed through a 14 nm LTO screen oxide (equivalent to the thin lot A device). Sample received the full thermal budget of the complete MOSFET process flow.

4.2 Phosphorus Channel Implant with Ozone Surface Treatment

Long channel ring-FETs were fabricated on p- and n-type Ge substrates (Sb: 0.16-0.22 Ω-cm, Ga: 0.42-0.46 Ω-cm). The devices were fabricated with same process flow and 6 nm ALD Al_2O_3 gate dielectric as the devices described in Section 3.3 (un-optimized O_3 process). As in the previous experiment, Ge n-FETs show enhanced electron mobility for increasing dose of phosphorus as shown in Figure 4.1. Implanted devices show no change in subthreshold swing (see Figure 5.6) and no evidence of buried channel operation, suggesting that a reduction in interface state density may be responsible for the improved mobility. A more detailed discussion of the measured characteristics of the devices in lot A will follow in Chapter 5.

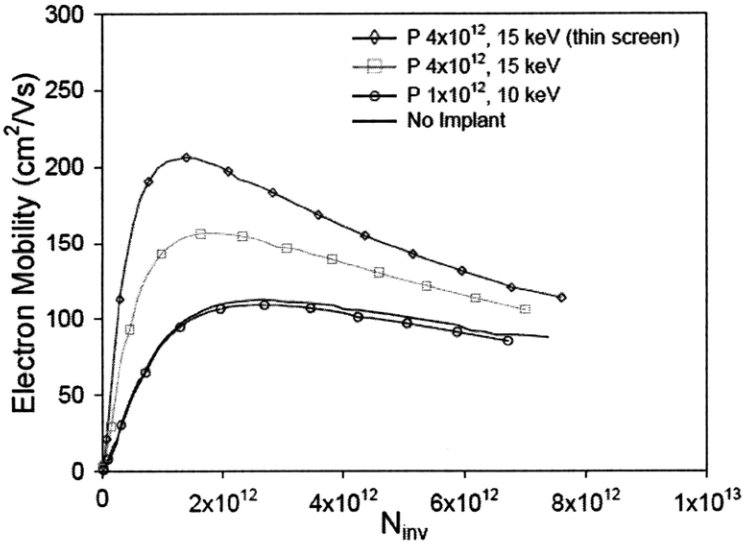

Figure 4.4. Effective electron mobility (split-CV) for Ge n-MOSFETs (lot A) receiving channel implants of phosphorus in addition to the O3 surface treatment (un-optimized)

4.3 Arsenic and Antimony Implantation

The lot B experiment investigated channel implants of arsenic and antimony as detailed in Table 4.2. Long channel ring-FETs were fabricated on p-type Ge substrates with the same ALD 40nm WN / 6 nm Al_2O_3 gate stack used in the lot A experiment, and again using the nominal O_3 treatment discussed in Section 3.4. It is assumed that the effective implanted dose in this experiment is higher than the lot A devices due to the thinner screen oxide used. Figure 4.5 shows the effective electron mobility for devices receiving two different doses of either As or Sb, indicating that they behave similarly. Even higher mobility enhancements are observed in this case, with the higher dose devices displaying higher-than-Si mobility at low inversion charge number density, N_{inv}. As shown in Figure 4.6, the higher dose devices do show some buried channel characteristics, as evident in the degraded subthreshold swing and C-V stretch-out compared to the lower-dose devices. This may account for some of the mobility enhancement at low N_{inv} as the inversion centroid forms further away from the gate interface. However a large mobility enhancement is still observed at high N_{inv} where even the $4x10^{12}$ devices become more surface-channel like (apparent from the similar value of $C_{gsd,max}$ in Figure 4.6). For comparison, the characteristics of the n-FET devices fabricated in the later lot C experiment are shown in Figure 4.7. These devices were fabricated with the same gate stack and very similar implant conditions (Sb only) as indicated in Table 4.2, and not surprisingly, show similar electron mobility as the lot B devices.

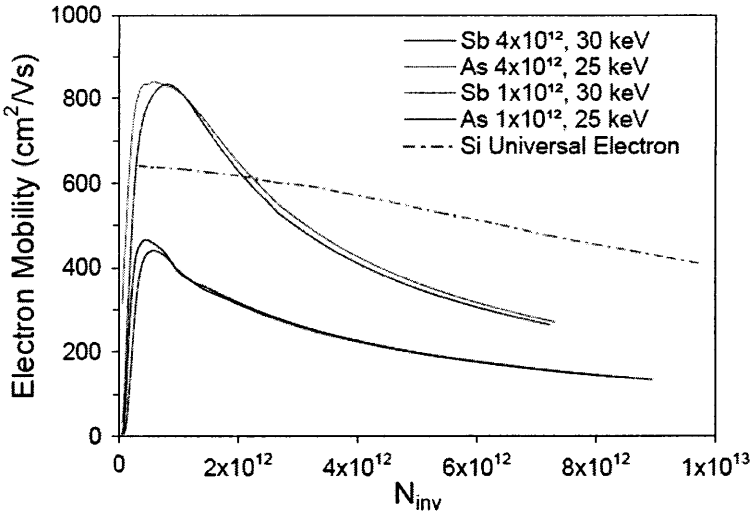

Figure 4.5. Effective electron mobility (split-CV) for Ge n-MOSFETs receiving channel implants of antimony and arsenic.

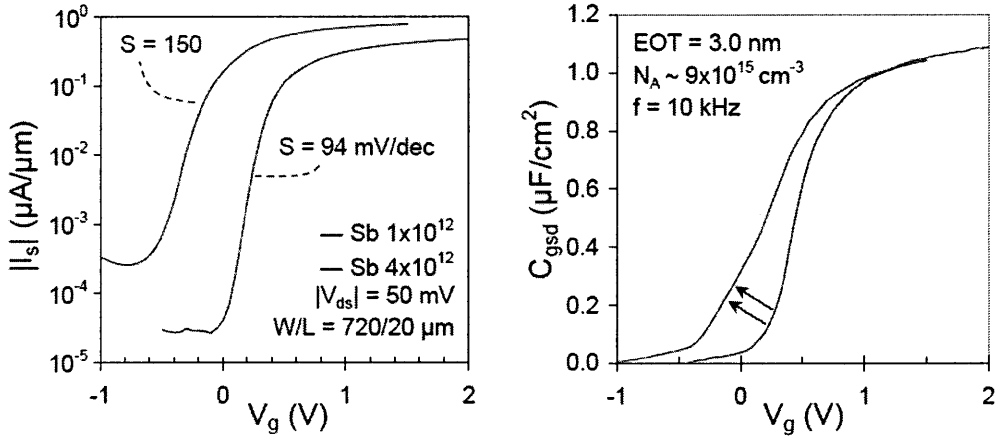

Figure 4.6. Typical Is-Vg and inversion-side C-V for the Sb implanted Ge n-FETs of lot B. The As implanted devices (not shown) behave similarly.

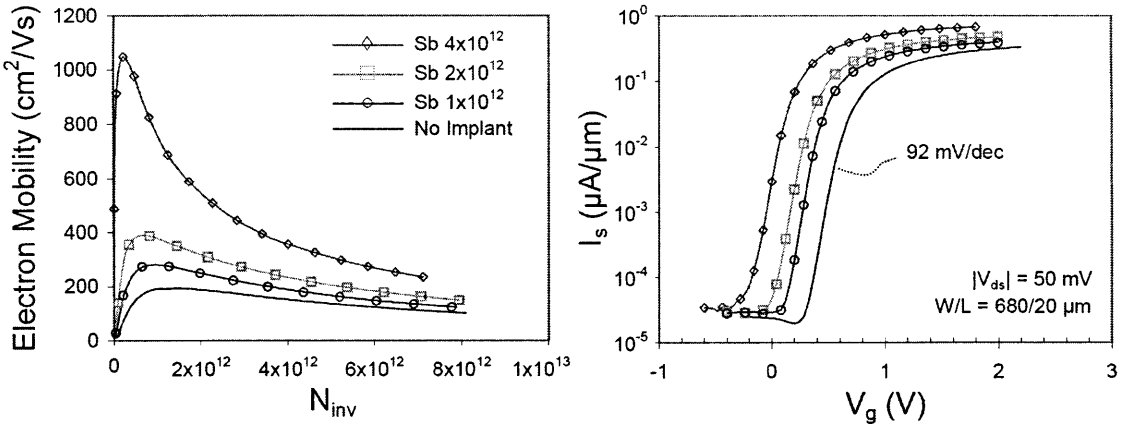

Figure 4.7. Effective electron mobility (split-CV) and the corresponding I_s-V_g curves for the Sb-implanted n-FETs of lot C. The measured CET of all devices is 3.9 nm.

This large mobility enhancement at high N_{inv} suggests a fundamental improvement in the quality of gate interface has occurred as a result of the n-type channel implant. In order gauge the influence of the implant on the Ge/high-k interface chemistry, XPS was performed on substrates receiving a $4x10^{12}$ cm^{-2} dose implant of Sb identical to the conditions in lot B. The analysis of the Ge related peaks is shown in Figure 4.8, and reveals no detectable change compared to a substrate receiving no implant (at least within the detection limits of XPS). Additionally, no Sb signature was evident, and no difference was observed in other peaks of interest (O1s, C1s, F1s). This is in contrast with the analysis of O_3-treated Ge discussed in Section 3.4, where significant changes in interfacial chemistry was observed. This implies that the mechanism for the mobility improvement is different in the case of the n-type implanted devices. Considerable evidence for improved interface quality and reduced D_{it} for these devices will be discussed in Chapter 5.

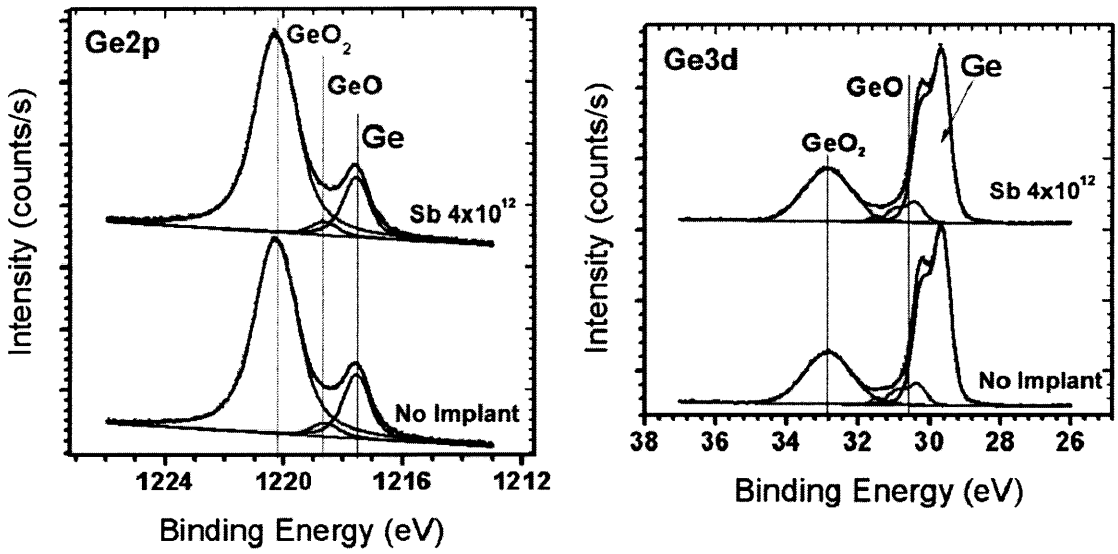

Figure 4.8. Germanium XPS spectra for samples receiving no implant and a $4x10^{12}$ cm^{-2} Sb implant. [R. Contreras, M. Milojevic and R.M. Wallace (UT Dallas)]

4.4 Impact on Germanium p-MOSFET

It was originally speculated by Ritenour et al. [52] that the observed mobility improvement in P-implanted Ge n-FETs could be the result of the suppression of some undesirable interfacial oxide. The XPS results presented in the previous section would imply this is not the case, and suggests the electron mobility enhancement is the result of a different mechanism. In order to gauge to impact of n-type dopant channel implants on hole transport, long channel Ge p-FETs were fabricated as part of the lot A and lot C experiments outlined in Table 4.2. The calculated hole mobilities for the lot A and lot C p-FETs are shown in Figure 4.9 and Figure 4.10, respectively. In contrast with the corresponding n-FET devices, no mobility enhancement is observed in the implanted p-

FET devices. In fact, slight mobility degradation is observed for P and Sb implanted devices that worsens for increasing implanted dose.

In this case, devices are fabricated on n-type substrates receiving an additional n-type channel implant, increasing the effective substrate doping concentration. In other words, these p-FET devices are operating at an increased effective field. In this light, the observed mobility degradation could be viewed as consistent with increased effective field operation. The actual effective field is difficult to estimate because the precise doping profile of the substrate is not known. Other methodologies for estimating the total depletion charge rely on knowledge of the flatband voltage, which is also difficult to estimate in the presence of significant interface trapping.

Nevertheless, it can be concluded that the n-type channel implants have no beneficial impact on hole transport. This again suggests that the nature of the observed electron mobility enhancement is not due to a passivation effect that is uniform across the Ge bandgap.

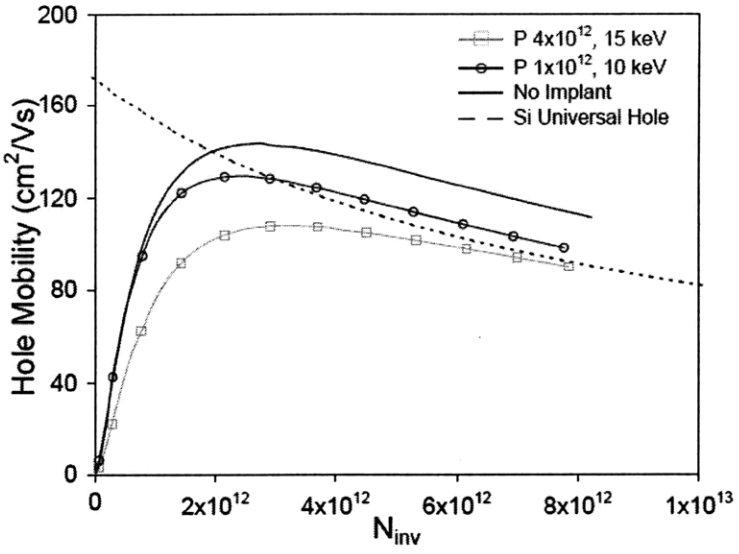

Figure 4.9. Effective hole mobility (split-CV) for Ge p-MOSFETs receiving channel implants of phosphorus (lot A).

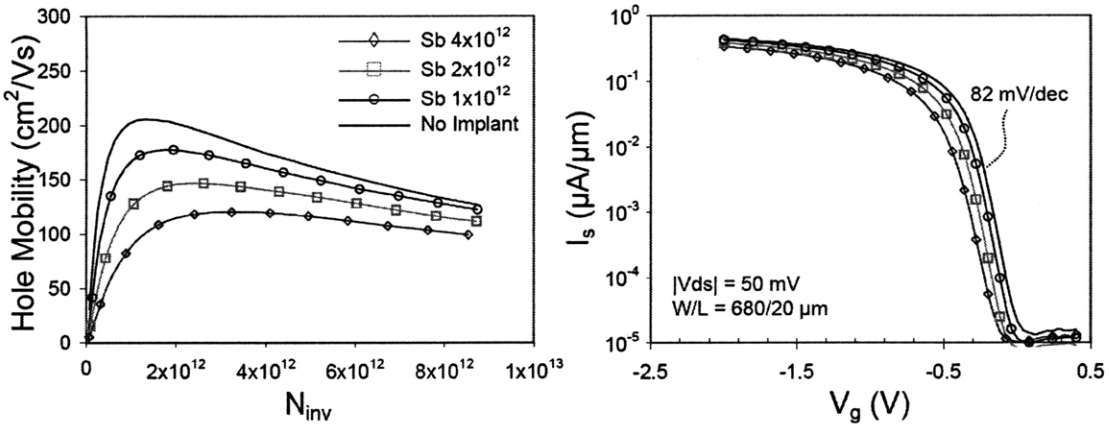

Figure 4.10. Effective hole mobility (split-CV) and corresponding Is-Vg characteristics for Ge p-FET devices receiving channel implants of antimony (lot C). The measured CET of all devices is 3.8 nm.

4.5 Chapter Summary

All n-type species investigated as channel implants prior to ALD gate stack deposition were observed to result in enhanced electron mobility in Ge n-FET devices. As and Sb implanted n-FETs exhibit electron mobility higher than Si for the first time, but degrade

at higher inversion densities. Ge p-FET devices implanted with P or Sb show degraded mobility compared to un-implanted devices, which is likely the result of increased effective field operation. This suggests that any electrical improvement to the Ge interface as a result of the n-type implant is energetically confined near the conduction band. This claim is investigated in more detail in the following chapter.

Chapter 5 - Improved Interface Characteristics for n-type Dopant Implanted Germanium n-MOSFETs

5.1 Introduction

In the previous chapter, results were presented that indicated significant electron mobility enhancements in Ge n-MOSFETs could be obtained through the use of n-type channel implants. These enhancements were largest at low inversion density, but even for inversion densities up to $8x10^{12}$ cm^{-2}, the mobility for the best performing devices was more than two times higher than for un-implanted devices (see Figure 4.5). This suggests that the mobility enhancements cannot be solely attributed to reduced effective field operation. Evidence will be presented in this chapter that n-type implants improve the electrical quality of the Ge-dielectric interface primarily through the reduction of trap states near the conduction band edge.

5.2 Substrate Bias Response

The application of a reverse bias between the source and the substrate increases the amount of depletion charge at a given gate bias and therefore increases the threshold voltage. It also pushes the average distance of the inversion charge distribution centroid closer to the gate interface, due to the increased magnitude of the electric field near the semiconductor surface. This effect can be exploited to compare the channel-implanted devices (particularly those that display buried-channel behavior) with un-implanted devices at an equivalent centroid distance. The concept of inversion centroid is illustrated

in Figure 5.1 via simulation of the electron concentration in a Ge n-MOSFET (Sentaurus^{TM} Device Simulator). The classical solution to Poisson's Equation for the electron concentration in the channel of a MOSFET yields a density profile that is peaked at the gate interface. A more accurate solution considering the quantum confinement of carriers in the 2D electron gas yields a profile that is peaked away from the interface and has a larger centroid. This more accurate solution is obtained by simultaneously solving Poisson's Equation coupled with Schrodinger's Equation to capture quantum effects. It is this increased centroid that leads to the discrepancy between the capacitance equivalent thickness (CET) and equivalent oxide thickness (EOT), particularly for thin gates.

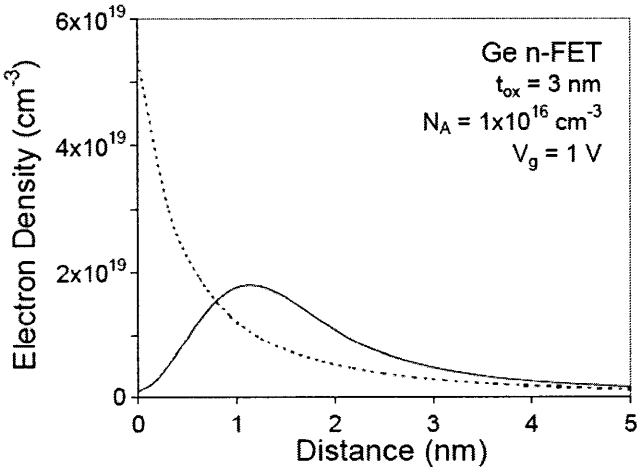

Figure 5.1. Sentaurus^{TM} simulation of electron density vs. vertical distance away from the gate interface for the classical case (dashed) and considering quantum confinement of the inversion charge (solid).

Figure 5.2 shows source current vs. gate voltage, I_s-Vg characteristics for un-implanted and implanted n-FET devices at varying substrate bias. The effect of the substrate can be seen to increase V_t in both devices and also to degrade I_s at high gate overdrive. Also, the 4x10^{12} implanted device shows improving subthreshold swing as the

buried-channel behavior becomes suppressed due to the shift in the inversion centroid. At approximately V_{sb} = -1 V, the $4x10^{12}$ device shows a subthreshold swing that is roughly equivalent to un-implanted device with no substrate bias. At this substrate bias (and larger), the implanted device maintains a significantly higher I_s than the un-implanted device, and also shows less overall degradation in I_s as a function of substrate bias. This is more clearly evident in Figure 5.3 where the effective mobility of these same devices is shown for different substrate biases. Even at a substrate bias of -2 V, the implanted device maintains more than 2x mobility relative to an un-implanted device at high N_{inv}.

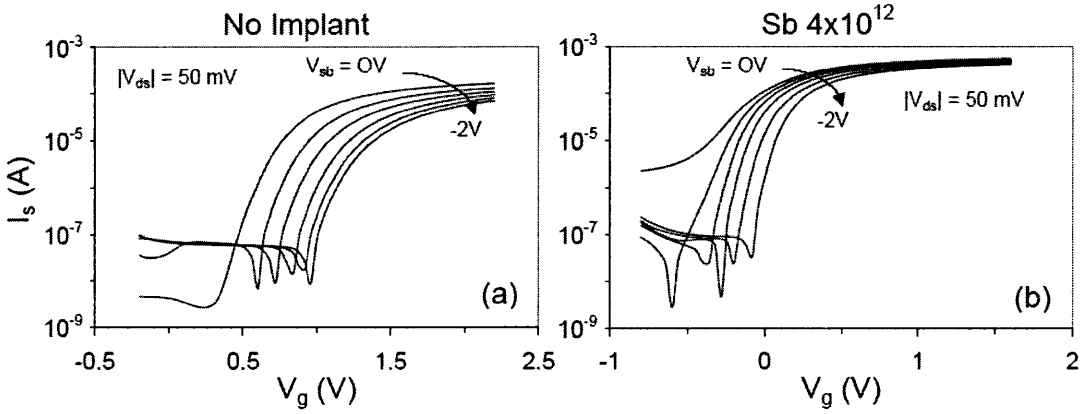

Figure 5.2. Is-Vg characteristics for (a) un-implanted and (b) Sb-implanted Ge n-FETs (lot B) at various substrate biases.

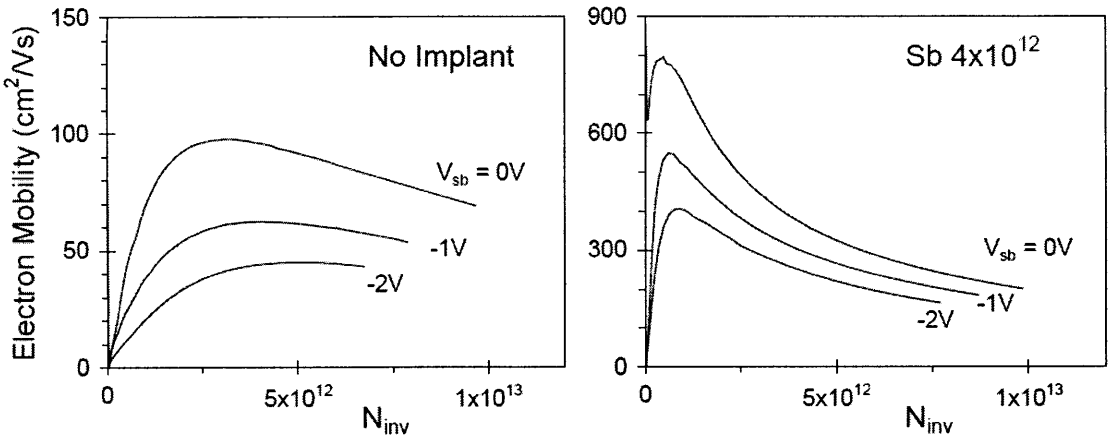

Figure 5.3. Effective electron mobility (split-CV) as a function of substrate bias for un-implanted and Sb-implanted Ge n-FET devices (lot B).

A similar analysis was performed on the p-FET and n-FET devices of lot C. Figure 5.4a shows the relative change in I_s for both un-implanted and Sb-implanted devices at a constant gate overdrive. In other words this is the measured I_s independent of the actual threshold voltage (V_t) of each device and independent of the increase in V_t caused by the application of a substrate bias. In this case V_t is defined by the linear extrapolation of the measured I_s-V_g curve at $|V_{ds}|$ = 50 mV. The actual I_s for each device is shown in Figure 5.4b.

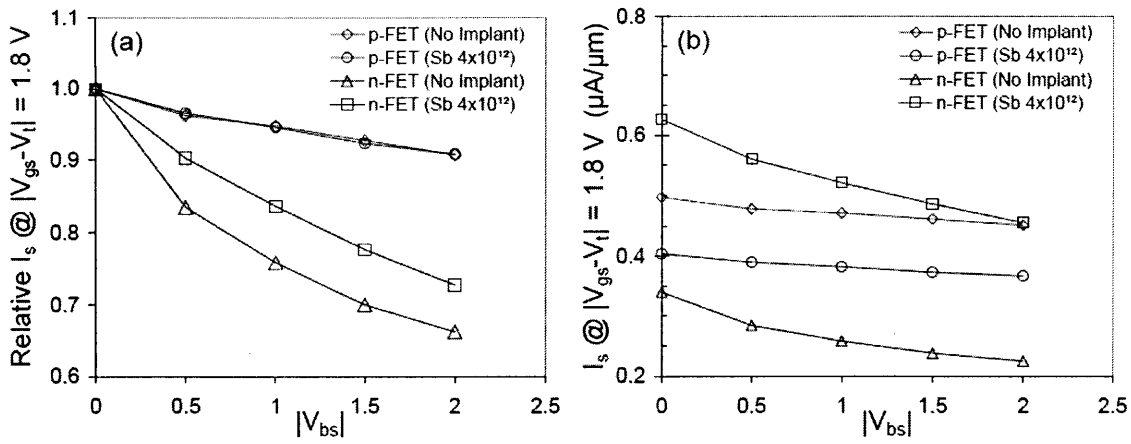

Figure 5.4. (a) Relative change in I_s ($|V_{ds}|$ = 50 mV) at a constant gate overdrive for the p-FET and n-FET devices of lot C and (b) the corresponding actual I_s at the same gate overdrive.

Of note is the large difference in the degradation of the p-FET devices compared to the n-FET devices, illustrating the superiority of the interface as it relates to hole transport. The implanted n-FET device has a higher actual drive current than the un-implanted device, but is also less severely degraded with application of substrate bias, suggesting a fundamental improvement in the quality of the interface for electrons. However, the relative change in current for the implanted p-FET device is nearly identical to un-implanted device, suggesting that improvement in the interface is energetically confined near the conduction band.

A simulation study was undertaken in order to verify that these qualitative claims regarding centroid modulation are consistent with theory. A Schrodinger-Poisson calculation of the inversion centroid in Ge was performed with the Sentaurus^{TM} device simulator using Ge band parameters. The average distance of the inversion centroid versus both inversion density and calculated vertical effective field is plotted in Figure 5.5. The implanted device was assumed to have a $4x10^{12}$ cm^{-2} dose implant peaked at the interface with a depth that roughly matches the SIMS profile in Figure 4.3. As expected,

the centroid distance is indeed larger for the implanted case when no substrate bias is applied. However with the application of V_{bs} = 2 V, the centroid distance becomes nearly equivalent to un-implanted case.

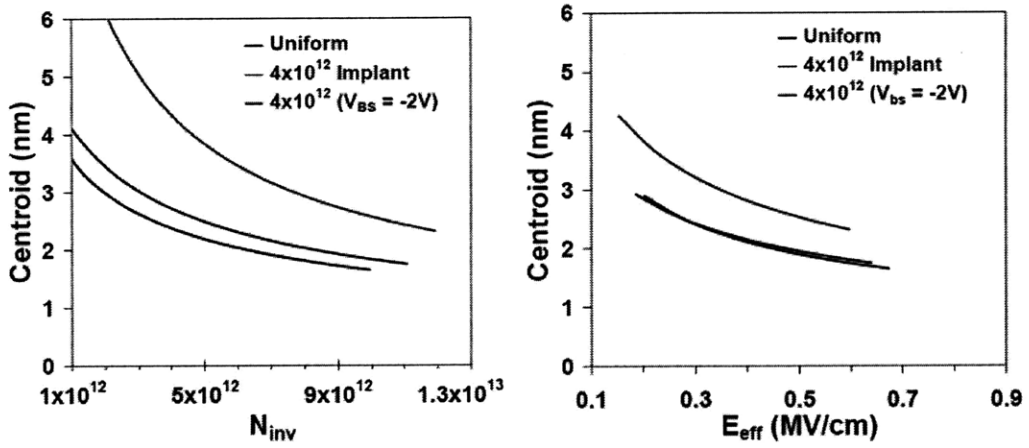

Figure 5.5. Simulation of inversion centroid in Ge for a uniformly doped substrate vs. an n-type implanted substrate with and without an applied substrate bias. A doping level of $N_A = 1x10^{16}$ cm^{-3} was assumed.

5.3 Threshold Voltage Behavior

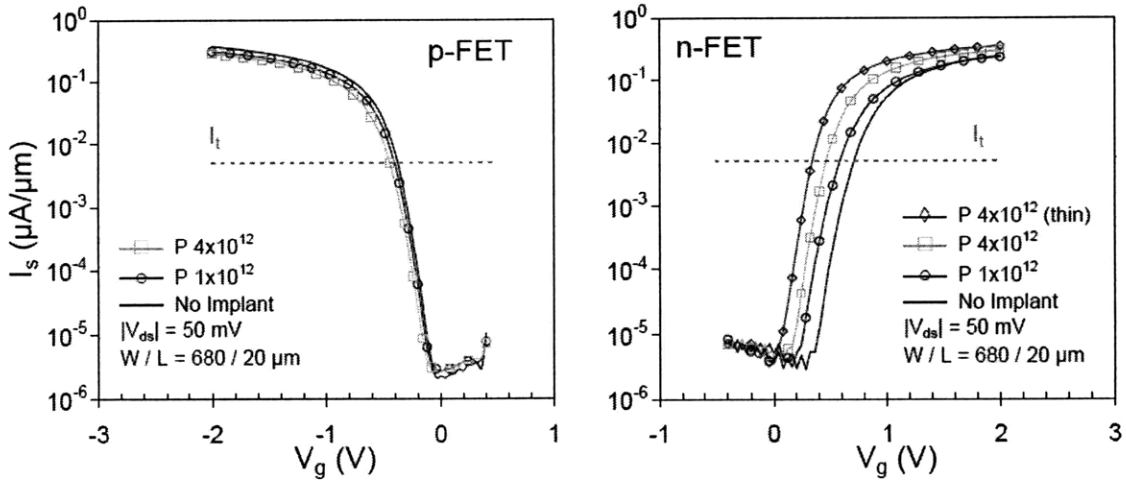

Figure 5.6. Measured I_s-V_g characteristics for the phosphorus implanted Ge MOSFETs in lot A.

Inspection of the I_s-V_g data in Figure 5.6 shows that while the n-FET devices of lot A show large shifts in V_t for increasing phosphorus dose, the corresponding p-FET devices show very little shift. It should be noted that the extracted value of V_t from I_s-V_g curves may vary depending on the choice of extraction method [48]. The simplest method is to specify a value of source or drain current and define the corresponding gate voltage as V_t, often referred to as the constant current method. This current value is somewhat arbitrary, but is often taken as $I_t = (W/L)\cdot 1x10^{-7}$ A [54]. For the device geometries used in this work, this corresponds to a width-normalized source current of $5x10^{-3}$ μA/μm, as labeled in Figure 5.7. A more common definition of V_t is the V_g-intercept in the linear extrapolation of I_s at low V_{ds} (see Figure 5.7). This may result in a different numerical value of V_t than the constant current method (or other methods), however in this chapter emphasis will placed on the measured shift in V_t values, which is expected to be less sensitive to the choice of extraction method.

For example, this excess V_t shift is even more apparent in the n-FET devices of lot B. As indicated in Figure 5.7, the observed shift in the extrapolated V_t (relative to an un-implanted device) for the device receiving a $1x10^{12}$ cm^{-2} Sb implant is approximately 340 mV. Using the constant current definition of V_t described above, the same shift is calculated as 400 mV. Interestingly, either value is larger than the maximum shift one could expect assuming the full dose as-implanted was present, active, and completely confined to the interface. In this limiting case the expected shift would be:

$$\Delta V_t = \frac{qD}{C_{ox}} = \frac{q(1x10^{12}\,cm^{-2})}{1\mu F/cm^2} = 160mV \qquad (3)$$

where q is the elementary charge, D is the implanted dose, and C_{ox} is the oxide capacitance. From the SIMS profile in Figure 4.3 it is clear that the implant profile extends at least 50 nm into the substrate, and it is also likely that some dopant loss into the screen oxide occurs during the activation anneal, both of which would reduce the expected shift in V_t from this maximum value.

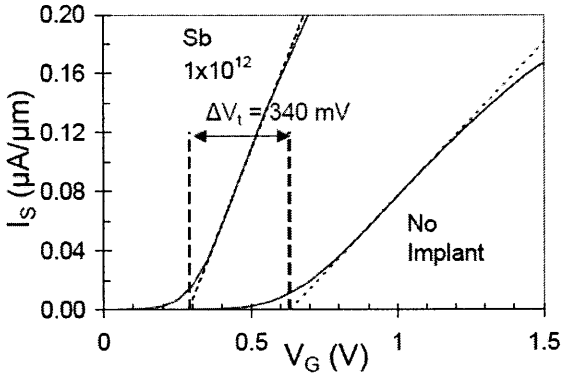

Figure 5.7. Observed shift in the linearly extrapolated threshold voltage for a $1x10^{12}$ cm^{-2} implantation of Sb in a Ge n-FET.

A more detailed analysis was performed on the n-FET and p-FET devices of lot C, which were also processed with a thinner screen oxide than the phosphorus implanted devices of lot A. The extrapolated V_t for all devices is summarized in Table 5.1. Once again, for the $1x10^{12}$ cm^{-2} dose n-FET the observed V_t shift is greater than could be predicted by the limiting case discussed above. A measurable V_t shift is now apparent in the p-FET devices, yet in every case the identically implanted n-FET shows a far greater shift. This additional shift could be attributed to a reduction of acceptor-like trap states. An acceptor trap in the upper half on the bandgap becomes negatively charged when occupied by an electron. This negative charge would otherwise result in a higher

threshold voltage for n-FET devices and degrade mobility through increased Coulomb scattering.

Table 5.1. Extrapolated threshold voltage from linear I_s-V_g characteristics for all lot C devices.

	$V_{t,PMOS}$ (V)	$\Delta V_{t,P}$ (V)	$V_{t,NMOS}$ (V)	$\Delta V_{t,N}$ (V)	$V_{t,N} - V_{t,P}$ (V)
No Implant	-0.28	*0*	0.59	*0*	0.87
Sb $1x10^{12}$ cm^{-2}	-0.32	*-0.04*	0.39	*-0.20*	0.71
Sb $2x10^{12}$ cm^{-2}	-0.37	*-0.09*	0.29	*-0.30*	0.66
Sb $4x10^{12}$ cm^{-2}	-0.46	*-0.18*	0.10	*-0.49*	0.56

In the absence of an applied back bias, the threshold voltage of a N(P)MOSFET with a uniform doping profile can be approximated by [55]:

$$V_{tN(P)} = V_{FB} + (-)\frac{2kT}{q}\ln\left[\frac{N_{A(D)}}{n_i}\right] + (-)\frac{\sqrt{2q\varepsilon_s N_{A(D)}}}{C_{ox}}\sqrt{\frac{2kT}{q}\ln\left[\frac{N_{A(D)}}{n_i}\right]} \quad (4)$$

where $N_{A(D)}$ is the substrate doping concentration, n_i is the intrinsic carrier concentration, ε_s is the semiconductor permittivity, and C_{ox} is the oxide capacitance. The flatband voltage, V_{FB} is given by [55]:

$$V_{FB} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_i}{C_{ox}} \quad (5)$$

where Φ_{MS} is the metal-semiconductor work function difference (Φ_M - Φ_S), and Q_f and Q_i are contribution from the fixed oxide charge and trapped interface charge, respectively.

The metal work function, Φ_M, of the WN produced by the ALD reaction used in this work has been reported elsewhere as 4.6 eV [56]. In the absence of any oxide fixed charge or interface-trapped charge, this value could be used to calculate ideal values of V_{tN} and V_{tP}. However, the quantity of oxide fixed charge is not known, and the large C-V

hysteresis and measured D_{it} values observed in this work imply that additional charge trapping may strongly impact V_{FB} (see Appendix D). Therefore, a fairer metric is the difference between V_{tN} and V_{tP}, which can be expressed, in the ideal case ($Q_i = 0$) as:

$$V_{tN} - V_{tP} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) + \frac{2\sqrt{kT\varepsilon_s}}{C_{ox}}\left[\sqrt{N_A \ln\left(\frac{N_A}{n_i}\right)} + \sqrt{N_D \ln\left(\frac{N_D}{n_i}\right)}\right] \quad (6)$$

which has no dependence on Φ_M or Q_f.

Using the un-implanted devices of lot C as an example ($N_A \approx N_D \approx 10^{16}$ cm^{-3}, $C_{ox} = 10^{-6}$ F/cm^2, $n_i = 2.4\text{x}10^{13}$ cm^{-2}), the ideal V_t difference calculated from Eq. 6 is $V_{tN} - V_{tP} = 0.40$ V. The actual measured V_t difference indicated in Table 5.1 is 0.87 V, far in excess of the ideal value. In this light, the excessive shift observed in the implanted n-FET devices can be viewed as consistent with reduced charge trapping, considering that V_{tN} - V_{tP} has been reduced. If one assumes that the excess difference in V_t for the un-implanted devices is due to trapped interface charge, Qi, then the density of that charge, D_{trap}, can be calculated as:

$$D_{trap} = \frac{Q_i}{q} = \frac{(\Delta V_{t,meas} - \Delta V_{t,ideal})C_{ox}}{q} \quad (7)$$

where $C_{ox} = 0.9$ μF/cm^2 for the lot C devices. This calculation yields a value for D_{trap} of $2.6\text{x}10^{12}$ cm^{-2}. The extent to which D_{trap} has been reduced for the implanted devices is difficult to assess because the exact doping profile is unknown and therefore the expected change in V_t is also unknown. However, in the next two sections low temperature measurements will be presented that suggest D_{it} near the conduction band edge has been reduced by a $4\text{x}10^{12}$ cm^{-2} n-type implant by approximately $7.7\text{x}10^{12}$ to $1.1\text{x}10^{13}$ cm^{-2}eV^{-1} depending on the technique used. For the portion of the Ge bandgap probed in these

techniques, this corresponds to a reduction in total trapped charge between $1.1x10^{12}$ and $1.7x10^{12}$ cm^{-2}, a large portion of the value for D_{trap} calculated above.

5.4 Low Temperature Characterization

A series of low temperature measurements were made on the As-implanted devices of lot B in order to provide further evidence for the reduction of interface-state density near the conduction band edge. Measurements were made with a liquid nitrogen cryostat from room temperature down to 80 K. A technique similar to the Gray-Brown method discussed in Chapter 3 compares the shift in threshold voltage as a function of temperature compared to the ideal amount expected [48][29]. Any additional shift in threshold voltage can then be attributed to increased charging of interface states that occurs as the Fermi level moves closer to E_C. This behavior is summarized in Figure 5.8 and shows a clear trend that is consistent with the mobility observations discussed in Chapter 4.

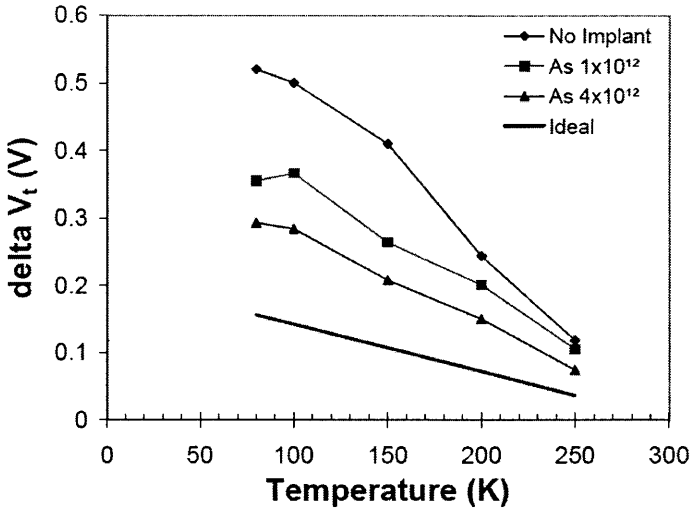

Figure 5.8. Threshold voltage shift as a function of temperature for Ge n-MOSFETs receiving As channel implants compared to an un-implanted device and the ideal case.

The interface state density can be calculated as:

$$D_{it} = \frac{(\Delta V_{t,meas} - \Delta V_{t,ideal})C_{ox}}{q\Delta E_F} \tag{8}$$

where $\Delta V_{t,meas}$ is the difference in the linearly extrapolated threshold voltage for a given change in temperature, and ΔE_F is the change in the position of the Fermi level (at inversion) over the same temperature range. As shown in Figure 5.9, this calculation yields an average value of D_{it} near the conduction band of 1.7×10^{13}, 9.6×10^{12}, and 6.1×10^{12} cm^{-2} eV^{-1} for the un-implanted, and 1×10^{12} cm^{-2}, and 4×10^{12} cm^{-2} implanted devices, respectively.

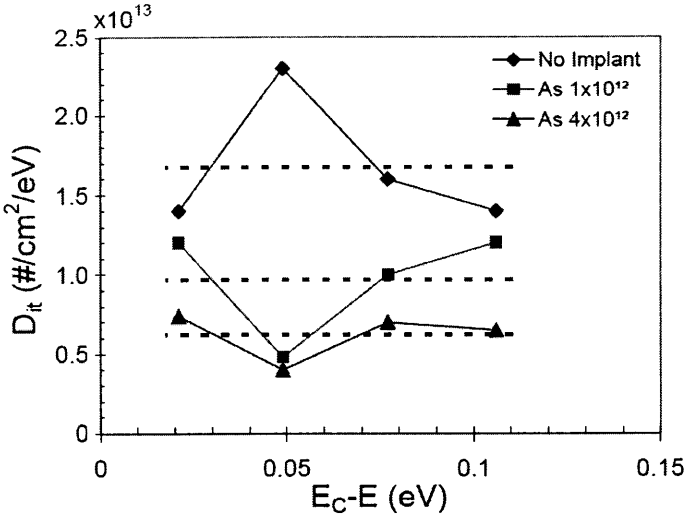

Figure 5.9. Interface state density near the conduction band edge calculated from the low temperature threshold voltage shift. Discrete points indicate calculated values of D_{it} for each step in temperature, while the dashed lines indicate the average of all values near E_C.

A similar analysis can be performed by measuring the change in subthreshold slope as a function of temperature. As a MOSFET turns on majority carriers can become trapped by interface states instead of contributing to the measured current. This becomes apparent as degradation in subthreshold swing, which can expressed as [48]:

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_D + C_{it}}{C_{ox}} \right) \tag{9}$$

where C_D is the capacitance of the depletion layer, C_{it} is the capacitance of charged interface states, and C_{ox} in the gate oxide capacitance. The interface state density can then be calculated by comparing the measured value of S to the ideal case where $C_{it} = 0$. Then, D_{it} can be expressed as [48]:

$$qD_{it} = C_{it} = \left[\frac{S_{meas}}{S_{ideal}} \left(1 + \frac{C_D}{C_{ox}} \right) - 1 \right] \frac{C_{ox}}{C_D} \tag{10}$$

Figure 5.10 again shows a trend in S that is consistent with the observed mobility. Calculating D_{it} from Eq. 10 for the measured S values at 80 K yields values of 1.3 $x10^{13}$, 9.0 $x10^{12}$, 5.3 $x10^{12}$ cm^{-2} eV^{-1} for the O_3-only, As-$1x10^{12}$, and As-$4x10^{12}$ devices, respectively. This is in good agreement with values of D_{it} calculated above by the V_t shift method. It is noted that the subthreshold swing of the implanted devices near room temperature is dominated by direct leakage from source to drain as a result of the over-compensated doping profile in the channel. This leakage is suppressed at lower temperatures, allowing the trap-limited swing to be measured.

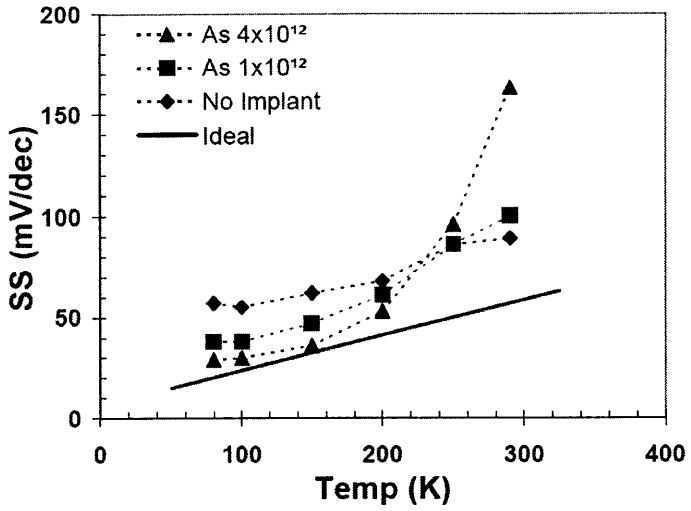

Figure 5.10. Subthreshold swing versus temperature for Ge n-MOSFETs receiving As channel implants.

5.5 Germanium MOS Capacitor Behavior

In order to quantify the impact of the n-type channel implant on fast traps near the conduction band, conductance measurements were made on n-type Ge MOS capacitors fabricated with identical conditions to the lot C MOSFETs described earlier in this chapter. Conductance measurements are possible on MOSFET structures [57][58], but the devices fabricated in this work use a thin gate metal that contributes a large series resistance to measured gate capacitance and conductance at high frequencies. The capacitors presented in this section were fabricated with the same Al_2O_3 and WN process as the lot C MOSFETs but capped with 250 nm Al metal. A post-metal RTA was performed at 500 °C for 1 min in N_2 in order to replicate the thermal budget of the typical MOSFET process flow.

The complete G_p/ω characteristics for the un-implanted and Sb-implanted capacitors can be found at the end of this section in Figure 5.13 and Figure 5.14. Interestingly, the measured profiles from room temperature down to 80 K are nearly identical for both devices. At 300 K where E_F is positioned near the middle of the bandgap, clear peaks are observed in the G_p/ω curves corresponding to a minimum D_{it} value of approximately $3x10^{11}$ $cm^{-2}eV^{-1}$. As discussed in Chapter 3, lowering the temperature will shift E_F closer to the conduction band edge (for an n-type capacitor), allowing different trap states to be sampled. The reduction in temperature also increases the time constant for the corresponding states, allowing them to respond to lower measurement frequencies. However in these samples, no distinct peaks are observed in the G_p/ω characteristics at 80 K indicating that the fast interface states near E_C maintain an associated time constant that is out of the range of these measurements. Therefore a precise value of D_{it} cannot be assigned to this trap level, although inspection of Figure 5.13 and Figure 5.14 would suggest a value at least an order of magnitude higher than the slower midgap states.

Again, as in Chapter 3, the Gray-Brown method was used in order to quantify the total amount of charge trapping present in these devices. Although it is clear from the conductance data that some states will not be 'frozen-out' at 80 K, this technique should still provide a qualitative comparison between the un-implanted and Sb-implanted samples. It should also capture the effect of slower states that are not accessible via the conductance method [59]. As shown in Figure 5.11, a greater flatband shift as a function of temperature is observed in the un-implanted n-type capacitor. Figure 5.12 summarizes the measured flatband shift in both capacitors in comparison with the ideal shift in the

absence of interface states. Comparing the total V_{FB} shift at 80 K to the ideal value, one obtains D_{it} values of $1.2x10^{13}$ and $5.0x10^{12}$ for the un-implanted and Sb-implanted capacitors, respectively. Once again, this corresponds well to the calculated D_{it} values from low temperature measurements on the As-implanted MOSFETs of lot B discussed in the previous section.

Although the precise value of 'fast' D_{it} cannot be ascertained from the conductance measurements, the similarity of the measured spectra in Figure 5.13 and Figure 5.14 would suggest that overall profile of fast traps is similar for un-implanted and implanted substrates. Combined with the significant reduction in trapping observed using the Gray-Brown method, this would suggest the primary effect of the n-type channel implant is a reduction in slow states near E_C. This is consistent with the observations of Khakifirooz [6], who performed pulsed I-V measurements on similar P-implanted Ge n-FETs, and concluded that the mobility enhancement observed in those devices was primarily the result of a reduction in slow trap states.

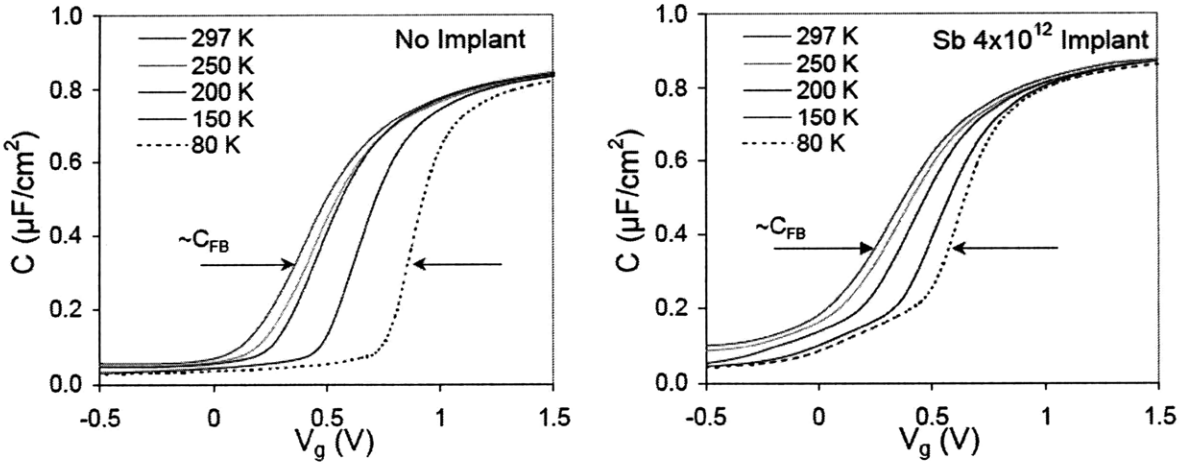

Figure 5.11 Measured low temperature C-V characteristics for n-type Ge MOS capacitors at f = 1 MHz with ALD WN/Al_2O_3 gate stack. The capacitor on the right received a $4x10^{12}$ cm^{-2} dose implant of Sb with a 600 °C activation anneal prior to gate deposition.

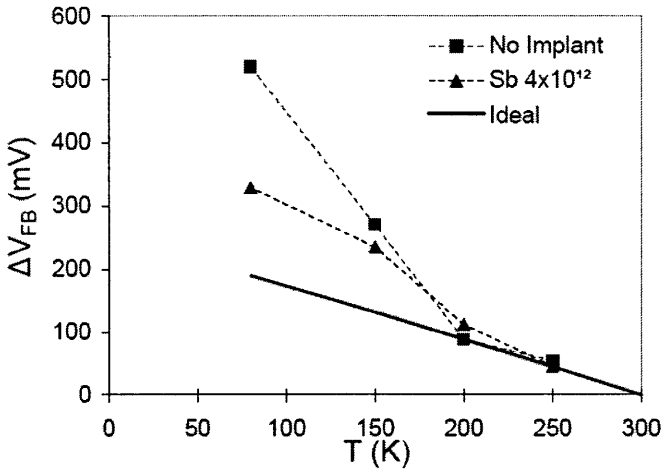

Figure 5.12. Measured shift in flatband voltage as a function of temperature for the C-V characteristics shown in Figure 5.11 with comparison to the ideal value in the absence of interface states.

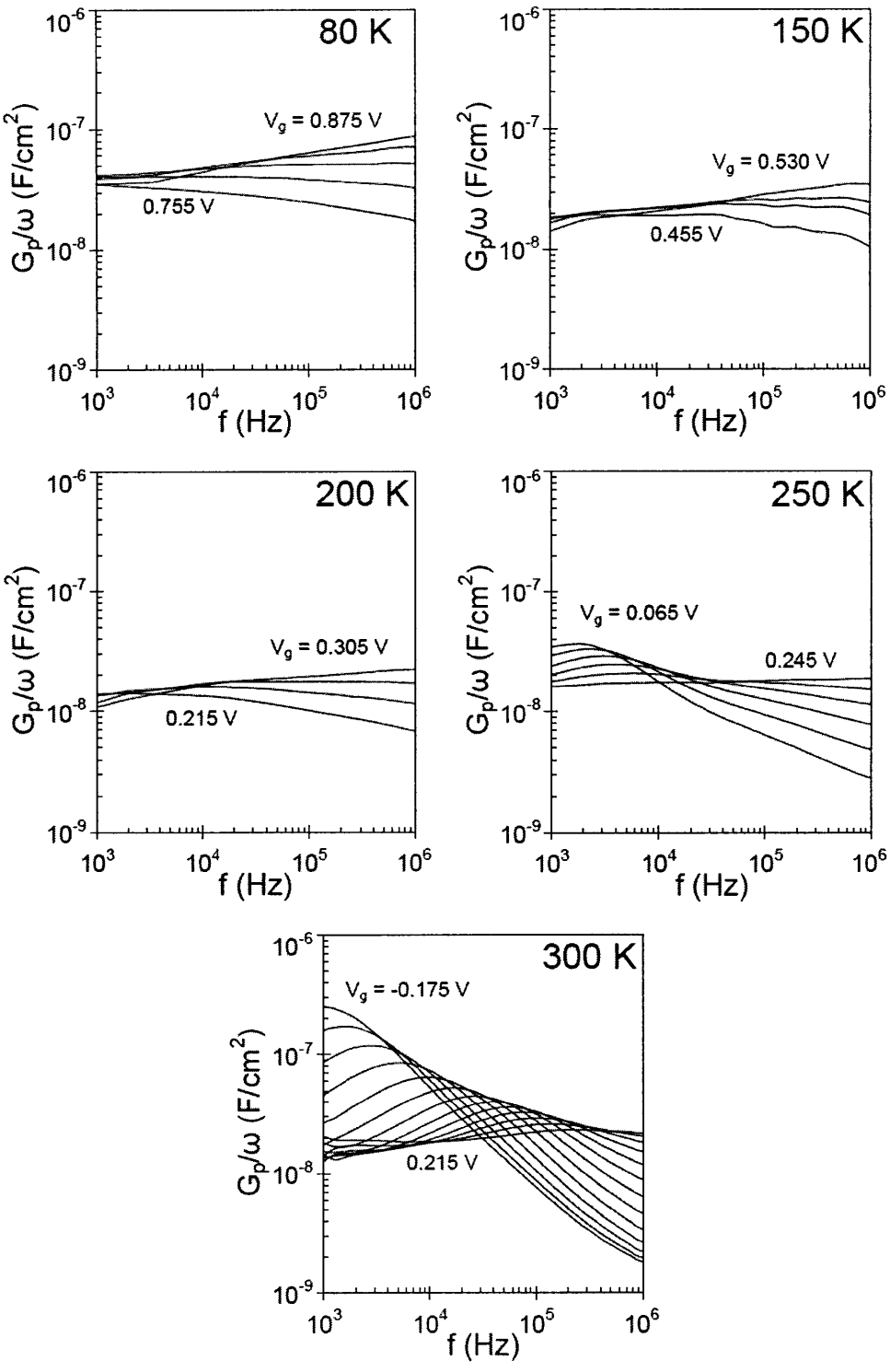

Figure 5.13. G_p/ω vs. frequency with gate voltage as a parameter at various temperatures for an n-type Ge MOS capacitor with no channel implant. The indicated gate voltages correspond to biasing in depletion where the conductance method is valid.

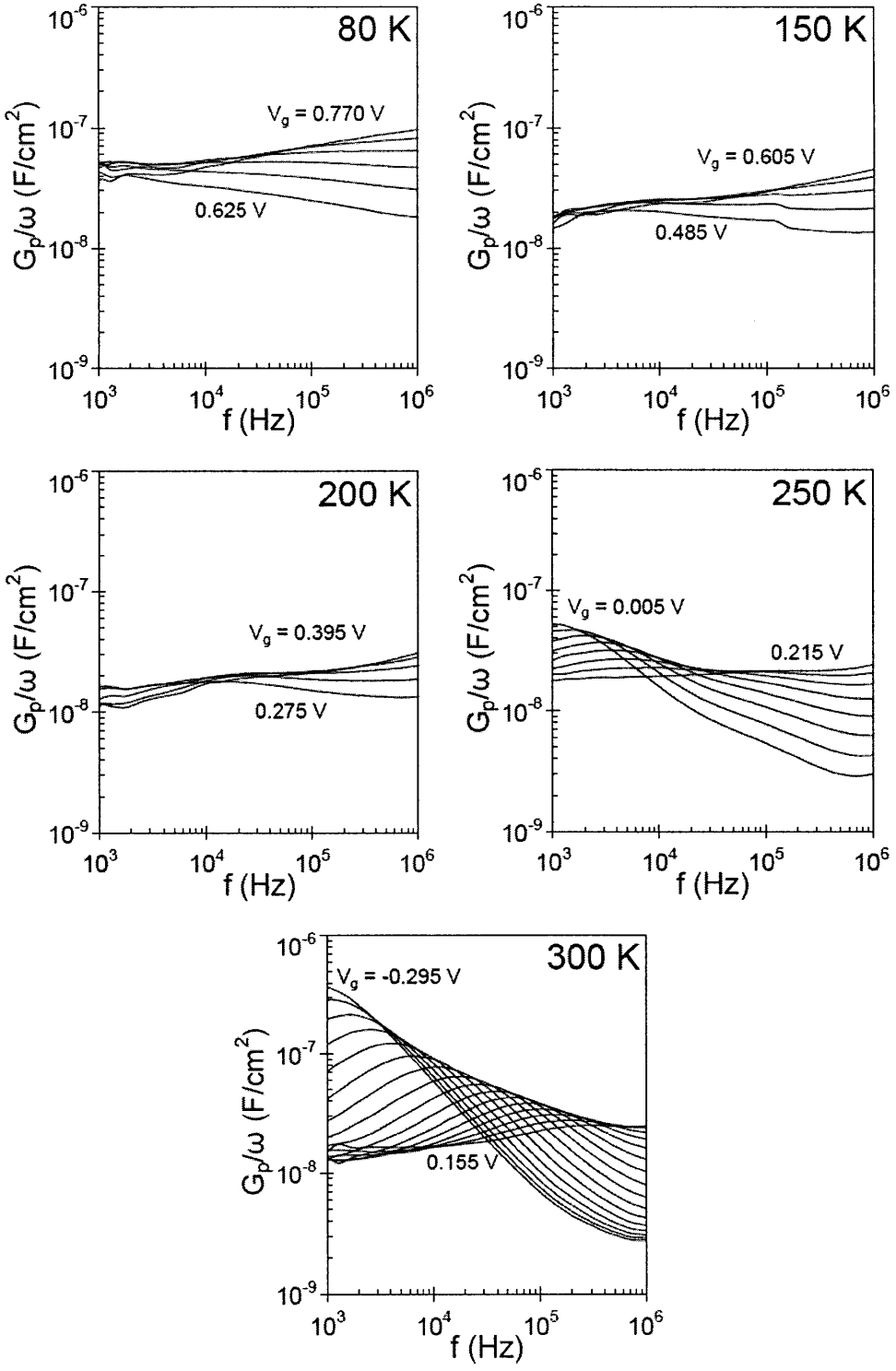

Figure 5.14. G_p/ω vs. frequency with gate voltage as a parameter at various temperatures for an n-type Ge MOS capacitor with a channel implant of Sb ($4x10^{12}$ cm^{-2}, 30 keV).

5.6 Chapter Summary

In this chapter significant evidence for D_{it} reduction resulting from n-type channel implants was presented. Substrate bias response suggests that the observed mobility enhancement is not the result of a shift in the inversion layer centroid. A comparison of the degradation in drive current for implanted and un-implanted n-FET devices suggests that a fundamental improvement in the electrical quality of the gate interface has occurred as a result of the n-type dopant channel implant.

Low temperature observations of MOSFET threshold voltage and subthreshold swing both suggest a reduction in slow trap states for implanted devices. This claim is further supported by that observation of excessive V_t shifts in implanted n-FET devices, which is consistent with a reduction in negatively charged acceptor-like trap states. Conductance measurements performed on n-type MOS capacitors seem to imply that the density of fast trap states has not been significantly affected by a $4x10^{12}$ cm^{-2} dose ion-implant of Sb. However, low temperature measurements performed on the same capacitors also show a large reduction in slow trap states, consistent with the MOSFET observations.

Other authors have reported observations of slow acceptor traps in Ge/oxide systems. Afanas'ev et al. reported that Ge/HfO_2 MOS structures appeared to be dominated by slow acceptor states attributed to defects in the near-interfacial oxide layer [60]. Kuzum et al. observed severe slow trapping of electrons in $Ge/GeO_2/Al_2O_3$ n-FETs attributed to the filling of GeO_2/Al_2O_3 border traps as a result of the low conduction band

offset between Ge and GeO_2 [25]. Martens speculated that the poor-performance of Si-passivated Ge n-FETs could be explained by a double-acceptor trap state near the Ge conduction band [61]. The analysis presented in this chapter suggests that the gate interfaces investigated in this work are also dominated by slow acceptor-like trap states near E_C that strongly influence the threshold behavior and electron mobility in Ge n-FETs. Channels implants of n-type dopant species are effective at reducing the density of these trap states with a resulting increase in electron mobility.

Chapter 6 - Conclusions

6.1 Summary

The key contributions of this thesis are:

1. Observation that the native oxide of Ge can provide a thermally stable interface with reduced D_{it} for subsequent deposition of high-k gate dielectrics.
2. Development and optimization of a novel O_3 passivation technique that can be performed at low temperatures and in-situ as part of an ALD gate stack. The optimal passivation recipe suggests that O_3 along with some contribution from NO_x species yields the lowest D_{it}.
3. The O_3 surface treatment results in reduced D_{it} across the Ge bandgap, lowest reported subthreshold swing for surface channel Ge MOSFETs, and higher-than-Si hole mobility with an EOT contribution of only 0.3 nm.
4. An experimental study on MOSFET S/D annealing temperature suggested that, unlike other similar methods, the surface treatment developed in this work is thermally stable at more typical Ge S/D activation temperatures.
5. A MOSFET lot was fabricated with ALD HfO_2 gate dielectrics indicating that the O_3 surface treatment is effective with multiple ALD materials, and near 1 nm EOT devices were demonstrated with very low gate leakage.
6. Several ion-implanted n-type dopant species were observed to result in significant electron mobility enhancement, particularly at low inversion densities, resulting in the first observation of higher-than-Si electron mobility in a Ge MOSFET.

7. Substrate bias measurements were performed that indicate that these mobility enhancements are not the result of reduced effective field operation or a shift in the inversion centroid.
8. Observations of excessive V_t shifting in implanted n-FET devices, as well as low temperature MOSFET and MOS capacitor characterization indicate a large reduction in charge trapping for n-type dopant channel implants.
9. The mobility enhancement is attributed to a reduction in slow acceptor-like trap states near the conduction band of Ge.

6.2 Future Work

The conclusions of Chapter 3 suggest that a combination of O_3 at low temperature plus some contribution from NO_x species provides additional reduction in D_{it} over O_3 alone. The exact impact of this additional NOx on the interfacial chemistry of the passivation layer is also not known, but a more detailed XPS study may be possible. The limits of the ozone generator in terms of N_2 dopant flow were reached in this experiment, however alternate methods for introducing NO_x during the passivation step may provide even better interface characteristics. These may include introduction of some nitrogen-containing plasma during the passivation step [62], or intentionally diluting the inlet O_2 stream of the generator with N_2 prior to discharge. The in-situ addition of NH_3 was investigated prior to, during, and following the O_3 surface treatment but was not observed to have any measurable impact on D_{it}.

All column V dopant species investigated in this work were observed to have a significant effect on charge trapping and electron mobility in Ge MOSFETs. The only

technique investigated in this work for introducing these species was ion-implantation. It is possible that other techniques may be more effective such as the epitaxial growth of a thin, highly-doped Ge layer, or attempting a solid-source doping technique prior to gate deposition. It is also noted that there exists an abundance of reports on the beneficial effects of sulfur [63][64] or fluorine [24][65] passivation on Ge surfaces. It may be possible that the investigation of column VI or column VII elements following the technique proposed in this thesis could provide additional improvements.

Appendix A - n-type C-V Behavior

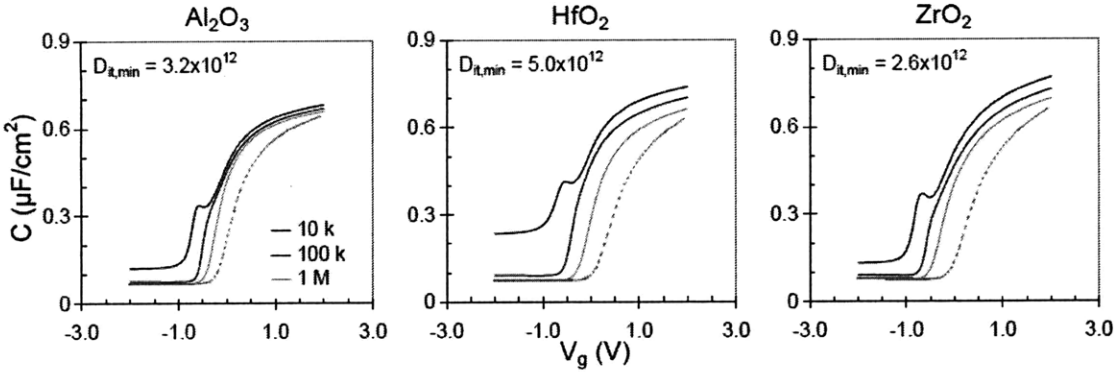

Figure A.1. Forward C-V characteristics at f = 1 kHz, 10 kHz, and 1 MHz, and reverse (dashed) at f = 1 MHz for n-type Ge capacitors with various ALD oxide interfacial layers (all capped with ALD Al_2O_3). Indicated D_{it} values were calculated with the conductance method.

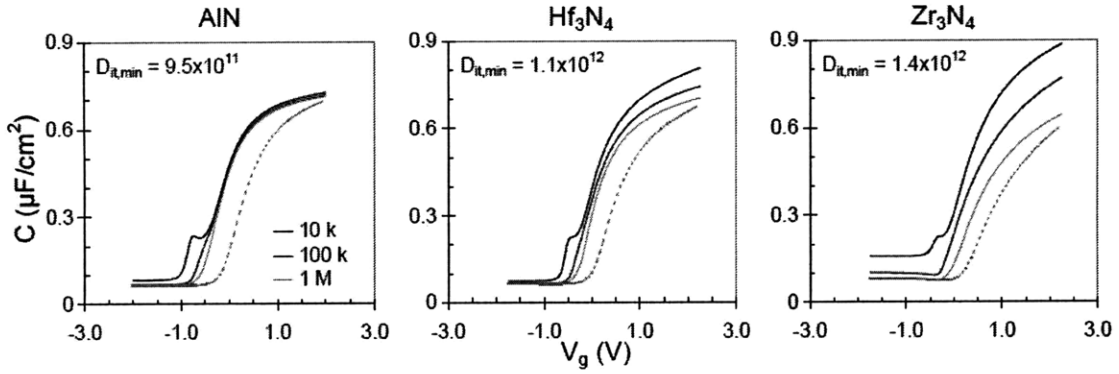

Figure A.2. Forward C-V characteristics at f = 1 kHz, 10 kHz, and 1 MHz, and reverse (dashed) at f = 1 MHz for n-type Ge capacitors with various ALD nitride interfacial layers (all capped with ALD Al_2O_3). Indicated D_{it} values were calculated with the conductance method.

Appendix B - ALD Recipes

Recipes were developed for a Cambridge NanoTech Savannah^{TM} 200 ALD reactor. The nitrogen carrier flow in all cases was fixed at 20 sccm. ALD-mode operation was confirmed by verifying a linear thickness dependence on the total number of ALD cycles. The thickness and uniformity of the deposition were measured on 150 mm Si wafers by spectroscopic ellipsometry, with a typical uniformity of < 2% variation across the wafer. Any non-linear thickness dependence or gross non-uniformity was considered a symptom of CVD contamination. This is usually evidenced by a gradual drop-off in film thickness measuring from the inlet to the outlet side of the chamber, as well as deposition rates much higher than 1 Å/cycle. This can addressed by reducing precursor dose (by reducing the pulse time or the precursor temperature), or by increasing the purge time between pulses. A thickness profile that is uniform starting from the inlet side of the chamber and then drops off rapidly is a symptom of an under-dosed ALD process. This can be addressed by increasing precursor dose.

The complete ALD window was not verified systematically for each recipe, but will vary as function of the precursor chemistry. In general, a chamber temperature that is too low will not allow for sufficient chemisorption of the precursor dose to allow ALD to occur. A chamber temperature that is too high will result in thermal decomposition of the adsorbate before the second precursor is introduced into the chamber. Both of these scenarios will generally result in small or sporadic deposition rates.

Table B.1. Aluminum oxide and aluminum nitride ALD recipes. (TDMAA = tris(dimethylamido)aluminum)

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TDMAA	110 °C	0.1	0	8
H_2O	RT	0.015	0	8
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 1.1 Å/cycle				

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TDMAA	110 °C	0.1	0	8
NH_3	RT	0.1	0.1	12
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 0.9 Å/cycle				

Table B.2. Hafnium oxide and hafnium nitride ALD recipes. (TEMAH = tetrakis(ethylmethylamido)hafnium)

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TEMAH	95 °C	0.1	0	8
H_2O	RT	0.015	0	8
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 0.9 Å/cycle				

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TEMAH	95 °C	0.1	0	8
NH_3	RT	0.2	0.2	12
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 1.0 Å/cycle				

Table B.3. Hafnium oxide and hafnium nitride ALD recipes. (TEMAH = tetrakis(ethylmethylamido)hafnium)

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TEMAH	95 °C	0.1	0	8
H_2O	RT	0.015	0	8
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 0.9 Å/cycle				

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TEMAH	95 °C	0.1	0	8
NH_3	RT	0.2	0.2	12
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 1.1 Å/cycle				

Table B.4. Zirconium oxide and zirconium nitride ALD recipes. (TDMAZ = tetrakis(dimethylamido)zirconium)

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TDMAZ	70 °C	0.1	0	8
H_2O	RT	0.015	0	8
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 1.0 Å/cycle				

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TDMAZ	70 °C	0.1	0	8
NH_3	RT	0.2	0.2	12
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 1.1 Å/cycle				

Table B.5. Tungsten nitride ALD recipe. (W = bis(tert-butylimino)bis(dimethylamino)tungsten)

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
W	90 °C	0.1	0	8
NH_3	RT	0.2	0.2	12
Notes: Substrate Temp ≈ 350 °C, Deposition Rate ≈ 0.35-0.45 Å/cycle				

Alternate Recipes

Table B.6. Aluminum oxide with trimethyl-aluminum as a precursor.

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TMA	RT	0.015	0	8
H_2O	RT	0.015	0	8
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 1.0 Å/cycle				

Table B.7. Aluminum oxide with aluminum chloride as a precursor.

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
$AlCl_3$	105 °C	0.2	0	8
H_2O	RT	0.015	0	8
Notes: Substrate Temp = 200 °C, Deposition Rate ≈ 0.9 Å/cycle				

Table B.8. Aluminum oxide with isopropyl alcohol as the oxidizing precursor.

Precursor	*Precursor T*	*Pulse (s)*	*Expo (s)*	*Purge (s)*
TMA	RT	0.015	1	8
IPA	RT	0.2	8	8
Notes: Substrate Temp = 250 °C (300 °C), Deposition Rate ≈ 0.6 (0.8) Å/cycle ALD not observed at lower substrate temperatures.				

Appendix C - Thermal Stability of O_3 Treatment

There have been several reports on the instability of GeO_2 passivation layers at elevated temperature, requiring reduced S/D activation anneals in order achieve best-case mobilities [24][25][26]. In order to gauge the stability of the O_3 treatment used in this work, the un-implanted MOSFETs from lot C were fabricated with two different activation anneals. Figure C.1 indicates that little change is observed in both hole and electron mobility as a function of activation temperature. This would suggest that the interface layer created by the O_3 surface treatment used in this work does not suffer degradation at more typical S/D annealing conditions.

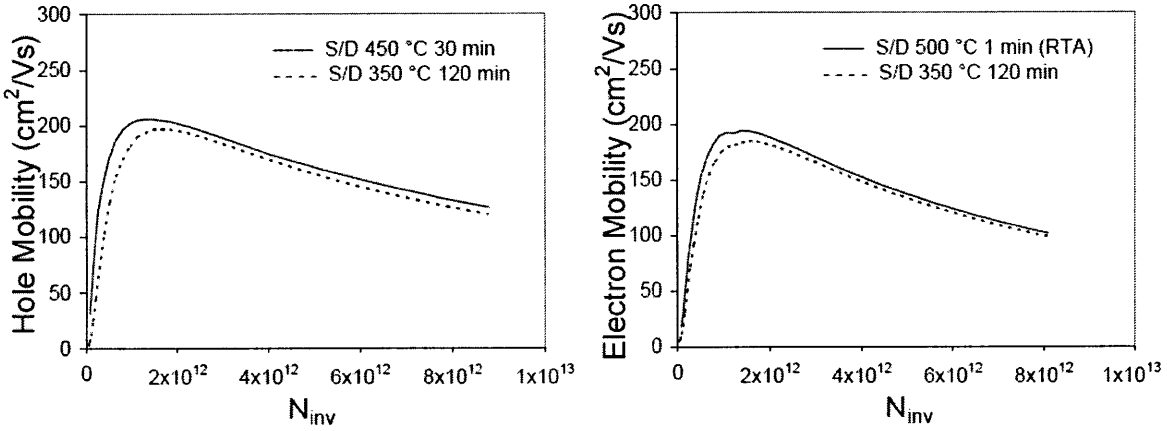

Figure C.1. Effective carrier mobility (split-CV) for Ge p- and n-MOSFETs fabricated with ALD 40 nm WN / 6 nm Al_2O_3 gate stack and two different source/drain activation conditions.

Appendix D - Slow Trapping Behavior

Significant slow trapping was observed in the ALD films investigated in this work, leading to moderate C-V hysteresis (see Figure 3.7 and Figure 3.8). The O_3 surface treatment was observed to have little impact on this hysteresis (see Table 3.1). The same slow trapping states also lead to large I-V hysteresis in the measured MOSFET characteristics. As indicated in Figure D.1, additional trapping also leads to a shift (towards larger $|V_t|$) in measured I_s-V_g characteristics for both p-FET and n-FET devices, consistent with hole and electron trapping respectively. This shift is observed to saturate after several sweeps into inversion, and detrapping does not occur as the gate voltage is swept back out of inversion. In other words, a stable hysteretic loop undergoes the same shift toward higher $|V_t|$.

Like the voltage hysteresis, this shift behavior is much more notable for electrons than holes. This behavior is summarized in Figure D.2 indicating that the increase in $|V_t|$ is approximately 8x higher for the un-implanted n-FET device of lot C than the equivalent p-FET device. A similar shift is observed in the measured split-CV characteristics, which can lead to significant errors in mobility calculations if care is not taken. For example, if the first measured I_s-V_g curve is used along with a subsequently measured inversion-side C-V, then the calculated mobility will be greatly overestimated, particularly at low inversion densities. In order to avoid this pitfall, the method used to calculate effective carrier mobility in this work was to perform repeated forward sweeps into inversion until no additional shifting was observed in either the I-V or C-V characteristic. Care was taken to sweep over the same voltage range and at the same sweep rate (~ 0.5 V/s) for both traces. It is these 'stable' characteristics that are presented

in the body of this work, and used for the calculation of V_t and subthreshold swing. It is noted from Figure D.1 that the subthreshold swing is not notably impacted by this shifting behavior.

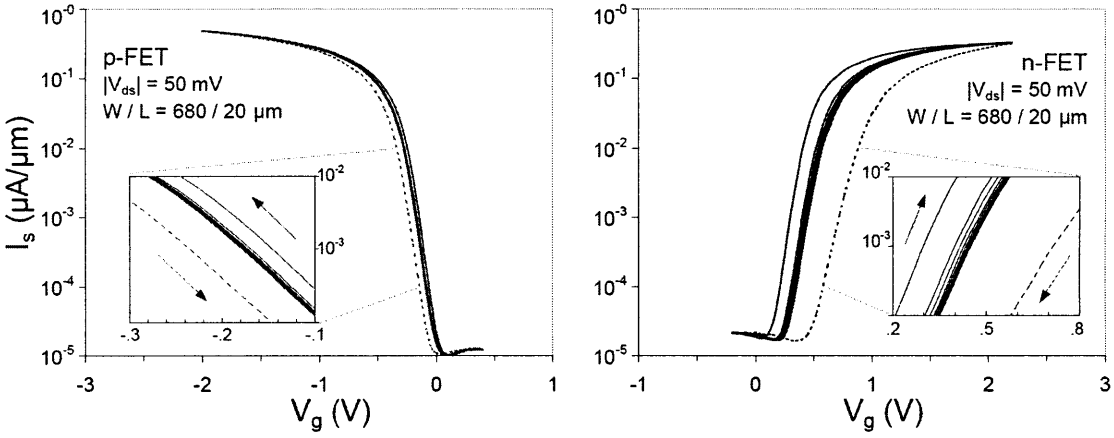

Figure D.1. Slow trapping behavior for eight repeated forward sweeps into inversion (solid lines) and I_s-V_g hysteresis (dashed line) for the un-implanted lot C MOSFETs (6 nm ALD Al_2O_3, optimal O_3 surface treatment, no implant).

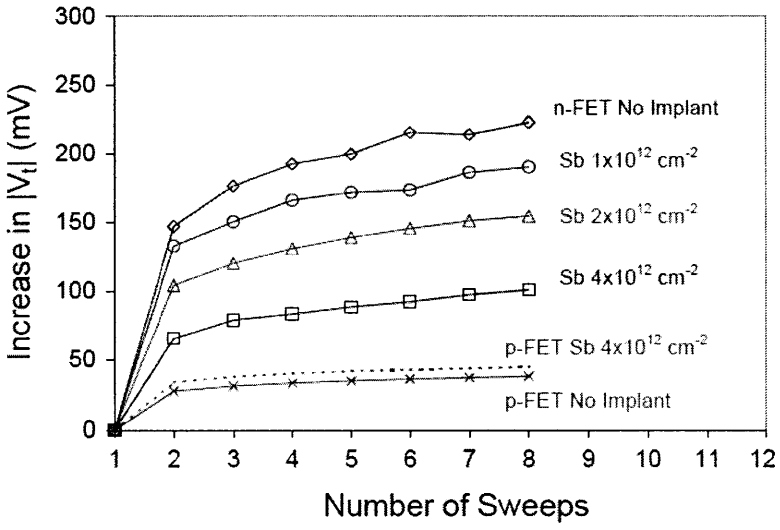

Figure D.2. Average shift in the extrapolated V_t of the lot C MOSFETs for successive sweeps into inversion.

A clear correlation between the reduction of the $|V_t|$ shift and implanted Sb dose was observed for n-FET devices as indicated in Figure D.2. Little impact was observed for p-FET devices receiving the same Sb implant. The same trend is also observed in the measured I_s-V_g hysteresis as indicated in Figure D.3. Both are consistent with the claims of reduced slow-trapping from n-type dopant channel implants presented in Chapter 5, and provide further evidence of the impact these slow trap states have on electron mobility.

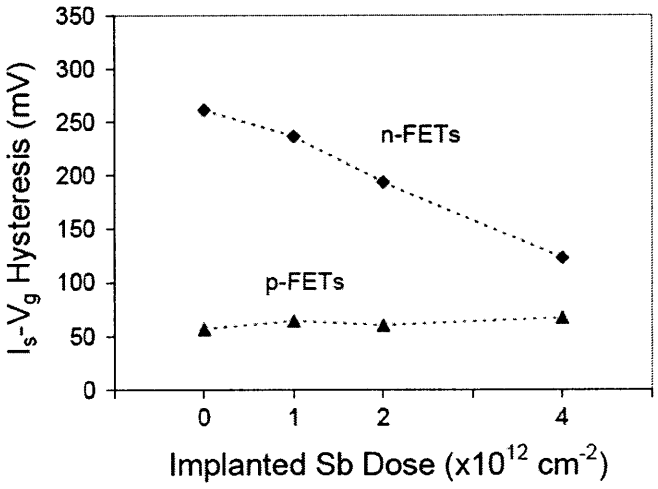

Figure D.3. Average measured I_s-V_g hysteresis (evaluated at $I_s = 1x10^{-3}$ μA/μm) for the lot C MOSFETs at various doses of ion-implanted Sb.

Also of note is a comparison of the same behavior for the HfO_2 devices discussed in Chapter 3. Figure D.4 shows that much larger $|V_t|$ shifts are observed for both the HfO_2 p-FETs and HfO_2 n-FETs compared to the Al_2O_3 devices above. This is consistent with the increased C-V hysteresis observed in MOS capacitors fabricated with ALD HfO_2, as well as the measured I_s-V_g hysteresis (for the same devices in Figure D.4) which increased from an average of 55 mV in the un-implanted Al_2O_3 p-FET to 155 mV for the

HfO_2 p-FET; and increased from 260 mV in the Al_2O_3 n-FET to 330 mV in the HfO_2 n-FET. It is interesting to note that although the HfO_2 p-FET devices show dramatically higher slow trapping behavior than their Al_2O_3 counterparts, the measured hole mobilities are nearly identical (see Figure 3.14). In contrast, the HfO_2 n-FET devices also show more slow trapping behavior than the Al_2O_3 n-FETs, yet the HfO_2 devices show degraded electron mobility. Combined with the observation above on the impact of Sb implants on the slow-trapping behavior of Ge MOSFETs, it becomes clear that these slow states have a large impact on electron mobility in Ge, but very little impact on hole mobility.

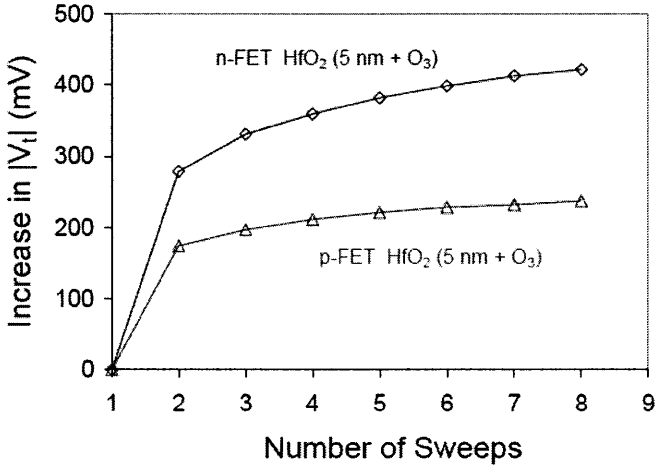

Figure D.4. Average shift in the extrapolated V_t of the O_3-treated 5 nm HfO_2 MOSFETs for successive sweeps into inversion.

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