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SiC APDs and Arrays for UV and Solar Blind Detection

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Abstract- We report advancements in APDs and arrays using 4H SiC. Novel structures, array designs and specialized read out integrated circuits have been developed towards the realization of UV and solar-blind detector arrays exhibiting appreciable quantum efficiency, low noise and Geiger-mode operation. Discussion will include the design, fabrication and testing of these devices, which may find use in a variety of applications.

INTRODUCTION

APDs working in the UV are of interest for several applications, including bio-aerosol detection, UV imaging, harsh environment gamma sensing [1] and long-range flame detection in the solar-blind window. Si detectors or PMTs have partly addressed these needs, however, they generally have limited deep-UV quantum efficiency and appreciable visible response. To realize visible or solar blindness, optical filtering may be required and when added, further limits their sensitivity and applicability.

Advancements in UV APDs have been made using wide bandgap semiconductors such as GaN [2] and SiC [3], which offer inherent visible blindness, harsh environment capability and low noise performance. GaN, further offers the potential for self-filtered solar-blind detectors with sharp responsivity cutoff [4], however, it commonly suffers from a high density of material defects limiting APD performance [5].

SiC has seen substantial improvements in substrate quality in part due to their usage in GaN-based light emitting diodes, and more recently in devices such as SiC diodes. Combined with improved fabrication methods, 3-inch wafers of 4H SiC provide a means to realize an appreciable yield of APDs that facilitate multi-pixel arrays.

Separate absorption and multiplication region designs were employed to maximize quantum efficiency while suppressing dark current originating from the bulk materials. As drawbacks of this design include a requirement for deeper etching to form the mesa, higher breakdown voltages and a reduced fill factor, p-i-n designs were also considered.

To realize SiC APD arrays, positively tapered sidewalls were formed to reduce surface leakage current, a technique commonly employed in power device design [6]. A 3 µm thick SiO2 layer was deposited, then selectively etched to realize a p and then n-type ohmic contacts using Ti/Al/Ti/Ni (100/200/200/2000 Å) and Ni (550 Å). An annealing step at 1050 °C, then inter and pad metals using Ti/Mo (2000/8000 Å) and Ti/Au (2000/4000 Å). An etch stop layer using 2000 Å Ni was used in the area immediately under the thin-film dielectric stack filter, that provided blocking in the UV outside the solar-blind window. Here, HfO2/SiO2 films were deposited for a total thickness of approximately 5 µm. Dry etching was used to enable access to the device electrodes, and a cross-section is shown in figure 1, with an example 16-element SiC APD array shown in figure 2.

Past variations in substrate defect density, epitaxy layer thickness and doping increased device-to-device non-uniformity lowering the likelihood that adjacent devices performed similarly in avalanche [7], thereby limiting APD array size without sophisticated electronics.

In this work, sections of the wafers measured were studied for uniformity, and an example is shown in figure 3. 4x4 APD arrays were tested at the wafer-level prior to dicing and without incident light on an automated probe station. Defining the breakdown voltage as the voltage at which 10 µA was reached, the top portion of figure 3 identifies the current bin at 95% of the breakdown voltage. The bottom identifies the breakdown range. Leakage current and breakdown voltage distributions show that while there are clear variations in both parameters, groups of devices are co-located which exhibit similar and suitable behavior for various applications.

Read-out integrated circuits (ROICs) were designed to interface to the SiC APDs. The ROIC consists of sixteen pixels that both detect and time-stamp avalanche events for each SiC APD in a 4x4 array. Each APD cathode connects to its own pixel front-end circuit that provides the necessary overbias voltage for Geiger-mode operation. When the front-end detects an avalanche, it will actively quench the APD, and register a capture signal which is passed to timing circuitry within the pixel to assign a time stamp to the event. The time stamp is passed to read-out circuitry that formats the data into a packet and streams it off-chip via one of sixteen serial output channels, where it may be post-processed by another device, such as an FPGA. For applications where timing information is not required, the timing circuitry can be bypassed and the capture signal sent directly to the chip output. The ROICs were fabricated in a 0.18-µm commercial CMOS process. SiC APD arrays were mounted on top of the ROIC, and the APD cathode-to-pixel front-end connections were made via wirebonds, as shown in Figure 4.

Photoresponsivity, dark current and Geiger-mode performance of these APDs will be discussed.
ACKNOWLEDGMENT

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REFERENCES


Figure 1. Cross-section of SiC APD array. The active area was approximately 44 µm and the p-n junction was about 100 µm wide.

Figure 2. SiC APD array with p-type contacts at the corners (250 µm wide), n-type contacts in the center (4 on each side).

Figure 3. Wafer-level dark current (top) and breakdown (bottom) voltage distributions for a section of a 3 inch wafer. Each square is an individual device and each grid element is a 4x4 array. White areas are test structures.

Figure 4. 4x4 SiC APD array mounted on a CMOS ROIC with the APD cathodes wirebonded to the pixel front-ends of the ROIC.