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On-Wafer Integration of Nitrides and Si Devices: Bringing the Power of Polarization to Si

Jinwook W. Chung, Bin Lu, and Tomás Palacios

Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology
77 Massachusetts Ave., Bldg. 39-567B, Cambridge, MA 02139, USA

Abstract — The seamless integration of AlGaIn/GaN transistors and Si CMOS electronics on the same chip will revolutionize digital and mixed signal electronics. In this talk we describe our group's effort on demonstrating this integration. Si-GaN-Si virtual substrates have been recently fabricated through substrate removal and wafer bonding processes. The very high thermal stability of nitrides allows for the fabrication of Si CMOS electronics on these substrates without degrading the performance of the embedded nitride layer. In addition, GaN transistors on Si (001) have been fabricated on these substrates for the first time. Some of the many new circuits and devices that this integration allows include high power analog-to-digital converters, high speed differential amplifiers, normally-off power transistors, and highly-compact power regulator circuits.

Index Terms — HEMT, High Electron Mobility Transistor, Integration, MOSFET, Nitride Semiconductors, Silicon.

I. INTRODUCTION

Moore's law has been one of the main drivers behind the unprecedented development of semiconductors in the last forty years. However, this economical and technological paradigm that has helped to create modern Si electronics is now jeopardizing its future. Traditional Si scaling is not only becoming unaffordable, but also the performance improvement due to scaling is diminishing [1].

Our group is working on an approach different from Moore's law to increase the performance of electronics: the heterogeneous integration of different semiconductor materials on the same wafer. In this paper, we describe our work on the seamless integration of GaN-based devices and Si electronics. While Si electronics has shown unsurpassed levels of scaling and circuit complexity, nitride semiconductors offer excellent optoelectronics and high frequency/power electronic properties [2, 3]. The ability to combine these two material systems in the same chip and in extremely close proximity would allow unprecedented flexibility for advanced applications.

II. SI-GAN-SI VIRTUAL SUBSTRATES

Using a substrate removal technology in combinations with wafer bonding, virtual Si (001) / GaN / Si (001) substrates have been fabricated for the first time. Figure 1 describes the main processing steps required for the

fabrication of one of these substrates and Figure 2 shows a scanning electron micrograph of the wafer cross-section. From the outside, the final wafer looks like a conventional Si wafer as there is a Si (001) layer on the top and bottom surfaces and the nitride epilayer is embedded 200 nm below the surface of the wafer. Due to the high thermal stability of GaN, Si CMOS devices can be processed in these new substrates without affecting the nitride layers underneath the surface. After the Si devices are fabricated, the Si material is removed from the regions where nitride devices are needed. Then, the nitride devices (transistors, LEDs, lasers or sensors) are processed at room temperature and, finally, an interconnection layer forms the final hybrid circuits (Figure 3).

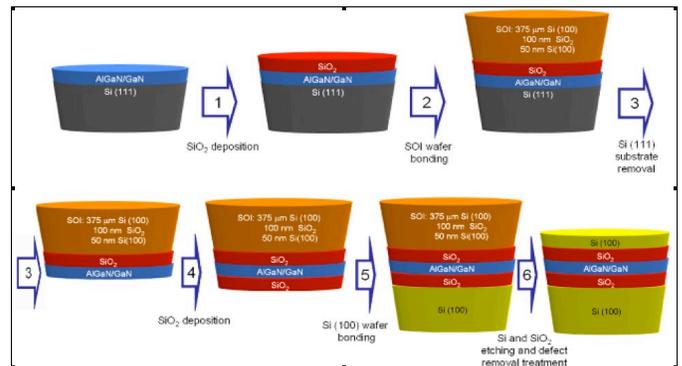


Figure 1. Main steps of the fabrication of Si-GaN-Si virtual wafers required for the seamless integration of GaN and Si electronics.

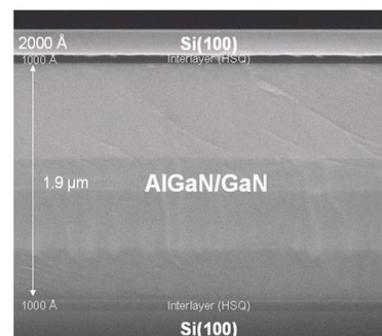


Figure 2. Scanning electron micrograph of a Si-GaN-Si virtual wafer.

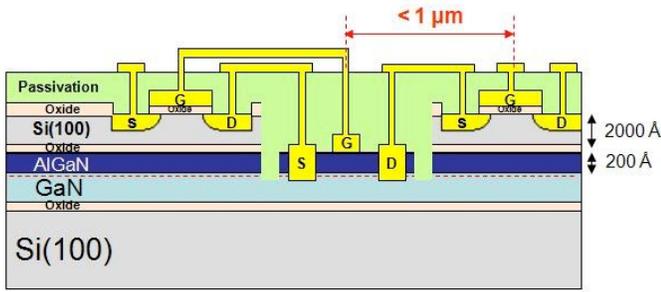


Figure 3. Schematic of the cross-section of a GaN/Si hybrid circuit.

Figure 4 shows a scanning electron micrograph of two transistors, one GaN HEMT and one Si p-MOSFET, fabricated side by side following the technology described in this paper. The current voltage characteristics of the GaN power transistor fabricated on the Si (001) wafer are shown in Figure 5. As observed from the I-V measurements, the integration with Si (001) does not degrade the device performance. The Si transistor did not show any degradation either.

Using this new technology, several hybrid circuits are currently being developed, including high power differential amplifiers and normally-off power transistors (Figure 6). These advanced circuits are just a few examples of the potential of heterogeneous integration and how the close integration of Si and other materials enables a vast array of new exciting opportunities for electronics.

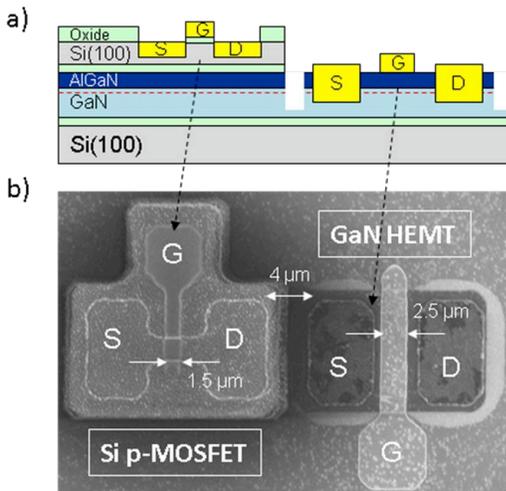


Figure 4. a) A cross-section schematic of fabricated Si p-MOSFETs and GaN HEMTs. b) A top SEM view of corresponding transistors.

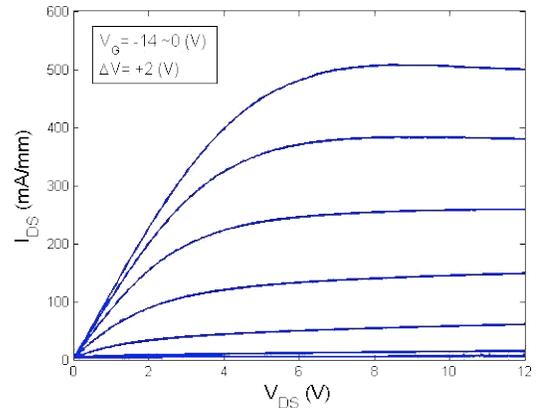


Figure 5. I_{DS} vs V_{DS} characteristics of the first AlGaN/GaN transistor fabricated on a Si (001) substrate.

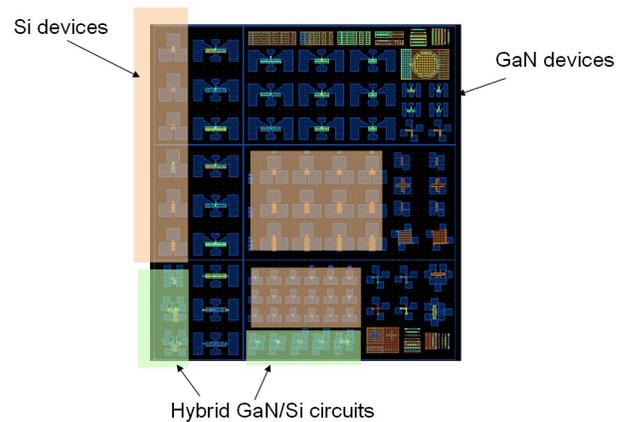


Figure 6. Layout of the mask being used to demonstrate the seamless integration of GaN and Si devices on hybrid circuits.

III. On-Wafer GaN-Si Power Regulator

The heterogeneous integration technology described in this paper can also find numerous applications in digital Si electronics. Power regulation is an important challenge in modern microprocessors due to the trade-off between power dissipation, operating voltage and input bias current. To keep a constant power dissipation in current and future microprocessors, the operating voltage has to be decreased, which increases the input current to levels well above 100 A per microprocessor. This very high input current increases conductive power losses and reduces the number of I/O pins available in traditional microprocessor packaging. One of the most promising solutions to this problem is to introduce the power into the microprocessor and distribute it at high voltages (and low currents) and then downconvert it to the required voltage, locally, in highly integrated on-wafer power regulator circuits. The fabrication of an all-Si solution is very challenging due to the low breakdown voltage and frequency performance of Si power electronics. The hybrid integration of GaN and Si devices, on the other hand, would enable on-wafer voltage regulators with unprecedented performance and

integration levels. Figure 7 shows the circuit diagram of one of these new hybrid regulators currently being developed in our group, a tapped-inductor DC-DC converter topology where GaN switches are used in the high voltage stress / low current part of the circuit and Si power MOSFETs are used in the low voltage / high current regions of the power circuit. The use of a tapped-inductor topology also extends the available duty cycle to allow high voltage conversion ratios and helps the soft-switching of both Si and GaN transistors.

Using the topology described before, we have designed a hybrid taped-inductor DC-DC converter with 12:1 conversion ratio and 10 W output power. A very high switching frequency of 300 MHz was chosen to allow for on-chip integration of the entire converter. The circuit operates in the soft-switching mode with duty cycle of 50%. The on-resistance and output capacitance in the SPICE model were obtained from measurements and data-sheets. The simulation shows that the use of GaN switches in the high voltage part of the circuit instead of Si devices reduces the circuit losses five fold. This result demonstrates the great potential of a hybrid GaN/Si power electronic circuit to enable local power conversion in high performance Si electronics. However additional work on the circuit topology and the design of the passive components is needed to increase efficiency above 85%.

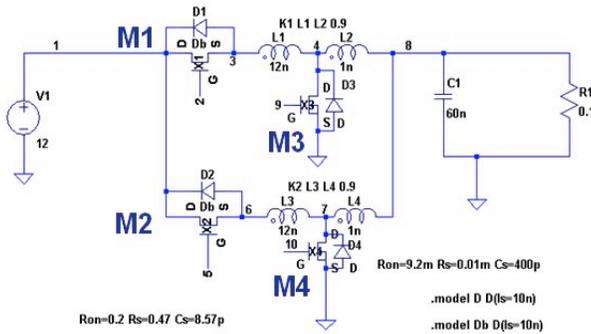


Figure 7. Circuit schematic of the new GaN-Si hybrid power converter. M1 and M2 are GaN-based power transistors while M3 and M4 are Si MOSFETs.

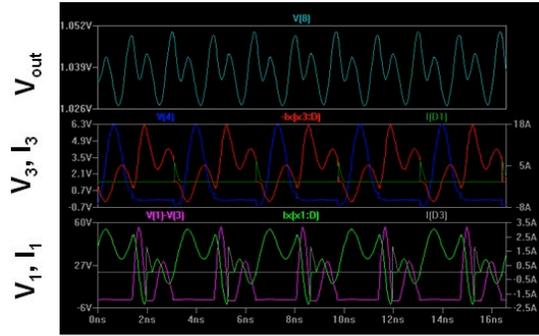


Figure 8. Simulation of the current and voltage waveforms in the 12:1 V hybrid voltage regulator studied in this project.

IV. Conclusion

No single semiconductor can provide the performance required by the complex communication systems of the future. Heterogeneous integration of several semiconductor families on the same chip will allow leveraging the best properties of each material system. The high thermal stability on nitrides makes them especially attractive for their integration with Si and many potential applications will benefit in the near future from the hybrid circuits enabled by this integration.

ACKNOWLEDGEMENT

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