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Wafer-Scale 3D Integration of Silicon-on-Insulator RF Amplifiers

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***Abstract* - RF amplifiers are demonstrated using a three-dimensional (3D) wafer-scale integration technology based on silicon-on-insulator (SOI) CMOS process. This new 3D implementation reduces the amplifier size and shortens interconnects for smaller loss and delay. In addition, 3D integration allows the stacking of wafers fabricated using different process technologies to optimize the overall circuit performance at the lowest cost. In RF amplifier examples, MOSFETs and passive components are placed on separate tiers to reduce the size. Measured amplifier performance agrees well with simulation and footprint reduction of approximately 40% comparing to conventional 2D layout can be achieved.**

***Index Terms* – RF amplifiers, SOI, three-dimensional integration**

I. Introduction

Integrating circuits vertically in three dimensions (3D) allows the combination of circuits fabricated with application specific processes, such as logic, memory, imaging, and analog/RF, to realize higher functionality and smaller footprint of conventional 2D circuits. Although vertical integration can be realized in packaging or by bonding diced chips, a 3D wafer-scale integration technology using silicon-on-insulator (SOI) wafers [1] offers the smallest pitch and shortest interconnects between wafer tiers and it is fully compatible with standard backend process. This technology has been applied to high-pixel-density imagers [2] and high-speed digital circuits [3]. In this work, the 3D SOI integration is used to realize RF amplifiers, providing novel approaches of folding amplifiers vertically to reduce the overall size. It also shows that conventional simulation tools are still valid for circuit design and opens up new possibilities for more complex RF/mixed-signal circuit applications.

II. Design and Fabrication

The 3D integrated circuit consists of three tiers of high-resistivity SOI wafers processed with 180-nm fully depleted (FD) SOI CMOS technology. The thicknesses of the SOI and buried oxide (BOX) layers are 45 and 400 nm, respectively. After separately fabricating three 150-mm-diameter SOI wafers, each processed with a different mask set, the tier-2 wafer is bonded to the tier-1 wafer with circuit sides facing each other using a precision infrared aligner. After initial bonding at room temperature, the oxide bond is strengthened by annealing at 275ºC. No adhesive is used and three-sigma alignment accuracy better than 0.5 μm can be achieved. The Si substrate of the tier-2 wafer is then completely removed with a combination of grinding and wet etch using the BOX of the tier-2 SOI wafer as a hard etch stop. Interconnects between bonded wafers are then made by conventional via etch and metal fill using standard lithography. The typical diameter of the 3D via used in this work is 1.75 μm. This process is repeated to bond and interconnect the tier-3 wafer on top of the tier-2 wafer. The SEM cross section of a completed three-tier 3D IC is shown in Fig. 1. Except for the bottom tier-1 wafer, Si substrates of all upper tier wafers are completely removed and their circuits flipped. The vertical distance of active SOI devices between tier 2 and tier 1 is approximately 10 μm and is 6 μm between adjacent upper tiers.

In the first 3D integration run, all three wafer tiers are fabricated using our standard digital 180-nm CMOS process. A large n-MOSFET with total gate width of 1 mm is used in a single stage 3 GHz amplifier with reactive impedance matching to demonstrate the advantage of area reduction. The FET is divided into eight smaller cells, each with twenty five 5-μm-wide gate fingers. Tiers 1 and 3 have four FET cells each and tier-2 circuit consists of only a 0.6-nH spiral inductor for input impedance matching. Although using more or larger inductors can improve the impedance matching, the loss associated with the metal resistance diminishes any added advantage and it was not adopted to simplify the circuit design. As shown in Fig. 2, the signal is input from the top tier-3, and sent immediately to the inductor on tier 2. The signal is then split into two paths and separately amplified by the FETs on tiers 1 and 3. The amplified signals are recombined at the output on tier 3. Typical distance of 3D-via connected metal from adjacent tiers is 3 μm, which is shorter than most metal interconnects in the same tier. The amplifier has total of 256 3D vias, many of which are in parallel for redundancy and no attempt was made to optimize the placement of the 3D vias for area reduction. A metal pad on top of the 3D circuits is connected to the source of tier-3 FETs and acts as the heat sink, which has shown being able to lower the temperature rise of the FET in tier 3 by as much as 35% [4].

A second amplifier is also realized with integration of three tiers of FDSOI wafers. To demonstrate the versatility and advantage of mixing fabrication processes, the top tier in this 3D stack is fabricated with our RF CMOS process, which includes a metal T-gate [5] to lower

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the gate resistance and thick top metal and dielectric layer to reduce the loss of RF passive components. As illustrated in the schematic of Fig. 3, the amplifier uses a cascode configuration with total gate width of 600 μm for each FET. Shunt inductors used for input and output impedance matching require large bypass capacitors for low-loss DC isolation. The RF ground for the common-gate FET is also provided by a capacitor. These 9-pF large bypass capacitors are realized using MOS capacitors similar to the MOSFETs and are implemented on tier-2. Although three tiers are used in this 3D integration process, this amplifier has no circuit components on tier-1.

III. Results

High yield of 10,000-link 3D-via chains through all three tiers has been verified. The propagation delay of a 93-stage 3D ring oscillator with adjacent inverters in a different tier is 40.2 ps per stage, which is comparable to the 31.6 ps for the same circuit realized in a single tier. The extracted equivalent capacitance associated with a single 3D-via is approximately 2 fF. Measured scattering (S) parameters show that the resistance and inductance of a single 3D via are less than 1 Ω and 10 pH, respectively. The small parasitics associated with the 3D-via have little effect on the amplifier performance.

A. 3-GHz amplifier

As shown by the layout of each tier in Fig. 4, the footprint of this amplifier is dictated by the tier-2 inductor which measures 210 × 220 μm. This is achieved by splitting the active SOI FETs in two tiers. The overall footprint of this amplifier is approximately 40% smaller than that implemented in a conventional 2D circuit. In general, the performance degrades with growing size of the FET because of added parasitics, such as loss and delay, associated with feeding and combining increasing number of gate fingers [6]. For instance, measured f_T of a single-tier FET with 100 5-μm-wide gate fingers is 22 GHz, which is substantially lower than the 50.5 GHz of a 10-μm-wide FET with only 2 gate fingers. Therefore, it is important to minimize the combined distance to all the gate fingers. Figure 5 compares such distance of amplifiers with multiple gate-finger FETs split on two tiers with that laid out in a conventional single-tier 2D circuit. In the 3D amplifier, the FETs is stacked vertically and metal interconnects can be replaced with 3D vias. Because 3D vias provide shorter interconnect than the metal lines in 2D, the overall distance to the gate fingers can be reduced by more than 30%.

Measured and simulated results of the amplifier are shown in Fig. 6. The peak gain of the amplifier is 4.5 dB, measured at 2.8 GHz. The input and output DC biases are 0.7 V and 1.5 V, respectively, and the total current is 62 mA. The gain increases to 4.8 dB by increasing the output bias to 1.8 V. This rather modest RF performance is largely the result of using a fabrication process intended only for digital circuits instead of more desirable RF SOI process, which is used for the amplifier in the next example. The high resistance adds to the loss and prohibits extensive use of inductors, resulting in rather poor impedance matching and further impairs the amplifier performance.

Negligible difference in DC and S-parameter data of as-fabricated FETs in each tier and those in the 3D stack confirms that any effect of 3D integration process is minimal [4]. Good agreement between measured and simulated RF results verifies that the models derived for conventional 2D FETs are still valid for circuit design of all three tiers.

B. 10-GHz amplifier

In the second 3D integration run, the f_{max} of tier-3 T-gate MOSFET with ten 10-μm-wide gate fingers is 50 GHz and it increases to 55 GHz by adding the integrated top-metal heat sink. The f_{max} of tier-2 and tier-1 non-T-gate FETs, which are the standard devices for the digital CMOS process, is approximately 30 GHz due to the ~100 times higher gate resistance without the metal T-gate.

The photos of the amplifier components on tier-2 and tier-3 before 3D integration are shown in Fig. 7(a) and 7(b), respectively. The small squares on the die are metal fill patterns required for process uniformity. The photo of completed amplifier after integrating tiers 2 and 3 is shown in Fig. 7(c). The thick top metal, used for inductors, is patterned after all the bonding and thinning of every tier is completed. Note that circuits on tier-2 and tier-3 are flipped horizontally during 3D integration. Each MOS capacitor has 240 10-μm-wide gate fingers and measures approximately 80 x 190 μm. All capacitors are realized on the second tier with standard digital CMOS process as shown in Fig. 7(a).

To take full advantages provided by the RF CMOS process for performance, the cascode FETs and spiral inductors are all placed on the top tier. Although MOS capacitors are fairly large, they can all be implemented on tier-2 with a total area still smaller than the tier-3 circuit, which dictates the overall footprint of the amplifier. No circuit components are fabricated on tier-1, which is a waste of usable Si, but further splitting the circuit into tier-1 does not provide any more area advantages in this design. If RF CMOS process is available for more tiers, the FETs and inductors can be allocated into these tiers and further reduce the footprint. This amplifier example illustrates the importance of choosing processes and types of circuits to maximize the advantages of 3D integrated circuits.

Measured amplifier results are shown in Fig. 8. The peak gain is 7.9 dB at 9.4 GHz which is slightly lower than targeted 10 GHz. Because of a slight process modification, the output characteristics of the FET shifted

from the device model used for the initial circuit design. However, overall simulation is still fairly accurate without using different models for 3D integrated circuits. The high gain demonstrated by this amplifier also verifies that the relatively low gain of the 3-GHz amplifier is limited mainly by the digital-only CMOS process instead of 3D integration process.

IV. Conclusions

Three-level 3D wafer-scale integration has been used to implement RF amplifiers. These examples demonstrate only the advantage of area reduction compared to the conventional 2D circuits. Functionality can be increased by mixing different type of circuits, such as control circuits or memory. By folding the amplifiers vertically, the total interconnect length is shortened by substituting metal lines with 3D vias. These examples also point out the importance of efficiently allocating circuit components to different tiers to take full advantages of the 3D integration. However, our optimization for the 10-GHz amplifier is limited by the availability of only one tier of desired RF CMOS process, resulting in un-used tier-1 area. To design 3D circuits, process availability, performance goal, complexity, and cost all need to be considered simultaneously for optimal performance. Although the model and simulation tools are still valid for our circuits, modified 3D models will be needed to improve accuracy, such as including inter-tier coupling at higher frequencies.

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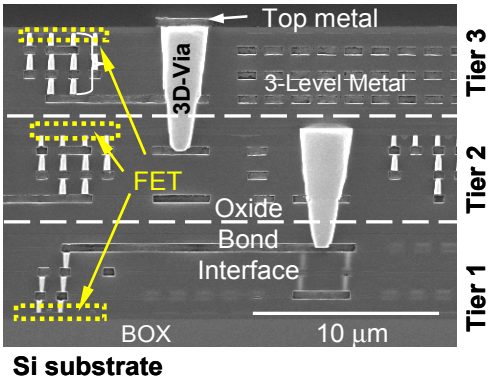

Fig. 1 SEM cross section micrograph of the 3D integrated circuits with 3 tiers of FDSOI wafers.

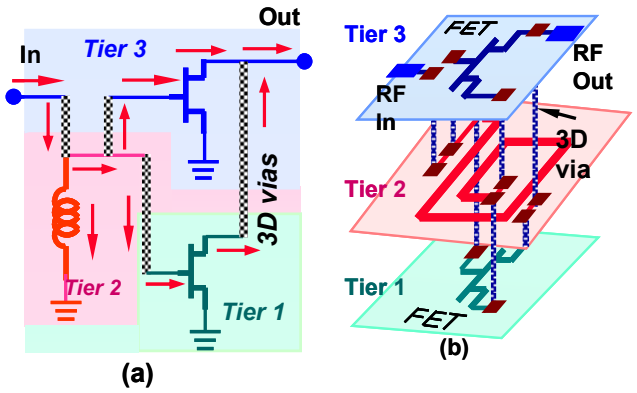

Fig. 2 Schematic diagram of 3-GHz 3D amplifier. (a) Circuit diagram and the signal paths. (b) Three dimensional view of the amplifier showing components in different tiers.

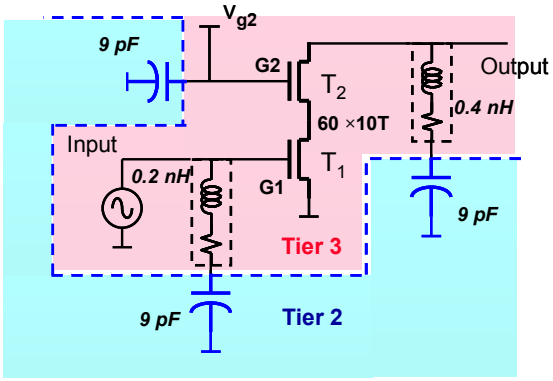

Fig. 3 Schematic diagram of the 10-GHz 3D cascode amplifier. The FET and inductors are in tier 3 while all the bypass capacitors are in tier 2.

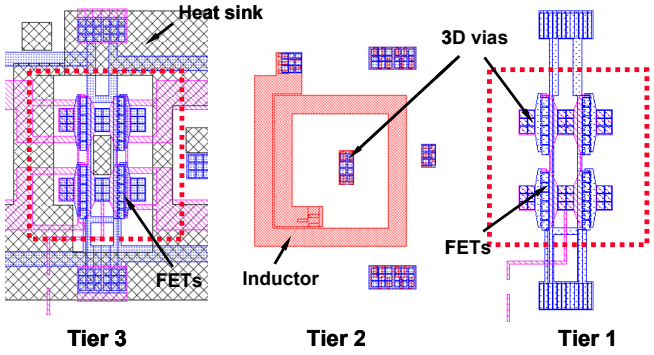

Fig. 4 Layout of 3-GHz amplifier in each tier. The dashed-line box shows the relative size of the tier-2 inductor in all three tiers.

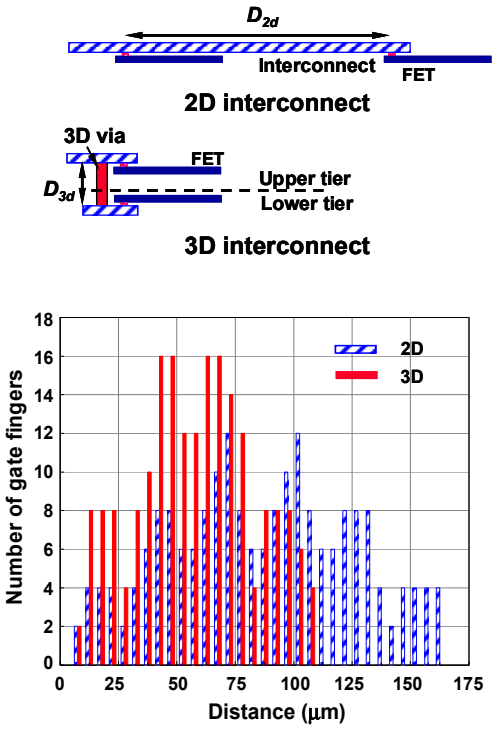

Fig. 5 Interconnects of FETs with multiple gate fingers are shortened in 3D integration by replacing metal lines with 3D vias. Plot shows distance of gate fingers from the input of the amplifier with a MOSFET of 200 5-μm-wide gate fingers in 2D and 3D configurations.

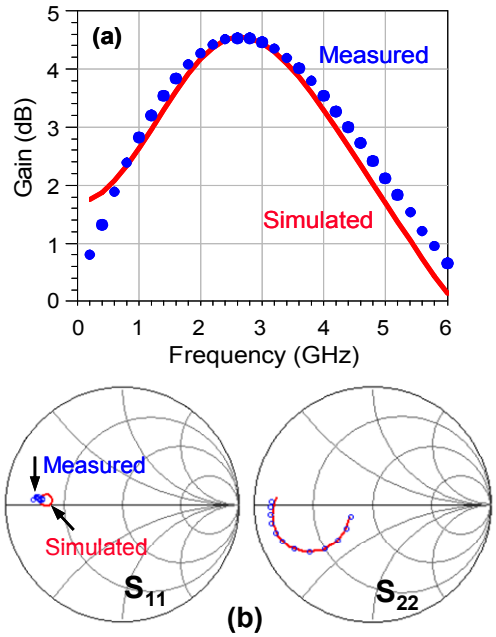

Fig. 6 Measured (circles) and simulated (solid curve) results of 3-GHz amplifier. (a) Gain. (b) Input and output S parameters from 0.2 to 6 GHz. The input and output DC biases are 0.7 and 1.5 V, respectively.

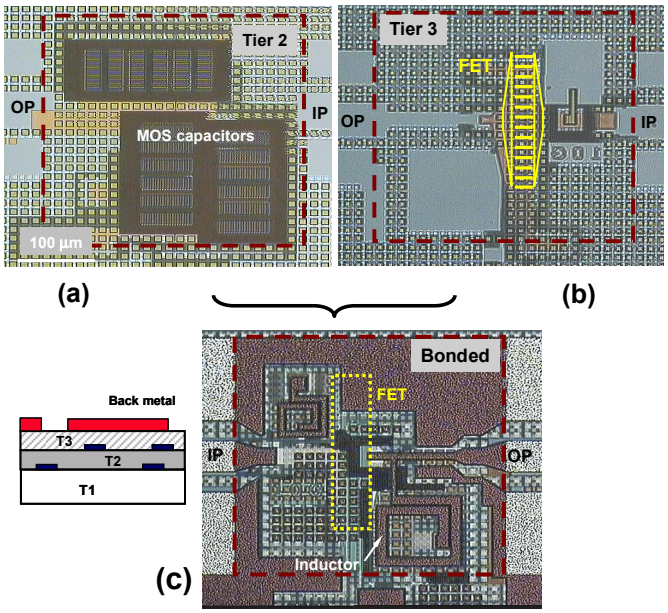

Fig. 7 Die photos of the 10-GHz amplifier. (a) Tier-2 before bonding. (b) Tier-3 before bonding. Dotted-line box is superimposed to highlight the location of the FET. (c) Finished amplifier after bonding tier-2 and tier-3 components. The final back-metal is patterned after bonding and substrate removal. The location of FET is highlighted for reference. Note that during bonding, both tier-2 and tier-3 wafers were flipped horizontally.

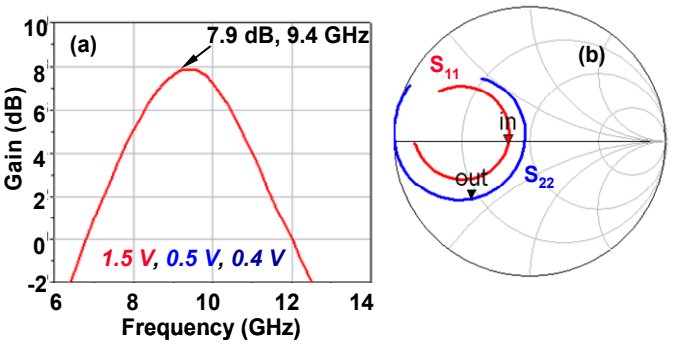

Fig. 8 Measured results of 10-GHz amplifier. (a) Gain. (b) Input and output S parameters from 6 to 13 GHz. The markers on S parameters plots are at 9.4 GHz. The output DC bias is 1.5 V and the gate biases for the common-source and common-gate FETs are 0.5 and 0.4 V, respectively.

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