Structure/Processing Relationships in Vapor-Liquid-Solid Nanowire Epitaxy

by

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ABSTRACT

The synthesis of Si and III-V nanowires using the vapor-liquid-solid (VLS) growth mechanism and low-cost Si substrates was investigated. The VLS mechanism allows fabrication of heterostructures which are not readily attainable using traditional thin-film metalorganic chemical vapor deposition (MOCVD). In addition to these heterostructures, the VLS mechanism allows exploration of Si substrates as platforms for advanced III-V devices, a long-standing goal of the III-V research community, because of the potential for significant cost reductions.

The approach to nanowire development first began by focusing on the binary Au/Si system. This system allowed us to understand critical parameters of our process including e-beam evaporation of Au thin-films, deposition of Au-colloid particles, pre-growth cleaning procedures and CVD growth conditions and times. Once controllable and repeatable Si nanowire epitaxy on Si substrates was established, we were able to focus on development of both III-V wires on Si substrates as well as Si substrates with topographic features and silicon-on-insulator (SOI) wafers.

Growth abnormalities between Au-colloid nanoparticle catalysts and Au thin-film catalysts revealed a correlation between Au coverage on the substrate surface and Si nanowire growth rate. We found an increasing growth rate with increasing concentrations of Au catalyst particles on the wafer surface. Systematic experiments relating the nanowire growth rate to the proximity of nearest-neighbor Au-particles and Au-reservoirs were carried out and the results were found to be in good agreement with a SiH_4 reaction model which associates decomposition to form SiH_2 with higher nanowire growth rates.

III-V nanowire growth on Si substrates was investigated as a possible route to the realization of high performance compound semiconductor devices on low cost substrates. For this study, GaP and InP were chosen as starting points for III-V nanowire integration with Si. Initial studies which focused on III-V wire epitaxy found that when Au-catalyst particles were treated with the group-III precursors before growth, there was an increase in the fraction of catalyst particles yielding wire growth and in the number of wires growing vertically from the substrate.

Axial nanowire heterostructures of $GaP_{(w)}/InP_{(w)}/GaP_{(w)}$ were fabricated using MOCVD on Si (111) substrates. Growth temperature was found to be critical in the formation of GaP/InP axial heterostructures with minimal simultaneous lateral

overgrowth of InP. Analysis of the second GaP segment on InP suggests that an increase in growth temperature while Au is in direct contact with InP results in the InP dissolving into the Au particle and disappearance of the heterostructure.

Si substrates were used as a foundation to explore more complex silicon structures, such as ordered arrays and SOI architectures. Although several routes initially looked promising for ordered array development, inverted pyramid arrays on Si (100) substrates were found to be the most successful. Silicon-on-insulator substrates were also explored for VLS nanowire growth and both Si nanowire field effect transistors and GaP nanowire cantilevers were successfully demonstrated on this platform.

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Figure 5.29 GaP nanowires grown on our SOI platform. The wires in a) and b) show both the wire growth on the top of the Si islands as well as horizontal growth from the {111} sidewall facets. The tilted SEM image in c) clearly shows the GaP cantilevers suspended over the BOX layer of the SOI substrate.

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1. Introduction and Context

1. Introduction and Context

Semiconductor growth and processing has been the most economically important, if not simply *the* most important area of materials research and development for the last 50 years. The relentless market for fast, small, and energy efficient products has pushed the semiconductor industry to adopt a cut-throat pace of research and development into device scaling [Figure 1.1] [1]. Many of the technological advances in the first 40 years of the semiconductor scaling age relied on problems which could be approached classically. However, as scaling continues, industry is finding problems which can no longer be approached classically. Materials of finite dimensions have properties which deviate from their bulk counterparts, yet do not quite reach into the atomistic regime are coined 'nanomaterials' and their structure/processing relationships are of great interest to the semiconductor community.

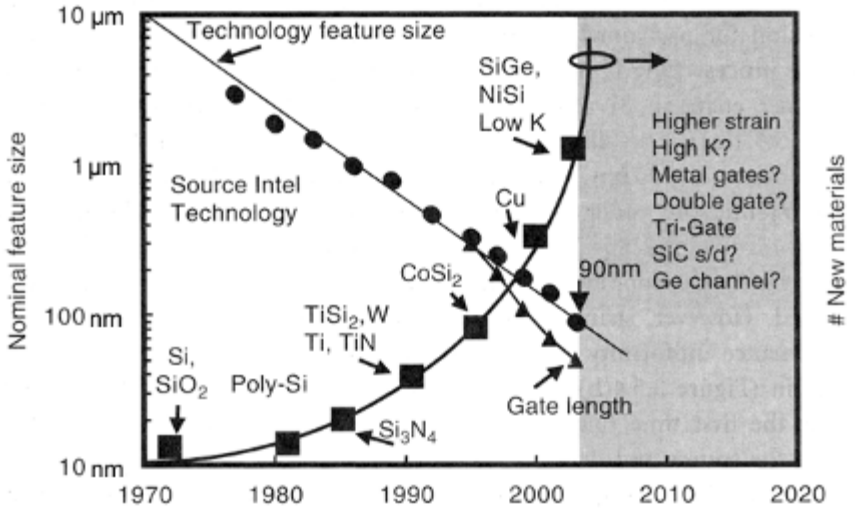


Figure 1.1 Plot of nominal feature size for transistors as a function of time, reproduced from [1]. While current (2010) technology has successfully scaled to the 32nm node through the use of things like High-K dielectrics and strained channels, the pathway to smaller node sizes has many technical hurdles which have yet to be addressed.

The scope of nanomaterials has implications to many different industries outside of semiconductors. From advanced composites which use carbon nanotubes and improve the toughness and lifetime of structural materials [8] to Fe-based nanoparticles which are used as biomarkers to improve MRI imaging [9], the impact of nanomaterials is undoubtedly tangible. Perhaps no nanomaterial is more pertinent to the semiconductor industry than Si and III-V 1-D, 'nanowire', geometries.

While the material's chemistry remains unchanged, altering the shape of the functional piece of a Si transistor or III-V light-emitting-diode might significantly impact the device's performance. In addition, unique properties of semiconductor nanowires may allow for new material combinations and interfaces which are otherwise impossible to fabricate in traditional semiconductor devices.

1.1 Light extraction enhancement

Light emitting diode technology has been under continual development since its inception nearly 50 years ago. The advancements made in both device design and material quality has enabled light emitting diodes to go from novelty indicators to light bulb replacements. The fundamentals of operation behind device operation have remained virtually unchanged throughout the years. Originally employing simple p-n junctions, light emitting diode technology now incorporates both quantum wells and quantum dots to enhance internal quantum efficiency. To date, significant progress has been made in material quality and device design which has enabled internal quantum efficiencies to approach nearly 100%[10] for some AlInGaP devices. Despite this tremendous success with internal quantum efficiencies, extraction efficiencies of LEDs

have not been able to reach the 100% level. Several techniques including chip-shaping [11], photonic crystals [12], and laser lift-off [13] have been able to increase extraction efficiencies of LEDs to the high 80% levels for specific wavelengths. However, the remaining 20% increase across the entire visible spectrum remains elusive. Furthermore, the processing techniques to create photonic crystals and shaped chips are often expensive, limited to specific geometries and inherently affect device yield. The demand for these LEDs is high enough to justify their unique processing, but any improvement to extraction efficiency with low cost of investment should prove to be important to the solid state lighting industry.

Nanowires inherently produce high extraction efficiencies due to their geometry and size scale. Snell's Law (Eq. 1.1) dictates the conditions for the angle of light reflection and transmission at an interface of two materials.

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 \qquad \text{(Eq. 1.1)}$$

When nanowire diameters below ~ 10^3 nm are combined with large refractive index differences, the efficiency of extracting light from a nanowire becomes substantial [14]. As the wavelength of light approaches the size of the structure from where it is being emitted, the opportunity for the light wave to become totally internally reflected and eventually reabsorbed is minimized. In a nanowire light will either be directly emitted from the edge of the wire or if it is wave-guided along the wire's long axis, it is likely to be emitted once it hits the wire's end [Figure 1.2].

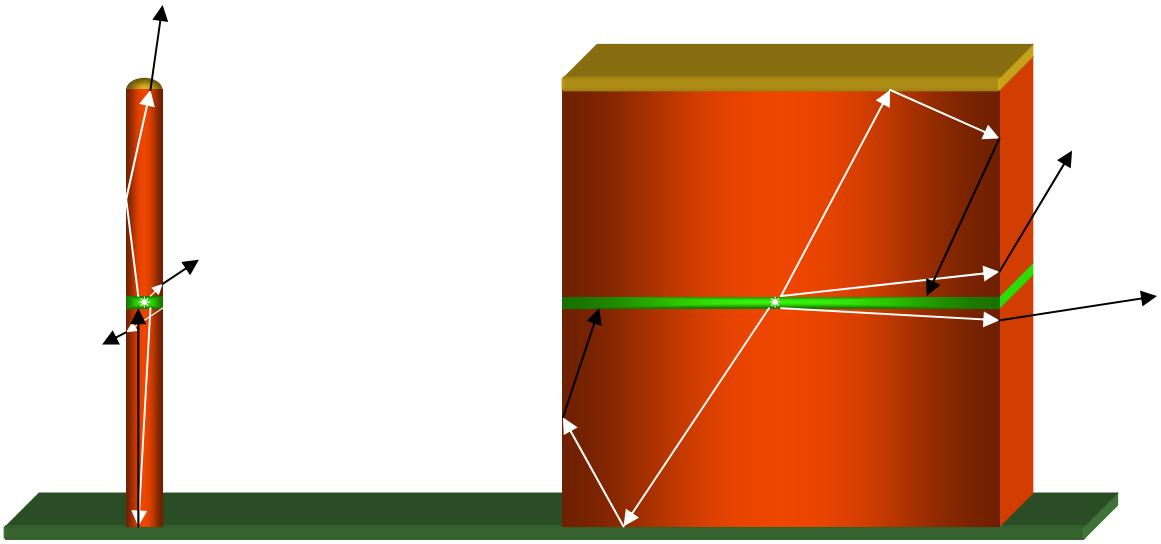


Figure 1.2 Schematic illustration of light emission in a nanowire and a conventional thin-film light emitting diode. Arrows indicate theoretical light reflections and emissions.

In addition, it is important to note that we are only considering nanowires between 20nm and 100nm. The critical wavelength, λ, which defines the crossover from conventional ray optics to quantum optics, is of the same order as the diameter of the wires we are fabricating. Therefore, in any realistic application of nanowire LEDs, the light emission and extraction should be at least partly governed by quantum or discrete processes as opposed to ray or continuous processes which are fairly well known [15].

Some preliminary experiments involving selective growth of GaN nanorods on sapphire substrates have shown substantial increases in light output compared to traditional LEDs with the same structure [16]. They cite a 4.3x increase in light emission from the GaN nanorod LEDs being facilitated by "a large sidewall surface area" because total internal reflection is minimized when the majority of light leaks out the LED sidewalls. In addition to increased light leakage, they note that the increase in LED efficiency is partly owed to the absence of threading dislocations which can hinder device

performance. This is evidenced by etched GaN LED structures which show an improvement in extraction efficiency, but are still hindered in any improvement of internal quantum efficiency because of existing threading dislocations from thin-film epitaxy.

1.2 Heterojunction engineering

Large band offsets between dissimilar materials provide the most efficient path for the electron-hole pair recombination responsible for light emission. Achieving these large offsets is only done by creating heterointerfaces of dissimilar materials. The principle difficulty in creating such a structure is maintaining high-quality crystalline junctions without creating defects which can act as non-radiative recombination centers for electron-hole pairs.

One of the most common approaches to creating defect-free heterostructures with significant band offsets in GaP and GaAs based systems is through the use of aluminum (Al) alloying. Al has the inherent ability to change the band structure of the material it's alloying with while not significantly changing the lattice constant. This minimizes the number of misfit dislocations and potential threading dislocations generated at the interface. However, there are several big limitations in this materials system. First the wider band gap of AlGaAs than GaAs defines the upper bound for the longest possible wavelength of light emission at that of GaAs's bandgap, ~870nm [Figure 1.3]. Secondly, the AlGaAs bandgap becomes indirect at about 45% Al mole fraction [17], which limits the lower bound for wavelength emission. In addition, as the AlAs fraction is increased, oxygen incorporation is also increased due to aluminum's affinity for oxygen bonds. This

has been shown to detrimental effects on radiative recombination in AlGaAs devices [18, 19].

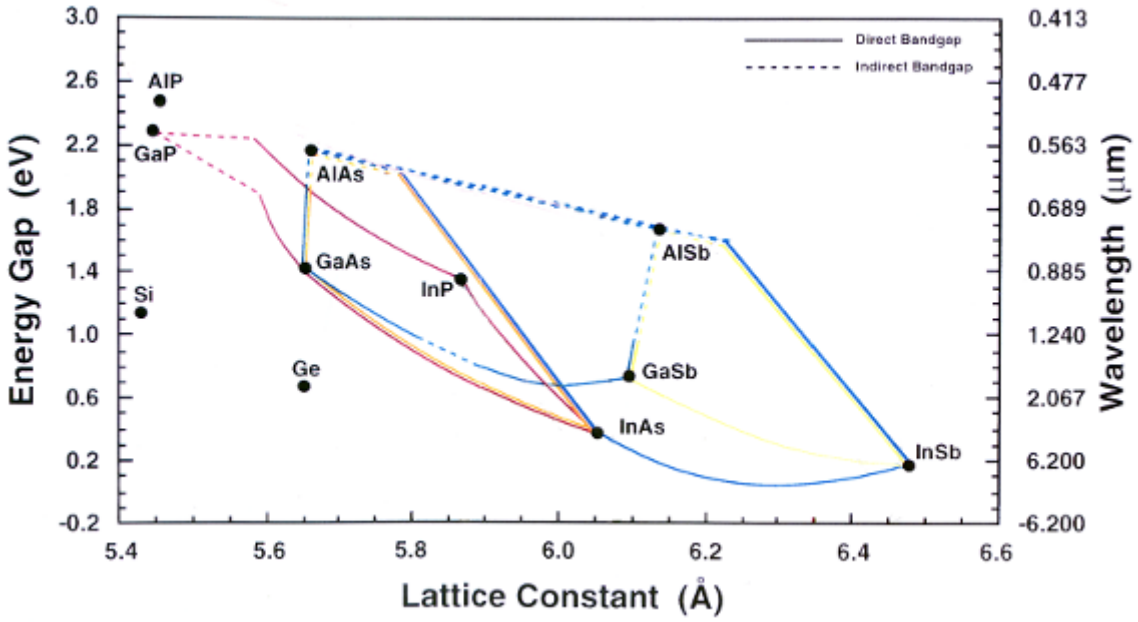


Figure 1.3 Energy gap and corresponding wavelength versus lattice constant for a wide range of III-V and group IV semiconductor materials. The lines indicate ternary III-V materials which are alloys of their respective endpoints. Figure adapted from V.G. Keramidas and R.E. Nahory.

To achieve emission wavelengths beyond the GaAs's infrared limit, indium (In) is often used as an alloying element. By alloying GaAs or GaP with In, the bandgap of the resulting ternary is decreased, thus allowing for devices with even longer wavelengths which are of key interest to the telecommunications industry. Another benefit of alloying with In is that it does not oxidize as rapidly and detrimentally as aluminum. Thus GaAs/InGaAs heterojunctions often have a more ideal type-I band alignment. Despite these advantages of using In as an alloying element for GaAs and GaP based devices, the significant challenge when creating these alloys is the accommodation the change in lattice constant from the addition of In. Unlike Al alloying, substitutional In atoms

increase the lattice constant of GaAs and GaP by non-trivial amounts. In some cases, this effect is a positive thing. For example, most all commercial red, amber and yellow LEDs are made of AlInGaP which is lattice matched to GaAs by the addition of In to AlGaP. Al is essentially used to control the band structure while In is used to match the lattice constant to the most viable commercially available substrate for this device, GaAs.

Lattice-matching is critical to thin-film optoelectronic devices. Strain between two differing materials must be accommodated in some way; In cases where a film is grown epitaxially on a substrate of a different lattice constant, the deposited film will initially stretch or compress to match the existing lattice [Figure 1.4]. As the film continues to grow, it will attempt to relax to its own lattice constant as each new layer is added. The thickness in which this happens is inversely proportional to the amount of lattice mismatch [20]. In cases where the lattice mismatch is high, it becomes thermodynamically favorable to generate defects in the growing film instead of absorbing strain in an additional layer. Typically in these cases, misfit dislocations form at the interface which allow the new film relax towards its preferred lattice constant. Dislocations must be nucleated from and terminated at a free surface. The most readily available free surface in thin-film epitaxy is the growth surface. Thus when a dislocation forms, it threads its way from the surface towards the interface to relieve stress. The threading dislocation through the length of the new layer is of primary concern for optoelectronic devices.

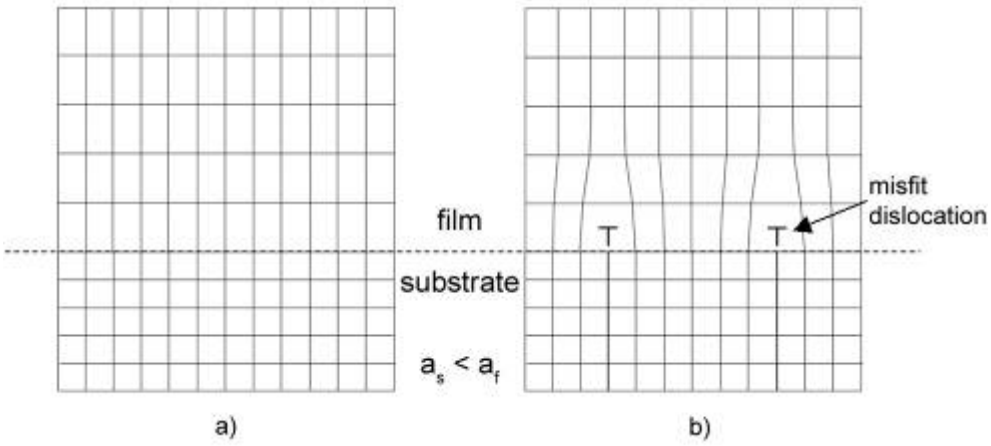


Figure 1.4 Schematic drawing of strain incorporation at lattice mismatched interfaces. Misfit dislocations are introduced at the interface to accommodate a change in lattice constant between the two materials. Figure reproduced from McGill[2]

Dislocations in semiconductor materials are detrimental to device performance. In optoelectronic devices, the broken bonds along dislocations provide energetically favorable sites, or traps, for electrons and holes to non-radiatively recombine. This significantly reduces device efficiency, performance and lifetime. Furthermore, in a high temperature environment, such as during operation, the mobility of dislocations can result in threading defects through the active region and ultimately provide a pathway for current shorting.

Although dislocations of serious concern for most electronic devices. Several methods have been employed which can limit dislocation nucleation. One method, mentioned above, uses In to lattice match device layers to commercially available substrates, as with AlInGaP on GaAs [21]. Another method employs graded layers, as with Ge on Si via SiGe [22]. This is a layer-by-layer technique where each layer is only slightly strained compared to the layer beneath it. By doing this, the lattice constant is slowly shifted such that no new dislocations are created and only existing dislocations are

used to relieve strain. Other methods such as selective area growth and epitaxial layer overgrowth employ the efficient use of geometry to control threading dislocations [23] and are of the most relevance to the work presented here.

Geometrical boundary conditions exploit the restriction of planes on which dislocations can lie and propagate. In the diamond cubic and zinc-blende crystal systems (Si, Ge, GaP, GaAs, InP, etc.) dislocations typically lie on {111} planes and are oriented in the <110> direction. Geometrically bounded growth ensures that even if dislocations to form the interface to relieve strain, they can be nucleated and terminated at a free edge or sidewall before reaching the surface. This method allows for columns or posts to change lattice constants relatively quickly without creating defects at the surface.

Axial nanowire heterostructures have significant advantages regarding dislocations and strain accommodation. In addition to the large amount of surface area which for dislocation termination, nanowires do not inherently have the same magnitude of biaxial strain compared to thin films. This strain strongly affects the distance over which the new film will relax in the direction normal to the substrate. In a nanowire the free surface can distort however is necessary for the lattice to relax to its equilibrium shape. By contrast, atoms in thin-films on substrates are effectively pinned by their neighboring atoms thus only near the free surfaces in thin films does the lattice relax. Models developed by Ertekin and Glas [3, 24] suggest that extremely high amounts of strain can be effectively accommodated into nanowire heterostructures than into thin-film heterostructures before dislocations nucleate to relieve strain [Figure 1.5]. In addition, it is important to note that the model proposed for strain accommodation in nanowires does not consider the role of kinetics in dislocation nucleation. Growth temperatures for

nanowire synthesis are often significantly lower than those used in thin-film epitaxy. At these lower temperatures, it may be difficult to for dislocations to overcome the activation energy barrier associated with nucleation.

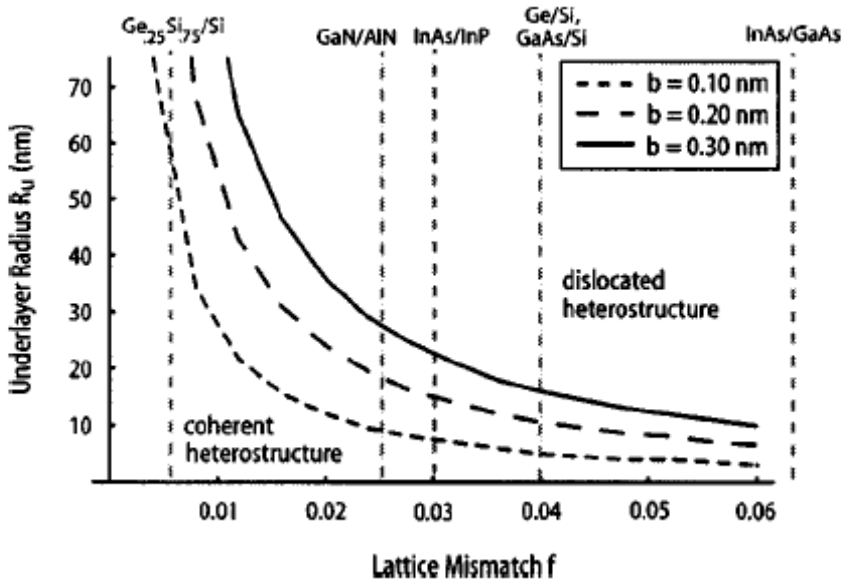


Figure 1.5 Equilibrium diagram illustrating regions in *f*, *Ru* space for which coherent and dislocated nanowire heterostructures are stable with respect to each other. Note the lattice mismatch for the InP/GaP system is greater than 0.07 and is not located on this plot. Figure reproduced from Ertekin, et al.[3]

New heterostructures enabled by nanowire geometry create the potential for new devices. Of particular interest here is the creation of a very strong type I band offset which cannot be created using thin-film epitaxy. To realize this, either InAs on GaAs or InP on GaP can be chosen as ideal systems. While most of the energies, and corresponding wavelengths, of interest between InAs and GaAs have already been developed for telecommunication applications, the band-gap energy near intrinsic GaP has yet to be adequately explored. AlInGaP has been developed previously to exploit the yellow and yellow-green wavelength close to the band edge of GaP. However, these devices suffer from the necessity of incorporating relatively high amounts of Al to create

the necessary band offsets. A GaP/InP/GaP double heterostructure does not theoretically need any Al to create the band offsets required for yellow and yellow-green light emission. Furthermore, it may be possible to create green or blue-green light emission from InP grown on AlGaP if enough confinement can be created between the two materials.

1.2.1 Nanowire Growth

Many methods are actively being explored for nanowire development. A 'top-down' approach to nanowire fabrication is perhaps the most actively pursued route by commercial researchers. This top-down approach utilizes photo-lithography combined with anisotropic etching to create one-dimensional structures with highly desirable electronic properties [Figure 1.6]. While this technique has only been recently enabled by developments in sub-micron lithography, the potential for seamless integration makes it very compatible with mass production needed for commercially viable technologies.

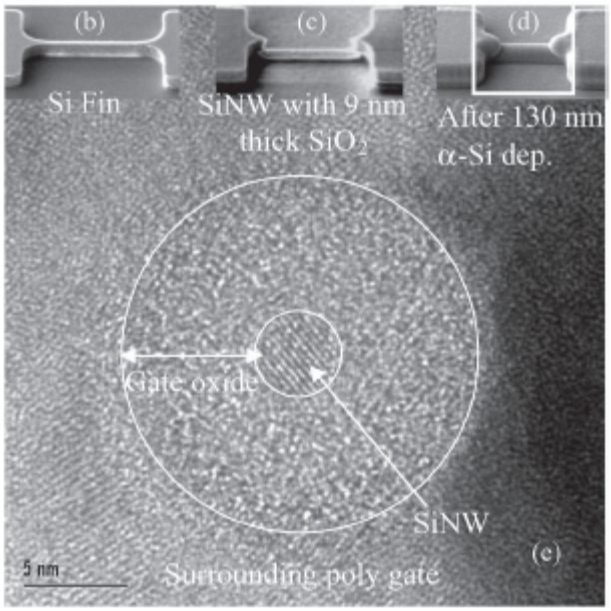


Figure 1.6 Top-down nanowire transistor fabricated by Singh, et al. using lithography. Note the process starts in b) with etching of a Si fin and then proceeds through additional processing in c) and d) to create the gate-all-around (GAA) configuration, seen in e). Figure reproduced from Singh, et al.[4]

Despite the possibilities of this technology, it is fundamentally limited by its top-down approach. Since epitaxy techniques are done in a layer-by-layer fashion, this leaves traditional lithography incapable of making one-dimensional lines which would extend through multiple epitaxial layers. Some groups have had success with opening a matrix of holes in a dielectric and subsequently growing epitaxially in selective areas [25]. These groups also take advantage of a small growth window which allows for primarily vertical pillar growth instead of lateral. However, despite some success with this method, the small processing window makes growth in these structures extremely difficult.

The other popular technique for nanowire growth takes what is essentially a 'bottom-up' approach to implementation. The vapor-liquid-solid, or 'VLS' method of nanowire growth was originally developed and explored in the 1960s by Wagner and Ellis [26] as a means of growing millimeter-scale single crystal 'whiskers' of silicon. This technique essentially involves three phases to achieve wire growth: A vapor phase precursor is used to supersaturate a liquid catalyst from which a solid phase single crystal is extruded [Figure 1.7]. This technique has been primarily characterized using the Au-Si system where Au is used as the catalyst material and some Si-based gas precursor is used to supersaturate and grow single crystal silicon.

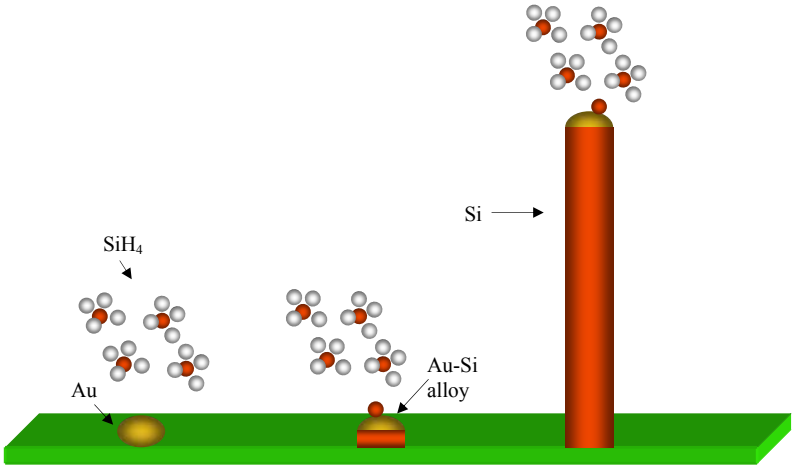


Figure 1.7 Schematic illustration of the VLS process. SiH_4 molecules in the vapor phase are flown over metal catalyst particles on a substrate. These molecules decompose preferentially at the catalyst to form a liquid droplet if the sample is held near or above the eutectic temperature. Lastly, a solid single crystal is extruded from the liquid melt.

The low solubility of Au in Si results in a low melting temperature eutectic point in the Au-Si phase diagram [Figure 1.8], and allows for VLS growth at temperatures around the eutectic melting temperature. Similarly, an analogous growth technique has been discovered for compound semiconductor materials [27] where vapor phase precursors of elements A and B can be used to saturate a metal catalyst and subsequently extrude a crystal of AB. Although the physical mechanisms for this type of crystal growth are not quite as well understood for compound semiconductors as they are for single elements, the success with this technique has made it very appealing to the semiconductor research community for future applications on the nano-scale.

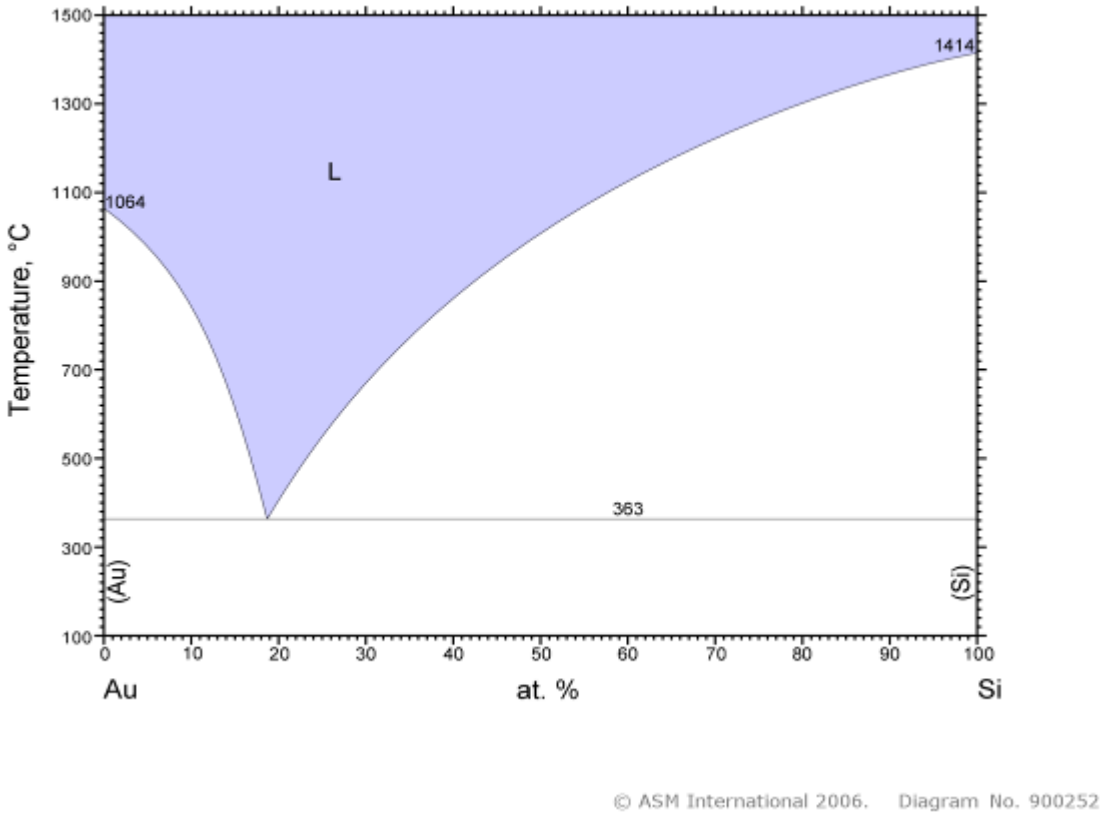


Figure 1.8 Au-Si phase diagram in atomic percent. The low eutectic temperature of 363 °C allows us to fabricate single crystal Si nanowires at growth temperatures much lower than those used for Si UHVCVD processes. Image reproduced from [5].

The device flexibility which the 'bottom-up' approach affords is especially attractive for a number of applications. Most semiconductor devices used in modern electronics have been based on planar epitaxy and 2-D structures. However, as mentioned previoiusly, it is only recently that 1-D structures have seen active research into their unique electronic and physical properties. While many theoretical calculations have explored the properties of nanowires in the so called 'quantum' regime, (below about five nanometer diameter) many properties of wires will deviate from their bulk and planar counterparts as they reach even 100nm in diameter. The origin of many of these

properties is not well understood beyond surface-to-volume ratios, which leaves much room for potential development of semiconductor devices between the bulk and quantum size regimes.

Most III-V and group IV semiconductor nanowires grown by the VLS mechanism typically show preferential growth along the <111> direction. This direction minimizes the surface energy of the exposed sidewall facets during growth. When the diameter of the nanowire reaches below around 20nm for Si, the preferential growth direction should theoretically switch to the <110> direction to minimize surface energy [28]. However, there are kinetic factors which can affect nanowire orientation [29], as is the case with most any equilibrium process.

Beyond the basic opportunities afforded by their 1-D geometry, VLS nanowires can be compositionally modulated either radially [30-33] creating a 'core-shell' structure or axially [34], creating superlattices along the length of the wire. This compositional modulation can be small to make n- and p- type material or can be significant and change materials altogether. This ability to readily change the nanowire composition theoretically enables a wide range of traditional devices to be fabricated in a new one-dimensional configuration. Many of the electrical and mechanical properties of these traditional planar devices break down as the geometry restrictions of nanowires change the models on which the devices are based. For example, the dramatically increased surface to volume ratio of nanowires is guaranteed to increase the number of surface states present for 1-D devices, however the impact of this new artifact has only begun to be adequately explored [25, 35].

1.3.1 Metal-organic chemical vapor deposition

The ability to grow nanowires using the VLS mechanism hinges directly on the ability to leverage gas-phase precursors which will decompose into appropriate semiconducting elements and compounds. Since different gases have different formulations and decomposition pathways, finding a compound which reacts in temperature and process window of interest is not always a given. For example, one of the primary reasons why the Au-Si system is so often chosen as the starting point for VLS nanowire research is because of gold's extreme nobility in most environments. Au has effectively no solubility of hydrogen or chlorine, the two elements with which Si is most commonly found in the gas phase. Once Au-Si has alloyed at temperatures above 360°C, it remains relatively stable in the liquid phase making many precursors available for nanowire growth (SiH_4, Si_2H_6, $SiCl_4$, $SiCl_2$, etc.).

Generally, the same gases used for thin-film growth are the ones used for nanowire growth. In the case of III-V's the group-III precursor is a metalorganic compound, such as trimethylindium, trimethylgallium, X-3Me. and the group-V precursor is phosphine, arsine, Y-H_3 or tertiarybutylarsine, tertiarybutylphosphine, (TBA, TBP). Similar to MOCVD the desired decomposition reactions should only be taking place at the surface site of interest. With the VLS mechanism, these are located on the Au catalyst particle and typically will have a lower energy barrier associated with that surface site than a site on the substrate.

The lower activation energy required for gas decomposition on the Au surface means a temperature window will exist such that most all reactions should be taking place on the catalyst and not on the substrate surface. Given that these reactions are

generally assumed to be typical chemical reactions with an Arrhenius temperature dependence, we assume that a negligible amount of adsorption and decomposition is happening on the substrate. This in turn causes the observed one-dimensional growth of VLS nanowires. The details of this growth mechanism are explored in more detail in Chapter 2.2.

2. Si Nanowire Growth

2. Si Nanowire Growth

For this research, silicon nanowires were chosen as the model system to develop and explore the VLS mechanism. In addition to the existing literature dating back to the 1960's, restricting the number of elements to that of the semiconductor and the metal catalyst helps simplify the VLS process. The addition of more precursors to create binary or ternary compounds via a metal catalyst significantly complicates the growth process as will be discussed in Chapters 3 and 4.

2.1 Parameter Space

The input variables for Si nanowire growth in our system are few. Before growth, substrate and catalyst materials must be selected and processed. During growth, our input variables are essentially limited to temperature and silane flow rate. Combinations of these different input parameters give us considerable room to explore and optimize nanowire growth. Although many of the input parameters may have complex interactions, e.g. annealing time before growth and catalyst thickness, we chose to start with the most 'upstream' parameters and optimize them in series as the parameter space for each became better understood.

2.1.1 Substrate Selection

The substrates chosen for the development of nanowires are all based on Si wafers. Si substrates are low-cost, readily available and provide a well known materials system to use as a starting point for nanowire development. Initially, Si wafers with a

native oxide were used as these were considered the most basic starting point from which to develop Si nanowire growth recipes. These oxide layers do not readily alloy with any of the potential catalysts we had planned to explore, thus we can investigate the catalyst and subsequent growth from the catalyst without complications from the substrate.

Once Si nanowires were demonstrated on native oxide substrates, growth efforts were then focused on homoepitaxial growth on Si <111> substrates. A <111> substrate has 4 <111> directions which point into free space from the substrate surface. A Si nanowire growing in one of the <111> directions of the substrate then has 4 equivalent options to pick for epitaxy. While growth in any of these 4 directions is epitaxial, selectively growing in the vertical direction is a benchmark for true control over the Si nanowire epitaxy and is dependant on a number factors including silane flow rate and substrate treatment prior to growth.

Early growths of Si nanowires on Si substrates were characterized by a relatively low fraction of Au catalyst particles yielding VLS nanowire growth [Figure 2.1]. A subsequent 10 sec dip in 1:1 HF:H_2O prior to growth revealed that a SiO_x forms on the surface of the Au catalyst when the Au catalyst is deposited directly on a hydrogen-terminated Si surface [Figure 2.2]. Si and Au are well known to rapidly inter-diffuse and even at room temperature this process occurs rapidly enough that Si will migrate through the catalyst particle and react with the ambient air to form an oxide shell all in a matter of minutes. Thus, all nanowire growths which employ a Si substrate also include an HF dip prior to growth which was later found to be consistent with Jagannathan, et al [36].

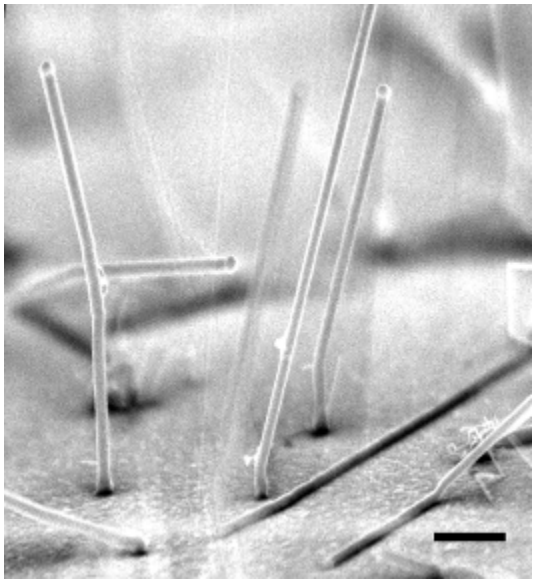


Figure 2.1 Tilted SEM image of Si nanowires grown on a Si (111) substrate using an e-beam evaporated Au catalyst. The native oxide in this case was not removed prior to growth, preventing smaller Au particles from facilitating wire growth. Scale bar is 500 nm.

Figure 2.2 Treatment of substrate in 1:1 HF:H_2O prior to growth for 10 sec revealed a drastic improvement in the fraction of Au catalyst particles yielding Si nanowires. Note that although the epitaxy here is imperfect, the range of nanowire diameters is much greater than those in Figure 2.1

2.1.2 Temperature

The MOCVD reactor allows for growth temperatures ranging from room temperature (~25^{o}C) to 800^{o}C. The substrate is heated by a graphite susceptor which sits directly above IR heating lamps. The graphite susceptor acts as large thermal mass which helps maintain stable temperatures inside the growth chamber. A thermocouple placed inside a quartz sheath and extends into a hole which has bored into the graphite susceptor. The thermocouple has three zones which measure the temperature at three points along the length of the susceptor. Despite the thermal controller's feedback loop which automatically adjusts the lamp power to maintain temperature, the thermocouple reading is still presumed to be about 40°C above the actual surface temperature due to the thermal gradient from the thermocouple location to the surface of the susceptor. In addition, the gaseous precursors are compressively stored in cylinders such that when they are used, the gas temperature drops considerably.

Despite the discrepancy between actual substrate and the thermocouple reading, the values taken from the controller unit were taken as the actual substrate temperature. This allowed for relative self-consistency from run to run, regardless of the substrates or gases used.

A temperature of 600°C was chosen as a starting point for Si nanowire growths. After a growth at 600°C, we observed significant wire growth [Figure 2.3] in addition to a Si thin-film on the reactor quartz tube, indicating non-selective SiH_4 decomposition to the Au-catalyst. Next, Si nanowire growth was explored at 500°C. However, few signs of Si nanowire growth were seen on these substrates [Figure 2.4]. Lastly, growth at 550°C was attempted and found to yield crystalline, non-tapering Si nanowires. After repeated

growths at 550°C, virtually no film deposition on the quartz tube could be observed so the Si nanowire growth temperature remained unchanged during these experiments.

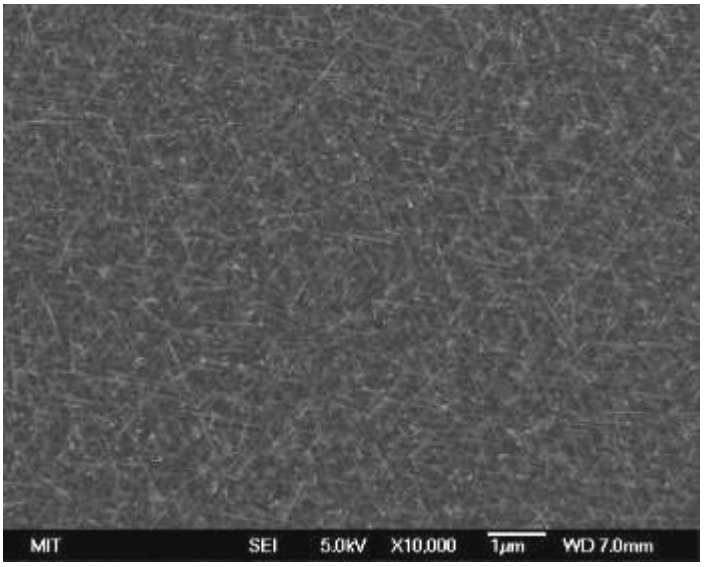


Figure 2.3 Silicon nanowires grown at 600°C. Despite the abundance of wires from this growth, a thin-film of Si was deposited on the quartz tube of the reactor, suggesting non-selective deposition to the Au-catalyst.

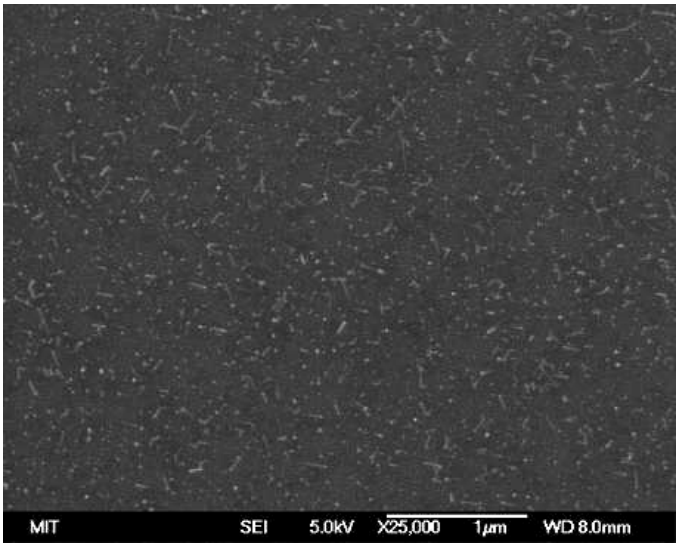


Figure 2.4 Silicon nanowires grown at 500°C. Despite several wires appearing to grow from the Au catalyst particles, the overall growth quality was considered to be poor compared to growths done at higher temperatures.

2.1.3 Flow Rates

In addition to the substrate and temperatures selected for each growth. Perhaps some of the biggest variability in wire morphology from run to run resulted from changes in silane flow. The carrier gas in all runs is held at 15 liters-per-minute (lpm) to ensure laminar flow. The silane MFC allows for a maximum of 100 standard cubic centimeters per minute (sccm), which is a relatively small amount of silane (0.67 %) compared to the carrier gas. When we also consider the boundary layer above the substrate, we can quickly conclude that changing the silane flow rate has essentially no effect on the laminar flow of the gas itself. Instead, the silane flow rate only changes the local partial pressure in the gaseous region directly above the substrate.

Initial growths used 15 sccm of silane balanced in H_2. For these growths, it was unclear if the silane flow would even be adequate to grow silicon nanowires using the VLS mechanism. Despite the success of these growths in realizing the VLS mechanism, the wires appear to be heavily kinked along their lengths [Figure 2.5]. Some initial review of the literature suggested that lower supersaturation levels of Si in Au catalyst might decrease the number of kinking defects along the length of the wires [37]. Dialing back the silane flow rate to 10 sccm nearly eliminated kinking defects along the length of the wires as seen in [Figure 2.6].

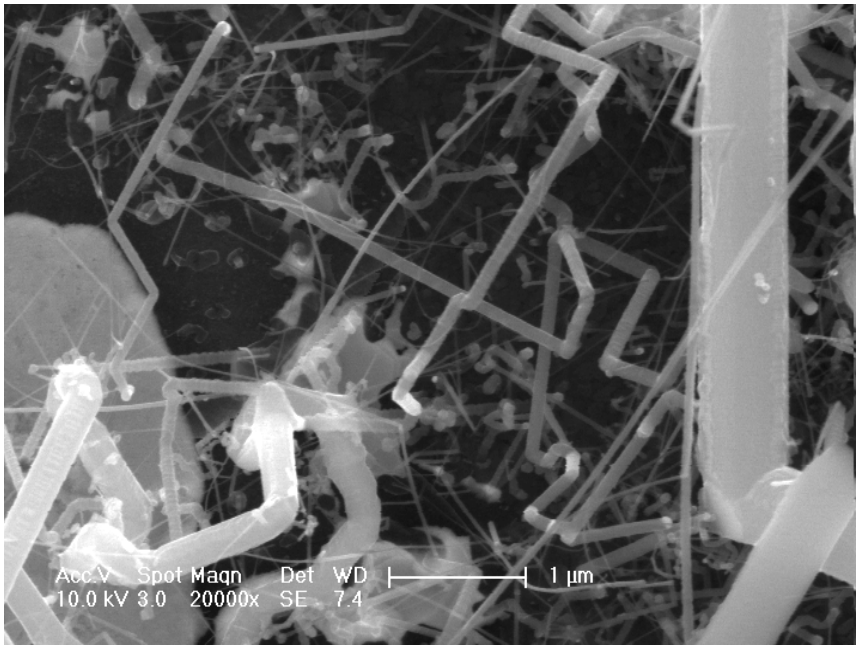


Figure 2.5 Top-down SEM image of Si nanowires grown on a Si (111) substrate using an e-beam evaporated Au catalyst. The silane flow rate in this case was ~15 sccm, which results in a large number of kinking defects. Scale bar is 1 um.

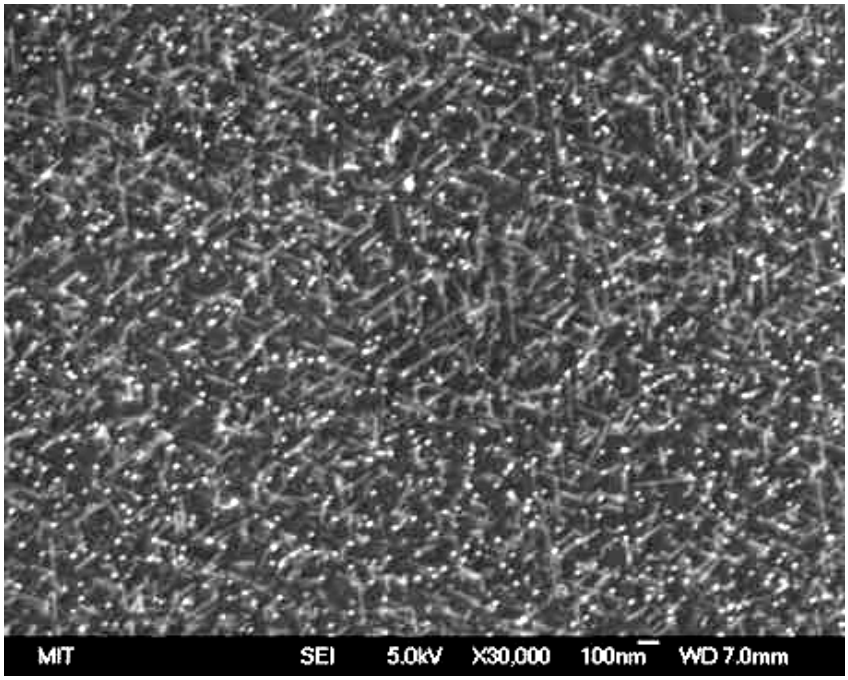


Figure 2.6 Growth at intermediate flow rates between 1 and 10 sccm SiH_4 consistently gave kink-free Si wires. However, the wires from these growths appear to be growing non-selectively to the normal <111> direction of the substrate.

Although we had some success with creating defect-free silicon nanowires, the epitaxy did not appear to be selective to the orthogonal <111> direction of the Si <111> substrate. Instead, the wires appear to grow unselectively in the 3 inclined <111> directions as well as the orthogonal <111> direction. Initially, the misorientation of wires growing in the inclined direction was thought to be the result of a kinking defect at the substrate-wire interface. However, as the kinking defects disappeared with a decrease in flow rate, this thought was virtually negated because epitaxy did not improve. An additional experiment attempting to seed Si nanowire growth at higher temperatures before continuing growth at a lower temperature also failed to show any improvement in vertical nanowire epitaxy.

Continuing on the trajectory of lower flow rates, Si nanowire growths were carried out at successfully lower flow rates from 10 sccm to 0.5 sccm. While not overly apparent at first, the number of kinking defects and wires growing in non-vertical <111> directions relative to the substrate decrease substantially as the flow rate (or partial pressure of silane P_{SiH4} since we are fixed at atmospheric pressure) is decreased [Figure 2.7]. Although difficult to quantify due to the homoepitaxial nature of Si on Si growth, qualitative post-growth SEM image analysis strongly suggested that lower silane partial pressures increase vertical epitaxy. Despite more wires appearing to grow vertically, a finite number of wires do not grow perpendicular to the substrate. Although at this point, our Si nanowires lack 100% yield in growing vertically from the substrate, growth on alternative substrates and platforms was developed and explored and is discussed in detail in Chapter 5.

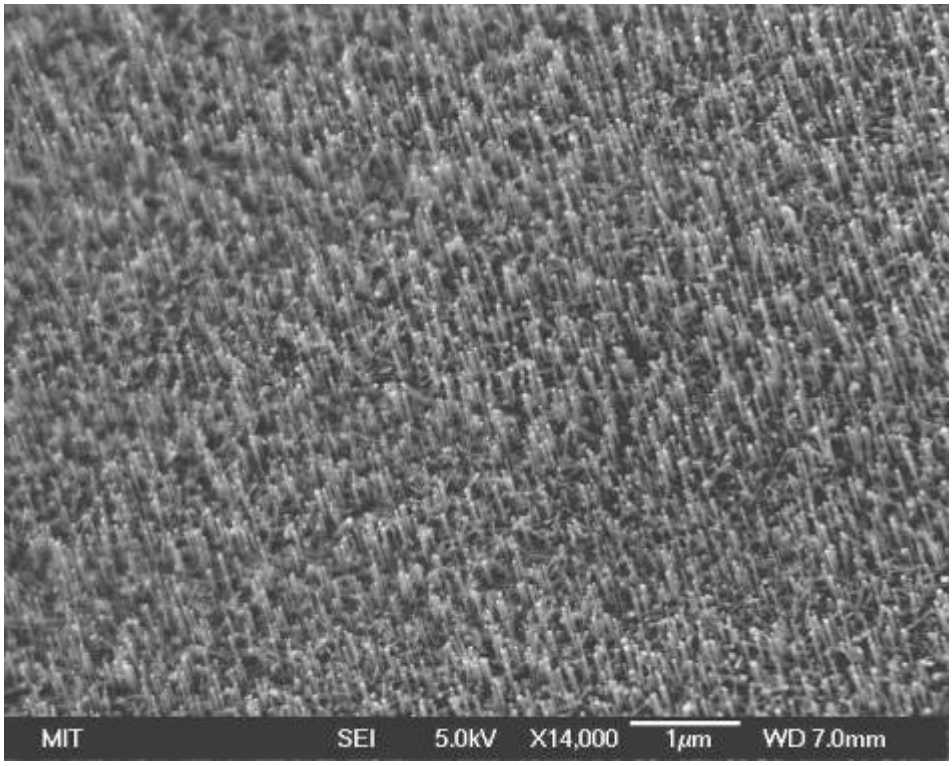


Figure 2.7 Tilted SEM image of Si nanowires grown on a Si (111) substrate using a 0.6-nm-thick e-beam evaporated Au catalyst. The flow rate of silane was ~0.50 sccm. Note that although the majority of the wires grow in the direction of the <111> normal to the substrate, a significant number of wires grow in other <111> directions. Scale bar is 1 um.

Silicon nanowire flow rate was further reduced from 0.50 sccm to 0.18 sccm with the growth time extended from 30 min. to 90 min. to produce wires of nominally equivalent length. When compared side by side to the wires grown at 0.50 sccm, there is a drastic increase in the vertical yield when the flow rate was reduced to 0.18 sccm [Figure 2.8]. This is somewhat surprising considering the minor differences seen in wire directionality when the flow rate was cut by an order of magnitude from 10 sccm to 0.50 sccm. Regardless, subsequent silicon nanowire growth leveraged the reduction in silane flow rate to produce nearly 100% vertical epitaxy yield. The correlation between the

decrease of silane partial pressure in the reactor and the corresponding increase in vertical nanowire epitaxy is consistent with some earlier findings [38, 39].

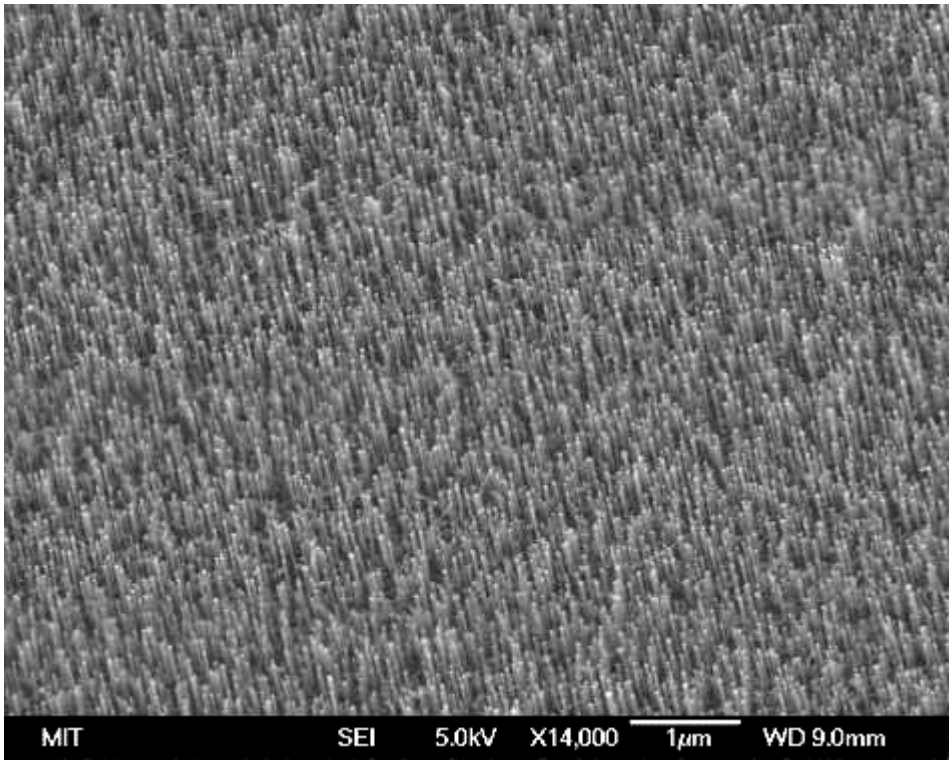
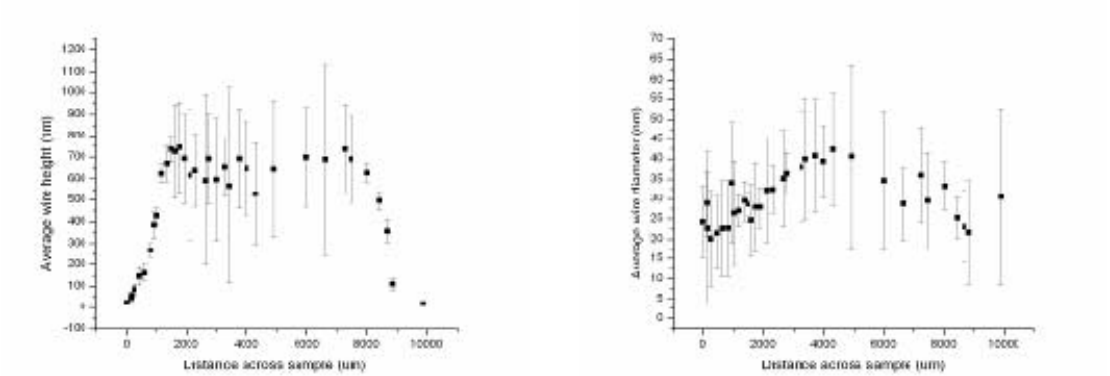


Figure 2.8 Tilted SEM image of Si nanowires grown on a Si (111) substrate using a 0.6-nm-thick e-beam evaporated Au catalyst. The growth conditions here are identical to those of Fig 3, except that the flow rate of silane is ~0.18 sccm. This difference appears to significantly improve vertical nanowire epitaxy. Scale bar is 1 um.

Later experiments (revealed that some of the vertical epitaxy might be dependant on the Au/Si substrate interface Chapter 2, Section b) and that the presence of any oxide may be a strong factor in whether or not a wire grows vertically from a (111) substrate. Partial pressure of the precursor then determines the likelihood of an instability occurring by which nucleation might occur on an inclined {111} facet of the Si substrate. This hypothesis was roughly supported by experiments where the time between individual steps such as oxide removal, Au deposition, and Si growth were minimized. Post-growth

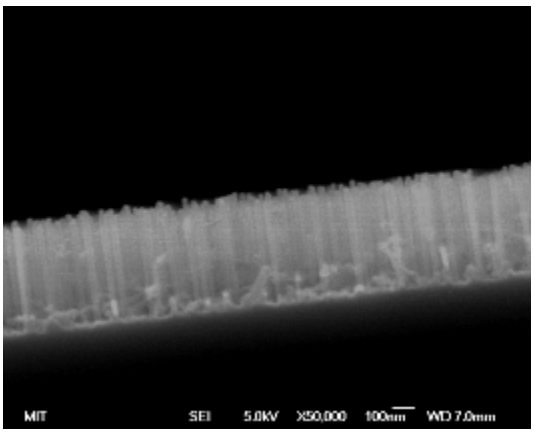
inspection of these samples revealed strikingly good vertical epitaxy yield despite having been grown using silane flow rates higher than 0.18 sccm.

Empirical evidence of the relationship between P_{SiH4} and epitaxial growth on Si (111) substrates can be seen by examining the length and directionality of wires across a sample. After Si nanowire growth using these optimal conditions, a sample was cleaved in half and imaged in SEM from one end to the other. Wire length and diameter was then measured at 37 points across the sample. The results shown in Figure 2.9a and 2.9b indicate a fairly linear gradient of growth rate in the edge exclusion region. However, towards the center of the sample we see a dramatic increase in the standard deviation of wire length. Comparing this transition to the wire images [Figure 2.10a, 2.10b], it is clear that the wires have reached some peak growth rate (P_{SiH4}) above which the Si wires no longer have a preference for the <111> direction normal to the substrate.



a) b)

Figure 2.9 Plots of average Si nanowire height (a) and diameter (b) as a function of distance across the sample diagonal cross-section. At each of 37 points, seven wires were measured at random for both length and height. The range is plotted as the error bars for both a) and b).

a) 

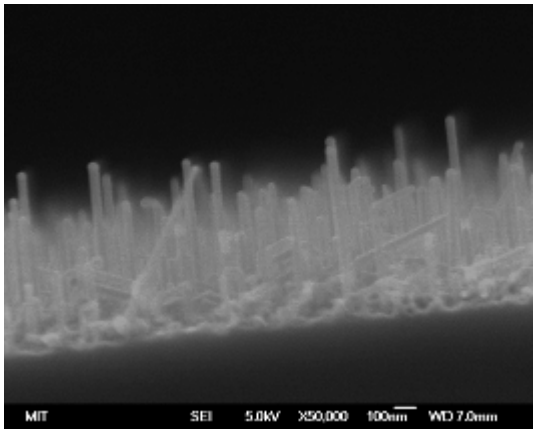
b) 

Figure 2.10 Cross-sectional SEM images taken from points 32 and 22 (of 37) are seen above in a) and b), respectively. Note the greater wire uniformity in a) than b), which is consistent with the measurements in Figure 2.9.

2.2.1 Catalyst Density Issues (adapted from [40])

This work is focused primarily on the relationship between Au-catalyst density and the Si nanowire growth rate. The ability to control the precise placement of the Au-catalyst particles and subsequent nanowire growth is fundamental to future nanowire integration. Borgström, et al [41] have suggested that the rate of III-V nanowire growth is affected by interparticle distance. Our preliminary experiments also show that isolated catalysts grow at very slow rates. Through a combination of reaction modeling and experimental design, we have identified a fundamental aspect of growth of Si nanowires using the VLS mechanism and a silane precursor in a cold-wall CVD system, where the precursor decomposition is selective to the catalyst surface. This observation has implications for device integration in the wide range of applications for which nanowires are potentially useful.

2.2.2 Experiments and Results:

Gold (Au) catalyst nanoparticles used in our experiments were made through two routes: 1) e-beam deposition of discontinuous Au films (Type 1) and 2) application and drying of Au-colloid solutions (Type 2). In order to optimize the recipe for vertical nanowire growth for our CVD chamber, we have used samples of type 1. Processing of type 1 can be easily controlled to yield an oxide-free Au catalyst template whereas the drying of Au-colloid solutions can leave residue of organics and oxide on the Au catalysts. Samples approximately 1-2 cm^2 were cut from lightly doped, *n*-type (<0.01 ohm-cm, As) Si(111) wafers. The wafer pieces were dipped in 50:1 HF:H_2O for 20 sec. to remove the native oxide and leave a hydrogen terminated surface. The samples for Au thin-film deposition were then immediately loaded into a Perkin Elmer e-beam evaporator and pumped down to 5 x 10^{-9} torr. Using a quartz crystal monitor for control, 0.6 nm of Au was deposited at 0.1 nm/min at room temperature. Au colloids were deposited by mixing various dilutions of H_2O with a 50nm aqueous Au colloid solution from Ted Pella Inc. Droplets of the solutions were placed in the center of each sample piece immediately purged with N_2. This process ensures both a clean Au-colloid – Si interface for epitaxy and simultaneously mitigates potential contamination from a poly-l-lysine adhesion layer [42]. Samples with Au pads serving as reservoirs were made on lightly doped, *n*-type (<0.01 ohm-cm, As) Si(100) wafer pieces. Photolithography, e-beam evaporation and lift-off were used to create patterns of pads. Au-colloid particles were deposited on these samples in the same way described previously.

Samples of both type 1 and type 2 were subjected to a second HF dip immediately before growth to ensure the removal of the silicon-oxide shell covering the metal catalyst.

Following oxide removal, the samples were loaded into a Thomas Swan atmospheric-pressure MOCVD reactor. This reactor has a custom designed quartz tube to ensure laminar flow of feed gas over a graphite susceptor and is traditionally used for III-V thin film growth. However, the double-dilution silane dopant line allows us to grow Si nanowires with a wide range of dilutions (20 sccm - 0.0002 sccm). The samples were purged first in 15 lpm of H_2 for a few minutes before the reactor temperature was brought up to 700^{o}C where it was held for 1 min. The temperature was then lowered to 550^{o}C for Si nanowire growth. This two-step pre-growth anneal and growth method has been adopted by several others and has been shown to improve nanowire epitaxy despite the fact that the exact cause is not certain [43, 44]. The growth temperature of 550^{o}C had been previously determined [Section 2.1.2] to be optimal for VLS silicon nanowire growth in our system.

The flow rate of SiH_4 was set to 0.18 sccm which minimized nanowire kinking as discussed above. Following this success in establishing controlled vertical nanowire epitaxy using e-beam films, Au colloid solutions were dispersed onto Si(111) wafers for nanowire growth. The samples were loaded into the reactor along with a piece of e-beam Au on Si(111) as a control. Nanowire growth was carried out to give the best vertical epitaxy for e-beam Au films on Si(111) using the same recipe as the one used to produce the wires in Figure 2.8. The contrast between the wires grown from Au colloids and e-beam films is clear [Figure 2.11a, 2.11b]. The wires from the Au colloid sample appear to be both full of kinking-type defects and are significantly shorter than the wires grown from e-beam films.

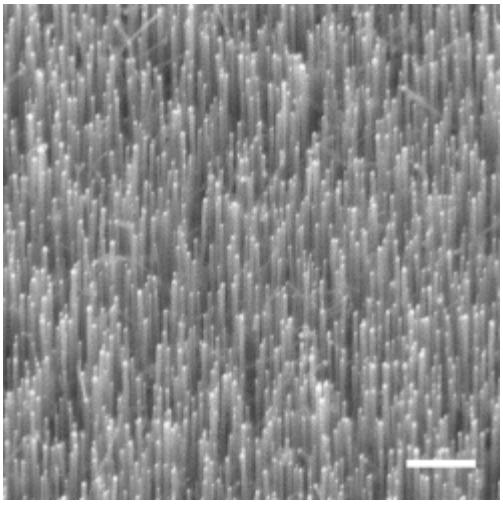
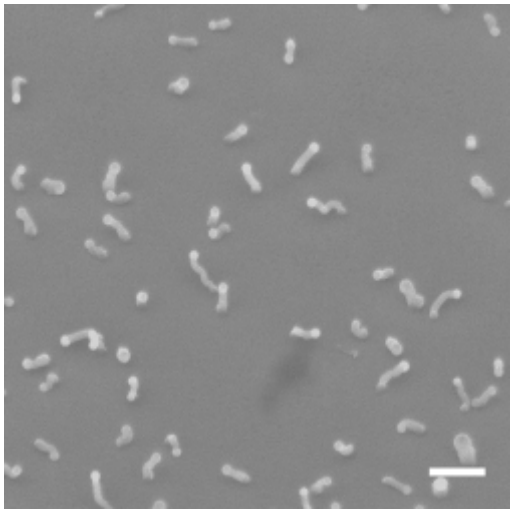
a)  b) 

Figure 2.11 Tilted SEM images of Si nanowires grown from e-beam evaporated Au catalysts a) and Au-colloid solutions b) on Si (111) substrates. The wires grown in a) grow predominately in the <111> direction of the substrate and are approximately 500 nm in length. The wires in b) exhibit poor epitaxy, as well as poor directionality and vary between 50 and 500 nm in total length. Scale bars are 500 nm.

An additional run was done to test Si nanowire growth from Au colloid particles. In this run, a drop of undiluted Au colloid solution was dispersed onto a piece of Si(111) and annealed in N_2 at 600^{o}C for 10 min. The samples were then HF dipped and loaded into the reactor. The sample was first annealed in H_2 at 700^{o}C for 10 min before being brought to 550^{o}C. The silane flow was increased for this growth from to 0.18 sccm to 10.0 sccm to eliminate any unforeseen artifacts related to diluted silane flow.

After growth the sample was inspected both at the edge of the Au-colloid solution droplet, as well as in the center region of the droplet. Images from the two regions are seen in Figures 2.12a and 2.12b. The average length of nanowires near the droplet edge is approximately ~6.8 um, whereas the average length of wires from the center region is only ~1.0 um. Wire growth was inspected around the circumference of the droplet and found to be fairly consistent. This helps rule out the possibility that precursor depletion associated with flow across the sample is affecting our results. The number of wires per

square micron is significantly greater in the region near the edge of the droplet, where the Au particle density is higher. This difference in Au colloid particle density is due to the 'coffee-stain effect' where particles in solution preferentially decorate the outer edge of a liquid droplet as it dries [45]. With everything else held constant in this run, the increase in the growth rate of wires at the outer edge of the droplet can be directly correlated with the increase in density of Au-colloid particles. The link between Au particle density on the surface of the sample and the growth rate of Si nanowires suggests that a synergistic effect between neighboring wires is present, as is the case for III-V wires as shown by Borgström, et al [41].

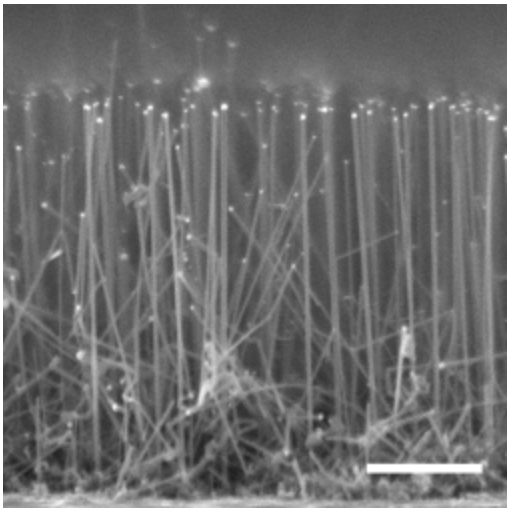
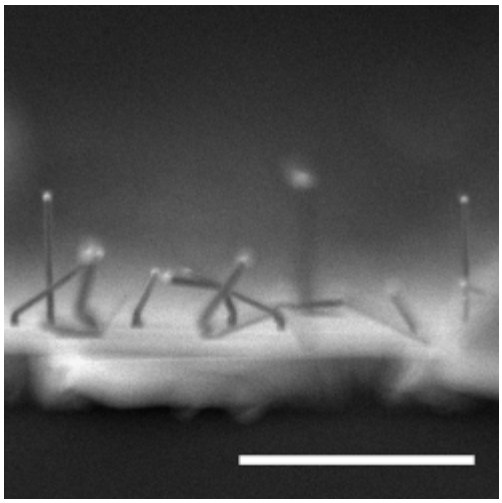
a)  b) 

Figure 2.12 Cross-sectional SEM images of Si nanowires grown from Au colloid solutions. Image a) was taken near the perimeter of the original droplet where the Au-colloid concentration is relatively high. Image b) was taken in the region near the center of the original Au-colloid droplet. The Au-colloid concentration here is significantly lower. Note the length of the wires in a) are considerably longer than the wires in b). Scale bars are 2.0 um.

A series of growths were carried out with varying dilutions of Au-colloids to explore the relationship between the Au particle spacing and the Si nanowire growth rate.

Dilutions of 0:1, 5:1, 50:1, and 100:1 were made by mixing DI water and Au colloid solution. The Au colloids in this case were dispersed onto Si(100) and Si(111) pieces and dried in flowing N_2 so as to prevent the coffee-stain pattern and give a more consistent spacing between particles. With a high rate of evaporation of the Au-colloid solution on the Si substrate, there is an inadequate amount of time to allow the nanoparticles to be driven towards the contact line by capillarity effects [45]. Silicon nanowires were then grown from these particles in the same manner as discusses previously with the initial anneal in N_2 at 600^{o}C from the previous growths omitted.

A series of SEM images were made at multiple locations on each sample. The numbers of Au-catalyst particles per unit area were counted and the lengths of the corresponding Si nanowires were measured and corrected for tilt and the <111> growth direction on the Si(100) substrates. A plot of nanowire growth rate versus interparticle distance is shown in Figure 2.13. The overall shape of the plot indicates a significant increase in the growth rate of Si nanowires around a spacing of 1.0 um between neighboring particles.

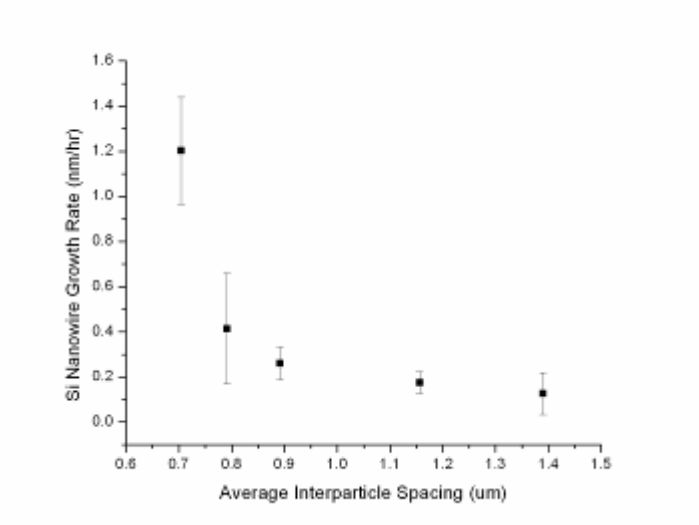


Figure 2.13 Plot comparing the Si nanowire growth rate versus the average interparticle spacing. Error bars in the y-direction were determined from the standard deviation of wire lengths in each image taken at the corresponding spacing.

Samples with Au-colloid particles interspersed among large patterned Au-reservoirs were fabricated to understand the role of exposed Au surfaces as they relate to nanowire growth. Photolithography, e-beam evaporation and lift-off were used to create Au patterns [Figure 2.14] of 30 nm, 60 nm, and 120 nm thickness on Si(100). Growth on these samples was carried out using the method described above where the samples were annealed for 10 min at 700 ^{o}C followed by 90 min of growth at 10 sccm of silane.

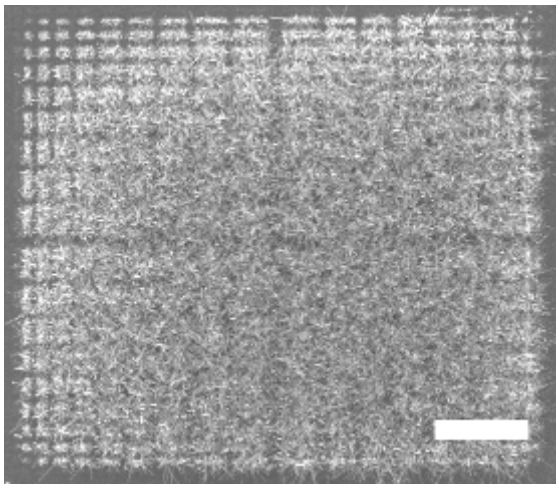


Figure 2.14 Top down SEM image of 60-nm-thick Au pads that serve as Au reservoirs after Si nanowire growth. Au-colloid particles were dispersed evenly across the surface of the wafer. Note that the reservoirs towards the center of the structure appear to have enhanced wire growth compared to the reservoirs along the outer edge of the structure. Scale bar is 50 um.

An SEM image series starting at 500 um away from the pattern edge to 100 um between the Au reservoirs is shown in Figure 2.15a. Representative images from this series are shown in Figure 2.15b-g. The length of each nanowire in the field of view of each image was subsequently measured and corrected for tilt. A summary of the

nanowire lengths and the respective distance from the Au reservoirs is shown in Figure 2.16.

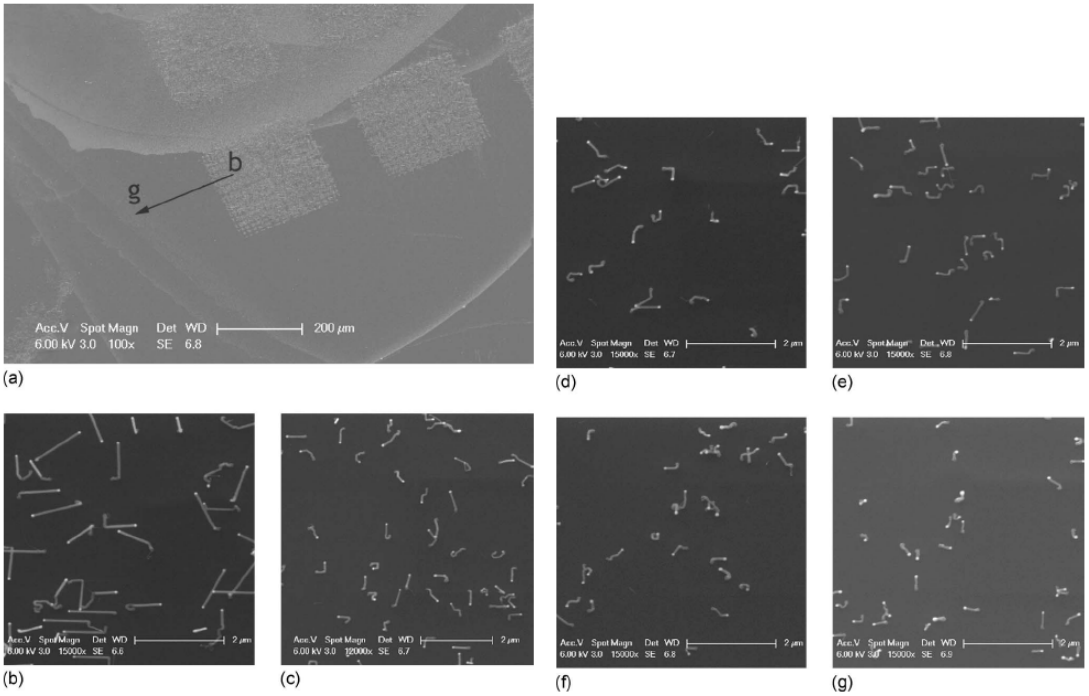


Figure 2.15 Image a) shows the line along which images b)-g) were taken. Images b)-g) show the change in wire length as the colloidal particles are progressively further from the reservoirs. Image 2.15b was taken between the Au reservoirs and 2.15g was taken ~200um away from the Au reservoirs.

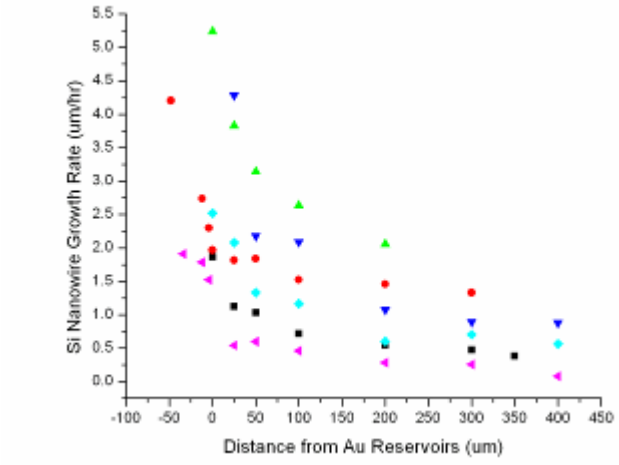


Figure 2.16 Plot of the nanowire growth rate vs. distance from Au reservoirs. Each color indicates a different set of Au reservoir thickness and colloid dilution. Negative values in distance indicate the wires

are growing between the channels of the Au reservoirs. (Pink Triangles – 30-nm-thick Au, 50:1 dilution ; Black Squares – 60-nm-thick Au, 0:1 dilution ; Light Blue Diamonds - 30-nm-thick AuPd, 0:1 dilution ; Red Circles – 30-nm-thick Au, 0:1 dilution ; Dark Blue Triangles - 120-nm-thick Au, 0:1 dilution ; Green Triangles – 120-nm-thick Au, 0:1 dilution)

The shape of the curve in Figure 2.16 is very similar to that of the curve in Figure 2.13. However, the relevant length scales in this case are much greater than with Au-colloid particles without near-by reservoirs. From the data it appears that Au reservoirs as far as 300 um away from the Au colloid particles may be affecting the growth of Si nanowires.

The nanowires growing in proximity to 120nm pads seem to exhibit a slightly higher growth rate than the wires growing the same distance from 30nm thick pads, even though the relative particle density is comparable. This suggests the ~10% increase in surface area of the 120nm pads can have an effect on the growth of nanowires in the near vicinity.

2.2.3 Model

To explain the correlation between enhanced growth rate and the local concentration of Au, we consider a model for SiH_4 decomposition and subsequent wire growth. First, we consider a simple reaction for silane decomposition on the catalyst surface [46]. This can be described by equation (1) if we assume direct decomposition of silane to form Si on the surface of the catalyst. This makes the silicon nanowire growth rate directly proportional to rate of reaction (1).

$$SiH_4(g) \rightarrow Si(s) + 2H_2(g) \quad (1)$$

Next we consider the physical process behind this reaction leading to Si nanowire growth. Reaction (1) can be broken down into four steps,

$$SiH_4(g) \rightarrow SiH_4^* \quad (2)$$

$$SiH_4^* \rightarrow SiH_4(g) \quad (3)$$

$$SiH_4^* \rightarrow Si(s) + 2H_2^* \quad (4)$$

$$2H_2^* \rightarrow 2H_2(g) \quad (5)$$

where an asterisk is used to indicate a surface-adsorbed species. Given a limited number of equivalent surface sites available for each reaction to take place, we denote each type of site independently as a fraction of the total sites available.

$$\Theta_{empty} + \Theta_{SiH_4^*} + \Theta_{2H_2^*} = 1 \quad (6)$$

Assuming first order reaction rates for (2) - (5), we define the following:

$$r_{SiH_4} = f_{SiH_4} p_{SiH_4} \Theta_{empty} \quad (7)$$

$$r_{-SiH_4^*} = f_{-SiH_4^*} \Theta_{SiH_4^*} \quad (8)$$

$$r_1 = f_{r_1} \Theta_{SiH_4^*} \quad (9)$$

$$r_{-2H_2^*} = f_{2H_2^*}\Theta_{2H_2^*} \qquad (10)$$

Where r_x represents the rate of each reaction and f_x is the reaction rate constant for reaction x. In addition, we recognize that in the steady state the growth rate, or eqn. 9 in this case, must be equal to eqn. 10, since neither can exceed the other (eqn. 11). In addition, the adsorption rate of silane (eqn. 7) must be equal to the sum of eqn. 8 and eqn. 9, giving eqn.12.

$$r_1 = r_{-2H_2^*} \qquad (11)$$

$$r_{SiH_4} = r_1 + r_{-SiH_4^*} \qquad (12)$$

Using equations (6) - (12) we find the following form for silicon nanowire growth rate in the steady state

$$r_1 = \frac{f_{r_1} f_{SiH_4} p_{SiH_4}}{f_{-SiH_4^*} + f_{r_1} + \left(1 + \frac{f_{r_1}}{f_{-2H_2^*}}\right) f_{SiH_4} p_{SiH_4}} \qquad (13)$$

Now we examine the rate-governing regimes of eq. 13 to understand a possible dependence on Au catalyst surface density. Increasing the Au concentration could, in principle, affect the probability in the reaction rate constant pre-factor of the silane

adsorption term, f_{SiH_4}. However, this only is relevant in cases where p_{SiH_4} is small and thus we would also expect a dependence on p_{SiH_4},

$$r_1 \approx \frac{f_{r_1} f_{SiH_4} p_{SiH_4}}{f_{-SiH_4^*} + f_{r_1}} \qquad (14)$$

Examining the wires in Figures 2.11b and 2.12a, a proportionality of P_{SiH4} to growth rate, r_1, was seen at reasonably dense Au-colloid concentrations. The growth rate in Figure 2.11b was approximately 2nm/min at 0.18 sccm and increased to 75nm/min at 10 sccm, as shown in Figure 2.12a. However, as shown in Figure 2.12b when the Au-colloid concentration is low, the growth rate is *not* proportional to P_{SiH4}, thus ruling out the Au-colloid's effect on the reaction rate constant term.

In the case where more Au in the vicinity of a growing nanowire might increase the pre-factor of the Si incorporation reaction, f_{r_1}, we would expect to find a dependence that should theoretically asymptote as the probability of this reaction occurring is increased (eqn. 15).

$$r_1 \approx \frac{f_{r_1} f_{-2H_2^*}}{f_{-2H_2^*} + f_{r_1}} \qquad (15)$$

This is also negated by the data in Figures 2.13 and 2.16 as the growth rate continues to increase as the amount of Au in the near vicinity is increased.

The growth regimes allowed in the model described by equations 1 and 13 do not seem to be supported by the experimental evidence from Si nanowire growth using Au-colloid particles with and without relatively large volumes of patterned Au, or 'reservoirs', nearby. To understand this, a more complex model was then evaluated for which it was assumed that an initial decomposition step from silane to silylene (SiH_2), shown in equation 16, is followed by silylene reaction to form adsorbed Si and wire growth.

$$SiH_4(g) \rightarrow SiH_2(g) + H_2(g) \rightarrow Si(s) + 2H_2(g) \qquad (16)$$

This is often assumed to be the likely decomposition path for silane [47, 48].

Similarly to reaction 1, reaction 16 can be expanded into eight steps:

$$SiH_4(g) \rightarrow SiH_4^* \qquad (17)$$

$$SiH_4^* \rightarrow SiH_4(g) \qquad (18)$$

$$SiH_4^* \rightarrow SiH_2^* + H_{2_1}^* \qquad (19)$$

$$H_{2_1}^* \rightarrow H_2(g) \qquad (20)$$

$$SiH_2(g) \rightarrow SiH_2^* \qquad (21)$$

$$SiH_2^* \rightarrow SiH_2(g) \qquad (22)$$

$$SiH_2^* \rightarrow Si(s) + H_{2_2}^* \qquad (23)$$

$$H_{2_2}{}^{*} \rightarrow H_2(g) \qquad (24)$$

Again, the surface sites are defined by the fraction of the total number of sites occupied by the various adsorbed species:

$$\Theta_{empty} + \Theta_{SiH_4{}^{*}} + \Theta_{SiH_2{}^{*}} + \Theta_{H_{2_1}{}^{*}} + \Theta_{H_{2_2}{}^{*}} = 1 \qquad (25)$$

The reaction rates are defined by their respective reaction rate constants and site availability.

$$r_{SiH_4} = f_{SiH_4} p_{SiH_4} \Theta_{empty} \qquad (26)$$

$$r_{-SiH_4{}^{*}} = f_{-SiH_4{}^{*}} \Theta_{SiH_4{}^{*}} \qquad (27)$$

$$r_1 = f_{r_1} \Theta_{SiH_4{}^{*}} \qquad (28)$$

$$r_{-H_{2_1}{}^{*}} = f_{-H_{2_1}{}^{*}} \Theta_{H_{2_1}{}^{*}} \qquad (29)$$

$$r_{SiH_2} = f_{SiH_2} p_{SiH_2} \Theta_{empty} \qquad (30)$$

$$r_{-SiH_2{}^{*}} = f_{-SiH_2{}^{*}} \Theta_{SiH_2{}^{*}} \qquad (31)$$

$$r_2 = f_{r_2} \Theta_{SiH_2{}^{*}} \qquad (32)$$

$$r_{-H_{2_2}{}^{*}} = f_{-H_{2_2}{}^{*}} \Theta_{H_{2_2}{}^{*}} \qquad (33)$$

Note that although silylene is only produced by reaction 19, both silane and silylene must compete for the same vacant surface sites. It is also assumed here that H_2 does not re-adsorb to the surface once it is in the gas phase.

In the steady state, the following conditions must hold:

$$r_1 = r_{-H_{2_1}^*} \tag{34}$$

$$r_2 = r_{-H_{2_2}^*} \tag{35}$$

$$r_{SiH_4} = r_1 + r_{-SiH_4^*} \tag{36}$$

$$r_{SiH_2} = r_2 + r_{-SiH_2^*} \tag{37}$$

Solving the system of equations (25) – (37) for r_2 in terms of the reaction rate constants and partial pressures of the reactants yields (38).

$$r_2 = \frac{1}{\dfrac{1}{f_{-H_{2_2}^*}} + \dfrac{1}{f_{r_2}} + \dfrac{\left(1 + \dfrac{f_{-SiH_2^*}}{f_{r_2}}\right) f_{SiH_4} \left(\dfrac{1}{f_{-H_{2_1}^*}} + \dfrac{1}{f_{r_2}} + \dfrac{1 + \dfrac{f_{-SiH_4^*}}{f_{r_1}}}{f_{SiH_4} p_{SiH_4}} \right) p_{SiH_4}}{f_{SiH_2} \left(1 + \dfrac{f_{-SiH_4^*}}{f_{r_1}}\right) p_{SiH_2}}} \tag{38}$$

In this analysis it is assumed that some fraction of the incoming silane will be converted to silylene. This fraction remains relatively constant during nanowire growth for a given condition in steady state. We introduce a parameter, β, which represents this fraction

$$\beta = \frac{p_{SiH_4}}{p_{SiH_2}} \qquad (39)$$

Substituting equation 39 into equation 38 gives equation 40:

$$r_2 = \frac{1}{\dfrac{1}{f_{-H_{2_2}^*}} + \dfrac{1}{f_{r_2}} + \dfrac{\left(1+\dfrac{f_{-SiH_2^*}}{f_{r_2}}\right) f_{SiH_4} \left(\dfrac{1}{f_{-H_{2_1}^*}} + \dfrac{1}{f_{r_2}} + \dfrac{1+\dfrac{f_{-SiH_4^*}}{f_{r_1}}}{f_{SiH_4} p_{SiH_4}} \right) \beta}{f_{SiH_2}\left(1+\dfrac{f_{-SiH_4^*}}{f_{r_1}}\right)}} \qquad (40)$$

Note that when $\beta = 1$, all silane is converted into silylene. When $\beta = \infty$, silylene production becomes the bottleneck and r_2 is quenched, which stops Si nanowire growth.

2.2.4 Discussion and Conclusions

To examine the form of r_2, a term proportional to the wire growth rate, all reaction rate constants were set to a fixed value and p_{SiH_4} and β were chosen as input

variables that describe the gas concentration within the boundary layer. A plot of r_2 vs. p_{SiH_4} for several values of β is shown in Figure 2.17. Clearly r_2 has little dependence on p_{SiH_4} except at extremely low values of p_{SiH_4}. This is supported by previous experiments where an increase in silane flow did not increase the growth rate of silicon nanowires.

Next, r_2 is plotted as a function of β for several values of p_{SiH_4}, seen in Figure 2.18. As β is increased from 1 to ∞ the nanowire growth rate drops off tremendously. For a fixed value of approximately $\beta > 40$ the nanowire growth rate is insignificantly increased as p_{SiH_4} is increased.

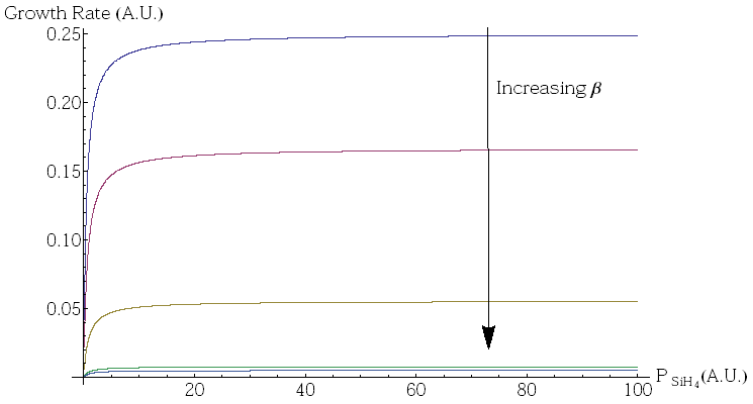


Figure 2.17 Plot of r_2 vs. p_{SiH_4} for several values of β, ranging from 1 to 100. The growth rate quickly asymptotes to a fixed value regardless of p_{SiH_4} for a fixed value of β.

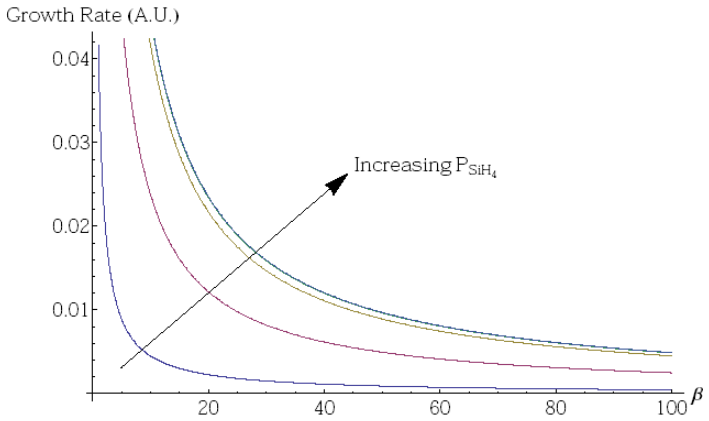


Figure 2.18 Plot of r_2 vs. β for several values of p_{SiH_4} ranging from 0.1 to 100. As β is decreased, the growth rate is enhanced dramatically. An order of magnitude difference in p_{SiH_4} can be negated by increasing β by a factor of 2 or less in the low p_{SiH_4} regime.

Lastly, we consider the connection between our experimental results and the β variable from equation 39. The growth conditions for the experiments were in a regime where the growth of amorphous and poly-Si is minimized while the growth rate of VLS Si is maximized. In order to do this, a temperature was chosen where the only silane decomposition that takes place is on Au surfaces. If reaction (17) can only occur on a Au surface, then an increase in the amount of exposed Au surface area should decrease β. In other words, as the average distance between Au islands is decreased, β should decrease as well. This is in good agreement with the experimental results of Figures 2.13 and 2.16 above.

The form of r_2 in equation 41 follows a reciprocal function with respect to β.

$$r_2 \propto \frac{x}{1+\frac{y\beta}{p_{SiH_4}}} = \frac{X}{1+Y} \qquad (42)$$

Using X and Y as fitting parameters (eqn. 42), we fit a curve to the data in Figure 13, yielding values of X and Y of -95 and -1.53, respectively. The Y value should be dependant on a number of factors including many of the reaction rate constants, thus its numerical value can not be calculated. However, the value of -95 nm/hr for X should simply describe the shape of the curve and not the horizontal shift. Next, an empirical value of Y was determined for our growth conditions and parameters from the e-beam thin film samples. For this determination, β is assumed to equal 1, p_{SiH_4} is 1.2 x 10^{-5}, and r_2 is approximately 500 nm/hr. Solving for Y in this case gives us a value of -1.428 x 10^{-5}.

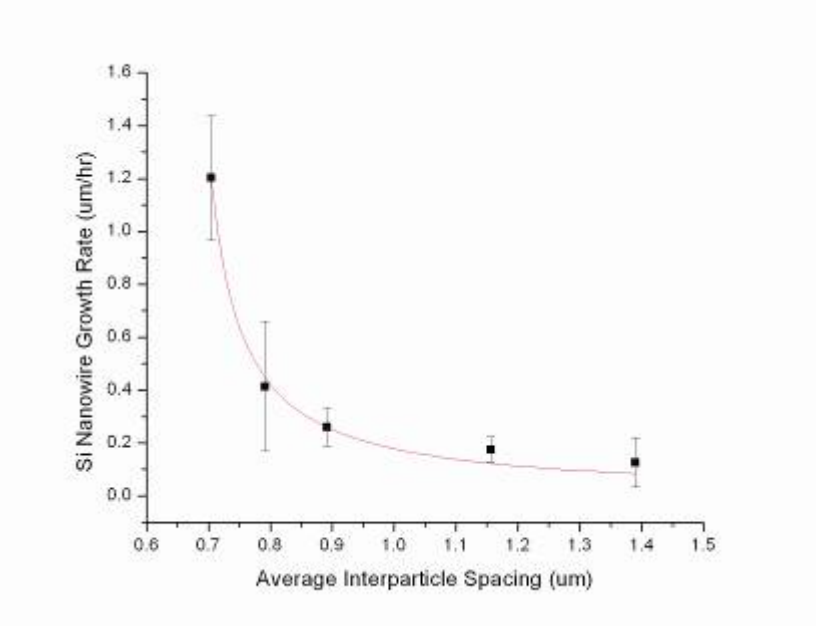


Figure 2.19 Data from Fig. 13 fit with a curve of the form given by equation 42. The value a = -0.095 um/hr is used to estimate values of β and $1/\beta$ (Figures 2.20 and 2.21).

Investigation of the model's fit to the data in Figure 2.16 reveals some spread of the growth rate for various catalysts materials and densities. This leads us to attempt to provide some explanation for the variance in our model. The first step comes by examining eqn. 42 and the dependence on P_{SiH4}. Precursor depletion across substrate surfaces is well known in CVD and MOCVD processes and many commercial CVD systems have engineered solutions to gas depletion in their reactor designs. Thus, it is very possible that some gas depletion is occurring across our sample surface since our reactor design does not account for this phenomenon. According to our model, small perturbations in P_{SiH4} are likely to have a significant impact on growth rate for a fixed value of β (which controls the shape of the curves in Figure 2.16). The other source of fit for the model comes from the reaction rate constants. Although these parameters are assumed to be constant, both the pyrolysis of silane and silylene are exothermic. Thus for a fixed reactor temperature, it is entirely possible that the surface of the catalyst is at a temperature higher than that of the bulk substrate. This would subsequently increase the reaction rate constants *exponentially* and thereby increase the nanowire growth rate with an apparent vertical shift of the plots in Figure 2.16. Considering the influence of both local temperature fluctuations and silane depletion across the substrate, the entire spread of the data in Figure 2.16 can be accounted for by a 30% decrease in P_{SiH4} and an increase in surface temperature of by as little as 20^{o}C if we assume the growth rate roughly follows the behavior of an activated process where E_a is 53.4 kcal/mole (the activation energy for silane pyrolosis [48]).

Furthermore, the model above allows us to extrapolate values of β for the curve in Figure 2.19 by using the p_{SiH_4} value of 6.66 x 10^{-4} and the X- and Y-values above. A table and plot of average inter-particle spacing, β, and $1/\beta$ is shown in Figures 2.20 and 2.21, respectively.

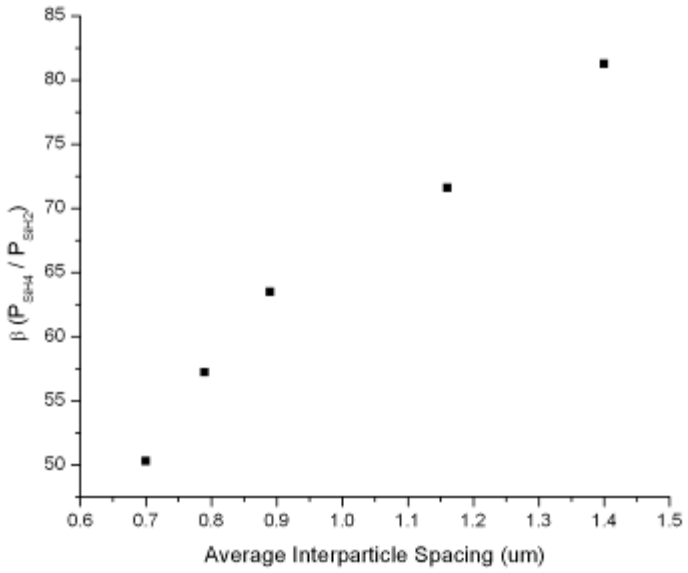


Figure 2.20 Plot of β vs. average interparticle spacing for the data in Fig. 19. As the average interparticle spacing increases, β also increases. Fig 18 indicates that regardless of p_{SiH_4}, β will dominate in determining the nanowire growth rate.

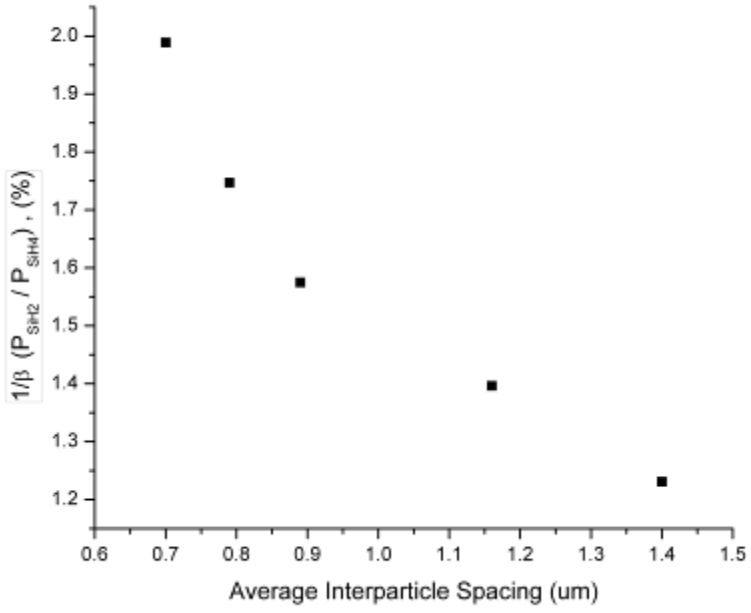


Figure 2.21 Plot of $1/\beta$ vs. average interparticle spacing taken from the data in Figure 2.19 and Figure 2.20. $1/\beta$ is the approximate percentage of SiH_4 which is converted to SiH_2 during steady state nanowire growth. According to this plot, only a very small fraction of incoming silane is being converted to silylene. This accounts for the suppressed growth rate of Si nanowires grown from a low density of Au-colloids, despite the relatively high p_{SiH_4} compared to Si nanowires grown with densely spaced colloids, as shown in Figure 2.9.

The approximate values of $1/\beta$ suggest that there is considerable room for enhancing the growth rate of silicon nanowires using a more reactive gas species, such as SiH_2 or Si_2H_6. This is consistent with the findings of reference [29], in which it is demonstrated that extremely high Si nanowire growth rates are obtained using a Si_2H_6 precursor. To further substantiate this idea, in our reactor we are able to produce growth rates that are more than 2 orders of magnitude faster for Au catalysts that are dispersed sparsely (i.e. inter-particle distance > 1 um) when an overhanging perforated gold mesh is

used. With an increased $1/\beta$ afforded by the proximity structure as shown in Figure 2.18, the growth rate can be controlled regardless of the inter-particle distance.

Furthermore, the strongly suppressed growth rates of Si nanowires from highly dilute Au-colloid solutions may impede the ability to create low density Si nanowires for discrete transistor or sensor applications. Many of the potential applications including single nanowire transistors and sensors may require relatively low nanowire densities for actual devices. The ability to grow the nanowire component in place using silane might involve either a process by which an excess of nanowires are grown simultaneously and then some are eliminated, or the addition of pre-cracking agent is used to convert SiH_4 to SiH_2 before reaching the metal catalyst particle for nanowire growth.

In summary, silicon nanowires have been grown using Au-catalyst particles and silane. The particles were deposited by using sub-continuous e-beam thin films or Au-colloid particles deposited from solution. The growth rate of silicon nanowires was found to be dependant on the inter-particle spacing of the Au-catalyst particles. A model for two-step silane decomposition into silylene and then silicon was used to explain the growth rate dependency on Au surface coverage.

3. III-V Nanowire Growth

3. III-V Nanowire Growth

Most of the work in the nanowire community to date has focused on Si nanowires because of their binary (metal/Si) components and relatively direct synthesis. While these studies have proven to be extremely insightful to the understanding of both basic growth mechanisms and design considerations for integration, the functionality of Si nanowires has proven to be somewhat limited. With silicon-microelectronics seamlessly transitioning into 'nanoelectronics' using conventional processing methods, the novelty of small Si transistors made using the VLS mechanism and long-standing questions about Au incorporation have kept them from entering mainstream production.

III-V materials such as InP and GaAs have well characterized physical and electrical properties. However, these materials have not seen nearly the amount of scaling in their device sizes as Si has over the past 40 years. Due to their inherently higher cost and the lack of stable dielectrics to enable CMOS logic, III-V devices are driven more by their high performance analog functions than by scaling. Because of this, any significant cost reduction to III-V devices which can be implemented without degradation to the device's performance are of tremendous interest to the semiconductor community. For example, the long elusive goal of many in the industry has been to realize III-V devices grown on low cost Si substrates. Despite the long-standing interest in bridging these two materials into one common platform, the technical barriers to doing so have prevented industrial fabrication of any devices.

III-V nanowires may indeed prove to be that critical bridge between high performance electronic devices and low cost Si substrates. As mentioned previously, predictions of tremendous strain accommodation with low defect densities and the ability

to grow these one-dimensional structures using vapor phase epitaxy has generated a great deal of interest among many of the key players in the III-V community. The approach taken in our case to realizing these structures began first by exploring growth of GaP and InP wires with little regard to the quality of epitaxy so much. This allowed us to find temperatures, flow rates and growth times for GaP and InP using Au and Ag catalyst particles. Secondly, once repeatable growth of GaP and InP nanowires was demonstrated, experiments were performed to elucidate the nature of III-V nanowire epitaxy on Si substrates. This problem has plagued the commercial semiconductor industry for decades, thus it is not surprising that we find our nanowires share common artifacts related to III-V/IV thin-film interfaces. Despite this, we demonstrate a reliable method for improving III-V nanowire epitaxy on Si <111> substrates.

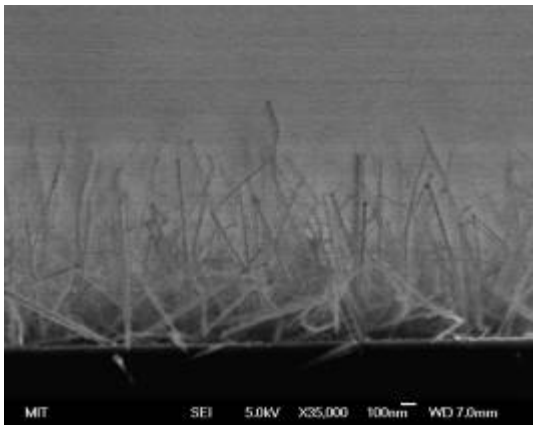
3.1 Gallium phosphide nanowire growth

Gallium phosphide (GaP) nanowire growth was initially developed based on considerations from previous Si nanowire growths, GaP thin film growth and various sources in the literature. The input parameters for III-V wires in our system include growth temperature, precursor flow rates, V/III (group V precursor to group III precursor) ratio, time and any combination of these. Samples were inspected after growth using plan-view and tilted SEM.

3.1.1 Temperature

The optimal temperature window for VLS growth will be where wires grow without any lateral overgrowth or uncatalyzed growth away from the metal particle. Initial growths at 500°C, 520°C and 540°C exposed a window between tapered nanowire growth (characteristic of completely lateral overgrowth) and large twinning defects along the wire's growth axis. At growth temperatures of 540°C we observed tapering along the length of the wires, with the top of the wires appearing to have a slightly smaller diameter than the base of the wires [Figure 3.1c]. At the GaP growth temperature of 500°C we observed faceting of the nanowires along their growth axis [Figure 3.1a]. At growth temperatures of about 520°C GaP wires did not appear to exhibit either tapering or faceting along their length [Figure 3.1b]. Though the facets may be too short in this case to readily been seen in SEM, the absence of non-catalyzed growth solidified the GaP growth temperature.

a) 

b) 

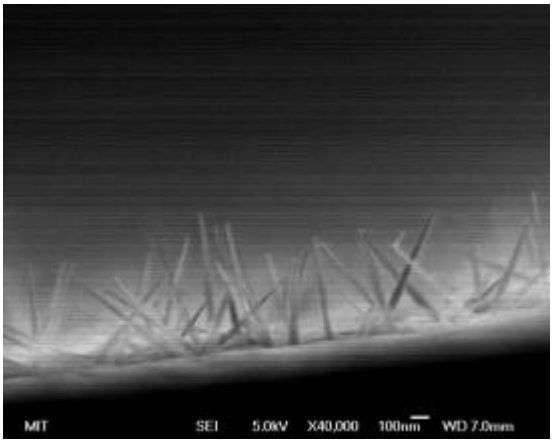
c) 

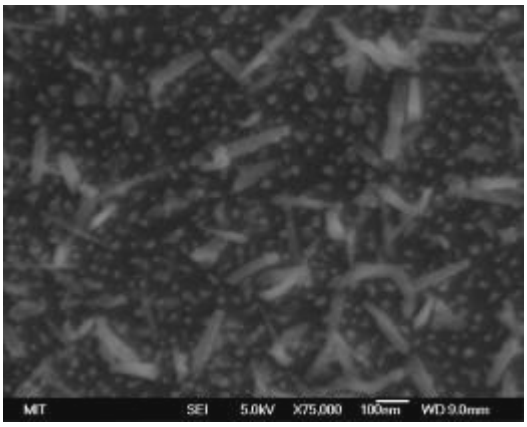
Figure 3.1 Cross-sectional SEM images of GaP nanowires grown on Si (111) substrates at 500°C, 520°C and 540°C, are seen in a), b) and c), respectively. Note the distinct faceting along the GaP wire seen in a). The wires in b) appear to be uniform along their length. The wires in c) have larger diameters toward their bases than compared to their tips.

3.1.2 Precursor flow rates

After the growth temperature was selected, efforts were made to optimize the precursor flow rates for GaP nanowire growth. In this case, both PH_3 and TMGa can be varied independently to affect nanowire growth. In traditional MOCVD for thin-films, the group-V precursor is kept at a substantially higher flow rate than the group-III precursor(s). Often with III-V materials, the group-V species has a high vapor pressure, such that when exposed to high temperature, the group-V atoms will leave the surface of the film and enter the vapor phase. The excessive group-V precursor overpressure ensures the surface does not readily decompose at higher temperatures. In addition, group-III metals tend to form droplets when they decompose in the absence of a group-V atom. By maintaining this high V/III ratio, the group III species limits the film's growth rate and ensures epitaxy. In the case of nanowire growth, we need eliminate uncatalyzed

homoepitaxy on the wire sidewalls while maintaining adequate VLS growth via the catalyst particle.

To understand the effect of V/III ratio on nanowire morphology and epitaxy, two nanowire growths were carried out under identical conditions except the V/III ratio was varied between ~870 and ~87. As revealed by SEM [Figure 3.2a and 3.2b], the wires grown with a V/III ratio ~10^3 exhibit tapering along their lengths, while the wires grown with a V/III ratio ~10^2 appear to be cylindrical with no signs of tapering along their lengths.

a) 

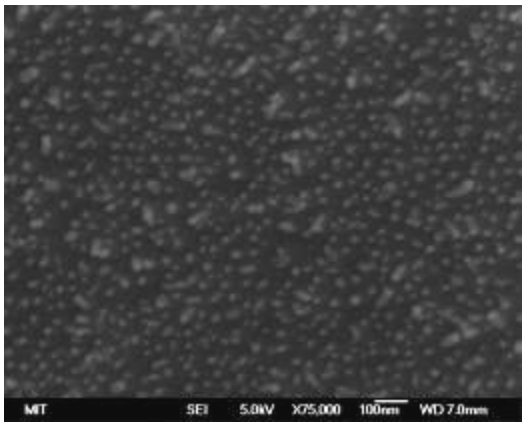
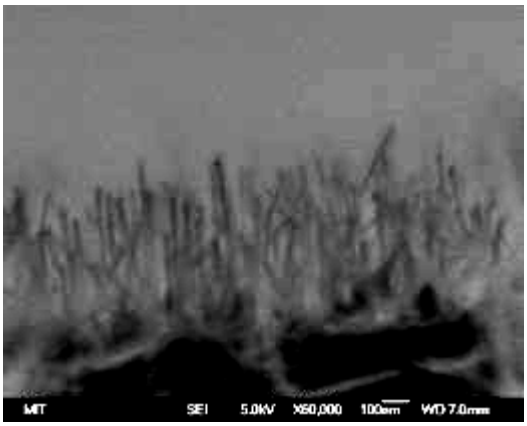
b) 

Figure 3.2 Top-down SEM images of GaP nanowires grown at 520°C with V/III ratios of ~870 and ~87 are seen in a) and b), respectively. Note that the wires in a) appear to have some tapering along their length, indicating simultaneous lateral overgrowth. The wires in b) are short but appear to be radially uniform along their length.

Flow rates of both cursors were then decreased in an attempt to increase the number of wires growing vertically from the substrate as was observed to be the case for Si nanowires. For the following experiment, the flow rate of TMGa was lowered to 0.09 sccm with a V/III ratio of 153 from 0.158 sccm using previously. There are nearly the lowest flow rates possible in the reactor while maintaining any kind of repeatability with the mass-flow controllers (MFCs). Following growth, the sample was inspected by plan

view SEM and nearly 40 vertical GaP wires per um^2 were observed [Figure 3.3a and 3.3b] which was seen as a dramatic improvement over previous growths which might have been lucky to have one or two per um^2.

a) 

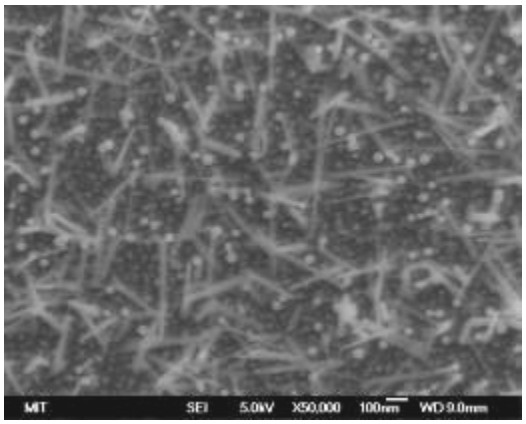
b) 

Figure 3.3 Cross-sectional (a) and top-down (b) SEM images of GaP nanowires grown with TMGa set to 0.90 sccm and a V/III ratio of ~150. The number of wires growing vertically from the substrate is clearly seen in both a) and b).

3.2 InP nanowire growth

Indium phosphide nanowires were initially grown based on the conditions established above for GaP nanowires. Minor modifications to the growth temperature and flow rates were expected, as discussed below. However, given that in the ultimate goal of $GaP_{(w)}/InP_{(w)}/GaP_{(w)}$ heterostructures we are primarily concerned with short (<100nm) InP wire segments which might serve as the active region in a nanowire device, demonstration of InP grown by the VLS mechanism was of primary importance here with secondary considerations given to ideal, non-tapered epitaxial InP nanowire growth on Si substrates.

3.2.1 Temperature

It is common knowledge among the III-V MOCVD community that trimethylindium decomposes at lower temperatures than trimethylgallium, so it was presumed that growth temperatures for InP nanowires would be lower than for those of GaP as is the case in thin-film growth. However, growth was initially explored at 450°C such that little or no temperature might be required when switching between materials for heterostructure formation. Refinement of InP nanowire growth temperature for GaP/InP heterostructures is explored in Chapter 4.

3.2.2 Precursor Flow Rates

Changes to the TMIn flow rates were necessary as the MOCVD plumbing for the TMGa and TMIn lines is not identical. In this case, the TMIn line is not equipped for H_2 dilution so the lowest flow setting we can achieve (and hence, slowest growth rate possible) is dictated by a combination of mass-flow controller (MFC) size and the recirculator bath temperature of the TMIn bubbler. The MFC for TMIn on our MOCVD is 500 sccm. This in turn limits our lowest controllable flow setting to about 25 – 50 sccm, 5 – 10% of the maximum flow rate, below which MFCs cannot be accurately controlled. The other knob with which to control InP nanowire growth rate is by controlling the TMIn bubbler bath recirculator. Previously, the TMIn bath temperature was set to 25.1°C as this was found by previous students to give an adequate growth rate for InP thin-films. However, our previous work on GaP nanowire growth revealed growth rates which were nominally 15 times faster than thin film growth rates for the same precursor flow settings. The TMIn bath temperature was cooled to 20.0°C to account for

this growth enhancement. This step reduced the TMIn vapor pressure from 2.596 torr to 1.732 torr according to equation 3.1 [49] below. Consequently, the amount of TMIn mixed with H_2 going into the reactor was reduced from 0.086 sccm to 0.057 sccm.

$$\text{Log } P \text{ (Torr)} = 10.52 - 3014/T \text{ (K)} \quad (3.1)$$

In accordance with GaP nanowires mentioned above, a V/III ratio was kept as low as possible in order to minimize lateral overgrowth. Given the inability to reduce the TMIn flow rate below .057 sccm and the inability to reduce the PH_3 flow rate below 8.3 sccm, the V/III ratio was fixed at 144 for InP nanowire growth.

3.2.3 InP nanowire quality

As seen in Figure 3.4, growth at 450°C with the V/III ratio and TMIn flow rates mentioned in sections 3.2.1 and 3.2.2 turned out to be surprisingly good with little to no tapering seen along the length of the wire and virtually no thin-film InP growth present on the surface of the silicon substrate. Tilted and cross-sectional SEMs in Figure 3.4b and 3.4c clearly show some wires growing in the inclined <111> directions relative to the substrate. However, enough wires growing epitaxially gave us reason to proceed with further development of nanowire heterostructures. Work in 3.3 explores this topic of III-V nanowire epitaxy on Si substrates in further detail.

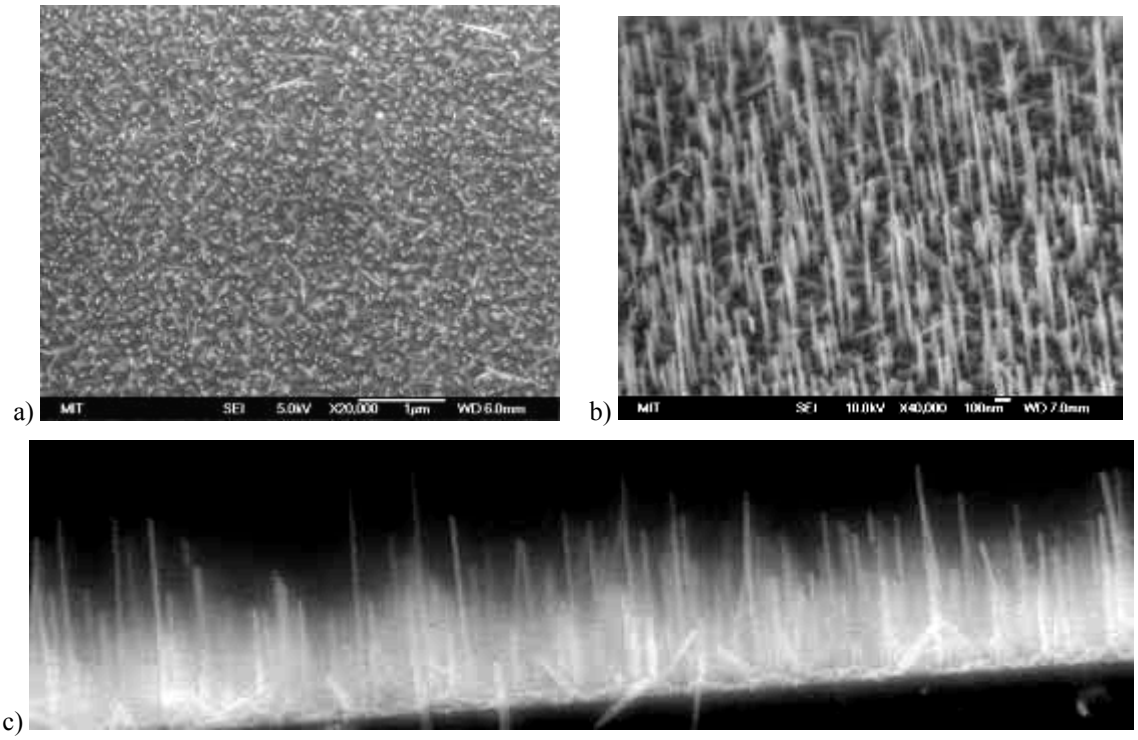


Figure 3.4 InP nanowire growth on Si (111) subtrates. Images in a), b) and c) were taken by top-down, 45 deg tilt, and cross-sectional SEM, respectively.

3.3 III-V nanowire epitaxy on Si substrates (adapted from [50])

Very little is known about the nature of VLS epitaxy involving III-V materials. However, III-V thin-film integration on Si and Ge has been studied extensively over the past 30 years and several important factors including polarity, anti-phase boundaries and lattice mismatch have all been found to play a critical role in material compatibility. As a result, many techniques have been developed to mitigate defects associated with the heterointerface. Surprisingly, little connection has been made between VLS growth and traditional thin film growth. Here, we find that nanowire growth initiation conditions are critical to controlling both the yield and relative orientation of InP nanowires. This is consistent with the techniques which have been found to influence the quality of III-V thin film epitaxy on Si and Ge, as well as Tomioka, et al.[51], who were able to control

the growth directions of catalyst-free InAs nanowires grown by selective area epitaxy (SAE) on Si substrates.

3.3.1 Experiment, Results and Discussion

Lightly-doped Si (111) wafers (<0.01 ohm-cm, As) were dipped in 50:1 H_2O:HF until the surface became visibly hydrophobic (~15 sec.) to remove the native Si oxide. The samples were then immediately loaded into a Perkin-Elmer e-beam evaporation system without water rinsing to ensure a hydrogen terminated surface for metal film deposition. A 0.6 nm-thick Au layer or a 1.0 nm-thick Ag layer were deposited at approximately 0.1 nm/min at room temperature.

Immediately before nanowire growth, the samples were etched in 1:1 H_2O:HF for two minutes to ensure removal of a silicon-oxide shell which covers the metal catalyst islands [36]. The formation of this shell is the result of Si diffusion through the metal particle, where it is oxidized in ambient air at room temperature [52]. The samples were then loaded into a Thomas Swan atmospheric pressure MOCVD reactor and purged with N_2 to prevent reoxidation.

Growth of the nanowires was then carried out using 15 lpm of H_2 as the carrier gas and Trimethylindium (TMIn) and Phosphine (PH_3) as the gas-phase precursors with a V/III ratio of ~100. A two step growth procedure was adopted as it was found to increase yield of Au catalyzed nanowire growth and epitaxy. The reactor was first brought to 700°C in carrier gas and held there for approximately two minutes before the system was cooled to 460°C for VLS growth. These growth temperatures and flow rates of TMIn and PH_3 were previously optimized such that precursor decomposition selective to the Au-

catalyst was maximized and nanowires grew in a stable and repeatable manner. Following growth, the samples were cooled to 350°C in PH_3 to prevent InP decomposition due to P desorption.

Introduction of the gas precursors was altered according to the design of experiment, schematically shown in Figure 3.5. For the first run, sample A, H_2 was introduced before the reactor was ramped up to the annealing temperature. After the anneal, PH_3 and TMIn were introduced simultaneously once the reactor temperature stabilized at 460°C. Sample B was exposed to H_2 at room temperature and then a mix of PH_3 and H_2 was introduced at 350°C. The sample was then annealed and brought down to 460°C when TMIn was introduced for wire growth. Finally, sample C was annealed in H_2 followed by a 90 s introduction of TMIn with H_2 at 460°C. PH_3 was then introduced to initiate wire growth. These different conditions were found to significantly affect wire growth.

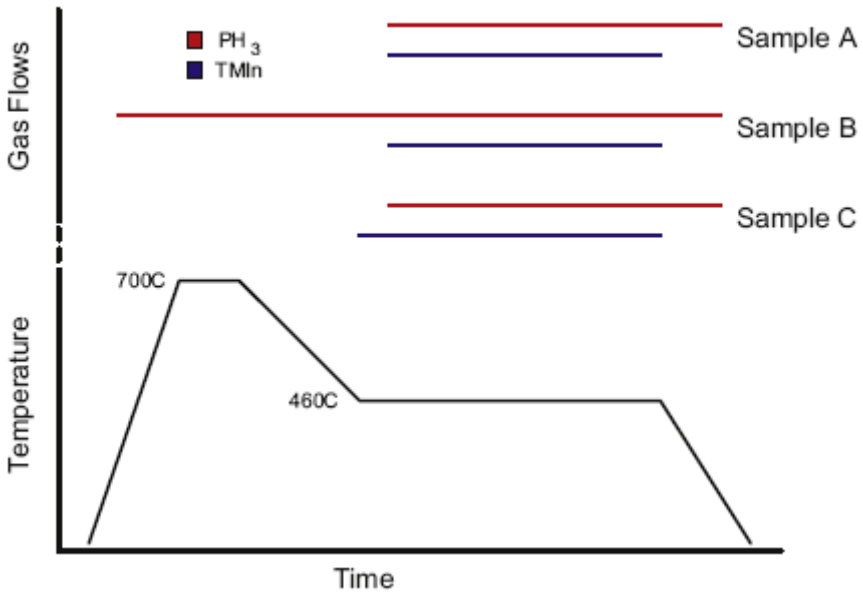


Figure 3.5 Temperature profile and gas introduction timing.

Following growth, samples were inspected using a scanning electron microscope (SEM). Images were taken from center area of the samples and are shown in Figure 3.6. A tilted SEM image of sample C is shown in Figure 3.6d, which correlates with the bright spots in top-down SEM images and vertical nanowires in Figure 3.6c. The bright spots can be used to determine the area density for vertical wire growth. The presence of 60° and 120° angles in Figure 3.6a is attributed to epitaxial growth in <111> directions inclined with respect to the substrate surface.

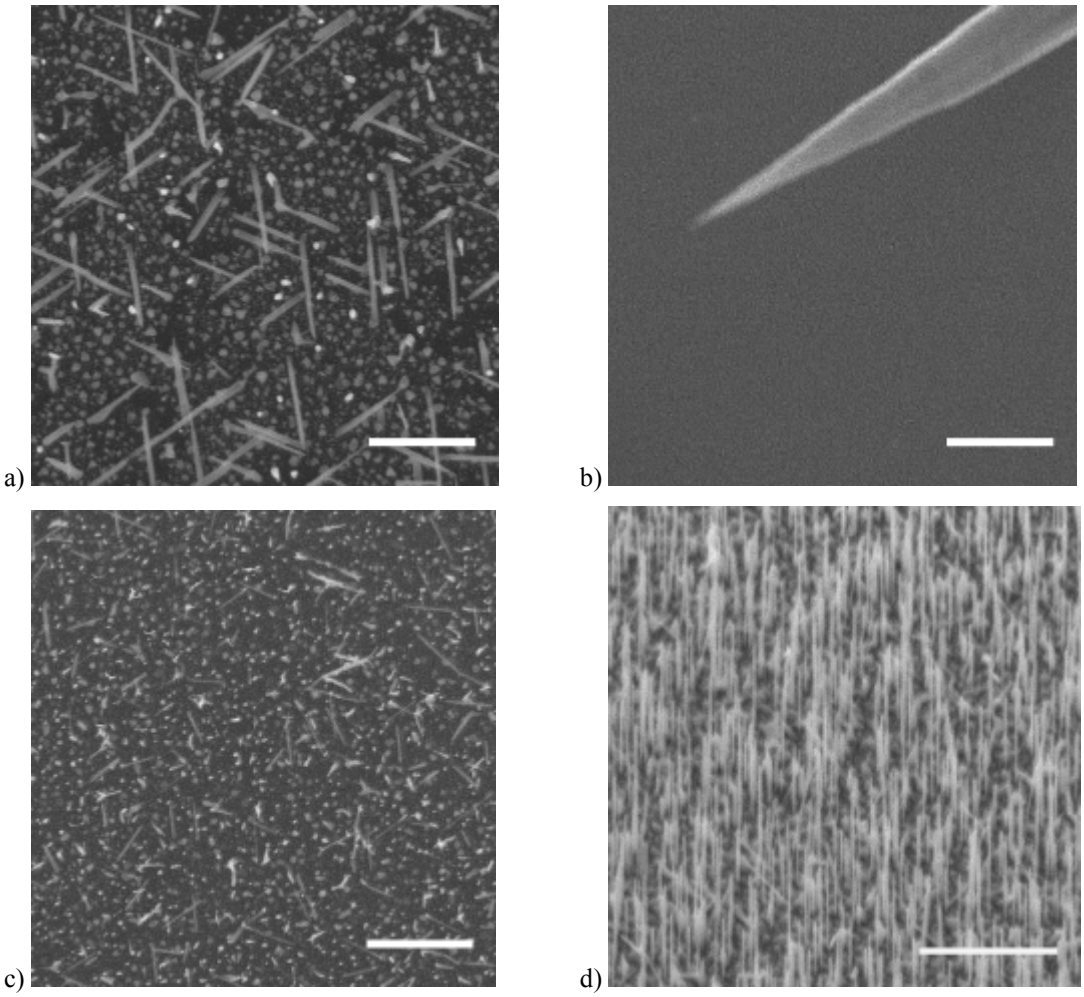


Figure 3.6 SEM images from each sample: a) is from Sample A where the precursors were introduced simultaneously; b) is taken from the P-rich Sample B. A large crystallite of InP can be seen at the top of the image. However, all the catalyst particles underneath appear to have no wire growth; c) is from the In-rich

sample C. A 45-deg tilt SEM of Sample C is seen in d) shows that the bright spots in 3.6c correspond to vertical nanowires. Scale bars are 1um.

From the SEM images, the influence of each precursor was clear. Sample B, which was annealed in PH_3, has a significantly lower yield of wires. Sample A, which was annealed in H_2 before the precursors were simultaneously introduced, appears to have an intermediate yield of vertical wires with a significant fraction growing in the inclined <111> directions. Sample C, which was exposed to TMIn before growth, has a relatively high density of vertical InP nanowires whose diameters are on the order of those of the Au catalyst particles.

The wires in sample A exhibit some tapering in contrast to the columnar wires seen in sample C. Tapering in nanowires is known to be caused by a competition between catalyst-mediated VLS growth and lateral overgrowth. Higher growth temperatures have been shown to lead to more radial overgrowth and tapering [35]. However, the tapering seen here is better explained by an increase in the precursor partial pressures which is consistent with results from InAs VLS nanowire growth [53]. A lower wire density in sample A consumes less precursor than the wire density in sample C and is likely leading to an effectively higher local concentration of precursor available for lateral overgrowth.

To further characterize this effect of precursor exposure, X-ray texture analysis was performed on each sample. Pole figures were produced for each sample with the 2-theta collection angle set to first detect Si {111} planes and subsequently detect InP {111} planes. Figure 3.7 shows the pole figures along the <111> axis.

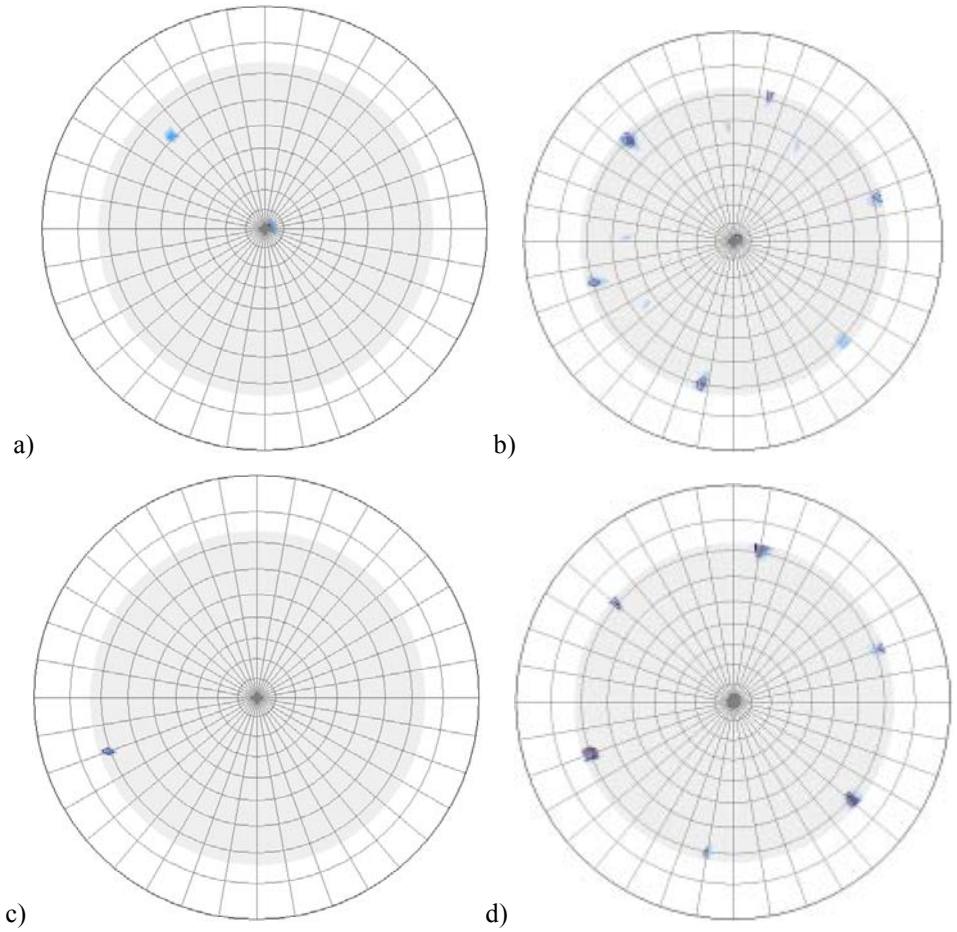


Figure 3.7 X-Ray pole figures showing texture of the Si substrates and InP wires: a) and c) show the strongest (111) peak of the underlying Si substrates for reference, b) shows InP (111) texture when the precursors are co-introduced, d) shows the stronger InP (111) texture when TMIn is introduced before PH_3.

The InP (111) pole figure for sample A, which was annealed in H_2 before growth, is shown in Figure 3.7b. Not only do the wires from this sample grow in inclined <111> directions of the substrate, but a 180^o twinning defect at the wire/substrate interface appears to be prevalent as well. This is evidenced by the nearly equal intensities of all 7 (111) reflections (1 normal (111), 3 (111) out of plane, and 3 mirrored out of plane (111)). Interesting to note on this sample are the indications of InP wires growing along their [111] direction, but on {110} and {112} planes of the substrate. While some groups have shown a directional preference for small diameter Si nanowires [54], there does not

seem to be a diameter variation in these wires which would explain the alternate growth directions.

Sample B, which was annealed in PH_3 and showed relatively little growth in the SEM images, did not give a sufficiently strong InP <111> signal to determine its texture relative to the substrate.

Sample C clearly had the highest yield of wire growth of the three samples and also showed the strongest (111) texture in x-ray analysis. While all 7 (111) reflections are present in this pole figure, the overwhelmingly predominate x-ray reflected intensities correspond to the normal [111] direction and 3 out of plane <111> directions of the substrate (Figure 3.7c).

Using sample C, energy dispersive x-ray (EDX) analyses were carried out in the SEM and were compared with images taken in the same area from the outer edge of the sample to the center. In each image the number of bright spots, corresponding to vertical nanowires, were counted per unit area to give a measure of the vertical growth density. This figure was then compared to the relative amount of In in the scan, which was approximated by dividing the In counts by the Si counts, as the Si counts should be roughly the same in each scan. Figure 3.8 shows a plot of vertical wire density with the corresponding In fraction. Scans were taken linearly from the front edge of the sample to the center and were marked as locations 1 to 5. This data clearly shows In depletion toward the center of the sample. The rough correlation of vertical wire density to the presence of In supports the data from X-ray analysis that indicates that In improves wire growth. This analysis was also repeated with P, but the EDX signal from P was too weak to be observed for each location.

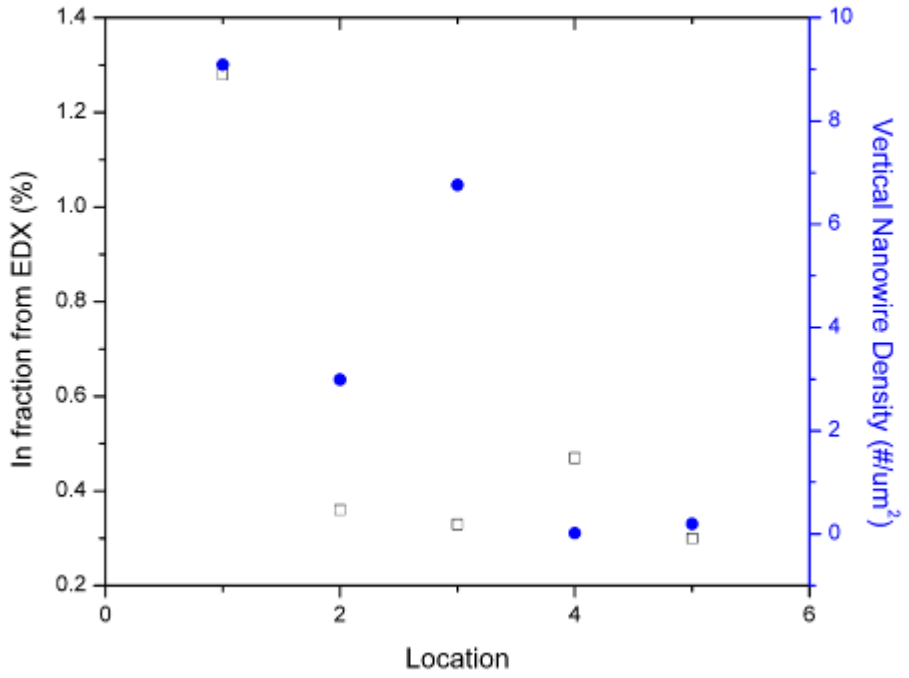


Figure 3.8 Plot comparing In/Si fraction (open squares) from EDX to the number of vertical nanowires (closed circles) in each image, for positions linearly spaced from the samples leading edge.

Cross sectional transmission electron microscopy (XTEM) samples were prepared to investigate the catalyst microstructure. First, the sample surfaces were coated with epoxy. They were then mechanically thinned and Ar-ion milled. The contrast seen in Figure 3.9 between catalyst particles from sample A and sample B is striking. For sample A (Figure 3.9a), the catalysts have alloyed to a significant depth into the underlying substrate. XTEM images from sample B (Figure 3.9b), which was annealed in PH_3 initially, shows that the Au catalysts in this case have not alloyed as deep into the substrate as the samples annealed in H_2 alone.

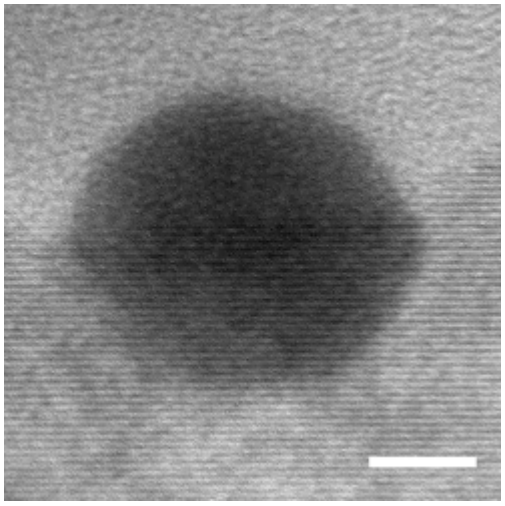
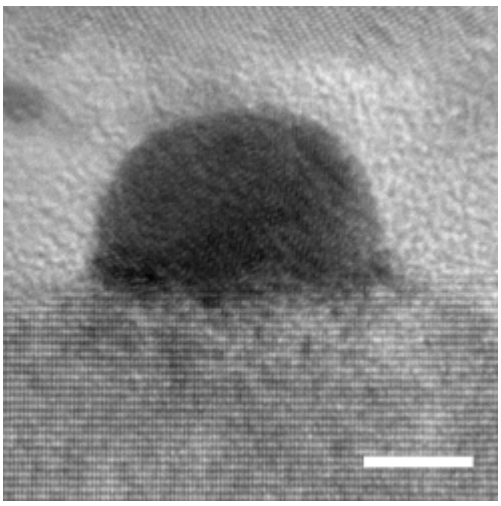
a)  b) 

Figure 3.9 XTEM of catalyst particles. Typical catalyst particles from samples A and B are shown in 3.9a and 3.9b, respectively. Scale bars are 5nm.

The catalyst particles seen in XTEM have two characteristic differences which may inhibit wire growth. First, the sample from Figure 3.9b had a significant amount of PH_3 exposure which presumably leads to phosphorous adsorption on the surface of the substrate and of the catalyst. Second, the lack of alloying seen in Figure 3.9b could prevent wire nucleation on the substrate thus inhibiting wire growth.

To investigate the possibility of phosphorous adsorbing on the exposed Si, two pieces of <111> Si with 0.6nm of Au, were etched in 1:1 HF:H_2O and one piece was exposed to the anneal/growth temperature profile with only H_2 flowing while the other sample was exposed to the same temperature history with a mixture of PH_3 and H_2 flowing. SEM images of the two samples are shown in Figure 3.10. The distribution of particle size is quite different after gas exposure. The H_2 exposed sample has Au islands alloyed with the substrate that have begun to coalesce while the temperature was held at 460 C for 10 min. In contrast, the PH_3 annealed sample shows no sign of coalescence or alloying. The difference might be attributed to the inhibited surface mobility of Au on Si

caused by P atoms adsorbing on exposed Si sites, either on the substrate or on the catalyst. This leaves the as-deposited Au microstructure essentially preserved. Gas purity is also a consideration as any contaminates in the precursors or upstream of the sample may be causing reoxidation either at the catalyst surface or catalyst/substrate interface. However, we have not seen any indications of this when growing III-phosphide materials in our reactor.

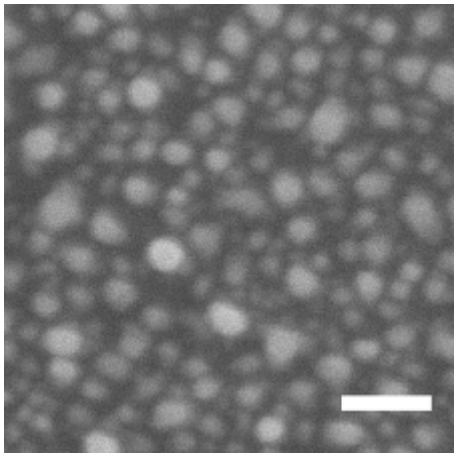
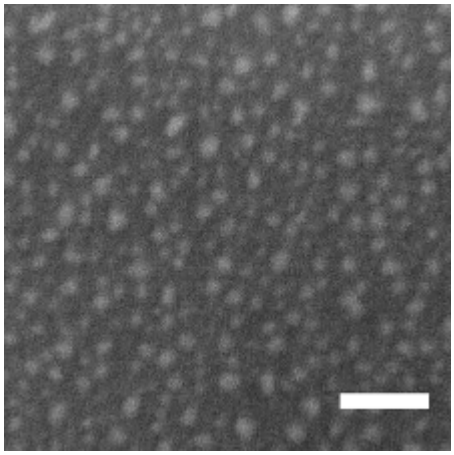
a)  b) 

Figure 3.10 SEM images of two samples of Au on Si. Figure 3.10a shows the sample which was exposed to the temperature profile in Figure 1 with only H_2 flowing. Figure 3.10b was exposed to a mix of PH_3 and H_2 during this same process. Scale bars are 20nm.

To investigate the lack of alloying without the early introduction of PH_3, a 1 nm film of Ag was deposited on a hydrogen terminated <111> Si wafer for catalyst-mediated InP growth. The Ag-Si phase diagram [5] indicates that Ag should not alloy with the substrate at any time during annealing or growth because the temperature never exceeds the Ag-Si eutectic at 835 C. The same recipe used for the growth of sample C was used for growth on the Ag film, except the growth time was reduced to 3.5 minutes. SEM images from this growth can be seen in Figure 3.11a. Initially the images suggest a relatively low yield, but XTEM images in Figure 3.11b indicate nearly 100% of the

catalyst particles lead to catalyst-mediated growth. X-ray analysis also indicates wire growth in the 4 <111> directions of the substrate as well as 3 mirrored <111> directions, although there is significant noise in the data which inhibits detection of other directions.

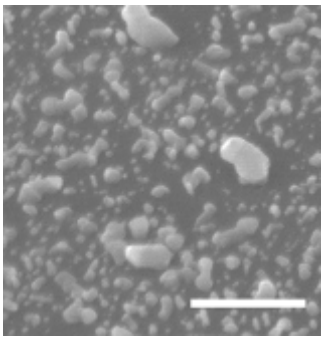
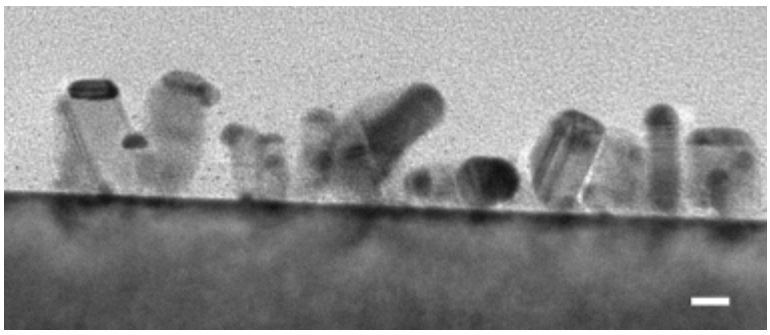
a)  b) 

Figure 3.11 InP nanowires and nanoparticles grown using a Ag catalyst on a Si substrate. Figure 3.11a is an SEM micrograph taken at 45 degrees and the scale bar is 500nm. Figure 3.11b is an XTEM image from the same sample. The scale bar here is 20nm.

The results described above for Ag indicate that alloying alone is not responsible for the low yield and poor growth of wires in the case of sample C. This then supports an argument that it is phosphine which is responsible for the low yield of Au catalyzed InP nanowires.

The observation of group V elements interfering with III-V *thin film* growth on Si or Ge has been well documented [55]. Among the many techniques used to control this problem in heteroepitaxy are use of offcut wafers, use of high growth temperatures and use of high V/III ratios [56], but perhaps the most relevant technique is the use of group III pre-layers [57]. The use of these pre-layers has been found to dramatically enhance the quality of epitaxy for GaP on Si grown by MBE [58, 59].

While the exact mechanism for the epitaxy improvement is unclear, there are several key factors which likely contribute to the beneficial role of initiating growth with group III atoms. First, as demonstrated by [6], wires growing in the <111>B direction

will need an In-terminated Si surface to grow vertically from the substrate. Second, P atoms are known to lock into Si surface sites when growing GaP films directly on Si [60] and during Si homoepitaxy, leading to dramatically reduced growth rates [61]. In addition, the Au-P system is completely immiscible below 935°C [5]. Therefore, any PH_3 decomposition at a Au surface should expel P atoms away from Au to a free Si surface.

Next we consider the mechanism by which wire growth is physically inhibited. In theory, the presence of Si-P bonding should not prevent InP growth. However, as P atoms migrate to the Au/Si interface and adsorb at the Si interface, it seems likely that a significant fraction of the Si atoms in the Au/Si droplet will no longer be able to re-adsorb epitaxially on the substrate surface. At this point, it remains unclear whether Si at the surface of the Au/Si droplet or at the droplet/substrate interface is forming a barrier by reacting with PH_3. In addition, the InP nanowires which were catalyzed with Ag particles have a much higher density of catalyst-mediated InP growth. This may be attributed to the lack of alloying between Ag and Si leaving very little excess Si to interfere with potential VLS growth. Regardless of which mechanism is physically responsible for this phenomenology, it is clear from the experimental results that direct interaction of PH_3 with Si is detrimental to VLS growth of InP nanowires on Si substrates and by initiating wire growth with excess indium, epitaxial wire growth can be improved.

3.3.2 Conclusions

In conclusion, we have studied the effect of pretreatments with PH_3 and TMIn on Au-catalyzed InP nanowire growth on Si substrates. SEM, TEM and X-ray analysis indicate that flow of PH_3 before introduction of TMIn results in virtually no wire growth,

with very little catalyst agglomeration and Au/Si alloying. Co-introduction of TMIn and PH_3 gives clear signs of nanowire epitaxy, although these wires contain a significant number of defects at the substrate/wire interface. The wires grown with a short 90 sec. burst of TMIn before PH_3 introduction showed the best epitaxy on Si substrates. X-ray results indicate far fewer 180^o rotational defects at the substrate/wire interface as the majority of growth appears to be either normal to the substrate or in one of the other inclined <111> directions of the substrate. The evidence from these growth conditions suggests PH_3 and subsequently P, may be adsorbing to Si and preventing wire growth. However, it is unclear at this point whether the early introduction of indium is actually improving wire growth, or simply preventing PH_3 from impeding wire growth.

4. III-V nanowire heterostructures

4. III-V nanowire heterostructures (adapted from [62])

4.1 Introduction

The unique electrical [4, 63], optical [31, 64, 65] and electro-optical properties [32] of semiconductor nanostructures have become of great interest to the semiconductor community over the last decade. Some of these properties may give rise to devices which either improve on existing technologies or open the door to new devices due to their previously unattainable band-gaps [66] and/or lattice constants.

In this letter we present a demonstration of gallium phosphide-indium phosphide-gallium phosphide ($GaP_{(w)}/InP_{(w)}/GaP_{(w)}$) nanowire heterostructures grown by the vapor-liquid-solid (VLS) mechanism. The thin-film equivalent of this heterostructure is nearly impossible to growth with any reasonably low dislocation density due to the large (~7%) lattice mismatch between GaP and InP. Nanowires on the other hand, are surrounded by free surfaces which theoretically [3, 24] provide for quick strain relaxation along growth direction preventing misfit or threading dislocations from forming in the material. In addition, the low growth temperatures used with the VLS mechanism may impose a kinetic barrier to dislocation nucleation which again might eliminate these non-radiative recombination centers in an opto-electronic device. Given the potential for small geometries of GaP/InP interfaces with low defect densities, GaP/InP/GaP nanowires grown by VLS are an attractive route to realizing high performance III-V devices on Si substrates.

4.2 Experimental Details and Results

GaP/InP/GaP nanowire heterostructures on Si substrates were fabricated using gold (Au) catalyst particles and the vapor-liquid-solid (VLS) mechanism. Epi-ready Si <111> wafers were dipped in a H_2O: HF, 50:1 (by volume) mixture for 15 s and immediately loaded into a Perkin-Elmer e-beam evaporator without rinsing. The evaporator was then pumped down to a base pressure of 10^{-9} torr for Au deposition. Approximately 0.6 nm of Au were deposited at 0.1 nm per minute at room temperature. Following Au deposition, the samples were again dipped in 50:1 H_2O:HF for 15 s and loaded into a Thomas Swan atmospheric-pressure metallorganic chemical vapor deposition system (AP-MOCVD) where they were purged with purified N_2 to prevent any oxidation of Si on the Au catalyst [36] before growth.

Nanowire growth was initiated in 15,000 standard cubic centimeters per minute (sccm) of hydrogen (H_2) gas. The samples were heated to 700°C and held there for 2 m to ensure sufficient alloying between the catalyst and the substrate. The temperature was then lowered to 450°C for nanowire growth. Following temperature stabilization, trimethylgallium (TMGa) was introduced alone at a rate of 0.02 sccm for 90 s to increase vertical epitaxy of GaP wires on Si <111> substrates [50]. Phosphine (PH_3) was flown at a rate of 8.23 sccm to commence nanowire growth for a varying amount of time depending on the desired length of the first GaP nanowire segment. The GaP VLS growth rate was previously found to be approximately 100 nm per minute for these growth conditions (Chapter 3). Trimethylindium was used to synthesis the InP nanowire segments and was flown at a rate of 0.07 sccm in all cases discussed below. Growth of InP was performed with the same PH_3 flow-rate as used for GaP. Nanowire growths were

terminated by turning off the group III precursor. However, PH_3 continued to flow in the reactor until the reactor had cooled to 350°C to prevent surface decomposition of the wire surface. After growth, bright field transmission electron microscopy (BF-TEM), energy-dispersive x-ray spectroscopy (EDX) and high angle annular dark field scanning transmission electron microscope (HAADF STEM) were used to confirm the InP/GaP heterostructures.

4.2.1 Single nanowire heterostructures

Some preliminary work involving the growth of InP nanowires on GaP <111> substrates using a Au catalyst revealed 2-D thin-film Frank-Van der Merwe (FM) type growth in addition to VLS growth when InP was deposited at 450°C. An example of this is seen in the cross-sectional TEM (XTEM) image in Figure 4.1.

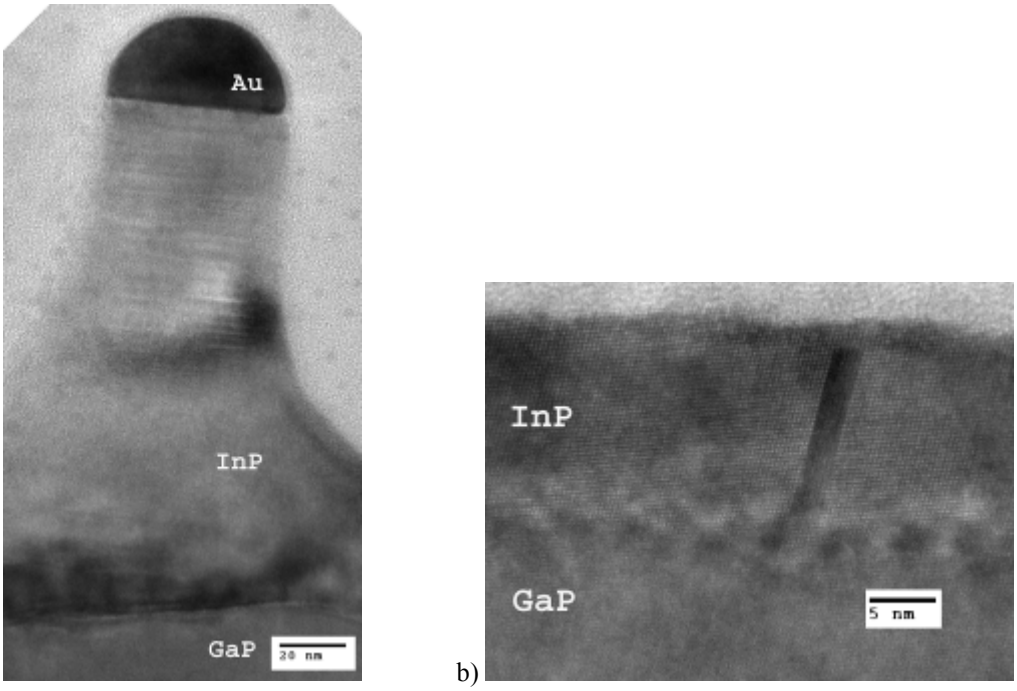
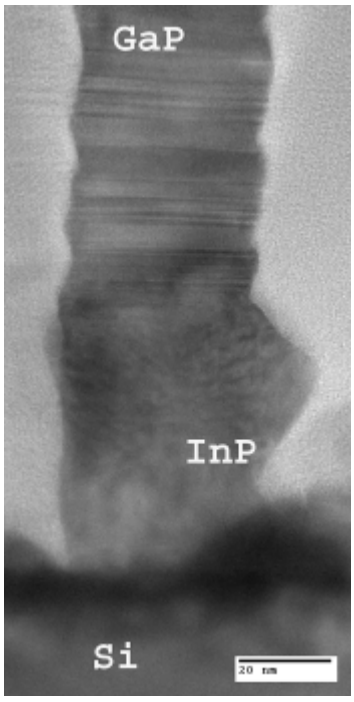


Figure 4.1 The XTEM in a) above shows Au-catalyzed InP VLS growth on a GaP <111> substrate which was grown at 450°C. The XTEM in b) is a thin film was of InP that was also grown on the GaP substrate indicating that both 1-D and 2-D growth is occurring at simultaneously.

Following these findings, a series of InP nanowire growths at successively lower temperatures (430°C, 410°C and 390°C) was conducted to optimize selective InP VLS growth on existing GaP nanowires. Growth of InP on GaP nanowires on Si <111> substrates at 430°C revealed selective TMIn decomposition to the Au catalyst particle. However, the features at the base of the GaP wires indicate that nearly all the indium is migrating to the trunk of the wire but not onto the Si substrate surface [Figure 4.2]. It is unclear whether this is the result of a concentration gradient of mobile indium along the length of the wire or it is due to preferential nucleation site towards the Si/GaP interface. Regardless, there is clearly no sign of InP growth underneath the catalyst particle.

a) 

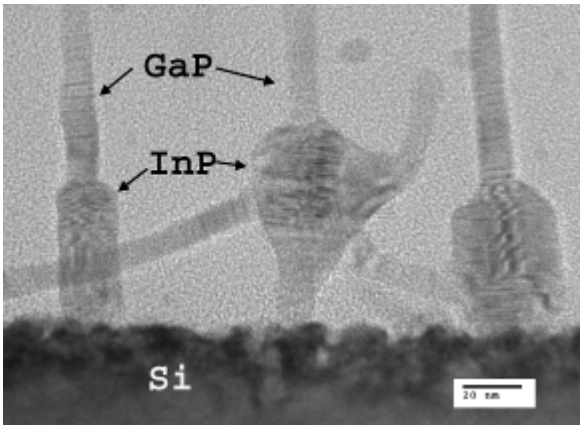
b) 

Figure 4.2 InP growing selectively at the base of GaP nanowires on Si substrates at 430°C can be seen in XTEM images in both a) and b). The GaP cores in these cases are relatively free of sidewell deposition except near the wire/substrate interface where InP has formed an radial heterostructure around the base of the wires.

Lowering the growth temperature another 20°C to 410°C produced definitive axial nanowire heterostructures in addition to small signs of lateral overgrowth [Figure 4.3]. In this case, In adatoms appear to be kinetically inhibited from migrating along the full length of the GaP nanowire core leaving patches of InP present on the outer shell of the GaP wire. Despite the small amount of 2-D growth on the shell of the GaP wire, a clear contrast is seen along the last 20nm of the wire [Figure 4.4]. Although we are unable to speculate on the sharpness of the interface due to drift in the STEM and interactions with the epoxy (in which the wire is embedded), changes in composition from GaP to InP and InP to Au are unmistakable.

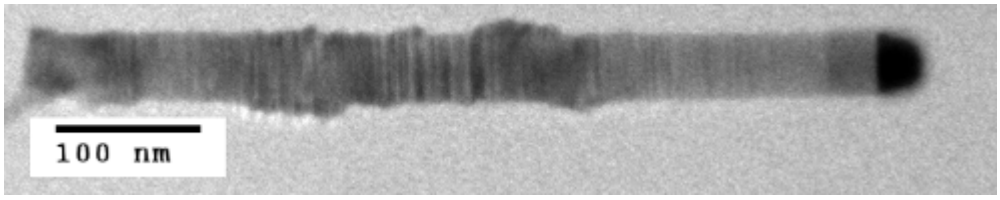
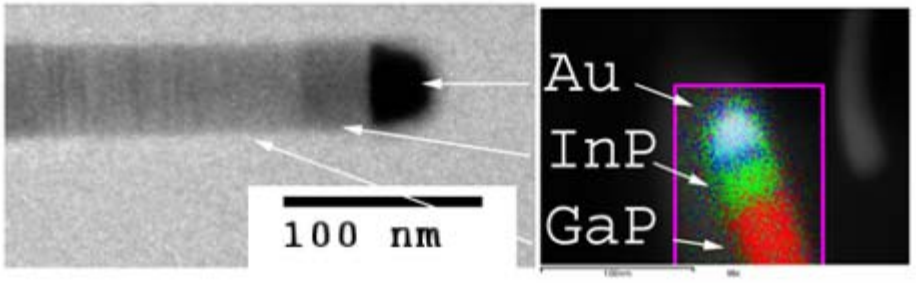
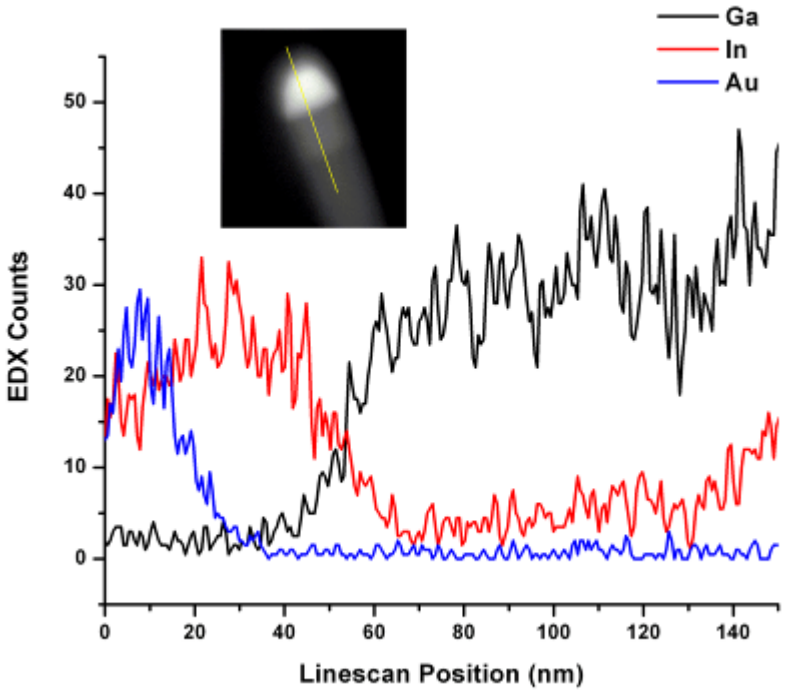


Figure 4.3 A XTEM image GaP/InP single nanowire heterostructure is shown above. At the InP growth temperature of 410°C there is a slight amount of lateral overgrowth occurring along the length of the GaP segment.



a)



b)

Figure 4.4 The image in a) matches the XTEM image from Figure 4.3 to an EDX map taken in HAADF STEM. The plot in b) is an EDX line scan taken along the tip of the wire (inset) clearly indicating an InP region separating the GaP and Au segments.

Further suppression of 2-D InP growth was explored by lowering the InP growth temperature to 390°C. XTEM inspection of samples revealed a thick coating of InP on the surface of the GaP nanowire cores along with significant surface roughness in somes cases and Au migration away from the tip of the wire [Figure 4.5]. At these growth temperatures it is apparent that decomposition of PH_3 is no longer a constant as is it often is at higher growth temperatures. Without excess phosphorous adatoms available (like in traditional MOCVD), indium is left unable to form InP on contact with the surface. The relatively long diffusion length of In atoms on free III-V nanowire surfaces is well known [67], so indium in this case is free to migrate around the entire GaP wire core and

eventually form a shell when it finds available phosphorous, even after TMIn has been shut off.

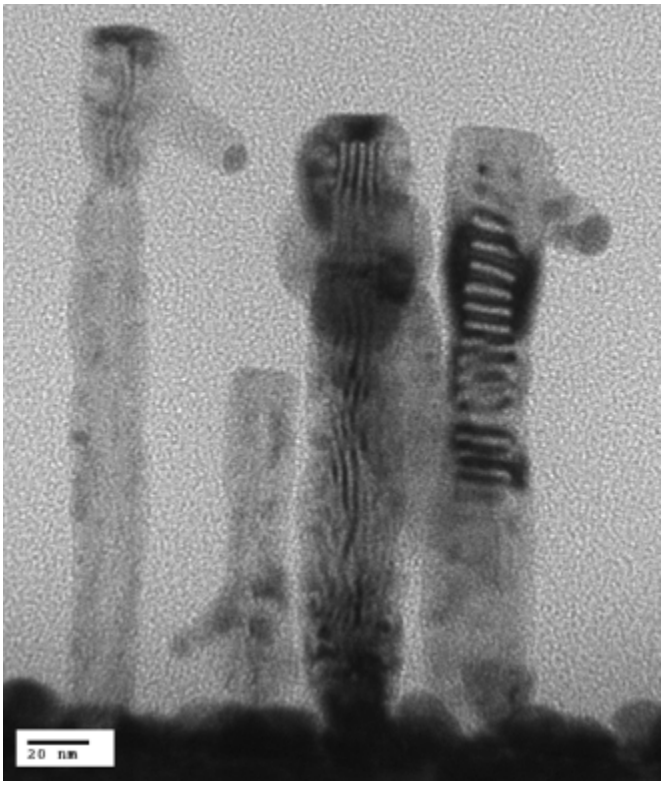
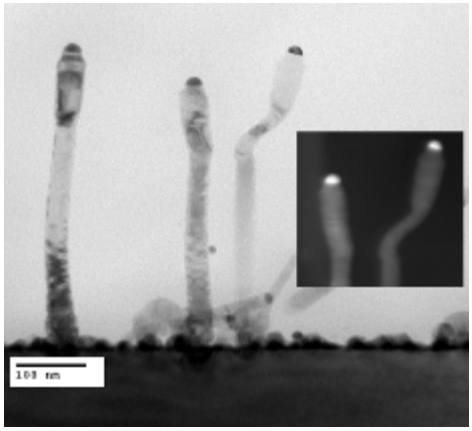


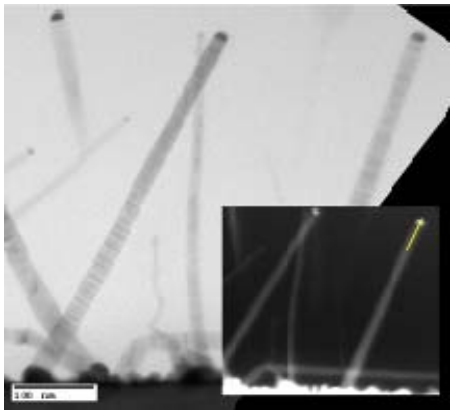
Figure 4.5 InP deposited at 390°C on GaP nanowires cores exhibits drastically different morphology compared to deposition at 410°C. The InP in this case completely encompasses the GaP core.

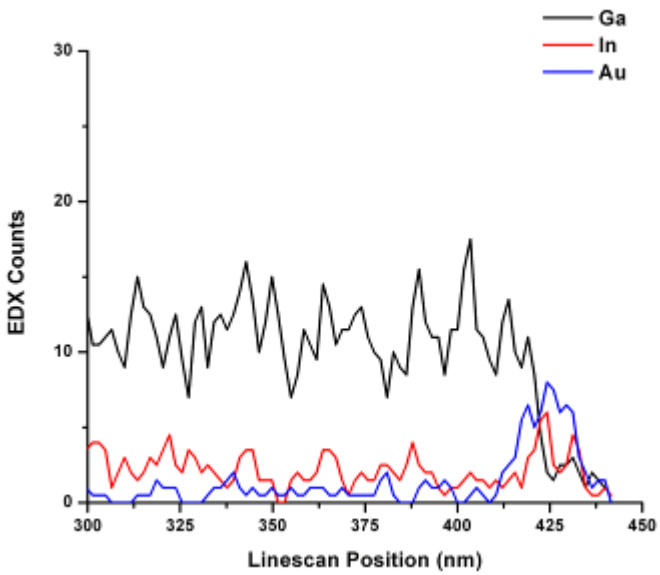
4.2.2 Double nanowire heterostructures

Development of the second heterostructures ($InP_{(w)}/GaP_{(w)}$) was initially explored by growing the first GaP segement at 450°C, cooling to 405°C to grow the InP segment, and then ramping the temperature back up to 450°C for GaP growth. The growth temperature of 405°C was chosen as it is hot enough to grow axial nanowire heterostructures and cool enough to minimize lateral overgrowth of InP. Inspection of these samples using HAADF STEM coupled with EDX revealed no significant InP

growth along the length of the wire [Figure 4.6]. However, despite the lack of In present along the length of the wire, there is a consistent change in wire morphology 300nm from the substrate. This is the expected length of the first GaP and the point at which we would expect to see InP if it were to have formed an axial nanowire heterostructure. EDX analysis towards the wire tip reveals a relatively strong presence of indium in the catalyst particle [Figure 4.6c]. The increase in temperature from 405°C to 450°C after InP growth could be resulting in an increase of InP solubility within the Au catalyst, consuming the InP beneath.

a) 

b) 

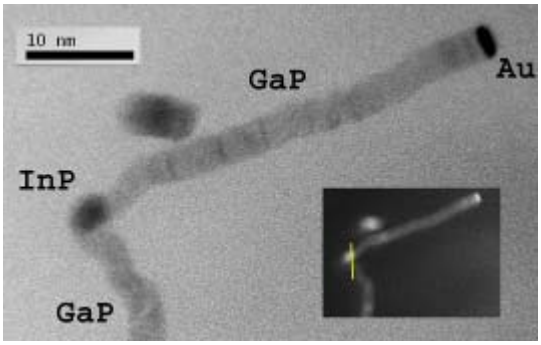


c)

Figure 4.6 The XTEM images in a) and b) show typical wire morphologies of when the second GaP segement is grown at 450°C. The wires in a) have a change in shape consistently occurring at about 400nm in their growth direction. However, there is no sign in STEM of InP. The inset in b) shows the location of the EDX line scan, shown in c). While very little indium is detectable along the length of the wire, there is a clear peak of indium matching that of the Au catalyst suggesting the wire may be re-dissolving InP as the temperature is increased from 405°C to 450°C.

Previous work (Chapter 3) on the development of GaP VLS nanowires had indicated that growth at lower temperatures results in longer facet lengths, consistent with Johansson, et al. [68], despite good epitaxy on Si substrates. However, it is unclear whether or not the longer facet lengths will actually have a detrimental role in electron-hole recombination/generation dynamics. Growth of the second heterostructure (InP/GaP) was then attempted while holding the reactor temperature constant at 405°C.

Post-growth STEM and XTEM can be seen in Figure 4.7. The resultant morphology shows some interesting growth artifacts regarding directionality and uniformity which may arise from any number of factors during growth. Despite this, some wires exhibit a two-tone contrast in HAADF STEM, highly suggestive of a GaP/InP/GaP double heterostructure [Figure 4.7a]. EDX analysis of these structures confirms the double heterostructure with InP between two GaP nanowire segments [Figure 4.7b]. Also notable is the lack of lateral overgrowth of InP on GaP or of GaP on InP.

a) 

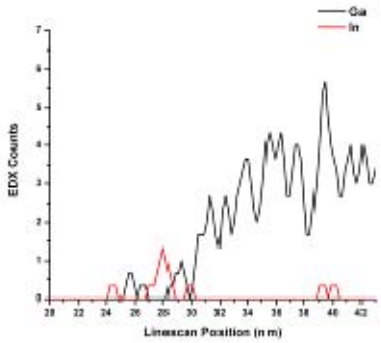
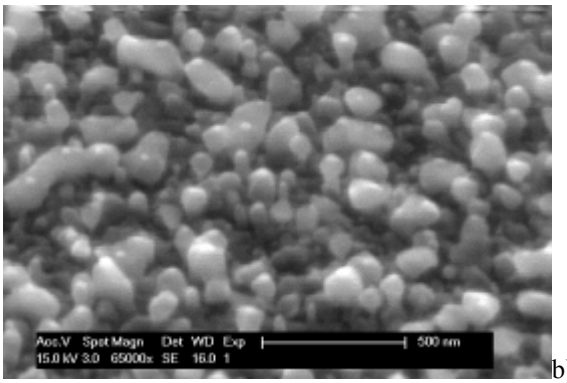
b) 

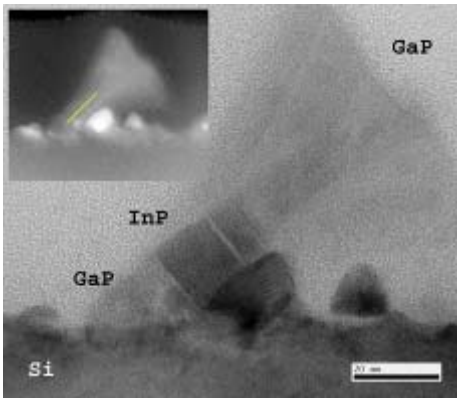
Figure 4.7 The XTEM and STEM (inset) in a) show a GaP/InP/GaP nanowire double heterostructure. The EDX linescan (shown in the inset of a)) cuts directly through the first InP/GaP transition. The EDX plot in b) shows a clear transition from GaP to InP as expected from the XTEM.

A second growth was performed with the same temperature profile mentioned above except an additional growth step of 2 min at 650°C was done at the end of the growth to coat the double heterostructure with GaP. The PH_3 flow rate was increased to 70 sccm and the TMGa flow rate was increased to 0.06 sccm to ensure uniform, non-selective GaP deposition. This step ideally passivates the exposed InP sidewall facets. SEM, XTEM and HAADF STEM images from this growth can be seen in Figure 4.8. HRTEM analysis of the InP segment reveals a wurtzite crystal structure with a lattice constant of a = 0.42 nm +/- 0.01 nm which is on the same order of the lattice constant a = 0.415 nm predicted and discovered by [69]. The measured c-plane lattice constant was c = 0.65 +/- 0.02 nm which is very close to the predicted value of c = 0.6777 nm from [69]. At this time we are unable to resolve the degree of strain within the wurzite layer. The compressive strain arising from GaP-coated InP should drive the InP lattice constant to smaller values, consistent with the observed measurements. No threading dislocations were visible using two-beam diffraction conditions. However, this does not rule out the

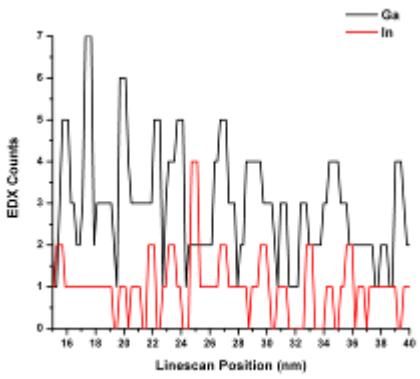
possibility of defects at the GaP/InP and/or InP/GaP interface. EDX in HAADF STEM additionally confirms the $GaP_{(w)}/InP_{(w)}/GaP_{(w)}/GaP$ double heterostructures. Additionally, we note that while the true the origin of the wurtzite InP crystal structure is unclear, some suggest this may be directly related to InP nucleation [70] on the GaP surface. The GaP overcoat on many wires also appears to be strongly faceted. This may be overcome in the future by changing the growth temperature of the final GaP layer to increase uniformity.



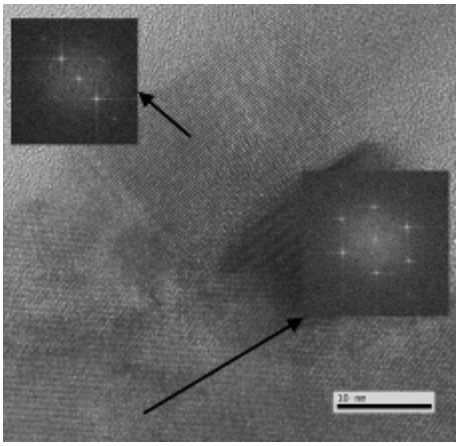
a)



b)



c)



d)

Figure 4.8 A 45-deg. tilt SEM image is seen in a). Note that the majority of wires in this region are growing vertically from the Si substrate. A XTEM image from this sample is seen in b) with a STEM as the inset in the upper left. The line drawn in the STEM image corresponds to the EDX linescan in c). The indium peak found in the EDX scan corresponds well with the region of dark contrast in XTEM. HRTEM in d) shows FFTs of both the substrate and the wurtzite InP region.

4.3 Conclusions

In summary, we have demonstrated $GaP_{(w)}/InP_{(w)}/GaP_{(w)}$/GaP nanowire double heterostructures grown using the vapor-liquid solid mechanism. The stable, controlled growth of InP on GaP is achieved by finding a temperature window in which InP deposition is limited to underneath the catalyst without changing the gas decomposition rates. Regrowth of GaP on InP was only achieved by growing GaP at the same temperature used for InP growth which prevented any disturbance of the Au/InP interface. Lastly, a GaP layer was grown to encapsulate the double heterostructure which could potentially reduce surface recombination in nanowire double heterostructure device.

5. Nanowire device integration

5. Nanowire device integration

Despite the many attractive features of nanowire based devices, perhaps the biggest hurdle to realizing their potential lies in the ability to integrate these wires into larger systems. Nanowires defined by lithography benefit from the fact that they are processed using the same methods as conventional transistors. However, as mentioned previously, top-down nanowires are basically limited to Si systems. This prevents them from exploiting the benefits of III-V devices built on a Si platform. Nanowires grown by the VLS mechanism first require the Au catalyst particle to be precisely placed before the nanowire is then grown into place. This allows for dissimilar materials to be used in each step as long as they can be integrated without negative interactions. However, one disadvantage to this whole method is that the semiconductor industry isn't used to using dissimilar materials at the device level. For the most part, Si transistors, GaN HEMTs and InP HBTs use Si, GaN and InP, respectively as the active elements in each device. Some minor material modifications to basic devices, such as silicide contacts or SiGe MOSFET channels, have been realized, but only after intensive research and development by the semiconductor community at-large. Despite this challenge we have undertaken some initial work to integrate III-V nanowire devices into Si systems using conventional semiconductor processing steps wherever possible to reduce redundancy.

5.1 Large Area Arrays

Arrays of discrete devices or functional elements are the basic building block behind many electronic products. Solid-state memory, photodetectors and displays are all technologies which rely on addressing unique locations of an array during operation. It is

essential to each of these devices that each pixel, crystal, magnet, etc. be positioned precisely in the right place otherwise the data gathered or displayed will be compromised. Diskette technology and lithography are among the most common approaches to fabrication of large area arrays.

Diskette technology goes back to the 1970s where the active element, such as a memory bit, is placed in direct line-of-sight with the read/write mechanism. For example, this read/write technology can be a laser, as with CDs and DVDs, or it could be a magnetic head, as with common hard-drives. Regardless, diskette type technologies require the combination of a simple array with a high-precision mechanism to read/write each bit. While such mechanical precision was once thought of as nearly impossible, advances in micro- and nano-manipulation have proven diskette technology to still be relevant some 40 years after its inception.

Photo-lithography-based arrays have become quite ubiquitous in the last decade or two as lithography has advanced into the sub-micron regime. As a result, the ability to pattern small features with high resolution has significantly contributed to the growth of the sensor and display markets. While the active element need not be on the sub-micron scale, as is the case for liquid-crystal displays (LCDs), lithography-based arrays hinge on the ability to pattern lines and interconnects to each individual component (crystal, sensor, etc.). This allows the elements to not only be individually activated, but also multiplexed by activating any or all of them simultaneously.

While multiplexing individual components in an array certainly has its advantages in terms of device capabilities, it also requires complex wiring which can be significantly cost prohibitive. Serial-addressing, as with diskettes, is adequate for many computer

applications so the need for expensive interconnects is not a burden. Instead, it makes the most sense to make the media as cheap as possible as long as it is compatible with the read/write mechanism. Optical data storage media, such as DVDs, CD-Rs, etc., are ideal in that one read/write mechanism is not limited to one media diskette.

In this research we have chosen to focus our efforts on large-area arrays which are compatible with Si substrates. This serves two purposes; Firstly, if complex wiring and multiplexing is desired for a lithographically-defined array, Si substrates provide the most practical platform for experimentation in terms of cost and availability. Secondly, Si substrates provide a relatively inert, highly planar and well characterized starting point to deposit or grow our nanowires. From these substrates the wires can be easily probed and characterized.

5.1.1 Au-colloid Self Assembly

One method for distributing catalyst particles into ordered arrays, which has gained attention over the last decade, is known as "self-assembly". Self-assembly is a technique by which particles (Au-colloid in this case,) are dispersed onto a substrate and spontaneously arrange themselves into a desired configuration. In this case we are concerned with simple patterns such as regular square arrays, hexagonal arrays, or linear chains.

Most self-assembly techniques involving Au-colloid particles try to leverage either the charged nature of the particle and shell or they try to exploit topography of the substrate to place the particles in their desired location. This work to develop catalysts for

nanowire growth focused primarily on Au-colloids dispersed onto Si substrates with topographic features.

The behavior of Au-colloid solutions dispersed onto blank SiO_2 substrates is fairly well understood. The hydrophilic nature of the SiO_2 surface will pin the droplet edges at their initial position. As the droplet evaporates a small volume of liquid from the center of the droplet is driven towards the droplet edge to maintain a fixed contact angle between the droplet and the substrate. During this process, additional Au-colloids push towards the outer edge of the droplet. When too great a volume of liquid has evaporated for the droplet to maintain its original perimeter and contact angle, the droplet will contract to reduce its surface area and perimeter. Once this happens, the contact angle is restored to its equilibrium and the whole process repeats itself until the droplet has completely evaporated. As discussed by [45], this is also the process responsible for the ring pattern of coffee stains.

To confirm this effect as a starting point for our later experiments with topographic features, 20nm Au colloids were dispersed onto SiO_2 covered Si substrates. Our Au-colloid particles clearly exhibited this phenomenon as seen in [Figure 5.1]. The bands of colloids from this "stick and slip" mechanism appear to be regular and well-defined. Examining the Au-colloids, it is clear that they appear to be in direct contact with each other. Nevertheless, nanowire growth was pursued on these substrates as a starting point for self-assembled catalyst research.

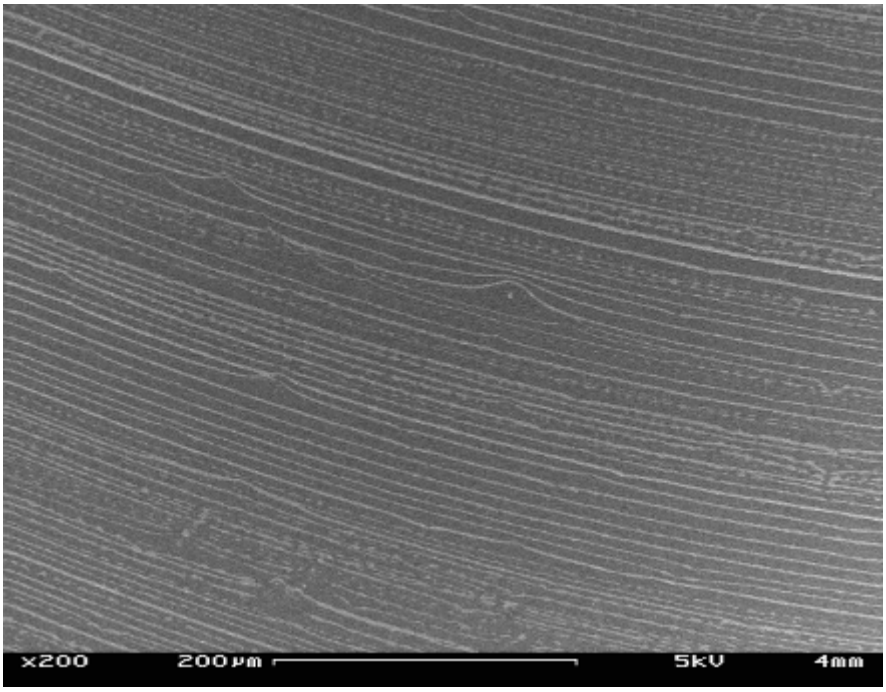


Figure 5.1 SEM image of 20nm Au colloids on 100nm-thick SiO_2 on Si (100) substrate. Note the distinct bands formed from the 'stick and slip' mechanism. (Courtesy S. Chang 2006)

To achieve epitaxial growth, the native oxide underneath the Au-colloid particles must be removed using HF-etching. However, it is expected that this HF dip will simultaneously etch the SiO_2 surface and possibly redisperse the Au-colloid particles. After HF-etching, the samples were loaded into the reactor and nanowire growth was commenced following the growth recipes developed in Chapter 2.

Post-growth SEM inspection revealed significant particle coalescence as the Au-colloids alloyed both with each other and the substrate underneath, seen in Figure 5.2. Wire growth appears to lack any directionality beyond the expected <111> directions of the substrate. Some Au migration appears to be bridging the particle bands, however, it's unclear if this is the result of Au migration or if this is from Au-colloids linking bands before growth.

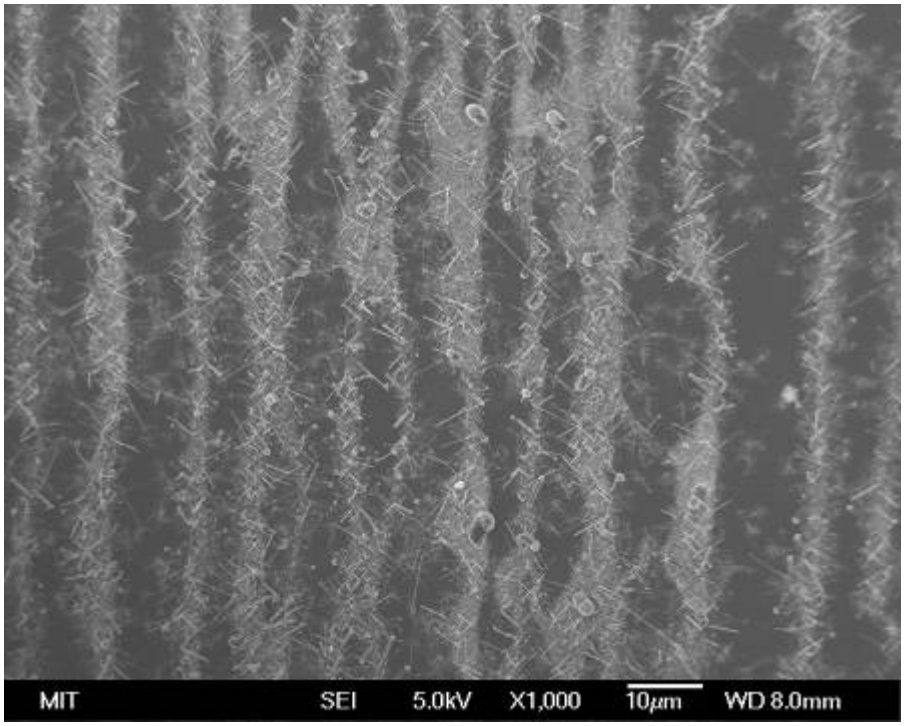


Figure 5.2 Top-down SEM image of Si nanowires grown from 20nm Au-colloid particles on Si (100) substrate. Note the bands have bridges in several places and the wires appear to have a wide range of sizes from microns in diameter down to the original 20nm size.

Topographic features on the Si substrate were developed using a Si (100) substrate with 55nm of thermally grown SiO_2 was subsequently patterned to produce holes which open to the Si substrate and were approximately 300nm in diameter with a 500nm pitch in a regular square array. The substrates were then dipped into a 50nm Au-colloid solution and slowly removed such that capillarity will drive the Au-colloid particles into the circular openings as the solvent evaporates. Proper control of the Au-colloid density, withdrawal speed and topographic feature size can lead to complete filling of the holes with minimal colloid deposition on the surface of oxide [Figure 5.3].

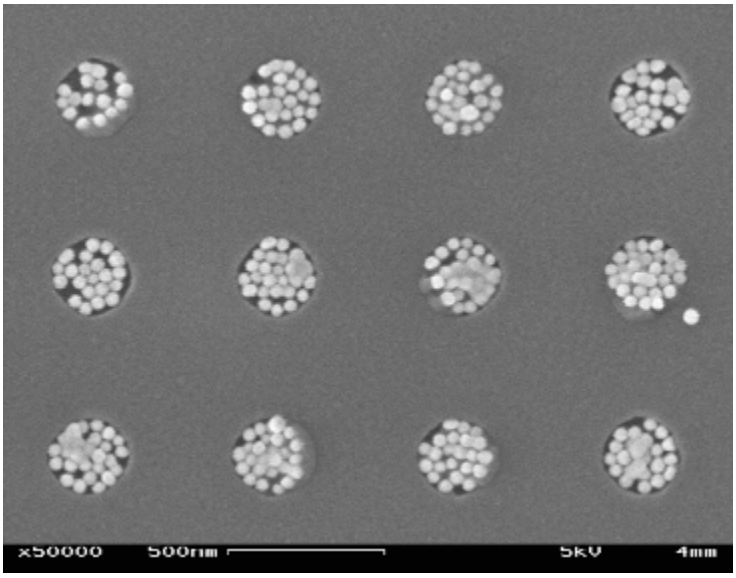


Figure 5.3 SEM image of 50nm Au-colloid particles dispersed onto a Si (100) substrate with 300nm holes pattered in a 55nm-thick SiO_2 layer. The particles naturally fill in these oxide holes as the substrate is slowly removed from the Au-colloid solution. (Courtesy S. Chang 2006)

The samples with SiO_2 holes and Au-colloid particles assembled in them were given a light 10s 50:1 H_2O:HF dip to promote epitaxial nanowire growth. Following this treatment, the sample was immediately loaded into the reactor. Growth was carried out using the recipe as for the "stick and slip" sample above.

Post-growth SEM inspection revealed some particle coalescence as the Au-colloids alloyed both with each other and the substrate underneath, seen in Figure 5.4. In addition to alloying with the substrate, it appears that some colloids first etched into the substrate following the phenomenon demonstrated by [71]. Again, no directionality preference was seen for these growth conditions other than the four <111> directions out of the plane of the <100> substrate, similar to the 'stick-and-slip' samples. Surprisingly, the wires appear to vary in diameter from the tens to hundreds of nanometers instead of being of a uniform 200nm indicating incomplete coalescence during annealing. In addition, it appears the Au-colloids are redistributed across the substrate, likely due to the

HF dip prior to growth. Given the complications with the self-assembled Au-colloids and imperfect arrays, other methods were subsequently explored for the development of large-area arrays of Si nanowires.

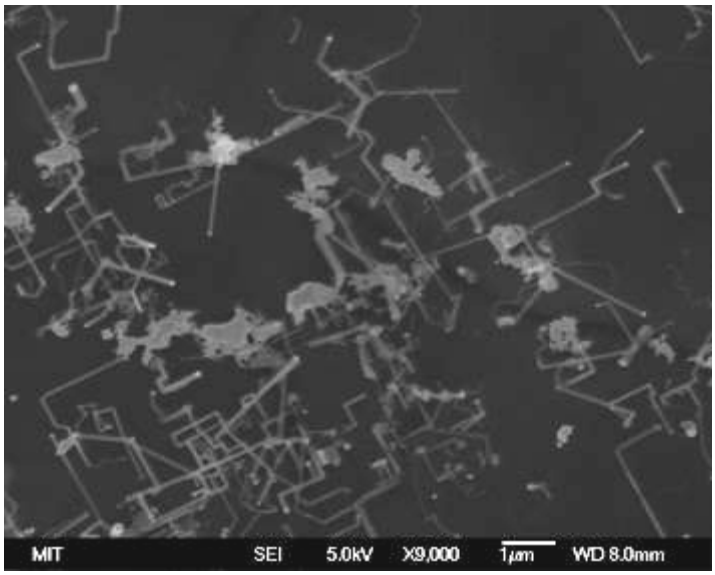


Figure 5.4 Top-down SEM of Si nanowires grown from the substrate in Figure 5.3. The wires appear to have lost most resemblance of the original holes in the oxide layer. The right angles of the wires relative to each other indicate vertical epitaxy to the Si (100) substrate. However, there appears to be no preferred <111> growth direction in this case.

5.1.2 Polystyrene Sphere Lithography

Polystyrene sphere lithography (PSL) is a way of patterning large area hexagonal arrays of Au and other materials. PSL is advantageous in that it requires very little raw materials or instruments to make a pattern. Originally developed and investigated by a number of groups for a wide variety of applications [72, 73], PSL was pursued in-house to support another project involving Au on Si. However, its portability to our application made it a natural choice for nanowire exploration.

The technique, fully documented elsewhere [73], employs a raft of polystyrene spheres (of essentially any diameter,) in an aqueous solution which naturally form into

large-domain close-packed 2-D hexagonal arrays. A substrate is then immersed into the solution and slowly removed so that the raft sets on the surface of the substrate. The substrate is then removed with the PS array on the surface and a Au thin-film is deposited by e-beam evaporation on the top of the spheres. This film decorates the tops of the spheres with Au while a small amount of Au is deposited between the spheres in the triple-junction where three spheres meet. A solvent such as acetone is then used to dissolve the polystyrene spheres and Au dots of triangular shape on the order of 100nm in diameter are left in a hexagonal array [Figure 5.5] with about 400nm between nearest neighbors.

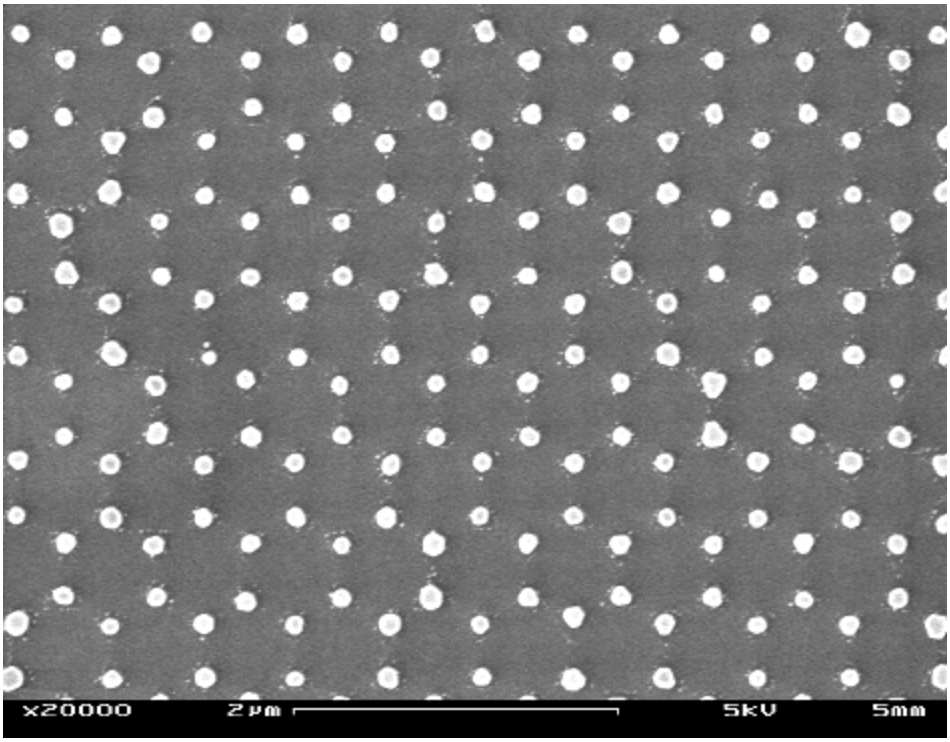
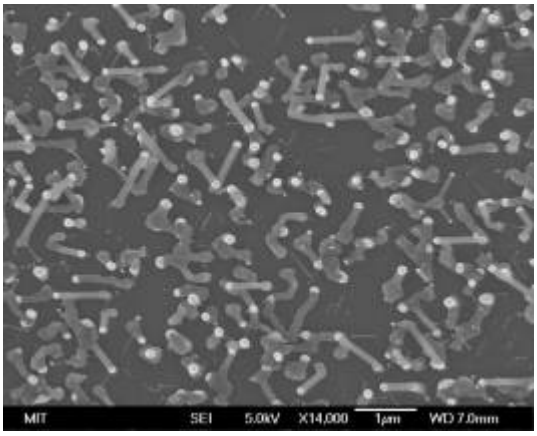


Figure 5.5 Au catalyst nanoparticles deposited on a Si (111) substrate using polystyrene sphere lithography. The particles here are approximately 100nm in diameter with 400nm between nearest neighbors. The hexagonal array is a result of the triple junctions between neighboring polystyrene spheres.

Following PSL and Au deposition on a Si(111) substrate, the samples were dipped in dilute HF-H_2O to remove the native oxide shell covering the Au catalyst

particle and the samples were immediately loaded into the reactor prevent re-oxidation of the catalyst. Si nanowire growth was then carried out according to the recipes mentioned previously in Chapter 2.

Following growth, the wires were inspected by SEM. The top-down SEM image in Figure 5.6 clearly indicates epitaxial growth from the Si (111) substrate. The triangular arrangement of wires indicates some wires are growing in off-axis out-of-plane <111> directions. Investigation by tilted SEM revealed many wires also growing vertically from the substrate despite some small perturbations at the substrate/wire interface. Recalling the deposition conditions for the Au film, we are unable to etch the native oxide between the spheres, so it is presumed that a native oxide remains present between the as-deposited Au and the Si substrate. As nanowire growth is commenced, the Au catalyst saturates with Si but the native oxide underneath the Au prevents it from immediately growing an epitaxial wire. The Au supersaturates and expels Si on top of the oxide and then migrates to H-terminated Si where the nanowire grows epitaxially. This oxide layer is likely at fault for the misoriented wires not growing vertically from the substrate. Due to the fundamental inability to strip the native oxide between the polystyrene spheres, this method leaves little room for development of epitaxial ordered arrays without a fundamental change in the process flow for catalyst deposition.

a) 

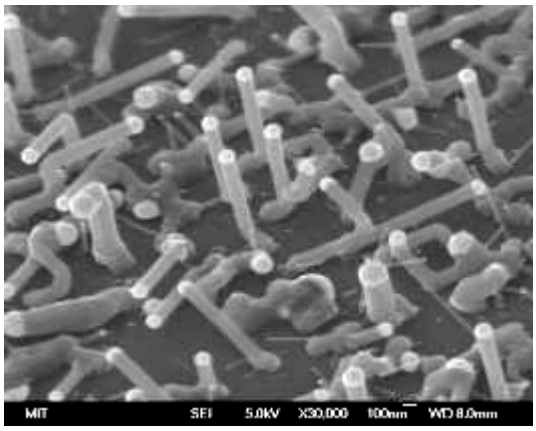
b) 

Figure 5.6 Top-down (a) and tilted (b) SEM images of Si nanowires grown from Au catalyst particles fabricated using polystyrene sphere lithography. The most of the wires appear to be single crystalline. However, the perturbations at the bases of each wire are likely the result of contamination between the Au catalyst particle and the Si (111) substrate. Note the presence of small (~ 10nm - 20nm) diameter wires originating from around the bases of the larger wires. These are likely a result of small residual Au particles during the Au agglomeration step.

5.1.3 Inverted Pyramid Arrays

Work by [6] revealed a repeatable method for producing mono-dispersed, isolated Au particles using inverted pyramids on Si substrates. These are synthesized by first opening holes in SiN_x layer on Si <100> substrates using reactive-ion etching and a photoresist etch mask. If the holes in the SiN_x layer were developed using interference lithography, then it is straightforward to create an array of holes with a 200-800nm pitch. Once the substrate is exposed at the bottom of the holes, the sample is then dipped in KOH to etch the substrate and reveal <111> planes creating inverted pyramids.

In the original work by Giermann, et al., the SiN_x was removed and a chemical SiO_2 layer was grown on the Si surface. Various thicknesses of Au were then deposited and a dewetting process was employed to deposit Au particles in the inverted pyramids [Figure 5.7]. For our work, alternate processing must be employed to realize ordered Si

nanowire arrays on these inverted pyramid substrates as the chemical oxide prevents epitaxy to the Si substrate.

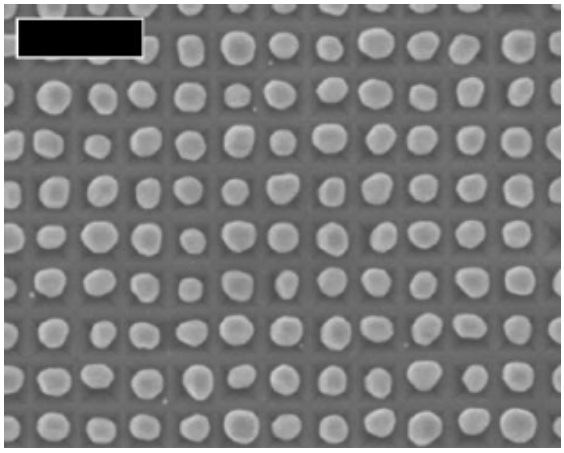


Figure 5.7 Ordered arrays of Au particles with a one particle per pit and no extraneous particles, 175nm period narrow-mesa substrate with 21nm thick film. The scale bar here is 500nm. Image reproduced from Giermann, et al[6]

Inverted pyramid array substrates with a pyramid edge length of 150nm and a pitch of 200nm which had not had a Au film-deposited, but were stripped of the nitride layer were first used to explore Si nanowire growth. These samples were dipped in 50:1 H_2O:HF for 10 seconds before being immediately loaded into a Perkin-Elmer e-beam evaporator and pumped to ~10^{-9} torr to prevent reoxidation of the substrate. 20nm of Au were then deposited on the substrate at 0.1 nm/sec at room temperature. Following Au deposition, the samples dipped in dilute HF:H_2O 1:1 for between 1m and 10m Si nanowire growth was initiated according to the recipes and methods discussed in Chapter 2 to achieve high quality vertical epitaxy from Au thin-films on Si (111) substrates.

Post-growth SEM can be seen in Figure 5.8. The wires from the sample which was HF-dipped for 1 m appear to grow in all of the <111> directions of the substrate despite growing with relatively high diameter uniformity. The lack of specific <111>

directionality can be attributed to the Au layer being thick enough to anneal into the substrate and dissolve the exposed facets which eliminates any topography induced growth direction preference. The sample which was dipped for 10 min. does not seem to show much wire growth, but rather the Au appears to have etched into the substrate [Figure 5.9] following the mechanism described by [71].

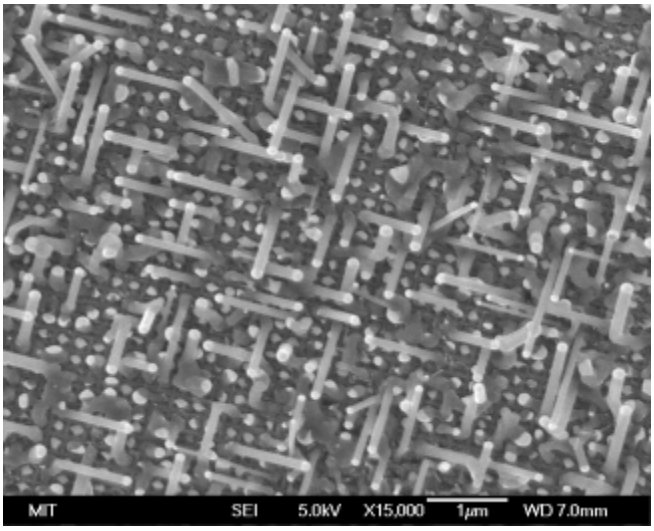


Figure 5.8 Si nanowires grown from a 20nm-thick Au film deposited at 0.1 nm/sec at room temperature on inverted pyramid array on a Si (100) substrate. This sample was subjected to 1m of HF:H_2O 1:1 treatment prior to growth.

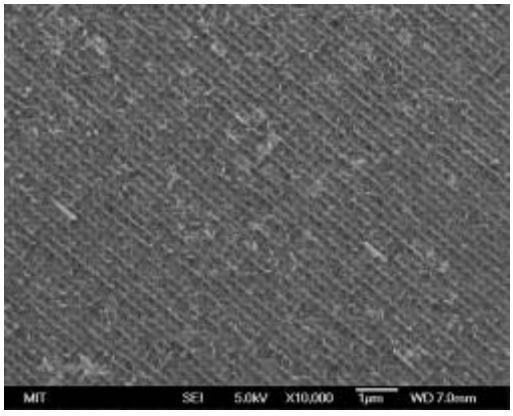


Figure 5.9 Image of identical sample to the one in Figure 5.8. However, this sample was subjected to 10m of HF:H_2O 1:1 treatment prior to growth. Note, there are only two nanowires growing in the entire field of view of this image.

A second Au-deposition of 1nm was done on fresh substrates of the same batch mentioned above (post-nitride etch). These samples were then grown on according to the same Si nanowire growth recipe used previously to ensure consistency. Post-growth SEM from these samples can be seen in Figure 5.10. Towards the edge of the sample in the region where no Si nanowire growth has occurred; it appears the Au has little or no selectivity to any topographic feature of the substrate, except perhaps some affinity to the facet intersections of the inverted pyramids. Investigation of the region where Si nanowire growth was ample revealed virtually no growth direction preferentiality. All the wires appear to maintain their original diameter based on the size distribution of Au catalysts, seen in Figure 5.11.

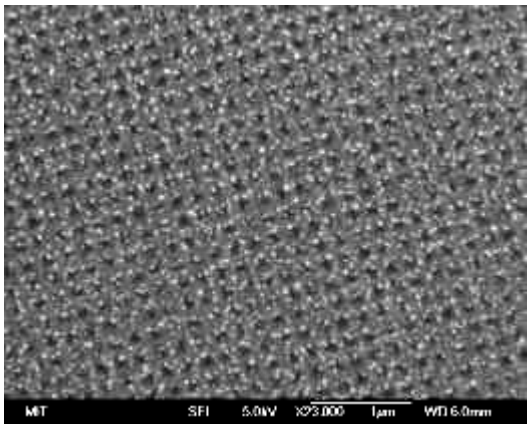


Figure 5.10 Top-down SEM image of a 1nm-thick Au film deposited at 0.1 nm/sec at room temperature on an inverted pyramid array on a Si (100) substrate. This image was taken in the edge-exclusion region of the sample where the nanowire growth is minimal allowing us to image the catalyst particles.

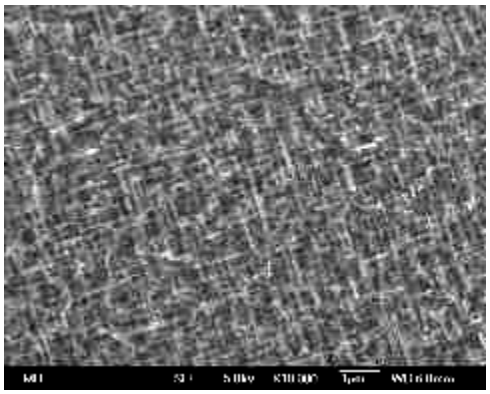


Figure 5.11 Top-down SEM image of the center region of the sample in Figure 5.10. The strong four-fold symmetry suggests no preference for any particular <111> direction of the substrate as is expected from the placement of the Au catalyst particles in Figure 5.10.

Following these growths, new substrates were fabricated which were not stripped of their SiN_x protective layer before Au deposition. These samples, which have the same pitch and pyramid dimensions as the ones used previously, were first dipped in 50:1 H_2O:HF for 30 sec to remove the native oxide on the pyramid sidewall facets, but careful attention was paid to make sure the SiN_x barrier layer was not etched during this process. The sample was then immediately loaded into the e-beam evaporator and pumped down to base pressure (~10^{-9} torr). For Au deposition, a tilted chuck was used to produce a 60 degree incline relative to the crucible. By aligning the pyramids normal to the tilt angle, we attempt to produce conditions such that Au is predominately deposited on just one of the four exposed sidewall facets. A 1nm-thick film of Au was then deposited at 0.01 nm per minute at room temperature. Following deposition, the sample was soaked in HF for 10 min to remove the SiN_x layer and loaded into the reactor for nanowire growth. Si nanowires were grown for 90 min with 0.18 sccm of silane at 550°C, essentially identical conditions to those used previously.

After growth, the samples were inspected by SEM. Top down imaging of the edge-exclusion region where no growth occurs [Figure 5.12] indicates a fairly high selectivity to three of the four pyramid sidewall facets, a result of the e-beam shadowing. An image taken from the region where wires grew to be ~1um similarly suggests some selectivity among the sidewall facets [Figure 5.13]. However, it is not entirely clear whether or not one sidewall facet is the preferentially nucleating wires as there are many instances of wires growing in all directions. Lastly, we examine the center region of the sample where the growth rate was the highest. In this case it appears that the overwhelming majority of wires are all growing in one of the four <111> directions of the substrate [Figure 5.14]. It is unclear whether this is the result of laminar flow pushing the wires to kink, collisions of growing wires which resulting in kinking, or possibly a feeding effect from the precursors. In addition, it appears as though the pyramids are not producing one wire per pit, but often two or sometimes three wires per pyramid.

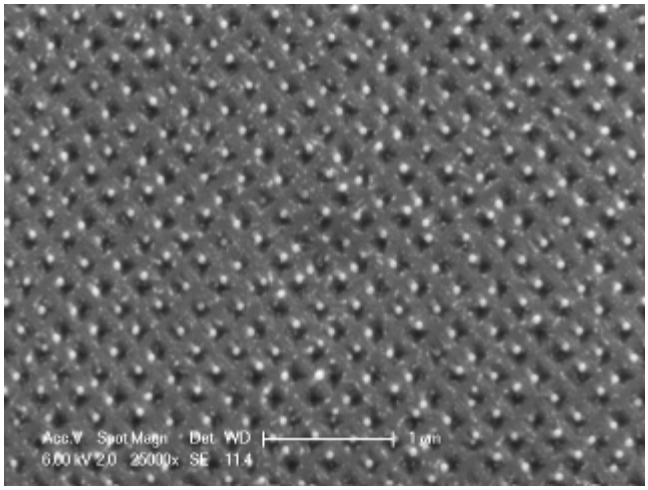


Figure 5.12 Top-down SEM image of a 1nm-thick Au film deposited at 0.1 nm/sec at room temperature onto an inverted pyramid array on a Si (100) substrate. Au deposition in this case was also done at a 60 degree incline relative to the Au flux before the SiN_x protective layer was removed. This image was taken in the edge-exclusion region of the sample where growth was minimal. The catalysts appear to have a preference for one of the four Si {111} facets of the inverted pyramids.

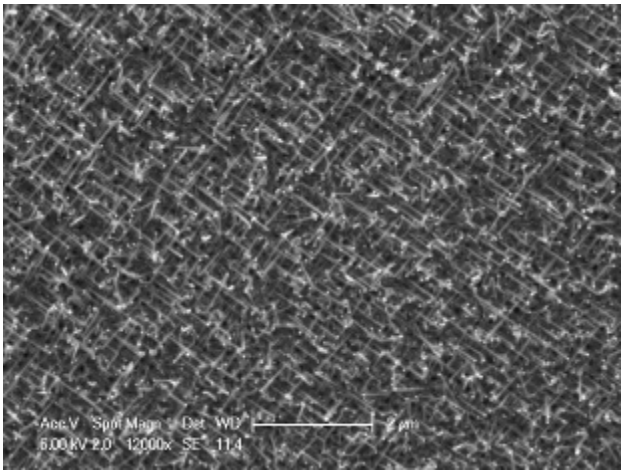


Figure 5.13 Top-down SEM of the substrate from Figure 5.12 taken in a region of moderate Si nanowire growth. Note that in this region the wires do not immediately appear to have any directional preference.

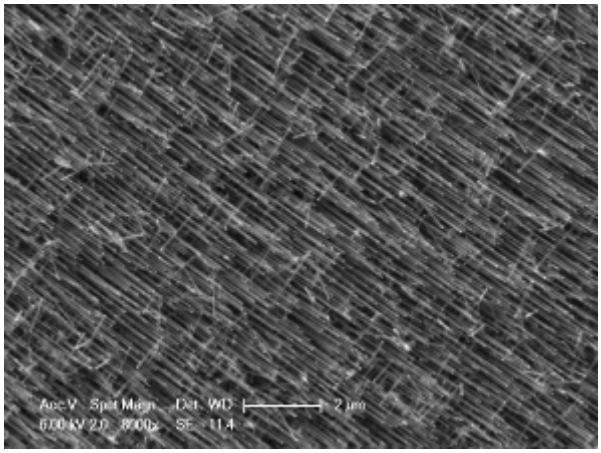


Figure 5.14 Top-down SEM of the substrate from Figure 5.12 taken in a region of rapid Si nanowire growth. In contrast to the wires in Figure 5.13, the wires in this region appear to have a significant preference for one of the four <111> directions of the underlying Si (100) substrate.

Additional inverted pyramid arrays with the nitride windows were again etched in dilute HF and loaded into an e-beam evaporator on a tilted chuck for angled deposition. A 1 nm-thick Au film was deposited at 0.01 nm/min, but this time at 350°C. At this temperature the Au should have enough mobility to migrate on the exposed {111} facets and coalesce into larger particles, ideally giving one particle per pit. After Au deposition, the samples were etched in HF for 2 min to lift off the nitride protective layer and

immediately loaded into the CVD reactor for Si nanowire. Growth was carried out according to the conditions mentioned above to produce high quality, defect-free Si wires.

Following nanowire growth, the samples were inspected using top-down and tilted SEM. Inspection of the edge-exclusion region clearly indicates decoration of one sidewall facet with minimal Au deposition on the shadowed sidewalls [Figure 5.15]. Although the inverted pyramids do not appear to only have one particle per pit, the two or three particles which sit on the sidewall facets are close enough together that they can expand and coalesce as they are supersaturated with Si during the VLS growth process. Investigation of the center region of the sample where the growth rate is fastest revealed near perfect growth selectivity in some regions [Figure 5.16]. A small percentage of wires appear to be growing in directions perpendicular and opposed to the dominant <111> direction [Figure 5.17]. Some regions of the sample did not see the nitride completely lift off [Figure 5.18] and have little resemblance of any epitaxy to the substrate.

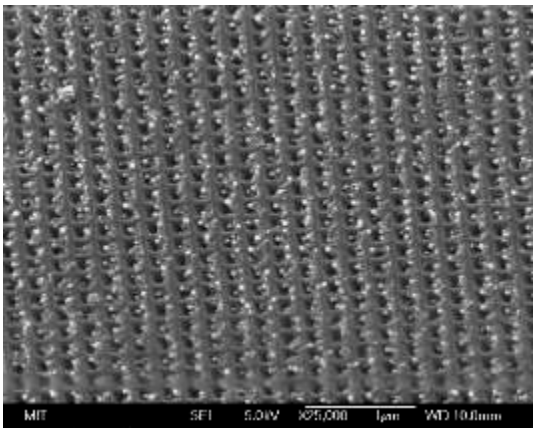
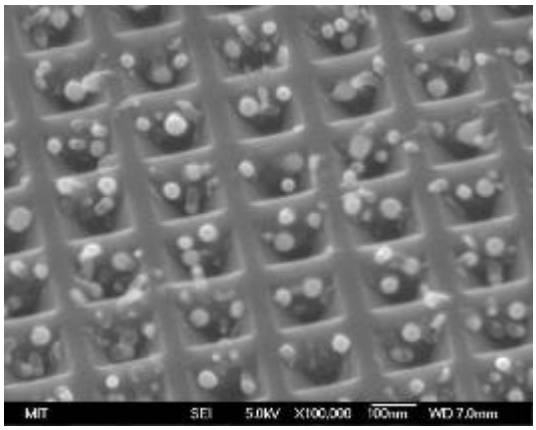
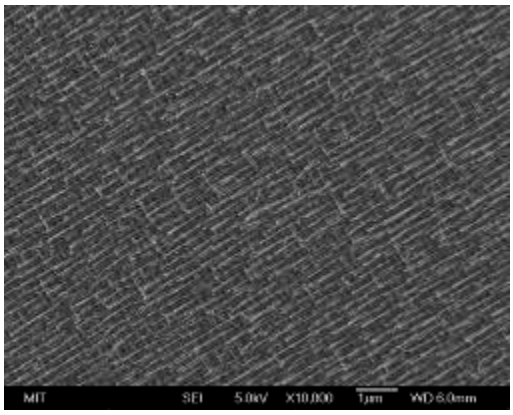
a)  b) 

Figure 5.15 Tilted SEM images of a 1nm-thick Au film deposited at 0.1 nm/sec at 350°C onto an inverted pyramid array on a Si (100) substrate. Similar to the sample in Figure 5.12, Au deposition in this case was done at a 60 degree incline relative to the Au flux before the SiN_x protective layer was removed. These images were taken in the edge-exclusion region of the sample where growth is minimal. Despite the high

sidewall selectivity, the particles do not have an ideal one particle per pit ratio thus yielding multiple wires per pit as seen in Figures 5.16 and 5.17.

a) 

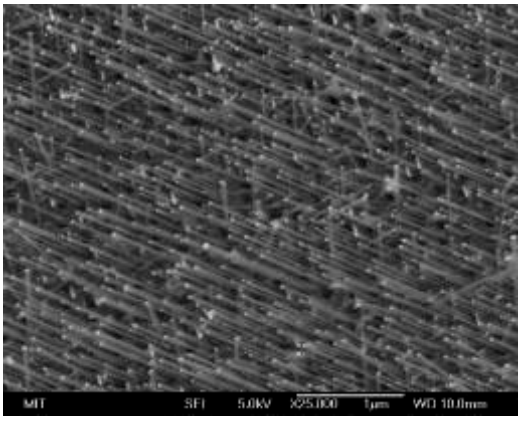
b) 

Figure 5.16 Top-down (a) and tilted (b) SEM images of Si nanowires grown from the substrate in Figure 5.15. The vast majority of wires appear to all be growing in the same direction with a very tight diameter distribution. Although the substrate does not have an ideal one particle per pit ratio, as the Au-catalyst particles saturate with Si prior to wire growth, many of the particles likely coalesce leading to a nearly 1:1 wire:pit ratio.

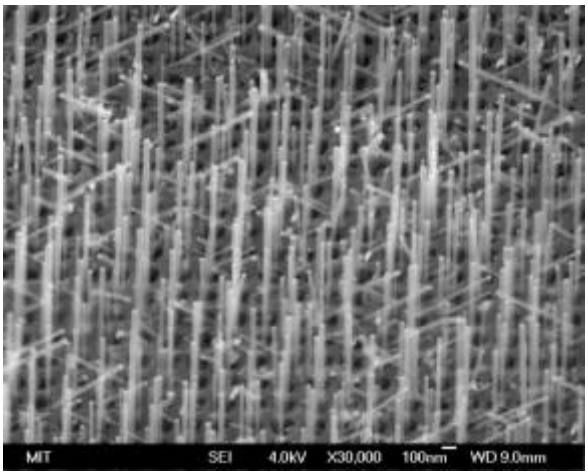


Figure 5.17 Tilted SEM image of the wires in Figure 5.16 taken at 90 deg. rotation relative to the image in 5.16b. Although most appear to be growing in one of the four <111> directions of the substrate, a number of wires are growing perpendicular to the primary growth direction.

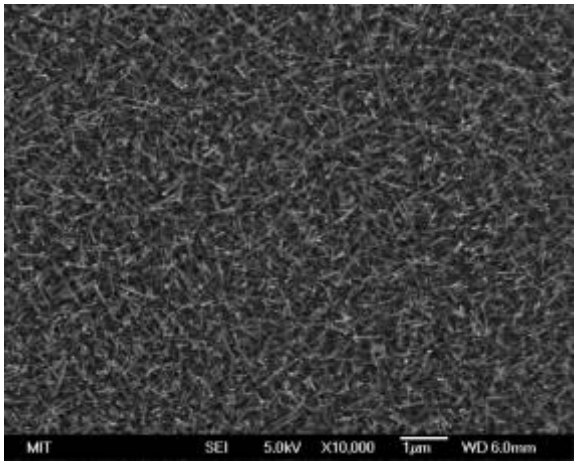


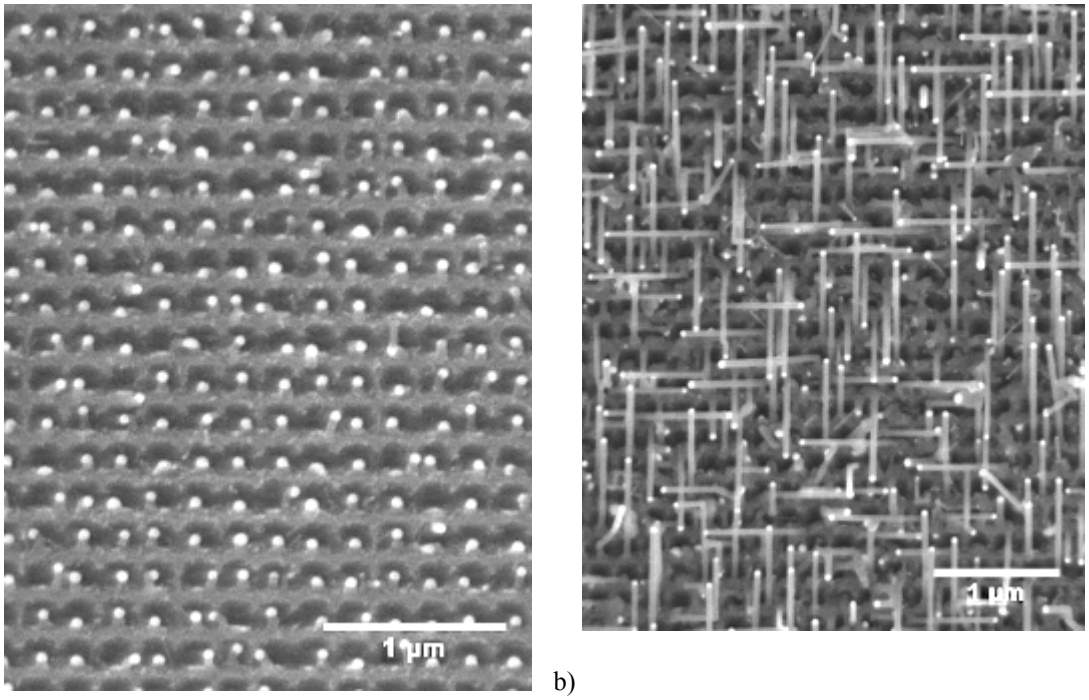
Figure 5.18 Top-down SEM image of Si nanowires grown from the substrate in Figure 5.15. The wires in this case are grown from a region where the SiN_x etch mask had not completely lifted off prior to wire growth, thus giving randomly oriented wires.

This growth marked the end of the supply of inverted pyramid arrays and substrates which gave highly repeatable results. Newly allocated substrates with questionable processing history up to the KOH etching step were used for future experiments.

Again, prior to growth these substrates were lightly dipped in HF to strip the native oxide but maintain the SiN_x layer. Au was deposited on the tilted chuck at 400°C, above the Au-Si eutectic melting temperature (~360°C [5], Figure 1.8). The Au evaporated on the Si surface instantly dissolves into the sidewall facet ideally preventing clustering from creating two or three Au particles per pit.

Following Au deposition, Si nanowire growth was carried out and post-growth inspection was done using SEM. Figure 5.19a revealed successful one particle-per-pit behavior in the edge-exclusion region. However, nanowire growth from this sample did not look as good as it did in previous growths [Figure 5.19b]. This is likely attributed to

the questionable processing history, premature Au-Si alloying or a weakly bonded nitride layer dissolving before Au deposition.



a) b)

Figure 5.19 Top-down SEM images of a 1nm-thick Au film deposited at 0.1 nm/sec at 400°C onto an inverted pyramid array on a Si (100) substrate. Similar to the sample in Figure 5.12 and 5.15, Au deposition in this case was done at a 60 degree incline relative to the Au flux before the SiN_x protective layer was removed. The image in a) was taken in the edge-exclusion region of the sample where growth is minimal. The particles appear to have an ideal one particle per pit ratio. However, after wire growth (b) the wires appear to have no preference for any particular <111> direction.

5.1.4 III-V nanowires in inverted pyramid arrays

Given the problems with Si nanowire growth on the sample with Au deposited at 400°C, GaP nanowire growth was pursued on substrates with Au deposited at 350°C. All deposition and processing parameters were identical to the ones used previously for Si wire growth. A sample was also stripped of the nitride layer in HF, and then set aside for SEM inspection to examine the pre-growth microstructure of the Au [Figure 5.20]. The

III-V growth recipe for this sample was the same recipe used for the single nanowire heterostructures with the InP layer grown at 410°C.

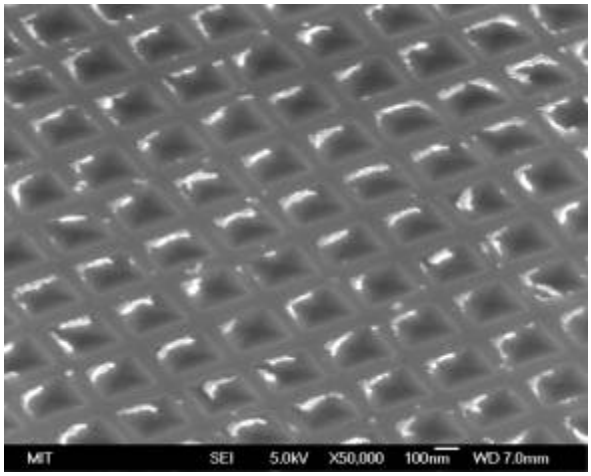


Figure 5.20 Tilted SEM image of a 1nm-thick Au film deposited at 0.1 nm/sec, 350°C, and at a 60 degree incline onto an inverted pyramid array on a Si (100) substrate. This image was taken immediately after the SiN_x protective layer was stripped.

Post nanowire growth inspection by SEM revealed some lateral overgrowth on the wires ([Figure 4.3], Ch.4). However, despite the rough morphology of the wires, the wire to pit ratio is nearly unity and the vast majority of wires appear to be growing from the sidewall facet of interest during Au deposition [Figure 5.21]. The growth recipe in this case has 90 s of TMGa deposited before PH_3 is initiated which likely contributing to some of the wires growing off other sidewall facets. Cross-sectional TEM samples were also made from this sample [Figure 5.22]. As seen in the TEM, the wire growth appears to be epitaxial with the wire growing directly from the center of the sidewall facet.

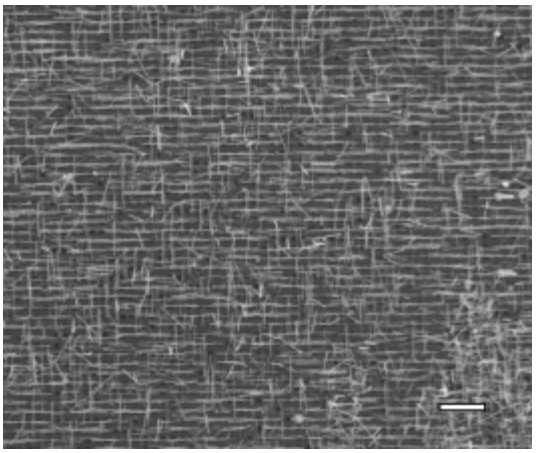
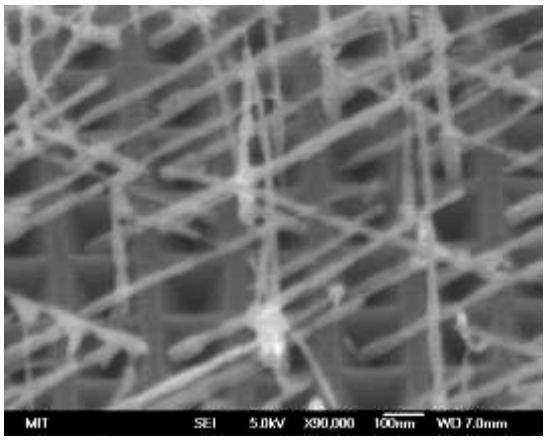
a)  b) 

Figure 5.21 Top-down (a) and tilted (b) SEM images of InP/GaP nanowires grown from the substrate in Figure 5.20. The majority of wires here appear to all be growing in the same <111> direction of the substrate. In addition, the sample appears to have a nearly 1:1 wire:pit ratio despite non-ideal wire heterostructures. The scale bar in a) is 1um.

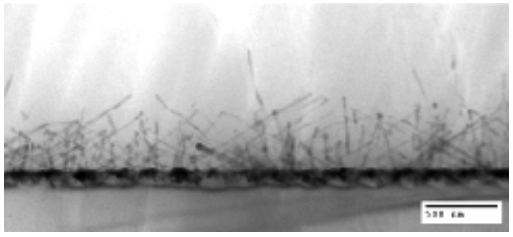
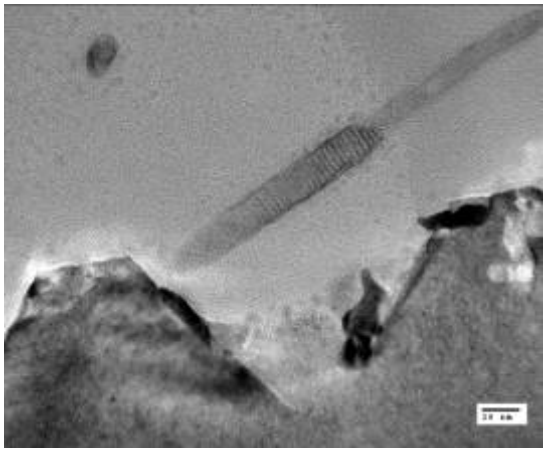
a)  b) 

Figure 5.22 XTEM images of the wires in Figure 5.21

5.2 Silicon-on-insulator Platform

In an attempt to leverage existing Si technologies, we have explored large-scale nanowire integration through the use of silicon-on-insulator (SOI) substrates. These substrates are traditionally used in state of the art CMOS devices because the buried oxide layer underneath the channel allows for superior gate control compared to bulk Si.

This superior gate control leads to both higher performance transistors, as well as lower power consumption by the device.

Our goal in this work is to employ discrete Si nanowires grown by the VLS mechanism in place of lithographically defined channels. This allows us to explore several things simultaneously. First, we can compare VLS-grown Si to lithographically defined and etched Si to understand the role residual Au from the catalyst has on device performance. Secondly, if we can control the number of wires serving as the channel between the MOSFET source and drain, then we can understand the critical aspects of wires running in parallel as these directly relate to current and current density in the device. Lastly, development of VLS silicon wires as the MOSFET channel on an SOI substrate might allow us to explore incorporating III-V wires as the channel of the device, thus giving us a pathway to realizing III-V devices on Si substrates.

The general approach taken to implementing VLS wires on SOI substrates has been demonstrated by several groups [74-76] in addition to our work [Figure 5.23]. First, a specialty SOI wafer is procured where the SOI layer is (110) with respect to the (100) handle wafer. Next, lithography (or some kind of masking) is used to define stripes, pads, or some feature. KOH is then used to etch these features. Because KOH selectively stops on Si {111} planes, perfectly perpendicular sidewall facets are created along the edges of the features. These {111} planes serve as an ideal spot from which to nucleate Si nanowires using the VLS mechanism. The preference for VLS wires to grow in the <111> direction means that these wires should grow horizontally above the buried oxide. If stripes or pads are defined, then we can create Si (or III-V) bridges between the two, laying the foundation for nanowire MOSFET devices.

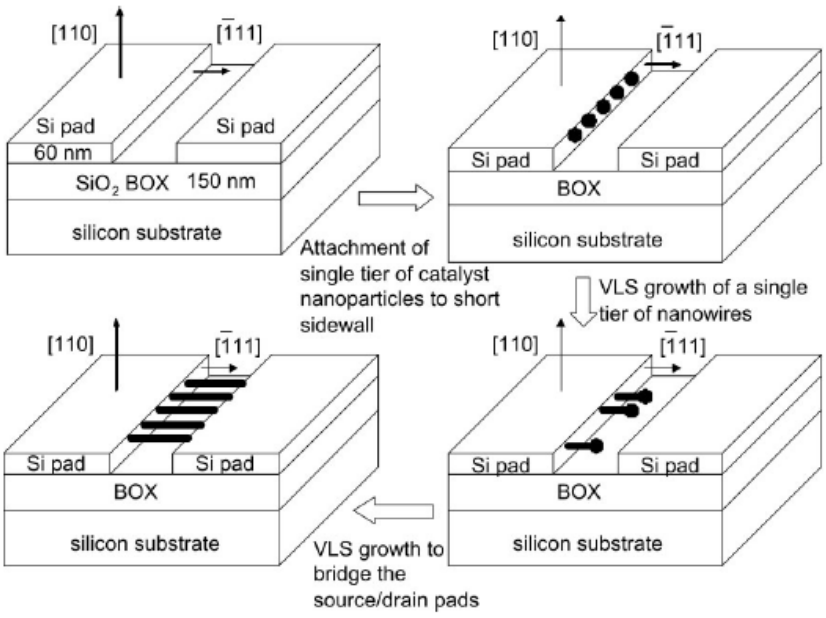


Figure 5.23 Schematic illustration of our SOI process reproduced from Nayfeh, et al [7]

The horizontal "bridging" configuration of these wires might also allow for rapid probing or characterization. In contrast to vertically grown wires, the line-of-sight to the nanowire's long axis permitted by the SOI platform allows for a wide variety of characterization techniques to directly examine the wire's structure and properties. From TEM to PL to mechanical manipulation, the orientation and arrangement of these wires is very appealing to many probing and characterization techniques.

5.2.1 Catalyst deposition and placement

One of the primary challenges in implementing SOI nanowire structures is precise and repeatable placement of metal catalyst particles. Similar to vertical nanowire arrays, catalysts for nanowire growth are pursued here using both Au-colloid nanoparticles, as well as e-beam evaporated Au thin-films. One unique difficulty in working with the SOI

structure is that the underlying BOX layer limits the amount of time the substrate can be exposed to hydrofluoric acid, which is used frequently in this work and is critical for ensuring good epitaxy.

Initial experiments focused on Au-colloids as the charged nature of these particles was thought to be one of the most direct method of implementing site-selectivity to the {111} sidewall facet. Work by Cui, et al.[77] suggested that the use of a positively charged poly-l-lysine adhesion layer would encourage Au-colloid particles to stick to the Si islands instead of the BOX or the SiO_2 layer capping the islands. The lysine adhesion layer is applied by spin-coating onto the post-KOH etched SOI substrate. Au-colloid solutions of various dilutions were then dispersed onto the substrate. As seen in Figure 5.24a the particles appear to adhere preferentially to the exposed Si sidewall facets.

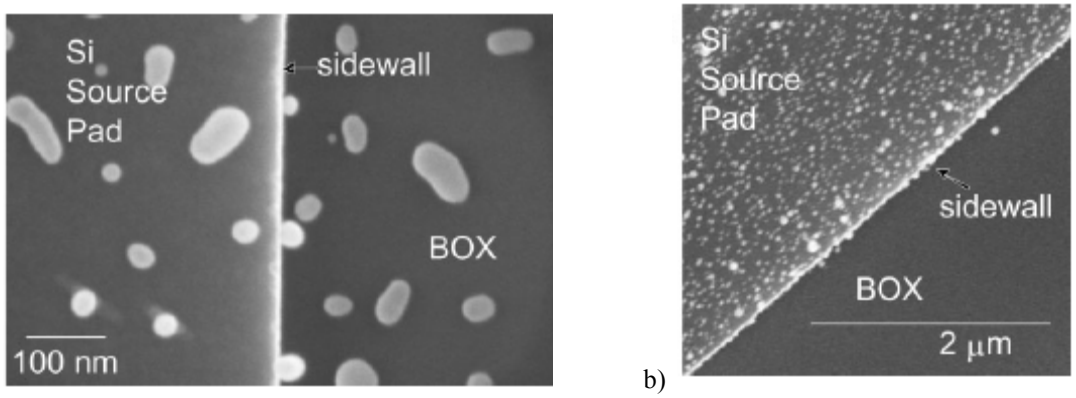


Figure 5.24 Top-down SEM images after Au deposition and rapid thermal annealing (RTA). Some decoration of the sidewalls with Au particles is clearly visible in (a). However, an abundance of particles is also visible on the BOX and on the top of the source pad. b) SEM image after etching in a KI solution to selectively remove unalloyed Au particles, which were in direct contact with SiO_2 during the RTA anneal. Adapted from Nayfeh, et al [7].

While this process was able to distribute Au-colloids selectively to the SOI, no real method for controlling the exact position of the particles could be established. Instead, the Au-colloids randomly distribute themselves onto the sidewall facets as the

solution evaporates. With the exception of varying the colloid dilution, it is nearly impossible to control the placement of the Au particles without secondary alignment through the use of topography, external field, or some other technique which can influence the movement of Au particles while in solution.

E-beam evaporative deposition was also explored as a way of depositing Au catalyst particles on SOI sidewall facets. The main challenge in working with thin films for these structures is that the films are deposited as nearly continuous blanket layers. Thus, a method for selective placement of the Au to the sidewalls must be established following film deposition.

To deposit Au using e-beam evaporation, post KOH-etched SOI substrates were dipped for one minute in dilute 50:1 H_2O:HF to remove the native oxide layer on the sidewalls and immediately loaded into the e-beam evaporator where they were pumped down to ~10^{-9} torr. To induce some sidewall selectivity, the samples were fixed to a tilted chuck such that they would be inclined at 65-degrees relative to traditional deposition stage. 1.3 nm of Au was then deposited at 0.1 nm/s at room temperature.

Following Au deposition, the samples were annealed at 700°C for 90 s to form Au/Si eutectic particles on the Si sidewall facets and to promote the coarsening of Au particles on the BOX surface. A quick Au-etch (potassium iodide based) was performed in an attempt to preferentially remove the Au from the BOX surface while leaving the Au/Si eutectic particles in place. While the Au is expected to etch regardless, the lamellar eutectic structure of Au/Si was thought to provide some etch selectivity with respect to the agglomerated Au particles on the BOX. Post-etch top-down SEM can be seen in Figure 5.24b which clearly shows the selectivity of this etch. The Au remaining on the

top surface of the SOI islands is a result of the protective oxide being removed after multiple hydrofluoric acid exposures. Although this excess Au on the top of the SOI islands will lead to ancillary wire growth, the findings in Chapter 2 suggest that this Au might actually be critical to successful nanowire bridge growth.

5.2.2 Si nanowire growth on SOI

Si nanowire growth on SOI substrates was carried out according to the growth recipes developed in Chapter 2. Despite the eventual success with growing Si nanowires from Au-colloid particles on planar Si substrates, early growths on SOI substrates using these catalyst particles were plagued with growth abnormalities due to lower catalyst densities [Figure 5.25].

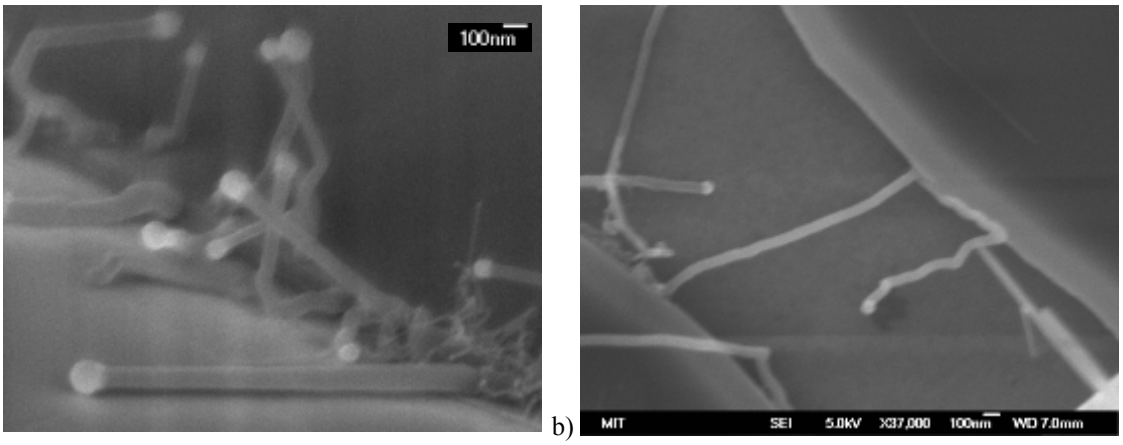


Figure 5.25 Si nanowires grown from SOI substrates using Au-colloid nanoparticles. Wires were grown for both short times (a) and longer times (b) allowing both the examination of the early stages of growth as well as the formation of bridging wires, as in 5.25b.

After Au-colloid deposition on SOI substrates, the samples were loaded into the CVD reactor for nanowire growth. Growth was initiated as mentioned previously with a 10 m anneal at 700°C in H_2. Following the annealing step, the reactor was cooled to

550°C and nanowire growth was carried out according to recipes developed above. As seen in Figure 5.25, nanowire growth from Au colloid particles appears to show little signs of true epitaxy to the Si islands. Despite a number of changes to the pre-growth processing and growth conditions (removal of the poly-l-lysine step, increase in silane flow rate, etc.), little change in wire morphology was seen Figure 5.25b. However, a very small fraction of wires appear to successfully bridge two adjacent SOI pads [Figure 5.25b].

Silicon nanowires grown from e-beam Au particles deposited on SOI substrates appear to produce wires with a much more familiar morphology. However, it is unclear whether or not this is due to the large number of wires all growing simultaneously or due to a cleaner surface between the Au and Si epitaxial surface. Growths on these samples were carried out using the recipes developed and described above which had repeatedly given the best wire morphologies. After growth, the samples were inspected by both top-down SEM and tilted SEM. The early growths were carried out for a limited amount of time in order to see the early stages of nanowire growth before overgrowth from the wires atop the SOI pads or fully bridged wires covered up important wire features as seen in [Figure 5.26].

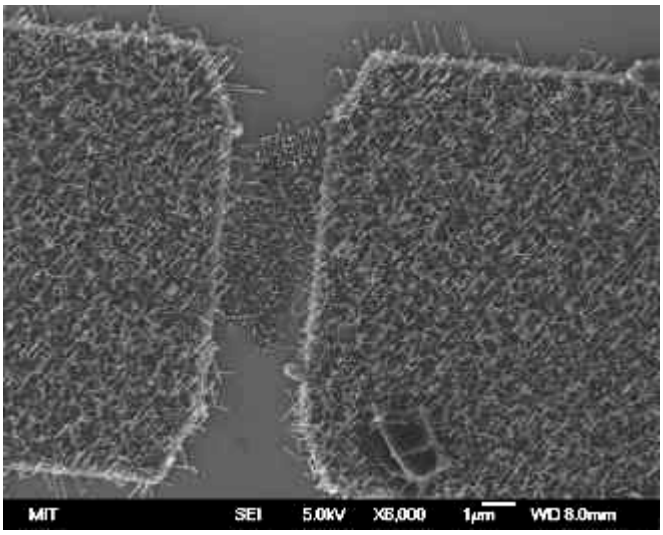
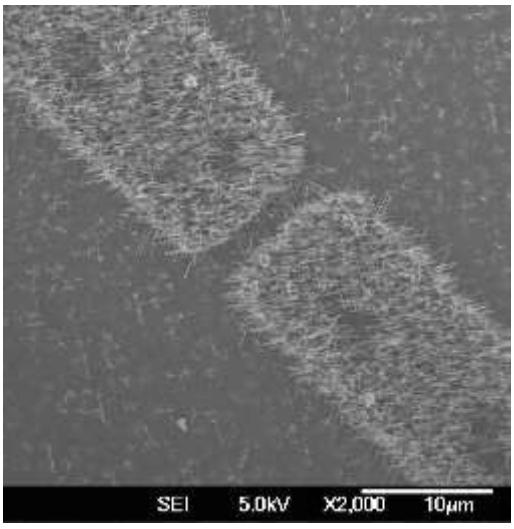


Figure 5.26 Top-down SEM of Si nanowires grown on SOI substrates with the Au catalyst particles deposited by e-beam evaporation. The growth time was limited in this case to allow for direct observation of wires growing from the Si {111} sidewall facets.

After clean, straight, epitaxial growth of Si nanowires to the SOI sidewall facets was established, growths were carried out attempting to completely bridge neighboring SOI islands. As seen in [Figure 5.27], Si nanowires are clearly bridging two SOI pads. In addition, overgrowth from Au on the top of the SOI islands overshadows and obstructs the view of these Si nanowire bridges. From the sides of the SOI islands, Si nanowires can be found extending horizontally over the BOX layer.

a) 

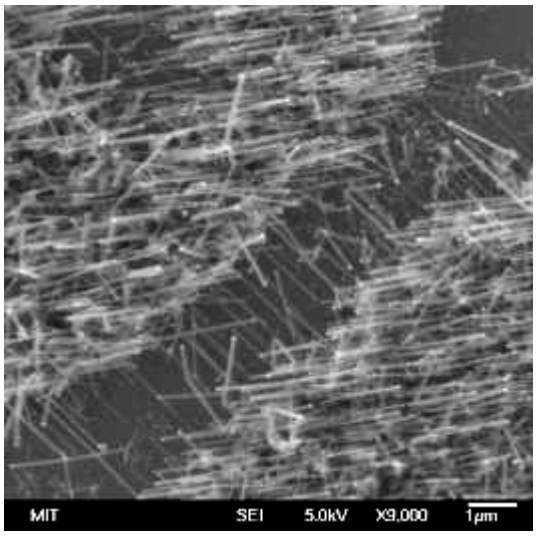
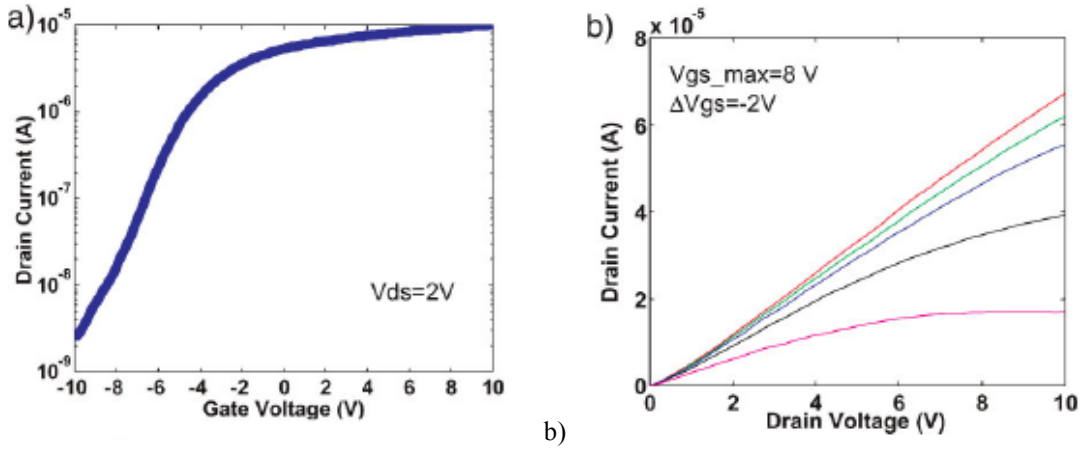
b) 

Figure 5.27 Top-down SEM of Si nanowires grown on SOI substrates with the Au catalyst particles deposited by e-beam evaporation at both low (a) and high (b) magnification. The growth time was increased relative to the sample in Figure 5.26 in an attempt to grow complete bridges between the neighboring Si islands.

Following nanowire growth, the samples were electrically characterized to confirm both pad to pad bridging, as well as MOSFET (metal-oxide semiconductor field effect transistor) behavior using the substrate as the back-gate for the transistor. Electrical measurements revealed n-channel FET characteristics for the VLS nanowire region [Figure 5.28]. The origin of this n-type behavior is likely traced to P or As contamination from the reactor tube as this tube is used for MOCVD growth of GaAs, InP and GaP thin-films and nanowires. A high group V overpressure is generally needed to keep III-V surfaces from decomposing and in this case, no overpressure is present to prevent the trace amounts of III-V compounds on the surface of the graphite susceptor and/or quartz tube walls from decomposing and mixing with the SiH_4 during Si nanowire growth. Nevertheless, the bridging nanowire structures confirm our ability to grow straight, epitaxial, free-standing wires microns in length between adjacent silicon pads and furthermore we are able to demonstrate ohmic contacts at each metallurgical junction along the length of the wire.



a) b)

Figure 5.28 Measured transfer log(IDS) versus VGS and output ID versus VDS (VGS = 8, 6, 4, 2 V) characteristics of a structure similar to that shown in Figure 5. The measurements were performed by using the planar substrate as the backgate and exhibit n-channel transistor characteristics, where the device is off under strong negative gate bias and on under strong positive gate bias. Reproduced from Nayfeh, et al [7].

5.2.3 III-V nanowire growth on SOI substrates

The growth of III-V nanowires on SOI substrates was pursued only after repeatable growth of Si nanowires on SOI substrates had been established. While limited success was achieved using Au-colloid particles as catalysts for Si nanowire growth, all successful III-V nanowire growth on Si (111) substrates utilized e-beam evaporated Au thin-films. Thus, for our work with III-V wires on SOI substrates, we have exclusively explored angled evaporation of Au thin-films on SOI sidewall facets as the method for catalyst deposition.

Successful growth of GaP on Si (111) substrates is detailed in Chapter 3, with the growth initiation step determined to be critical to vertical epitaxy of III-V nanowires on Si substrates. For growth on SOI substrates, a minimal number of parameters were changed between the Si (111) and SOI substrates, such that vertical epitaxy on (111) and

hence horizontal epitaxy on SOI can be achieved. The SOI substrates in this case were chosen from the work in 5.2.2 which had 1.0 nm of Au deposited at 350°C at an 60 deg angle relative to the Au flux direction. These substrates gave the best epitaxy to the sidewall facets with minimal complications from extraneous Au particles which might be on the BOX layer. In addition, the necessity of a 90 sec TMGa burst before PH_3 introduction to ensure high quality epitaxy may deposit Ga droplets on the BOX and Si surfaces which can self catalyze nanowire growth. However, this step is considered critical and therefore was not skipped. The GaP nanowire length was targeted for 800 nm with a V/III ratio of 200 and the growth temperature held constant at 450°C. The gap distances for these SOI substrates is 2 um, the same as used previously. A wire length of 800 nm allows us to investigate the quality of GaP wire epitaxy without complications from wire overgrowth or wires colliding as they approach from opposite sides of the gap.

Post-growth SEM was done to inspect the wire's epitaxy and registry to the SOI substrate [Figure 5.29]. Initial observations note the spotty patches of growth on the BOX layer with wires emanating from these regions without any apparent directional preference. Secondly, wires are observed to be growing from the top of the SOI islands indicating consistent processing problems related to the SOI protective layer. Lastly, from the edges of the SOI pads we see fine comb-like structures indicating successful growth of GaP nanowires 800nm in length from the Si (111) sidewall facets of the SOI substrate. Tilted SEM of these samples [Figure 5.29] reveals the wires are completely free-standing with respect to the BOX layer and grow predominately from one sidewall facet which was preferentially decorated during Au deposition. The wires growing from

the opposite side of the SOI gap are likely the result of Au migration during the pre-growth anneal at 700°C either on the BOX layer or from the top of the SOI pad.

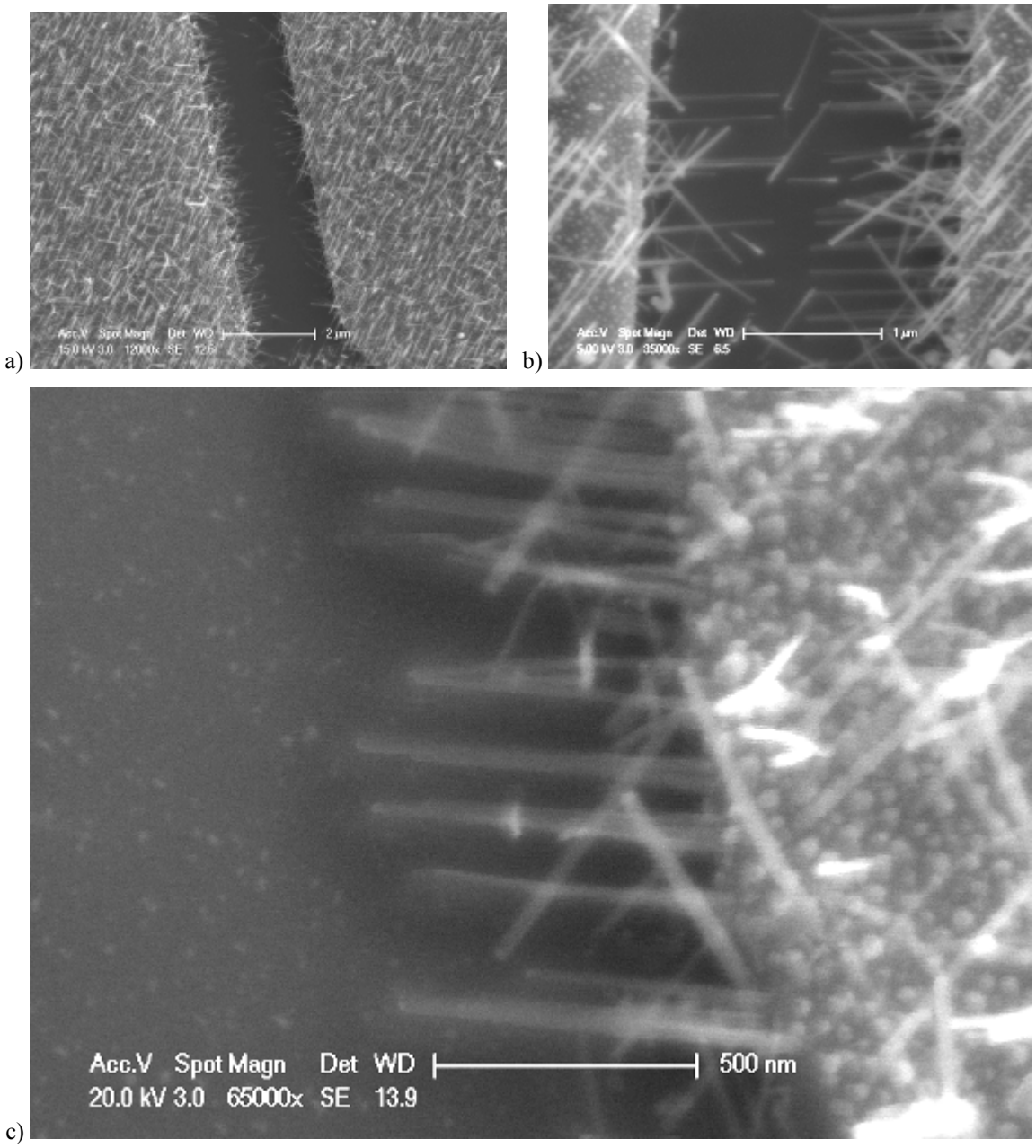


Figure 5.29 GaP nanowires grown on our SOI platform. The wires in a) and b) show both the wire growth on the top of the Si islands as well as horizontal growth from the {111} sidewall facets. The tilted SEM image in c) clearly shows the GaP cantilevers suspended over the BOX layer of the SOI substrate.

6. Summary and Future Work

6.1 Summary

The theme of this work revolved around the ability to understand, control and engineer metal catalyst particles, the substrates on which they are deposited, and subsequent VLS growth from which nanowires are synthesized. While attention in the literature has focused on the attractive mechanical, optical and electrical properties of single crystal semiconductor nanowires, very little is usually said with regard to how these properties might be utilized in future devices. The focus of this work lay primarily in understanding the critical steps in the real world integration of nanowire devices, as these components will ultimately determine how and when nanowire devices might be adopted by the semiconductor industry for use in real systems.

Of the critical components of semiconductor nanowire integration, we focused on four main pieces of catalyst engineering and nanowire growth. The first research thrust involved establishing stable and repeatable growth of Si nanowires on Si (111) substrates. Achieving this allowed us to converge on a 'baseline' set of parameters from which we could systematically change input variables depending on our desired goal. Next we explored a fundamental relationship between catalyst density, VLS growth rate and nanowire morphology. A long-standing complication to realizing our desired Si nanowire bridging structures on SOI substrates was the inability to grow Si nanowires from low-density Au colloid solutions. Only after isolating proximity effects and finding a probable cause were we able to develop a work-around solution in the form of e-beam-deposited thin-films. Our third focus was in determining critical factors which affect the growth of III-V nanowires on Si substrates. We discovered that initiating growth with a group-III precursor led to tremendous improvement in nanowire vertical epitaxy, which is key to

any potential III-V nanowire device integration on Si substrates. Although this improvement did not enable 100% catalyst activation (Au catalysts yielding epitaxial wires), it lay the foundation for future work and also suggests that a different reactor designs (e.g. showerhead), may be key to further improvements in nanowire growth. Lastly, we explored the fundamental growth parameters of axial heterojunction formation and demonstrated growth of $GaP_{(w)}/InP_{(w)}/GaP_{(w)}/GaP$ nanowire heterostructures. The creation of a junction based on alternating group III species is unique in that most III-V nanowire heterostructures created to date involve the modulation of the group V species. Since the group V species is always assumed to decompose at temperatures above ~400°C, the creation of these heterostructures simply requires a change in precursor. By contrast, the creation of our GaP/InP heterostructures required careful adjustments of temperature and gas flow rates to create stable interfaces.

A significant amount of work was also done with respect to substrate engineering for nanowire integration. While this work was useful in that it demonstrates possible pathways to realizing large area arrays and functional nanowire devices, the scope of the work was limited because of the non-existent demand for nanowire devices at this time. Simply put, this work on large area arrays and the SOI platform is a demonstration of potential pathways for future nanowire integration.

6.2 Future Work

Although enthusiasm amongst the nanowire community has died out in the past couple years, due to slow real-world integration and possibly over-sold device

performance properties, possibilities still exist for nanowires (including VLS nanowires) to have an impact in the semiconductor community.

Recent developments in the metal-assisted-etching technique for Si nanowire fabrication have made high-aspect ratio single-crystalline wires nearly ubiquitous and have left little for further development of Si nanowires and ordinary Si nanowire arrays. This solution-based technique gives the ability to synthesize a tremendous number of wires much more cost-effectively and uniformly than the VLS method. However, one benefit (or drawback) of this technique (and any top-down etching technique, for that matter,) is that the wires all have relatively rough sidewalls. By contrast Si nanowires grown by the VLS mechanism have smooth, yet slightly faceted sidewalls. Some work has already been done by Hochbaum, et al.[78], which discusses the differences in phonon transport between nanowires with smooth and rough sidewall surfaces. In the future, this comparison may prove useful in exploring electronic and photonic properties in addition to the thermal properties of Si nanowires.

The development of III-V nanowire heterostructures is still in its relative infancy, although it's unclear as to whether or not they will be able to have an impact on the semiconductor community. The complexity of fabricating useful nanowire heterostructures requires significant investments of both time and money to overcome. While the potential exists to fabricate LEDs or laser diodes of unexplored wavelengths in wires, the highly competitive and fast pace of the industry at-large is likely the biggest hurdle to the realization of these devices.

Regarding the VLS growth method, a great deal of value may exist in this unique method of fabrication which is not actively being explored. The VLS mechanism is

unique in that it allows for the creation of perfect, single crystalline structures at relatively low temperatures using only gas-phase precursors. It then might be possible to create single crystalline composite materials which are otherwise impossible to fabricate. For example, if a small well of high aspect ratio is etched into a Si wafer and Au is deposited at the bottom of this well, the VLS mechanism should allow for the filing of this hole with a different semiconductor material. If we imagine a strip of silicon acting as a waveguide in a photonic device, it may be possible to grow a photon source or photon detector WITHIN the waveguide itself. This would eliminate the need for the secondary laser and detectors which might not be compatible with the photonic structure. A schematic of the process flow described above is shown in Appendix 2. In addition, the processing temperature of the VLS mechanism can extend below 300°C for some materials [79] making it highly attractive to semiconductor devices with small thermal budgets or latter stages of processing where thermal budgets are limited.

Lastly, a great deal of potential lies in the ability to rapidly incorporate nanowires and nanowire devices into existing technologies. One potential pathway, which was not explored in this work, uses Si (110) wafers processed much in the same way as the SOI wafers from Chapter 5. Si or III-V nanowires can be grown across trenches (with {111} sidewall facets), fabricated into the top surface of the substrate. Hydrogen (H_2) could theoretically then be implanted and a SmartCut^{TM} process would transfer nanowire bridges directly onto the BOX layer of the Si handle wafer. A schematic of the process flow described above is shown in Appendix 3.

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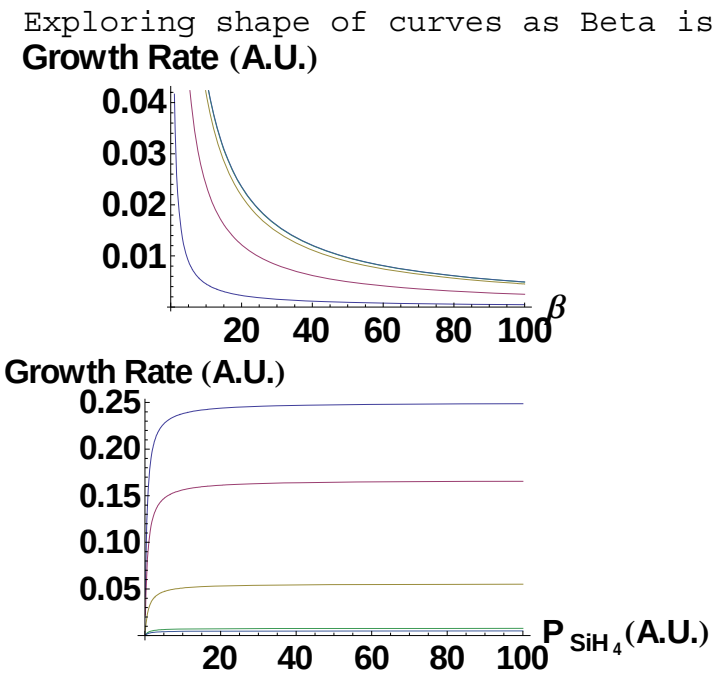
Appendix 1 - Example of Mathematica Code from Chapter 2.2

Mathematica code and plots for Chapter 2.2 – Catalyst Density Issues

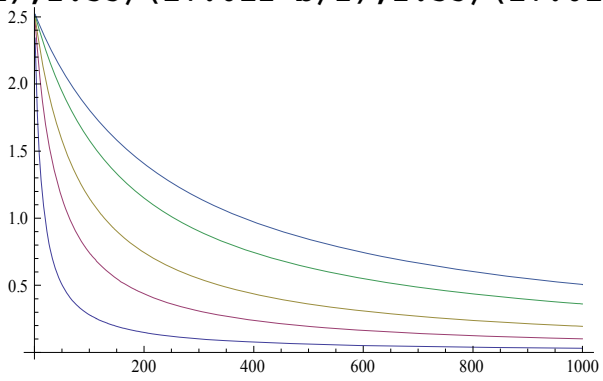
```
"Exploring shape of curves as Beta is varied"


SetOptions[Plot,BaseStyle→{FontFamily→"Trebuchant",FontWeig
ht→"Bold",FontSize→22}];
Plot[{1/(2+A (2+2/.1)),1/(2+A (2+2/1)),1/(2+A
(2+2/10)),1/(2+A (2+2/64)),1/(2+A
(2+2/100))},{A,1,100},AxesLabel→{"β","Growth Rate (A.U.)"}]
Plot[{1/(2+1(2+2/P)),1/(2+2(2+2/P)),1/(2+8(2+2/P)),1/(2+64(2
+2/P)),1/(2+100(2+2/P))},{P,0.1,100},AxesLabel→{"P"Subscrip
t["SiH"Subscript[4]]["A.U."],"Growth Rate (A.U.)"}]
```



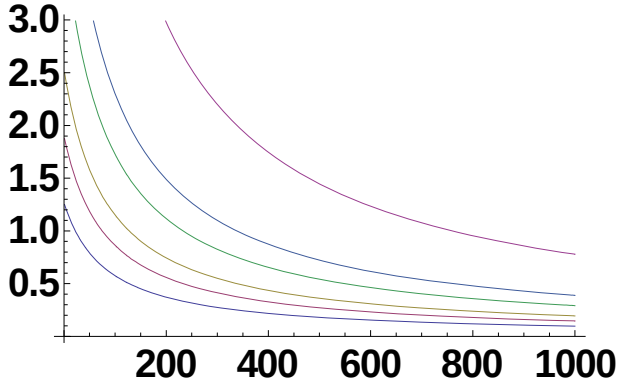
"Modulation of Psih4 and reaction rate constants for varying Beta"

Modulation of Psih4 and reaction rate constants for varying Beta

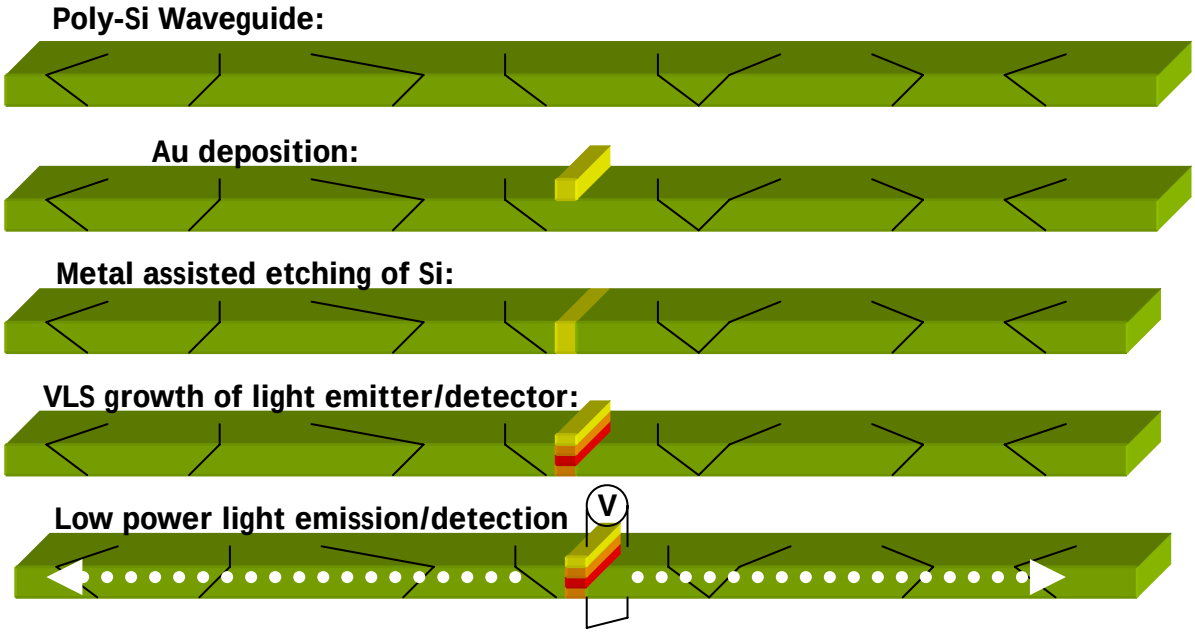
```
Plot[{2.53/(1+.012*b/.15),2.53/(1+.012*b/.5),2.53/(1+.012*b/
1),2.53/(1+.012*b/2),2.53/(1+.012*b/3),}, {b,1,1000}]
```




```
Plot[{(2.53*.5)/(1+.012*b),(2.53*.75)/(1+.012*b),(2.53*1)/(1
+.012*b),(2.53*1.5)/(1+.012*b),(2.53*2)/(1+.012*b),(2.53*4)/
(1+.012*b),}, {b,1,1000}]
```

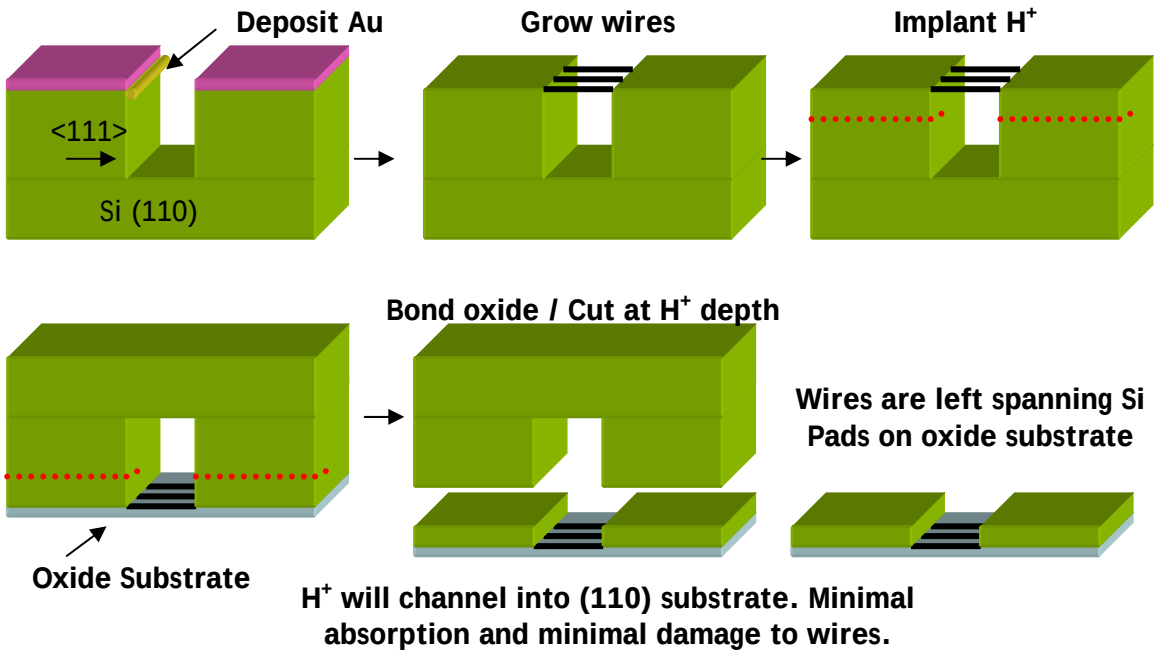


Appendix 2 - Process flow for VLS crystal within a Si waveguide



Above is a proposed process flow for a VLS-grown light emitter or detector within a Poly-Si waveguide structure. This fabrication route could potentially be used to fabricate any number of composite structures where a single crystal of a VLS-grown material is located within the bulk of another material.

Appendix 3 - SmartCut™ process with pre-existing wires



Above is a SmartCut™ process for Si (110) substrate with pre-existing silicon wires spanning across a trench. The process is applicable to placement of III-V, Si, Ge, or any other wire material depending on the application. The final substrate can be oxide, Si, sapphire or any material with a planar surface.