Controlled Growth and Doping of Core-shell GaAs-based Nanowires

by

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University of California, Santa Barbara, 2005

Submitted to the Department of Materials Science and Engineering in
Partial Fulfillment of the Requirements for the Degree of

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ABSTRACT

The use of compound semiconductor heterostructures to create electron confinement has enabled the highest frequency and lowest noise semiconductor electronics in existence. Modern technology uses two-dimensional electron gasses and there is considerable interest to explore one-dimensional electron confinement. This thesis develops the materials science toolkit needed to fabricate, characterize, and control the compositional, structural and electronic properties of core-shell GaAs/AlGaAs nanowires towards studying quasi-one-dimensional confinement and developing high mobility electronics

First, nanowire growth kinetics were studied to optimize nanowire morphology. Variations in nanowire diameter were eliminated by understanding the role Ga adatom diffusion on sidewall deposition and vertical growth was enabled by understanding the importance of Ga and As mass-transport to nanowire nucleation. These results demonstrate that arrays of vertically-aligned GaAs nanowires can be produced. Then, the deposition of epitaxial AlGaAs shells on GaAs nanowires was demonstrated. By reducing the nanowire aerial density the stability of the nanowire geometry was maintained. A variety of analytical electron microscopy techniques confirmed the shell deposition to be uniform, epitaxial, defect-free, and nearly atomic sharp. These results demonstrate that core-shell nanowires possess a core-shell interface free of many of the imperfections that lithographically-defined nanowires possess.

Finally, the adverse effect of the Au seed nanoparticle during n-type doping was identified and n-type doping was achieved via the removal of the Au nanoparticle prior to doping. A combination of energy dispersive X-ray spectroscopy, current-voltage, capacitance-voltage, and Kelvin probe force microscopy demonstrated that if the Au seed nanoparticle is present during the shell deposition, Au diffuses from the seed nanoparticle and creates a rectifying IV behavior. A process was presented to remove the Au nanoparticle prior to shell deposition and was shown to produce uniform n-type doping. The conductivity of GaAs/n-GaAs nanowires was calculated as a function of donor concentration and geometric factors taking into account the effects of Fermi level pinning. The control demonstrated over all of these parameters is sufficient enough for core-shell nanowires to be considered candidates for high mobility electronics.

Thesis Supervisor: Silvija Gradečak
Title: Assistant Professor of Materials Science and Engineering

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Chapter 1. Introduction and Motivation

Nanotechnology, the study and practical application of the unique properties of the nanoscale, holds great promise for improved performance and novel functionality in devices. One device that already utilizes the unique properties of the nanoscale is the high electron mobility transistor. By confining electrons to two dimensions, transistors with increased frequency response and lower noise have been produced and form the foundation of modern mobile telecommunications. Recently demonstrated quasi-one-dimension semiconductor structures, nanowires, may be able to confine electrons to one dimension expanding current understanding of electronic conduction and provide a platform for future high mobility devices. This thesis develops the materials science toolkit needed to fabricate, characterize, and control the compositional, structural and electronic properties of core-shell GaAs/AlGaAs nanowires towards studying quasi-one-dimensional confinement and developing high mobility electronics

1.1 A problem with scientific and technological interest

Beginning with Richard Feynman's vision in 1959 [1] and bolstered by the unprecedented scientific, technological, and societal advancements that the microelectronics industry created, the notion of controlling matter down to the nanometer scale has generated substantial interest from both scientists and technologists. For the scientist, nanostructures allow the study of the atomistic mechanisms controlling materials properties in an unprecedented way. For the engineer, nanostructures present the ultimate building blocks to create devices with improved performance or novel functionality. This convergence of scientific and technological interest has led many to predict that the study of materials at the nanometer scale, commonly referred to as nanotechnology, is the next great frontier of scientific advancement and economic growth [2].

The belief that a field with both scientific and technological interest is a breeding ground for novel technology has precedent. Consider the development of the high electron mobility transistor. Band theory predicts that creating a heterointerface between two materials with different bandgaps creates an energy potential well. This energy well creates electron

confinement, which enhances carrier mobility by suppressing vibrational scattering mechanisms. The belief that epitaxial heterostructures could lead to improved performance electronics generated both scientific and technological interest. When the ability to epitaxially grow thin films of GaAs/AlGaAs with exceptionally low defect densities was developed in the 1960's, scientists were able to experimentally study the effect of reduced dimensionality on electron conduction. They confirmed the presence of two-dimensional free electron gas (2D FEG) and also found that the conduction band offset was able to trap free carriers from a doped layer many tens of nanometers away from the heterointerface. This effect, known as modulation doping [3], enabled a transistor with electron mobility twice that of its doped counterpart [4] creating electronics with higher frequency response and lower noise than any other semiconductor technology.

Nanotechnology may hold the key to continuing advancement in high mobility electronics. To extend the study of reduced dimensionality on electron conduction from 2D to 1D requires the ability to produce quasi one-dimensional single crystalline heterostructures that support transport of charge carriers along their length while maintaining nanoscale effects across their diameter. This structure is referred to as a semiconductor nanowire.

1.2 The semiconductor nanowire for high mobility electronics

There exist two fundamentally different approaches to fabricate nanowires. The first approach to producing nanowires is the top-down approach. Top-down nanowires are produced by carving out a nanowire from a piece of bulk semiconductor material using lithography and etching. This approach utilizes the mature fabrication technology of the semiconductor industry allowing for easier integration with current CMOS technology. However, the top-down approach suffers many of the same materials quality issues inherent to lithography and etching, such as

surface roughness and surface traps. Attempts to create one-dimensional conduction with top-down nanowires failed because the surface roughness inherent to this fabrication method produced additional scattering centers [5]. So while top-down nanowires may be useful for near-term applications in integrated circuits [6], top-down nanowires are unsuitable as a platform for continued advancement in high mobility electronics.

The second approach to producing nanowires is the bottom-up approach. Bottom-up nanowires are produced by inducing single-crystalline semiconductor growth in a nanowire shape. Since the nanowire structure is produced by epitaxial crystal growth, bottom-up nanowires have shown heterointerfaces with the same crystalline quality as MODFETs both perpendicular and parallel to the substrate orientation [7, 8]. As a result, bottom-up nanowires are ideally suited as a platform to study the effect of reduced dimensionality of electron [9, 10] and phonon [11, 12] conduction. There exist various methods to produce bottom-up nanowires such as selective area epitaxy [13] and solution-liquid-solid growth [14], but the most widely studied method is the Au-mediated vapor-liquid-solid (VLS) mechanism [15], which has been shown to produce GaAs nanowires [16, 17] as well as proof-of-concept transistors [18-24], light emitting diodes (LEDs) [25], lasers [26-28], and photovoltaics [29, 30].

Au-mediated VLS nanowire growth utilizes a seed Au nanoparticle as a preferential decomposition site for gallium precursor and creates a driving force for the heterogeneous nucleation of a quasi-one-dimensional single crystal of GaAs. The GaAs/AlGaAs material system is an ideal system to study quasi-one-dimensional conduction since the GaAs/AlGaAs system has only 0.13% misfit enabling heterointerfaces with low defect densities and bulk GaAs exhibits electron mobilities as high as 8500 $cm^2/V\text{-}s$ at room temperature.

1.3 Outline of thesis topic and work

In order to study quasi-one-dimensional conduction in GaAs/AlGaAs nanowires towards high mobility applications, a materials science toolkit is first needed to fabricate an appropriate test structure. A method to produce GaAs nanowires must be demonstrated with control over nanowire morphology and structure. Once GaAs nanowire growth is understood, the deposition of an epitaxial AlGaAs shell deposition must be demonstrated. In order to ensure an epitaxial heterointerface capable of producing quasi-one-dimensional confinement, the structural and core-shell interfacial properties must be characterized and deemed to be free of imperfections that add additional scattering centers. Finally, the electronic properties of core-shell nanowires must be understood and methods devised to provide controllable doping.

Prior to this thesis work had been done to fabricate core-shell GaAs/AlGaAs nanowires, however the morphology of these structures were not controlled, the nanowire structural and core-shell interfacial properties were not known, and n-type doping in GaAs nanowires had not been achieved [31-35]. This thesis studied the growth and properties of core-shell GaAs/AlGaAs nanowire heterostructures and accomplished the following three objectives. First it demonstrated the ability to fabricate uniform vertically-aligned GaAs/AlGaAs nanowires. Second, the structural, compositional, and core-shell interfacial properties of GaAs/AlGaAs nanowires were characterized and shown to be defect-free, uniform and nearly atomically sharp, respectively. Third, the adverse effect of the Au seed nanoparticle was understood and overcome yielding uniform n-type shell doped GaAs nanowires. This work creates the materials science toolkit to use n-type doped core-shell GaAs/AlGaAs nanowires to study reduced dimensionality on electronic conduction and develop core-shell nanowire electronics.

The thesis is organized in six chapters, as follows. Chapter 2 explains in detail the experimental methods and protocols utilized to fabricate and characterize nanowires [36]. The reader is directed to read this chapter if interested in the specific details of the experiments used to prove the results presented in Chapters 3 through 5. Chapter 3 presents studies on fabricating uniform vertically-aligned arrays of GaAs nanowires. The growth kinetics of nanowires were understood and optimized to control nanowire morphology [37]. These results demonstrate that arrays of vertically-align GaAs nanowires can be produced, making them viable candidates for integrated device applications [38]. Chapter 4 presents studies exploring the deposition and characterization of AlGaAs shells on GaAs nanowires. These results demonstrate that the morphology, composition, and crystalline quality of core-shell nanowires can be controlled precisely enough for applications in high mobility electronics [39]. Chapter 5 presents studies on n-type doping via the deposition of a doped shell. These results highlighted the adverse effect of the Au seed nanoparticle and demonstrated that doping can be achieved in radial heterostructures [40]. Finally, Chapter 6 summarizes the results and provides insight and opinions on the future of core-shell GaAs/AlGaAs nanowire research for high mobility applications.

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Chapter 2. Background & Experimental

The purpose of this chapter is to introduce the various experimental techniques used in this thesis. First, the metal-organic chemical vapor deposition technique used for the growth of nanowire is presented, including a discussion of reactor design and reaction chemistry. Second, the electron microscopy techniques used to investigate the structural, compositional, and core-shell interfacial properties core-shell nanowires are presented. This includes a discussion of scanning electron microscopy, transmission electron microscopy, scanning transmission electron microscopy, and energy dispersive X-ray spectroscopy. Finally, the processing and measurement techniques used to investigate the electrical properties of individual nanowires are presented, including a discussion of depositing contacts on individual nanowires, electrical measurement techniques, and Kelvin probe force microscopy.

2.1 Nanowire fabrication

As explained in Chapter 1 this thesis will study the epitaxial growth of bottom-up GaAs/AlGaAs core-shell nanowires. Inducing epitaxial growth in the nanowire geometry has two requirements. First, a substrate preparation process must be developed to only permit nucleation and growth on predefined areas of a substrate. Second, growth conditions must be engineered to create kinetic barriers to crystal growth in all but one direction. Two growth mechanisms have been shown to produce epitaxial nanowires: metal-free selective area epitaxy (SAE) and the metal nanoparticle mediated vapor-liquid-solid (VLS) growth mechanism.

SAE growth of GaAs nanowires was first reported by Fukui in 1991 [13]. The nucleation sites are defined by creating nanoscale pores in a silicon dioxide mask atop a GaAs (111)B substrate using lithography. The sample is then inserted into a metal-organic chemical vapor deposition chamber and grown under carefully designed conditions to promote selective growth in the <111> direction. This method has been shown to produce uniform arrays of GaAs nanowires and is a promising approach for future commercial devices based on GaAs nanowires. However, SAE has not been shown able to produce nanowires with diameters less than 60 nm

[41] due to lack of clear facet formation at low diameters. This would prevent the study of electron conduction at important quantum mechanical length scales.

To achieve smaller diameters, the use of a metal nanoparticle to seed the nanowire growth is required. The VLS mechanism utilizes a metal nanoparticle to act as a gettering source for the gallium and arsenic source material and the solubility limit of GaAs in the metal nanoparticle to induce phase separation of the GaAs from the metal nanoparticle. This method has been shown with CMOS compatible metals such as Mn [42], however nanowire growth experiences kinking and structural defects. On the other hand, VLS nanowires grown using Au as the seed nanoparticle have shown GaAs nanowire growth free of kinking and structural defects [16], making it ideal for the fabrication of a test structure to study lower dimensional conduction. If studies on Au-grown nanowires reveal that GaAs/AlGaAs nanowires may be viable candidates for commercial applications, then nanowire growth using a CMOS-compatible metal or SAE can be explored.

Nanowires have been demonstrated using a variety of growth systems including conventional III-V growth techniques such metal-organic chemical vapor deposition (MOCVD) [13] and molecular beam epitaxy [43]. For thin-film electronics, MBE is known to achieve higher purity films and is commonly used to prototype a device, whereas metal-organic chemical vapor deposition can achieve commercial-scale throughput and is used demonstrate process scalability and compatibility with commercial techniques. It might seem logical to use MBE to produce a test structure to study quasi-1D conduction. However, VLS nanowire growth requires the creation of a kinetic barrier to growth in all but one direction. Since MOCVD growth introduces reagent material in the form of chemical precursors, it allows for selective area epitaxy since metal nanoparticles can act as a preferential decomposition and nucleation site for

precursor. MBE introduces reagent material in elemental form, which means that reagent material can spontaneously react before reaching the Au nanoparticle. Hence MBE is less desirable than MOCVD for VLS nanowire growth because it is less able to provide selective area nucleation and growth.

Fabricating nanowires by the Au mediated VLS mechanism is a three-step process. First GaAs wafers ready for epitaxial growth (epi-ready) were diced into smaller samples. To protect the epi-ready surface of the GaAs, a protective layer of silicon dioxide was deposited by plasma enhanced chemical vapor deposition prior to dicing. Once epi-ready die were prepared gold was deposited to seed nanowire growth and this section describes the three methods utilized to deposit Au nanoparticles: evaporation of a thin film, deposition of colloidal gold nanoparticles, and galvanic reaction on a lithographic template. Once gold seed particles are on the substrate, nanowire growth is conducted by metal-organic chemical vapor deposition (MOCVD). This section presents an overview of MOCVD theory as well as the growth conditions used for core-shell nanowire growth.

2.1.1 Preparation of GaAs substrates for nanoparticle deposition

Prior to further processing, GaAs substrates were coated with a layer of silicon dioxide and polymer to protect the top surface. Wafers were then cut with a die saw into squares and cleaned using solvents and oxygen plasma.

Nanowire growth substrates were prepared from 2" single-side polished GaAs wafers. Both (100) and (111)B substrates were used. GaAs (111)B substrates were used for vertical nanowire growth while GaAs (100) substrates were used since it is the orientation most often used in commercial applications. Small samples of the substrate were cut by use of a diesaw. For dicing, a 500nm thick protective silicon dioxide layer was deposited at 250°C using a Surface

Technology Systems plasma-enhanced chemical vapor deposition reactor. This layer ensured that no organic material or particulate matter came into contact with the polished surface. A second protective layer of PMMA A4 resist, was spin coated at 3000 rpm and soft baked on a hotplate at 180°C for 1.5 min. The final layer thickness was 400 nm. The resist was deposited to ensure the wafers did not cleave during dicing. Individual die were then cut 8mm by 8mm using a Disco Abrasive System Model DAD-2H/6T diesaw.

Prior to nanoparticle deposition, the substrates underwent cleaning to remove any organic contamination. The substrates underwent a 3-solvent cleaning procedure, followed by oxygen plasma cleaning. The 3-solvent clean consisted of ultrasonic cleaning in a bath of acetone (99.5% purity), methyl alcohol (99.8% purity), and then isopropyl alcohol (IPA) (99.5% purity) each for 10 min. After cleaning in isopropyl alcohol, the samples were blown dry in a nitrogen stream (99.9% purity). As a final clean, a Plasmod 4" barrel oxygen plasma cleaner operating at 100 W was used to clean the substrates for 10 min. Nanoparticle deposition took place within 30 min of plasma cleaning.

Substrates to be patterned by electron beam lithography were spin coated with PMMA 950K (1 wt% in anisole) purchased from Microchem, then soft baked on 180°C hotplate for 3 min before exposure. The thickness of the coated PMMA was about 50 nm measured by a KLA-Tencor P10 profilometer. The substrates were exposed on a Raith-150 scanning electron beam lithography (EBL) system at an accelerating voltage of 30 kV with a dot dose of 0.04 $pA \cdot s \cdot cm^{-2}$.

The PMMA was developed in methylisobutylketone (50% in IPA) for 30 s at 21°C and then rinsed in IPA for 30 s. Lift-off was performed by immersing the samples in a 1,2-dichloroethane (DCE) solution [44] followed by 10 min of O_2 plasma cleaning in a Plasmod 4" barrel oxygen plasma cleaner operating at 100W.

2.1.2 Deposition of gold on GaAs substrates

As mentioned above, gold was deposited by one of three methods: colloidal solution, thin film, or electron beam lithography with galvanic displacement. For deposition from colloidal solution, the surfaces of the GaAs growth substrates were made hydrophilic by deposition of poly-*l*-lysine solution (40mL). After 10 min, the substrates were then gently rinsed in stream of deionized (DI) water and dried in a stream of nitrogen (99.9% pure). Next, 40 mL of commercially available colloidal gold solution with diameters ranging from 5 - 100 nm was dropped onto the substrate surface. The colloidal solution was left on the substrate for 5 - 20 min to allow the colloids to precipitate on the substrate surface. The sample was then gently rinsed in stream of DI water and then gently blown dry in a stream of nitrogen gun (99.9% pure). For thin film gold deposition the GaAs growth substrates were inserted into a Sloan 8 kV electron beam evaporator. A thin film of gold was deposited at a background pressure of 3×10^{-6} torr and a deposition rate of 1Å/s and the final film thickness was 0.6 - 3.0 nm.

Finally for the galvanic displacement deposition, the Au^{+3} solutions were prepared by dissolving hydrogen tetrachloroaurate (III) trihydrate into deionized water. Prior to the galvanic reaction, the substrates were immersed in a 2% (v/v) aqueous hydrofluoric acid (HF) solution for 5 min to remove the native oxide layer. The growth substrates were patterned to provide diameter- and position-controlled deposition of Au nanoparticles. The patterned GaAs 111[B] substrates were patterned by EBL and then immersed in Au^{+3} solution of 5×10^{-5} M for reaction time of 20 min.

The reaction is shown in Figure 2-1. Au^{+3} ions diffuse to the surface of the GaAs substrate due to the concentration equilibrium effect. Once the Au^{+3} ions contact the surface directly, a spontaneous reduction occurs due to the difference in the standard reduction potential

(the Au^{+3} /Au pair, 1.42 V versus a normal hydrogen electrode (NHE), is higher than those of Ga^{+3} /Ga, -0.56 V versus NHE, and the As^{+3}/As pairs, 0.234 V versus NHE) [45]. The Au^{+3} ions receive reducing electrons from the bonding electrons of the GaAs substrate (valence band) [46] forming Au nanoparticles and producing gallium and arsenic oxide on the surface of the GaAs substrate. After the reaction, all the samples were thoroughly washed by DI water to remove the residual Au^{+3} ions.

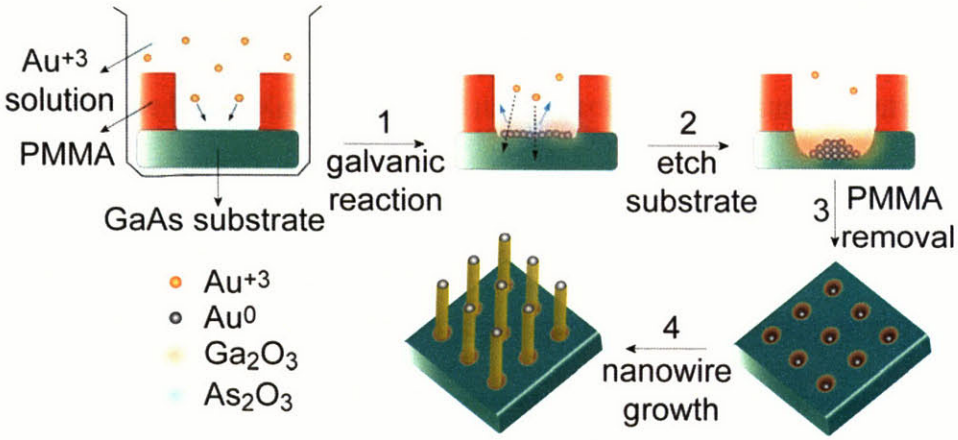


Figure 2-1: The galvanic reaction to deposit Au on GaAs. 1) A patterned substrate is immersed in Au^{+3} solution. 2) Au^{+3} ions replace Ga^{+3} and As^{+3} ions producing oxides. 3) PMMA is removed. 4) GaAs nanowires are grown by MOCVD

2.1.3 Metal-organic chemical vapor deposition

Metal-organic chemical vapor deposition is the commercial standard for epitaxial growth of single crystalline III-V semiconductors. It is highly scalable and capable of very high throughput, unlike molecular beam epitaxy, and offers greater control over composition and purity than other methods such as hydride chemical vapor deposition or liquid phase deposition. Complete descriptions of MOCVD can be found elsewhere [47]. What follows is a general description of MOCVD operation and the key concepts required to understand the work presented in this thesis.

The process operates by introducing the growth elements from the vapor phase within a chemical compound known as a precursor. A combination of thermodynamics and fluid dynamics creates a chemical potential difference that drives the precursors to the growth surface. Once there, a series of decomposition and deposition reactions occur. These reactions break down the precursor yielding the growth element, out-react the decomposition reaction by-products, and drive the crystal growth of the semiconductor material.

A metal-organic chemical vapor deposition reactor consists of two major subsystems: a gas delivery system and a reaction chamber. Each of the two subsystems independently controls one of the two primary process parameters of the growth. The gas delivery controls the partial pressure of the reagent gasses. This correlates directly to the amount of reagent supplied to the reactions. The reaction chamber controls the reaction temperature, which directly affects the reaction rates.

The gas delivery system is a network of valves and mass flow controllers designed to create a controlled mixture of carrier and precursor gasses flowing into the reaction chamber. Each precursor gas supplies an element of the material to be deposited contained within a chemical compound. The carrier gas is a constant flow of gas not containing a deposition material. The carrier gas stabilizes the flow of the gas mixture as the flow rate of the carrier gas is always greater than one hundred times the total flow of the precursors and kept constant throughout the process.

The reaction chamber is a heated chamber where the precursor gasses decompose and deposit material on the samples. In this thesis a horizontal reactor, as shown in Figure 2-2, was used. The chamber and all of its components are made from single crystalline quartz to operate at temperatures up to 800°C. The input gas is delivered from the gas delivery system into the

reactor. The inlet is designed to ensure the flow of gas is laminar and evenly distributed over the chamber. The samples are placed atop a graphite susceptor, which is indirectly heated by infrared lamps. The susceptor, with a much larger thermal mass than the samples', ensures the temperature of the samples stays uniform. The indirect heating ensures that only the graphite susceptor is directly heated while the quartz chamber is not. This is known as a "cold-wall" configuration and is designed to ensure that the precursors primarily diffuse to and decompose on the samples and not on the quartz chamber.

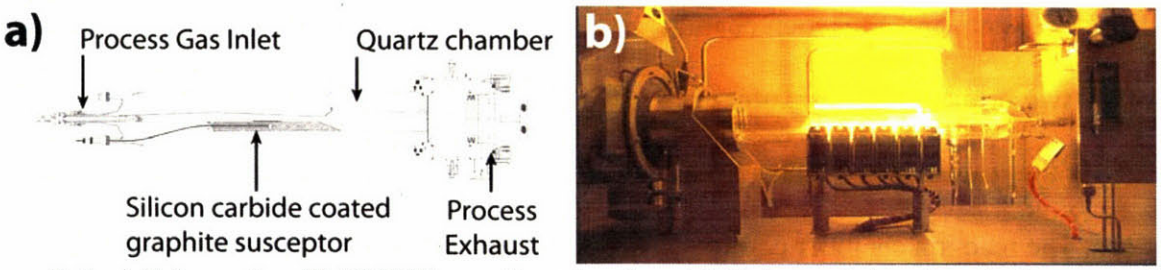


Figure 2-2: a) Schematic of MOCVD reaction chamber. b) Picture of chamber during operation.

The deposition of material by MOCVD occurs via two distinct types of reactions: decomposition and deposition. The reactions for GaAs are shown in Equation (2-1).

$$Ga(CH_3)_3 + AsH_3 \xrightarrow{H_2} Ga + As + 3H + 3CH_3 \longrightarrow GaAs + 3CH_4 \qquad (2\text{-}1)$$

The first reaction is the decomposition of the precursors to yield the desired deposition element. It should be noted that many sub-reactions occur and the decomposition reactions produce by-products that must diffuse away. Both of these facts can affect the growth kinetics of nanowires [48]. The second reaction is the deposition of material; this reaction is simply the elements supplied by the precursor incorporating into the lattice of the substrate. In this thesis, the composition of all deposition materials can be generalized as $Al_xGa_{1-x}As:Si_y$ where x is the percentage of aluminum in the AlGaAs alloy and y is the doping level of silicon in the AlGaAs alloy.

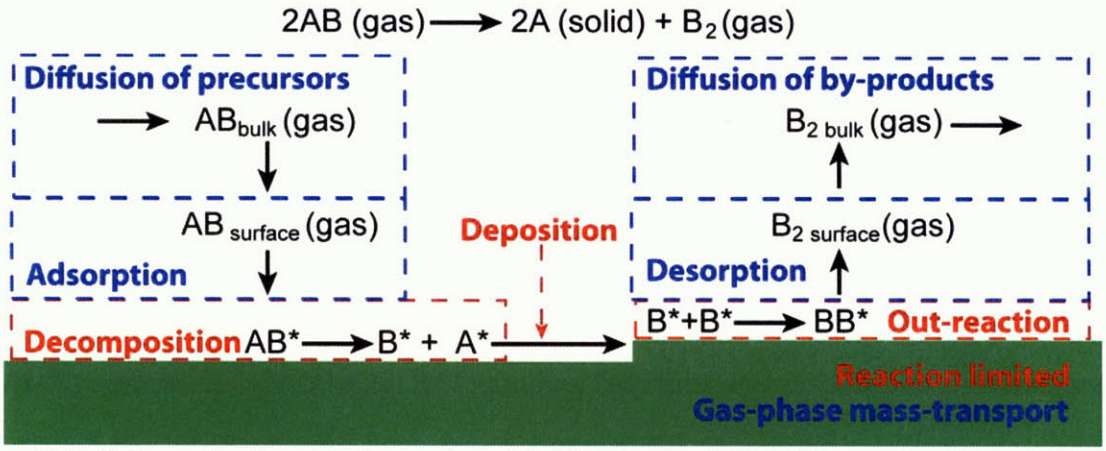


Figure 2-3: Schematic showing the various kinetic steps in MOCVD growth. Steps in blue are categorized as gas-phase mass transport limited steps and steps in red are categorized as kinetically-limited steps. Adapted from [49]

Understanding how growth conditions will effect the composition of the material produced requires an understanding of the reaction kinetics. In general, there are a variety of different kinetic steps that occur in this process, as shown in Figure 2-3. The slowest one is referred to as the "rate-limiting step" and determines the overall reaction rate. These steps can be divided into two categories. The first category is gas-phase mass-transport, which includes the diffusion of precursor to the sample, the adsorption of the precursor onto the surface, the desorption of reaction by-products, and the out-diffusion of reaction by-products. If the rate limiting step is a gas-phase mass-transport step, then the parameters x and y in are determined by the relative flow rates of the precursor gasses and the total growth rate is determine by the total flow rate. The second category of kinetic steps is referred to as reaction steps, which includes precursor decomposition, material deposition, and the out-reaction of by-products. If the rate limiting step is a reaction step, then the parameters x and y as well as the growth rate are determined by the growth temperature. Since the temperature typically determines the crystallinity of the deposition material, it is undesirable to have a reaction step be the rate-

limiting step. MOCVD reactors are typically designed to operate such that a gas-phase mass transport step is the rate-limiting step.

2.1.4 Growth of core-shell nanowires by MOCVD

In this thesis, a Thomas Swan CS6320 atmospheric-pressure cold-walled, horizontal flow metal-organic chemical vapor deposition reactor was utilized. The precursors used for gallium, aluminum, arsenic, and silicon were trimethyl gallium (TMGa), trimethyl aluminium (TMAl), arsine (AsH_3), and silane (SiH_4), respectively. The carrier gas was H_2 at a flow of 15 standard liters per minute.

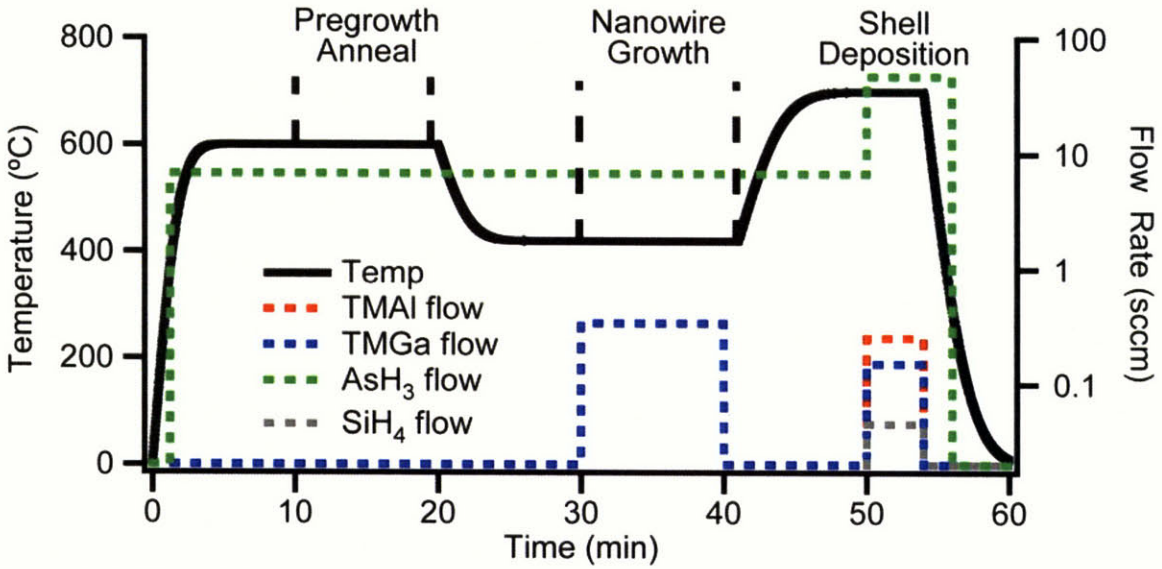


Figure 2-4: Plot of the temperature (left axis) and precursor flow (right axis) profile during a typical core-shell nanowire growth

The temperature and flow profile of a typical core-shell nanowire growth is shown in Figure 2-4. The substrates were heated to 600°C, and annealed in AsH_3 for 10 min to allow the nanoparticles to form, alloy with the GaAs substrate, and create a eutectic Au-Ga liquid. Annealing also removed any organic residue on the surface of the substrate. Flow of AsH_3 was engaged as soon as the sample reached 350°C to prevent desorption of arsenic from the surface

of the GaAs substrate. After annealing, nanowire growth by the vapor-liquid-solid (VLS) mechanism [15] was initiated by cooling the substrate to 420-480°C and introducing TMGa flow. The TMGa flow was maintained for 5 – 20 min, yielding nanowires 5 – 20 μm in length. After NW growth, epitaxial shell deposition by the VS mechanism was initiated heating the substrates to a temperature in the range of 650°C – 750°C and introducing the desired Group III and Group IV precursors. The Group III and IV precursor flow was maintained for 1.5 – 8 min resulting in shells 20 - 200nm thick. Lastly, the substrates were cooled to room temperature. AsH_3 flow was disengaged when the samples were cooled below 350°C to prevent arsenic out-gassing [50].

2.2 Electron microscopy characterization

Electron microscopy (EM) is a standard technique for microstructural and compositional analysis of single-crystalline materials [51]. EM describes a variety of imaging and analysis techniques produced by bombarding a sample with a beam of electrons and collecting the electrons and electromagnetic radiation that are transmitted through, diffracted by, or emitted from the sample. Bombarding a sample with a beam of electrons produces a number of signals that are shown in Figure 2-5.

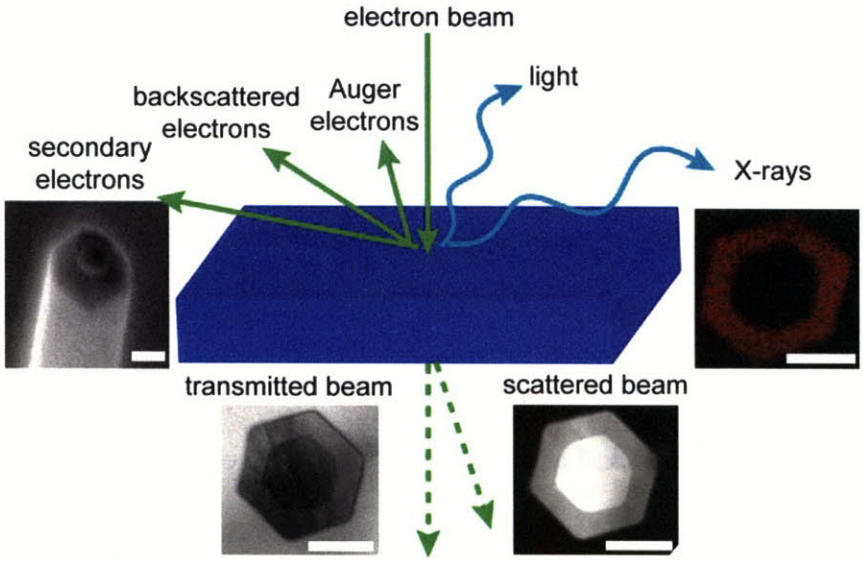


Figure 2-5: Schematic of the various signals that can be produced and collected in an electron microscope. All images have scale bar equal to 100nm. Adapted from [52].

2.2.1 Electron microscopy sample preparation

Scanning electron microscopy (SEM) required no preparation before imaging. Two types of transmission electron microscopy (TEM) were prepared: planview and cross-sectional. Planview samples were used to investigate the properties individual nanowires as they varied across the length of the nanowire. Cross-sectional samples were used to investigate the properties of individual nanowires as they varied within the nanowire cross-section.

Planview samples were prepared, as shown in Figure 2-6, by immersing the as-grown GaAs substrates into 50-100 μL of ethanol in a vial. The volume was set so that there was just enough ethanol to fully immerse the substrate and ensure that the nanowire density in the solution was as high as possible. The vial was immersed into a Crest 175DA ultrasonic cleaner for 10 s. To ensure that the sonication did not break the nanowires, the power of the ultrasonics was kept below 5W. To ensure that nanowires were suspended in the solution. A small droplet of solution was dropped onto a glass slide to verify the presence of nanowires in the suspension. In a Nikon Eclipse LV100 optical microscope, nanowires appear as iridescent rods in dark field

mode at a magnification of 500 or greater. Once optical microscopy confirmed the presence of nanowires in suspension, TEM samples were prepared by depositing a 2 μL droplet of solution onto lacey carbon/formvar TEM grids (Ted Pella 1881-F), then drying in air for 5 min. To increase the density of nanowires on the TEM grid, 5 – 20 droplets of nanowire solution were typically dropped.

Cross-sectional samples were prepared using a three-step process (Figure 2-6): 1) Nanowires were transferred to a plastic coverslip by rubbing the coverslip onto the substrate, 2) The cover slip was embedded in epoxy pre-molds, and 3) The cross-sections were sliced with a diamond knife using a microtome.

Epoxy premolds were made using Eponate-12 epoxy, purchased from Ted Pella. The epoxy was prepared by mixing proprietary Eponate 12 resin (49.9% by mass), double distilled dococenyl succinic anhydride (DDSA) (14.8% by mass), n-methyl anhydride (NMA) (32.6% by mass), and benzyldimethylamine (BDMA) (2.7% by mass) in a fume hood for five min. The epoxy was then poured into a mold so that each mold was half-filled. The molds were baked for 18 hours at 60°C, until solid.

Thermonox plastic coverslips, purchased from Ted Pella, were sliced 2 mm by 1 cm long using a pair of scissors. An as-grown substrate was affixed to a horizontal surface using double-sided carbon tape. Using a pair of tweezers, the coverslip was rubbed across the surface in a uniform direction. Multiple strokes were made to increase the density of nanowires on the coverslip. The coverslips were then placed on top of the epoxy premold, with care taken to assure that the edge of the coverslip was perfectly perpendicular to the edge of the premold. This process ensures that the nanowires, which lie in the plane of the coverslip oriented along the direction of rubbing, will be perpendicular to the diamond blade during microtomy. A second

batch of the epoxy, prepared exactly as the premold was prepared and deposited on top of the coverslips. The samples were cured again for another 18 hours at 60°C.

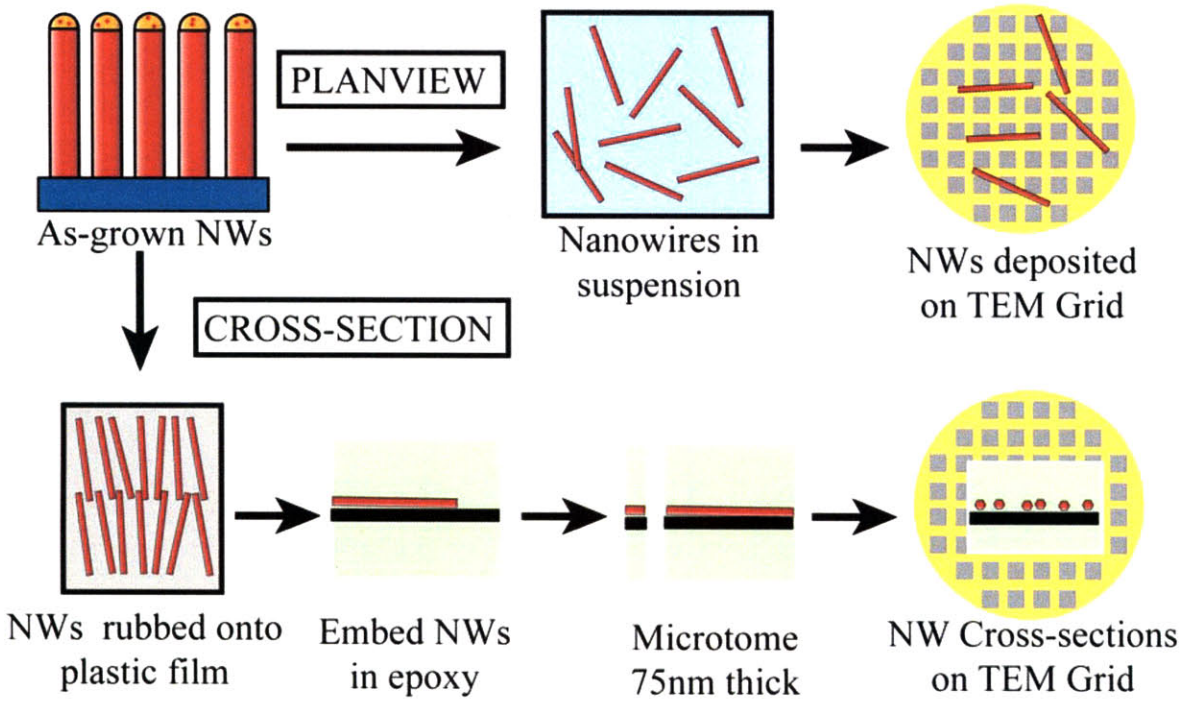


Figure 2-6: Schematic showing the preparation process for plan-view and cross-section nanowire TEM samples.

After curing the samples were trimmed to a trapezoidal shape using either a razor blade or a glass knife. The samples were sliced with a target thickness of 75 nm using a Leica UCT Microtome and a Diatome Histo diamond blade. Slices were transferred onto TEM grids by immersing the TEM grid into the water bath. The end results are microtome slices resting on top of a TEM grid.

2.2.2 Scanning electron microscopy theory and techniques

Scanning electron microscopy (SEM) was utilized for imaging the morphology of as-grown nanowire samples. In a scanning electron microscope, an electron beam accelerated through a voltage of 0.1 – 50 kV is irradiated on a bulk samples. The beam interacts with the

sample producing secondary electrons, which are collected for imaging. SEM was conducted using a JEOL 6320FV SEM with a LaB_6 thermal field emission gun. Imaging was performed at an accelerating voltage of 5 kV using a JEOL ORION charge-coupled device (CCD) camera. The only post-processing of digital images was adjustment of levels and the gamma factor. Under these conditions a maximum resolution less than 2 nm could be achieved[1]. To enable high resolution SEM imaging, all nanowires were grown on degenerately doped substrates.

Nanowire height could be determined from tilted SEM images by measuring the apparent height, $h_{apparent}$, and calculating the real height, h, from $h = h_{apparent}/\sin(\theta)$. The diameter distribution and aerial density of gold nanoparticles was quantitatively determined from SEM images built-in functions of using ImageJ software.

2.2.3 Transmission Electron Microscopy

In transmission electron microscope (TEM) an electron beam is irradiated on a sample less than 500 nm thick. Since the electron beam is accelerated through a voltage of 80 -1000 kV, the impinging electrons are accelerated to a speed of 50 – 95% of the speed of light according to special relativity [53], so the majority of electrons penetrate through the sample. However, some electrons will by scattered by the sample and spatially-dependant variations in electron scattering create the contrast that is used to form TEM images. Images in TEM are formed by a combination of three contrast mechanisms: mass-thickness, diffraction, and phase contrast [51]. These contrast mechanisms and their applications to characterizing nanowires will be discussed. In addition, the electron beam generates X-rays, which can be used for compositional analysis in energy dispersive X-ray spectroscopy. This method will be discussed in the next section.

[1] Measured by Michael Frongillo of the CMSE Electron Microscopy Shared Experimental Facility.

Bright field transmission electron microscopy

Bright-field TEM allows imaging the morphology of samples with a resolution of less than one nanometer. In this mode there are two primary contrast mechanisms: mass-thickness contrast and diffraction contrast. Mass-thickness contrast is based on the principle that the number of electrons scattered by the sample will increase with increasing mass or thickness of the sample. As a result, heavier and thicker regions of the sample will appear darker in bright field imaging.

Crystallographic defects can be imaged using diffraction contrast. Given that electrons exhibit wave-particle duality, the electron can be considered to behave like a wave with a characteristic wavelength of 0.00251 nm at 200 kV. In a perfect crystal with uniform mass and thickness the electron scattering is uniform across the sample, hence the sample appears uniform. However, a structural imperfection such as a dislocation, twin plane or stacking fault will create a diffraction plane for the electrons. The presence of this diffraction plane will create a variation of the scattering profile of the sample, which is referred to as diffraction contrast. Determining the properties of structural defects requires a more in-depth TEM analysis known as "two-beam analysis" and the Howie-Whelan equations [51].

Transmission electron microscopy was performed using a JEOL 2010F field emission TEM operated at 200 kV and equipped with a thermal field emission gun and Gatan Orius CCD camera Model 831 SC600. The only post-processing of digital images was adjustment of levels and the gamma factor. Since nanowire growth was optimized towards eliminating structural defects, the only information required was whether a sample possessed structural defects or not. Therefore, samples were simply imaged by bright-field TEM over a variety of tilt angles and the presence of defects was noted.

High resolution transmission electron microscopy

Resolving atomic columns can be achieved using phase contrast. As the electron beam passes through a sample, interactions with the sample will shift the phases of the electrons' wave functions. If the sample is randomly oriented, these phase shift are sporadic and average themselves out. However, if the specimen is tilted onto an axis of high symmetry such that the beam impinges parallel to the atomic columns (called a zone axis), and then the interaction of the beam with atomic columns will result in uniform phase shifts that correspond with the lattice spacing of the crystal. The net effect is an apparent image of the atomic columns. It should be noted that since there can be many sources of phase contrast in a crystal and the in microscope itself, lattice-resolved images produced by phase-contrast images require comparison with simulation for quantitative interpretation. Nevertheless, phase contrast images can provide useful qualitative information about the crystalline structure without the use of simulation.

Lattice-resolved phase contrast images, commonly referred to as high resolution (HR) images, were imaged in the same microscope and imaging conditions as bright field TEM with the following exceptions. HR images were produced by tilting a sample onto a zone axis using a double-tilted TEM sample holder. For plan view and cross-sectional samples, the <110> and <111> zone axes were used. The zone axis was found by centering the high symmetry nexus of the Kikuchi pattern.

Scanning Transmission Electron Microscopy

Scanning transmission electron microscopy (STEM) is technique complimentary to transmission electron microscopy that allows for the imaging of thin specimens by use of an electron beam transmitting through the sample. The key difference between STEM and TEM is the shape of the beam utilized in the imaging. TEM creates a parallel beam of electrons that

circumscribes the sample. Since different electrons impinge on different parts of the sample, different electrons experience different scattering and phase shifting, which creates the image contrast. In STEM, the electron beam is converged to a single point and scanned over the surface so all electrons impinge at the same point on the sample. As a result, STEM images are directly interpretable, because phase and diffraction do not contribute significantly to image formation. However, in STEM the resolution is determine by the size of the converged beam, which is determined by the spherical aberration of the condenser lenses. Atomic resolution in STEM requires the use of a spherical aberration corrector, whereas atomic resolution can be achieved in HR TEM without the use of aberration correction.

Atomically-resolved STEM enables simultaneous chemical and lattice contrast. Utilizing high angles in dark field STEM increases the chemical contrast. This technique is referred to as high angular annular dark field (HAADF) STEM. It is also more commonly referred to a Z-contrast STEM, due to its acute chemical contrast. Lattice resolved images of nanowire cross-sectional samples were taken using a JEOL 2220FS aberration-corrected microscope with a CEOS aberration corrector at the Oak Ridge National Laboratories. The sample was irradiated by a spread beam for 30 min to desorb any residual hydrocarbons on the sample, then tilted onto the nanowire's <111> zone axis using the corresponding Kikuchi pattern to collect lattice-resolved HAADF STEM images. It should be noted that the cross-sectional method presented involved embedding the nanowires into an insulting material. This makes the sample susceptible to charging effects, particularly at high magnifications where a lot of charge is concentrated on the sample.

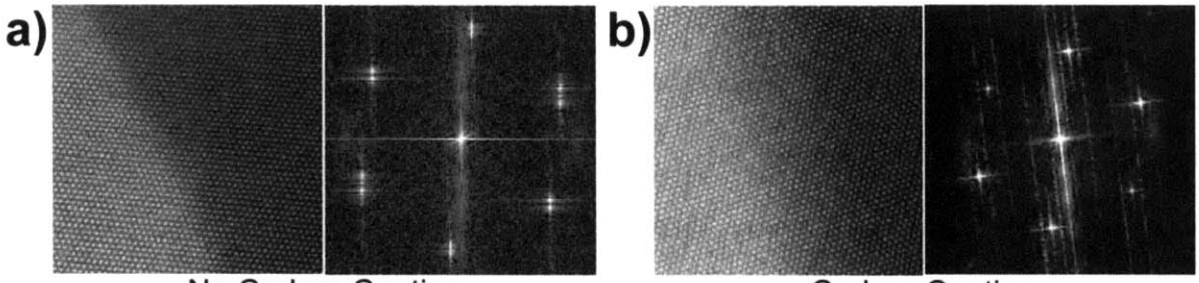


Figure 2-7: HAADF STEM images and corresponding Fourier transforms taken on the same sample a) with and b) without carbon coating.

Images were recorded using less than a 5 s exposure time; however charging still can be seen in the image, particularly the image Fourier transform (FT), as seen in Figure 2-7. After imaging the sample was removed from the microscope and then coated with conductive carbon coating. The samples were reimaged in the same location by the same procedure as above. In these images the Z-contrast is distorted by the carbon coating, but there is no charging, as can be seen in the corresponding FT. Using these two imaging methods, uncoated samples were used to demonstrate the sharp compositional contrast, while FTs of images of the carbon coated samples were used to demonstrate the crystal structure [38].

2.2.4 Energy Dispersive X-Ray Spectroscopy

The X-rays were utilized for compositional analysis in energy dispersive X-ray spectroscopy (EDX). When a high energy electron interacts with the inner core electrons of an atom, inner core electrons get promoted to higher energy states and then relax emitting an X-ray characteristic of the specific transition. Since the emission is caused by the core electrons and not the conduction band electrons, the X-ray emission is determined strictly by atomic percentage and not the bonding states of the material. This makes EDX a robust technique for compositional analysis. Its accuracy is limited the presence of X-rays not generated by the sample. In an EM, when electron lenses redirect the electron beam, the deceleration of the electron beam generates

an X-ray signal referred to as Brehmsstrahlung (braking radiation). As a result of the background radiation from Brehmstrahlung as well as possible X-ray reabsorption in the material, the accuracy of a composition as determined by EDX was taken to be 1-2% depending on imaging conditions. Chemical analysis was performed in a JEOL 2010F field emission TEM and a VG HB603 STEM. Both instruments were operated in STEM mode and equipped by an INCA XSight silicon lithium X-ray detector.

2.3 Nanowire Electrical Characterization

Characterization of the electrical properties required depositing nanowires from ethanol suspension onto pre-patterned grids. Grids were produced as a batch process on 4" silicon wafers using optical lithography and liftoff. Once deposited on grids, the locations of the nanowires were mapped using optical microscopy and custom mapping software. Characterization was conducted by either depositing Ohmic NiGeAu contacts using aligned e-beam lithography and liftoff or the surface potential of the nanowires was probe using Kelvin probe force microscopy.

2.3.1 Preparation of characterization grids

Thermally oxidized (200nm) 4" degenerately doped n-type silicon wafers were used to produce grids. First, the layer of oxide on the back of the wafer, the back-oxide, was removed to ensure a grounding connection to the sample holders for e-beam lithography and electrical characterization. To remove the back-oxide, a layer of AZ5214 photoresist 1μm thick was deposited and cured in a convection oven for 30 min at 90°C. Next, the samples were immersed in a diluted solution of buffered oxide for 10 min to remove the back oxide. After etching, the wafers were inspected by ensuring that their back surfaces were hydrophobic using a DI water jet. The protective resist was removed by immersion in acetone (99.5% purity) for 2 min, followed by a rinse in methyl alcohol (99.8% purity), then IPA (99.5% purity). Samples were

dried in a flow nitrogen (99.9% purity), then cleaned in a Matrix 106 Plasma Asher operating at 1000W for 5 min.

With the back-oxide removed, the grid pattern could be written on the wafers to determine the position of the nanowires. The wafers were coated with AZ5214 resist spin coated at 4000 rpm, then baked in a convection oven for 30 min at 90°C. The wafers were then aligned to a mask and exposed using an EV1 mask aligner for 1.6 s. After initial exposure, the wafers were baked on a metal slab in a 120°C convection oven for 1.5 min. To reverse the image, the wafers were exposed without a mask using an EV1 mask aligner for 60 s. With the lithography complete, the wafers were developed by immersing in MIF 422 developer for 2.5 min, and then being blown dry in a DI water stream. Wafers were inspected using a fluorescent microscope to ensure the pattern was fully developed. If fully developed, the wafers were then inserted into a Temescal FC2000 electron beam evaporator. A stack of Ti/Au (10nm/40nm) was deposited at a base pressure of 3×10^{-6} torr and a deposition rate of 1Å/s. Liftoff occurred in bath of n-methyl pyrrodine heated to 120°C. The wafers were immersed for 20 min or until the metal appeared entire removed. Wafers were then rinsed in a DI water stream and blown dry in a nitrogen stream (99.9% purity).

Once the pattern was defined, the wafers were then diced for individual usage. A protective layer of OCG was applied at 4000 rpm to protect the top surfaces of the wafers. The wafers were then diced into 8 mm x 8 mm die using a Disco Abrasive System Model DAD-2H/6T diesaw. Individual die were screening using optical microscopy. A 4" wafer with 116 die yielded approximately 70 passable die.

2.3.2 Fabrication of contacts on individual nanowires

Nanowires were electrically characterized by depositing nanowires from ethanol suspension onto predefined grids, then defining contacts using electron beam lithography and electron beam evaporation. This process consisted of three distinct steps: nanowires were deposited from solution onto grids, nanowires were mapped onto a pattern file, and contacts were defined and deposited.

Nanowire suspension was prepared by the same process described in section 2.2.1. The desired density of nanowires on the glass droplet was 20 – 100 NWs·mm^{-2}. If the density was low, multiple drops would be deposited. If the density was too high, an in-situ dilution method was utilized. First a droplet of pure ethanol, with volume x was deposited on the sample. Then a droplet of volume y was dropped immediately after. The volumes x and y were chosen to satisfy the following equations:

$$x = (5\ \mu\text{L}) \times \frac{\rho_{\text{desired}}}{\rho_{\text{actual}}}\ ,\ y = (5\ \mu\text{L}) - x \qquad (2\text{-}2)$$

After NW deposition, the samples were gently rinsed in an IPA stream, and then blown dry in a nitrogen stream (99.9% purity). Any residual organic contamination was removed by cleaning in a Plasmod 4" barrel oxygen plasma cleaner operating at 100W for 10 min.[2] Within 30 min of plasma cleaning, a bilayer electron beam resist was spin coated on the sample. First, a layer of PMMA 950K copolymer 11 wt% in ethyl lactate (hereafter referred to as MMA) was spin coated at a speed of 4000 rpm for 55 s to produce a layer 400 nm thick. To prevent the centrifugal force of the spin coating from removing the deposited nanowires, the resist was dynamically dispensed at 500 rpm, then accelerated to 4000 rpm at a ramp speed of 500 rpm per

[2] Published reports suggest this will form a layer of gallium oxide no more than 4nm [54], however the presence of an oxide layer has shown no effect on the contacts. This is likely due to the contact annealing step.

second. To cure the MMA, the sample was baked on a hotplate at 150°C for 1.5 min. Next, PMMA 950K 2% (wt) in anisole, purchased from Microchem, was spin coated at 5000 rpm to produce a layer 90nm thick. To promote uniformity, the resist was dynamically dispensed at 500 rpm. To cure the PMMA, the sample was baked on a hotplate at 180°C for 3 min.

The locations of the nanowires were determined by recording optical images of the nanowires on the grid and the grid markers by optical microscopy at a magnification of 1000. From these images, we can measure the (x,y) positions of the nanowires and calculate the corresponding (u,v) co-ordinated for the lithography design file. The images were then imported into a custom mapping program. This program determined the (u,v) co-ordinates of the ends of the nanowires in relation to the grid markers. The program calculates the co-ordinates of the nanowire using the following equations.

$$\begin{aligned} u_{NW} &= u_{TL} + s \times [(x_{NW} - x_{TL})\cos(\theta) - (y_{NW} - y_{TL})\sin(\theta)] \\ v_{NW} &= v_{TL} + s \times [(x_{NW} - x_{TL})\sin(\theta) + (y_{NW} - y_{TL})\cos(\theta)] \end{aligned} \tag{2-3}$$

Here the (u_{NW},v_{NW}) are the co-ordinates in the CAD file for a point on the nanowire. Typically the locations of both nanowire ends were recorded. The co-ordinates (u_{TL},v_{TL}) are the location of the reference point on the top left grid marker in the image. Similarly the co-ordinates (x_{NW},y_{NW}) and (x_{TL},y_{TL}) are the co-ordinates of the nanowire and the top left grid marker in the image co-ordinate system, typically in units of pixels. The factors s and θ are the scale factor and rotational angle between the image co-ordinate system and the CAD file co-ordinate system, which are calculated as

$$s = \frac{\sqrt{\left((x_{TL} - x_{BR}\right)^2 + \left((y_{TL} - y_{BR}\right)^2}}{50\sqrt{2}\,\mu\text{m}}$$
$$\theta = \arctan\left(\frac{y_{TL} - y_{BR}}{x_{TL} - x_{BR}}\right) - \frac{\pi}{4} \qquad (2\text{-}4)$$

Here, the co-ordinates (x_{BR},y_{BR}) is the location of the reference point on the bottom right grid marker in the image. An example CAD file is included in Appendix A. To define the contacts, the samples were inserted into a Raith 150 electron beam lithography system. The write was conducted using an accelerating voltage of 30 kV and an exposure dose of 150 $\mu A \cdot s \cdot cm^{-2}$. After exposure the samples are developed in methyl-isobutylketone (33% in IPA) for 90 s, and then rinsed in IPA for 30 s to cease development.

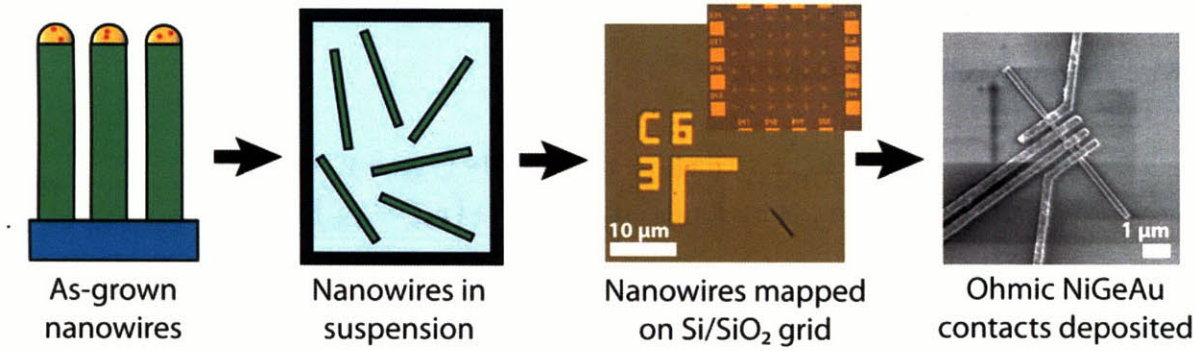


Figure 2-8: Schematic of contacting process showing sonication of nanowires into suspension, deposition of nanowires on the grid, and deposition of contacts.

After acid cleaning, the samples were baked on a hotplate at 105°C for 90 s to desorb any residual water vapor. The samples were immediately inserted into the chamber of a Sloan 8 kV electron beam evaporator with a base pressure less than 3×10^{-6} torr. As an Ohmic contact to GaAs, a Ni/Ge/Au/Ge/Au was deposited. The nickel and germanium layers were deposited at a rate of 1 $Å \cdot s^{-1}$ to a final thickness of 250 Å. The gold layers were deposited at a rate of rate of 2 $Å \cdot s^{-1}$ to a final thickness of 1500 Å. After metal deposition, liftoff was conducted in a bath of n-methyl pyridine (NMP) overnight. Immediately upon removal from the NMP bath, the samples

were rinsed in an acetone, methyl alcohol, IPA, and then nitrogen stream (99.9% purity) until all metal was removed. The contacts were then annealed using an AG Associates Heatpulse 410 rapid thermal annealer (RTA) at 420°C for 30 sec.

2.3.3 Electrical characterization

The completed device was loaded in a Cascade probe station connected to an Agilent 4155c parameter analyzer. Two-probe DC measurements were conducted utilizing an applied voltage sweeped from -2.5 V to 2.5 V with a 25 μV voltage step and a 0.1 ms integration time. In order to accurately determine the resistivity of a sample, one must be able to distinguish the resistance of the specimen (R) from the resistance of the contacts (R_C). This is not possible in a two-point measurement, as evidenced when examining its equivalent circuit. The measured resistance, found by calculating dV/dI, is equal to $R + 2R_C$. From this, it is impossible to distinguish R and R_C since there is only one equation and two variables. Therefore, accurate measurement of resistivity must be carefully designed to eliminate the contacts resistance from the measurement.

Measuring the resistivity of a thin film

In this thesis, the deposition of doped layers was used as a control sample for deposition of a doped shell on the sidewalls of a nanowire. To do so, the sheet resistances of these samples were determined by the accepted Van der Pauw method [55].

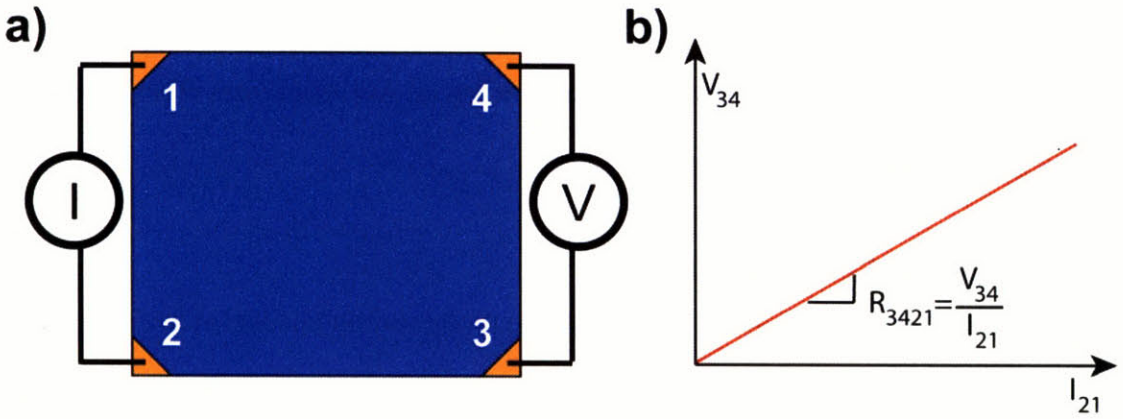


Figure 2-9: a) Schematic of thin film sheet resistance measurement using the Van der Pauw method. b) Expected IV curve

As illustrated in Figure 2-9, four Ohmic NiGeAu contacts were deposited on the corners of the sample. Two contacts were connected to a current source and the other two contacts were connected to a voltage source. Resistance measurements were made by varying the current and, subsequently, measuring the voltage difference. The measured resistance $R_{ABCD} = dV_{AB}/dI_{CD}$. The sample was then rotated 90° and the measurement were retaken. In this case the resistance measured was R_{BCDA}. These two resistances were inserted into the Van der Pauw equation (2-5) and the sheet resistance, R_S, was determined. This equation holds true regardless of the sample shape to provide an accurate determination of the sheet resistance.

$$e^{\frac{-i\pi R_{ABCD}}{R_S}} + e^{\frac{-i\pi R_{BCDA}}{R_S}} = 1 \qquad (2\text{-}5)$$

Measuring the resistivity of a nanowire

The resistance of individual nanowires can be found by measuring the direct current I-V curve of nanowires. However, care must be taken to assure that the measured resistance is that of the sample, and not of the contacts. In this section, different methods for measuring nanowire resistance are presented and their relative accuracy discussed.

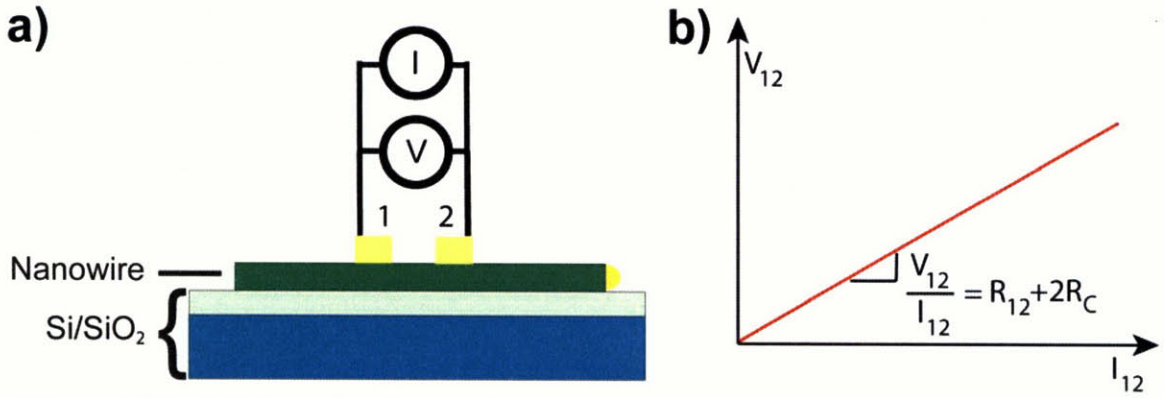


Figure 2-10: a) Schematic of nanowire two-point measurement. b) Expected IV curve and physical meaning of measured resistance

The simplest approach to measuring the resistance of a nanowire is to contact it at two points, introduce a current flow across the wire and measure the resulting voltage, as illustrated in Figure 2-10. However, the measured resistance is not the true resistance of the nanowire. Current flow passes through contact 1, through the nanowire between points 1 and 2, then through contact 2. As a result, the measured voltage includes a voltage change at the contacts equal to $\Delta V = 2I \times R_C$. Therefore the slope of the measured I-V curve is $dV_{12}/dI_{12} = R_{12} + 2R_{12}$.

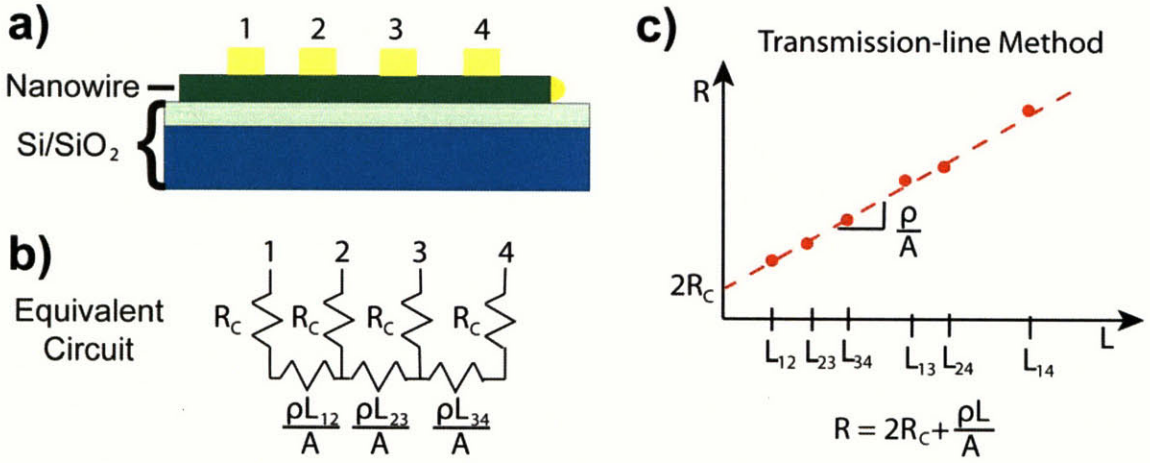


Figure 2-11: Transmission line method measurement on single nanowire. a) Schematic of contacted nanowire. b) Equivalent linear circuit. c) Plot of resistance versus length.

To measure both the nanowire and contact resistances, a more versatile characterization method is needed. Resistances were measured by the transmission-line-method (TLM) [56]

illustrated in Figure 2-11. Consider the circuit diagram for a nanowire with four Ohmic contacts, each with a different separation between the contacts. If the specimen is assumed to have a constant resistance per length, then the resistance is $R_{i,j} = \frac{\rho}{A} L_{i,j}$ and the measured resistance, $R_{measured} = 2R_C + \frac{\rho}{A} L_{i,j}$. When plotted in a resistance versus length graph, the data shows a linear relationship where the y-intercept in $2R_C$ and the slope is the resistance per length, $\frac{\rho}{A}$. On a real measurement this data is plotted and the resistances of the nanowire and contacts are determined by numerical fitting to the formula. The accuracy of this measurement can be increased by measuring across more contacts, thereby providing greater statistical accuracy to the measurement. Since the measurement involves a linear fit of resistance versus length data, a TLM measurement can be performed with as few as three contacts, though it is typically done with four contacts for greater statistical accuracy. This approach is advantageous for nanowire characterization because it can be performed on nanowires where not all contacts function and it can give a qualitative indication of the uniformity of the device. If the fitting of data does not fit the equation well, either the nanowire resistance or contact resistance is non-uniform over the sample.

Capacitance-Voltage Profiling

If a sample is observed to exhibit rectifying behavior, the built-in voltage can be measured by capacitance-voltage (C-V) profiling. C-V profiling utilizes the fact that an energy barrier in the conduction band, which occurs in the presence of a reverse-biased diode must be caused by an electrostatic field. An electrostatic field can only be created by a separation of charge, which exhibits a capacitance in the equivalent circuit.

$$\frac{1}{C^2} \propto (V - V_{bi}) \tag{2-6}$$

In a C-V profile, a reverse-biased diode acts as a parallel-plate capacitor except that the plate separation varies with the applied voltage as modeled by Equation 2-6, which can be derived from the analytical formula of a parallel plate capacitor with thickness equal to that of the voltage-dependant space-charge region thickness [56]. Similar to I-V analysis, a single diode can only be identified in a complex circuit at a point of high impedance, which occurs just below the turn on voltage. Hence, diodes in the equivalent circuit can be identified by plotting the inverse of the measured capacitance squared as a function of applied voltage and looking for linear regions. The built-in voltage may then be determined by plotting estimating the point of infinite capacitance, which occurs at $1/C^2 = 0$.

2.3.4 Kelvin probe force microscopy

By maintaining a conductive scanning probing microscopy (SPM) tip at constant height, Kelvin probe force microscopy (KPFM) is able to measure variations in the surface potential.

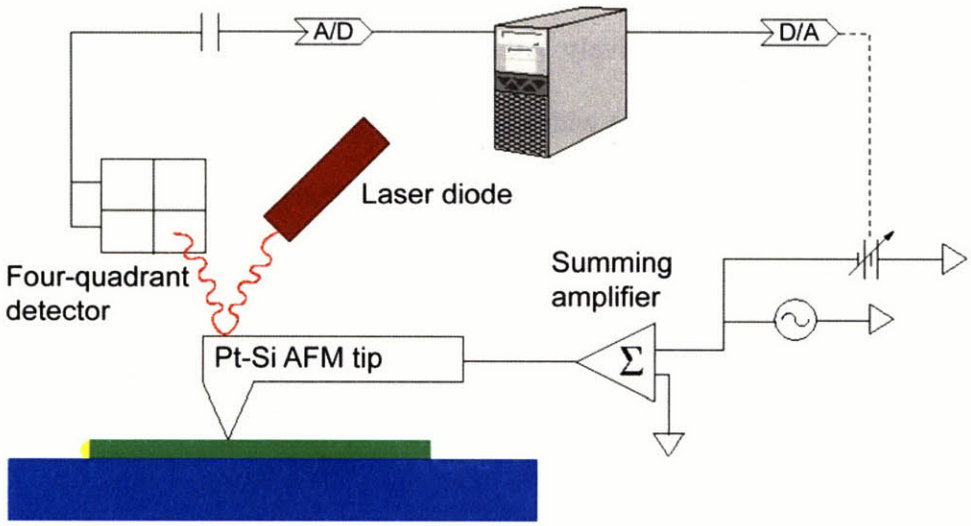


Figure 2-12: Schematic of Kelvin probe force microscopy measurement.

The measurement setup is illustrated in Figure 2-12. The tip height is measured by shining a laser on the tip, detecting the laser with a four-quadrant detector. As the tip height changes, the position of maximum reflected laser intensity also changes, which alters the relative intensities measured by the four quadrants of the detector. Meanwhile the potential at the tip is measured, which is taken to be the surface potential. Kelvin probe measurements were performed in collaboration with postdoctoral scholar Shenqiang Ren. Nanowire samples were prepared by depositing nanowires from ethanol suspension onto Si/SiO_2 grids (section 2.2.1). Samples underwent oxygen plasma treatment for 20 min prior to Kelvin probe force measurement. Samples were not inspected with SEM prior to Kelvin probe force measurement, since SEM inspection creates carbon deposition that affects the surface potential.

Kelvin probe measurements were conducted in a Dimension 3100 SPM with a Nanoscope IV Kelvin controller. The topography and the surface potential were detected simultaneously using the bias modulation technique with two different frequencies for the topography and Kelvin signal, respectively. All measurements were performed in non-contact mode, meaning the tip (Pt coated Si top with a radius less than 25 nm) oscillates with a resonance frequency of the cantilever $\omega_{res} = 68.75$ kHz at a distance of 50 nm above the sample surface. For the Kelvin signal measurements an alternating current bias voltage of 0.5V at the resonance frequency of the cantilever.

Chapter 3. Controlled growth of vertically aligned GaAs nanowire arrays

The purpose of this chapter is to explain the nucleation and growth of GaAs nanowires in order to fabricate a uniform array of vertically-aligned GaAs nanowires. First, the vapor-liquid-solid nanowire growth process is explained and the conditions required to achieve nanowire growth are presented. Next, specific metrics of nanowire morphology are defined and the effects of the different growth parameters on the metrics are explored. An optimal growth temperature of 420°C was found to prevent sidewall deposition and defect formation. A kinetic model was developed, which describes the observed results in the context of Ga adatom concentrations and diffusion. Vertically-aligned nanowires were realized by reducing the group-III flow rate. A kinetic model was developed to explain the flow rate dependence on vertical epitaxy based on Ga and As mass-transport. Finally, the optimized vertical array of GaAs nanowires is presented and possible applications are discussed.

3.1 Demonstration of nanowire growth

In this section, the theory behind the vapor-liquid-solid growth is presented, which includes a brief review of published literature on the growth mechanism. Next, the growth of GaAs nanowires by the vapor-liquid-solid method is demonstrated; however the nanowires are randomly aligned and exhibit variation in their diameter. Next, a set of morphology metrics is introduced and will be used to guide the optimization of GaAs nanowire growth, which will be presented in the remainder of this chapter.

3.1.1 Nanowire growth mechanism

Nanowire growth was conducted using the vapor-liquid-solid mechanism first discovered for Si nanowires in 1964 [15], then shown to apply to GaAs nanowires in 1996 [57].

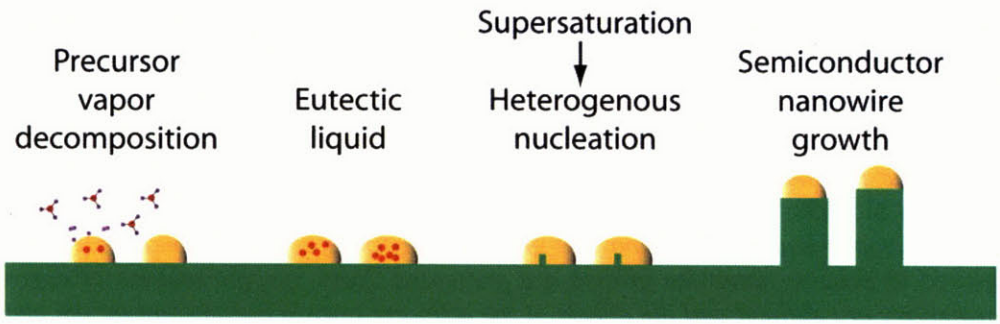


Figure 3-1: Schematic showing the steps of GaAs nanowires by the Au assisted vapor-liquid solid mechanism.

As a first-order approximation, GaAs nanowire growth can be thought of as a four-step process, as illustrated in Figure 3-1. First, the gallium and arsenic arrive from the vapor phase in the form of trimethyl gallium and arsine precursor gasses. The presence of Au locally increases the decomposition rate of the precursors leaving Ga and As adatoms to diffuse on the surface and alloy with the Au nanoparticles. Once the gallium and arsenic reach a critical concentration within the nanoparticles, phase separation between Au and GaAs becomes energetically favorable and a heterogeneous nucleation event occurs at the Au-substrate interface. In equilibrium conditions, this nucleation event would reduce the concentration of Ga and As below the critical level and the phase separation would cease. During the growth, however, Ga and As atoms are continuously being supplied, so the phase separation continues at a steady state until precursor flow is ceased [15].

The enhanced precursor decomposition rate in the presence of Au has been observed by noting that the precursor decomposition rate varies with the aerial density of Au nanoparticles on the substrate [48] and the nucleation of single crystalline material from the Au nanoparticle has been directly observed by *in situ* TEM growth. While the precise mechanism of the increased precursor decomposition rate is not agreed upon, it is widely believed that the nanowire growth

kinetics are dominated by the surface kinetics of Ga precursor and adatoms at the Au nanoparticle surface.

$$r = r_0 e^{-\Delta G/kT} \tag{3-1}$$

Early investigations into the VLS mechanism attributed the increase in decomposition rate to a catalytic effect of the Au nanoparticle on the decomposition reactions of the Ga and As precursors. If the Au were acting as a catalyst, the activation energy for growth, ΔG in equation (3-1), would be reduced. However temperature-dependant studies of nanowire growth rate reveal that there is no reduction in the activation energy for growth [58, 59]. Thus the reaction co-efficient, r_0 in (3-1), must be increased. Researchers speculate that the Au liquid nanoparticle has an increased accommodation probability over the solid GaAs surface, which increases the reaction co-efficient. In other words, the surface kinetics of Ga precursor and adatoms control the kinetics of nanowire growth. That surface kinetics control the growth of nanowires is evidenced by the research on nanowire growth without the use of seed nanoparticles [41].

This model is useful to develop an understanding of the growth process, but it is not complete. To date, there are still many open questions regarding the precise driving force for nanowire heterogeneous growth and considerable effort is being devoted towards developing a unified growth model for III-V nanowires [60]. This thesis will provide a conceptual understanding of the growth process as well as specific details essential to understanding how to control the properties of the nanowires.

3.1.2 Demonstration of GaAs nanowires

According to the growth model proposed in Figure 3-1. The growth of GaAs nanowires should be achieved by depositing nanoparticles gold on a GaAs substrate, then introducing

precursors at a temperature too low for spontaneous decomposition of precursors and deposition of the semiconductor material. This forces the precursors to decompose selectively at the Au nanoparticles and produces GaAs nanowires, consistent with published reports of GaAs nanowire growth [17, 61, 62]. The proper growth conditions for GaAs nanowires can be predicted from the standard enthalpies of formation of the two precursors. For arsine this is 66.4 kJ/mol and for TMGa this is 54.5 kJ/mol [63]. The activation energies of gallium and arsenic precursor suggest that spontaneous growth, which occurs at a rate $r = r_0 e^{-\Delta G/kT}$, can be suppressed below a temperature of 550°C. To test this, nanowire growth was attempted by depositing Au nanoparticles on a substrate, then introducing Ga and As precursor at a temperature below 550°C. Growth samples were prepared by evaporating a film of Au, 6Å thick, on a GaAs substrate, then annealing at 600°C to allow the film to dewet. This method has been shown to produce high densities of epitaxial GaAs nanowires grown by the VLS mechanism [17].

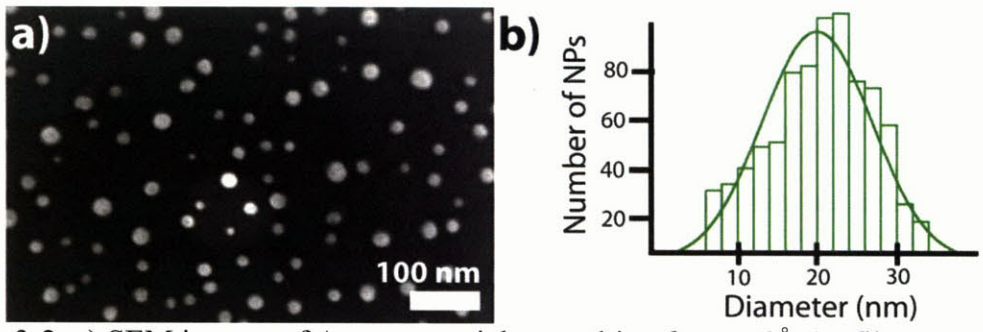


Figure 3-2: a) SEM images of Au nanoparticles resulting from a 6Å Au film annealed at 600C. b) Histogram of nanoparticle diameters, after annealing at 600°C, taken from many SEM images.

Evaporation and annealing produced Au nanoparticles, as shown in Figure 3-2a, uniformly across the substrate. The diameter distribution of these nanoparticles was determined by image analysis, as described in Section 2.2.2. The result, as shown in Figure 3-2b, was a Gaussian distribution of nanoparticles. The average nanoparticles diameter was 20 nm and the standard deviation was 9 nm or 40% of the total diameter.

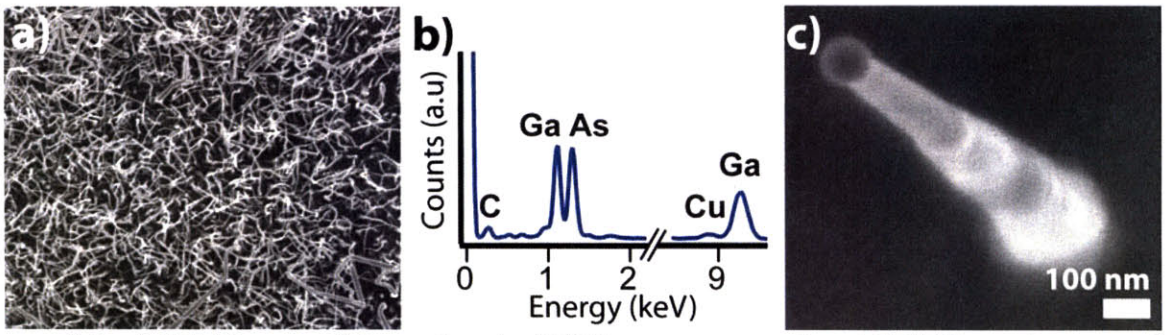
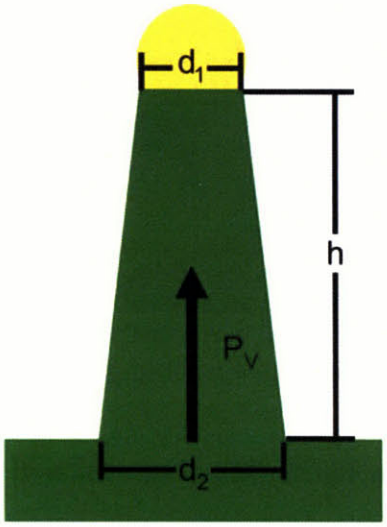


Figure 3-3: a) SEM image of dense forest of VLS-grown nanowires. b) EDX spectrum proving GaAs composition. c) SEM image of a lone nanowire showing tapered morphology.

As shown in Figure 3-3a, nanowire growth can be achieved at 480°C. The composition of the nanowires was confirmed to be GaAs by energy dispersive X-ray spectroscopy in TEM, as shown in Figure 3-3b. However, the nanowires have a random position, diameter, and orientation on the substrate. Inspection of a lone wire, found at a region of low catalyst density and shown in Figure 3-3c, also reveals that the nanowire diameter can vary considerably across the length of the nanowires. While these results demonstrate that the growth of GaAs nanowires is achievable, the properties of each wire are not controlled enough for practical applications. Therefore, a thorough exploration of the effect of different growth parameters on the morphology of GaAs nanowires is necessary to achieve an array of vertically-aligned GaAs nanowires with uniform properties.

3.1.3 Metrics of nanowire morphology

When setting out to control the morphology of GaAs nanowires, it is important to quantify precisely what parameters to control. In this thesis, a set of morphology parameters is defined and methods to control every parameter are presented. The parameters, as illustrated in Figure 3-4, are the nanowire diameter (d), the tapering rate (TR), the probability of vertical nanowire growth (P_V), and the nanowire height (h).



Nanowire Morphology Metrics

Diameter	$\bar{d} \pm \Delta d$	Average and standard deviation of diameters
Tapering Rate	TR	$\frac{\text{Diameter change}}{\text{Nanowire length}} = \frac{d_2 - d_1}{h}$
Vertical Probability	P_V	$\frac{\text{Number of vertical NWs}}{\text{Total number of NWs}}$
Height	$h \pm \Delta h$	Average and standard deviation of heights

Figure 3-4: Schematic of a vertical GaAs nanowire showing the morphology metrics.

Tunablility of diameter with a small standard deviation is desired to ensure that nanowire devices can be designed with little variation in performance. A tapering rate of zero is desired to establish independent control of radial and axial elongation. A vertical probability of 100% is desired to ensure that all fabricated nanowires result in working devices. Similar to the nanowire diameter, tunablility of height with a small standard deviation is desired to ensure that nanowire devices show little variation in performance. However, since some proposed vertical device integration schemes involve removing the top of the nanowire by chemical mechanical planarization [22], variation in nanowire height may not be prohibitive to device development.

3.2 Preparation of Au nanoparticles to control radius and position

The radius of a GaAs nanowire is determined by the diameter of the gold nanoparticles. Therefore, it is important to develop a method that produces gold nanoparticles of uniform and tunable diameter. Dewetting of gold thin films is an inherently stochastic process [64], so diameter control can not be achieved unless the substrate is templated [65]. Instead, a less processing-intensive approach to achieving diameter and position control of nanowires was

explored. In this section, two methods of catalyst preparation are presented: colloidal deposition and galvanic reaction on lithographically patterned substrates. The deposition of Au nanoparticles from colloidal solution produced nanoparticles with controlled diameter, but no control over position. This method was used in the nanowire growth studies presented, since position control is not needed to understand nanowire growth. However, device applications will require position control of the catalyst. Therefore, the deposition of Au nanoparticles using galvanic reaction on substrates patterned by electron beam lithography is also presented. This method produced uniform arrays of GaAs nanowires with precise control over nanowire position and diameter.

3.2.1 Deposition of gold from colloidal solution.

In order to achieve greater uniformity in the nanowire radius, Au colloids were deposited from commercially available Au colloidal solution, as described in Section 2.1.2. The colloidal nanoparticles were purchased[3] with a standard deviation of nanoparticle diameter of less than 1nm. To determine the effect of the pre-growth anneal on the diameter distribution samples were annealed at 600°C for 10 min, imaged by SEM, and the diameter distribution measured by quantitative image analysis.

[3] Colloids purchased from Ted Pella Inc. with measured diameter uniformity.

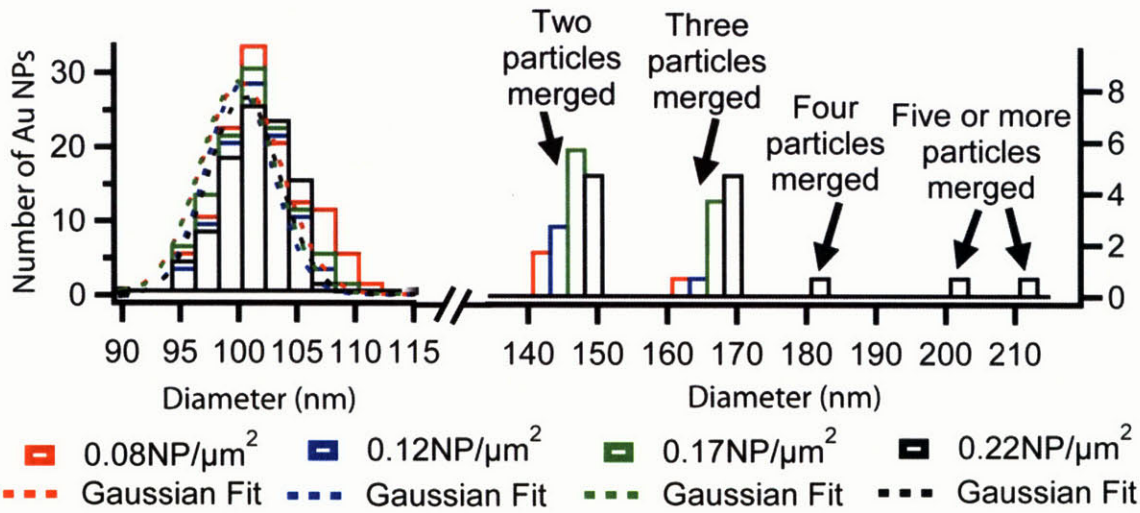


Figure 3-5: Diameter distributions of Au nanoparticles on GaAs 111B substrates at different aerial catalyst densities after annealing at 600°C for 10 min. The left and right histograms show the same data over different diameter ranges.

As seen in Figure 3-5a, the diameter distribution was found to broaden slightly around its original average after annealing, but larger diameter particles also appeared. The broadening of the diameter distribution around the original average can be attributed to either Oswalt ripening [66] or non-uniform particle wetting angles. The larger particles can be attributed to merging with each other, since Au nanoparticles are known to diffuse on semiconductor surfaces [65]. The larger particles appear at discrete diameters corresponding to integer multiples of the original nanoparticle diameters. Moreover, the number of larger particles increased with increasing nanoparticles aerial density, since the average nanoparticle-nanoparticle separation decreases with increasing aerial nanoparticle density. This is uniquely characteristic of nanoparticle surface diffusion and merging.

The extent of the merging can be quantified by defining the merging percentage, *M*, equal to the number of nanoparticles that experienced a merging event divided by the total number of nanoparticles. The merging percentages found for each catalyst density are shown in Table 3-1.

Nanoparticle Aerial Density (NP/μm^2)	Merging percentage
0.08	4.7 %
0.12	6.1%
0.17	16.0%
0.22	19.3%

Table 3-1: The percentage of nanoparticles that undergo a merging event as a function of initial nanoparticle aerial density.

Here a sharp transition occurs between 0.12 and 0.17 NP/μm^2. This suggests that at approximately 0.15 NP/μm^2 the nanoparticles' nearest neighbor separation was equal the surface diffusion length of the nanoparticles. If we assume a uniform distribution of nanoparticles with a nearest neighbor spacing of L, then the area containing one nanoparticle is L^2. Since the area containing a single nanoparticle is also equal to $1/\sigma$, where σ is the nanoparticle aerial density, then $L = \frac{1}{\sqrt{\sigma}} \approx 2.5\mu m$. Reducing the aerial nanoparticle density of nanoparticles gives a uniform distribution of nanoparticles could be achieved, however a method to deposit Au nanoparticles that do not diffuse on the surface is needed to control the position of VLS-grown nanowires.

3.2.2 Au nanoparticle arrays by lithography and galvanic reaction

In collaboration with visiting student Chun-Hao Tseng, a method to create an ordered array of Au nanoparticles that do not diffuse during the pre-growth anneal and seed nanowire growth was developed [38].

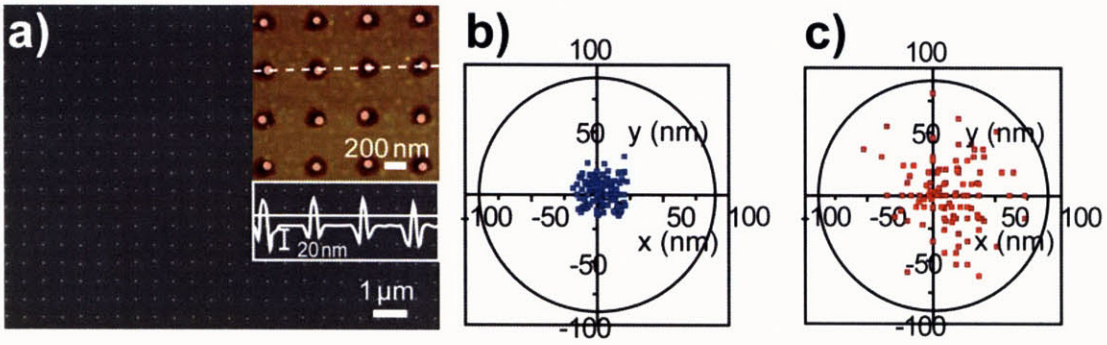


Figure 3-6: a) SEM image of nanoparticles arrays prepared using electron-beam lithography and galvanic reaction after annealing at 600°C for 10 min. Inset is AFM image with height profile. The distribution of nanoparticle positions relative to the mask are shown b) before and c) annealing at 600°C for 10 min.

This method, described in sections 2.1.1 and 2.1.2, consisted of using electron-beam lithography to define a pattern and depositing Au nanoparticles using galvanic reaction. The results are shown in Figure 3-6a. The specific reactions that occur are listed below.

$$4HAuCl_4 + 2GaAs + 6H_2O \rightarrow 4Au^0 + Ga_2O_3 + As_2O_3 + 16HCl$$
$$As_2O_3 + 3H_2O \rightarrow 2H_2AsO_3^- + 2H^+ \quad (3\text{-}2)$$

It should be noted that the reaction creates an etched pit containing the Au nanoparticle and the gallium oxide produced during the galvanic reaction appears in the form of a ring surrounding the Au nanoparticle, as evidenced by the AFM image in Figure 3-6a. Position control can be quantified by plotting the position of the Au nanoparticles relative to their designated position before and after annealing, as shown in Figure 3-6b and c. Nanoparticles were positioned within 50 nm of their designated position before annealing and found to diffuse a net distance of no more than 50 nm after annealing. The reduction of net diffusion length from 2.5 µm to 50 nm can be attributed to either the presence of the etched pit or the inability of the Au nanoparticles to diffuse across the gallium oxide halo. The latter of which is consistent with reports of Au nanoparticle diffusion being prevented on SiO_2 versus Si [67]. Moreover, the

diffusion distance of 50 nm can be reduced by optimizing the galvanic displacement process to produce smaller etched pits. As a result, this method is suitable for producing uniform position-controlled arrays of Au nanoparticles that will not diffuse during the pre-growth anneal required for epitaxial VLS nanowire growth [17].

3.3 Optimizing growth temperature

3.3.1 Preventing variation in nanowire diameter

Variation in GaAs nanowire diameter results from the spontaneous deposition of GaAs on the nanowire sidewalls. Even at temperatures too low for the spontaneous decomposition of precursors, deposition of GaAs material along the sidewall was observed. However, the growth rate along the length was observed to be greater than the growth rate along the sidewall. This suggests that growth conditions can be optimized to kinetically prevent sidewall deposition without simultaneously preventing nanowire growth. Published results on MOCVD growth [47] in thin films suggest that at temperatures below 550°C the rate limiting step is a kinetically-limited step. Hence, growth rates should exhibit a strong dependence on growth temperature. Assuming sidewall deposition is a thermally activated process, decreasing the temperature should decrease the deposition along the sidewall. To test this, nanowires were grown at different temperatures and the growth rate along the sidewall relative to the nanowire was determined.

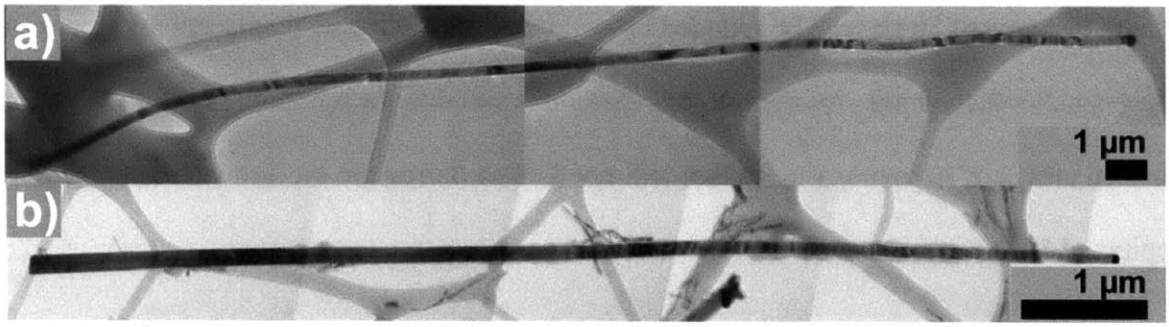


Figure 3-7: TEM images of nanowires grown at 420C (a) and 480C (b).

The results are shown in Figure 3-7. At a temperature of 480°C, significant deposition along the sidewall occurs. This results in the nanowire diameter doubling over a length of 4.6μm. At a temperature of 420°C, however, no significant sidewall deposition is observed, thus confirming the hypothesis that reducing nanowire growth temperature reduces nanowire tapering.

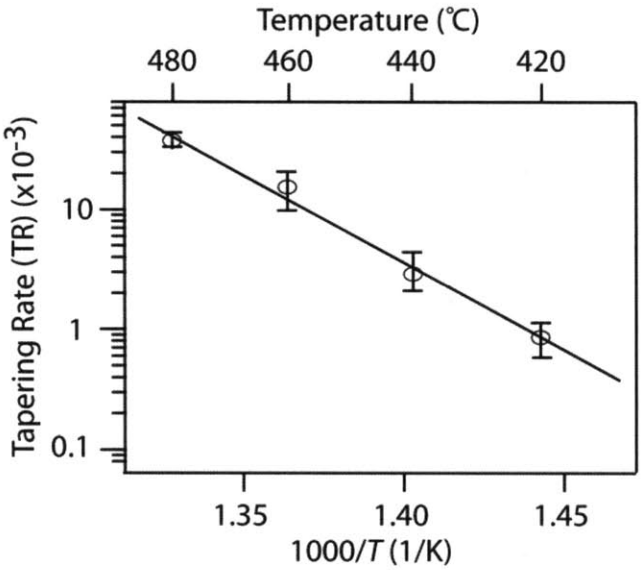


Figure 3-8: The tapering factor plotted on an Arrhenius plot showing shell deposition is a thermally-activated process with activation energy of 56 kcal/mol.

This can be quantified by plotting the tapering rate, as defined in section 4.01.03, versus temperature on an Arrhenius plot. The data exhibits a linear behavior, confirming that shell deposition is a thermally activated process. From Figure 4-9, the activation energy of sidewall

deposition relative to VLS growth is calculated to be 56 kcal/mol. Using this result, sidewall deposition can be minimized by finding an optimal growth temperature that kinetically inhibits shell deposition without hindering the VLS growth of the nanowire. In this case, that temperature is 420°C.

3.3.2 Structural properties of GaAs nanowires

It was also observed that the structural properties of GaAs nanowires varied as a function of temperature.

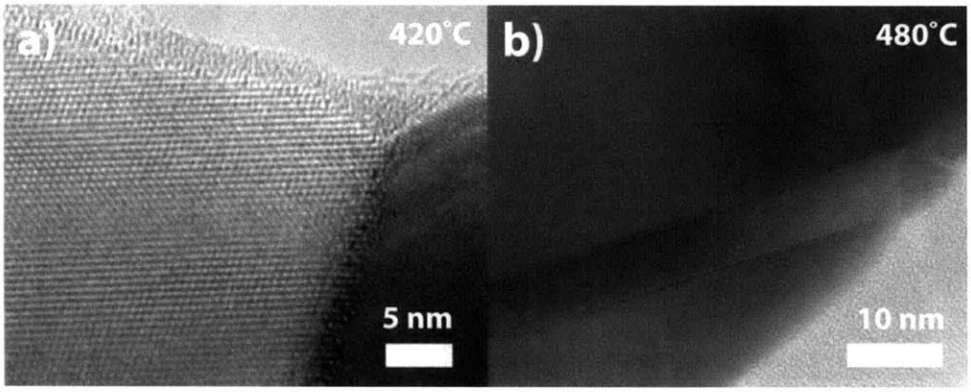


Figure 3-9: High resolution TEM image of a GaAs nanowire grown at 420°C. b) Bright-field TEM image of twinning in a nanowire grown at 480°C.

As shown in Figure 3-9, while nanowires grown at 480°C frequently experience twinning, no structural defects were found in nanowires grown at 420°C. This was confirmed by looking at a statistically significant set of over 50 nanowires, an accepted method to confirm nanowires are free of structural defects [68]. This observation agrees with reports published since [69, 70].

3.3.3 Kinetic model explaining temperature effect

From these results, a kinetic model for the nanowire axial and radial elongation can be developed, which sheds light on why spontaneous growth occurs along the sidewall of the nanowire below 550°C. The nanoparticle acts as a preferential decomposition site for the metal-

organic precursors forming either elemental adatoms [37] or partially decomposed precursor [48]. However, as discussed in section 3.1.1, the rate-limiting kinetic processes are surface kinetics processes at either at the Au-vapor interface or at the Au-GaAs interface [62, 71]. This implies that not all Ga adatoms created by precursor decomposition at the Au surface are able to incorporate into the Au. Hence there exist excess Ga adatoms on the Au surface able to diffuse down the nanowire sidewall and deposit spontaneously [37].

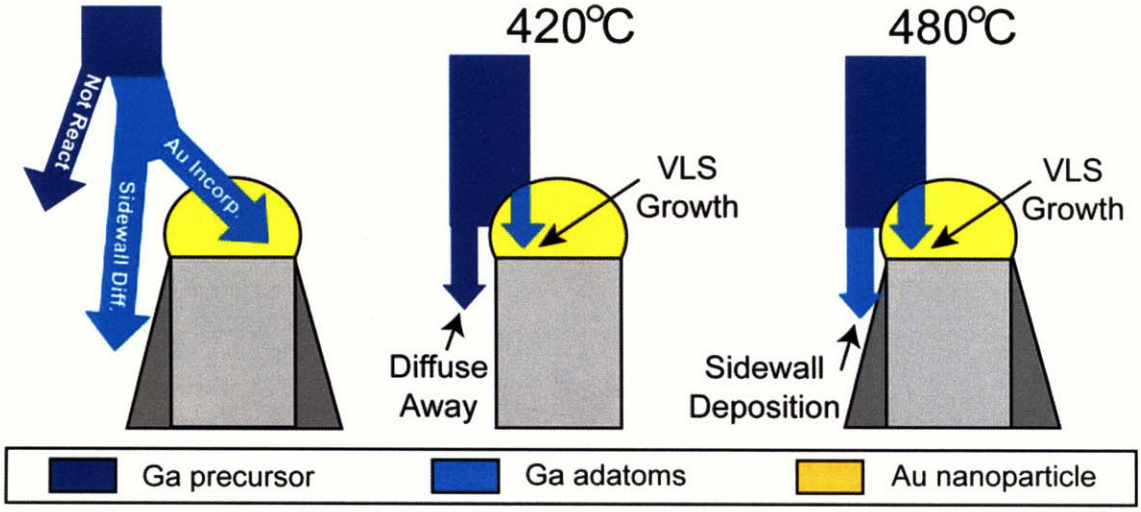


Figure 3-10: Schematic showing the pathways for TMG and how excess Ga adatoms can create radial growth in nanowires.

The effect of temperature on the amount of excess Ga adatoms is illustrated in Figure 3-10. The VS deposition rate can be approximated by the following kinetic growth model. It should be noted that this model does not account for partially decomposed precursors, precursor decomposition away from the Au nanoparticles, or the Gibbs-Thomson effect. The model can be derived by assuming

$$\Gamma_{VS} \propto \frac{\Phi_{\text{excess Ga}}}{A_{\text{sidewall}}} \tag{3-3}$$

Here, Γ_{VS} is the growth rate of sidewall deposition. This is proportional to the flux of excess Ga atoms ($\Phi_{excess\ Ga}$) diffusing down the sidewalls, which determines the volume of the material that will be deposited, divided by the surface area of the nanowire sidewall ($A_{sidewall}$). Expanding further,

$$\Gamma_{VS} = \frac{\Phi_{\text{TMGa decomposition}} - \Phi_{\text{Au incorporation}}}{6RL_{\text{Ga}}} \tag{3-4}$$

Here $\Phi_{TMGa\ decomposition}$ and $\Phi_{Au\ incorporation}$ are the fluxes of Ga adatoms decomposing at the Au surface and incorporating in the Au nanoparticles, respectively. By conservation of mass $\Phi_{TMGa\ decomposition} = \Phi_{Au\ incorporation} + \Phi_{excess\ Ga}$ only if $\Phi_{Au\ incorporation} < \Phi_{TMGa\ decomposition}$. If this is not the case, $\Phi_{excess\ Ga} = 0$. $A_{sidewall}$ is the surface area of sidewall reachable by Ga adatoms. By simple geometry this is the perimeter of the nanowire, which for a hexagon is $6R$, multiplied by the diffusion length of Ga adatoms, L_{Ga}. If the functional form for these adatom fluxes is included, then

$$\Gamma_{VS} \propto \frac{\left(p_{TMGa}\eta_{TMG-Au}(T) - 2\pi R^2 \alpha_{\text{Ga}}(T)\left(p_{TMGa}\eta_{TMG-Au}(T) - p_{eq}\right)\right)}{6RL_{\text{Ga}}} \tag{3-5}$$

Here, the factors p_{TMGa} and $\eta_{TMG\text{-}Au}$ are the partial pressure of trimethyl gallium and the decomposition efficiency of trimethyl gallium at the Au interface, which determine the total amount of Ga adatoms decomposed from precursor. The factor α_{Ga} is the per area incorporation rate of Ga into Au, since it is known that surface incorporation of the Ga is the rate-limiting step to nanowire growth [72] [73]. The results of Figure 3-8 are primarily driven by the precursor decomposition efficiency, $\eta_{TMG\text{-}Au}$, since it is the most sensitive to changes in temperature [72] [73]. Recent work estimating the decomposition efficiency of TMGa, $\eta_{TMG\text{-}Au}$, at Au seed particles suggests that at 480°C TMG decomposition may be 5-10 times as efficient [69]. Hence,

at 480°C there exists an overabundance of Ga adatoms unable to incorporate into the Au, which leads to sidewall deposition. At 420°C, however, there is little to no overabundance of Ga adatoms, and hence no spontaneous sidewall deposition.

Moreover, this model explains the presence of defects at increased temperature. At 480°C, the decomposition of precursor at the Au seed particle is very efficient. Since $\Phi_{Ga} = 2\pi R^2 \alpha_{\mathrm{Ga}} \left(p_{Ga} - p_{eq}\right)$, the increased decomposition creates excess Ga adatoms, driving the incorporation of Ga atoms into the Au and thereby accelerating the growth rate of the nanowire. In this case, the growth occurs so rapidly that the Ga and As adatoms do not have sufficient time to find a proper lattice site. Hence, structural defects form. At 420°C, however, there are not excess Ga adatoms to accelerate nanowire growth. The reaction occurs slowly enough for Ga and As atoms to find the proper lattice sites without forming defects.

In this model, one also expects the V/III ratio to influence the tapering rate since the presence of arsine is known to enhance the decomposition of metal-organic precursors [74]. This effect has been observed in ternary alloy nanowires [37] and in selective area epitaxial growth of GaAs nanowires [35], however variation of V/III ratio did not have an observable effect on tapering. This is likely the result of growth conditions chosen such that $\Phi_{Au\ incorporation} > \Phi_{TMGa\ decomposition}$. A V/III ratio of 20 was used during the optimization of the growth temperature.

In summary, reducing the growth temperature prevents the spontaneous deposition of GaAs along the nanowire sidewalls by preventing the creation of excess Ga adatoms, which diffuse along and spontaneously deposit on the nanowire sidewalls. Reducing the temperature also enables nanowire growth free of structural defects by allowing the Ga and As atoms enough time to find a proper lattice site. The optimal growth temperature is 420°C. This temperature is

low enough to provide a kinetic hindrance to sidewall deposition while high enough to drive defect-free VLS nanowire growth.

3.4 Maximizing probability of vertical growth

In a practical application, one non-vertical wire could mean the difference between a working device and a short-circuited device. Therefore, it is necessary to develop an acute understanding of the nucleation of GaAs nanowires and design growth conditions uniquely tailored to promote vertical growth. Without such an understanding, large scale integration of nanowires for practical applications can not be considered. In this section, the effects of substrate orientation and group-III flow rate on vertical probability, P_V, are explored. Then, a kinetic model explaining the conditions needed for vertical growth is presented.

3.4.1 Effect of substrate orientation

In order to achieve vertical nanowire growth, the effect of substrate orientation on vertical growth was investigated. For comparison nanowires were grown on both GaAs (100) and (111)B substrates.

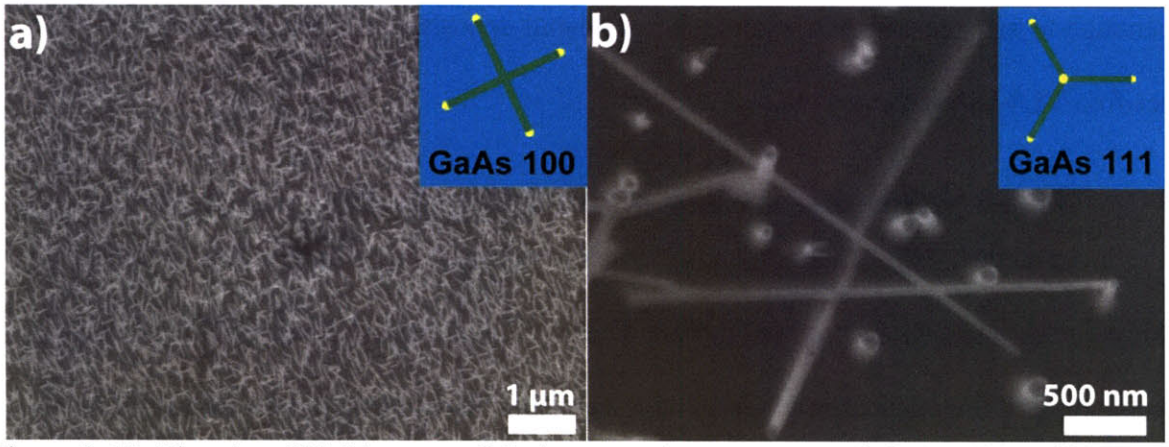


Figure 3-11: Planview SEM images of GaAs nanowires grown on a) GaAs 100 and b) GaAs 111B substrates with observed texturing in inset.

The results, shown in Figure 3-11, show that different substrate orientations give rise to distinct texturing of the nanowires on the substrate. This is shown in the insets of Figure 3-11. This texturing results from the epitaxial growth of nanowires on the host substrate. Hence, the observed texturing is characteristic of the specific growth directions of the nanowires. Assuming that nanowires grow exclusively along one family of planes, the observed texturing indicates that the preferred growth direction is the <111> direction.

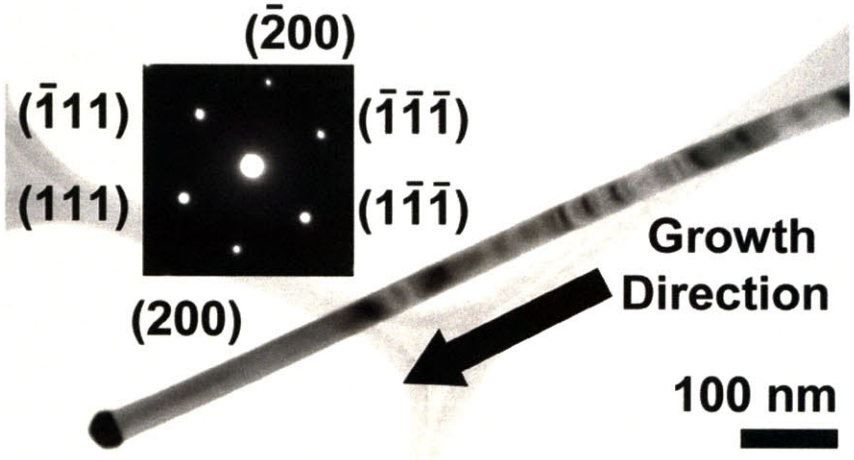


Figure 3-12: Bright-field TEM of GaAs nanowire with SAD pattern, (01-1) zone axis.

To confirm that nanowire growth direction controls texturing, the growth direction of individual nanowires was characterized by bright-field TEM, as described in Section 2.2.3.

Nanowires were tilted to a <1-10> zone axis and selected area diffraction patterns were taken, as shown in Figure 3-12. This selected area diffraction (SAD) pattern agreed with reported SAD patterns of zinc-blende GaAs along the <1-10> zone axis [51], confirming that our nanowires are zinc-blende single crystals growing along the <111> growth direction. Similar analysis was performed on over 20 nanowires with the same results, indicating that the GaAs nanowires grow exclusively along the <111> direction. Thus, it can be concluded that since GaAs nanowire can be made to grow exclusively along the <111> direction, obtaining a uniform array of vertical nanowires may be accomplished using a (111) oriented substrate. This is important to note, given that the growth of wurzite GaAs nanowires [75] as well as zinc-blende GaAs nanowires growing along the <110> direction [76] have been reported.

3.4.2 Effect of total group-III flow rate

While vertical growth is achievable on GaAs 111B substrates, non-vertical growth along alternate <111> directions is also evident in Figure 3-11. To attain an array of vertical nanowires, the mechanism controlling which <111> direction the nanowires grow along must be identified and growth conditions must be engineered to ensure exclusive growth along the vertical <111> direction. Since all of the <111> directions are thermodynamically equivalent[4], obtaining vertically-align nanowires hinges on one simple question: can any one <111> direction be made kinetically preferred?

[4] There should be a slight influence of polarity on the free energy of growth, but this has not been observed to influence the growth of GaAs nanowires

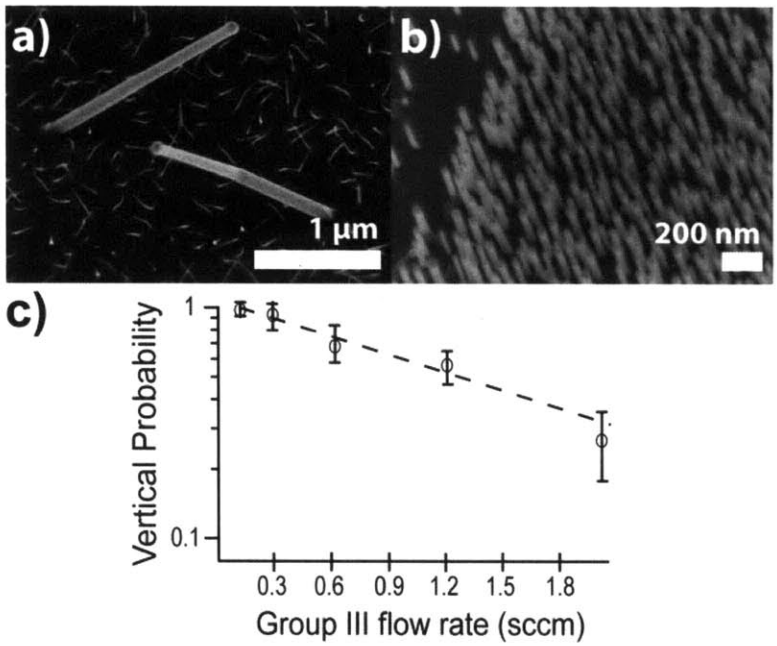


Figure 3-13: Tilted SEM images of GaAs nanowire grown at a) TMGa flow = 2.0 sccm and b) TMGa flow = 0.3 sccm with V/III ratio constant. c) The vertical percentage versus flow rate.

To determine the effects of growth kinetics on vertical alignment, the total group-III flow rate was varied at constant temperature and V/III ratio. The hypothesis is that if changing the growth kinetics changes the vertical probability, a strategy to promote vertical growth can be developed. The result of this experiment is shown in Figure 3-13. At a TMGa flow rate of 2.1 sccm, 22% of the nanowires grow vertically, whereas at a TMGa flow rate of 0.3 sccm, 94% of the nanowires grow vertically. In fact, plotting the vertical probability as a function of group-III flow rate shows that vertical probability increases monotonically with TMG flow rate. This result was obtained from inspection of multiple SEM images. It should be noted, however, that these results depend strongly on the local aerial catalyst density, which could vary significantly in any given sample. Increased density gave rise to less vertical growth. This result is consistent with the growth kinetics being strongly influenced by the surface diffusion of partially decomposed Ga precursor [48], and the error bar in Figure 3-13c was largely affected by the unequal distribution of nanoparticles.

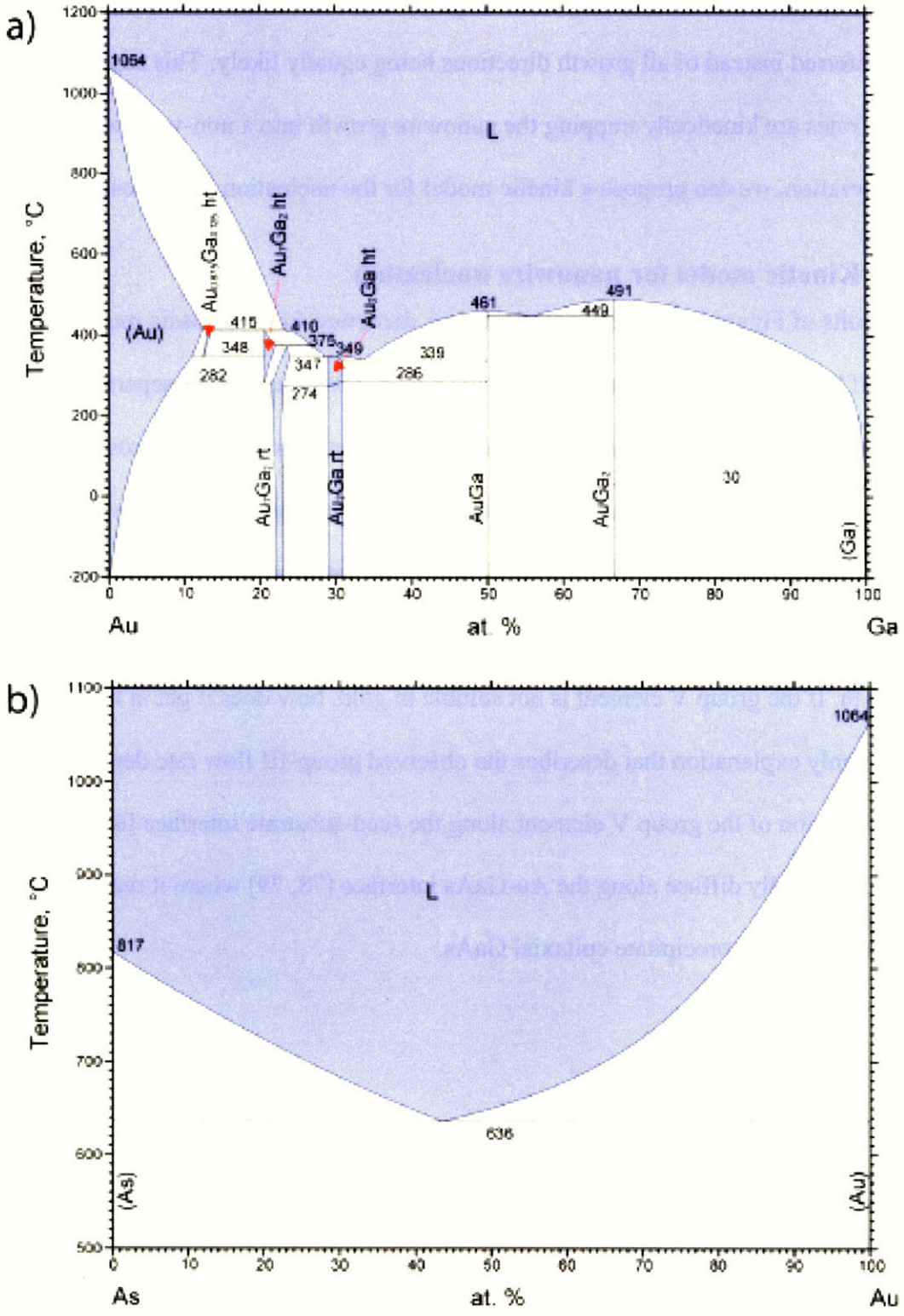


Figure 3-14: Phase diagram for the a) Au-Ga system and b) Au-As system.

One surprising result of this experiment was that at increased flow rates, off-vertical growth was preferred instead of all growth directions being equally likely. This suggests that increased flow rates are kinetically trapping the nanowire growth into a non-vertical direction. From this observation, we can propose a kinetic model for the nucleation of vertical nanowires.

3.4.3 Kinetic model for nanowire nucleation

The results of Figure 3-13c demonstrate a clear departure from the basic model presented in Figure 3-1. If both Ga and As incorporate into the nanoparticles and phase separate in a eutectic process, why would increased flow rate of Ga give rise to non-vertical growth? The answer can be found by inspecting the Au-Ga and Au-As phase diagrams [77], as shown in Figure 3-14. At the growth temperature of 420°C, arsenic is not soluble in gold whereas gallium is soluble. This trend holds true for all III-V compounds and complicates the nature of III-V nanowire growth. If the group V element is not soluble in gold, how does it get in to the nanowire? The only explanation that describes the observed group-III flow rate dependence is rapid surface diffusion of the group V element along the seed-substrate interface [60]. Arsenic has been found to rapidly diffuse along the Au-GaAs interface [78, 79] where it reacts with Ga in the liquid metal particle to precipitate epitaxial GaAs.

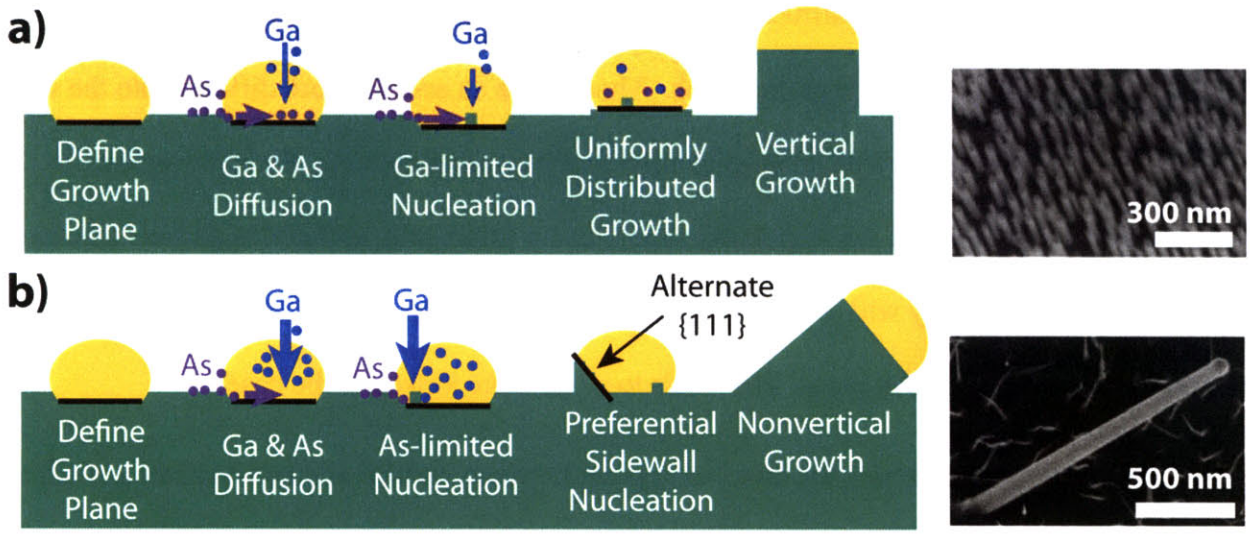


Figure 3-15: a) Schematic of Ga-limited nucleation with corresponding SEM image showing vertical growth. b) Schematic of As-limited nucleation, with corresponding SEM image showing non-vertical growth.

Therefore, a more specific model for Ga and As mass transport during nanowire growth is illustrated in Figure 3-15a&b. First, the Au nanoparticles are annealed allowing the gold define the growth plane as the vertical (111) plane. Next gallium and arsenic are introduced. The gallium incorporates into the gold, supersaturates, and precipitates out to the Au-GaAs interface, while the arsenic adsorbs on the surface and diffuses along the Au-GaAs interface. This distinction is significant because these two reactions occur at different rates. To illustrate the influence of these two growth rates, the resulting growth under gallium-limited and arsenic-limited growth are illustrated in Figure 3-15a & Figure 3-15b, respectively.

If the gallium diffusion and super-saturation is the rate-limiting step, as shown in Figure 3-15a, then the Au-GaAs interface should be arsenic rich. Thus, when a gallium atom diffuses to the surface, it can quickly form with an arsenic atom to form epitaxial GaAs. Since the gallium is diffusing from the liquid, the nucleation should be spatially uniform across the Au-GaAs interface. This leads to uniform vertical growth that follows the vertical (111) growth plane defined during the annealing step. The result is a vertical nanowire.

If the arsenic interfacial diffusion is the rate-limiting step, as shown in Figure 3-15b, then the Au-GaAs interface should be gallium rich. Thus, when an arsenic atom diffuses into the seed particle, it will quickly form with an arsenic atom to form epitaxial GaAs. Since the arsenic is diffusing along the interface, the nucleation should occur principally at the seed particle sidewall. This spatial inhomogeneity will alter the growth interface leading to a non-vertical (111) plane becoming the primary growth plane. This leads to a nanowire kinked at the base.

According to this model, the cross-over point between vertical and non-vertical growth is determined by how far the arsenic can diffuse on the surface before interacting with a gallium atom. If the As atoms can reach the center of the nanoparticles, the growth will be spatially uniform. If the As atoms can not, the growth will be localized to the sidewalls giving rise to instability during the nucleation phase that can lead to non-vertical growth. To quantify this, first consider the Ga side of the equation. In this process, increasing TMGa flow rate increases the chemical potential difference driving Ga out of the Au-Ga mixture and onto the Au-GaAs interface. This chemical driving force can be approximated as

$$\Delta\mu = \mu_{\text{supersaturated}} = kT \ln\left(\frac{p_{\text{Ga}}}{p_{eq}}\right) \tag{3-6}$$

Here p_{eq} is the partial pressure of gallium in Au at the solubility limit. This supersaturation creates a flux of Ga adatoms impinging on the Au-GaAs interface, with an impingement rate given as

$$r = r_0 e^{\Delta\mu/kT} = r_0 \gamma \frac{p_{\text{Ga}}}{p_{\text{eq}}} \tag{3-7}$$

Here r_0 is the attempt frequency of impingement, and taken as constant in this model. Given the rate of Ga atoms impinging on the Au-GaAs interface, the average time for a gallium atom to react with an arsenic atom can be approximated as

$$t = \frac{1}{r} = \frac{p_{eq}}{r_o \gamma p_{\mathrm{Ga}}} \tag{3-8}$$

Now consider the arsenic side of the equation. For spatially uniform growth, the average distance the arsenic must be able to diffuse must be greater than the nanowire radius. This means that deposition can occur at the center as well as the edge. Assuming a constant diffusivity, then the diffusion length of arsenic along the interface, L, is

$$\begin{aligned} R < L_D &= \sqrt{4 D_{\mathrm{As,interface}} t} \\ t &> \frac{R^2}{4 D_{\mathrm{As,interface}}} \end{aligned} \tag{3-9}$$

Here, $D_{\mathrm{As,interface}}$ is the diffusivity of arsenic along the Au-GaAs interface and t is the average lifetime of arsenic as determined by the precipitation rate of Ga from the Au-Ga liquid. The condition for growth stability can then be, as shown in (3-10).

$$p_{Ga} < \frac{4 D_{\mathrm{As,interface}} p_{eq}}{r_o R^2} \tag{3-10}$$

It should be noted that the partial pressure of arsine does not affect the diffusion length of arsine along the surface, because the mass-transport of arsenic to the Au-substrate interface is not a rate-limiting step. Hence, only the value of the group III flow influences vertical epitaxy. This model explains the observed phenomena and predicts that higher temperature promotes vertical epitaxy. This effect has been observed in literature for the GaAs system [70]. It should be noted that with decreasing diameter, the rate limiting step controlling Ga impingement will become

dominated by the Gibbs-Thomson effect which will increase the factor p_{eq}. This will make epitaxy more difficult for smaller radius nanowires. It should also be noted that this effect is only observed during nanowire nucleation. In fact, published reports have shown nanowires will not kink during steady-state growth. However, if nanowire growth is stopped, the sample cooled, and nanowire growth re-initiated, then kinking can occur [70]. This demonstrates that the kinetic instability described in the model presented is a transient instability that only appears during the initial nucleation event. This is reasonable considering that supersaturation forces are strongest during the initial nucleation event.

In summary, nanowire growth with a probability of vertical alignment in excess of 95% was achieved by using GaAs (111)B substrates and reducing the total group III flow rate below 0.3 sccm at a constant V/III ratio of 20. If the group-III flow is higher, nanowires become susceptible to a transient instability in growth direction during the nucleation phase, which kinetically favors non-vertical growth.

3.5 Optimized vertical GaAs nanowire arrays

At this point, an understanding of the growth parameters on the nanowire morphology has been developed. Combining lithography with galvanic reaction, Au nanoparticles have been demonstrated with less than 10% diameter variation and greater than 50 nm position accuracy.

Process Parameter	Optimized Value
Growth Temperature	420°C
TMG flow rate	0.30 sccm
V/III ratio	20

Table 3-2: Optimized growth parameters for vertical GaAs nanowire growth

By understanding the relative growth kinetics of VLS nanowire growth and spontaneous VS deposition on nanowire sidewalls, an optimal growth temperature of 420°C was determined

at a V/III ratio of 20. At this temperature, sidewall deposition is kinetically inhibited, but VLS nanowire growth is not. The result is a tapering factor of 0.001. This is low enough to claim independent control over axial and radial elongation. By understanding that increased group III flow rate can create a transient instability in nanowire growth direction, a TMGa flow rate under 0.3 sccm was chosen to allow greater than 95% of grown nanowires to be vertical. The effect of V/III ratio on nanowire growth was also studied, however no significant effect was observed. An optimized set of growth parameter has been determined, as summarized in Table 3-2.

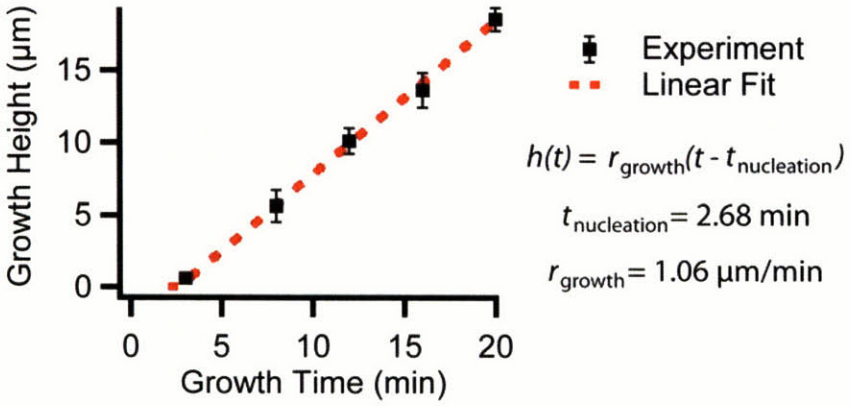


Figure 3-16: Growth rate calculation for GaAs nanowire growth.

The only process parameter left to optimize is the growth time. This will depend entirely on the desired nanowire height. At these optimized set of growth parameters, the axial growth rate was calculated by growing nanowires for different times and recording their height. The data is summarized in Figure 3-16. The nanowire height depends linearly on the growth time. Using this data, the nanowire height (h) as a function of growth time (t) is $h(t) = r_{growth}(t - t_{nucleation})$. Here, the axial growth rate, r_{growth}, is 1.06 μm/min and the nucleation time, $t_{nucleation}$, is 2.68 min.

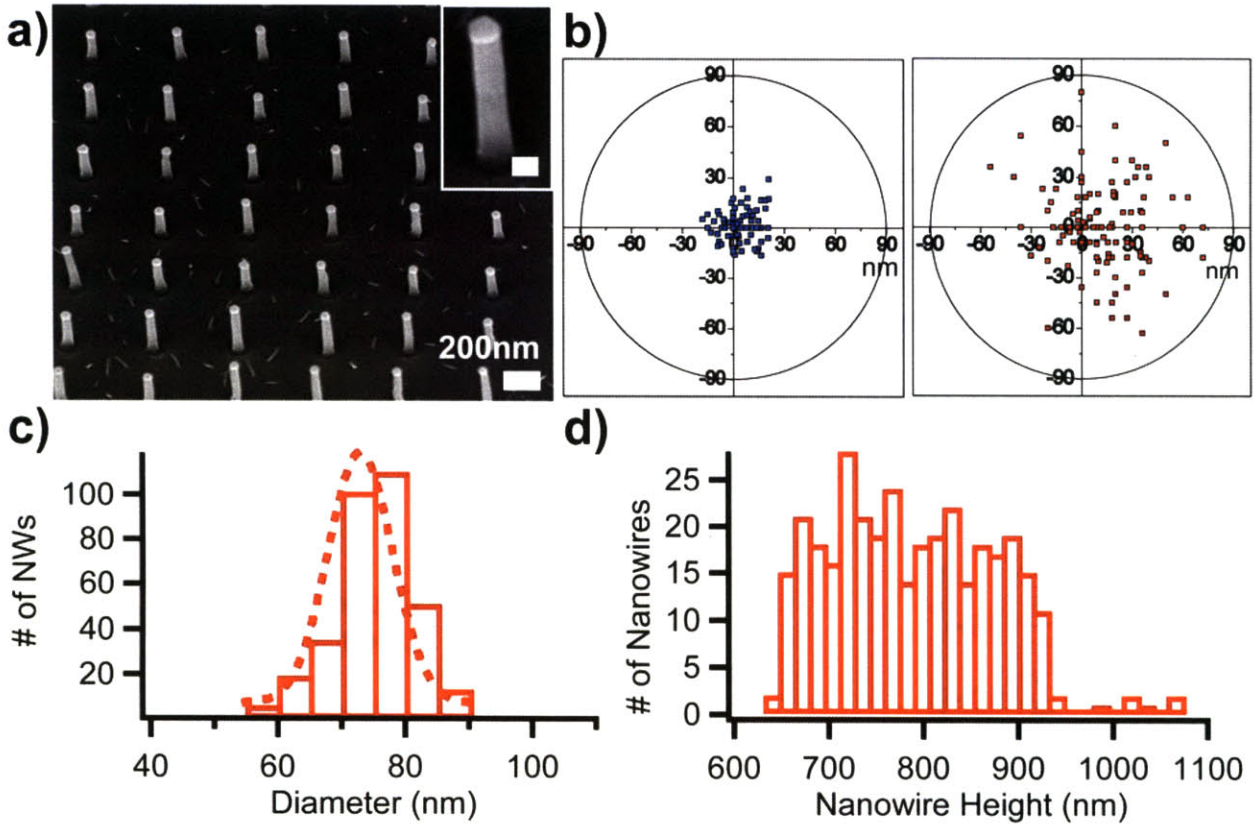


Figure 3-17: a) SEM image of an optimized vertical GaAs nanowire array. Distributions of the b) positions, c) diameters, and d) heights the nanowires grown from the Au nanoparticle array shown in Figure 3-6.

An optimized GaAs nanowire array can thus be achieved by using galvanic reaction and electron beam lithography to deposit an ordered array of Au nanoparticles and the optimized growth recipe presented in Table 3-2 to achieve vertical GaAs nanowires. To achieve a height just under 1 μm for vertical transistors [20], a growth time of 3 min was utilized. The result is shown in Figure 3-17a. To quantify the quality of the uniformity of this array the position, diameter, and height distributions have been calculated. Figure 3-17b shows the position of the Au nanoparticles before annealing and after nanowire growth. Since the nanowire position is defined during the pre-growth anneal and the same sample was used, this data is identical to the data presented in Figure 3-6b. Figure 3-17c shows the diameter distribution of the optimized vertical GaAs nanowire array. Calculation of the diameter distibution reveals a diameter of 73 ±

7 nm. This corresponds to a 10% variability in nanowire diameter and can be attributed to variations in the nanoparticle diameter. Further optimization of the lithography and galvanic reaction processes should be able to reduce this variation. However, a 10% variation is small enough to fabricate proof-of-concept strucutures based on vertically aligned GaAs nanowire arrays. Figure 3-17d shows the height distribution of the optimized vertical GaAs nanowire array. The distribution appears to be evenly distributed beween 650 and 925 nm. This suggests that variation in the nanowire diameter may not be the driving factor behind this instability, which would suggest the height distribution to be Gaussian, like the diameter distribution. Instead, it is possible that variation in the nanowire nucleation time accounts for this variation. Further studies into the process parameter dependance of nanowire nucleation time and its standard deviation would be of value, but are beyond the scope of this thesis.

In conclusion, by understanding the effect of different process parameters on the properties of individual nanowires, uniform arrays of vertically-aligned GaAs nanowire arrays have been demonstrated and the underlying nucleation and growth mechanisms modelled. The rest of this thesis will now focus on the use of vertically-aligned GaAs nanowires to achieve core-shell GaAs/AlGaAs heterostrucutres and n-type doping via the deposition of an n-type epitaxial GaAs shell.

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Chapter 4. Growth and properties of core-shell GaAs/AlGaAs nanowires

This chapter presents the growth and in-depth characterization of vertically-aligned core-shell GaAs/AlGaAs nanowire heterostructures. By optimizing the shell deposition temperature and catalyst density, high temperature stability was maintained and AlGaAs shell deposition was achieved. Analysis demonstrated the shell to be of constant composition with the shell thickness changing by 2 nm/μm. BF-TEM and lattice resolved HAADF STEM structural analysis demonstrated the core-shell interface to be epitaxial and defect-free. Measuring the intensity profile of the HAADF image of the core-shell interface revealed the interfacial sharpness to be 1.4 nm, which can be attributed to either compositional grading or core-shell interfacial roughness. These results demonstrate that the morphology, composition, and crystalline quality of core-shell nanowires can be controlled precisely enough for applications in high mobility electronics.

4.1 Realizing epitaxial shell deposition

The fabrication of core-shell nanowire heterostructures has been demonstrated was first demonstrated for Si/Ge [80] using a two temperature process. First, the core is grown at low temperature via the VLS mechanism as described by Chapter 3. Then, the shell is deposited at higher temperatures typical of thin-film epitaxy, to ensure uniform shell deposition. The core-shell nanowire heterostructure and then applied to the III-V materials in GaN/AlGaN and used to make proof-of-concept electronics [25] and optoelectronic [81] devices. These devices demonstrated the potential benefit of independently controlling axial and radial semiconductor growth for device applications.

Towards high mobility electronics, the GaAs/AlGaAs system was explored. Initial studies into the GaAs/AlGaAs system [35, 82, 83] have suggested that core-shell nanowire fabrication may be realized in the GaAs/AlGaAs system with an aluminum fraction less than 15%. These reports demonstrated the core-shell morphology using photoluminescence measurements, but provided no information regarding the morphology, uniformity, or crystal

structure of these nanowires. Only one report existed concerning the structural properties of GaAs/AlGaAs nanowires. That report used a scanning tunneling microscopy technique [32] to demonstrate that it is possible to achieve a GaAs/AlGaAs core-shell interface free of threading dislocations, however it could not measure the coherency or sharpness of the core-shell interface.

For core-shell GaAs/AlGaAs nanowires to be used for high mobility electronics, it must be demonstrated that the structure and composition of the nanowires are uniform in both the axial and radial direction and that defect-free epitaxial and coherent core-shell interfaces are achievable. Moreover it is desirable to achieve AlGaAs shell deposition in order to provide increased conduction band offset. This chapter focuses on demonstrating core-shell GaAs/AlGaAs nanowire growth and conducting in-depth characterization of the shell to determine the structural and compositional properties achievable in core-shell GaAs/AlGaAs nanowires.

4.1.1 Shell deposition process

Core-shell nanowire fabrication was conducted utilizing a two-step approach based on methods previously reported for core-shell nanowires [80], as described in Section 2.1.4.

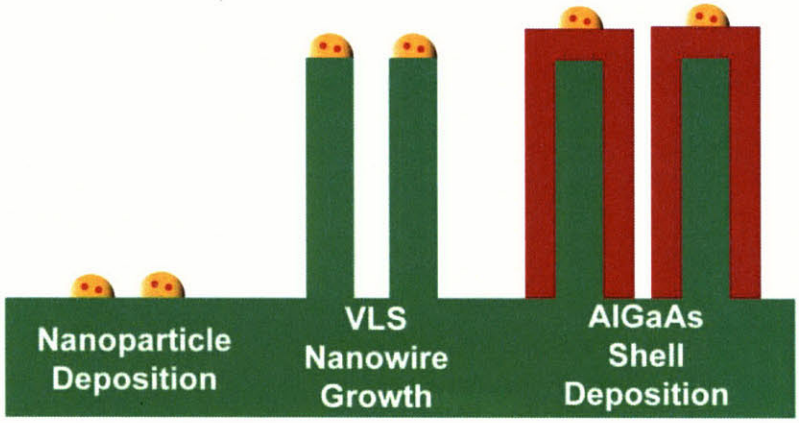


Figure 4-1: Schematic showing the shell deposition process.

The core-shell nanowire fabrication process is illustrated in Figure 4-1. Au seed particles are first deposited on the substrate. Vertically-aligned nanowires were grown by the VLS mechanism according to the optimized growth recipe presented in section 3.5. To enable the uniform deposition of an epitaxial shell, the temperature was increased above 650°C to remove any kinetic barriers to the spontaneous decomposition of precursors and deposition of semiconductor material.

4.1.2 High temperature stability of nanowires

Shell deposition was attempted by growing vertically-aligned GaAs nanowires according to the recipe in Section 3.5, increasing the chamber temperature to 650˚C, and introducing gallium, arsenic, and aluminum precursor. While increasing the reactor temperature above 650˚C enables spontaneous precursor decomposition and material deposition, it also revealed a morphological instability in the semiconductor nanowires.

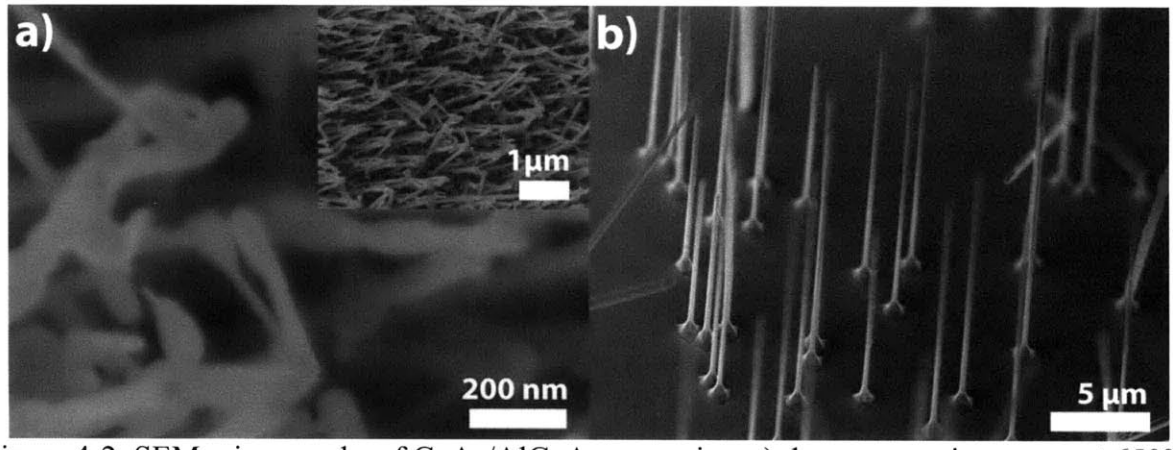


Figure 4-2: SEM micrographs of GaAs/AlGaAs nanowires a) dense nanowire grown at 650°C showing morphological instability, inset is sample at lower magnification and b) sparse nanowire grown at 700°C maintaining morphological stability.

This morphological instability is clearly seen in GaAs/AlGaAs nanowires grown from dense catalyst at 650°C. The vertical nanowires either collapse onto the substrate or fuse with neighboring nanowires, as shown in Figure 4-2a. Closer examination of the nanowires reveals that variations in the total diameters of the nanowires emerge. Interestingly, reducing the average catalyst density to less than 0.1 nanoparticles/μm^2 significantly improves the nanowire stability in the shell deposition temperature range, as shown in Figure 4-2b.

These results indicate that while the nanowire geometry is not the energetically most preferred geometry, it is a metastable geometry that can be maintained so long as the nanowire is not given a pathway to evolve into an energetically preferred geometry. This instability occurred during non-vertical nanowire growth over an aerial density range of 0.1 - 5 nanowires/μm^2 and during vertical growth above an aerial density of approximately 1 nanowires/μm^2. From these results it was concluded that this instability occurred when individual nanowires were able to touch one at high temperature. Further annealing experiments (not shown) proved unable to determine the pathway of this structural evolution, so the exact mechanism of this instability

could not be determined. However, it was found that high temperature stability could be maintained with vertical nanowire growth at an aerial density less than 1 nanowire/μm^2.

Possible mechanisms include the Rayleigh instability and shell island formation [84]. This effect has been observed in both silicon [85, 86] and III-V [87] nanowires and their behavior has been shown to depend on a number of factors. To explain the appearance and behavior of morphological instability in nanowires, different mechanisms have been proposed. These mechanisms include the Rayleigh instability [88] and shell island nucleation [84], however no model of nanowire morphological instability exists that can account for all behaviors reported in literature. In our system it is unclear whether the diameter variations are limited to the shell or occur both in the core and the shell. Therefore, it is possible that one or more of the instability mechanisms that have been proposed in literature may be responsible. Since however, this thesis seeks to demonstrate that this instability can be avoided, a systematic study of the mechanism of nanowire instability is therefore beyond the scope of this thesis.

4.1.3 Realization of core-shell nanowires

Shell deposition was conducted at a temperature of 700°C to enable decomposition and deposition of AlGaAs material along the sidewalls of the nanowire. To ensure uniform deposition, the V/III ratio was increased to 200, as compared to a V/III ratio of 20 used for nanowire growth. Due to the limited flow control range of the MOCVD reactor used, achieving a V/III ratio of 200 required reducing the group-III rate from the 0.30 sccm used in VLS growth to 0.21 sccm. In order to ensure significant Al incorporation in the shell, the group III flow was 75% TMA.

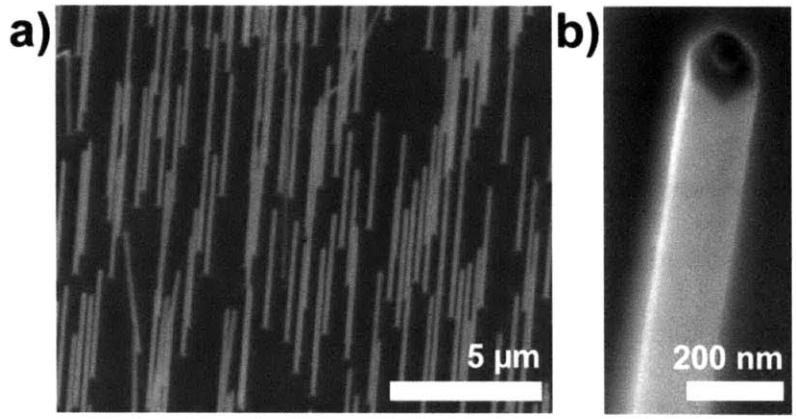


Figure 4-3: SEM micrographs of vertical core-shell nanowires showing a) 80 - 90% of nanowires maintain a stable morphology and b) the shell is faceted with a hexagonal cross-section.

These growth conditions yielded stable nanowire growth, as shown in Figure 4-3. SEM images of core-shell nanowires (Figure 4-3a) demonstrate that 80 - 90% of the nanowires maintain a stable morphology through the high temperature shell deposition. SEM images near the tip of nanowires after shell deposition (Figure 4-3b) show symmetric overgrowth around the Au seed nanoparticle, suggesting uniform shell deposition. Moreover, it was noted that the overgrowth was faceted with a hexagonal cross-section, which suggests an epitaxial relationship with the nanowire core.

As shown in Figure 4-4a, TEM images of GaAs nanowire cores show straight nanowires of constant diameter that is always less than the catalyst nanoparticles indicating catalyst mediated growth of the core. Bright-field TEM images of core-shell nanowires, shown in Figure 4-4b, show sharp contrast at the core-shell interface. It should also be noted that a small axial elongation also occurred during the high temperature shell deposition; based on TEM observations we estimate the growth rate of the high temperature axial elongation to be approximately the same as the shell deposition. We also estimate the growth rate of the high temperature axial elongation to be at least one order of magnitude less than the low temperature growth rate of the GaAs nanowire core.

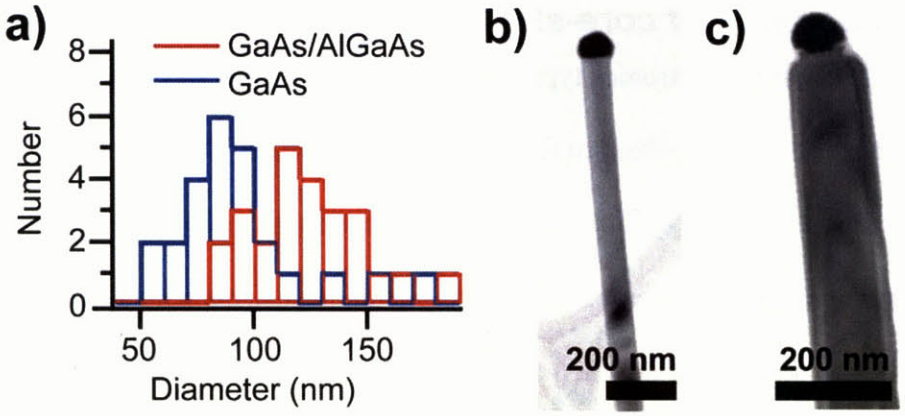


Figure 4-4: a) Histogram of nanowire diameter before and after shell deposition as well as TEM micrographs of nanowires b) before and c) after shell deposition

To confirm an increase in nanowire diameter after shell deposition and to determine the average shell thickness, the diameters of over 25 nanowire cores as well as over 25 core-shell nanowires with shells deposited for 1.5 min were measured from TEM images, as shown in Figure 4-4c. By fitting a Gaussian function to the measured nanowire diameter distribution, the average diameters[5] were determined to be 84 ± 15 nm and 132 ± 13 nm before and after the shell deposition, respectively, indicating an average shell thickness of 24 nm. The observed variations in the shell thickness are most likely due to a non-uniform distribution of catalyst nanoparticles on the substrate causing variations in the local precursor concentrations during growth [48]. Further improvement in the shell thickness control could be achieved by preparing GaAs nanowires in ordered arrays, as presented in section 3.2.2.

Hence, by utilizing an aerial catalyst density less than 1 nanowire/μm^2, a growth temperature of 700°C, and a group III-flow rate of 0.21 sccm, uniform shell deposition on a VLS-grown GaAs nanowire core has been demonstrated.

[5] The observed variations in core diameters are most likely due to diffusion of Au nanoparticles during the pregrowth anneal. The apparent diameter measured by TEM depends on the azimuthal rotation of the nanowire on a TEM grid. If the nanowire rests on a facet instead of a facet corner, the measured diameter will be a factor of $2/\sqrt{3}$ greater.

4.2 Composition of core-shell nanowires

Since high mobility electronics typically utilize a GaAs/AlGaAs heterostructure, it is important to measure the composition of the core-shell nanowires. That the shell is composed of AlGaAs was confirmed by energy dispersive X-ray spectroscopy measurements conducted in scanning transmission electron microscopy. Modeling the nanowires with a hexagonal cross-section enabled quantification of the shell thickness and composition from EDX line scans.

4.2.1 Energy dispersive X-ray spectroscopy measurement

The compositions of the nanowires were measured by EDX in a STEM. Since STEM utilizes a converged electron beam, it is able to measure composition at a point (single point quantification) or measure the composition profile along a line (line scan) or in an area (compositional mapping).

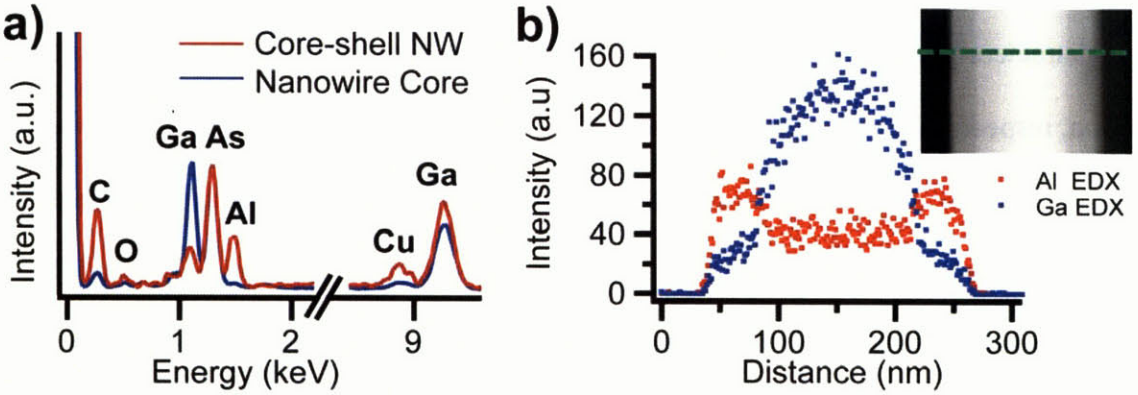


Figure 4-5: a) EDX spectra of a nanowire core and a core-shell nanowire. Signal normalized for As K line. b) Ga and As EDX profiles across the diameter of a core-shell nanowire. Inset is STEM image of core-shell nanowire.

Energy dispersive X-ray spectroscopy (EDX) analysis, as shown in Figure 4-5a, verified the presence of AlGaAs in the core-shell nanowires. The EDS spectra of plan-view core-shell nanowires show a strong Al signal as compared to no Al signal in GaAs nanowires and confirm the presence of Al in the nanowires after the shell deposition. To determine the distribution of GaAs and AlGaAs in the core-shell nanowire, the Ga and As profiles were recorded across the

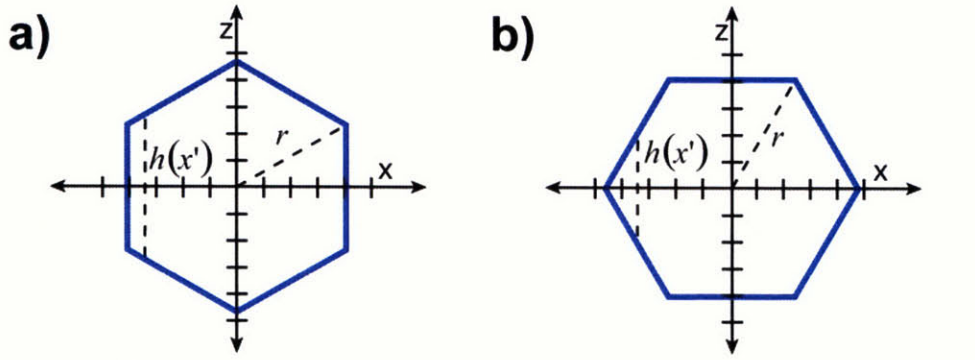
diameter of the nanowire, as shown in Figure 4-5b. Since the intensity of the Ga and Al signals are proportional to the amount of these elements, the ratio of the Al to Ga signal is indicative of the aluminum percentage, x, in the $Al_xGa_{1-x}As$ alloy in that region. Qualitatively, these data show a greater concentration of aluminum in the shell than in the core, as expected. Quantification was performed by comparing measured EDX profiles to models.

4.2.2 Modeling EDX compositional profiles

Before attempting to quantify the composition, two things must be noted. First, the measured composition profile is the composition of the sample averaged in the vertical direction. For example, a thin foil of $Al_{0.25}Ga_{0.75}As$ would produce the same EDX profile as a thin foil of $Al_{0.50}Ga_{0.50}As$ sitting atop a thin foil of GaAs with equal thickness. Since the shell sits atop the core, the observed EDX profile is the sum of the core and shell profiles. Hence the morphology of the sample, in this case the cross-sectional profile of the nanowire, must be accounted for in the quantification of the EDX signal. Second, the electron beam exciting X-rays has a finite diameter, σ. Thus, when irradiating the sample at $x = 0$, X-rays are observed from $-\sigma < x < \sigma$. Since the electron beam has a Gaussian intensity profile, this phenomenon is known as Gaussian beam broadening. Therefore, the EDX profile for element X, $I_X(x)$, can modeled according to Equation (4-1).

$$I_X(x) = \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{\infty} \sum_i x_{X,i} h_{X,i}(x') e^{-\frac{(x-x')^2}{2\sigma}} dx' \qquad (4\text{-}1)$$

Here, $x_{X,i}$ is composition of element X in structure i (i = core or shell) and $h_{X,i}(x')$ is the height profile of structure i. In order to model the match the measured EDX data to a model, the height profile of the nanowire must be known.



$$h(x')=\begin{cases} 2r-\dfrac{2|x'|\sqrt{3}}{3} & |x'|<\dfrac{r\sqrt{3}}{2} \\ 0 & |x'|>\dfrac{r\sqrt{3}}{2} \end{cases} \qquad h(x')=\begin{cases} r\sqrt{3} & |x'|<r/2 \\ 2r\sqrt{3}-2x'\sqrt{3} & r/2<|x'|<r \\ 0 & |x'|>r \end{cases}$$

Figure 4-6: Height profile for a hexagonal cross-section nanowire resting on a) a facet corner and b) on a facet.

Based on the images of the shell shown in Figure 4-3, a regular hexagonal cross-section was assumed for the height profile, as shown in Figure 4-6. It should be noted that the height profile of the nanowire will depend on the azimuthal orientation of the nanowire. If the nanowire lies on a facet corner, which can occur if the nanowire falls into a valley of the lacey carbon coating on the TEM grid, then the height profile will be given by Figure 4-6a. If the nanowire lies on a flat surface, then the height profile will be given by Figure 4-6b. The height profile of the hexagonal shell was modeled as a hexagon according to Figure 4-6 minus the height profile of the inner core, which was also modeled as a hexagon according to Figure 4-6.

4.2.3 Quantification of core-shell nanowire composition

Measured EDX profiles were compared to simulated EDX profiles in order to determine what shell thickness and composition best fits the measured profile. EDX profiles were simulated according to (4-1) assuming a hexagonal cross-section with a height profile shown in Figure 4-6.

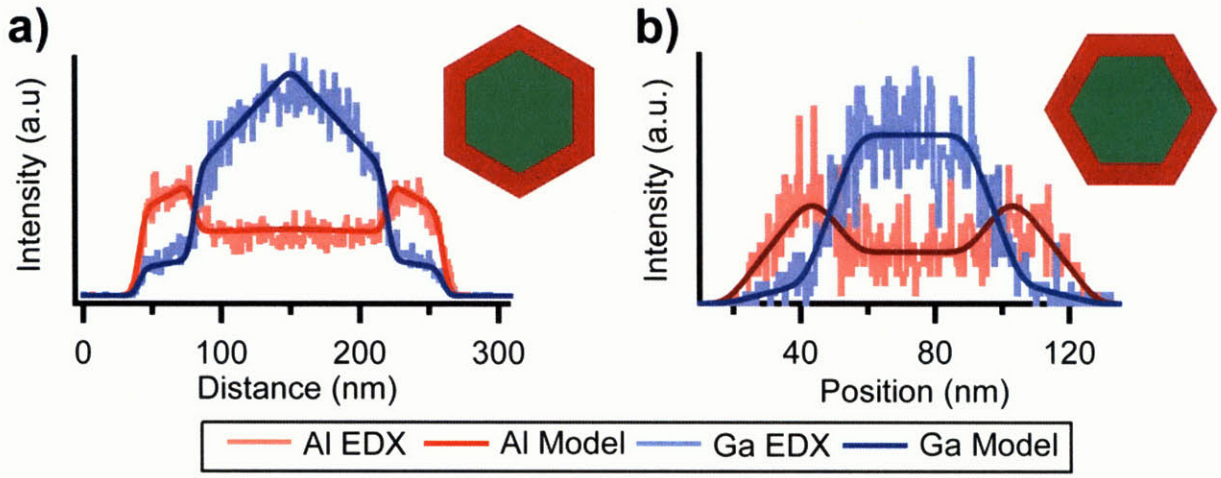


Figure 4-7: EDX profiles for Ga and Al signals in core-shell plotted alongside Gaussian beam broadening model for a core-shell nanowire a) laying on a facet corner and b) laying on a facet sidewall.

The nanowire measured in Figure 4-5b was well modeled by a core-shell $GaAs/Al_{0.89}Ga_{0.11}As$ nanowire laying on a facet corner with core radius of 62.2 nm and a shell thickness of 41.6 nm, as shown in Figure 4-7a. As observed in Figure 4-7b, nanowires were also observed to match the height profile shown in Figure 4-6s, which corresponds to the nanowire lying on a facet. The azimuthal orientation of the nanowire can be seen by examining the Ga signal in the core. For a nanowire lying on a facet, this profile is flat. For a nanowire lying on a facet edge, this profile exhibits an inverted V shape.

In order to ensure that the nanowire posses a height profile given by either Figure 4-6a or Figure 4-6b and not an arbitrary angle in between, the Kikuchi pattern of the nanowire was measured to determine the azimuthal tilt. The height profile of Figure 4-6a corresponds to a [1-10] zone axis, whereas the height profile of Figure 4-6b corresponds to a [11-2] zone axis. Quantitative EDX measurements were performed on nanowires tilted to within 1° of the zone axis. It should be noted, however, that quantitative EDX was never performed on nanowires

tilted precisely on their zone axis because electron channeling effects [89] substantially reduced the EDX signal.

Measuring over 15 nanowires revealed that the shell possessed a composition of 89 ± 3% aluminum. This was confirmed by single-point EDX quantification at the nanowire shell. Based on the signal-noise ratio, presence of Brehmstrahlung, and X-ray reabsorption [90], we estimate the error in the EDX calculation to be at least 3%. Hence we conclude that the AlGaAs shells were consistently composed of 89% aluminum within the accuracy of the measurement.

This consistency in shell composition is surprising given that variations in local Au nanoparticle density created variations in the shell thickness, as seen in Figure 4-4. In order to probe the effect of flow rate on shell composition, the flow of TMA and TMG was altered from 75% to 50% Al by vapor pressure, which resulted in $Al_xGa_{1-x}As$ shell composition of $x = 0.86 \pm 0.02$. We also deposited AlGaAs shells at 680°C and 75% Al by vapor pressure resulting in $x = 0.71 \pm 0.06$ and at temperatures below 650°C, which resulted in amorphous shell growth with $x < 0.05$ detectable by EDS. These results suggest that shell composition is primarily controlled by shell deposition temperature and variations in local precursor flow rates will not cause compositional variation.

4.3 Morphological & compositional uniformity of core-shell nanowires

By performing multiple line scans at different distances from the Au seed particle, imaging the nanowires in their cross-section, and creating a 3D reconstruction of the core-shell nanowire using electron tomography, it was determined that the shell thickness and composition are axially and radially uniform.

4.3.1 Axial uniformity of core-shell nanowires

The axial uniformity of our core-shell nanowires was measured to quantify shell deposition quality along the nanowire length. A series of EDX line scans were performed along the length of our nanowires and these EDX profiles were fitted to models to extract the shell thickness and composition.

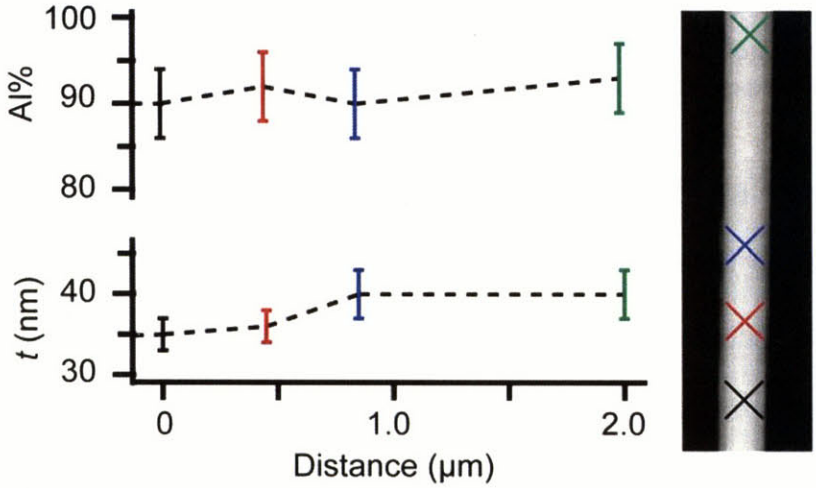


Figure 4-8: The shell composition and thickness of a representative core-shell nanowire measured by EDX at different point along the length of the nanowire.

Figure 4-8 shows the results from a representative core-shell nanowire with the average shell composition of 90% with a 2-3% variation along the nanowire length - within the error of the measurement. The overall diameter increases with increasing distance from the Au seed particle along the growth direction at a rate of approximately 2 nm/μm. With a typical FET gate length of 150 nm or less, this shell thickness variation is not likely to affect device performance.

4.3.2 Radial uniformity of core-shell nanowires

To determine the spatial distribution and uniformity of the AlGaAs shell, high angular annular dark field (HAADF) and EDX analysis was conducted on nanowire cross-sections.

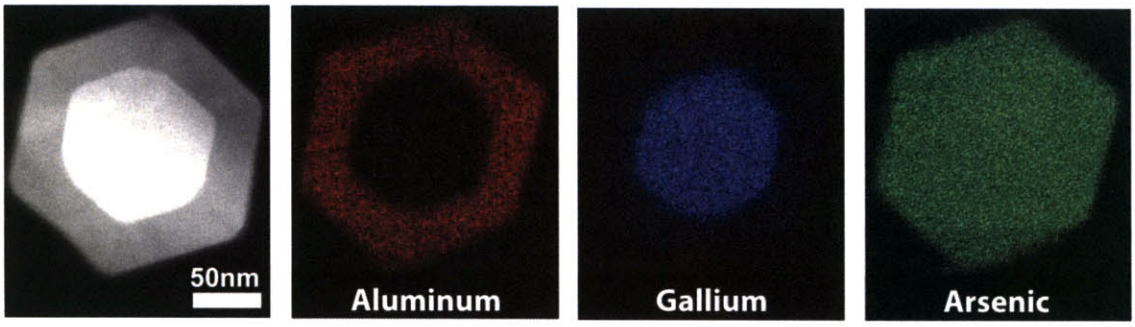


Figure 4-9: High angular annular dark field STEM image of core-shell nanowire cross-section and corresponding chemical maps for aluminum, gallium, and arsenic.

As shown in Figure 4-9, the Z-contrast images match the EDX elemental mappings with Al signal detected only in the nanowire shell and together confirm the targeted core-shell structure. HAADF STEM images of core-shell nanowires show darker contrast in the nanowire shell than in the core, which indicates deposition of a material with lower average atomic number in the shell. Measurement of the shell thickness along each of the six facets reveals that the difference in thickness between the narrowest and thickest facet is 1.2 nm. Measurement of the shell composition by single-point EDX quantization along each of the six facets also reveals that the composition is uniform to within 3%, the accuracy of the measurement. This measurement confirms the accuracy of the regular hexagonal model presented in Figure 4-6. Moreover, this variation is not likely to effect the performance of a FET based on a core-shell nanowire and could be reduced by optimizing the growth conditions of the shell deposition.

4.3.3 3D reconstruction of core-shell nanowires

To simultaneously measure the axial and radial uniformity of the core-shell nanowires, electron tomography in high angular annular dark field STEM was performed in collaboration with Dr. Peter Cherns at CEA Grenoble [91]. Electron tomography consists of imaging a sample at multiple tilt angles to develop a 3D representation of the sample. High angular annular dark field STEM is used because the image contrast is highly sensitive to atomic composition [92].

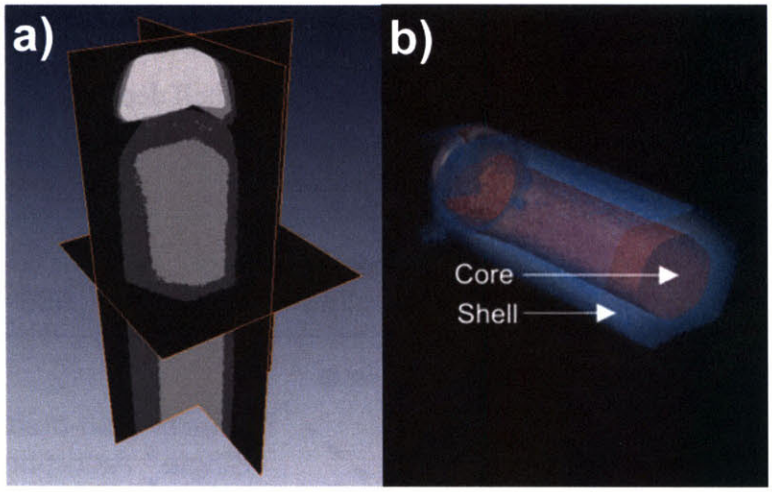


Figure 4-10: a) HAADF STEM images of core-shell nanowires taken at different angles. b) 3D reconstruction of a core-shell nanowire imaged using HAADF STEM tomography. Images courtesy of Dr. Peter Cherns, CEA Grenoble.

A 3D reconstruction of a core-shell nanowire is shown in Figure 4-10. Utilizing the sensitivity of image contrast on chemical composition and applying threshold image brightness values, the core and the shell regions can be distinguished. In agreement with the axial uniformity studies shown in Figure 4-8, the shell thickness and composition are uniform along the length of the nanowire. Moreover, no significant non-uniformities are observed in the cross-section of the nanowire. This suggests that the thickness and composition of the shell deposition is uniform along the axial and radial directions. Examination of the core-shell interface shows no significant roughness or non-uniformity, however an in-depth study of the core-shell interface using cross-sectional TEM samples, which will be presented in section 4.4.2, is needed to quantify the interfacial roughness.

4.3.4 Effect of shell deposition conditions on uniformity

The effect of growth temperature and group III flow rate on the deposition of the epitaxial shell was studied to estimate the growth parameter range over which uniform and single crystalline shell deposition may be achieved. Since this chapter focuses on understanding the

structural and compositional properties of GaAs/AlGaAs nanowires in order to determine their viability for high mobility applications, a full exploration of shell deposition parameter space was beyond the scope of this thesis.

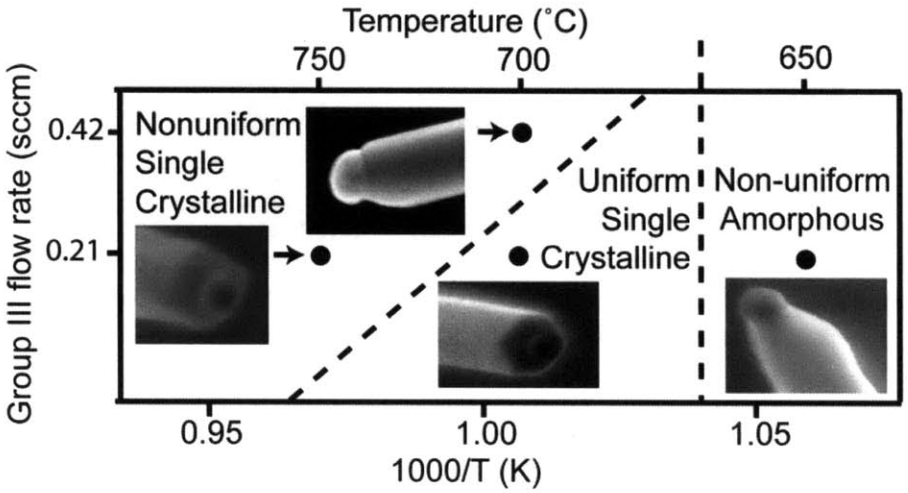


Figure 4-11: Basic zone diagram for shell deposition.

The results of this basic exploration of parameter space are presented in Figure 4-11. The optimal conditions were determined to be a group III flow rate of 0.210 sccm and a temperature of 700°C. Under these conditions, shell deposition was found to be uniform by SEM analysis and epitaxial by TEM analyses (will be described in more detail later in this chapter). Reducing the shell deposition temperature resulted in non-uniform and amorphous deposition. No polycrystalline region was observed.

Increasing the shell deposition temperature to 750°C also resulted in epitaxial shell deposition, however the shell was found to be non-uniform in the radial direction. The cause of non-uniform shell deposition was hypothesized to be an increased the shell deposition rate resulting from increased temperature. This hypothesis is supported by the observation of non-uniform shell deposition at 700°C and a group III flow rate of 0.42 sccm. Therefore it can be proposed that there exists a threshold growth rate above which shell deposition is non-uniform.

Assuming an Arrhenius functional form of the shell deposition rate, as shown in Equation (4-2), this threshold can be denoted by the slanted dashed line in Figure 4-11. Proof of this hypothesis and precise determination of the terms r_0 and ΔG would require in-depth growth studies and are beyond the scope of this thesis.

$$r = r_0 e^{-\Delta G/kT} \tag{4-2}$$

In order to probe the effect of flow rate on shell composition, the flow of TMA and TMG was altered from 75% to 50% Al by vapor pressure, which resulted in $Al_xGa_{1-x}As$ shell composition of $x = 0.86 \pm 0.02$. AlGaAs shells were also deposited at 680°C and 75% Al by vapor pressure resulting in $x = 0.71 \pm 0.06$ and at temperatures below 650°C, which resulted in radial shell growth with $x < 0.05$ detectable by EDS. These results suggest that shell composition is primarily controlled by shell deposition temperature, which is indicative of kinetically-limited growth. Since the presence of the Au is known to enhance the decomposition of Ga and Al precursor, it is possible that the presence of Au effectively transitions the shell deposition from the mass-transport-limited to kinetically-limited regime. As will be explained in Chapter 5, the removal of the Au nanoparticle prior to shell deposition is required to achieve n-type doping. Therefore, realization of n-AlGaAs with tunable composition should be achievable if the Au seed nanoparticle is removed prior to shell deposition.

Hence, shell deposition was found to be morphologically and compositionally uniform in both the axial and radial direction. Based on a basic exploration of shell deposition parameter space, uniformity seems achievable below a threshold growth rate. To further evaluate core-shell GaAs/AlGaAs nanowires as candidates for high mobility applications, the crystalline structure of the nanowire and core-shell interface must be precisely characterized.

4.4 *Structural properties of core-shell nanowires*

In order to be considered candidates for high mobility electronics, core-shell nanowires must be free of structural defects such as dislocations, twin planes, and antiphase boundaries as structural defects scatter electrons and reduce the electron mobility [93]. The GaAs/$Al_{0.9}Ga_{0.1}As$ system has 0.12% misfit, which is compressive to the $Al_{0.9}Ga_{0.1}As$. It has been shown [94, 95] that for lattice-mismatched heterostructures the nanowire core-shell geometry has significantly greater critical film thickness than planar structures, because the nanowire core can accommodate part of the strain. To determine if dislocation formation is expected in GaAs/AlGaAs core-shell nanowires, the coherent strain energy and the energy associated with the presence of strain-relaxing dislocations in this system were calculated based on the methodology for determining coherency limits in core-shell nanowires [94, 95]. For a core-shell GaAs/$Al_{0.9}Ga_{0.1}As$ nanowire with a core diameter of 100 nm and shell thickness of 50 nm the additional energy associated with the presence of a dislocation is greater than the energy reduction of strain relaxation making dislocation formation not thermodynamically favorable.

4.4.1 Structural analysis along nanowire length

To confirm this prediction, the structures of individual nanowires were studied using transmission electron microscopy. TEM is capable of atomic resolution and can precisely the Burgers vectors of any defects observed [51]. Examining many nanowires at a variety of tilt angles is an accepted method of characterizing the structure of nanowires [68].

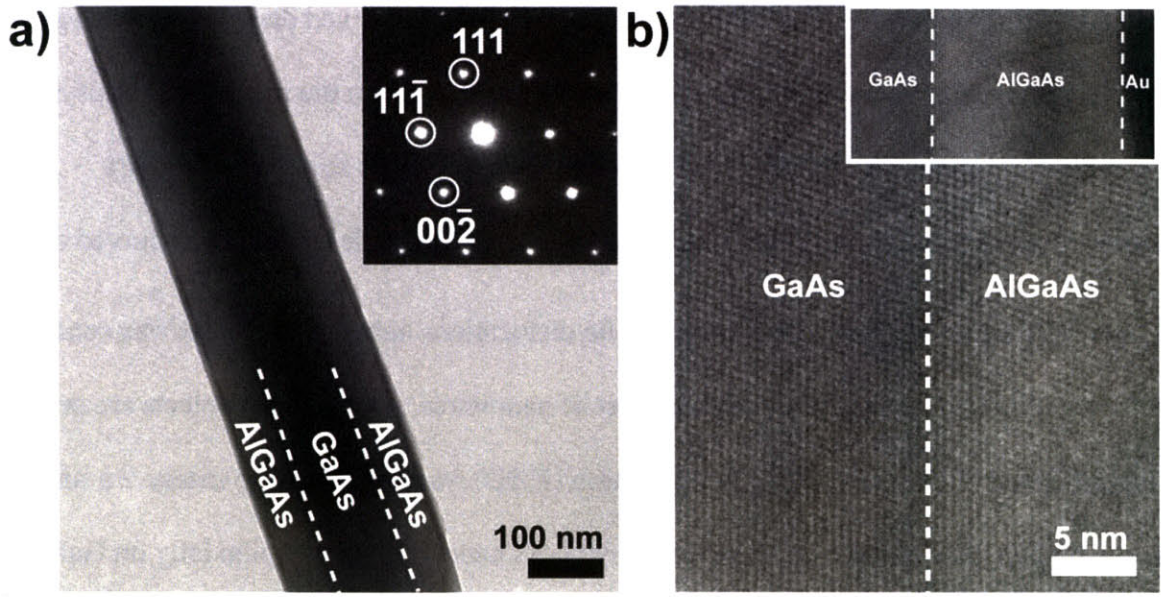


Figure 4-12: a) Bright field TEM micrograph of a core-shell nanowire. Inset is selected area diffraction pattern along <110> direction. b) Lattice-resolved TEM micrograph of GaAs/AlGaAs interface between the GaAs nanowire and the Au seed nanoparticle. Inset is same image at lower magnification showing relative positions of GaAs, AlGaAs, and Au.

Low magnification bright-field TEM images and selected area diffraction patterns, shown in Figure 4-12, reveal the core-shell nanowires have a single crystalline zinc-blende structure, grow along the [111] direction, and are free of structural dislocations. The single crystalline zinc-blende structure and growth direction can be seen from the selected area diffraction pattern shown in Figure 4-12a. The growth direction was determined by indexing the diffraction spots and determining which spot is parallel to the growth direction. As seen in Figure 4-12a, the nanowire grow direction is parallel to the line between the [111] direction and the transmitted beam. This indicates a [111] growth direction.

The presence of structural defects such as a dislocation or twin plane would perturb the symmetry of the crystal and hence create diffraction contrast. The result would be a dark and straight line appearing in the image. Since diffraction contrast can disappear when the sample is tilted to specific high symmetry directions, the samples were tilted over a wide range of angles to

ensure that no dislocations were present. It should be noted that curved dark lines (not shown) were often observed in nanowires and attributed to internal strain in the nanowires resulting from they way they lay on the TEM grid. These contours, also known as strain contours, are commonly observed in nanowires [68] and be distinguished from defects by their curved shape.

Over 25 nanowires were inspected and no dislocations appeared, hence it was concluded that after examining a statistically significant set of nanowires, no structural defects are present. It should be noted that the use of X-ray diffraction (XRD) was considered to measure a much larger set of nanowires. However, these GaAs/AlGaAs nanowires grow epitaxially on GaAs [111]B substrates, which makes dislocation analysis using XRD challenging or impossible; XRD data would be unable to distinguish defects in the nanowires from defects in the GaAs substrate due to the significantly larger (four orders of magnitude) volume of the substrate compared to that of the nanowires.

To investigate the properties of the GaAs/AlGaAs interface, lattice-resolved TEM images were recorded along the AlGaAs growth between the Au seed nanoparticle and the GaAs nanowire core. The TEM investigations suggest epitaxial deposition of AlGaAs, however variations in sample thickness prevent precise characterization of the GaAs/AlGaAs interface using planview TEM. Precise characterization of the core-shell interface is better conducted on cross-sectional TEM samples where the core-shell interface is not buried under the shell and there exist no thickness changes between the core and the shell.

4.4.2 Characterization of core-shell interface

Precise characterization of the core-shell interface was conducted on the cross-sectional TEM sample shown in Figure 4-9. Since imaging was performed using HAADF STEM instead of diffraction contrast TEM, the images are directly interpretable [96]. Moreover, since HAADF

STEM provides sharp chemical contrast and atomic resolution, this method can be used to determine both the coherence and sharpness of the core-shell interface.

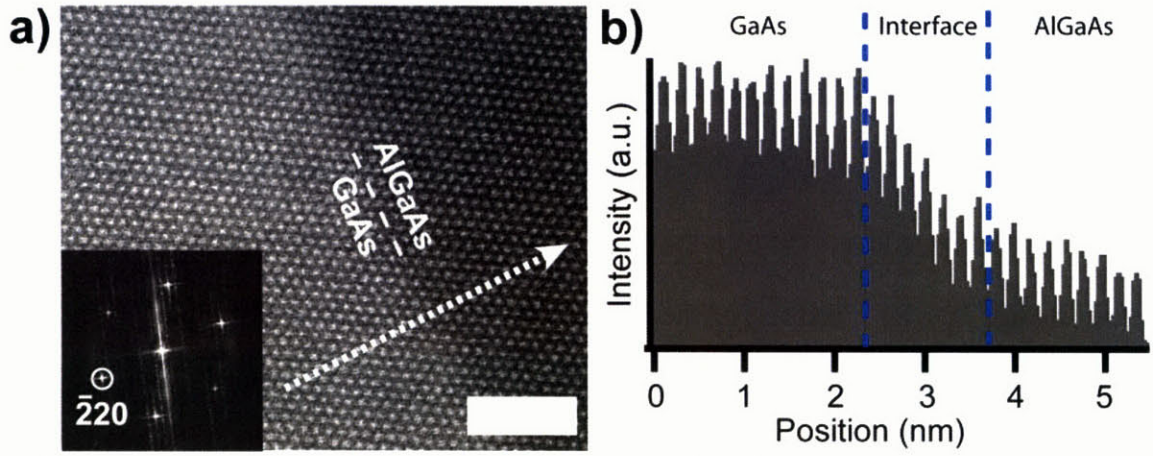


Figure 4-13: a) Lattice-resolve high angular annular dark field STEM image of core-shell interface in cross-section with Fourier transform in inset and b) STEM intensity profile of the core-shell interface along the dashed line in (a). Blue dashed line denotes interfacial region.

Lattice-resolved HAADF STEM images, shown in Figure 4-13a, of nanowire cross-sections obtained along [111] zone axis reveal no distortion from a perfect zinc-blende single crystal. Hence it can be concluded that the shell is epitaxial, defect-free, and atomically sharp in the plane of the cross-section. To quantify the atomic sharpness along the length of the nanowire, the intensity profile of the image was measured and shown in Figure 4-13b. The profile was recorded along the dotted arrow shown in Figure 4-13a. The intensity profile is brightest between $x = 0$ nm and $x = 2.2$ nm, which indicates pure GaAs, and dimmest between $x = 3.6$ nm and $x = 5.4$ nm, which indicates AlGaAs. Between $x = 2.2$ nm and $x = 3.6$ nm, the intensity profile decrease gradually. This gradual decrease can be caused by one of two phenomena. It could be the result of compositional grading at the interface to alleviate the strain caused by the misfit between the GaAs and AlGaAs. Or this gradual decrease can be the result of a core-shell surface roughness. Since the observed intensity is averaged over all of the atoms in the atomic column, it is possible that the region between $x = 2.2$ nm and $x = 3.6$ nm contains both GaAs and AlGaAs.

The limits of the measurement technique make it impossible to distinguish between these two effects.

It is important to note that sidewalls of hexagonal nanowires grown along the [111] direction can belong to either the (110) or (112) families of planes, which can have significant impact on the electronic properties of the core-shell interface. For example, carrier mobilities in the GaAs (110) plane are known to be a factor of ten times greater than in the GaAs (112) plane [97]. From the fast Fourier transform of the lattice resolved images, shown in Figure 4-13, it was determine that the facets are aligned along (110) assuring the potential of these core-shell nanowires for high mobility electronics.

4.5 Summary

The controlled growth of core-shell GaAs/AlGaAs nanowire heterostructures has been demonstrated. The nanowire geometry was shown to be metastable at high temperatures, with morphological evolution occurring if individual nanowires were allowed to come in physical contact with one another. SEM measurements revealed that by growing vertically-aligned nanowires at an aerial density below 1 nanowire/μm^2, the stability of the nanowire geometry was maintained and uniform faceted shells were deposited. EDX analyses confirmed the core-shell morphology and consistently determine the shell to be $Al_xGa_{1-x}As$ with $x = 0.89 \pm 0.03$. Axial uniformity analysis demonstrated the shell to be of constant composition with the shell thickness changing by 2 nm/μm. HAADF STEM and EDX analyses of cross-sectional samples demonstrated the shell composition was the same on all six facets and that the shell thickness changed by less than 2%. A three-dimensional reconstruction of the nanowire provided further evidence of the compositional and morphological uniformity of the nanowires in the axial and radial directions. BF-TEM and lattice resolved HAADF STEM structural analysis demonstrates

the core-shell interface to be epitaxial and atomically sharp. Measuring the intensity of the profile of the HAADF image of the core-shell interface revealed the core-shell interface sharpness to be 1.4 nm, which can be attributed to either compositional grading or core-shell interfacial roughness.

These results demonstrate that core-shell GaAs/AlGaAs nanowires may be fabricated with precise control over morphology, composition, and structure. The control demonstrated over all of these parameters is sufficient enough to be considered candidates for high mobility electronics. While further studies would be needed to provide full quantitative control over nanowire dimensions and composition, the viability of core-shell nanowires for high mobility applications has not yet been demonstrated. The electrical properties of core-shell nanowires must first be investigated to determine if controllable n-type doping is achievable in core-shell nanowires. This is the focus of Chapter 5.

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Chapter 5. N-type doping of GaAs nanowires by the deposition of an n-GaAs shell

The purpose of this chapter is to explain the fundamental solid-state and surface physics involved in n-type GaAs nanowire doping via the deposition of an epitaxial n-GaAs shell. The I-V properties of undoped nanowires were measured and the growth conditions for n-GaAs deposition were designed to minimize the impurity incorporation. GaAs/n-GaAs nanowires demonstrate an unintended rectifying I-V behavior, which was further investigated by a combination of energy dispersive X-Ray spectroscopy, current-voltage measurement, capacitance-voltage profiling, and Kelvin probe force microscopy. A model of Au diffusion and charge depletion was proposed to explain the observed rectification. Utilizing this model, non-rectifying n-type GaAs/n-GaAs nanowires were realized by removing the Au seed nanoparticle prior to shell deposition. The electrical properties of these n-type nanowires were characterized and a model to predict the conductivity of GaAs/n-GaAs nanowires including the effects of Fermi level pinning is presented.

5.1 Nanowire Electronic Properties

While proof-of-concept nanowire transistors [24, 98], light emitting diodes [25], and lasers [27, 99] have been demonstrated, the viability of Au-grown nanowire devices requires controllable doping in nanowire systems. To determine a promising approach to doping in GaAs, it is important to examine the body of published work on nanowire wire doping.

5.1.1 A review of nanowire doping

An increasing body of evidence now suggests that controllable doping is achievable in certain nanowire systems with varying degrees of difficulty. Co-introducing dopant precursor during the VLS growth has realized n- and p-type doping in silicon [24, 100, 101], germanium [102, 103], and indium phosphide [104] nanowires. Since the co-introduction of dopant precursor during the VLS growth requires no additional processing steps, it is the most desirable method to dope nanowires.

Attempts to dope GaAs by co-introduction of dopant precursors have highlighted the specific challenges to doping GaAs. Co-introduction of zinc precursor has yielded controllable p-

type doping [105]. However, examination of the diameter dependence on the nanowire resistance revealed that a minimum nanowire radius of 80 nm was needed to achieve p-type doping at a concentration of 10^{18} cm^{-3} in a GaAs nanowire. Exposed GaAs surfaces possess a substantial density of midgap surface states that trap free carriers and create a surface depletion layer. This phenomenon is referred to as Fermi level pinning and is well documented, particularly in literature concerning contact formation to GaAs [106]. While this phenomenon is documented in both p-GaAs and n-GaAs, it is known to be more significant in n-GaAs [106].

Currently, only two reports of n-type Au-grown GaAs nanowires exist, but neither demonstrates controllable n-type nanowire growth. In the first report, n-type doping was unintentionally achieved[6] and the gate response measurements demonstrated substantial charge trapping [107] indicative of surface pinning. In the other report, n-type doping was achieved using co-introduction of tellurium in MBE grown GaAs nanowires [30], however it was noted that doping was achieved at a temperature of 550°C. At this temperature, growth does not occur exclusively via the VLS mechanism and the observed tapering rate (section 3.3.1) was greater than 200 nm/μm. Though this growth temperature was not justified by the authors, recent theoretical work has calculated that the incorporation of dopant increases exponentially with growth temperature [108], so the most likely explanation for this growth temperature was to increase the incorporation of tellurium dopant in the GaAs nanowire. These results suggest that doping by co-introduction of doping precursor during VLS growth can be achieved, but has an adverse impact on the nanowire morphology. This result is in agreement with recent results on selective area epitaxy grown GaAs nanowires [109].

[6] The authors of that work attribute the unintentional doping to carbon background doping, but comparison with the results of this thesis suggests that the use of a silicon substrate allowed silicon to diffuse from the substrate into the nanowire.

An alternate approach to achieving n-type doping is the deposition of an epitaxial shell. With an epitaxial shell, free carriers can be provided either conduction band discontinuity [8, 110] at a core-shell heterointerface or by doping the shell [111]. Initial studies into the electrical properties of the core-shell GaAs/AlGaAs nanowire heterostructures presented in Chapter 4, however, revealed no significant increase in current resulting from the presence of a heterointerface suggesting the deposition of an epitaxial doped shell (hereafter referred to as shell doping) was required. Shell doping has been demonstrated to be an effective method of p-doping in InAs nanowires [111], which is significant because both InAs and GaAs are well-documented to experience Fermi level pinning [106].

5.1.2 Shell doping process

Shell doping, is essential to the development of devices based on radial nanowire heterostructures [81]. The process to deposit an n-type GaAs, illustrated in Figure 5-1, was virtually identical to the core-shell nanowire growth process presented in Chapter 4.

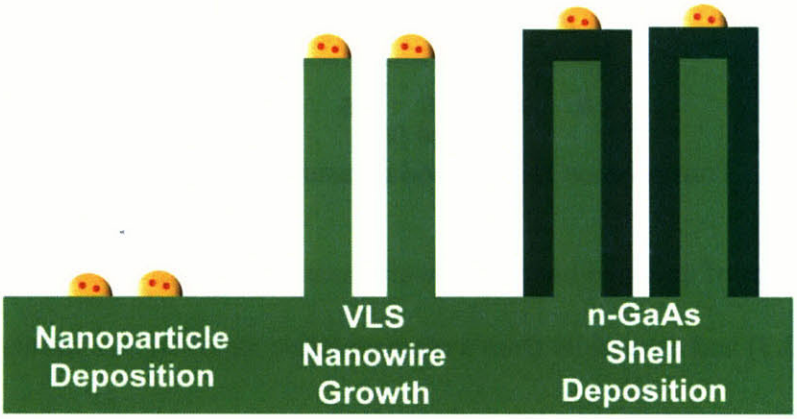

Figure 5-1: Schematic of shell doping process

First, Au seed nanoparticles were deposited on the substrate from colloidal solution. Next, a GaAs nanowire was grown via the VLS mechanism at 420°C to promote anisotropic

axial elongation of the nanowire. Finally, the temperature was increased above 650°C and a doped shell was deposited by co-introducing silane, arsine, and trimethylgalium.

5.1.3 IV properties of undoped GaAs nanowires

Individual nanowires were deposited on Si/SiO_2 substrates and Ohmic Ni/Ge/Au/Ge/Au (25/25/150/25/150 nm) multilayer contacts were deposited using aligned electron beam lithography and physical vapor deposition, as described in Section 2.3.2. To ensure the contacts maintained conformity on the nanowire sidewalls, the metallization thickness was always greater than the radius of the nanowire. The minimum line width written was always twice the metallization thickness to ensure successful liftoff. Further optimization of the contacting process may enable the deposition of smaller contacts.

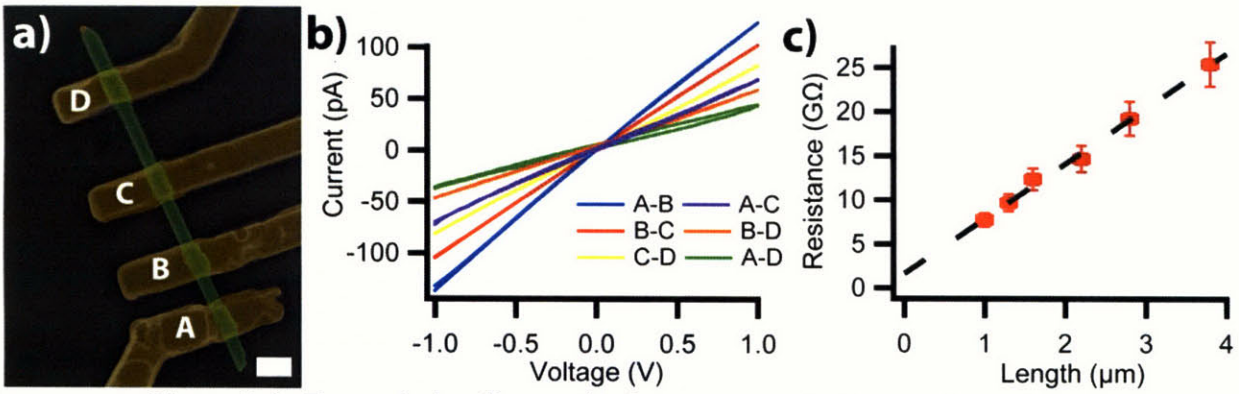

Figure 5-2: Transmission line method measurement of nanowire resistance

The resistances of undoped nanowires were measured by the transmission-line-method (TLM) (Section 2.3.3) and the results from a representative nanowire are shown in Figure 5-2. The measured resistances exhibited a linear dependence contact separation, l, with R_C = 800 MΩ and an observed conductivity of 5.2 x 10^{-5} Ω-cm as calculated from the TLM measurements according to Equation (5-1).

$$\sigma = \frac{1}{R/l \, A_{cross\,section}} = \frac{8}{3d^2 R/l \sqrt{3}} = e\mu N \tag{5-1}$$

Here d is the nanowire diameter as measured by SEM, R/l is the resistance per length as determined by a linear fitting of the resistance versus length plot shown in Figure 5-2c, e is the charge of single electron, μ is the carrier mobility, and N is the charge carrier density. Based on similar reports of undoped GaAs thin films grown by atmospheric pressure MOCVD [112], the carrier mobility was assumed to be 2000 $cm^2/V\text{-}s$. Given that nanowires are grown by a different growth mechanism, the assumed electron mobility must be considered a rough estimation.

Based on this analysis, the carrier concentrations of undoped nanowires were found to be in the range of 10^{10} - 10^{12} cm^{-3}. These values are between two and four orders of magnitude higher than the intrinsic carrier concentration of 10^8 cm^{-3} [112]. The precise source of conduction electrons could not be determined. However, it was noted that the measured resistance of a nanowire would be greater six months after device fabrication than immediately after device fabrication, which would suggest that surface chemistry strongly influences nanowire conductivity. Because, the measured carrier concentrations are too low for functional devices [56, 113], investigations were made into doping GaAs nanowires via the deposition of an n-GaAs shell on an undoped VLS grown nanowire core. Since a current density greater than 0.1 mA/cm^2 is needed for functional devices [113], the deposition of an doped shell needed to increase the net conductivity of the nanowire at least five orders of magnitude.

5.1.4 Determination of growth conditions

The growth conditions for an n-GaAs shell were modeled after the optimized growth conditions for AlGaAs shell deposition, presented in section 4.1.3. This consisted of a growth temperature of 700°C, total group III flow of 0.23 sccm, and a V/III ratio of 200. A IV/III ratio

of 1/8 was selected to achieve a silicon incorporation of 10^{18} cm^{-3} based on previous results on the same reactor [50]. To determine the concentrations of impurities, an n-GaAs/n-AlGaAs thin film heterostructure was grown under the same conditions with a growth time of 5 min and the compositions were measured by secondary ion mass spectroscopy.[7]

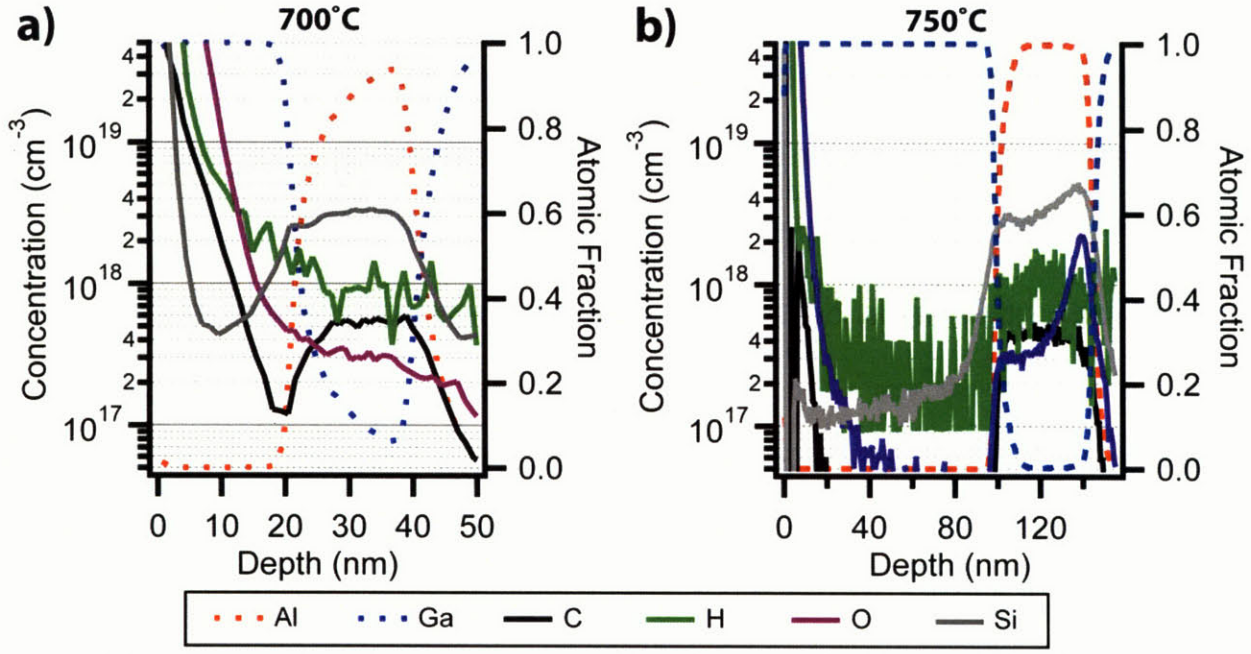

Figure 5-3: Secondary Ion Mass Spectroscopy data for n-GaAs/n-AlGaAs thin-film growth a) 700°C and b) 750°C

The composition of a doped thin-film GaAs/AlGaAs multilayer grown at 700°C is shown in Figure 5-3a. As expected, the predominant impurity was silicon, but the presence of carbon, oxygen and hydrogen was noted. Being a group IV element, silicon is an amphoteric dopant, which means that silicon can form substitutional defects by occupying either a Ga or As lattice site. However, the energy required for Si to occupy a Ga site is known to be lower than the energy for Si to occupy an As site, hence silicon is almost exclusively an n-type dopant [114]. The amphoteric behavior of silicon is only observed when the concentration of silicon atoms occupying Ga sites exceeds 10^{19} cm^{-3} [115].

[7] Data collected by EAG Labs Inc.

The presence of carbon, oxygen, and hydrogen impurities are also noted. Being a group IV element, carbon is also an amphoteric dopant, but unlike silicon, the energy required for carbon to occupy a gallium site is almost equal to the energy required to occupy an arsenic site [115]. Therefore, in the presence of high concentrations of n- or p-type extrinsic doping, carbon will tend to form acceptor or donor-like impurity states to counteract the effect of the extrinsic doping. Oxygen is also electrically active in GaAs and known to oppose n-type silicon doping by forming [Si-O] complexes [116] as well as trap free carriers by forming a wide variety of Ga and hydrogen containing complexes [117]. Hydrogen incorporation has been documented to not significantly impact the electronic properties of GaAs. Since the atomic radius of hydrogen is one third that of gallium or arsenic, hydrogen incorporates into GaAs an as electrically inactive interstitial defect.

Hence, to achieve n-type doping in GaAs, growth parameters must be designed to minimize the concentrations of oxygen and carbon impurities. Previous results [50] on the same MOCVD reactor indicated that the oxygen incorporation can be reduced by increasing growth temperature to 750°C. The composition of a doped thin-film GaAs/AlGaAs multilayer grown at 750°C with all other growth parameters identical to sample shown in Figure 5-3a is shown in Figure 5-3b. The sum of concentrations of oxygen and carbon impurity was less than 10^{17} cm^{-3}, while the silicon doping level was greater than 10^{17} cm^{-3}. These data demonstrate that growing n-GaAs at a temperature of 750°C and targeting a silicon concentration between 10^{17} and 10^{18} cm^{-3} will ensure a sufficient concentration of electrically active silicon to overcome the auto-compensating effect of oxygen and carbon impurity. It should be noted that n-type doping may be possible at 700°C if other parameters are adjusted, but a full investigation of parameter space was not investigated.

5.2 *The adverse effect of Au on n-type doping*

The doping of GaAs nanowires via the deposition of an n-type epitaxial shell was attempted by depositing an n-GaAs shell on a VLS-grown GaAs nanowire at 750°C with a targeted carrier concentration of 10^{18} cm^{-3}. For comparison, a thin-film was deposited under identical conditions to highlight the specific challenges of doping in nanowires.

5.2.1 Unintended electrical rectification in nanowires

In order to compare doped shell deposition with doped thin-film deposition, the VLS nanowire growth and shell deposition were performed in separate growths. First, vertically-aligned GaAs nanowires were grown from colloidal Au according to the recipe presented in Section 4.5. Then, the growth chamber was opened, a semi-insulting GaAs (100) substrate was inserted, and the growth chamber was resealed for n-GaAs deposition. The purpose of the GaAs (100) sample was to serve as a control for nanowire shell deposition and to test if the growth conditions designed in Section 6.01 yield reproducible n-type GaAs material.

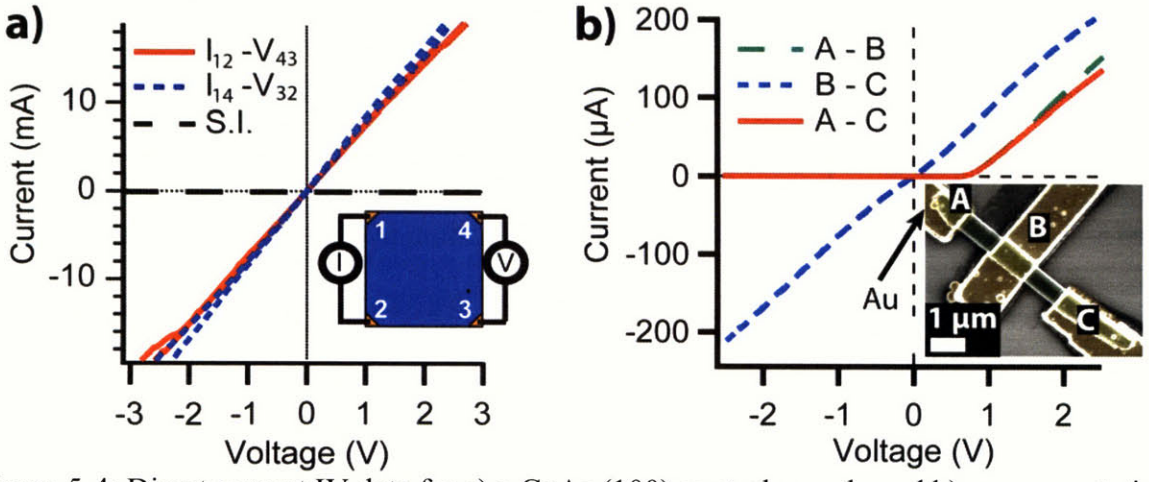

Figure 5-4: Direct current IV data for a) a GaAs (100) control sample and b) a representative GaAs/n-GaAs core-shell nanowire with false-colored SEM of shell contacted nanowire.

The IV data for the GaAs (100) control sample and a representative GaAs/n-GaAs core-shell nanowire are shown in Figure 5-4. The control thin film sample shows Ohmic behavior and

an increase in conductivity of five orders of magnitude as compared to the semi-insulating wafer, as shown in Figure 5-4a. The sheet resistance of the n-GaAs thin film was calculated to be 680 Ω/□ using the Van der Pauw equation (Section 3.3.3). This resistivity corresponds to a carrier concentration of 3.1×10^{17} cm^{-3} assuming a carrier mobility of 2000 $cm^2/V \cdot s$. Hence, the growth conditions produce n-GaAs material with properties close to the predictions of Section 5.1.4.

In contrast to the homogeneous doping observed in the control thin film sample, the IV properties of the GaAs/n-GaAs core-shell nanowire varied along the axial length of the nanowire. Away from the Au nanoparticle, the nanowire exhibited Ohmic conduction with a conductivity six orders of magnitude greater than undoped nanowires (Section 5.1.3); this is consistent with n-type doping. Assuming a mobility of 2000 cm^2/V-s, the carrier concentration between contacts B and C can be estimated as 7.9×10^{17} cm^{-3}. This value is over twice as large as the value measured in the thin-film control, which is most likely the result of the Au nanoparticle assisting the decomposition of silane. However, an unexpected rectification behavior with a built-in voltage around 0.6 V appeared near the Au nanoparticle. As shown in Figure 5-4, this behavior appeared on all measurements involving contact A, which contacts the nanowire near the Au nanoparticle. It should be noted that near the Au seed particle, the shell thickness decreases, as seen in the SEM micrograph in Figure 5-4b. Therefore, to ensure that variations in shell thickness were not the cause of the observed rectification, contact A was designed to extend far enough past the Au nanoparticle so as to contact the shell at its largest thickness. To ensure this rectification behavior was not an anomaly, more than 20 doped-shell nanowires were measured and all nanowires exhibited rectifying behavior with directionality determined by the position of the Au nanoparticle and a turn-on voltage of approximately 0.6 V.

5.2.2 Characterization of rectification & estimation of band structure

In order to better understand the rectifying behavior observed in Figure 5-4 and distinguish the electrical properties of the nanowire from contact effects, a combination of I-V and capacitance-voltage (C-V) profiling was utilized. A rectifying circuit element can be approximated as a diode, which possesses a leakage current I_0, an ideality factor n_0, and a built-in voltage V_{bi}. The current of a diode increases exponentially with applied voltage, as shown in Equation 5-2, such that the logarithm of the current increases linearly with applied voltage.

$$\ln(I) = \ln(I_0) + \ln\left(e^{qV/n_o kT} - 1\right) \approx \frac{qV}{n_o kT} + \ln(I_0) \tag{5-2}$$

When plotting the I-V behavior on a semi-log plot, the measured slope can be used to determine the diode ideality factor and the $V = 0$ intercept can be used to determine the diode leakage current. Moreover, the capacitance of a diode will vary with applied voltage, as shown in Equation 5-3, such that the inverse squared capacitance is found the decrease linearly with voltage. When plotting $1/C^2$ versus applied voltage, the $1/C^2 = 0$ intercept can be used to determine the diode built-in voltage.

$$\frac{1}{C^2} \propto (V - V_{bi}) \tag{5-3}$$

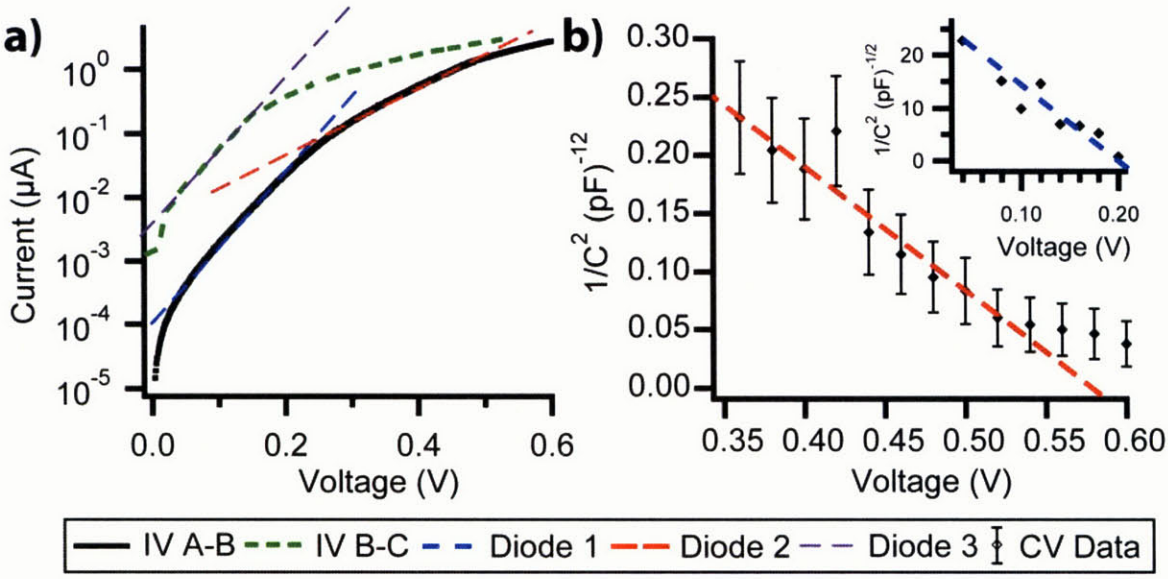

Figure 5-5: Electrical characterization between contacts A & B showing a) direct-current I-V behavior and b) C-V profiling using an AC bias of 500 mV at 1kHz. Inset is same data in a different voltage region and scaled accordingly.

The dc I-V curve and ac C-V curves between contacts A and B are shown in Figure 5-5. Rectifying circuit elements were identified by noting the presence of linear regions in both the I-V and C-V data at similar voltage regions[8]. This comparative analysis suggested the presence of two rectifying circuit elements between contacts A and B. The first rectifying element between contacts A and B, referred to as diode 1, is dominant from $0 < V < 0.20$ V. This diode is noted in the I-V and C-V data as the blue dashed line in Figure 5-5. From the I-V data this diode could be modeled with a leakage current $I_1 = 1.2 \times 10^{-4}$ μA and an ideality factor $n_1 = 1.4$. This diode was also observed in the C-V data, (located in the inset of Figure 5-5b) with a measured built-in voltage of 210 ± 10 mV. The second rectifying element between contacts A and B (labeled diode 2) appears dominant in the range of $0.25 \text{ V} < V < 0.45$ V. This diode is noted in the I-V and C-V data as the red dashed line in Figure 5-5. From the I-V data this diode could be modeled with a leakage current $I_2 = 1.8 \times 10^{-3}$ μA and an ideality factor $n_2 = 2.4$. This diode was also observed

[8] The "apparent" turn-on voltage in the I-V data will be less than the built-in voltage measured in the C-V data due to the nanowire resistance I-V data dominating the I-V behavior when the diode is nearly "on".

in the C-V data, (located in the inset of Figure 5-5b) with a measured built-in voltage of 580 ± 20 mV.

Close inspection of the I-V data between contacts B and C suggested the presence of one rectifying circuit element, labeled diode 3 in Figure 5-5a. Diode 3 was noted to have the same ideality factor (1.4) as the first diode (diode 1) observed between contacts A and B. Moreover, both diodes exhibit very similar built-in voltages of approximately 0.2V. The only difference between the two rectifying circuit elements was that the leakage current of diode 3 (2.6×10^{-3} μA) was 20 times greater than the leakage current of diode 1 (1.2×10^{-4} μA).

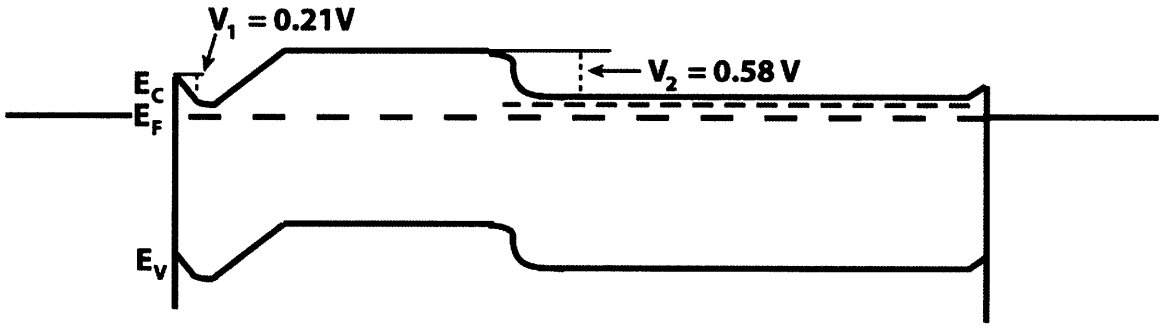

Figure 5-6: Proposed band structure of GaAs/n-GaAs nanowire between contacts A and B.

The built-in voltage of 0.58V observed in Figure 5-4 is not consistent with the presence of an Au-GaAs Schottky contact, since the Au-GaAs barrier height is known to be 0.9 V [118]. Instead, the observed rectifying behavior can be explained by the existence of an axial segment in the GaAs nanowire, in which the Fermi level is pinned midgap, as shown in Figure 5-6. In this case, the built-in voltage of diode 2, 0.58 V, should be equal to the difference between the conduction band of the GaAs under contact A and contact B. As the measurement between contacts B and C in Figure 5-4 demonstrates, the nanowire is doped under contact B, so the Fermi level can be approximated as $E_F = E_V + 1.42$ V under contact B, the level of the silicon

donor state in GaAs. Therefore, the Fermi level under contact A is 0.58V further from the conduction band, which is $E_F = E_V + 0.84$ V.

If diode 2 is caused by an energy barrier contained within the nanowire, then it can be hypothesized that both diode 1 and diode 3 were caused by the annealed NiGeAu contacts. Both diodes exhibited similar ideality factors and built-in voltages. Moreover, it is well-documented that annealed NiGeAu contacts are thermionic contacts with an energy barrier width that decreases when the donor level of the GaAs increases [106]. Hence, the decreased leakage current of contact A (diode 1) versus contacts B and C (diode 3) would indicate that the Fermi level must be further from the conduction band under contact A than under contacts B and C. These features are included in the band diagram shown in Figure 5-6. It should be noted that the band diagram shown in Figure 5-6 is estimated since the precise concentrations and spatial distributions of Si, Au, and Ge (from the NiGeAu contact) impurities could not be measured.

In this model the impedance of diode 1 was assumed to be zero above 0.2V. There could, however, exist a voltage drop across contact A above 0.2V. In this case, the energy barrier in the nanowire would be less than 0.58V. Therefore, the Fermi level under contact A is estimated to be 0.89 ± 0.05 eV above the valence band. Moreover, while this model is consistent with the I-V data, C-V data, and published literature on NiGeAu contacts; there may exist other models capable of explaining the data. Rectifying contacts have been documented to create multiple diodes with different ideality factors [56]. Therefore, to explore whether the observed energy barrier, measured as diode 2, is contained within the nanowire itself and is not somehow an artifact of the contacts, a simple Kelvin probe force microscopy measurement (KPFM) was performed.

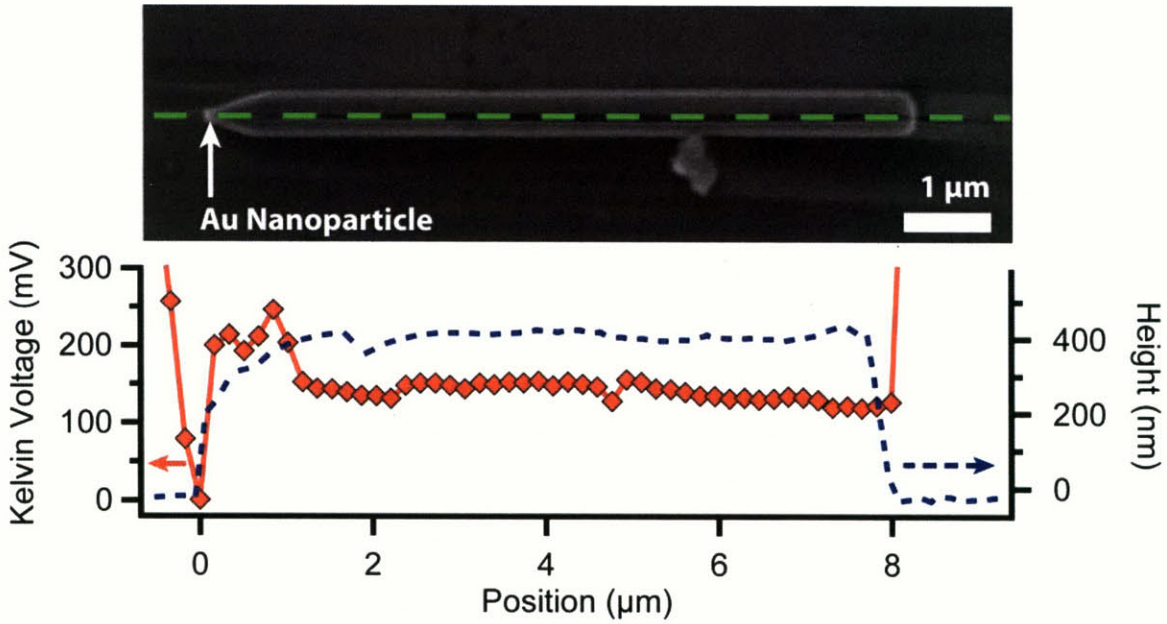

Figure 5-7: Kelvin probe force microscopy of a representative nanowire along the dotted green line pictured in the corresponding SEM image. The red diamonds with connecting line are measured Kelvin potential, normalized to value of the Au nanoparticle and the blue dashed line is the nanowire height profile.

KPFM utilizes a conductive AFM tip to measure the surface potential of a sample, which would experience a steep change in the presence of a diode-like energy barrier. Since the tip is maintained a constant height above the surface[9], the measured potential will not depend on variations in sample height. The measured Kelvin potential, AFM height profile and SEM image of a representative nanowire is shown in Figure 5-7. The positions and voltages measured were taken relative to the position and measured potential of the Au seed nanoparticle. Examination of the Kelvin potential indicates the presence of a diode-like energy barrier along the length of the nanowire. The first region, located from x = 0.1 - 1.2 µm (here x is defined as distance from the Au nanoparticle along the length of the nanowire), exhibits a Kelvin potential of 220 ± 30 mV. The second region, located from x = 1.2 µm – 8.3 µm, exhibits a Kelvin potential of 160 ± 20 mV. These results indicate the presence of a potential difference, ΔV_K, of 60 ± 30 mV at x = 1.2

[9] The measurement is performed in tapping mode so the tip height oscillates, however the minimum separation between tip and sample during each oscillation is held constant.

± 0.2 μm. The measured Kelvin potential difference of 60 ± 30 mV is comparable to a reported conduction band difference of 85 ± 5 mV across a *p-i* junction in a GaAs nanowire for which the difference in Fermi level was estimated to be 0.7 V [119]. It should, however, be noted that the Kelvin potential was performed in ambient atmosphere, which may affect the value of the measured voltage [64]. Since the surface chemistry of the nanowire could not be controlled in our experimental measurement, precise quantification of the measured Kelvin potential was not attempted.

Both I-V and C-V measurements revealed the presence of two diode-like energy barriers in the conduction path. Both diode-like energy barriers agree with a model of an axial nanowire segment with the Fermi energy located 0.89 ± 0.05 eV above the valence band. This finding is in accordance with Kelvin probe force microscopy, which confirms the presence of an axial segment with Fermi energy lower pinned midgap. To explore the physical cause of this axial segment, compositional analysis by energy dispersive X-ray spectroscopy was conducted near the Au seed nanoparticle.

5.2.3 Direct observation of Au diffusion in the GaAs nanowire

To understand why rectification always occurred near the Au nanoparticle, the composition profiles of shell-doped nanowires were measured by EDX. EDX is able to detect the atomic composition of a material to an accuracy of approximately 1% by measuring the X-rays produced from electronic transitions of inner core electrons. The sensitivity of this measurement is limited by background noise and X-ray absorption in the material. EDX is sensitive enough to observe compositional differences in a sample, but not sensitive enough to detect impurity doping directly.

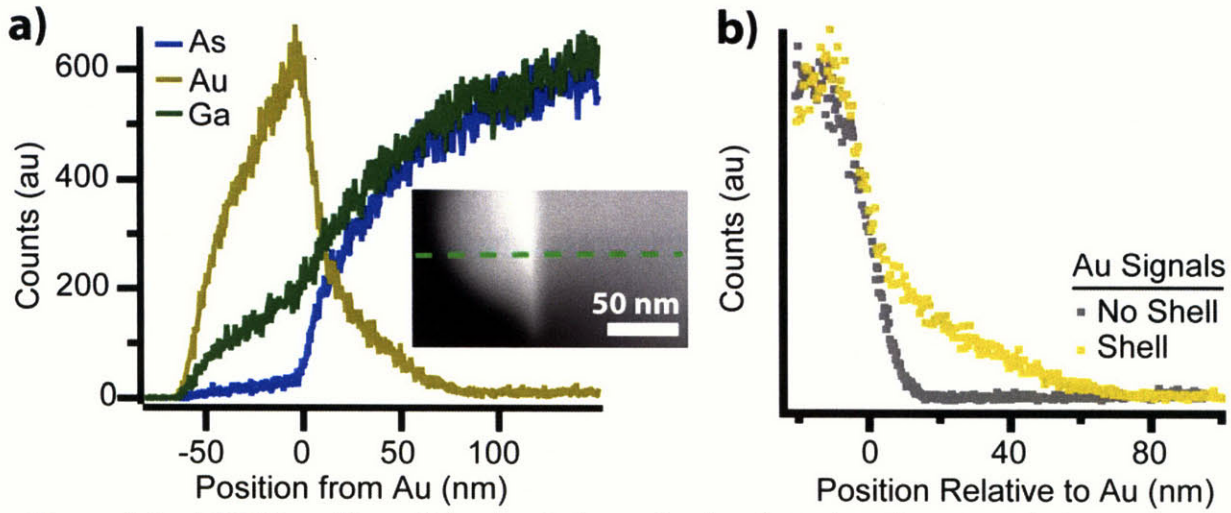

Figure 5-8: a) EDX profiles of Ga, As, & Au at the Au-GaAs interface. Inset is STEM image with linescan shown as the green dashed line b) Comparison of Au EDX signal in a doped shell versus undoped nanowire. The signals were normalized to their maximum Au count.

The EDX data from a representative nanowire are shown in Figure 5-8a. The Au EDX signal shows a distinct diffusion tail with Au EDX signal detectable as far as 90 nm away from the Au-GaAs interface. This distance is too large to be attributable to beam broadening effects or other artifacts of the measurement. Moreover, the behavior of the gallium and arsenic profiles indicate that the EDX signal is accurately measuring the compositional profile. It has been reported that when GaAs nanowires are annealed, gallium (soluble in gold) diffuses into the gold nanoparticle, while arsenic (not soluble in gold) does not [120]. The arsenic signal falls steeply to zero at the Au-GaAs interface, whereas the gallium signal penetrates the entire length of the Au nanoparticle. To identify when during the growth process the observed Au diffusion occurs, VLS-grown GaAs nanowires also underwent similar analysis. A comparison of the gold profile in nanowires with and without an n-GaAs shell, as shown in Figure 5-8b, reveals that the Au EDX signal of a the core-shell nanowire extends five times as deep as the undoped nanowire, which proves that the observed diffusion occurred during the shell deposition.

5.2.4 Discussion

Based on these results, it can be concluded that during the high temperature shell deposition step, Au diffuses from the Au seed nanoparticle creating a segment of the GaAs nanowire with Fermi energy pinned at $E_V + 0.84$ eV. The segment with lower Fermi energy creates a conduction band barrier equal to the difference in the Fermi level, 0.58 V. Moreover, the reduced Fermi level in the GaAs near the Au increases the energy barrier of the NiGeAu, making the thermionic nature of the contact more pronounced. This model agrees with the EDX, IV, CV, and Kelvin probe measurements and confirms that the presence of Au at 750°C prevents the fabrication of a uniform n-GaAs nanowire. It should be noted that the only intentional n-type doping in GaAs nanowires published were grown by gas source molecular beam epitaxy at a temperature of 550°C [30]. It is possible that this result was achieved because the growth temperature of 550°C is too low to observe significant diffusion of Au or to make diffused gold electrically active in GaAs.

There are two possible explanations for the observed Fermi level pinning at $E_V + 0.84$ eV: the gap states are either gold-induced (gold impurities are creating midgaps states), or the gold is creating a small degenerately doped p-type region and the observed midgap states are intrinsic GaAs defect states located in the diode depletion region.

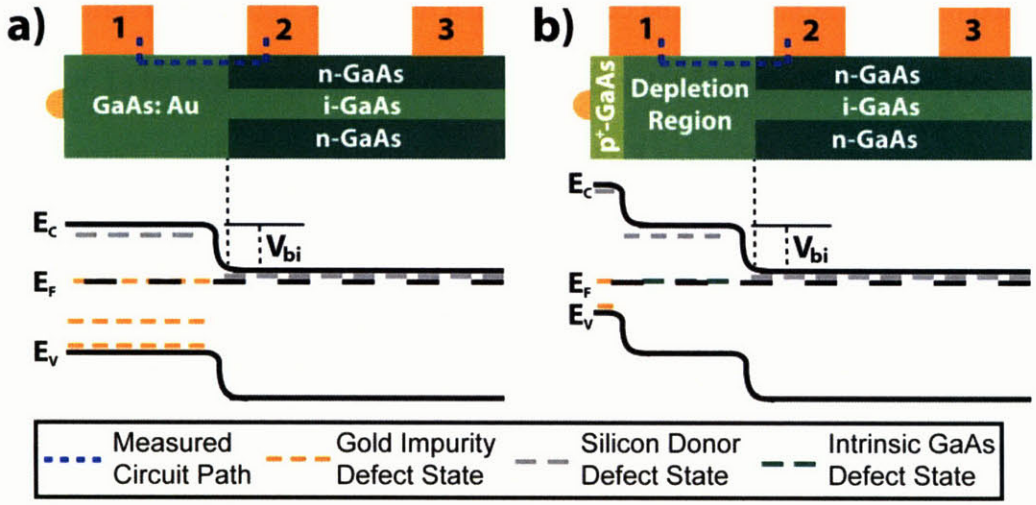

Figure 5-9: Proposed models for rectification. a) Au diffusion creates midgap states with observed rectification between Si- and Au-doped segments. b) Au diffusion creates degenerately p-doped region with observed rectification between the n-GaAs and diode depletion region.

The case where Au is creating midgap states is illustrated in Figure 5-9a. Gold has been reported to create an acceptor at $E_V + 0.04$ eV and a deep trap at $E_V + 0.40$ eV in GaAs [121, 122], however the properties of all electronically active gold-related defects in GaAs are not fully understood. The existence of an Au-Ga complex state at $E_V + 1.07$ eV has been proposed [123] and other midgap states related to Au may exist, which pin the Fermi level near the measured value of $E_V + 0.84$ eV.

The case where Au creates a degenerately p-doped region and the observed midgap states are intrinsic defects in the diode depletion region is illustrated in Figure 5-9b. GaAs possesses midgap surface state in the range of 0.7 eV - 0.9 eV above the valence band. Given the increased surface-to-volume ratio of the nanowire geometry and the depletion of free carriers due to the p^+-n junction, the Fermi level could be pinned at the value of the fixed surface potential. On the other hand, intrinsic point defects such as gallium vacancies (E3, located at $E_V + 1.10$ eV [124, 125]) and arsenic antisite defects (EL2, located at $E_V + 0.83$ eV [5, 126, 127]) are known to be electronically active. If the diffusion current of Au into the GaAs nanowire is matched by

diffusion of gallium into the gold, the density of Ga vacancies and As antisite defects would be greatly increased. Since the EL2 is at a lower energy than the E3 level, the Fermi level would be pinned at the EL2 level of $E_V + 0.83$ eV.

Precise determination of the density of origin of the midgap states would require deep level transient spectroscopy studies performed on shell-doped nanowires grown under various growth conditions and measured under various external stresses to determine the variation of the defect level with stress [127, 128]. Moreover, the extent and spatial uniformity of the diffused gold within the nanowire would need to be precisely measured to determine if the extent of the pinned segment exceeds the extent of the Au diffusion. Future work will focus on more precise measurement such as local electron atom probe (LEAP) microscopy, and efforts are underway to gain access to a LEAP microscope at Oak Ridge National Laboratires. Since, however, the results of Chapter 4 indicate that shell deposition must be conducted above 650°C to achieve epitaxy in MOCVD-grown core-shell GaAs nanowire, it can be concluded that regardless of what specific point defect pins the Fermi level at $E_V + 0.84$ eV, the fabrication of a uniform n-GaAs nanowire – the objective of this chapter – requires the removal of Au prior to shell deposition.

5.3 Realization of n-type GaAs nanowires via Au removal

The electrical properties of GaAs/n-GaAs nanowires with and without the presence of the Au nanoparticle were compared to provide final proof of the adverse effect of Au on n-type doping in GaAs nanowires and to fabricate a uniform n-type shell doped GaAs nanowire. It should be noted that the Au seed particle has no function during shell deposition. Its function is strictly to seed VLS nanowire growth, so the Au nanoparticle was removed immediately following nanowire growth.

5.3.1 Electrical properties of Au-removed doped shell nanowires

One method for removing gold in GaAs commercial applications is immersion in triiodide solution (commonly referred to as TFA solution). Utilizing TFA etchant to remove the Au seed nanoparticles has been shown in Ge nanowires [129] and proven compatible with the shell deposition process [130].

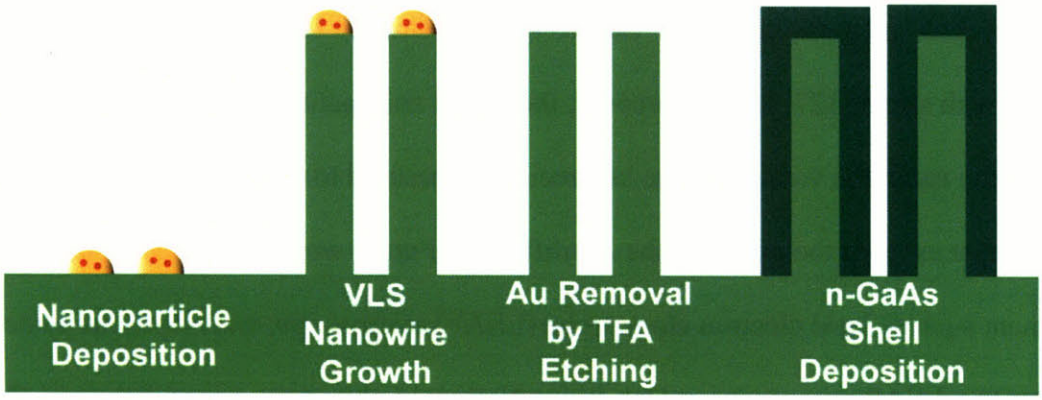

Figure 5-10: Schematic of modified shell doping process including TFA etching process.

A modified shell doping process, shown in Figure 5-10, was developed and the effect of gold on the electronic properties of GaAs/n-GaAs nanowires was tested as follows. Vertically-aligned GaAs nanowires were grown from colloidal Au on two samples according to the recipe presented in Section 4.05. The two substrates were removed from the growth chamber. One sample was immersed in commercially available TFA etchant for 5 sec and rinsed in deionized water for thirty seconds. The other control sample was not immersed in TFA etchant, but still rinsed in DI water for thirty seconds. Both samples were then reinserted for n-GaAs deposition.

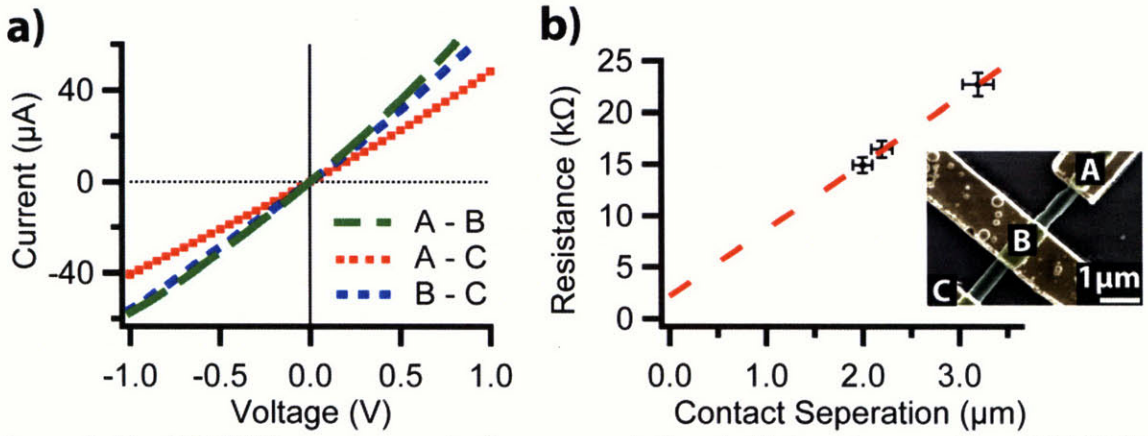

Figure 5-11: a) DC IV measurement of a representative shell-doped nanowire and b) TLM measurement of resistance versus length. Inset is false-colored SEM of contacted nanowire.

The IV behavior of a representative shell doped nanowire produced after Au removal is shown in Figure 5-11a. The nanowires were contacted using the same three-point scheme as the nanowires exhibiting rectifying behavior. The nanowires that were immersed in triiodide solution exhibited linear Ohmic behavior across all contacts. The nanowires not immersed in triiodide solution exhibited the same rectifying properties exhibited in Figure 5-4, proving that the presence of Au during the high temperature shell deposition step causes rectifying behavior and that removing Au prior to shell deposition enables the fabrication of uniform GaAs/n-GaAs nanowires.

Quantification of the conductance was conducted by transmission-line-method measurements, as shown in Figure 5-11b. The measured resistances exhibited a linear dependence contact separation, l, with $R_C = 2.17$ kΩ and $R/l = 6.42$ kΩ/μm, which corresponds to an observed conductivity 29.9 Ω-cm. This conductivity is six orders of magnitude greater than the conductivity measured for the undoped nanowire, which indicates successful doping.

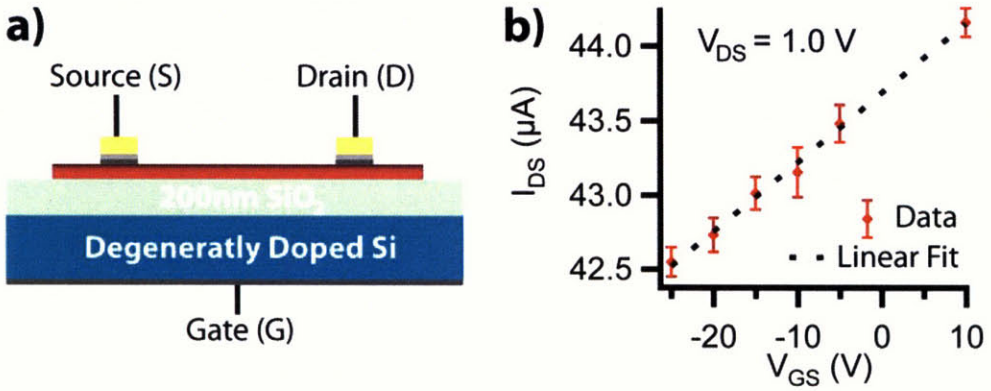

Figure 5-12: a) TLM determination of nanowire and contact resistance and b) back gated IV of the nanowire shown in Figure 5-11 between A-B showing n-type conduction. Error bars are difference between forward and reverse sweep opf source-drain voltage.

That the conduction in the shell doped nanowires was n-type was confirmed by applying a voltage on the backgate and measuring the effects on the net conductivity, as illustrated in Figure 5-12a. Application of a backgate voltage effectively modulates the electron charge in the nanowire through field effect. Using this setup, the carrier sign and mobility in the nanowire can be estimated by measuring the effect of varying the gate voltage on the source-drain current was measured on the nanowire. For each point, the gate voltage was held constant, while the source-drain voltage was swept from 0V to 5V then back to 0V. The average values are plotted in Figure 5-12b, with the error bars defined by the difference in the forward and reverse source-drain voltage sweep. The change in source-drain current with gate voltage, dI_{DS}/dV_{GS}, was measured to be +0.045 μA/V at an applied voltage of 1.0 V. The fact that the source-drain current increases with applied back gate voltage proves that removal of the Au nanoparticle prior to shell deposition enables n-type doping via the deposition of an n-type epitaxial shell. The carrier mobility can be estimated to be 30 cm^2/V-s, from the measured value of dI_{DS}/dV_{GS} according to Equation 5-4.

$$\mu = \frac{dI_{DS}}{dV_G}\frac{L^2}{I_D C_G} = \frac{dI_{DS}}{dV_G}\frac{2t_{ox}L}{I_D \varepsilon_{SiO_2}\varepsilon_0 d} \tag{5-4}$$

Here, it is assumed that the gate capacitance is a layer of silicon dioxide with a thickness of t_{ox} and a dielectric constant of ε_{SiO_2}. The nanowire is assumed to have a hexagonal cross-section with one facet, *d/2* wide and *L* long, in contact with the oxide. This value is much less than the assumed mobility of 2000 cm^2/V-s. Examination of multiple wires found variation in the measure mobility in the range of 30 – 70 cm^2/V-s. Based on this measurement, the estimation of carrier concentration for VLS doped nanowire was underestimated by one or two orders of magnitude, although this does not change the fact that the nanowires are still insulating. Given the presence of surface states in n-GaAs, the measured mobility from back-gated measurements has limited accuracy. A back gated measurement operates on the principle that an external voltage can induce or deplete charge in the nanowire by the field effect. However, surface states can screen the applied voltage, reducing the induced charge and lowering the measured mobility. Hence, the measured field effect mobilities cannot be trusted. Accurate determination of the mobility would require Hall measurements, but the backgated results prove that shell doped nanowires are n-type.

It was noted that some of the GaAs/n-GaAs nanowires produced using TFA etchant exhibited non-uniform shell deposition. A representative non-uniform shell GaAs/n-GaAs nanowire is shown in the inset of Figure 5-11b. TEM inspection of the nanowire samples noted that the Au etching process roughened the sidewalls of the nanowire with a root-mean-squared amplitude of approximately 2 nm. This is consistent with reports of Au removal in Ge nanowires and indicates that optimization of the etching chemistry and time is required to remove the Au without affecting the GaAs nanowire core.

By removing the Au nanoparticle prior to shell deposition, it was demonstrated that axially uniform n-type doping via the deposition can be achieved. These results provide final

verification of Au diffusion-depletion theory and represent a significant leap forward in the understanding of the influence of gold on the electronic properties of VLS-grown nanowires. While the demonstration of proof-of-concept devices has suggested that the adverse effects of Au may not prevent the creation of functional devices, the need to understand the role of Au on device performance has been frequently acknowledged. While there have been reports seeking to measure the concentration of Au in VLS-grown nanowires [131, 132], to the best of the author's knowledge, this is the first report detailing the impact of Au on the electronic properties of Au-grown nanowires. As such, these results provide a useful guide to the design and development of functional nanowire devices.

5.3.2 Predictive model for the conductivity of n-GaAs nanowires

GaAs is well-documented to exhibit Fermi level pinning resulting from a significant density of surface traps. Since a nanowire device can have a surface-to-volume ratio higher than ten times as a thin-film device, correctly predicting the conductivity of a shell doped nanowire requires an understanding of the impact of Fermi level pinning on the nanowire conductivity.

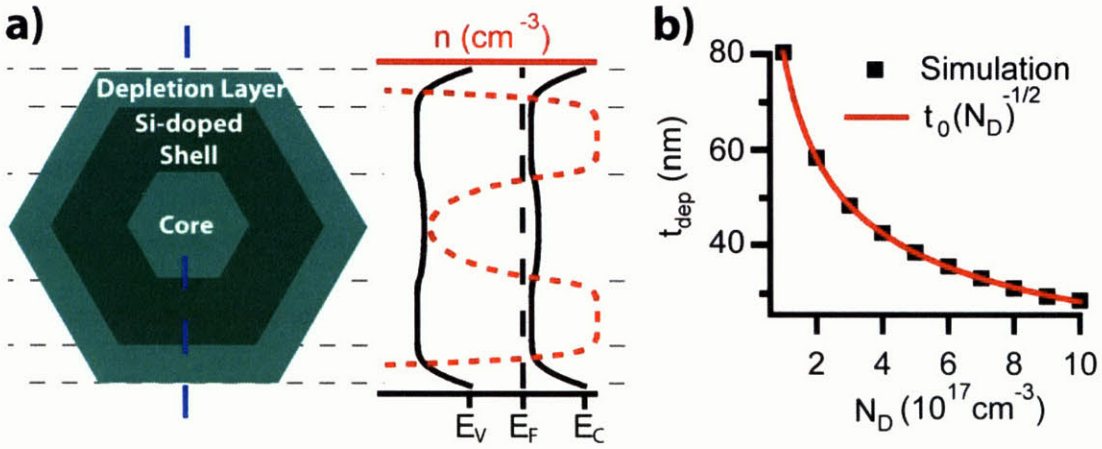

Figure 5-13: a) Schematic of effect of Fermi level pinning on free electron density, and b) thickness of surface depletion layer at different donor concentrations

The effect of Fermi level pinning on a GaAs/n-GaAs nanowire is illustrated in Figure 5-13a. Surface states surface pins the Fermi level at a fixed energy above the valence band. The pinned Fermi level results in a surface layer depleted of free carriers, known as the depletion layer, which reduces the effective thickness of the n-type shell. To quantify the effect of Fermi level pinning on predicted conductivity, Schrödinger-Poisson simulations [133] were conducted to simulate the carrier profile of GaAs/n-GaAs core-shell nanowires at various shell thicknesses and carrier concentrations. From these simulations, the thickness of the depletion layer, t_{dep}, can be determined as the distance from the surface when the $n = 0.5N_D$. By performing simulations at various donor concentrations, the dependence of the depletion layer thickness on the donor concentration can be determined, as shown in Figure 5-13b. The dependence of depletion layer thickness on carrier concentration could be approximated according to Equation 5-5.

$$t_{dep}(N_D) \cong t_0 \sqrt{\frac{1}{N_D}} \tag{5-5}$$

If the surface potential is assumed to be equal to 580 mV, then the value t_0 in Equation 5-5 is 2.53 x 10^{10} nm·cm$^{-3/2}$. This would be the case if the nanowires discussed in Section 5.2 were

depleted and pinned to the surface potential. However, as discussed in Section 5.2.4, the measured pinning potential could not be due to surface pinning, in which case the value of t_0 in Equation 5-5 would be different. The approximate dependence of t_{dep} on N_D can be understood by considering a pinned surface as having a fixed number of trap states. The number of free carriers needed to fill these states is $N \sim N_D \times L \times t_{dep}^2$, where N_D is the density of free carriers and $L \times t_{dep}^2$ is the volume over which carriers are taken. Knowing the thickness of the depletion layer, the measured nanowire conductivity can be predicted by assuming the measured conductivity of the nanowire is the conductivity of the doped shell averaged times the cross-sectional area of the actively doped shell divided by the total cross-sectional area of the nanowire.

$$\sigma = \left\{ \begin{array}{ll} q\mu_n N_D \dfrac{(t+r-t_0\sqrt{\dfrac{N_0}{N_D}})^2 - r^2}{(t+r)^2}, & t > t_{dep} \\ q\mu_n N_i, & t < t_{dep} \end{array} \right\} \qquad (5\text{-}6)$$

Here, the shell's measured conductivity, as calculated from TLM measurements by Equation 5-1, is predicted by Equation 5-6. Here, the actively doped shell's conductivity is given by $q\mu_n N_D$, where q is the charge of an electron, μ_n is the electron mobility, and N_D is the donor concentration in the shell. This conductivity was corrected by a geometric factor of the doped shell's cross-sectional area, the cross-sectional area of a hexagonal with radius $t + r - t_{dep}$ minus the cross-sectional area of the core with radius r divided by the total cross-sectional area of the nanowire. Here, t is the total shell thickness, r is the core radius, and t_{dep} is the depletion layer thickness determined from Schrödinger-Poisson simulations shown in Figure 5-13. If the nanowire is entirely depleted, which occurs when $t < t_{dep}$, then the conductivity of the nanowire

would be the same as an undoped nanowire with an intrinsic carrier concentration N_i measured to be ~ 10^{11} cm^{-3}.

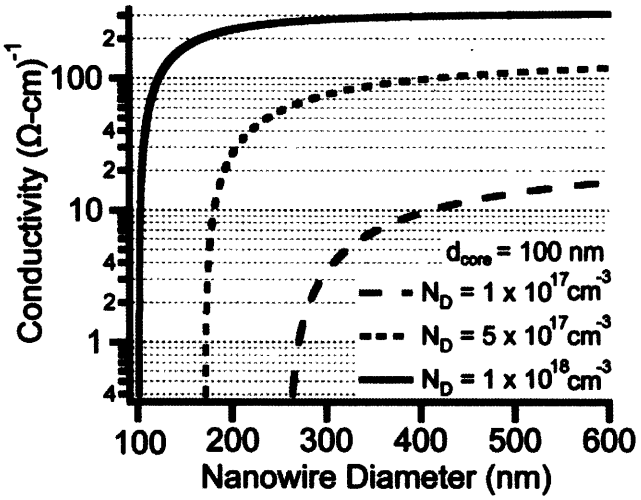

Figure 5-14: Simulated conductivity of core-shell GaAs/n-GaAs nanowires at different shell thickness and carrier concentrations assuming core radius = 50 nm and μ_n = 2000 cm^2/V-s.

Utilizing Equation 5-6, the dependence of expected conductivity on carrier concentration and shell thickness can be calculated, as shown in Figure 5-14. These simulations were performed using a core radius of 50 nm, an electron mobility of 2000 cm^2/V-s, and a surface potential of E_V + 0.84 V. As expected, the conductivity increases with increasing shell thickness and falls to nearly zero when the shell thickness is less than the depletion layer thickness. Applying this formula to the nanowires shown in Figure 5-11, the carrier concentration is 1.3 x 10^{-17} cm^{-3} at a mobility of 2000 cm^2/V-s. This value is within expectation. While the donor concentrations of the shell-doped, Au-removed shell doped nanowires, and thin-film samples should not have same donor concentrations, all samples are showing donor concentration on the order of 10^{17} cm^{-3}.

Precise determination of the carrier concentration would require precise measurement of carrier mobility by Hall measurement. If the mobility is lower than 2000 $cm^2/V\text{-}s$, then the magnitude of the conductivity will be scaled down. Moreover the precise value of

5.4 Conclusions

In this chapter doping via the deposition of an epitaxial doped shell was presented. Undoped nanowires were shown to be semi-insulating with a carrier concentration less than 10^{12} cm^{-3}. Growth conditions of 750°C, V/III ratio = 200, and IV/III ratio = 1/8 were chosen to minimize the concentrations of autocompensating impurities. It was shown that if the Au seed nanoparticle is present during the shell deposition step, conducted at 750°C for 5 min, an unexpected rectification behavior was observed near the Au nanoparticle. A combination of energy dispersive X-ray spectroscopy, current-voltage, capacitance-voltage, and Kelvin probe force microscopy demonstrated that the observed rectification was caused by Au diffusing from the Au nanoparticle and creating a nanowire segment depleted of free carriers. An equivalent circuit and band diagram was presented to explain this. Understanding the adverse effect of gold on n-type shell doping, a process was presented to remove the Au nanoparticle prior to shell deposition and was shown to produce uniform n-type doping. Using the energy barriers measured on rectifying nanowires, the conductivity of GaAs/n-GaAs nanowires was calculated as a function of donor concentration and geometric factors taking into account the effects of Fermi level pinning.

In all, a general method to achieve doping via the deposition of an epitaxial shell has been presented. The adverse effect of the Au nanoparticle should also be present in other semiconductor nanowire systems and the approach of preventing Au diffusion-depletion via Au nanoparticle removal is also generalizable to other materials systems. These results represent a

significant advancement in the understanding of doping in nanowire systems and should further the development of functional devices based on core-shell nanowire heterostructures.

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Chapter 6. Conclusions

In summary, this thesis studied the growth and properties of core-shell GaAs/AlGaAs nanowire heterostructures and accomplished the following three objectives. First the ability to fabricate uniform vertically-aligned GaAs/AlGaAs nanowires was demonstrated. Second, the structural, compositional, and core-shell interfacial properties of GaAs/AlGaAs nanowires were characterized and shown to be defect-free, uniform and nearly atomically sharp, respectively. Third, the adverse effect of the Au seed nanoparticle was understood and overcome yielding uniform n-type shell doped GaAs nanowires.

Chapter 3 presented studies on fabricating uniform vertically-aligned arrays of GaAs nanowires. The growth kinetics of nanowires were understood and optimized to control nanowire morphology. The tapering rate (TR) was reduced to 1nm/μm by understanding that adatom diffusion causes sidewall deposition [37]. The probability of vertical nanowire growth was increased above 95% by growing nanowires on GaAs 111B and reducing the flow rate of Ga precursor to ensure the VLS growth is limited by the Ga supply at the gold-substrate interface. These results demonstrate that arrays of vertically-align GaAs nanowires can be produced, making them viable candidates for integrated device applications [38].

Chapter 4 presented studies exploring the deposition and characterization of AlGaAs shells on GaAs nanowires. The nanowire geometry was shown to be metastable at high temperatures with morphological evolution occurring if individual nanowires were allowed to come in physical contact with one another. The controlled growth of core-shell GaAs/AlGaAs nanowire heterostructures was demonstrated. SEM measurements revealed that by growing vertically-aligned nanowires at an aerial density below 1 nanowire/μm^2 the stability of the

nanowire geometry was maintained and uniform faceted shells were deposited. EDX analyses confirmed the core-shell morphology and consistently determined the shell to be $Al_xGa_{1-x}As$ with $x = 0.89 \pm 0.03$. Axial uniformity analysis demonstrated the shell to be of constant composition with the shell thickness changing by 2 nm/μm. HAADF STEM and EDX analyses of cross-sectional samples demonstrated the shell composition was the same on all six facets and that the shell thickness changed by less than 2%. A three-dimensional reconstruction of the nanowire provided further evidence of the compositional and morphological uniformity of the nanowires in the axial and radial directions. BF-TEM and lattice resolved HAADF STEM structural analysis demonstrates the core-shell interface to be epitaxial and atomically sharp. Measuring the intensity of the profile of the HAADF image of the core-shell interface revealed the core-shell interface sharpness to be 1.4 nm, which can be attributed to either compositional grading or core-shell interfacial roughness.

Chapter 5 presented studies on n-type doping via the deposition of a doped shell. These results highlighted the adverse effect of the Au seed nanoparticle and demonstrated that doping can be achieved in radial heterostructures [40]. Undoped nanowires were shown to be semi-insulating with a carrier concentration less than 10^{12} cm^{-3}. Growth conditions of 750°C, V/III ratio = 200, and IV/III ratio = 1/8 were chosen to minimize the concentrations of autocompensating impurities. It was shown that if the Au seed nanoparticle is present during the shell deposition step, conducted at 750°C for 5 min, an unexpected rectification behavior was observed near the Au nanoparticle. A combination of energy dispersive X-ray spectroscopy, current-voltage, capacitance-voltage, and Kelvin probe force microscopy demonstrated that the observed rectification was caused by Au diffusing from the seed nanoparticle and creating a nanowire segment depleted of free carriers. An equivalent circuit and band diagram was

presented to explain the observed rectifying behavior. Understanding the adverse effect of gold on n-type shell doping, a process was presented to remove the Au nanoparticle prior to shell deposition and was shown to produce uniform n-type doping. Using the energy barriers measured on rectifying nanowires, the conductivity of GaAs/n-GaAs nanowires was calculated as a function of donor concentration and geometric factors taking into account the effects of Fermi level pinning.

6.1 Research impact & suggested future directions.

These results demonstrate that core-shell GaAs/AlGaAs nanowires may be fabricated with precise control over morphology, composition, structure, and electronic properties. The control demonstrated over all of these parameters is sufficient enough for core-shell nanowires to be considered candidates for high mobility electronics.

Use of the methods demonstrated in this thesis, or recently published reports methods of GaAs/AlGaAs fabrication by selective area epitaxy (SAE) [109], should enable a renewed study of quasi-one-dimensional conduction in the GaAs/AlGaAs system. Following the work done in the 1970s and 1980s on quasi-two-dimensional conduction, the most promising approach to studying quasi-one-dimensional conduction would be to grow the nanowire by MOCVD, since the precursor decomposition step is crucial to producing the high aspect ratio structures reported in this thesis, then depositing the shell by molecular beam epitaxy (MBE) to achieve the best purity and crystalline quality. For studies of quasi-one-dimensional conduction, the use of Au-grown nanowires is more appropriate than SAE since SAE-grown nanowires have not been demonstrated with diameters less than 60nm [41].

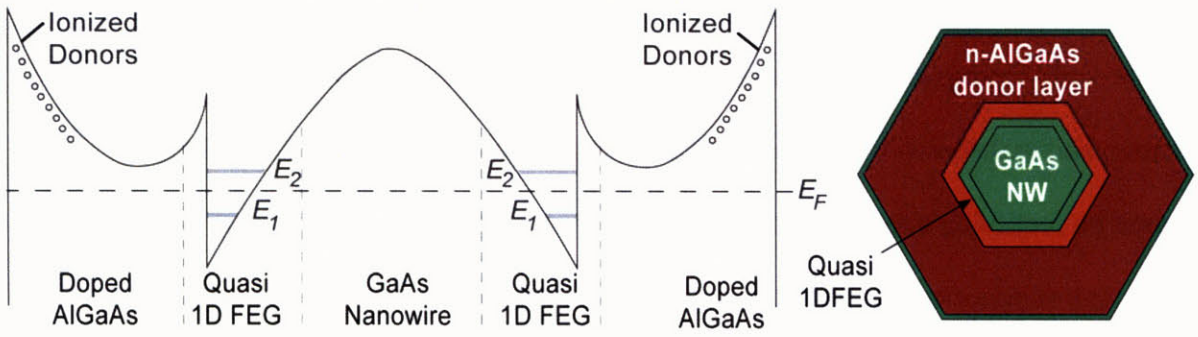


Figure 6-1: Band diagram and proposed structure of core-shell GaAs/AlGaAs structure.

A suggested test structure is shown in Figure 6-1. The GaAs nanowire is grown by the Au-mediated VLS mechanism in MOCVD. The sample is then removed from the growth chamber, the Au seed particle is removed, and the nanowire is reinserted into the growth chamber for shell deposition. This growth chamber can be either a MOCVD or an MBE. In this context, the VLS –grown nanowire is analogous to a semi-insulating substrate providing a quasi-one-dimensional template for epitaxial layer growth. The suggested shell deposition sequence is GaAs/AlGaAs/n-AlGaAs/n-GaAs. The first two layers create the channel. The thickness of these layers will depend on the shell composition, but following the literature from thin-film work [93]. The $Al_xGa_{1-x}As$ should have $x = 0.25$ to provide the most electron confinement without introducing DX centers. At this composition, the suggested thicknesses for each layer are 20nm for the GaAs and 10nm for the AlGaAs to provide sufficient confinement for the electron wavefunction. The n-AlGaAs donor layer provides carriers to the device. Based on thin film literature the aluminum fraction should be the same or higher in this layer to ensure than free electrons will drift from the donor layer to the potential well. Based on the results of this thesis, the carrier concentrations in the donor layers should be greater than $10^{18}cm^{-3}$ and the thickness of the AlGaAs should be greater than 50nm. The final layer, an n^+-GaAs capping layer is simply to aid contact formation. It should be about 5nm thick and as heavily doped as possible.

This work creates the materials science toolkit needed to use n-type doped core-shell GaAs/AlGaAs nanowires to study reduced dimensionality on electronic conduction and develop core-shell nanowire electronics. In so doing, it also creates the possibilities for other applications as well.

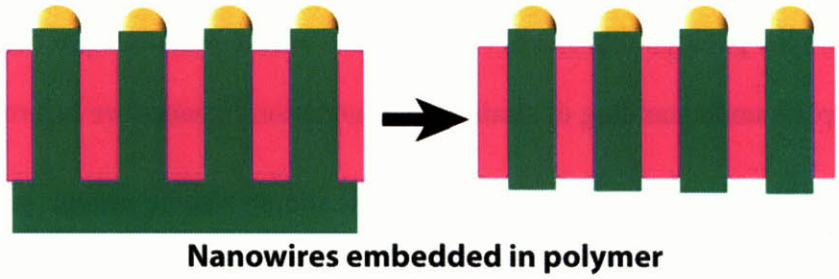


Figure 6-2: Schematic of nanowires embedded in organic materials for a solar cell.

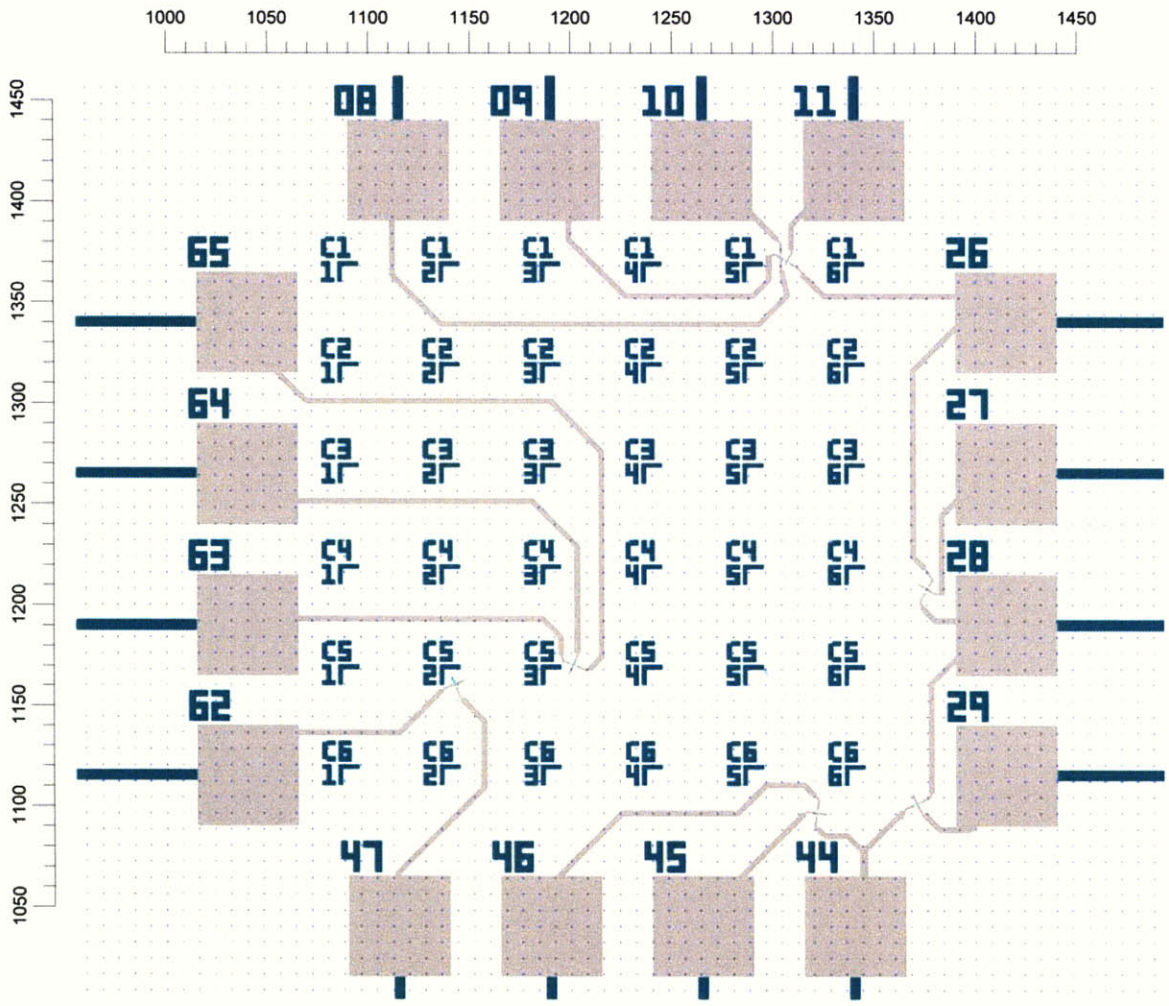
These arrays can be used as a template to produce aligned single-crystalline material embedded within organic materials [29], as shown in Figure 6-2. Initial results in this direction have already demonstrated that vertical GaAs nanowire arrays may be a cost-effective way to integrate single-crystalline semiconductor material with efficient light absorption with polymeric solar cells [134].

The characterization techniques presented in Chapter 4 are broadly applicable to all core-shell nanowires and the structural results prove the capability of bottom-up core-shell nanowires to produce a nanowire free of the many structural imperfections that hindered quasi-one-dimensional conduction studies using top-down nanowires. Moreover, the powerful characterization techniques presented in Chapter 4 combined with recent theoretical results suggesting that use of a GaAs nanowire core with diameter less than 20 nm may increase the critical thickness for dislocation-formation of $In_xGa_{1-x}As$ on GaAs by a factor of 2 at all values of x, creates a unique platform [94] to study strain accommodation of the integration of highly

misfit materials. Future work should attempt to apply the core-shell fabrication methods presented in Chapter 4, reduce the core diameter down to below 30 nm, fabricate GaAs/InGaAs nanowires at various shell thicknesses and compositions and determine the critical dimensions for dislocation formation. These results can be compared with theoretical models to ensure the full thermodynamics are captured in the models. Then, using convergent beam electron diffraction (CBED) the position dependence of the strain accommodation can be studied in order to develop a complete understanding of strain accommodation in nanowire heterostructures.

Lastly, the adverse effect of the Au nanoparticle should also be present in other semiconductor nanowire systems and the approach of preventing Au diffusion-depletion via Au nanoparticle removal is also generalizable to other materials systems. These results represent a significant advancement in the understanding of doping in nanowire systems. The demonstration that removal of Au prior to shell deposition prevents the adverse effects of Au should further the development of functional devices based on core-shell nanowire heterostructures. A large obstacle to the commercialization of Au-grown nanowires is the presence of the Au nanoparticle. However, being able to grow nanowires then remove the Au nanoparticles post-growth is a significant step towards overcoming this obstacle. In summary, this thesis provides the materials science toolkit required to use core-shell GaAs/AlGaAs nanowires to study mobility and electron transport in lower dimensional systems and develop high mobility applications.

Appendix A: Nanowire contacting: example pattern file



Example pattern file for nanowires dropped onto predefined grid (green), mapped, and aligned contacts (gray) defined.

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Appendix B: Matlab code for core-shell EDX modeling

```
function output=EDXProfileEhexagonal(param,xdata)
%fit includes Gaussian broadening of the electron beam
%fit of the Al and Ga profiles simultaneously of the hexagonal AlGaAs core-
shell nanowires with different Al concentration in core and shell for the
following parameters:
% param[1]= R1, big side
% param[2]= R2, small side (core)
% param[3]= starting x
% param[4]= calibration for Al (multiplication number for counts)
% param[5]= calibration for Ga (multiplication number for counts)
% param[6]= concentration of Al in shell
% param[7]= concentration of Al in core

R1=param(1);
R2=param(2);
x0=param(3);
CalGa=param(4);
CalAl=param(5);
Alshell=param(6);
Alcore=param(7);
broad=0.5;

[tmp,sizedata]=size(xdata);
data=xdata-x0;

%define border points
x1=R1/2;
x2=1.5*R1;
x3=R1*2;
x4=R1-R2;
x5=R1-0.5*R2;
x6=R1+0.5*R2;
x7=R1+R2;

%calculation of the thickness of the wire (core and the total wire)
for i= 1:sizedata
    x=data(i);
%definition of the thickness of the total wire for different x positions
        if data(i) < 0
            rezultat(i,1) = 0;
        elseif data(i)<= x1
            rezultat(i,1) = x*sqrt(3);
        elseif data(i)<= x2
            rezultat(i,1) =R1*(sqrt(3)/2);
        elseif data(i)<= x3
            rezultat(i,1) = sqrt(3)*(2*R1-x);
        else
            rezultat(i,1)=0;
        end
%definition of the thickness of the inner core for x positions
        if data(i) < x4
            rezultat(i,2) = 0;
        elseif data(i) <= x5
            rezultat(i,2)=sqrt(3)*(x+R2-R1);
```

```
        elseif data(i)<= x6
            rezultat(i,2) = R2*(sqrt(3)/2);
        elseif data(i)<= x7
            rezultat(i,2) = (R1+R2-x)*sqrt(3);
        else
            rezultat(i,2)=0;
        end

        %Al concentration
        rezultat(i,3)=Alshell*(rezultat(i,1)-
rezultat(i,2))+Alcore*rezultat(i,2);

        %Ga concentration
        rezultat(i,4)=(1-Alshell)*(rezultat(i,1)-rezultat(i,2))+(1-
Alcore)*rezultat(i,2);
end

%influence of the beam broadening
sx=data;
syAl=rezultat(:,3);
syGa=rezultat(:,4);

%define beam broadening
for i=1:sizedata
   x0=sx(i);
   for j=1:sizedata
       Alconv(j)= (1/(sqrt(2*pi)*broad))*exp((-((x0-
sx(j))/broad)^2)/2)*syAl(j);
       Gaconv(j)= (1/(sqrt(2*pi)*broad))*exp((-((x0-
sx(j))/broad)^2)/2)*syGa(j);
   end
   %integrate at each x contribution from the beam broadening
   rezultat(i,5)=trapz(sx,Alconv);
   rezultat(i,6)=trapz(sx,Gaconv);
end

%final result
reztemp(:,1)=CalAl*rezultat(:,5);
reztemp(:,2)=CalGa*rezultat(:,6);
output=reztemp;

function izlaz=plotsve(x,all,param)

hold off;
plot(x,all(:,1),'*','color','red');
xlabel('position (nm)');
ylabel('counts');

hold on;
plot(x,all(:,2),'*','color','blue');
fit=EDXProfileVhexagonal(param,x');
%fit=EDXProfileECrosssection(param,x');
plot(x,fit(:,2),'color','magenta');
plot(x,fit(:,1),'color','green');

izlaz=1;
```

List of Abbreviations

BDMA	Benzyldimethylamine
CCD	charged coupled device
C-V	capacitance-voltage
DCE	Dichloroethane
DDSA	Dodecenyl succinic anhydride
DI	Deionized
EBL	Electron beam lithography
EDX	Energy dispersive X-ray spectoscopy
EM	Electron microscopy
FT	Fourier transform
HAADF	High angle annular dark field
HF	Hydrofluoric acid
IPA	Isopropyl alcohol
I-V	Current-voltage
KPFM	Kelvin probe force microscopy
MMA	Methyl methacrylate
MOCVD	Metal organic chemical vapor deposition
NMA	N-Methylnadic anhydride
PMMA	Poly-(methyl methacrylate)
RTA	Rapid thermal annealing
SAD	Selected area diffraction
SEM	Scanning electron microscopy
SPM	Scanning probing microscopy
STEM	Scanning transmission electron microscopy
TEM	Transmission electron microscopy
TLM	Transmission line method
TMA	Trimethyl aluminum
TMG	Trimethyl gallium
VLS	Vapor-liquid-solid
VS	Vapor-solid

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