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Massachusetts Institute of Technology

# Extraction of Virtual-Source Injection Velocity in sub-100 nm III-V HFETs

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## ABSTRACT

We have experimentally extracted the virtual-source electron injection velocity, $v_{x0}$, of various III-V HFETs at room temperature. This is the carrier velocity that matters for logic applications of these transistors. Sub-100 nm devices with $\mu_n >$ 10,000 $cm^2$/V-s exhibit $v_{x0}$ in excess of $3 \times 10^7$ cm/s even at $V_{DD}$ = 0.5 V. This is over 2 times that of state-of-the-art Si devices at $V_{DD}$ > 1. We have verified our extraction methodology for $v_{x0}$ by building a simple charge-based semi-empirical model for the I-V characteristics of III-V HFETs. This model yields an excellent description of the entire I-V characteristics of the devices from subthreshold to inversion and from linear to saturation regimes with fitted electron velocities that are very close to those independently obtained through our proposed extraction methodology.

## INTRODUCTION

The outstanding transport properties of III-V compound semiconductors have fueled interest on these materials for use in the channel material of a future scaled CMOS technology [1, 2]. Certain III-Vs are endowed with very high electron mobilities and peak velocities that result in record values of high frequency responses as indicated by $f_T$ and $f_{max}$. For logic, however, what matters is the electron injection velocity at the virtual source, $v_{x0}$ [3]. This quantity is what determines the drain current and the transistor switching speed. To date, there have been very few evaluations of the source injection velocity in III-V FETs [4].

In this work, we carry out a rigorous extraction of the source injection velocity in InGaAs and InAs HFETs with $L_g$ from 130 nm down to 30 nm. The device design and technology used in this work have yielded world-record frequency response [5, 6] which makes these devices ideal for this study. We also show that a simple physical FET model, originally developed for Si MOSFETs, provides an accurate description of the HFET I-V characteristics over its entire regime of operation with source injection velocities consistent with those obtained experimentally.

## METHODOLOGY

The normalized drain current density ($I_D$) in an FET in saturation is given by the product of the areal charge density ($Q_{i_x0}$) and the velocity ($v_{x0}$) at the top of the energy barrier in the channel near the source (x = $x_0$) [3]. This is the so-called "virtual source" (**Fig. 1**). In our approach, $Q_{i_x0}$ is estimated first, and then $v_{x0}$ is obtained from $v_{x0} = I_D/Q_{i_x0}$. Previous efforts to extract $v_{x0}$ have used simplified models for $Q_{i_x0}$, such as, for example, a linear dependence of $Q_{i_x0}$ on $V_{GS}$ above $V_T$ [7]. However, in sub-100 nm devices, even a minor error in $Q_{i_x0}$ results in significant error in the velocity. In our work, we have extracted $Q_{i_x0}$ by integrating measurements of the intrinsic gate capacitance $C_{gi}$ at different $V_{GS}$ points in the linear regime. The process is as described next. In particular, we illustrate it on an $In_{0.7}Ga_{0.3}As$ HFET [6].

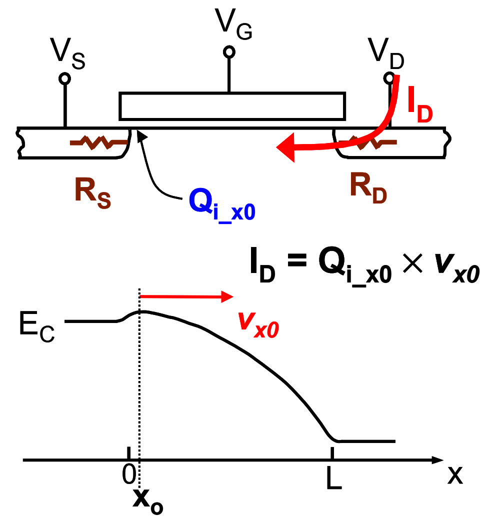


**Fig. 1** Concept of "virtual source (VS)" electron velocity ($v_{x0}$). The virtual source point is the location where the potential barrier between the source and channel goes through a maximum. $v_{x0}$ is the electron velocity at that point, and also named as injection velocity.

First, we obtain the total gate capacitance, $C_g$=$C_{gs}$+$C_{gd}$, at various bias points for different $L_g$ devices from high frequency S-parameter measurements at $V_{DS}$ = 10 mV. Separately, we measure the source and drain resistances, and determine the intrinsic values of $V_{GSi}$ and $V_{DSi}$. This allows us to graph gate capacitance ($C_g$) as a function of $V_{GSi}$. Next, we remove a parasitic portion of $C_g$ by subtracting $C_g$ ($V_{GS}$ = -0.4 V), as shown in the inset of **Fig. 2** as a function of intrinsic gate overdrive ($V_{GSi}$ – $V_T$) at $V_{DS}$ = 10 mV. At constant gate overdrive we graph $C_g$ – $C_g$ ($V_{GS}$ = -0.4 V) versus $L_g$, as shown in **Fig. 2**. We see a linear dependence of $C_g$ upon $L_g$. Here, the Y-intercept points and slopes of each line corresponding to different gate overdrives give the inner sidewall overlap capacitance ($C_{ov_inner}$) and the intrinsic gate capacitance per unit area ($C_{gi}$), respectively. This allows us to eliminate $C_{ov_inner}$ and extract $C_{gi}$. **Fig. 3** shows a typical result for $C_{gi}$ versus $V_{GSi}$. To get $Q_{i_x0}$ at a certain $V_{GSi}$, we integrate $C_{gi}$ with $V_{GSi}$. This is also shown in **Fig. 3** (see right Y-axis).

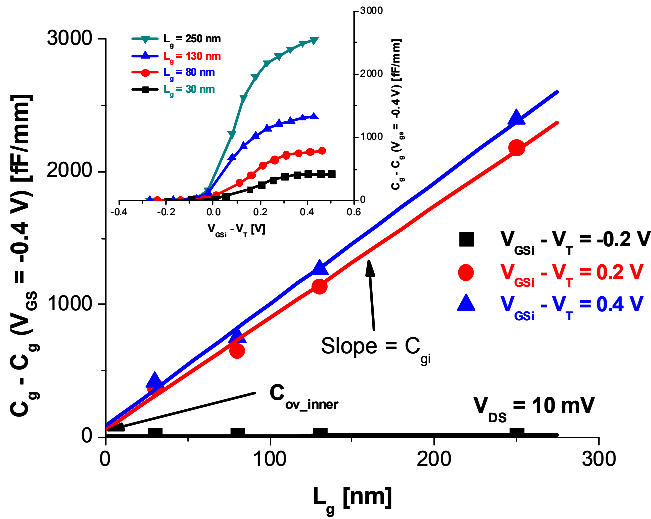


**Fig. 2** Gate capacitance ($C_g$) as a function of $L_g$ for different values of gate overdrive ($V_{GSi} - V_T$) at $V_{DS}$ = 10 mV. Inset is measured $C_g$ versus gate overdrive ($V_{GSi} - V_T$) from small-signal S-parameter measurement at $V_{DS}$ = 10 mV.

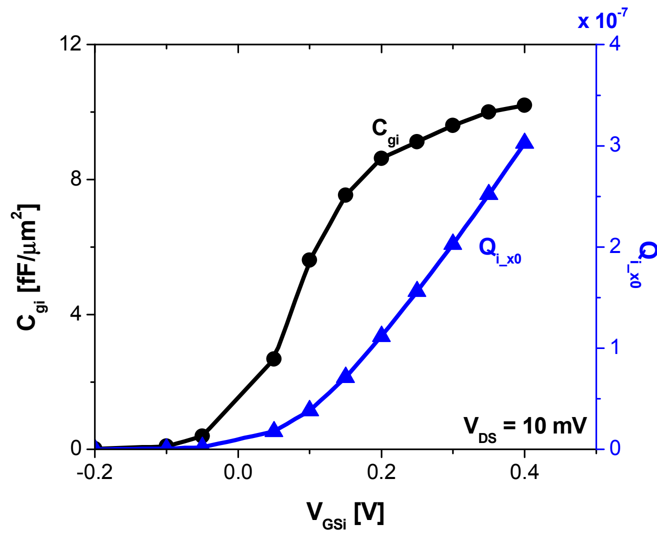


**Fig. 3** Extracted intrinsic gate capacitance $C_{gi}$ as a function of $V_{GSi}$ at $V_{DS}$ = 10 mV. Integral of $C_{gi}$ provides $Q_{i_x0}$, and $V_{GSi}$ can be given as ($V_{GS} - I_D \times R_S$).

The next step uses drain current measurements at various values of $V_{DS}$ and $V_{GS}$. Using again the measured values of $R_S$ and $R_D$, we extract the intrinsic bias of the device, $V_{GSi}$ and $V_{DSi}$. **Fig. 4** shows an example of $I_D$ versus $V_{GSi}$ for different values of $V_{DS}$.

The final step to obtain $v_{x0}$ is to divide $I_D$ by $Q_{i_x0}$ at the same values of $V_{GSi}$ and $V_{DSi}$. When doing this, the $V_T$ shift due to DIBL must be taken into account since the $Q_{i_x0}$ data are obtained at $V_{DS}$ = 10 mV, but the $I_D$ measurements are obtained at much higher values of $V_{DS}$. For this, we have used a $V_T$ definition of 1 μA/μm. **Fig. 5** shows $Q_{i_x0}$ appropriately shifted by DIBL at different values of $V_{DS}$. Note how the shift is larger at low values of $Q_{i_x0}$ than at high values. The larger shift is because for the same $V_{DS}$, $V_{DSi}$ is larger at low values of current as opposed to high values.

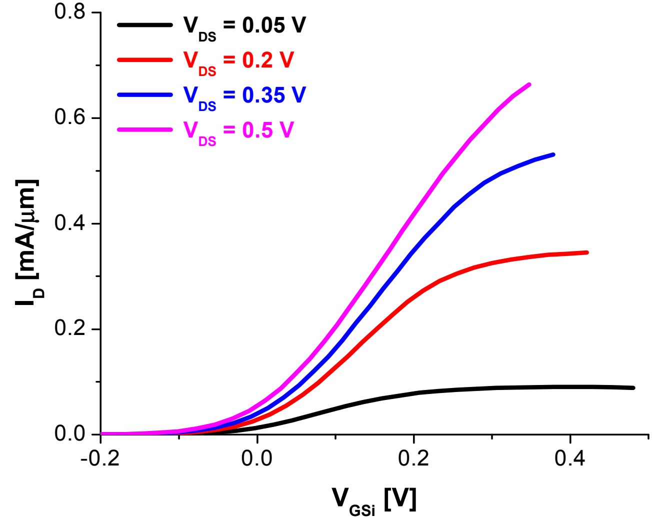


**Fig. 4** $I_D$ against $V_{GSi}$ for device with $L_g$ = 30 nm, at different values of $V_{DS}$. $V_{GSi}$ can be computed from ($V_{GS} - I_D \times R_S$).

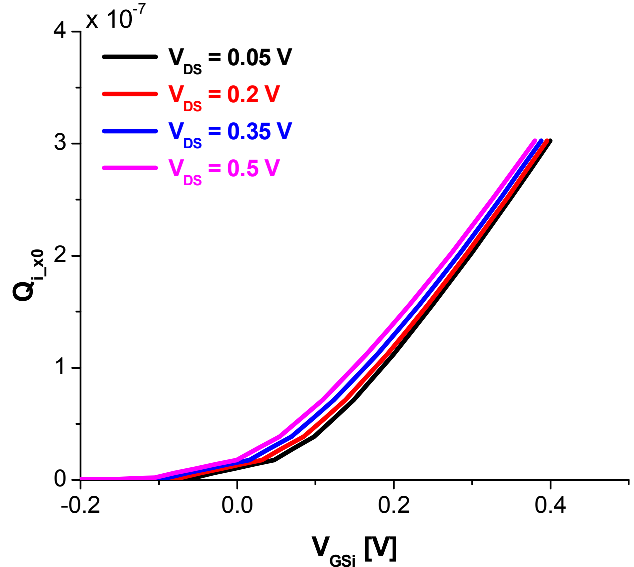


**Fig. 5** Computed $Q_{i_x0}$ against $V_{GSi}$ for device with $L_g$ = 30 nm, at different values of $V_{DS}$. The shape of the $Q_{i_x0}$ vs. $V_{GSi}$ curve is shifted using DIBL at different values of $V_{DS}$.

**Fig. 6** shows extracted $v_{x0}$ against $V_{GSi}$ at different values of $V_{DS}$ for a 30-nm device. We observe a general increase of $v_{x0}$ with $V_{DS}$ and a reduction with $V_{GS}$ as the device enters the linear regime. **Fig. 7** shows $v_{x0}$ against ($V_{GS}$–$V_T$) for devices with different values of $L_g$, at $V_{DS}$ = 0.5 V. As $L_g$ decreases, $v_{x0}$ increases, but it tends to saturate at $L_g$ ~ 40 nm to a value of about $3.3 \times 10^7$ cm/s.

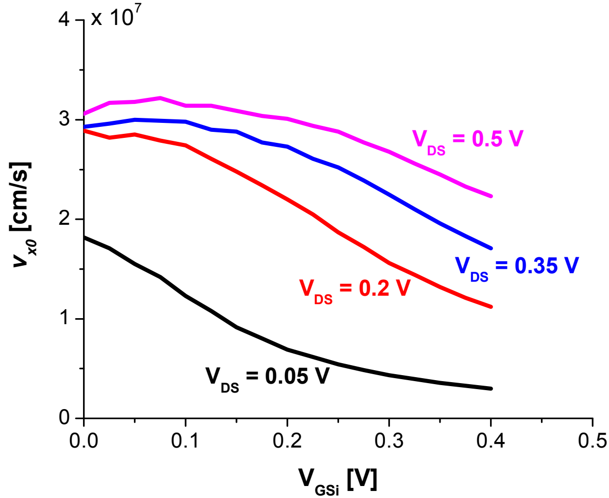


**Fig. 6** Extracted $v_{x0}$ as a function of $V_{GSi}$ for device with $L_g$ = 30 nm, at different values of $V_{DS}$. $v_{x0}$ is extracted using $I_D/Q_{i_x0}$ from **Figs. 4 & 5**.

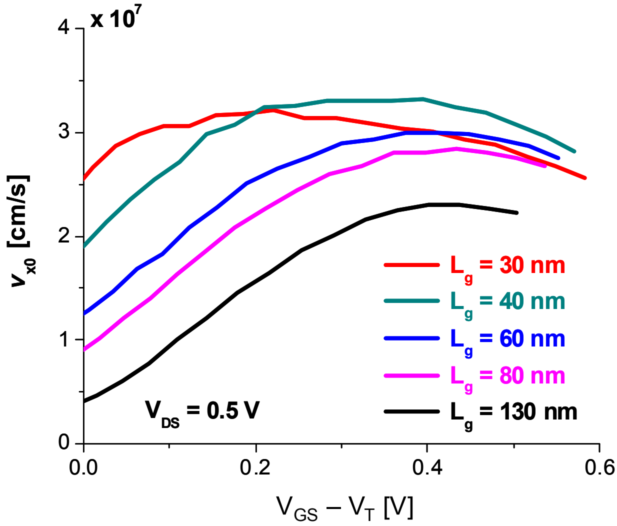


**Fig. 7** Extracted $v_{x0}$ vs. $(V_{GS}–V_T)$ for devices with different values of $L_g$ from 130 nm to 30 nm, at $V_{DS}$ = 0.5 V.

## DISCUSSION

We have carried out this extraction process on three collections of devices fabricated on different heterostructures. **Fig. 8** shows peak $v_{x0}$ vs. $L_g$ on devices with $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$ [6] and InAs channel [5] with $\mu_n$ = 9,500, 11,000 and 13,000 $cm^2/V.s$ at 300 K, respectively, all at $V_{DS}$ = 0.5 V. For comparison, the figure also includes $v_{x0}$ for advanced Si nFETs at $V_{DS}$ = 1.1 ~ 1.3 V. Clearly, III-V HFETs exhibit more than 2× higher $v_{x0}$ than advanced Si devices, even at the lower $V_{DS}$ = 0.5 V. For 30 nm InAs HFETs, a maximum velocity of 3.7 × $10^7$ cm/s is obtained. An important observation in **Fig. 8** is that $v_{x0}$ increases as the InAs composition and the mobility in the channel increases. This is likely due to a reduction in effective mass with an increased InAs composition.

It is known that in a given device technology, the carrier velocity increases as the electrostatic integrity diminishes [8]. This is because the distance within which backscattering to the source can occur decreases as DIBL increases. As a result, when comparing different device technologies, it is of great importance to plot velocity at constant DIBL. **Fig. 9** plots $v_{x0}$ against DIBL for III-V HFETs at $V_{DS}$ = 0.5 V, together with those of Si nFETs at different voltages [4, 9]. As noted [8], $v_{x0}$ increases as DIBL increases. At $V_{DS}$ = 0.5 V and DIBL = 100 mV/V, the virtual source velocity in III-V HFETs is about 7× higher than that of state-of-the-art strained Si MOSFETs [4].

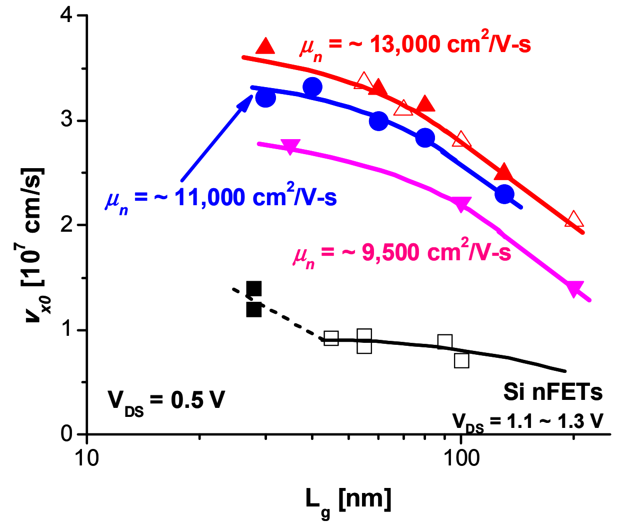


**Fig. 8** Extracted $v_{x0}$ vs. $L_g$ for various III-V HFETs with different Hall mobility ($\mu_n$) at $V_{dd}$ = 0.5 V, together with those of advanced Si nFETs with $V_{dd}$ = 1.1 to 1.3 V.

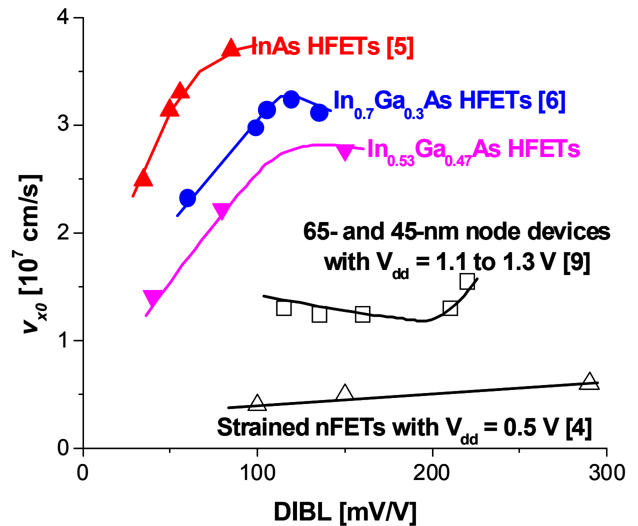


**Fig. 9** Extracted $v_{x0}$ vs. DIBL at $V_{dd}$ = 0.5 V, together with those of 65- and 45-nm nFETs at $V_{dd}$ = 1.1 to 1.3 V and state-of-the-art Si nFETs at $V_{dd}$ = 0.5 V.

## VERIFICATION

We verified our $v_{x0}$ extraction process by constructing a charge-based model for the I-V characteristics of the HFETs and comparing it with our experimental results. This is a simple semi-empirical model originally developed for short-channel Si MOSFETs that is continuous from weak to strong inversion and from the linear to saturation regimes of operation [7, 10]. This "top of the barrier transport" Virtual Source (VS) model uses only nine parameters: seven are obtained from standard device measurements; $C_g(V_{GS}=V_{dd})$, subthreshold swing, DIBL coefficient, a current value in weak inversion $I_{Dwi}(V_{GSwi}, V_{dd})$, $R_S$ and $R_D$, and effective channel length ($L_c$). There are two additional fitted parameters: the low-field effective mobility, $\mu_e$, and the virtual-source velocity in saturation, $v_{x0s}$. This model has shown remarkable agreement with published state-of-the-art strained-Si devices using physically meaningful values of the fitted physical parameters [7, 10].

**Fig. 10** compares the predictions of the VS model with measured I-V characteristics of a 30 nm $In_{0.7}Ga_{0.3}As$ HFET [6]. **Fig. 11** compares the extracted $v_{x0}$ from the VS model and from the independent process discussed above (**Fig. 6**) for the same device with $L_g$ = 30 nm. Excellent agreement is achieved which increases the credibility of our extraction process. It is interesting to note that the fitted $\mu_e$ = 1,500 $cm^2$/V.s for 30-nm devices and it increases to $\mu_e$ = 5,000 $cm^2$/V.s from $L_g$ = 130 nm, indicating that values of effective mobility from large structures should be considered with caution in modeling short-channel devices. For reference, $\mu_e$ = 250 $cm^2$/V.s and $v_{x0s} = 1.4 \times 10^7$ cm/s are found in $L_g$ = 30 nm strained-Si nFETs [7, 10].

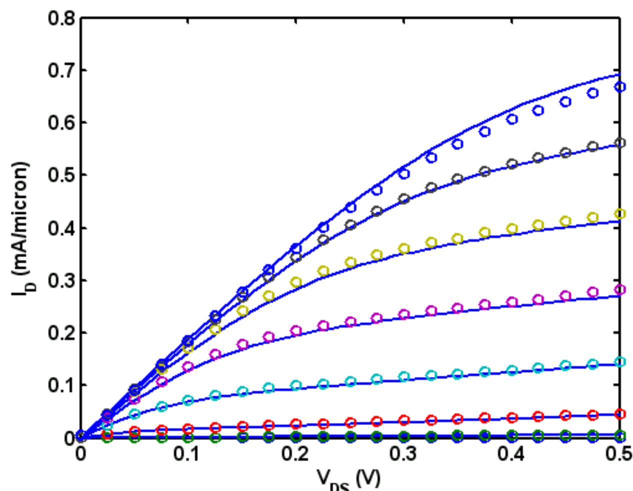


**Fig. 10** Comparison of output characteristics between measured (circles) and modeled (solid lines) 30-nm $In_{0.7}Ga_{0.3}As$ HFETs.

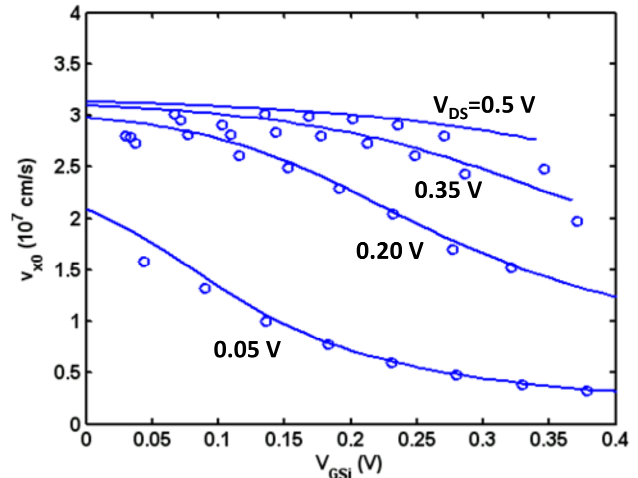


**Fig. 11** Comparison of the virtual-source velocity ($v_{x0}$) between extracted (circles) and modeled (solid lines) $In_{0.7}Ga_{0.3}As$ HFETs.

## CONCLUSION

In summary, we have extracted the virtual source electron injection velocity in III-V HFETs at the top of potential barrier. Sub-100 nm devices in heterostructure with $\mu_n$ > 10,000 $cm^2$/V-s exhibit $v_{x0} > 3 \times 10^7$ cm/s at $V_{DS}$ = 0.5 V and room temperature. This is over 2 times that of state-of-the-art Si devices at $V_{DS}$ = 1.1 ~ 1.3 V. Consistent with these extracted values, a simple semi-empirical model of III-V HFETs yields an excellent description of the entire I-V characteristics of the devices from subthreshold to inversion and from linear to saturation regimes.

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