

MIT Open Access Articles

An energy-efficient all-digital UWB transmitter employing dual capacitively-coupled pulse-shaping drivers

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

Citation: Mercier, P.P., D.C. Daly, and A.P. Chandrakasan. "An Energy-Efficient All-Digital UWB Transmitter Employing Dual Capacitively-Coupled Pulse-Shaping Drivers." *Solid-State Circuits, IEEE Journal of* 44.6 (2009): 1679-1688. © Copyright 2010 IEEE

As Published: <http://dx.doi.org/10.1109/JSSC.2009.2020466>

Publisher: Institute of Electrical and Electronics Engineers

Persistent URL: <http://hdl.handle.net/1721.1/59989>

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

Terms of Use: Article is made available in accordance with the publisher's policy and may be subject to US copyright law. Please refer to the publisher's site for terms of use.



An Energy-Efficient All-Digital UWB Transmitter Employing Dual Capacitively-Coupled Pulse-Shaping Drivers

Patrick P. Mercier, *Student Member, IEEE*, Denis C. Daly, *Student Member, IEEE*, and Anantha P. Chandrakasan, *Fellow, IEEE*

Abstract—This paper presents an all-digital, non-coherent, pulsed-UWB transmitter. By exploiting relaxed center frequency tolerances in non-coherent wideband communication, the transmitter synthesizes UWB pulses from an energy-efficient, single-ended digital ring oscillator. Dual capacitively coupled digital power amplifiers (PAs) are used in tandem to attenuate low frequency content typically associated with single-ended digital circuits driving single-ended antennas. Furthermore, four level digital pulse shaping is employed to attenuate RF sidelobes, resulting in FCC compliant operation in the 3.5, 4.0, and 4.5 GHz IEEE 802.15.4a bands without the use of any off-chip filters or large passive components. The transmitter is fabricated in a 90 nm CMOS process and occupies a core area of 0.07 mm². The entirely digital architecture consumes zero static bias current, resulting in an energy efficiency of 17.5 pJ/pulse at data rates up to 15.6 Mb/s.

Index Terms—All-digital, capacitive combining, capacitive coupling, IR-UWB, pulse-based, RF, transmitter, ultra-wideband (UWB), wireless.

I. INTRODUCTION

THE demand for increased performance and battery life in consumer, medical, and industrial electronics has emphasized the importance of energy aware circuit and system design. Since energy sources are ultimately the bottleneck in terms of size and usability of sensors networks and medical monitoring applications, the general goal of maximizing performance is instead replaced by the goal of minimizing energy consumption for a given performance specification. Typically in these types of energy-starved applications, radio components dominate the energy budget. Thus, improving the energy efficiency of RF circuits is paramount, and has been a key driving force behind the IEEE 802.15.4 and 802.15.4a standards [1], [2].

Due to their inherently duty-cycled nature, pulsed ultra-wideband (UWB) architectures have been shown to be amenable to low-power solutions [3], [4]. In particular, transmitter signal generators and power amplifiers (PAs), two blocks that typically dominate the power budget of narrowband systems, can be replaced by simple digital pulse generators and CMOS buffers [5], [6], [4]. Furthermore, non-coherent communication relaxes

Manuscript received December 03, 2008; revised March 17, 2009. Current version published May 28, 2009. This work was supported in part by the Defense Advanced Projects Agency (DARPA) HI-MEMS Contract FA8650-07-C-7704 and by the Natural Sciences and Engineering Council of Canada (NSERC). Chip fabrication was provided by STMicroelectronics.

The authors are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology (MIT), Cambridge, MA 02139 USA (e-mail: pmercier@mit.edu).

Digital Object Identifier 10.1109/JSSC.2009.2020466

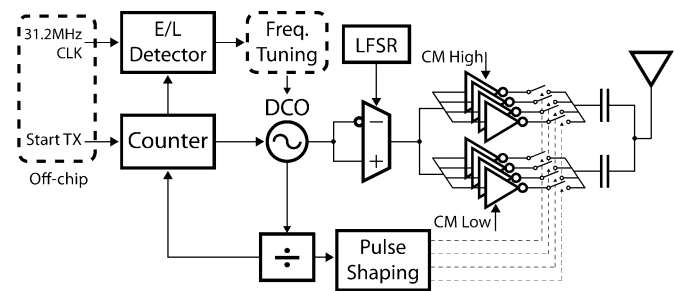


Fig. 1. Transmitter block diagram.

center frequency tolerances, thus allowing for reduced hardware complexity and enabling the use of highly digital architectures [7]–[9].

There are two distinct methods for generating UWB pulses using highly digital circuits: exciting a delay line [8], [10], or modulating the output of an oscillator [11], [12]. A ring oscillator-based solution can be advantageous since it requires fewer delay stages than an entire delay line, is highly amenable to bursting multiple pulses back-to-back, and can be used in conjunction with an integrated down-converting receiver. For spectral compliance purposes, pulse shaping may be implemented in the delay-line approach by using variable current sources at the output of each delay cell [13]; ring oscillator-based designs can instead dynamically activate high-speed drivers in parallel [12].

Unfortunately, static CMOS-based pulse generation has significant DC content that is difficult to remove via pulse shaping alone, making spectral compliance challenging. Previous work has relied on baluns [10] or off-chip filters [8], [14] to remove this low-frequency content and achieve spectral compliance. This typically requires significant chip or board area, thus increasing the size and cost of the wireless node.

This paper presents an all-digital pulsed-UWB transmitter in 90 nm CMOS, operating in the 3–5 GHz UWB band at the three channels specified by the 802.15.4a standard [15]. Low-frequency content is attenuated by capacitively combining two signal paths which are in-phase at RF, but have counter-phase common mode components that are cancelled. In concert with digital pulse shaping, the capacitive coupling results in FCC compliant operation without the use of a balun or off-chip filter. The all-digital architecture consumes 17.5 pJ/pulse and does not require a slow start-up phase-locked loop (PLL), permitting aggressive duty cycling for ultra-low-power operation. A top-level block diagram of the transmitter is shown in Fig. 1.

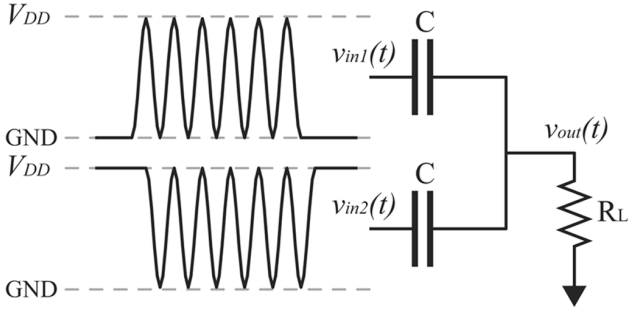


Fig. 2. Dual capacitively coupled paths.

This paper is organized as follows. Section II begins by introducing the capacitive combining approach and providing some theoretical analysis. Section III describes the implemented transmitter circuits. Section IV presents measured results from the fabricated chip. Section V summarizes the presented results, and finally, an Appendix provides mathematical formulas that are useful for predicting measurement results of pulsed-UWB signaling.

II. DIGITAL CAPACITIVELY COUPLED PULSE GENERATION

Digital pulse generators typically require high-order filters or large-area baluns in order to reduce emissions in the stringent 960–1610 MHz FCC band [8], [10]. This stems from the fact that digital static CMOS logic offers only two stable reference voltages: GND and V_{DD} . Capacitively coupling the output of a driving inverter does not sufficiently attenuate low-frequency components, due to the short pulse duration and single-order roll-off.

The proposed solution involves capacitively combining two digitally generated pulses which have in-phase RF components, yet have out-of-phase baseband (i.e., common-mode) components that are cancelled. Fig. 2 illustrates the dual-path approach. Waveforms $v_{in1}(t)$ and $v_{in2}(t)$ are given by (1) and (2) for single rectangular pulses (i.e., burst length of one with no pulse shaping):

$$v_{in1}(t) = \frac{1}{2}V_{DD}(1 - \cos(\omega_0 t))[u(t) - u(t - \tau_c)] \quad (1)$$

$$v_{in2}(t) = V_{DD} - \frac{1}{2}V_{DD}(1 + \cos(\omega_0 t)) \times \left[u\left(t - \frac{\pi}{\omega_0}\right) - u\left(t - \tau_c - \frac{\pi}{\omega_0}\right) \right]. \quad (2)$$

Here, ω_0 is the carrier frequency, τ_c is the pulse (or chip) width, and $u(t)$ is the unit step function. Note that π/ω_0 is equivalent to half of an RF cycle in time.

To better understand the spectral-effects of the capacitive combining scheme, it is useful to perform circuit analysis in the frequency domain. The Laplace domain transfer function of the network is given by

$$V_{out}(s) = \frac{sR_L C(V_{in1}(s) + V_{in2}(s))}{1 + 2sR_L C}. \quad (3)$$

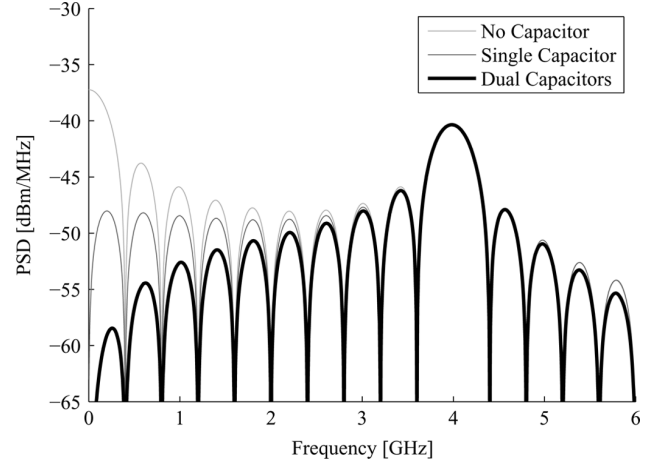


Fig. 3. Power spectral densities of three different output coupling approaches using rectangular pulse shapes.

The two input signals may also be represented by their Laplace equivalents as given by (4) and (5):

$$V_{in1}(s) = \frac{V_{DD}}{2}(1 - e^{-\tau_c s}) \left(\frac{\omega_0^2}{s(s^2 + \omega_0^2)} \right) \quad (4)$$

$$V_{in2}(s) = V_{DD}\delta(s) - \frac{V_{DD}}{2}e^{-\frac{\pi}{\omega_0}s}(1 - e^{-\tau_c s}) \left(\frac{\omega_0^2}{s(s^2 + \omega_0^2)} \right). \quad (5)$$

Here, τ_c must be an integer multiple of $2\pi/\omega_0$ for the expressions to sufficiently simplify. In other words, the pulse must be composed of an integer number of RF cycles.

The resulting output power spectrum is the cascade of a single-order high-pass filter and the sum of the two input signals, described by

$$V_{in1}(s) + V_{in2}(s) = V_{DD}\delta(s) + \frac{V_{DD}}{2} \left(1 - e^{-\frac{\pi}{\omega_0}s} \right) (1 - e^{-\tau_c s}) \left(\frac{\omega_0^2}{s(s^2 + \omega_0^2)} \right). \quad (6)$$

Thus, near the carrier frequency ($s = j\omega \approx j\omega_0$), the signals propagate to the output undisturbed. At low frequencies ($\omega \ll \omega_0$, or for frequencies at even multiples of ω_0), the signals are attenuated in an exponential fashion, regardless of the coupling capacitor sizes (provided the capacitors are matched). The resulting power spectral densities are illustrated graphically in Fig. 3, with $C = 1$ pF, $R_L = 50 \Omega$, and $\omega_0/2\pi = 4$ GHz.

This particular example yields 4.4 dB of additional attenuation at the edge of the stringent 960–1610 MHz GPS band over the first-order high-pass filter. The high-pass filter offers 2.7 dB of attenuation over direct coupling. As shown in Section IV, the proposed capacitive combining scheme, in concert with an appropriate pulse shaping scheme, offers sufficient attenuation to achieve FCC spectral compliance without requiring inductors. It should be noted that in physical design, the coupling capacitors should be sized larger than the desired high-pass cutoff as a trade-off with signal attenuation resulting from capacitive division of the coupling capacitors and parasitic capacitors.

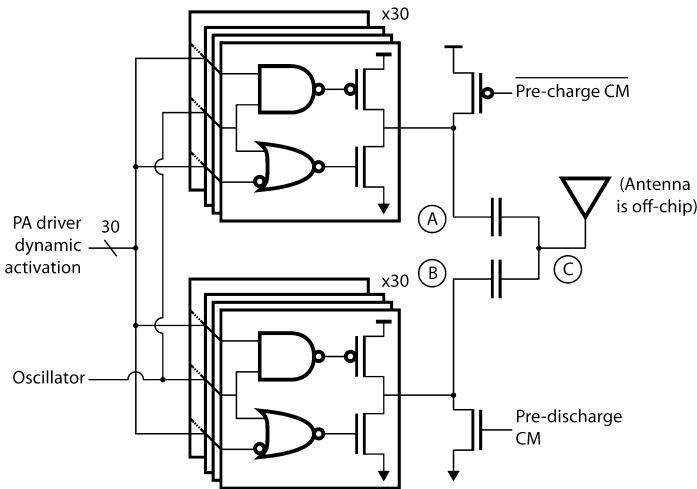


Fig. 4. Dual digital power amplifiers.

III. TRANSMITTER DESIGN

A. Architecture

A block diagram of the proposed transmitter is shown in Fig. 1. The transmitter is designed to operate in all three channels of the low-band group of the 802.15.4a standard. As per the 802.15.4a specifications, payload data is modulated using time-hopped (TH)-pulse-position modulation (PPM), where a PPM symbol is represented by a burst of several back-to-back pulses contained in a fixed window of time. In idle mode between bursts, all transmitter circuits are off and the transmitter consumes only leakage power.

The transmitter is activated on the rising edge of the off-chip *Start-TX* signal. This edge enables a digitally controlled oscillator (DCO), whose output is synchronously divided to a 499.2 MHz clock as specified by the 802.15.4a standard. The divided DCO signal is the transmitter's global clock, which activates a programmable counter to control the number of pulses transmitted per burst. Pulses are generated by BPSK-scrambling the DCO output via a run length limiting linear feedback shift register (LFSR), and buffering the resulting signal through dual single-ended digital power amplifiers (PAs) employing capacitive combination. Several phases of the 499.2 MHz divided clock are used by pulse shaping circuitry to dynamically shape the PA envelope to one of four discrete levels. The DCO output frequency is calibrated and dynamically adjusted using an early-late detector in a digital frequency-locked loop (FLL).

B. Dual Digital Power Amplifiers

A key challenge in pulsed-UWB PA design is how to achieve energy efficiency and spectral compliance while requiring as little chip and circuit board area as possible. Traditional differential analog power amplifiers (PAs) operating in their linear region can easily achieve spectral compliance, but typically have poor power efficiency [16]. Digital and switched-mode PA implementations offer superior energy efficiency compared to their analog counterparts [17]; however, they often require high order off-chip filters and/or baluns to achieve spectral compliance.

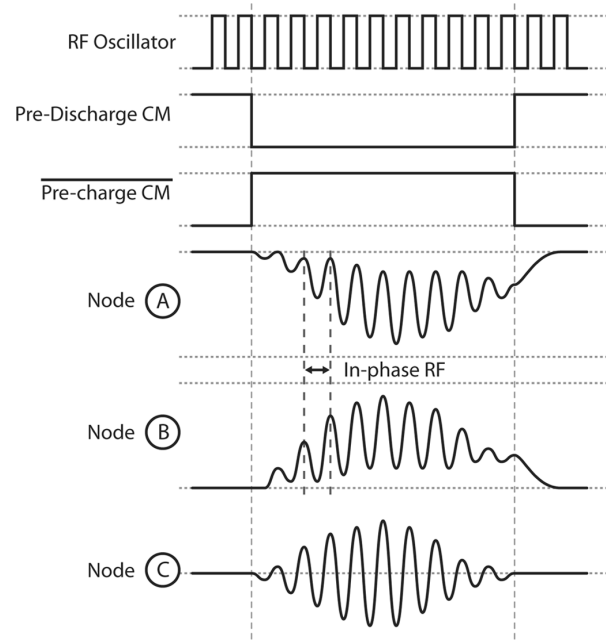


Fig. 5. Timing diagram for the dual digital power amplifiers.

An added benefit of digital PAs is that they are generally more amenable to continued scaling in advanced CMOS processes.

As discussed in Section II, one technique to reduce low frequency content generated from single-ended digital power amplifiers involves capacitively combining two paths which have in-phase RF components, yet have counter-phase common-mode components which are canceled. The circuit shown in Fig. 4 achieves this goal by driving two coupling capacitors with two single-ended digital PAs.

Both PAs consists of 30 identical and independently controlled tri-state inverters. A single oscillator signal is fed as an input to all 60 tri-state inverters, thus ensuring both paths receive in-phase RF signals. Each tri-state inverter is sized such that all 60 inverters operating in parallel can drive the antenna and associated parasitics up to approximately 700 mV when switching at 4 GHz. Output power control is achieved by programming the number of tri-state inverters enabled at a given time. Furthermore, by dynamically adjusting the number of enabled tri-state inverters during pulse transmission, pulse shaping is realized.

The differential baseband pulses (i.e., opposite common mode low-frequency pulses) are generated by ensuring that the outputs of the two PAs are at opposite supply rails immediately before and after pulse generation. Thus, during pulse generation, the two coupling capacitors begin to charge and discharge low-frequency content at the same rate, resulting in attenuated low-frequency content on the output. The opposite common modes for the two PA outputs are set by pre-charge and pre-discharge transistors during idle mode between pulses (i.e., when the PA outputs are tri-stated), as shown in Fig. 4. The dynamic PA control logic ensures that the pre-charge and pre-discharge transistors are never turned on during pulse generation in order to avoid static power dissipation. Since the PA outputs can be tri-stated, the transmitter can easily share the antenna with an integrated receiver without requiring an explicit transmit/receive switch. If required, the DC voltage of

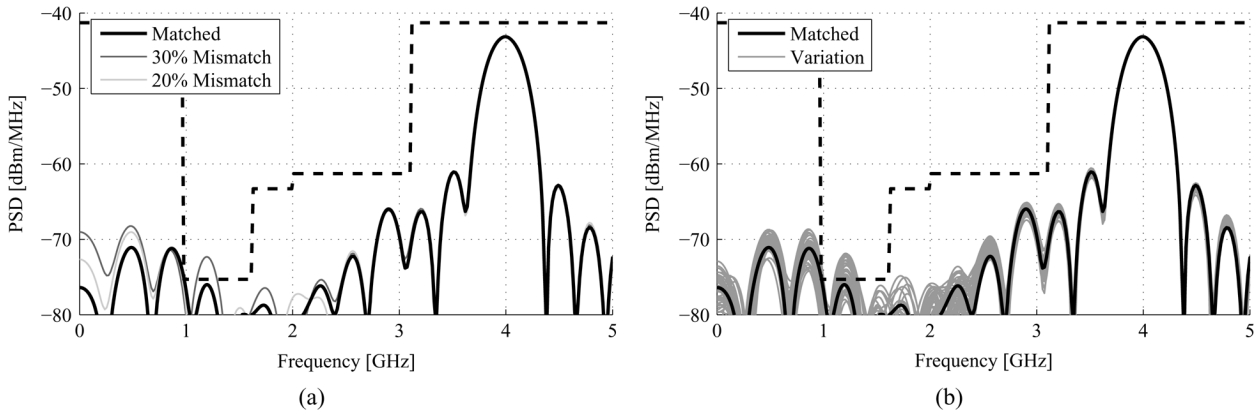


Fig. 6. Simulated output spectra with (a) coupling capacitor mismatch and (b) Monte Carlo process variation.

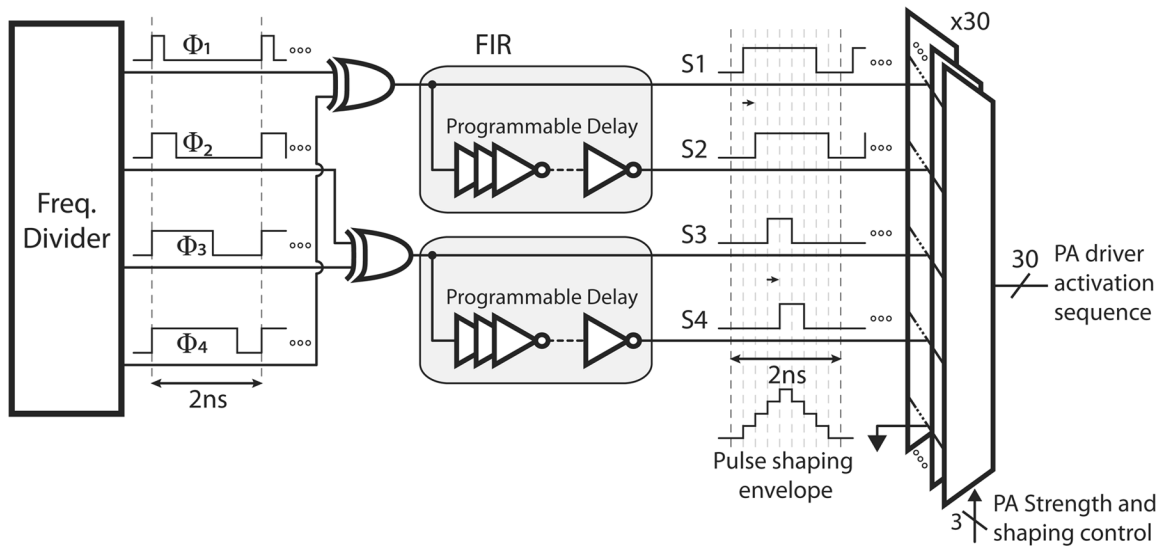


Fig. 7. Pulse shaping logic.

node C can be set with a large resistance or inductor to GND in order to eliminate any potential build up of charge.

Fig. 5 shows a representative timing diagram of the dual digital power amplifiers with pulse shaping applied. Since the coupling capacitors are charging and discharging at roughly the same rate, the average voltage of nodes A and B approach the same value (ideally $V_{DD}/2$) during pulse generation. For this reason, a very visible low-frequency transient is seen on nodes A and B at the end of pulse generation when the pre-charge/discharge devices are turned on. If the two paths are matched and the pre-charging and pre-discharging begin at the same voltage on nodes A and B , this low-frequency transient will be attenuated at the output (node C).

However, if the two paths are not matched, nodes A and B will discharge with different initial conditions, thus leading to some low-frequency content on output node C . For example, Fig. 6(a) shows the simulated output spectrum of the dual PAs with ideally matched paths overlaid on top of spectra generated with coupling capacitor mismatches of 20% and 30%. Even with an extreme mismatch of 30%, there is only an 8 dB degradation at DC and a 4 dB degradation at 1.2 GHz. A mismatch of 20% results in a 4 dB degradation at DC and zero degradation at 1.2 GHz. Fig. 6(b) shows the output spectrum resulting from

a Monte Carlo simulation of process variation, resulting in a maximum of 4 dB degradation at 1.2 GHz. Provided there are enough pulse shaping configurations to circumvent local variation, there is a high probability that the FCC mask can be met. This is discussed in more detail in Section III.C. Section IV presents measured, FCC-compliant spectra.

C. Pulse Shaping Logic

A block diagram of the pulse shaping circuitry is shown in Fig. 7. The divider, realized in true single-phase clock (TSPC) logic [11], produces internal clock phases with duty cycles that vary approximately linearly from 10% to 90%, depending on the divide ratio. Since the period of each phase is equal to the RF pulse duration of 2 ns, it is possible to combine several of these phases to generate the waveforms required for pulse shaping. This signal generation is illustrated in Fig. 7, where clock phases Φ_{1-4} are appropriately chosen to have duty cycles of approximately 20%, 40%, 60%, and 80% based on the divider configuration.

By XOR-ing Φ_1 with Φ_4 , and Φ_2 with Φ_3 , two pulse shaping signals are generated. These two pulse shaping signals are each passed through simple one-tap finite impulse response (FIR) filters to increase the number of pulse shaping signals to four (sig-

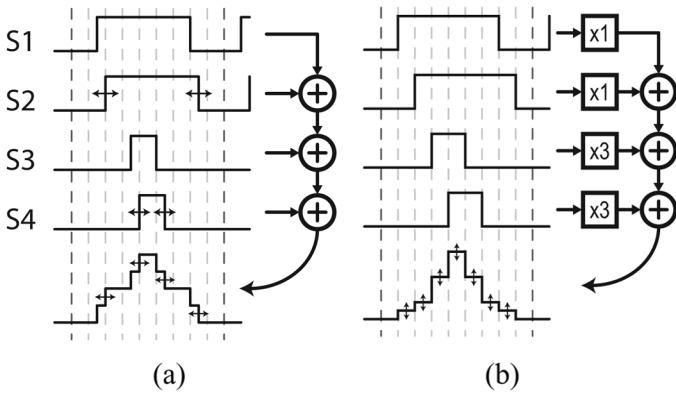


Fig. 8. Modifying pulse shapes by changing (a) delays and (b) weights.

nals S1–S4). The delay elements of the FIR filters are comprised of a programmable number of inverters.

Each tri-state inverter of the dual PAs is individually programmed through a five-input multiplexer network to receive one of the four pulse shaping signals as a dynamic activation input. The fifth multiplexer input is grounded in order to allow statically disabled tri-state inverters for gain control. The four pulse shaping signals can be thought of as the output of FIR filter taps which are added together at the input of the coupling capacitors via the parallel combination of PA tri-state inverters, as illustrated in Fig. 8. Maximum PA output swing is achieved when all four pulse shaping signals are high, i.e., the maximum number of PA inverters are enabled in parallel simultaneously. This pulse shaping configuration also ensures that the output signal amplitude is zero during BPSK phase transitions in order to avoid common-mode glitching and inter-pulse interference.

The resulting pulse shape is configured through two different methods: adjusting the pulse shaping signal timing and PA drive strengths. Timing adjustments are accomplished by selecting different frequency divider phases or changing the FIR filter delay elements, illustrated with an example in Fig. 8(a). This adjustment control is typically only used to calibrate delays to ensure equal time intervals between pulse shaping signals. The FIR filter delays have $2^3 = 8$ possible permutations (not including the selection of different frequency divider phases).

Adjusting the drive strengths involves changing how many tri-state inverters receive a particular pulse shaping signal. This is similar to choosing the weights of the FIR tap coefficients, and can be used to more closely approximate a raised-cosine shape [18]. An example pulse shape is shown in Fig. 8(b). There are approximately $2^{30} \approx 10^9$ total pulse shape strength permutations. If the dynamic range of these combinations is such that global variation can be tolerated, then the sheer number of permutations should be able to guarantee, with a reasonable degree of confidence, that local random variation can be overcome and thus the FCC mask can be met. The idea of implementing redundancy and/or massive reconfigurability in order to guarantee desired operation is often used in high density memory design, and is becoming more popular for other types of circuits such as analog-to-digital converters (ADCs) [19], [20] and near-field modulators [21]. Given the extremely large number of permutations, it is challenging to design calibration schemes for such highly redundant systems; further research is required to improve calibration performance.

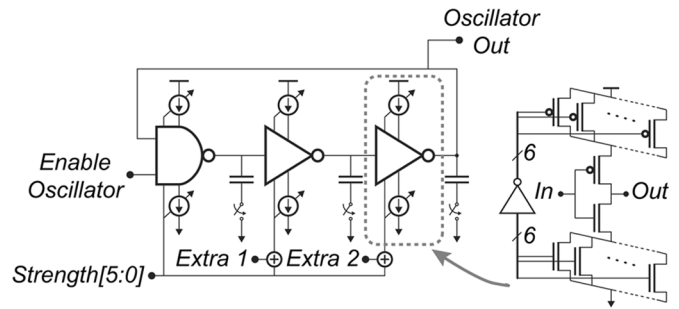


Fig. 9. Digitally controlled oscillator.

D. Digitally Controlled Oscillator

Since the transmitter is designed for use in non-coherent UWB systems, precise phase and frequency accuracy is not required. For example, receiving a non-coherent 500 MHz signal whose center frequency is only accurate to within 6000 ppm results in a maximum of 0.04 dB received power loss. Taking this into account, the resulting DCO is a 3-stage current-starved ring oscillator, shown in Fig. 9. The highly digital, single-ended structure is designed to have a fast turn-on time on the order of 2 ns in the typical case to reduce energy consumption in duty-cycled operation. The single-ended operation requires minimum energy when running, as a trade-off for increased susceptibility to power supply noise.

Phase scrambling is achieved by passing the DCO output through a single-to-differential converter that contains delay-matched paths: the inverted path consists of a static CMOS inverter, while the non-inverted path consists of a transmission gate that is sized for equivalent delay [22]. Simulation results show that up to 10 ps of delay mismatch is tolerated before spectral lines with 1 dB amplitude above the regular spectrum begin to appear. Depending on the process corner, there is a variation between the two paths of $+2$ ps/ -1 ps around the nominal 180° phase shift. Monte Carlo analysis of circuit variation indicates that the standard deviation is 1.2 ps, which is sufficiently small to not have a noticeable impact on the resulting spectrum.

Coarse DCO frequency tuning is provided by switchable load capacitors, while fine frequency tuning is provided with NMOS and PMOS current-starving DACs. To simplify the frequency locking algorithm, all three current-starving DACs are set to the same digital value, except that the second and third stage DACs can be individually incremented by one for increased resolution. This technique results in a resolution of 7.5 bits from the DACs and 2 bits from the three thermometer encoded capacitors, totaling 9.5 bits. This resolution of frequency control is sufficient to meet non-coherent wideband receiver sensitivity requirements. The worst-case measured frequency step size in the 3–5 GHz band is 10 MHz, corresponding to an accuracy of 2800 ppm.

In order to guarantee operation at the 3.5, 4.0, and 4.5 GHz channels of the 802.15.4a proposal, the DCO must be over-designed to account for process variation. In this manner, the DCO targets a tuning range of 2.2–6.0 GHz in the typical corner at 25°C and $V_{DD} = 1.0$ V. Fig. 10 shows the measured tuning curves of the DCO overlaid with simulated curves at the slow, typical, and fast design corners, where the typical corner is also run at various temperatures and supply voltages.

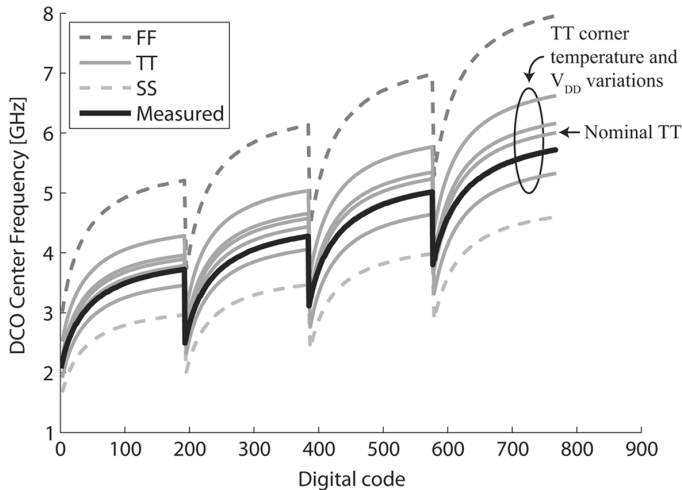


Fig. 10. Measured DCO tuning curve compared to simulated results, with TT simulations operating between 0.9–1.1 V and 0°C–75°C.

The on-chip early-late detector provides hard early-late information by comparing the falling edge of *Start-TX* with the output of a programmable count length using a single flip-flop. Typically, since *Start-TX* operates at 31.2 MHz, the counter, which operates at 500 MHz, should count to eight. The output of the early-late detector is fed to a SAR algorithm for initial turn-on frequency calibration. This algorithm, which was implemented off-chip, converges within 12 pulse-bursts, i.e., 0.77 μ s when operating at 15.6 Mb/s.

Once the DCO has been calibrated, the early-late detector can be used in a low-power FLL to dynamically update the current-starving bits for robustness against PVT [23].

E. LFSR With Run Length Limiting

As specified by the 802.15.4a standard, a 16 bit LFSR is used to BPSK-scramble the phases of individual pulses within a burst. Although phase modulation is not used to represent data in non-coherent systems, phase scrambling is still employed to attenuate spectral lines, thus maximizing the average power spectral density (PSD) under FCC regulations.

As discussed in [24], one method to increase communication distance in low-pulse-rate UWB systems is to limit the length of time where no phase inversions occur within a burst of pulses. That is, the sequence of BPSK scrambling bits should be void of long single-polarity runs. Assuming sufficiently long runs occur infrequently, the average PSD remains unaffected. However, the “tone-like” long runs without phase inversions are eliminated; thus, peak power is spread away from the center frequency and the absolute maximum peak power is reduced. Since low-data-rate pulsed-UWB systems are peak power limited (as opposed to average-power limited) [16], this technique increases communication distance by increasing available average power for a given peak power limit. The Appendix of this paper presents formulas for predicting pulsed-UWB measurement results, giving mathematical insight as to why peak power decreases when run length limits (RLLs) are imposed.

In the proposed transmitter, run length limiting is accomplished by buffering the LFSR outputs and comparing to a pre-

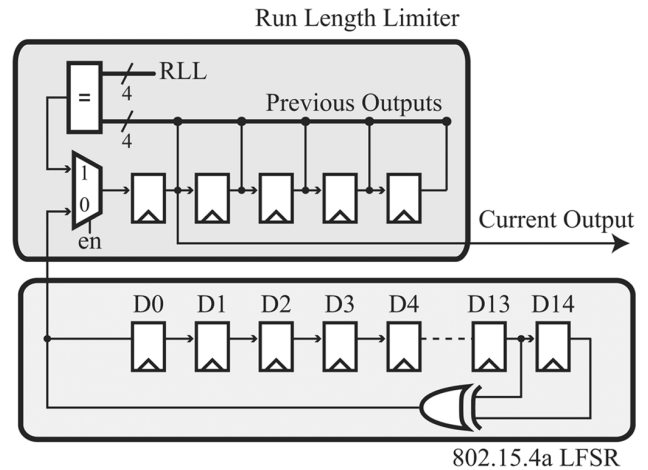


Fig. 11. LFSR with run length limiting for peak power reduction.

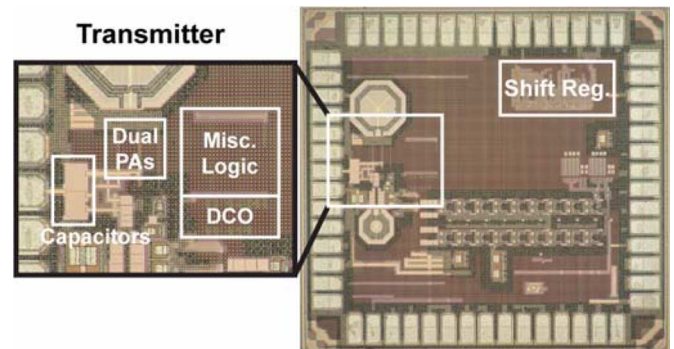


Fig. 12. Die photo of fabricated transmitter.

programmed RLL, as shown in Fig. 11. If a run of a single polarity is encountered, the next bit in the LFSR sequence is discarded, and a bit with opposite polarity to the run is inserted in the first stage of the buffer, thus ensuring that it propagates to the output on the following clock cycle. Since the bit is inserted in the buffer, another run is not possible for at least the RLL.

IV. MEASUREMENT RESULTS

The transmitter was fabricated in a 90 nm CMOS process and operates on a 1 V supply. The chip was packaged in a 40-lead, wirebonded QFN package; all measurement results were taken from the packaged chip. A die photograph is shown in Fig. 12. Note that the DCO and programmable shift register are shared between the transmitter and an integrated receiver (which is not discussed in this paper). The transmitter and DCO occupy a core area of 0.07 mm². The transmitter operates at data rates from 0 to 15.6 Mb/s. It has a turn-on time of 7.2 ns, measured as the time it takes pulses to appear at the output of the dual PAs after the rising edge of *Start-TX* has arrived.

Fig. 13(a) presents a measured 3.5 GHz transient waveform of a burst of five individually BPSK modulated pulses. Fig. 13(b) shows the time-averaged envelope of a similar burst, illustrating the discrete four-level pulse shaping. Measurements were taken with a Tektronix TDS 8000 Sampling Oscilloscope with an 80E04 sampling module.

The resulting pulse-bursts achieve both indoor and outdoor FCC compliance in all three bands without requiring the use

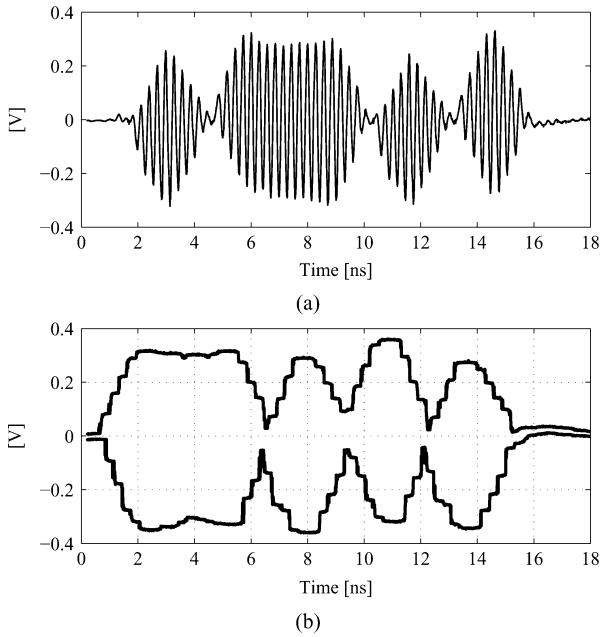


Fig. 13. (a) Measured transient waveform of a burst of five individually BPSK-modulated pulses, and (b) time-averaged envelope of a different burst.

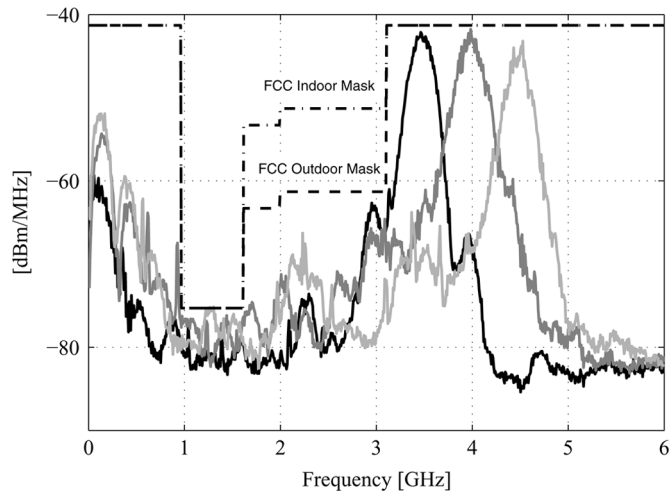


Fig. 14. Overlaid power spectral densities of the three channels in the low-band of the 802.15.4a proposal.

of an off-chip filter, as shown in Fig. 14. Fig. 15 illustrates the effects of capacitive combining and pulse shaping. Capacitive combining achieves up to 12 dB of low frequency attenuation compared with simple capacitive coupling, while pulse shaping realizes 15–20 dB of sidelobe rejection. Note that these results should not be directly compared with the results in Fig. 3, since the aforementioned figure uses rectangular pulses and does not anticipate parasitics or any circuit non-idealities. Unless otherwise noted, all power spectral density measurements were performed by directly coupling the transmitter output to an Agilent MXA N9020A Spectrum Analyzer using a 1 MHz resolution bandwidth (RBW) in RMS averaging mode with a typical corner die.

It should be noted that the effect of capacitive combination is more pronounced for bursts containing few pulses. Every time

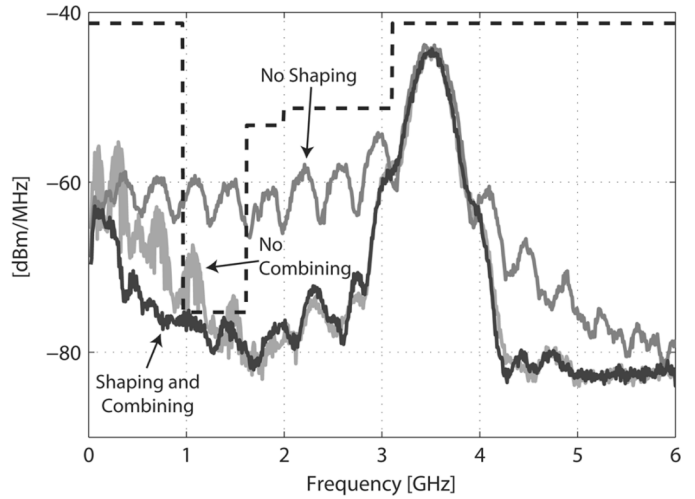


Fig. 15. Overlaid power spectral densities with shaping disabled, combining disabled, and normal operation.

pulse generation begins and ends, low-frequency content is generated by charging and discharging the average DC voltage across the coupling capacitors. When transmitting a single pulse at a time, there is an overhead cost for every pulse. When bursting several pulses at a time, there is only an overhead cost for the entire burst. Thus, for an equivalent output power around the carrier, bursting many pulses will always result in less low-frequency content. However, it is still beneficial to support single pulse transmission, as a non-coherent receiver may be designed with a short integration window in order to provide increased ranging resolution. Furthermore, in extreme multi-path environments it is often beneficial to transmit only a few pulses at once, as the channel may spread a considerable amount of energy over the receiver's entire integration window.

The dual PAs have 16 programmable gain settings. Since all tri-state inverters are sized to have the same drive strength, the increase in gain through parallel combination is linear, and a 13 dB range is observed. The maximum output voltage swing is 710 mV.

Fig. 16 illustrates the peak power effects of run length limiting. For $RLL = 3$ and bursts of 16 pulses, peak power is reduced by 3 dB, resulting in approximately a 2x increase in communication distance for low data rate operation [24]. This measurement should ideally be taken with a RBW of 50 MHz to comply with FCC regulations; however, the maximum RBW on the N9020A (with no extra options) is 8 MHz. In this case, the FCC recommends measuring peak power in the highest RBW available, with the detector set to peak-hold mode. The limit for an 8 MHz RBW is $20\log(8\text{ MHz}/50\text{ MHz}) = -15.9\text{ dBm}$ (see the Appendix, Section A).

Operating on a 1 V supply, the transmitter draws 4.36 mW when generating 16-pulse bursts at a symbol repetition frequency (SRF) of 15.6 MHz. This results in an energy efficiency of 280 pJ/burst, or 17.5 pJ/pulse.¹ Note that the transmitter (including the DCO) is duty cycled between bursts to save energy.

¹This was previously reported as 19 pJ/pulse [15]. Energy was reduced by enabling fewer DCO capacitors and increasing current-starving to achieve the same center frequency.

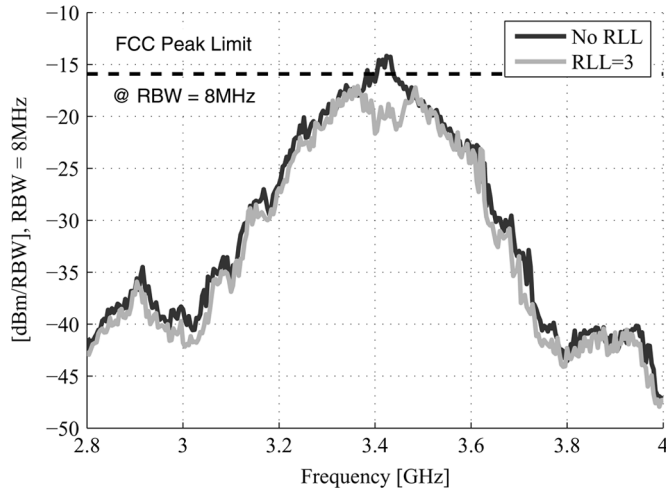


Fig. 16. The effects on peak power when setting RLL = 3 for bursts of 16 pulses.

TABLE I
TRANSMITTER PERFORMANCE SUMMARY

Specification	Value	
Process	90nm CMOS	
Active Die Area	0.07mm ²	
Modulation	PPM+BPSK	
SRF Range	0-to-15.6MHz	
Supply	1V	
	Standby Power	Active E/pulse
Power Amplifier	22μW	2pJ
DCO/Clock/Control	83μW	15pJ
Shift Register	11μW	-
I/O and ESD	7μW	<1pJ
Total	123μW	17pJ
Output Voltage Swing	165mV _{pp} -to-710mV _{pp}	
DCO Frequency Range	2.1GHz-to-5.7GHz	
Turn-on Time	7.2ns	
Symbol Rate (SRF)	100kHz	15.6MHz
Energy/16-pulse-burst	1.6nJ	280pJ
Energy/pulse	103pJ	17.5pJ
Total power	164μW	4.36mW
Output power	-25dBm	-16.4dBm

The total output power in this configuration is -16.4 dBm. Table I summarizes the transmitter's performance.

Since all transmitter circuits are off between burst transmissions, the power consumption scales with data rate. However, the impact of leakage power becomes significant at burst rates below 1 MHz. This is illustrated in Fig. 17, where the energy efficiency of the transmitter, and other recently published work, is plotted versus symbol (i.e., burst) rates. It should be noted that the total output power of the transmitter was set to be as close as possible to -16 dBm for all measurements to obtain maximum output power under FCC limits. Due to the limited output swing of the dual power amplifiers, -16 dBm total output power could not be reached for symbol rates under 500 kHz. For these measurements, the maximum PA gain was chosen. The dashed line in Fig. 17 illustrates the effective energy per pulse if the transmitter output power was not scaled with symbol rate, but instead retained the PA gain settings of the 15.6 MHz symbol rate

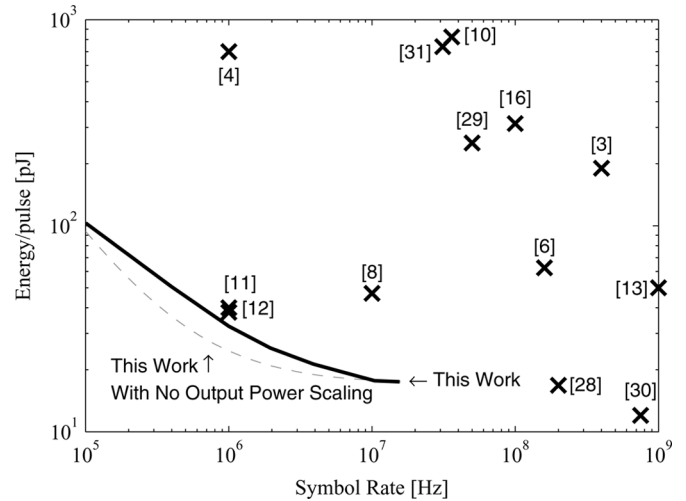


Fig. 17. Energy per pulse for the proposed transmitter compared to previously published results.

measurement (i.e., the instantaneous radiated power remains the same, while the average radiated power decreases proportionally to the decrease in SRF).

V. CONCLUSION

This paper presents an ultra-low-energy all-digital pulsed-UWB transmitter operating in three channels from 3 to 5 GHz. The transmitter achieves energy efficient operation by synthesizing pulses using a simple single-ended ring oscillator and digital output buffers. Consuming zero static bias current, the transmitter achieves energy efficiencies of 103 to 17.5 pJ/pulse at data rates of 100 kb/s to 15.6 Mb/s. It is demonstrated that inductor-based high-pass filters and baluns may be eliminated while still achieving FCC compliant operation by using four-level pulse shaping and capacitive combining techniques. These techniques offer robust and configurable operation without any significant increase in area or power.

APPENDIX

A. Pulsed-UWB FCC Regulations

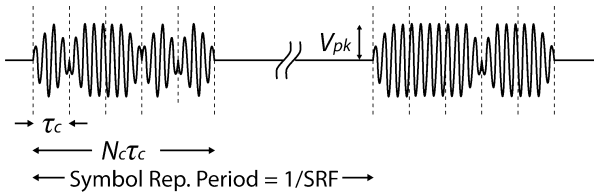
In the United States, the FCC places limits on both the peak and average radiated output power in the 3.1–10.6 GHz UWB band [25]. The two key FCC regulations are as follows:

- 1) the *average* PSD must be less than or equal to -41.3 dBm in the 3.1–10.6 GHz band;
- 2) the *peak* power may not exceed 0 dBm at the UWB signal's center frequency in a 50 MHz RBW.

Since most spectrum analyzers are not equipped with a 50 MHz intermediate frequency (IF) filter, the peak power measurement is typically performed at a lower RBW and the limit is conservatively set to be $P_{pk} \leq 20 \log_{10} (RBW/50 \text{ MHz})$.

B. Predicting Pulsed-UWB Measurement Results

This section presents mathematical formulas for predicting pulsed-UWB measurement results using a spectrum analyzer (SA). To begin, some notation is introduced in Fig. 18. τ_c is the chip period of an individual pulse, N_c is the number of chips


 Fig. 18. Two bursts of five individually BPSK modulated pulses (i.e., $N_c = 5$).

(i.e., pulses) per burst, and V_{pk} is the peak voltage of the waveform.

Most UWB pulses have a narrow pulse width $\tau_c < 0.1/\text{RBW}$ relative to the intermediate frequency of an SA. Thus, the SA measures the impulse response of its own IF filter, rather than the response of the UWB pulse. To predict certain measured results from an SA, a pulse desensitization correction factor (PDCF) will be introduced [16], [26].

Ideally, the spectral response of a periodic BPSK-modulated pulse (or burst) train should contain spectral lines at integer multiples of the SRF.² This effect will be observed on an SA if its RBW is less than the SRF, since the SA will have sufficient resolution to display the spectral lines. This measurement regime is called the *high-SRF region*, and occurs when $\text{RBW}/\text{SRF} < 0.3$. If, on the other hand, the RBW is greater than the SRF, the SA does not have sufficient resolution and individual spectral lines are blended together. This measurement regime is called the *low-SRF region*, and occurs when $\text{RBW}/\text{SRF} > 1.7$. The peak and average powers in these two regions can be predicted using the equations derived below. Unfortunately, measurements in the region around $\text{SRF} \approx \text{RBW}$ depend heavily on modulation statistics and are much more difficult to predict [27].

For both low and high SRF BPSK-modulated signals, the the average power can be found by using (7):

$$P_{\text{avg}} = 10 \log \left(\frac{V_{pk}^2}{Z_0} \right) + 20 \log(\tau_{\text{eff}}) + 10 \log(\text{PRF}_{\text{eff}} \cdot \text{RBW}). \quad (7)$$

Here, V_{pk} is the peak voltage of the pulse, Z_0 is the characteristic impedance, and PRF_{eff} is the effective *pulse* repetition frequency (i.e., for bursting, $\text{PRF}_{\text{eff}} = \text{SRF} \times N_c$). τ_{eff} is the effective individual pulse width, as illustrated by Fig. 19 and given by

$$\tau_{\text{eff}} = \int_0^{\tau_c} \frac{p(t)}{V_{pk}} dt. \quad (8)$$

Here, $p(t)$ is a single pulse, and τ_c is the time interval which contains all the energy of $p(t)$.

The peak power in the high-SRF region is given by

$$P_{pk,h} = P_{\text{avg}} + P_{m,h}. \quad (9)$$

Here, $P_{m,h}$ typically ranges from 7 dB to 11 dB, and depends on both the modulation statistics and the length of time the peak measurement is taken over [26].

²These lines are different than the undesired spectral lines produced by non-phase-scrambled, PPM-modulated pulse trains.

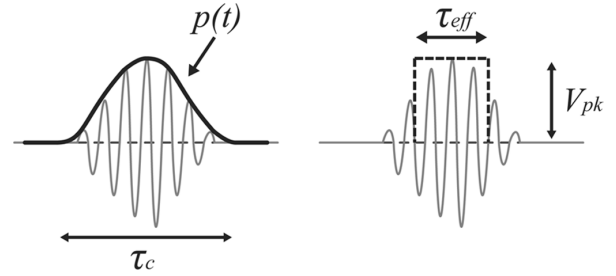


Fig. 19. Effective pulse width of a non-rectangular pulse envelope.

The peak power in the low-SRF region is given by

$$P_{pk,l} = 10 \log \left(\frac{V_{pk}^2}{Z_0} \right) + \text{PDCF} + P_{m,l}. \quad (10)$$

Here, $P_{m,l}$ is a fitting factor based on modulation statistics and typically varies from -3 dB to $+3$ dB. The pulse desensitization correction factor is given by

$$\text{PDCF} = 20 \log(\tau_{b,\text{max}} \cdot \text{RBW} \cdot k_{\text{pulse}}). \quad (11)$$

k_{pulse} relates the RBW frequency to an effective IF bandwidth for pulsed signals. It depends on the SA used and typically varies from 1.5 to 1.617 [26]. $\tau_{b,\text{max}}$ is the worst-case effective burst width and is given by

$$\tau_{b,\text{max}} = \left| \int_0^{\frac{1}{\text{SRF}}} \frac{p_{b,\text{max}}(t)}{V_{pk}} dt \right|. \quad (12)$$

Here, $p_{b,\text{max}}$ is the inter-burst chip sequence with the worst-case peak power, which occurs when the chip sequence contains a minimum number of phase inversions. For single-pulse transmissions, $p_{b,\text{max}} = p(t)$. Thus, without affecting the average PSD, peak power may be reduced by limiting the phase scrambling run length.

ACKNOWLEDGMENT

The authors thank Nathan Ickes for testing support.

REFERENCES

- [1] *Part 15.4: Wireless MAC and PHY Specifications for Low-Rate Wireless Personal Area Networks*, IEEE Std. 802.15.4, 2003.
- [2] *IEEE 802.15.4a Wireless MAC and PHY Specifications for LR-WPANs*, IEEE Std. 802.15.4a, 2007 [Online]. Available: <http://www.ieee802.org/15/pub/TG4a.html>
- [3] Y. Zheng, Y. Tong, C. W. Ang, Y.-P. Xu, W. G. Yeoh, F. Lin, and R. Singh, "A CMOS carrier-less UWB transceiver for WPAN applications," in *IEEE ISSCC Dig. Tech. Papers*, 2006, pp. 378–387.
- [4] T. Terada, S. Yoshizumi, M. Muqsith, Y. Sanada, and T. Kuroda, "A CMOS ultra-wideband impulse radio transceiver for 1 Mb/s data communications and ± 2.5 cm range findings," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 891–898, Apr. 2006.
- [5] H. Kim, D. Park, and Y. Joo, "All-digital low-power CMOS pulse generator for UWB system," *IEE Electron. Lett.*, pp. 1534–1535, Nov. 2004.
- [6] L. Smaïni, C. Tinella, D. Héral, C. Stoecklin, L. Chabert, C. Devaulcelle, R. Cattenoz, N. Rinaldi, and D. Belot, "Single-chip CMOS pulse generator for UWB systems," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1551–1561, Jul. 2006.

- [7] L. Stoica, A. Rabbachin, H. Repo, S. Tiuraniemi, and I. Oppermann, "An ultrawideband system architecture for tag based wireless sensor networks," *IEEE Trans. Veh. Technol.*, vol. 54, no. 9, pp. 1632–1645, Sep. 2005.
- [8] D. D. Wentzloff and A. P. Chandrakasan, "A 47 pJ/pulse 3.1–5 GHz all-digital UWB transmitter in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 118–119.
- [9] F. S. Lee and A. P. Chandrakasan, "A 2.5 nJ/bit 0.65 V pulsed UWB receiver in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2851–2859, Dec. 2007.
- [10] T. Norimatsu, R. Fujiwara, M. Kokubo, M. Miyazaki, A. Maeki, Y. Ogata, S. Kobayashi, N. Koshizuka, and K. Sakamura, "A UWB-IR transmitter with digitally controlled pulse generator," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1300–1309, Jun. 2007.
- [11] J. Ryckaert, G. V. der Plas, V. D. Heyn, C. Desset, G. Vanwijnsberghe, B. V. Poucke, and J. Craninckx, "A 0.65–1.4 nJ/burst 3–10 GHz UWB digital TX in 90 nm CMOS for IEEE 802.15.4a," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 120–121.
- [12] D. Marchaland, F. Badets, M. Villegas, and D. Belot, "65 nm CMOS burst generator for ultra-wideband low data rate systems," in *IEEE RFIC Symp. Dig.*, 2007, pp. 43–46.
- [13] Y. Zhu, J. D. Zuegel, J. R. Marciano, and H. Wu, "A 10 GS/s distributed waveform generator for sub-nanosecond pulse generation and modulation in 0.18 μm standard digital CMOS," in *IEEE RFIC Symp. Dig.*, 2007, pp. 35–38.
- [14] X. Chen and S. Kiaei, "Pulse generation scheme for low-power low-complexity impulse ultra-wideband," *IEE Electron. Lett.*, Jan. 2007.
- [15] P. P. Mercier, D. C. Daly, and A. P. Chandrakasan, "A 19 pJ/pulse UWB transmitter with dual capacitively-coupled digital power amplifiers," in *IEEE RFIC Symp. Dig.*, 2008, pp. 47–50.
- [16] D. D. Wentzloff and A. P. Chandrakasan, "Gaussian pulse generators for subbanded ultra-wideband transmitters," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, pp. 1647–1655, Jun. 2006.
- [17] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.
- [18] A. Oncu, B. B. M. W. Badalawa, and M. Fujishima, "22–29 GHz ultra-wideband CMOS pulse generator for short-range radar applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1464–1471, Jul. 2007.
- [19] D. C. Daly and A. P. Chandrakasan, "A 6b 0.2–0.9 V highly digital flash ADC with comparator redundancy," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 554–555.
- [20] B. P. Ginsburg and A. P. Chandrakasan, "Highly interleaved 5b 250 MS/s ADC with redundant channels in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 240–241.
- [21] A. Babakhani, D. B. Rutledge, and A. Hajimiri, "A near-field modulation technique using antenna reflector switching," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 188–189.
- [22] B. Razavi, K. Lee, and R.-H. Yan, "A 13.4-GHz CMOS frequency divider," in *IEEE ISSCC Dig. Tech. Papers*, 1994, pp. 176–177.
- [23] V. De Heyn, G. Van der Plas, J. Ryckaert, and J. Craninckx, "A fast start-up 3 GHz–10 GHz digitally controlled oscillator for UWB impulse radio in 90 nm CMOS," in *Proc. IEEE European Solid-State Circuits Conf. (ESSCIRC)*, 2007, pp. 484–487.
- [24] P. P. Mercier, D. C. Daly, M. Bhardwaj, D. D. Wentzloff, F. S. Lee, and A. P. Chandrakasan, "Ultra-low-power UWB for sensor network applications," in *Proc. IEEE ISCAS*, 2008, pp. 2562–2565.
- [25] *First Report and Order*, FCC 02–48, Feb. 2002.
- [26] Spectrum Analysis: Pulsed RF., Agilent Technol., Palo Alto, CA, Applicat. Note 150-2, May 2005.
- [27] W. Kissick, "The temporal and spectral characteristics of ultra-wide-band signals," NTIA, U.S. Dept. Commerce, Boulder, CO, Rep. 01-383, Jan. 2001.
- [28] T.-A. Phan, V. Krizhanovskii, and S.-G. Lee, "Low-power CMOS energy detection transceiver for UWB impulse radio system," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2007, pp. 675–678.
- [29] Y. Zheng, Y. Tong, J. Yan, Y.-P. Xu, W. G. Yeoh, and F. Lin, "A low power noncoherent CMOS UWB transceiver ICs," in *IEEE RFIC Symp. Dig.*, 2005, pp. 347–350.
- [30] V. Kulkarni, M. Muqsith, H. Ishikuro, and T. Kuroda, "A 750 Mb/s 12 pJ/b 6–10 GHz digital UWB transmitter," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2007, pp. 647–650.
- [31] Y. Zheng, M. A. Arasu, K.-W. Wong, Y. J. The, A. P. H. Suan, D. D. Tran, W. G. Yeoh, and D.-L. Kwong, "A 0.18 μm CMOS 802.15.4a UWB transceiver for communication and localization," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 118–119.

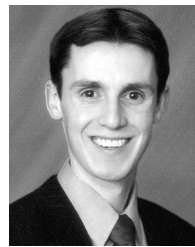


Patrick P. Mercier (S'04) received the B.Sc. degree in electrical and computer engineering from the University of Alberta, Edmonton, AB, Canada, in 2006, and the S.M. degree in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2008, where he is currently pursuing the doctoral degree.

From May 2008 to August 2008, he worked in the Microprocessor Technology Lab at Intel Corporation, Hillsboro, OR, designing spatial encoding and low-swing circuits for multi-core on-chip communi-

cation networks. His research interests include the design of energy-efficient RF circuits and digital systems for both wired and wireless communication applications.

Mr. Mercier was the recipient of a Natural Sciences and Engineering Council of Canada (NSERC) Julie Payette Fellowship in 2006, and the NSERC Postgraduate Scholarship in 2007.



Denis C. Daly (S'02) received the B.A.Sc. degree in engineering science from the University of Toronto, Toronto, ON, Canada, in 2003, and the S.M. degree from the Massachusetts Institute of Technology (MIT), Cambridge, MA, in 2005, where he is currently pursuing the doctoral degree.

From May 2005 to August 2005, he worked in the Wireless Analog Technology Center at Texas Instruments, Dallas, TX, designing transceiver modules. From May 2003 to August 2003, he worked on high-speed signaling systems at Intel Laboratories,

Hillsboro, OR. His research interests include low-power wireless transceivers, sensor networks, and highly digital RF and analog circuits.

Mr. Daly received the Natural Sciences and Engineering Research Council of Canada (NSERC) Postgraduate Scholarships in 2003 and 2005. He was awarded a Student Paper Prize at the 2006 RFIC Symposium, and won third place in the 2006 DAC/ISSCC Student Design Contest (Operational System Category).



Anantha P. Chandrakasan (F'04) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, in 1989, 1990, and 1994 respectively.

Since September 1994, he has been with the Massachusetts Institute of Technology, Cambridge, where he is currently the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering. He is the Director of the MIT Microsystems Technology Laboratories. His research interests include

low-power digital integrated circuit design, wireless microsensors, ultra-wideband radios, and emerging technologies. He is a coauthor of *Low Power Digital CMOS Design* (Kluwer Academic, 1995), *Digital Integrated Circuits* (Pearson Prentice-Hall, 2003, 2nd edition), and *Sub-threshold Design for Ultra-Low Power Systems* (Springer, 2006). He is also a coeditor of *Low Power CMOS Design* (IEEE Press, 1998), *Design of High-Performance Microprocessor Circuits* (IEEE Press, 2000), and *Leakage in Nanometer CMOS Technologies* (Springer, 2005).

Dr. Chandrakasan has been a corecipient of several awards, including the 1993 IEEE Communications Society's Best Tutorial Paper Award, the IEEE Electron Devices Society's 1997 Paul Rappaport Award for the Best Paper in an EDS publication during 1997, the 1999 DAC Design Contest Award, the 2004 DAC/ISSCC Student Design Contest Award, the 2007 ISSCC Beatrice Winner Award for Editorial Excellence and the 2007 ISSCC Jack Kilby Award for Outstanding Student Paper. He has served as a technical program co-chair for the 1997 International Symposium on Low Power Electronics and Design (ISLPED), VLSI Design'98, and the 1998 IEEE Workshop on Signal Processing Systems. He was the Signal Processing Sub-committee Chair for ISSCC 1999–2001, the Program Vice-Chair for ISSCC 2002, the Program Chair for ISSCC 2003, and the Technology Directions Sub-committee Chair for ISSCC 2004–2009. He was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1998 to 2001. He served on SSCS AdCom from 2000 to 2007 and he was the Meetings Committee Chair from 2004 to 2007. He is the Chair for ISSCC 2010.