Low-temperature germanium ultra-high vacuum chemical vapor deposition for back-end photonic integration

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Kevin A. McComber, Jifeng Liu, Jurgen Michel, *Member, IEEE,* and Lionel C. Kimerling, *Member, IEEE*

Abstract—**Polycrystalline germanium (poly-Ge) grown on amorphous Si (a-Si) by ultra-high vacuum chemical vapor deposition (UHVCVD) over oxide barriers at low temperatures (T≤450° C) exhibits a larger grain size and lower defect density than the as-grown poly-Ge next to the oxide barriers. Poly-Ge as deposited at 450° C is p-type, but the introduction of PH_3 during Ge deposition gives n-type poly-Ge with n=2.1x10^{18} cm^{-3}. The possible defect reduction and range of doping make poly-Ge a strong candidate for application to CMOS-compatible back-end photonic devices.**

***Index Terms*—Polycrystalline germanium, UHVCVD, grain engineering, lateral overgrowth**

I. Introduction

THE integration of photonic devices with electronic integrated circuits has emerged as a leading technology to continue the dimension shrink and the performance increase of microprocessors [1,2]. Germanium (Ge) has been identified as a promising material for the fabrication of CMOS-compatible photodetectors and modulators operating in the C telecommunications band (1520-1560 nm) [3]. Currently, such devices are made from Ge grown epitaxially on a single-crystal Si substrate at temperatures above 600° C [4,5]. However, these devices consume valuable real estate on the Si wafer substrate; in order to achieve dense electronic-photonic integration, it will be necessary to build back-end photonic devices while maintaining electronic devices at the substrate level. Figure 1 depicts the envisioned monolithic integration of a back-end photonic device.

Back-end processing dictates the use of low processing temperatures (≤450° C) as well as non-epitaxial growth for the photonic device fabrication. Previous researchers have attempted to fabricate poly-Ge photodetectors [6,7], but the devices have suffered from the high defect densities of the material. Increasing the poly-Ge grain size should decrease the grain boundary density, but the ability to engineer the grain size is severely restricted by the low-T requirement of back-end processing.

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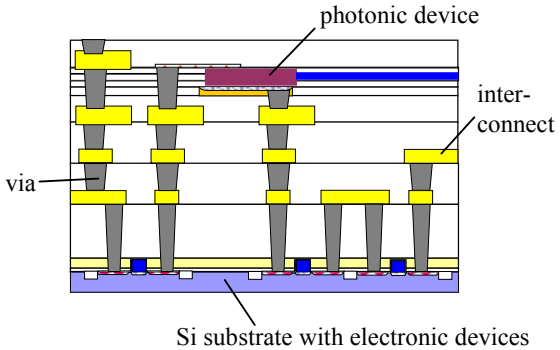

Fig. 1. Schematic of monolithic photonic plane integration using back-end processing.

Here, we present a method for engineering poly-Ge grains at temperatures ≤450° C, using selective growth of Ge on a-Si by UHVCVD.

II. Experimental Procedure

A 6" p-type (100) Si wafer was thermally oxidized to produce a 500 nm oxide layer on the Si. 50 nm of a-Si was then deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350° C and 200 nm of PECVD SiO_2 was deposited on the a-Si at 400° C. The PECVD oxide was patterned by photolithography and dry etching with reactive ion etching to expose the underlying Si in features with dimensions on the order of 1 μm. The wafer was RCA cleaned and loaded into a hot-walled UHVCVD chamber idling at 450° C and <10^{-8} Torr. The wafer was annealed for 3 hours at temperatures up to 450° C to degas hydrogen from the PECVD a-Si and oxide. GeH_4 was subsequently flowed at 10 sccm for 100 minutes at 360° C and then at 7.5 sccm for 8 hours at 450° C for selective Ge deposition on the a-Si. The wafer was then removed from the growth chamber and allowed to cool to room temperature before being removed from vacuum.

In a separate experiment, blanket poly-Ge was grown on a-Si by flowing 7.5 sccm GeH_4 and 0.5 sccm PH_3

simultaneously for 4 hours at 450° C in UHVCVD.

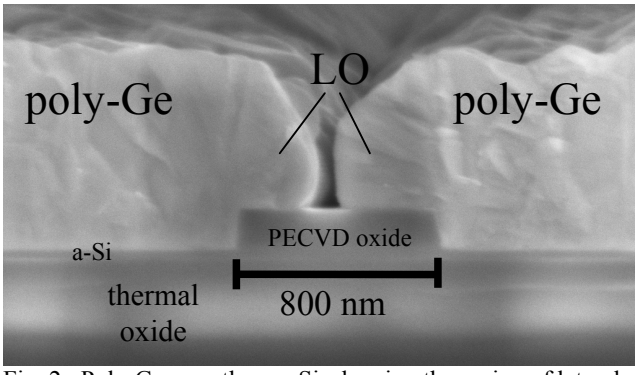

Fig. 2. Poly-Ge growth on a-Si, showing the region of lateral overgrowth (LO) over the PECVD oxide.

III. Results and Discussion

Figure 2 shows a cross-section scanning electron microscope (SEM) image of the poly-Ge growth. We observe that the poly-Ge grows selectively on the a-Si but also grows laterally over the PECVD oxide barriers; this will be called lateral overgrowth (LO). At 450° C in UHVCVD, the poly-Ge grows at approximately 100 nm/hour, so 8 hours of growth is barely enough to grow the poly-Ge across the oxide barriers. While the LO regions in Figure 2 did not coalesce, the regions did coalesce in other areas of the same sample, thus showing some variation in processing results.

Figure 3 shows a cross-section transmission electron microscope (TEM) image of two coalesced LO regions as well as the as-grown poly-Ge region. Using the image's heterogeneous strain contrast (striations) as a measure of defect density, it is apparent that the LO region has less heterogeneous strain density and thus a lower defect density than does the as-grown region.

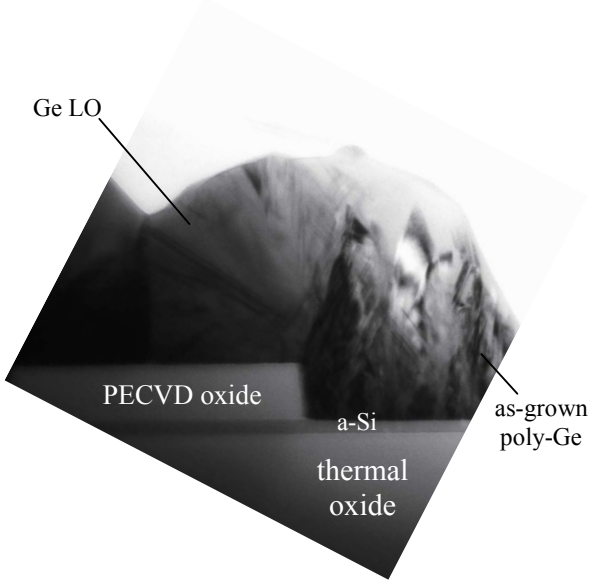

Fig. 3. TEM image of the LO region and the as-grown poly-Ge region.

From Figure 3, it is evident that the character of the poly-Ge changes dramatically between the as-grown region and the LO region. The LO region growth can be envisioned as simultaneous horizontal and vertical polycrystalline homoepitaxy, with the grains in the as-grown region serving as the vertical substrate for horizontal growth over the PECVD oxide. Since poly-Ge does not deposit on the oxide itself, the growth that originates at the sides of the as-grown poly-Ge grains can continue uninhibited across the full width of the PECVD oxide barrier. Homoepitaxial Ge growth also occurs vertically on these horizontally-growing grains.

From observing the LO region with a double-tilt TEM sample holder, which allows the sample to be rotated while in the TEM, we noted two distinct areas in the LO region that appear to change independently of each other. This is interpreted as either two distinct grains in the observed LO region or one grain with a twin boundary. In contrast, there are several observable distinct grain boundaries and/or twin boundaries in the as-grown region. Additionally, the interface of the LO Ge and the PECVD oxide appears smooth in Figure 3, but more work will be done to determine the nature of the interface between the coalesced LO regions.

Due to the electrical activity of the grain boundaries [8], our as-deposited blanket poly-Ge is p-type with $p=1.9\text{x}10^{18}$ cm^{-3}. By flowing PH_3 during the Ge deposition process at 450° C, we have attained blanket poly-Ge films with $n=2.1\text{x}10^{18}$ cm^{-3}. This study has convinced us that the complete range of n- and p-type doping necessary for photonic and electronic poly-Ge devices is possible at low T.

IV. Conclusion

Poly-Ge was grown at 450° C over oxide barriers of approximately 800 nm in width. The growth was examined with SEM and TEM, and we observed in TEM that the LO has a lower defect density and larger grain size than adjacent as-grown poly-Ge. We also achieved n-type doping of blanket poly-Ge. The lowered defect density and range of possible doping make LO poly-Ge applicable for CMOS-compatible back-end photonic device fabrication.

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