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# Characterization of Three-Dimensional-Integrated Active Pixel Sensor for X-Ray Detection

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**Abstract**—We have developed a back-illuminated active pixel sensor (APS) which includes an SOI readout circuit and a silicon diode detector array implemented in a separate high-resistivity wafer. Both are connected together using a per-pixel 3-D integration technique developed at Lincoln Laboratory. The device was fabricated as part of a program to develop a photon-counting APS for imaging spectroscopy in the soft X-ray (0.3–10-keV) spectral band. Here, we report single-pixel X-ray response with spectral resolution of 181-eV full-width at half-maximum at 5.9 keV. The X-ray data allow us to characterize the responsivity and input-referred noise properties of the device. We measured inter-pixel crosstalk and found large left–right asymmetry explained by coupling of the sense node to the source follower output. We have measured noise parameters of the SOI transistors and determined factors which limit the device performance.

**Index Terms**—Active pixel sensor (APS), correlated double sampling (CDS), interpixel coupling, readout noise, X-ray,  $1/f$  noise.

## I. INTRODUCTION

ACTIVE PIXEL sensors (APSS) are being developed for a rapidly growing number of imaging applications in response to dramatic improvements in sensor performance. One area of recent interest is direct spectrally resolved photon-counting imaging in the soft X-ray (0.3–10-keV) band. This application is vital for high-energy astrophysics and, at the moment, is entirely dominated by charge-coupled devices (CCD). In principle, APSS offer a number of advantages over CCDs in this role. Several of these advantages stem from the much higher readout rates, for a given level of power consumption, promised by APSS. They include better time resolution, higher count-rate capability, less demanding (or no) requirements for detector cooling, and better tolerance for out-of-band (mainly visible) stray signal. The latter feature may allow thinner out-of-band blocking filters and, therefore, better in-band detection efficiency. Since APSS do not transfer charge over significant distances, they do not suffer the CCD's sensitivity to radiation-induced displacement damage in the space environment in which X-ray observatories must function. Finally, to the extent that APSS can be integrated with downstream analog and digital

signal processors, they may facilitate astronomical instruments with higher throughput, that are lighter, consume less power, and cost less.

X-ray imagers for scientific applications differ from commercial visible light sensors in several respects. Efficient X-ray photon detection requires a much thicker photosensitive volume because X-rays in this band are generally more penetrating than visible photons. Good X-ray detection efficiency also requires back illumination, since refractive optics cannot be used to compensate for the lower fill factor of front-illuminated devices. Excellent charge collection efficiency is required for good X-ray spectroscopic performance, and this implies that the photosensitive volume must be fully depleted. Very low read noise is essential to measure the very small charge packets (on the order of  $10^2$ – $10^3$  electrons) deposited by X-ray photons.

Substantial progress toward these goals has been achieved at MPI Halbeitahtator (see [1]). These devices combine a fully depleted silicon detector and a unique charge-sensing structure on different sides of a single silicon wafer. Another approach has been pursued by Teledyne [2], which is developing hybrid detectors with silicon photodiodes mated to CMOS readout circuitry initially developed for IR light detection. Very recently, impressive X-ray results have been reported by Sarnoff [3], which has developed a monolithic sensor with CMOS circuitry built on a high-resistivity epitaxial silicon layer of which approximately  $15\ \mu\text{m}$  is depleted.

In this paper, we describe the results from a hybrid detector that was built using 3-D integration technology developed at MIT Lincoln Laboratory (see [4] for details of this technology). A silicon diode array is fabricated in one wafer (or “tier”) and then integrated with CMOS readout circuitry on a separate SOI wafer from which the substrate has been removed. This scheme allows much tighter integration than other hybrid technologies, and since more than two tiers can be stacked together, its signal processing capabilities are almost limitless. The potential advantages offered by this approach include the design flexibility of the hybrid architecture, allowing detector and readout circuitry to be optimized independently, a relatively low-capacitance intertier connection, and, because multiple tiers can be stacked, the capability to integrate significant signal processing capabilities in a low-power four-side abutable device. Here, we report the first X-ray performance data from a sensor fabricated with this technology.

## II. DEVICE DESCRIPTION

The device is an array of  $256 \times 256$  pixels. The pixel size is  $24 \times 24\ \mu\text{m}^2$ , which is typical for scientific X-ray sensors. It

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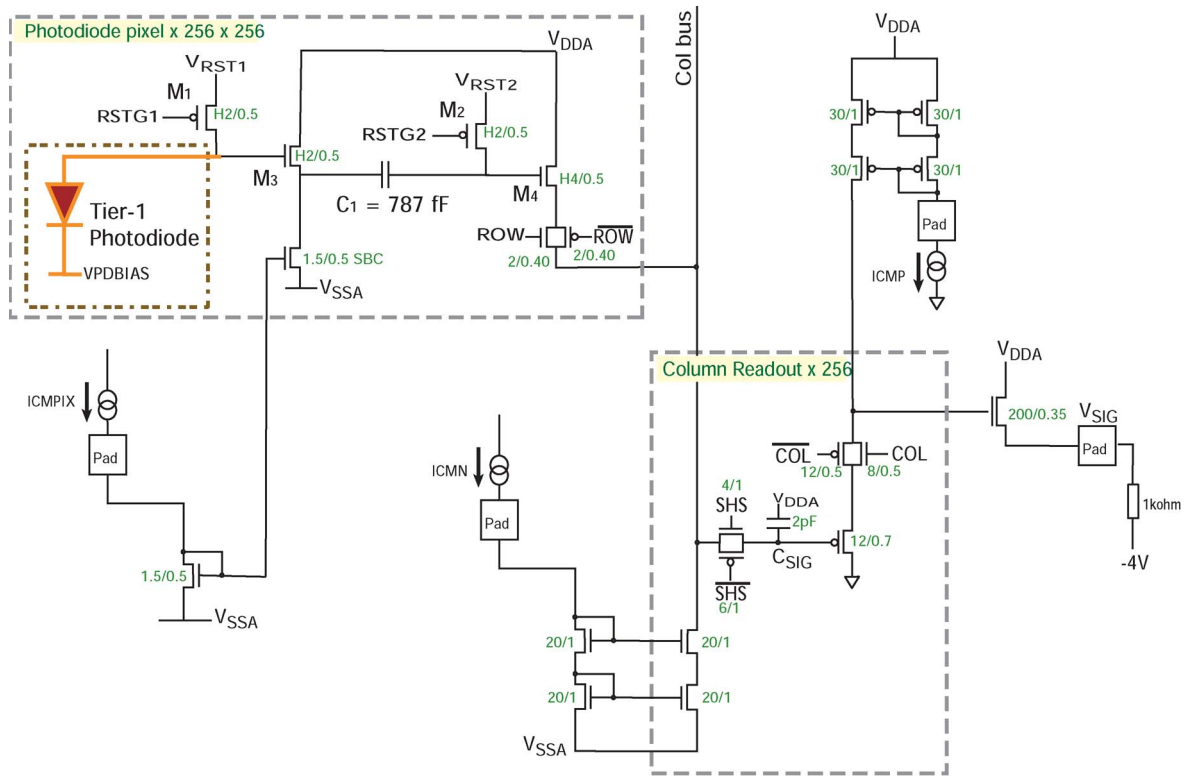


Fig. 1. Schematic of the described device. Only signal readout chain is shown here; row and column decoders are omitted.

includes two separate tiers—a photodiode made on an n-type high-resistivity substrate ( $3000 \Omega \cdot \text{cm}$ ) and an SOI CMOS readout circuit. On the side that is connected to the CMOS readout, the diode has circular p+ islands, each of them being  $10 \mu\text{m}$  in diameter. They are surrounded by n+ channel stop regions that separate pixels. The wafer is thinned to  $50 \mu\text{m}$ . The illuminated side is doped with phosphorus and then laser annealed. The p+ region of each diode is connected by a tungsten plug to the gate of the NMOS transistor in the SOI readout circuit, implemented on a different wafer. The details of the integration of the photodiode wafer with the readout tier were described elsewhere [4]. During operation, the n+ regions of the diode are connected to a positive voltage with the intention to fully deplete the entire volume.

The SOI CMOS is fabricated in a 350-nm gate length technology with 3.3-V operating voltage. The device schematic is shown in Fig. 1. Its pixel includes two stages. The first one contains a sense-node reset transistor  $M_1$  and a source follower. The second stage, separated by a large capacitor  $C_1$ , is introduced in order to reduce reset noise, as described in [5] and [6]. This in-pixel capacitor is formed between a doped polysilicon gate and SOI active regions, separated by a thin oxide (7.2 nm). We estimate a 787-fF value from the layout.

A significant advantage of the SOI technology is the possibility to use both n- and p-channel transistors in the pixel. We used p-channel transistors as reset switches, thus avoiding the problem of dealing with “soft reset” lag. In order to minimize parasitic leakage paths, an H-gate geometry was utilized for all the transistors in the pixel. We have also found that such transistors have substantially lower noise (see Section III-E).

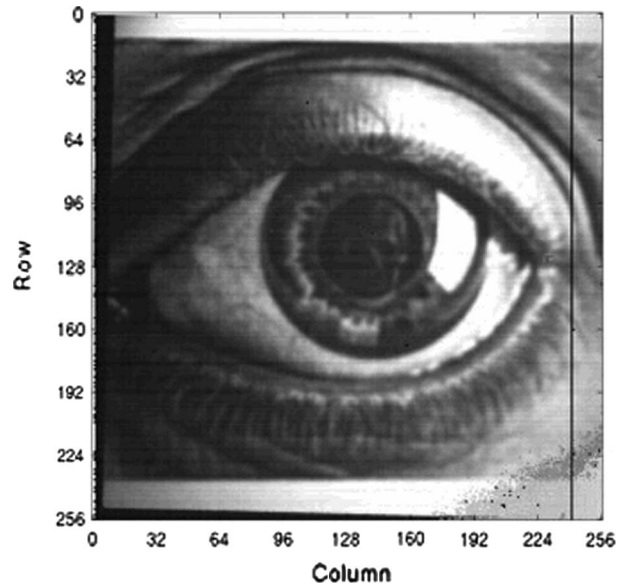


Fig. 2. Optical image produced by the device.

### III. DEVICE PERFORMANCE

The entire device is functional; a sample of an optical image taken at room temperature is shown in Fig. 2. We found that achieving satisfactory X-ray performance is a much more challenging task for a number of reasons. A very detailed characterization of device parameters was undertaken in order to better understand the limitations of the current design. The results are described in the following sections.

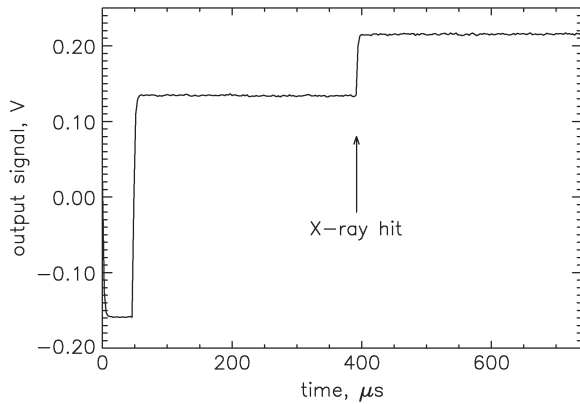


Fig. 3. Sequential 260 samples of signal at the output of the sensor showing reset pulse and an X-ray hit. The sampling frequency in this case was 350 kHz.

#### A. X-Ray Performance

X-ray detection may be the most demanding test of the quality of a detector. In order to get high-energy resolution, signal losses of any type have to be negligible. Since the signal is very small, the noise level also needs to be very low. When an entire array is clocked out, pixel nonuniformities of all kinds mask the intrapixel X-ray performance and make it difficult to diagnose the limits of the technology, which was the purpose of this paper. For this reason, we focused mainly on single-pixel testing. We have been able to achieve very good X-ray performance, and that has allowed us to measure many parameters with accuracy that is not achievable by other means.

For the X-ray tests described here, we chose a mode in which one pixel was reset once while the output signal was sampled multiple times. The total number of samples per reset was 260, with 16 of those samples taken during reset. A typical set of data points, including one full period from one reset pulse to another and containing an X-ray event, is shown in Fig. 3. X-ray amplitude was determined by averaging ten readout samples before the X-ray hit and ten samples after and then taking the difference of the averages. In such a mode, the reset noise is suppressed since all the samples before and after an X-ray event are taken during one reset cycle; the sense node is not being reset between those samples. This is an analog of the correlated double sampling (CDS) readout, although, here, the processing of double samples (or, in fact, multiple samples) is done in the digital form in the computer, not in the analog domain, as it is traditionally done. Moreover, in this mode, most of the  $1/f$  noise is eliminated because an interval containing 20 samples is short compared to the time corresponding to frequencies below the  $1/f$  knee (see Section III-D). The white noise component is also significantly reduced by averaging repeated readout samples before and after an X-ray hit.

We determined the equivalent noise of this measurement by applying the same procedure that is used for X-ray pulse-height computation to the readout sequences without X-rays. Every time an X-ray is detected, a reset cycle that is ten reset pulses prior to this hit is analyzed; ten samples before and ten samples after the sample that corresponds to the hit are averaged, and the averages are subtracted. A histogram of these nonexistent events produces a peak around zero, and its width is the noise of

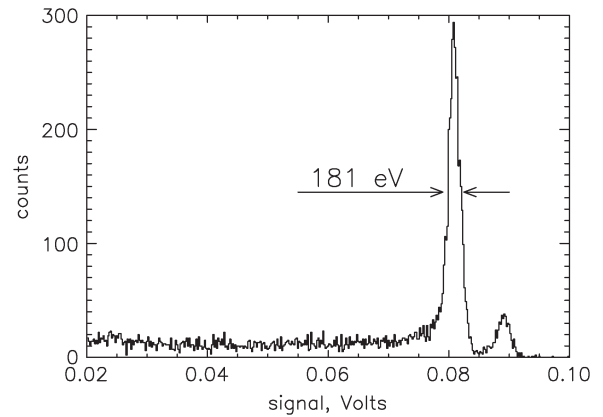


Fig. 4. Histogram of X-ray events collected by a device illuminated by an  $\text{Fe}^{55}$  source. The FWHM of the Mn  $K_{\alpha}$  line at 5.89 keV is 181 eV.

such measurement, which was determined to be 12.6 electrons rms. Conversion into electrons is based on the location of the 5.89-keV line, a result that is described hereinafter.

Fig. 4 shows a histogram of the X-ray events accumulated when the chip was illuminated by  $\text{Fe}^{55}$  radioactive source. Characteristic  $K_{\alpha}$  and  $K_{\beta}$  emission lines of Manganese at 5.89 and 6.4 keV are very well resolved. The energy resolution of  $K_{\alpha}$  line of 181-eV full-width at half-maximum (FWHM) is close to the Fano factor limited resolution of 162 eV for the readout noise level of 12.6 electrons, clearly indicating that charge collection efficiency is very high. This is particularly remarkable since this is a histogram of all events exceeding a certain threshold; no selection of events has been made based on the analysis of the signal amplitude in the adjacent pixels. Our previous experience with X-ray detection in CCDs suggests that excluding the so-called split events (the ones that have charge in two or more neighboring pixels) can noticeably improve energy resolution.

The X-ray data presented here were acquired with the detector cooled to  $-60^{\circ}\text{C}$ . While X-rays are reliably detected at room temperature, we found that energy resolution improves at lower temperature. A behavior strongly resembling charge trapping and detrapping is observed at elevated temperatures, the result being degradation of spectral resolution. The exact mechanism that is responsible for this phenomenon is not clear at this point; further investigation is planned.

Once the X-ray peak is found, it is easy to calculate the responsivity and the sense-node capacitance of the detector. The responsivity was calculated to be  $4.6 \mu\text{V}/\text{electron}$ , and the node capacitance is 24.7 fF when the voltage applied to the charge-collecting photodiode is 18 V. In order to accurately determine the sense-node capacitance, one needs to know the gain of all the chains between the sense node and the output. This was measured by finding the response of the output to a known signal applied to the reset drain while the reset gate is grounded.

#### B. Interpixel Coupling

Another detector feature that can be very accurately evaluated by studying X-ray response is interpixel interaction. It has been shown [7]–[9] that adjacent pixels in hybrid detectors can exhibit substantial crosstalk due to interpixel capacitance.

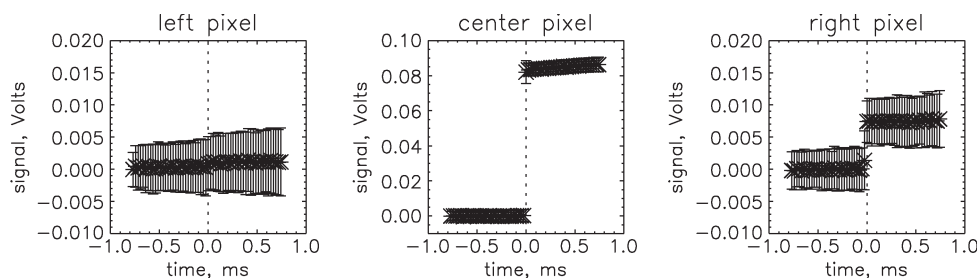


Fig. 5. Averaged signal time profiles in three adjacent pixels corresponding to an X-ray event in the center pixel. Note the different vertical scale for the pixels on the sides.

A popular method to measure this crosstalk is pixel correlation analysis [9]–[11]. This involves a complex mathematical treatment and, importantly, assumes symmetrical crosstalk to the left and to the right. We found that the latter assumption is not valid in our sensor. X-ray detection is a direct and precise way to study interpixel interaction, because in this case, a known quantity of signal charge is instantaneously deposited in a pixel. The reactions of that pixel and the adjacent ones to this stimulus can provide the desired parameters.

To measure interpixel crosstalk, we employed a mode that is very similar to the one described in the previous section for single-pixel testing but extended it to include multiple pixels. Four pixels in the same row were held in reset, and then each of them was read out one after another. The cycle of reading out four sequential pixels was repeated 130 times without resetting any of them. The device was illuminated by an  $\text{Fe}^{55}$  source. For each of the four pixels, X-ray events were selected based on threshold crossing criterion, and then, to determine the amplitude, we applied the same algorithm that was developed for single-pixel event processing. As explained in Section III-A, this leads to very significant reduction of noise. For each of the four pixels, a signal histogram that is similar to the one shown in Fig. 4 was made.

One of the mechanisms that can certainly produce crosstalk is charge splitting between adjacent pixels in the photodiode due to carrier diffusion. This occurs when a cloud of photo-generated signal carriers is formed near a pixel boundary or in undepleted portions of the photodiode. We clearly detect charge splitting (most of the events in the low-energy tail below the peak in Fig. 4 are due to charge diffusion losses), but in order to measure interpixel capacitance, we need to exclude charge diffusion effects. To do this, only events with amplitudes that are above the centroid of the peak in the histogram were considered. Such events must be single-pixel events for which signal charge is fully collected, since, otherwise, they would have lower amplitude. For all the events thus selected, an average event time profile was constructed by shifting the times of all the X-ray hits in a given pixel to the same artificial zero time point and then averaging signal values at each sampling time. The result for the second of the four pixels is shown in Fig. 5 in the middle panel. Since signal values in adjacent pixels were recorded (with one sample time shift), it is easy to trace the average signal amplitude there also. The corresponding plots are shown for the left and the right pixels in the same figure. The signal in the adjacent pixels jumps at the time of the photon arrival in the center pixel, clearly indicating crosstalk.

The crosstalk signal is very different in the left and right pixels. On the left side, the level of crosstalk is very small (only 0.85%), while on the right, it is 8.8%. We verified this result by reversing the addressing sequence and reading columns in the opposite direction. This did not affect the observed asymmetry. One conclusion from the nonsymmetrical reaction to a given stimulus is that, unlike in the Teledyne devices [9], the crosstalk in our structure cannot originate in the photodiode, because the diode structure is perfectly symmetrical. Neither can it come from the capacitance between the adjacent tungsten plugs that connect photodiode with the SOI readout; such capacitive crosstalk would be identical on both sides.

Our analysis of the pixel layout led us to a conclusion that the relatively large crosstalk on the right side can be explained by the capacitance between the output of the first source follower and the sense node of the adjacent pixel. The large capacitor  $C_1$  is located on the right-hand side of the pixel, close to the sense node of the pixel on the right and far from the sense node on the left. Thus, the signal on the sense node raises the voltage at the outputs of the pixel source followers, and that rise, through capacitive coupling, causes voltage change on the floating sense node of the adjacent pixel on the side that is nearby. The output of source follower on the left-hand side is not affected (in spite of the capacitive coupling) because its potential is not floating; it is defined by the voltage at its input connected to the relatively remote sense node on the left.

Since the sense-node capacitance is known (see the previous section), it is not hard to calculate the cross-coupling capacitance from the corresponding capacitive divider. Its value is 2.1 fF. This can be substantially reduced with certain changes in pixel layout that are under consideration for the next-generation design.

### C. Sense-Node Capacitance

The sense-node capacitance includes two components connected in parallel: the input capacitance of the readout circuit and the capacitance of the charge-collecting photodiode. The capacitance of the photodiode is a strong function of the voltage applied to the p-n junction, while the circuit capacitance is decoupled from it (see pixel schematic shown in Fig. 1). This presents an interesting opportunity to separate the contribution of these components by varying the voltage applied to the photodiode. The result of such measurement is shown in Fig. 6. Each experimental point on this plot was produced by acquiring substantial amount of data at a given voltage applied to the

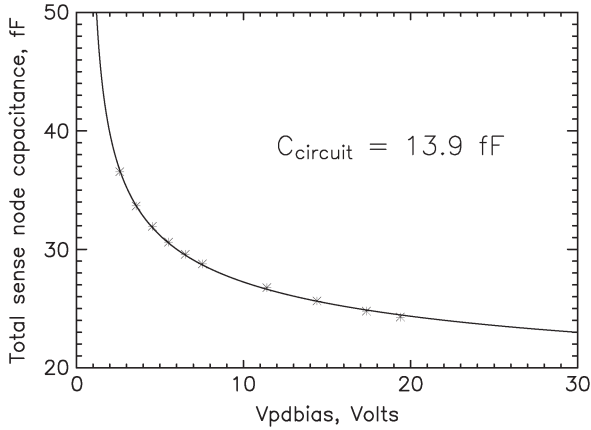


Fig. 6. Sense-node capacitance measured with  $\text{Fe}^{55}$  X-rays at different voltages applied to the photodiode. Stars indicate experimental data points; solid line is the best fit function describing capacitance of the p-n junction with linearly graded dopant distribution.

photodiode with  $\text{Fe}^{55}$  source illuminating the device. Capacitance values were extracted from the location of the 5.89-keV line. The capacitance data points were then approximated by an analytical expression describing capacitance as a function of voltage in the following form:

$$C_{\text{node}} = C_{\text{circuit}} + \frac{k_0}{\sqrt[3]{V - V_i}} \quad (1)$$

where  $C_{\text{node}}$  is the total sense-node capacitance,  $C_{\text{circuit}}$  is the capacitance of circuit component,  $k_0$  is a constant determined by junction parameters,  $V$  is the voltage applied to the photodiode, and  $V_i$  is the built-in voltage of the p-n junction. The aforementioned equation describes the capacitance of the junction with linearly graded distribution of dopant (in parallel with the voltage-independent circuit component  $C_{\text{circuit}}$ ), and it fits the experimental points reasonably well. The free parameters in fitting process were  $C_{\text{circuit}}$  and  $k_0$ . The best fit value of the circuit capacitance  $C_{\text{circuit}}$  is 13.9 fF. We found that the more common expression for an abrupt junction produces a much poorer fit to the data. This makes sense once the details of the diode structure are taken into account.

A cross section of the photodiode is shown in Fig. 7. The central p+ region is surrounded by a phosphorus doped n+ channel stop. The phosphorus implantation was made through a mask that was tapered near the edge in order to reduce the dopant concentration near the junction. That is the reason why (1) results in a much better fit than the expression for an abrupt junction. More accurate simulation should, of course, take into account the 3-D nature of the problem. Our estimates and numerical simulations indicate that the channel stop region surrounding the central p+ diode (the corresponding capacitance denoted as  $C_{\text{ch-stop}}$  in Fig. 7) entirely dominates the diode capacitance (a total of 10.4 fF at 18 V applied to the diode), while the capacitance between the p+ region and the opposite n+ plate,  $C_{\text{depl}}$  in Fig. 7, constitutes approximately 1.5 fF when the diode is fully depleted.

This explains why there is no obvious knee point on the  $C$ - $V$  curve in Fig. 6 corresponding to the transition from the partially depleted state to the full depletion of the photodiode.

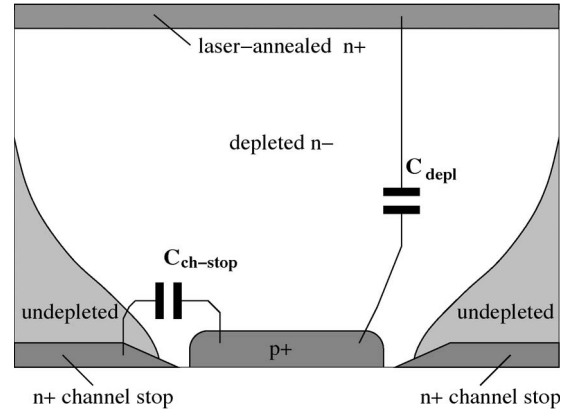


Fig. 7. Cross section of the photodiode tier.

While such a transition should occur at approximately 10 V, as indicated by the simulations, and should be reflected as diminished rate of change of  $C_{\text{depl}}$  as a function of voltage, the large value of  $C_{\text{ch-stop}}$  makes it unobservable. In the next iteration of the sensor design, the diode capacitance will be significantly diminished.

The components that contribute to the 13.9 fF of  $C_{\text{circuit}}$  are the capacitance of the tungsten plug which connects the diode to the CMOS circuit and the input capacitance of this circuit. Calculations indicate that the input capacitance of the transistor  $M_3$  after taking into account the Miller effect (diminishing gate to source capacitance by a factor of  $(1 - A_1)$ , where  $A_1$  is the source follower gain) constitutes approximately 1.5 fF. Together with source-to-gate capacitance of the reset transistor  $M_1$ , which was determined from the amplitude of the reset feedthrough to be 0.6 fF, they form approximately 2 fF of transistor-related circuit input capacitance.

We believe that the rest of  $C_{\text{circuit}}$  is due to the capacitance of the tungsten plug to the nearby metal lines in the circuit. As described in Section III-B, we have determined that the capacitance between the tungsten plug and the adjacent metal line that connects capacitor  $C_1$  and the gate of transistor  $M_4$  is 2.1 fF. We have also found that there is a capacitive coupling between the signal line RSTG2 and the sense node; the measured feedthrough amplitude allows one to deduce that the corresponding capacitance is also approximately 2.2 fF. There are other lines, coupling to which is not directly measurable, but the capacitance values must be close to the ones that we have determined. The conclusion here is that pixel layout must be done very carefully in order to minimize all those capacitances. There certainly is enough room in a pixel to significantly reduce them, and that could result in a much better device sensitivity.

#### D. Noise Measurements

Readout noise is a key factor in the detection of miniscule charge packets produced by X-ray photons. When an entire array is clocked and read out, it is very difficult to diagnose what the contributions of different noise components are and which portions of the device introduce them. However, we found that reading out a single pixel repeatedly allows one to do very elaborate studies of noise sources in the device. This mode of operation allowed us to demonstrate very decent

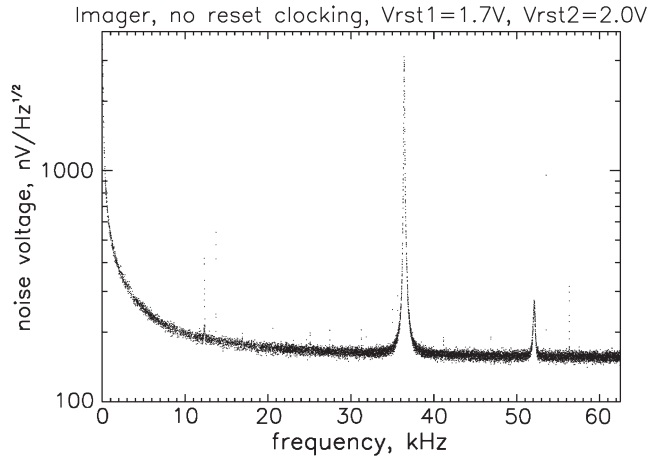


Fig. 8. Noise spectrum of the source followers. No clocks on the chip are running. Reset and SHS transistors in the conductive state.

X-ray performance, as described in Section III-A; we also found it extremely useful for noise characterization.

The most basic test that can be done in this regime is to hold the gates of both reset transistors  $M_1$  and  $M_2$  at low voltage (for the p-channel reset transistors, this means that the channel is conducting all the time), turn on sample-and-hold transistors, and sample output signal multiple times. No signals are clocked on the entire chip. The state of signal RSTG1 actually does not matter because the source of the transistor  $M_2$  is connected to a constant voltage VRST2. Variations of the output signal in such a regime are caused entirely by the noise introduced by the three source followers downstream the voltage source VRST2.

The output signal was read out  $65536 = 2^{16}$  times every  $8 \mu\text{s}$  (125 kHz), and the values were recorded in a computer. For convenience, we will call such a set of data a single frame. The entire process was repeated multiple times, with a large number of single frames acquired. For each frame, a fast Fourier transform was performed. Spectrum averaged over 500 frames is shown in Fig. 8. Measured spectrum is the spectrum of noise produced by all the MOSFETs in the source followers downstream the VRST2 voltage source.

The shape of the spectrum shows a strong  $1/f$  component, which is not too surprising for a MOSFET circuit. A sharp line at 36.5 kHz is an artifact of the measurement system; it was produced by a computer monitor. The  $1/f$  component in the acquired data presents itself as signal dc level changes that occur randomly on the scale of hundreds or thousands of pixels. We found that dividing each frame into groups of 256 sequential pixels and subtracting a median of the pixel values in each group make the histogram of the entire data much narrower, and such a histogram takes a Gaussian shape (a histogram is shown in Fig. 9). We use the width of such histograms as a measure of device noise for the tests described in this section. This procedure of group-based median subtraction (the group size of 256 samples was chosen for convenience; it is more or less arbitrary number) is equivalent to removing noise components with frequencies below  $125 \text{ kHz}/256 = 488.3 \text{ Hz}$ . In this respect, the procedure is somewhat similar to the CDS made outside the chip, which would also suppress  $1/f$  noise. The width of the Gaussian was converted into electrons using the results

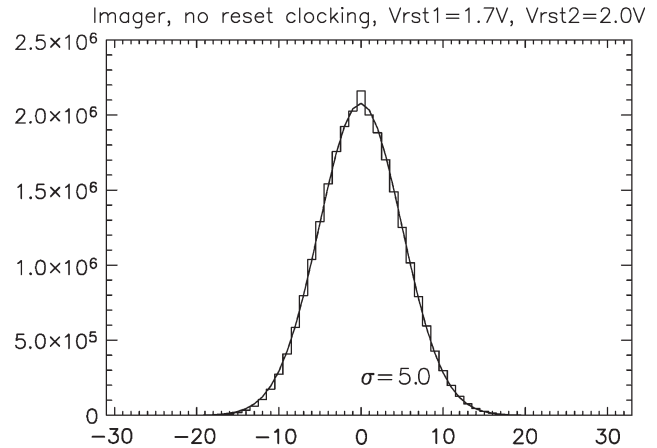


Fig. 9. Histogram of the signal at the imager output. No clocks are running. Reset and SHS transistors in the conductive state. For each group of 256 pixels, a median of the signal values is subtracted in order to suppress the  $1/f$  noise seen in the previous plot. This explains why the histogram is centered around zero.

TABLE I  
SENSE-NODE REFERRED NOISE IN DIFFERENT CLOCKING REGIMES

Regime	Noise, electrons rms	
	measured	calculated
No clocking	15.6	-
SHS only	14.6	17.5
Rstg2 only	24.9	19.7
Rstg1+Rstg2 reversed	61.7	65.1
X-ray operation	12.6	-

of the sense-node calibration with X-rays, as described in Section III-A. The results of noise measurements expressed in electrons rms referred to the input node for this, and subsequent measurements are summarized in Table I. The numbers there were calculated assuming a sense-node capacitance of 24.7 fF (18 V applied to the photodiode) and a source follower gain of 0.932 (it was measured by applying signal to the reset drains). The resulting 15.6 electrons of noise is mostly white noise produced by the source follower transistors. The measured source follower noise is much higher than anticipated. The reasons for that noise and a way to improve it are explained in Section III-E.

We applied the same technique of continuous sampling of the output with no signals applied to measure reset noise introduced at different stages of readout circuitry. In the next experiment, we tested whether the sample-and-hold transistors introduce reset noise when they turn off to store charge on the  $C_{\text{sig}}$  capacitor. Once again, both RSTG1 and RSTG2 were held low, but this time, the SHS gates were clocked. For the large 2-pF sample-and-hold capacitor expected reset voltage noise  $kT/C$  can be calculated to be  $45 \mu\text{V}$ , which is equivalent to 8.1 electrons if referred to the sense-node capacitance  $C_{\text{node}}$ . To refer the noise to the sense node, voltage signal  $N_v$  at the sample-and-hold capacitor should be translated to the sense node. To do this, it has to be divided by corresponding gains of two stages between these nodes,  $A_1$  and  $A_2$ , and then converted to equivalent number of electrons  $N_e$

$$N_e = \frac{N_v}{qA_1A_2} C_{\text{node}} \quad (2)$$

where  $q$  is the electron charge. Since the noise is summed in quadrature, its contribution is small compared to the source follower noise measured earlier. The total noise measured in this mode is about the same as that without clocking sample-and-hold gates, which is probably explained by limited accuracy of the measurement system. One well-known fact that becomes very obvious from (2) is that input-referred noise is directly proportional to the sense-node capacitance and that its reduction helps both to reduce the noise and to increase the signal.

Clocking signal RSTG2 will introduce the  $kT/C$  noise of resetting the large blocking capacitor  $C_1$ . In the voltage domain, calculation of  $kT/C$  predicts  $72.5\text{-}\mu\text{V}$  rms at the input of the second source follower (gate of  $M_4$ ). Referred to the sense node, that is equivalent to 12 electrons of noise rms. Since we can only measure that noise coupled together with the noise of the source followers, the expected number is  $\sqrt{12^2 + 15.6^2} = 19.7$  electrons rms. The measurement yielded 24.6 electrons, which, while not the same, is not too far off. One possible explanation of this discrepancy could be that the real value of the blocking capacitor may be somewhat different from the one intended in the design stage.

Finally, clocking both reset transistors  $M_1$  and  $M_2$ , but in a mode where  $M_2$  shuts off earlier than  $M_1$ , should result in the noise of resetting the small sense-node capacitance being brought to the chip output. The calculated value of  $kT/C$  in this case is 63.2 electrons rms or, with noise of source followers added to that, 65.1 electrons. Our measurement yielded a very close value of 61.7 electrons rms. This result is consistent with the measurement of the sense-node capacitance described in Section III-C. As expected for reset noise, the spectrum of the output signal is white.

The last line in the table shows the equivalent noise achieved in our X-ray measurement described earlier in Section III-A. As explained there, to perform that measurement, relatively complicated analysis was implemented to beat down each of the noise components.

These experiments helped us to identify the main bottlenecks that resulted in relatively high values of noise in the current design. The most critical parameter that clearly needs to be improved because, in fact, it determines all the noise levels, when referred to the input, is the sense-node capacitance. Another problem is unexpectedly high noise of the source followers, and it motivated us to further investigate where it comes from.

### E. Transistor Noise

We measured the noise spectra of individual transistors that constitute the SOI circuit readout chain using a wafer-level probe setup with ground-signal-ground probes. The transistor gate was biased with an Agilent 3631A power supply through a low-pass filter. The transistor drain was biased using Stanford Research System SR570 Low Noise Current Preamplifier. An Agilent 3567A spectrum analyzer was used to acquire the voltage noise. The instrumentation setup and lab environment had a usable range of 0.4–100 kHz.

The floating body of SOI transistors introduces additional components to the low-frequency noise observed in bulk

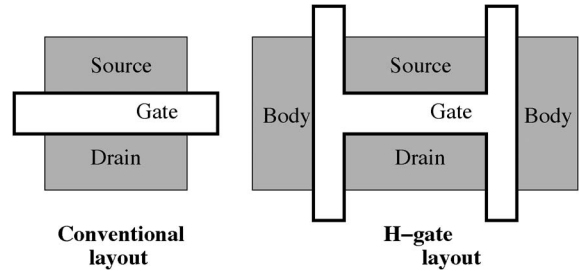


Fig. 10. Two configurations of SOI transistors used in the current design.

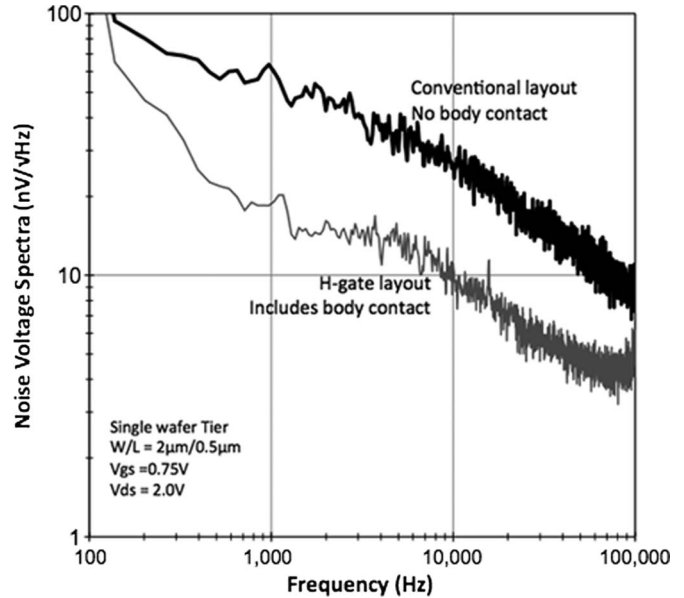


Fig. 11. Comparison of noise spectra of an H-gate transistor and a conventional layout transistor before 3-D integration.

MOSFETs [12]. Under bias conditions that create a high electric field near the drain, majority carriers, generated by impact ionization, will accumulate in the transistor body, lower the threshold voltage, and lead to the so-called “kink effect.” This effect can be suppressed through the use of body contacts that provide a path for the majority carriers to be evacuated from the transistor channel.

One method to implement a body contact is through an H-gate layout. Fig. 10 compares a conventional SOI transistor layout to an H-gate layout. The conventional layout is substantially more compact and has lower gate-to-source and gate-to-drain capacitances, an important consideration for the sense node. However, this layout contains a parasitic island-sidewall transistor leakage path that can degrade pixel dark current if the island sidewall threshold is too low or if the sensor is subjected to ionizing radiation.

We implemented an H-gate layout for both reset transistors and source follower transistors in the pixel. The H-gate layout provides a body contact that can suppress the “kink effect” and does not contain a parasitic island-sidewall transistor. We found that H-gate transistors with body contact have much lower noise than conventional layout transistors, the difference being particularly large at elevated drain voltages. The effect is also much more pronounced for p-channel transistors. This is illustrated in Fig. 11 which shows noise spectra of both transistor types with



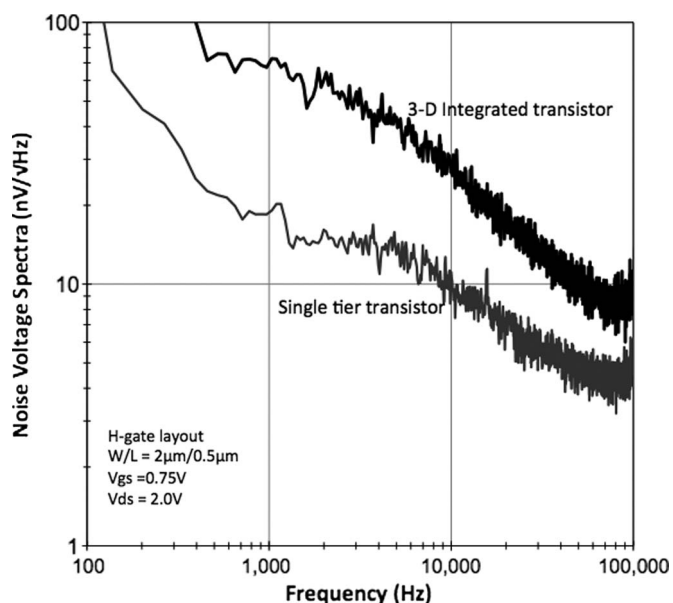


Fig. 12. Comparison of noise spectra of H-gate transistors before and after 3-D integration.

the same channel parameters. The data shown were obtained from discrete transistors that had not yet completed the 3-D integration process. Noise level in the transistors with body contact is comparable to that of the ordinary CMOS transistors, confirming recently reported results [13]. However, many of the transistors that are downstream of the pixel in the analog signal chain were implemented with a conventional (non-body-tied) layout, which is one of the factors that explain the relatively high noise numbers described in Section III-D.

Another factor contributing to the elevated noise level was also uncovered in the process of transistor characterization. Fabrication steps for the image sensor described in this paper include those required for 3-D integration as well as for back-illuminated operation. The back-illumination process used here reduces detector layer to 50- $\mu\text{m}$  thickness, dopes the back surface, and mounts the completed image sensor with an adhesive to a temporary support wafer before packaging. This adhesive prevents the use of high-temperature defect passivation steps, which could be used to reduce damage created during back illumination and packaging preparation. We see in Fig. 12 that even body-tied H-gate devices show increased gate-referred noise after 3-D integration relative to a single tier device. We propose that interface states created at the SOI/buried oxide interface lead to excess pixel noise in this sensor.

The next-generation sensor will include body-tied layouts through the entire analog signal chain, and the fabrication method will be modified to permit additional defect passivation steps before chip packaging.

#### IV. CONCLUSION

We have designed an APS which combines silicon photodiodes on a high-resistivity wafer with an SOI readout circuit using new 3-D integration technology developed at the MIT Lincoln Laboratory. Multiple sampling of a single pixel allowed us to reliably detect 5.9-keV X-rays with an energy resolution

of 181 eV (FWHM). As a result, we were able to very accurately determine sense-node capacitance and its dependence on the diode biasing voltage. This measurement makes it possible to separate photodiode and circuit capacitance. We found that the photodiode capacitance is dominated by the channel stop contribution, which can be substantially reduced by changing the channel stop configuration. Again, using X-rays, we were able to measure the interpixel crosstalk and found that it is asymmetrical. The larger of the crosstalks constitutes 8.8% (a corresponding interpixel capacitance is 2.1 fF); the other one is a factor of 10 smaller. The asymmetry is caused by the capacitive coupling between the sense node in one pixel and the output of source follower in the adjacent pixel. Pixel layout optimization can significantly reduce this link. The circuit-related input node capacitance is dominated by the metal lines surrounding the tungsten plug connecting the diode tier and the SOI circuit and can also be reduced with a revised pixel layout.

We have analyzed noise components of the readout circuitry and found a relatively high level of noise in the chain of source followers. Noise measurements of individual transistors demonstrated that transistors having H-gate configuration with body contact have low noise level that is similar to that of regular CMOS transistors. Transistors without body contact have a higher level of noise, probably due to avalanche multiplication of carriers in the channel. Three-dimensional integration was found to be another factor that contributed to the elevated level of noise. Replacing transistors without body contact with H-gate ones and modifying annealing regimes should significantly improve the noise properties of the sensor.

Our results have indicated that this is a promising technology that offers serious advantages over both monolithic CMOS and more traditional bump-bonded hybrid devices. It is more suitable for X-ray detection than monolithic CMOS, because it makes it much easier to implement thick fully depleted detector layer. More tight integration than in bump-bonded devices can produce sensors with better responsivity and lower noise. To realize the full potential of the technology, more iterations are necessary to remove the bottlenecks that were found during the course of this study.

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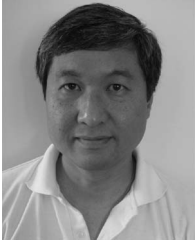
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