A Low-Voltage Zero-Crossing-Based Delta-Sigma Analog-to-Digital Converter

by

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Abstract

A zero-crossing-based (ZCB) switched-capacitor technique is presented for operation under low power supply voltages without gate boosting. Voltage ramp generators maintain common-mode level at each integrator output. Correlated level-shifting is used to increase the effective output impedance of gated current sources. The technique was used to design a single-bit 4th-order delta-sigma analog-to-digital converter for audio applications. The prototype ADC was implemented in 0.13 μm CMOS and achieves 11.9 ENOB for 60 kHz input bandwidth while dissipating 1.2 mW power.

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Electrical Engineering

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Chapter 1

Introduction

1.1 Motivation

Each generation of CMOS scaling imposes increasingly difficult design constraints on the switched-capacitor circuits which are the typical building blocks of analog sampled-data systems.

In general, a switched-capacitor circuit is composed of a network of switches and linear capacitors connected around an operational amplifier (opamp) in negative feedback. The error in these feedback systems is inversely proportional to the gain of the opamp. However, because of the shorter channel lengths and lower power supply voltages of scaled CMOS, it becomes difficult to implement high gain opamps. Consequently, future analog sampled-data circuits will need topologies that do not depend on high gain opamps.

To alleviate the need for opamps in these systems, techniques such as comparator-based switched-capacitor (CBSC) [1] and zero-crossing-based circuits (ZCBC) [2] were proposed. The CBSC technique, demonstrated in the multiply-by-two stage of a pipelined analog-to-digital converter (ADC), replaced opamps with unclocked comparators and gated current sources. In ZCBC, the CBSC comparator was generalized into a zero-crossing detector.

Another challenge of CMOS scaling is the constraint on transistor threshold voltages. It is desirable to scale threshold voltages with power supply voltage in order for

the same circuit topologies to work across technology generations. However, threshold voltage scaling is limited by the increased subthreshold leakage and the decreased noise margins. Thus, threshold voltage scaling has not kept pace with the scaling of power supply voltages [3][4], leading to a decrease in available gate overdrive voltage ($V_{gs} - V_t$). The switched-opamp technique [5], opamp-reset switching [6], and switched-RC [7] addressed low power supply voltage issues in opamp-based switched-capacitor circuits.

Because the gated current sources at the output of a ZCB circuit are already off once the charge-transfer is completed, the ZCB technique can be combined with inspiration from switched-opamp circuits to create a new low-voltage ZCB (LV-ZCB) design. This new technique uses no clock boosting or gate bootstrapping and can be implemented in a standard CMOS logic process without extra processing steps. The concept is demonstrated with a 4th-order delta-sigma modulator for audio applications.

1.2 Thesis Organization

Chapter 2 provides an overview of the ZCB technique.

Chapter 3 discusses design limitations for sampled-data circuits under low power supply voltages.

Chapter 4 reviews existing switched-capacitor integrators- the conventional opamp-based switched-capacitor integrator, the switched-opamp integrator, and the zero-crossing-based integrator.

In chapter 5, a new low-voltage switched-capacitor technique which combines the switched-opamp and zero-crossing-based techniques is introduced.

Chapter 6 covers the delta-sigma ADC, and how designing a delta-sigma ADC with zero-crossing-based integrators compares with using opamp-based switched-capacitor integrators.

Chapter 7 describes the design and testing of a delta-sigma ADC using LV-ZCB integrators.

Finally, chapter 8 summarizes the contributions of this thesis and suggests areas for future work.

Chapter 2

Zero-Crossing-Based Circuits

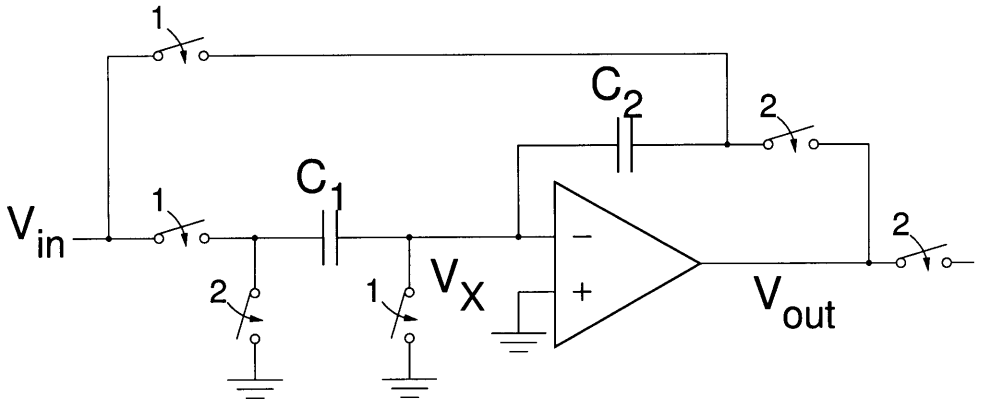
This chapter provides a brief overview of the **zero-crossing-based** (ZCB) switched-capacitor technique, which replaces the opamp of a **conventional switched-capacitor** circuit with a zero-crossing detector and one or more gated current sources. In this overview, a zero-crossing-based switched-capacitor gain stage is compared with the corresponding conventional switched-capacitor gain stage. In Ch. 4, a zero-crossing-based integrator is compared with the corresponding conventional switched-capacitor integrator in more extensive detail.

2.1 ZCB Concept

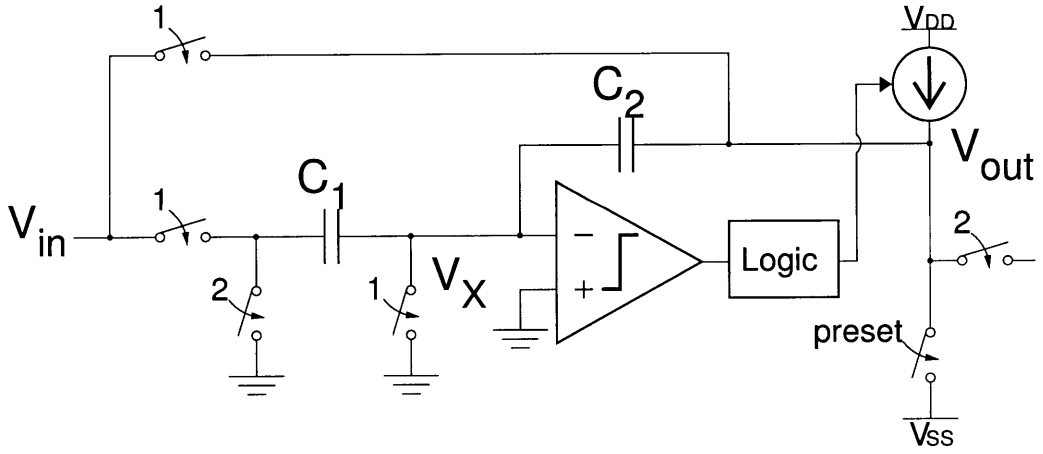
The central idea behind the ZCB technique is that the voltages of a sampled system only need to be correct at the instant the output voltage is sampled. In a switched-capacitor circuit, this means that the voltage of the virtual ground node only has to be at virtual ground at the end of the charge-transfer phase. While a conventional switched-capacitor circuit uses an opamp to drive this virtual ground condition, its ZCB counterpart uses a crossing detector to detect the virtual ground condition.

2.2 ZCB vs. Conventional Switched Capacitor

Fig. 2-1 illustrates two comparable designs for a switched-capacitor gain stage. Fig. 2-1(a) shows the opamp-based conventional switched-capacitor circuit, while Fig. 2-1(b) shows its ZCB counterpart.



(a) Conventional opamp-based gain stage.



(b) Zero-crossing-based gain stage.

Figure 2-1: Switched-capacitor gain stages. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase, ϕ_2 = "2". For the ZCB circuit, "preset" is the first segment of the charge-transfer phase.

Both the conventional switched-capacitor gain stage and the ZCB gain stage operate on two non-overlapping clock phases, ϕ_1 and ϕ_2. The sampling phase, ϕ_1, for

both circuits is the same and is shown in Fig. 2-2.

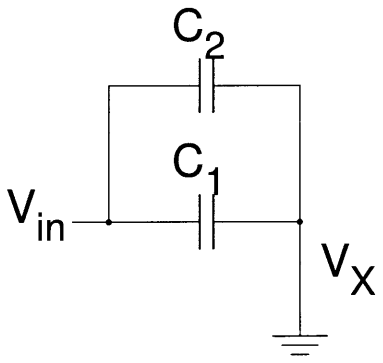


Figure 2-2: Sampling phase for both opamp-based and zero-crossing-based gain stages.

The charge-transfer phase, ϕ_2, for the conventional switched-capacitor gain stage of Fig. 2-1(a) is illustrated in Fig. 2-3. At the beginning of this phase, the voltage at

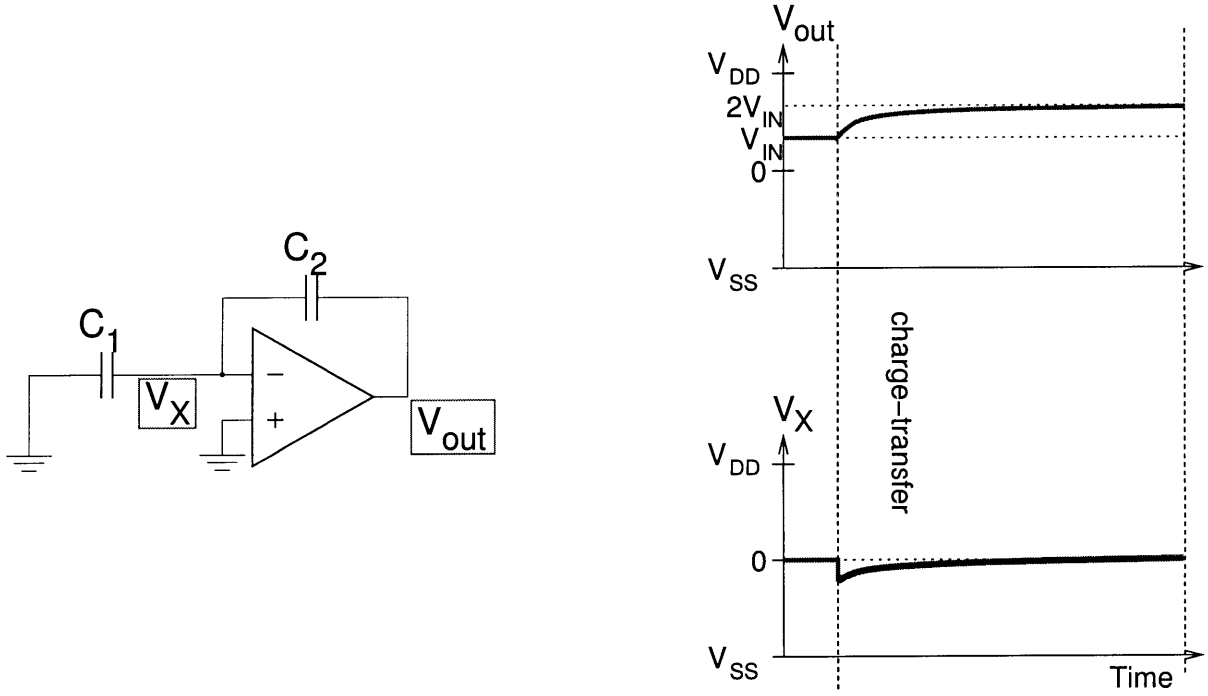


Figure 2-3: Charge-transfer phase for opamp-based gain stage.

the virtual ground node, V_X, is disturbed when capacitor C_1 is switched from V_{in} to a reference voltage. The opamp, which is in negative feedback through capacitor C_2, then drives the output voltage, V_{out}, so that the voltage at V_X settles exponentially back to the virtual ground reference voltage. At the end of the charge transfer phase,

the voltage at V_{out} is sampled.

The charge-transfer phase, ϕ_2, for the ZCB gain stage of Fig. 2-1(b) is different than that for the conventional switched-capacitor stage of Fig. 2-1(a). The charge-transfer phase for the ZCB gain stage is illustrated in Fig. 2-4. At the beginning of

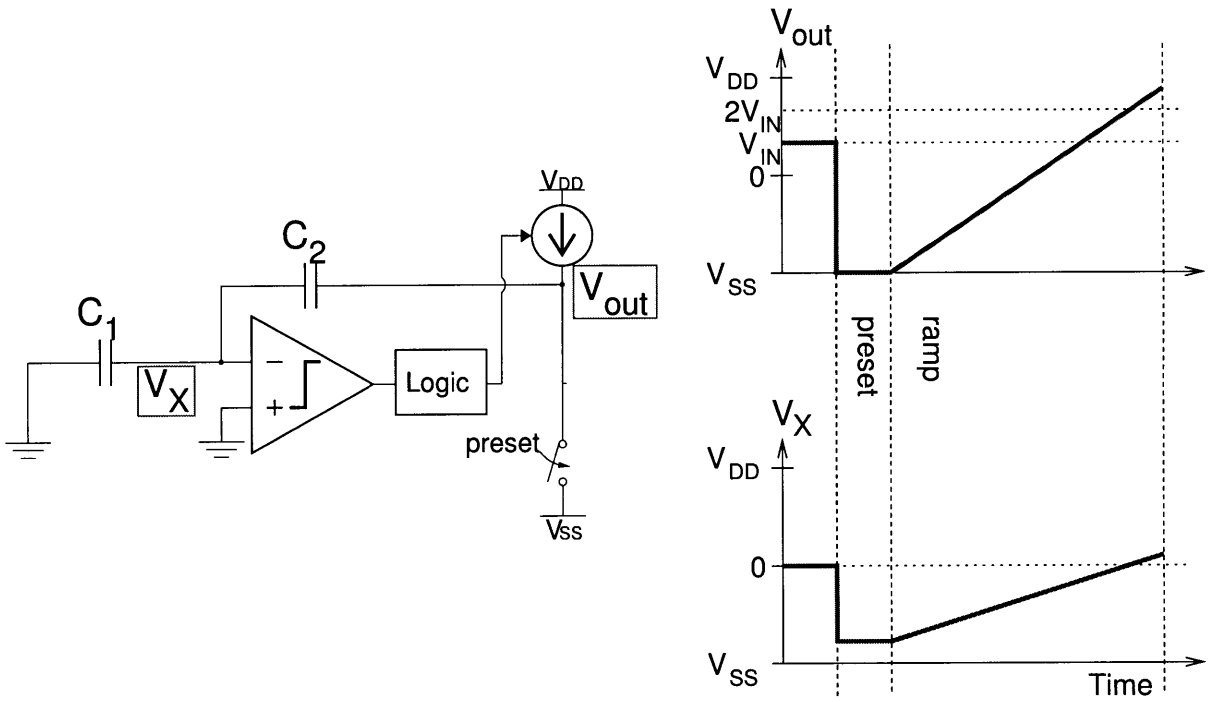


Figure 2-4: Charge-transfer phase for zero-crossing-based gain stage.

the charge-transfer phase, the voltage at the virtual ground node, V_X, is disturbed when capacitor C_1 is switched from V_{in} to a reference voltage. Also, a brief preset operation occurs, where the output node, V_{out}, is shorted to the lowest voltage in the system, V_{SS}, further disturbing the voltage on V_X. After the preset, a gated current source charges V_{out} towards V_{DD} at a constant rate. V_{out} continues to ramp up until the crossing detector detects the virtual ground condition, at which point the voltage at V_{out} is sampled and the gated current source is turned off. Thus, the crossing detector, not a clock edge, defines the sampling instant. Due to the delay of the crossing detector and related logic, the output voltage will slightly overshoot the desired value. Not counting this overshoot error, the output voltage sampled from a ZCB circuit is the same as from its opamp-based counterpart.

2.3 Dual-Ramp ZCB

If the amount of overshoot from a single charge-transfer ramp is too large, the dual-ramp ZCB circuit of Fig. 2-5 can be used in place of the single-ramp ZCB circuit of Fig. 2-1(b).

In the operation of this circuit, the first (coarse) charge-transfer ramp is followed by a second (fine) charge-transfer ramp which corrects for the error of the first ramp. For the second charge-transfer ramp, V_{out} is charged in the opposite[1] direction of the first ramp by a gated current source with a smaller current. V_{out} is then sampled after the second charge-transfer ramp has completed. Because the fine charge-transfer ramp uses a current source with less current, a given crossing detector delay will lead to a smaller overshoot in voltage V_{out}. A graph of the associated signals is shown in Fig. 2-6.

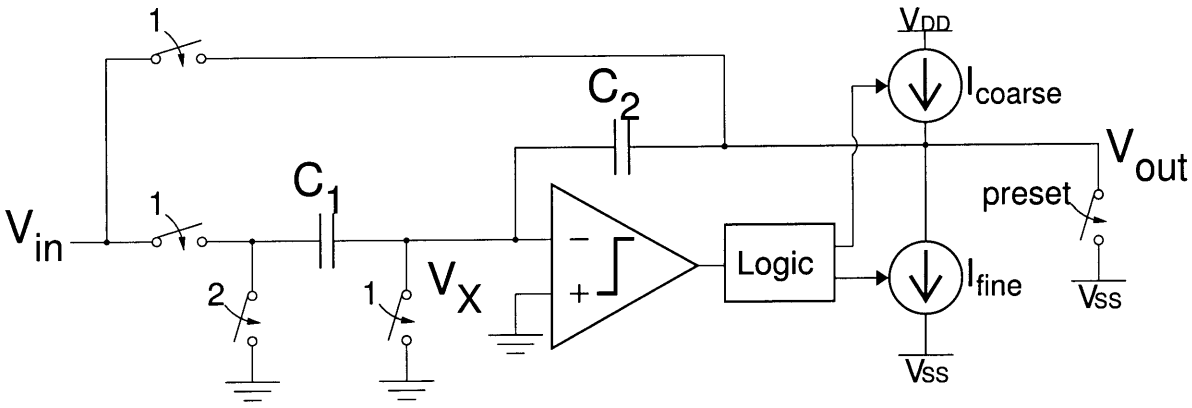


Figure 2-5: Dual-ramp zero-crossing-based gain stage. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase, ϕ_2 = "2". "Preset" is the first segment of the charge-transfer phase.

[1]It is also possible to stop the first charge-transfer ramp before the virtual ground condition is reached so that the second charge-transfer ramp can be in the same direction as the first [8].

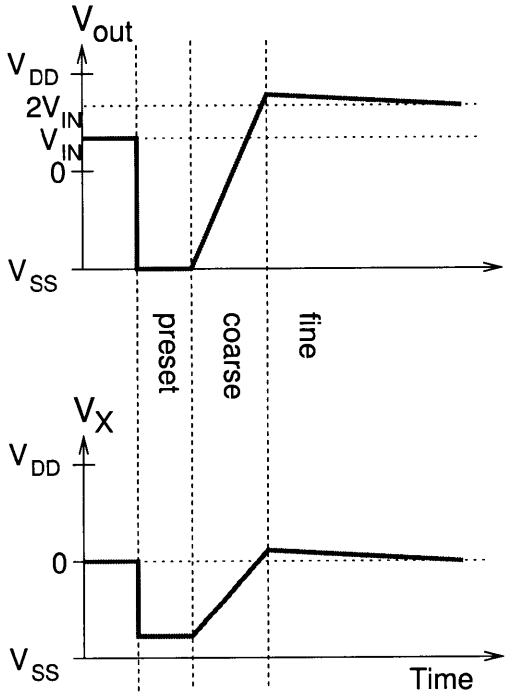


Figure 2-6: Signal graph for dual-ramp ZCB gain stage.

Chapter 3

Low-Voltage Design Issues

This chapter discusses the challenges faced in designing sampled-data circuits under low power supply voltages. For purposes of this project, low-voltage is defined as an environment where

$$V_{DD} - V_{SS} \quad < \quad V_{tn} + |V_{tp}|, \tag{3.1}$$

that is, the power supply voltage range is less than the sum of the NMOS and PMOS threshold voltages.

The ability for a sampled-data circuit to function under low power supply voltages may be a requirement for scaled CMOS designs due to power supply limitations. There are also situations where the ability is desirable as an added feature. If the power consumption of a mixed-signal system with a shared supply voltage is dominated by the digital circuits, the power supply voltage can be lowered to allow the digital circuits to function in a more power-efficient region [9] which will lead to an increase in battery life. Also, when a chip is in danger of overheating, the power supply voltage can be lowered to decrease power dissipation.

3.1 Operational Amplifier

The shorter channel lengths of scaled CMOS make the devices more susceptible to channel length modulation and drain-induced barrier lowering, resulting in decreased

output impedance, r_o, which in turn lowers device gain, $g_m r_o$ [10][11]. Because individual scaled CMOS devices have less voltage gain, to retain total opamp gain, devices must be combined, either through cascoding transistors or cascading amplifier stages.

Cascoding increases the output impedance of a common-source amplifier by isolating the drain from the output node via a common-gate current buffer, minimizing channel length modulation. Because the common-source and common-gate devices are in series, extra bias current is not required. However, this configuration reduces output voltage swing due to the voltage drop needed to keep the cascode devices in saturation.[1]

Cascading amplifier stages increases gain without reducing output voltage swing. As stages are chained, the individual gains multiply and the phase shifts sum. In a negative feedback topology, the extra phase shift makes compensation for stability more difficult.

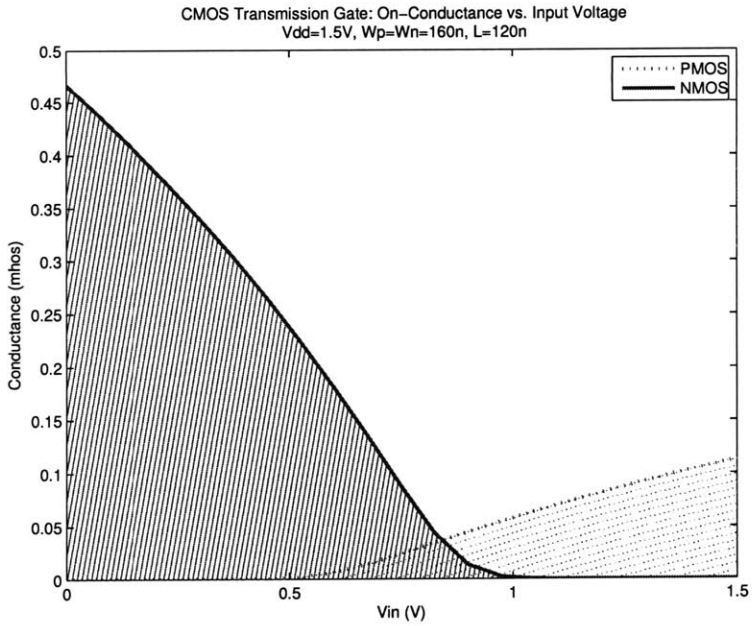
The zero-crossing-based (ZCB) technique [12] (Ch. 2), alleviates the problem of opamp gain by replacing opamps with crossing detectors and gated current sources.

3.2 CMOS Transmission Gate Switch

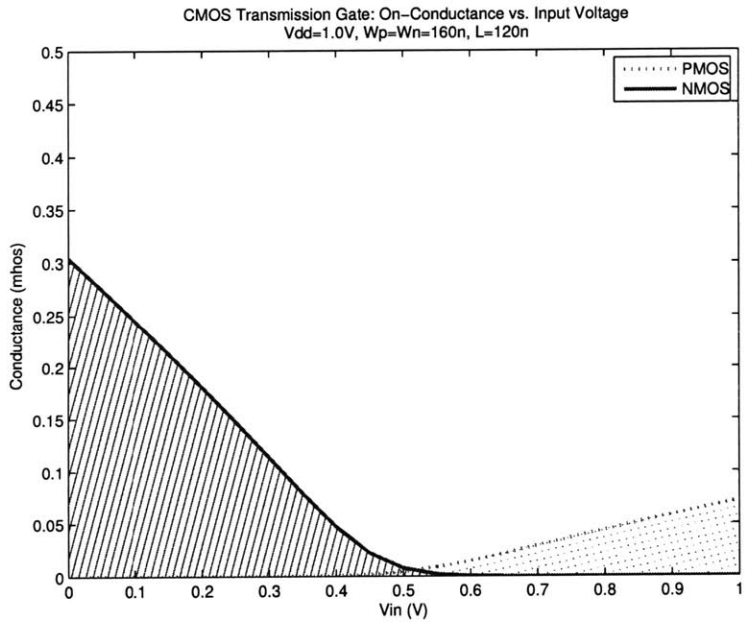
The typical CMOS switch is a transmission gate consisting of an NMOS and a PMOS transistor in parallel. If gate voltages are limited to the power supply range, $[V_{SS}, V_{DD}]$, the switch is in its most conductive state when V_{DD} is applied to the NMOS gate and V_{SS} is applied to the PMOS gate. The NMOS transistor is then conductive for input voltages $V_{in} < V_{DD} - V_{tn}$, and the PMOS transistor is conductive for input voltages $V_{in} > V_{SS} + |V_{tp}|$. This conductance is illustrated in Fig. 3-1(a). Under low power supply voltages (as defined in Eq 3.1), there exists a region of mid-range voltages for which

$$V_{DD} - V_{tn} < V_{in} < V_{SS} + |V_{tp}| \tag{3.2}$$

[1]Since an opamp directly drives the output of a switched-capacitor circuit, decreased swing at the output of the opamp is the same as decreased swing at the output of the switched-capacitor circuit. Depending on the topology, this limited output swing limits the linear input range. To preserve SNR with a smaller input, noise will have to decrease at the cost of increased power.



(a) $V_{DD} = 1.5$ V.



(b) $V_{DD} = 1.0$ V. At $V_{in} = 0.53$ V, neither the NMOS nor PMOS conduct.

Figure 3-1: Conductance vs. input voltage for CMOS transmission gate NMOS (V_{tn} = 0.43 V at $V_{SB} = 0$) and PMOS (V_{tp} = -0.42 V at $V_{BS} = 0$) transistors.

and thus neither the NMOS nor the PMOS transistor has sufficient gate overdrive to conduct (Fig. 3-1(b)); therefore the CMOS switch cannot pass a full-swing voltage signal under low power supply voltages. The gate voltages that would be required to turn the transmission gate completely on for these inputs are outside the range of allowable voltages $[V_{SS}, V_{DD}]$. Fig. 3-2 illustrates the resultant distortion.

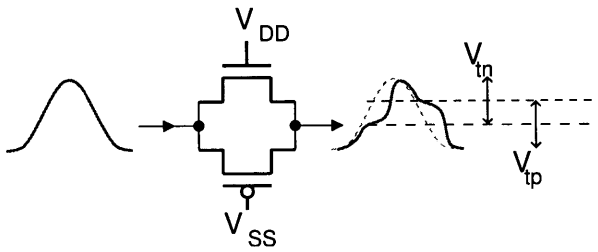


Figure 3-2: CMOS transmission gate in conducting state without gate boosting. Distortion of full-swing input signal under low power supply voltages is shown.

Some strategies to avoid this distortion are to use clock boosting or gate-bootstrapping [13], driving transistor gates with voltages outside of the power supply range. However, these approaches can be complex and may reduce the reliability of the circuit [14].

3.3 Gated Current Source

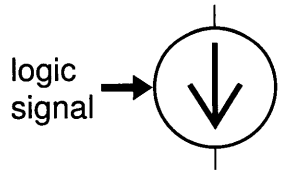


Figure 3-3: Circuit symbol for gated current source.

Fig. 3-3 shows the circuit symbol for a gated current source, which is an integral part of zero-crossing-based circuits (Ch. 2). The current source is either fully on or fully off depending on the value of the logic input. Fig. 3-4 demonstrates some possible implementations of a gated current source. Each of these methods focuses on turning off a current source transistor by using a switch to disconnect the drain/source terminal or to change the gate voltage. The compatibility of each method with low power supply voltages is discussed below.

- A transistor with a switch at the **drain position** (Fig. 3-4(a)) is not compatible with low power supply voltages because the switch must conduct all possible output voltages.

- A transistor with a switch at the **source position** (Fig. 3-4(b)) is compatible with low power supply voltages because the switch only needs to conduct a fixed power supply voltage (V_{DD} or V_{SS}). However, an output-dependent delay occurs when the current source is turned off; after the switch at the source opens, the source terminal must discharge to either the output (drain) voltage, or to within a threshold voltage of the gate before charge stops flowing. Thus, using this current source to charge a capacitor in a CBSC/ZCB stage will lead to nonlinear output-dependent overshoot error.

- When the current source is used to charge a sampling capacitor (Fig. 3-4(c)), a **sampling switch** may be placed between the sampling capacitor and a fixed power supply voltage (V_{DD} or V_{SS}). This configuration is compatible with low power supply voltages and is recommended for its simplicity, for its speed (the sampling capacitor stops charging immediately when the sampling switch is opened), and because the switch causes no output-dependent error in the voltage sampled onto the sampling capacitor.

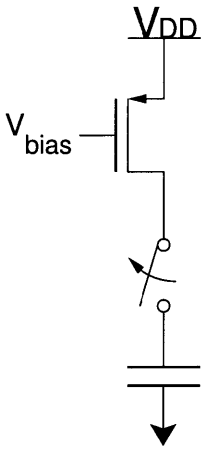
- Using a **cascode transistor** as a switch (Fig. 3-4(d)) is compatible with low power supply voltages. The advantages are the same as for a cascode current source - increased output impedance at the cost of reduced output voltage swing. If the cascode bias voltage cannot be conducted by a switch under low power supply voltages (Sec. 3.2), then the voltage can be connected to the cascode transistor using a series resistor. The trade-off is that there is a delay when turning on the current source while the cascode transistor gate voltage settles to the proper value.

- A **current mirror** may be used to set the gate voltage of the current source transistor (Fig. 3-4(e)). To turn the current source off, a switch discharges

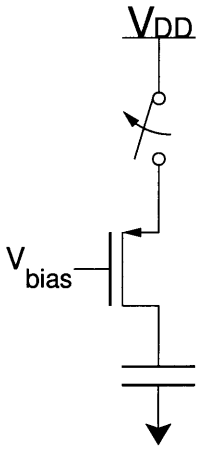
the gate node of the current mirror transistors to V_{DD} or V_{SS}. However, a delay occurs when turning on the current source while the gate voltage settles to the proper value. Also note that one of the other gated current source topologies (i.e. transistor with switch in source position) must be used to bias the current mirror; using a constant (always on) current source for the bias is not recommended because of the trade-off between switch conductance and parasitic capacitance at the gate node, both of which are functions of switch width.

Note that the implementations of a gated current source which are compatible with low power supply voltages (source switch, sampling switch, cascode switch, current mirror switch) also offer advantages under higher power supply voltages; because their switches only conduct constant voltages, they don't suffer from output-dependent charge injection in the way that low-voltage incompatible implementations do.[2]

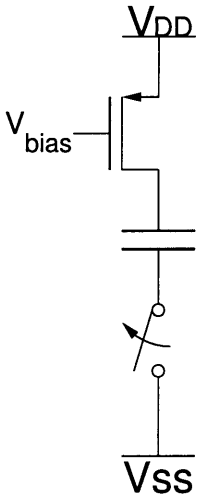
[2]For reference, in the LV-ZCB integrators (Ch. 5) of the implemented delta-sigma ADC, the gated current sources for both the coarse and fine charge-transfers are turned on using a switch in the source position (Fig. 3-4(b)), and turned off with a cascode transistor switch (Fig. 3-4(d)). However, before turning off the gated current source at the end of the fine charge-transfer, a sampling switch (Fig. 3-4(c)) is used to sample the final charge on the integration (C_{FB}) and load capacitors (C_{IN} of the next stage). The cascode bias voltages are controlled using current mirrors switches (Fig. 3-4(e)).



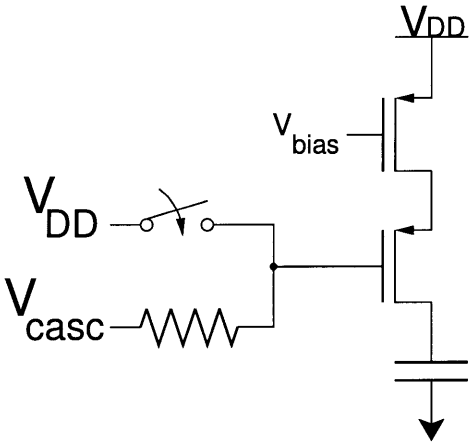
(a) Drain switch. Not compatible with low supply voltages.



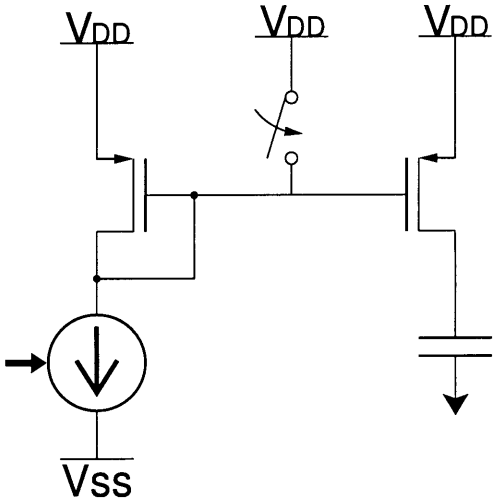
(b) Source switch.



(c) Sampling switch.



(d) Cascode switch.



(e) Current mirror switch. Can be biased using transistor with source switch (b).

Figure 3-4: Methods of implementing a gated current source.

Chapter 4

Overview of Switched-Capacitor Integrators

This chapter describes the evolution of switched-capacitor integrators. The **conventional** opamp-based switched-capacitor integrator is briefly reviewed. Next, the **switched-opamp** integrator and how it works under low power supply voltages is explained. Then, the **zero-crossing-based** (ZCB) integrator and how it eliminates the use of opamps in switched-capacitor circuits is covered.

4.1 Conventional Switched-Capacitor Integrator

The conventional switched-capacitor integrator is shown in Fig. 4-1. The integrator is controlled by two non-overlapping clock phases, ϕ_1 and ϕ_2. During the first clock phase, ϕ_1, the input voltage, V_{in}, is sampled onto capacitor C_{IN}. During the second clock phase, ϕ_2, capacitor C_{IN} is connected between reference voltage, V_{REF}, and the inverting terminal of an opamp. The opamp is in a negative feedback topology, with its output, V_{out}, adjusting the voltage at its inverting input, V_X, through the voltage divider comprised of capacitors C_{FB} and C_{IN}. Through this negative feedback, the opamp forces the voltage at V_X to settle to the virtual ground reference voltage on its noninverting terminal, V_{CM}. The change in charge on capacitor C_{IN} during ϕ_2 is

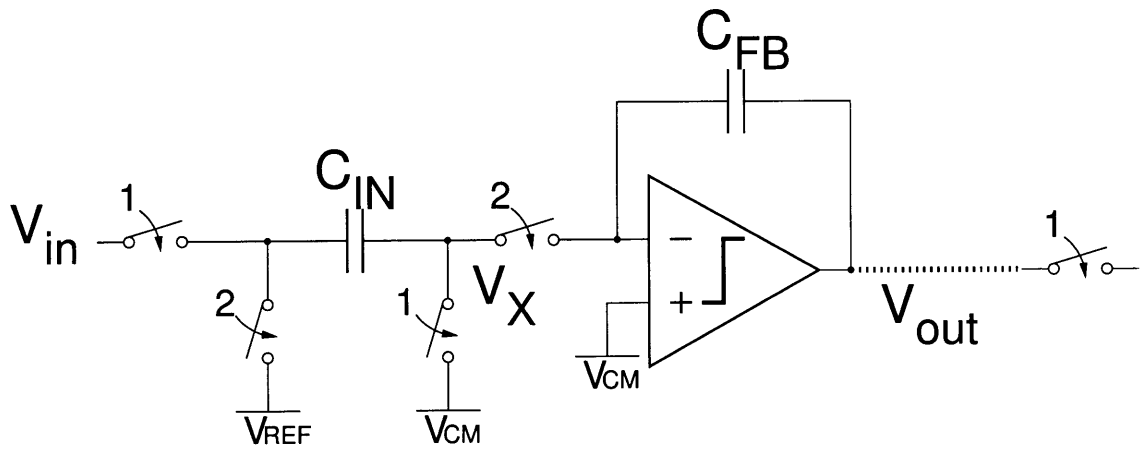


Figure 4-1: Conventional switched-capacitor integrator [15]. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase, ϕ_2 = "2". The series switch at the input of the next stage is shown.

proportional to the change in the voltage across it:

$$\begin{aligned} \Delta Q &= C\Delta V \\ &= C_{IN}[(V_{CM} - V_{REF}) - (V_{CM} - V_{in})] \\ &= C_{IN}(V_{in} - V_{REF}). \end{aligned} \tag{4.1}$$

Because C_{IN} and C_{FB} are connected in series, the current from the opamp transfers identical charge to both capacitors, resulting in a per cycle change in the output voltage of

$$\Delta V_{out} = \frac{\Delta Q}{C_{FB}} = \frac{C_{IN}}{C_{FB}}(V_{in} - V_{REF}). \tag{4.2}$$

Because the change in voltage at the output of the circuit is proportional to the input voltage, this circuit functions as an integrator.

The building blocks of the conventional switched-capacitor integrator are linear capacitors, an opamp, and switches. Linear capacitors can be implemented as vertical parallel plate (a.k.a. back-end-of-line vertical natural) structures in a standard logic process without requiring extra processing steps. However, the opamps and some of the switches can present problems under low power supply voltages.

4.1.1 Series Switch

The series switch at the input of the conventional switched-capacitor integrator, between V_{in} and C_{IN}, must pass all input voltages. The rest of the switches only need to conduct constant voltages. Under low power supply voltages, the values of the constant voltages can be carefully chosen to allow their respective switches to function. In contrast, the series switch cannot pass mid-range voltages, thus restricting the functional input voltage range under low power supply voltages (Sec. 3.2).

4.1.2 Opamp

Virtual Ground

The opamp in the conventional switched-capacitor integrator drives the virtual ground voltage continuously. An advantage of this persistence is the flexibility to generate signals with different timings and polarities simply by changing the clock phases of the switches. Fig. 4-2 illustrates delay-free, half-cycle delay, and full-cycle delay timings for the conventional switched-capacitor integrator. A disadvantage of this persistence is the consumption of static power to continuously drive the virtual ground which is only required to be valid at one sampling instant per cycle.

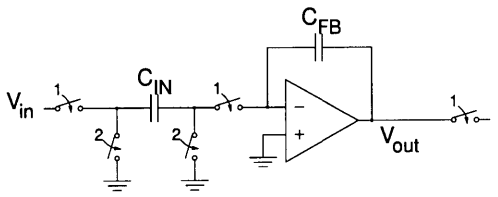
Finite Gain

The analysis leading to Eq. 4.1 assumed that the opamp has infinite gain. If instead the opamp has finite gain, A, then at the end of the charge-transfer phase, ϕ_2, the virtual ground condition is not fulfilled completely:

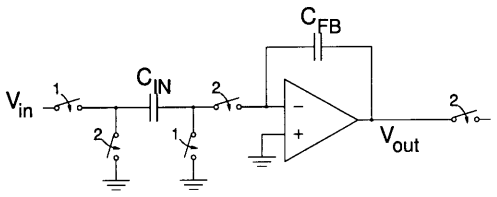
$$\begin{aligned} V_{out} &= A(V_{CM} - V_X) \\ V_X &= V_{CM} - \frac{V_{out}}{A}. \end{aligned} \tag{4.3}$$

We define V_{CFB}, the voltage across the integrating capacitor:

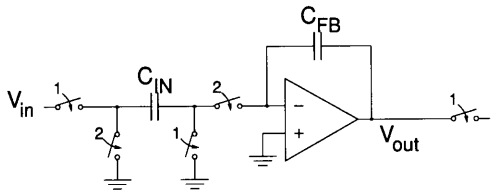
$$V_{CFB} = V_{out} - V_X. \tag{4.4}$$



(a) Delay-free inverting integrator. Input and output sampled at end of ϕ_1.



(b) Noninverting integrator with half-cycle delay. Input sampled at end of ϕ_1, output sampled at end of next ϕ_2.



(c) Noninverting integrator with full-cycle delay. Input sampled at end of ϕ_1, output sampled at end of next ϕ_1.

Figure 4-2: Modifying the switch phases of a switched-capacitor integrator results in different signal timings and polarities.

Substituting Eq. 4.3 into Eq. 4.4, we get

$$\begin{aligned} V_{CFB} &= V_{out} - V_{CM} + \frac{V_{out}}{A} \\ &= V_{out}\left(1 + \frac{1}{A}\right) - V_{CM}, \end{aligned} \tag{4.5}$$

which shows that finite opamp gain causes a gain error between V_{CFB} and V_{out}.

Taking Eq. 4.3 into account, the amount of charge transferred during ϕ_2 (Eq. 4.1) becomes

$$\begin{aligned} \Delta Q &= C_{IN}[(V_X - V_{REF}) - (V_{CM} - V_{in})] \\ &= C_{IN}\left[\left(V_{CM} - \frac{V_{out}}{A} - V_{REF}\right) - (V_{CM} - V_{in}\right)\Big] \\ &= C_{IN}\left(V_{in} - V_{REF} - \frac{V_{out}}{A}\right). \end{aligned} \tag{4.6}$$

This analysis is treated more rigorously in Sec. 6.2.2. However, it can be seen from

Eq. 4.6 that the transferred charge now has an output-dependent error. Also, the integrator no longer has infinite DC gain; for example, if V_{in} is a DC signal, the amount of charge integrated each cycle decreases as the magnitude of V_{out} grows.

4.2 Switched-Opamp Integrator

The switched-opamp technique [5] modifies conventional switched-capacitor circuits to allow them to function under low power supply voltages by avoiding the problem of passing full-swing voltage signals through switches[1]. In switched-opamp topologies, all switches operate around a constant voltage level near V_{DD} or V_{SS}, so that signal distortion does not occur under low power supply voltages (see Sec. 3.2). Similarly, the DC operating point of the virtual ground node is chosen to be close to a power supply rail. To allow full-scale input voltages, the series switch at the input is eliminated. In the case of multiple cascaded integrators, instead of using a switch to disconnect the input of each integrator, the output of the preceding integrator is disabled by switching off the opamp that drives that output. Because no full-swing voltage signals are passed through switches, switched-opamp topologies can theoretically work at power supply voltages as low as $V_{DD,\min} \approx V_t$, where V_t is the larger of V_{tn} or $|V_{tp}|$.

An additional benefit of the switched-opamp topology is that PMOS-only and/or NMOS-only switches can be used instead of a full CMOS transmission gate, resulting in lower parasitic capacitances. Also, because each switch operates around a constant voltage, switch resistance and charge-injection are not signal-dependent.

A limitation of the switched-opamp topology is that it can only be used to create delay-free and half-cycle delay circuits.[2] Consider the case of applying the switched-opamp technique to the conventional switched-capacitor integrators of Fig. 4-2. In the delay-free integrator of Fig. 4-2(a), the opamp can be switched off during ϕ_2 in place of the switch at the output. Similarly, in the half-cycle delay integrator of Fig. 4-2(b), the opamp can be switched off during ϕ_1. However, the opamp of the full-cycle delay

[1]Variations of the switched-opamp technique include switched-RC [7] and unity-gain-reset opamps [6].

[2]However, full-cycle delay circuits can be created by cascading two half-cycle delay stages.

integrator in Fig. 4-2(c) cannot be switched off during the charge-transfer phase, ϕ_2, because then it would not be available to drive the transfer of charge onto C_{FB} and no integration would occur.

4.2.1 First Switched-Opamp Stage

Special attention has to be paid to the input of the first switched-opamp stage, which has no preceding opamp to disable. A few possible designs [5][16][17] to control the first input have been proposed.

In [5], a series resistor, R_{IN}, replaces the series switch at the input. An example of a switched-opamp integrator incorporating a series resistor at the input is shown in Fig. 4-3. The value of R_{IN} is chosen as a compromise between the off-resistance

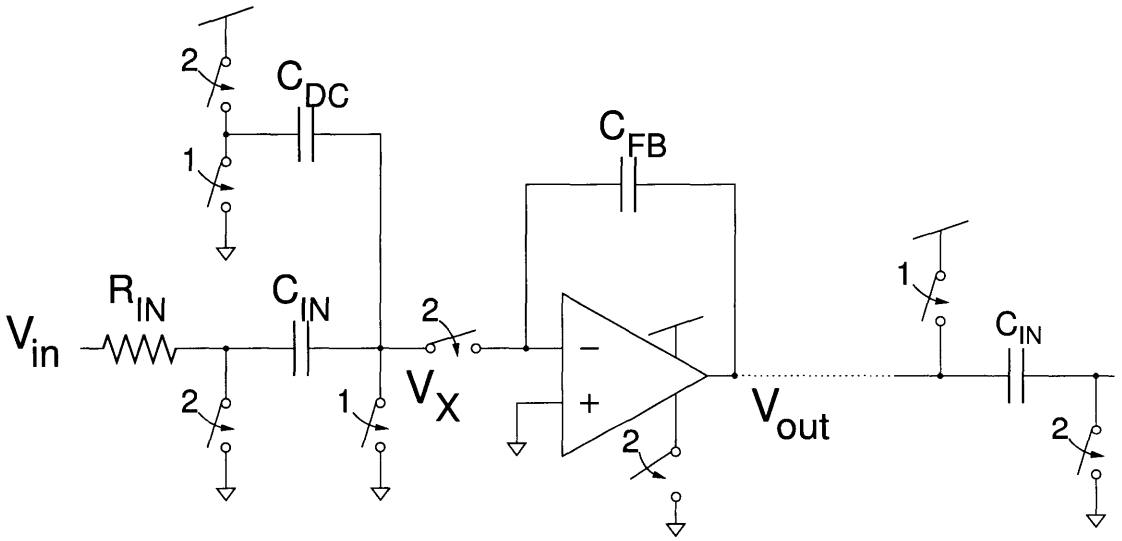


Figure 4-3: Switched-opamp integrator. The sampling capacitor of the next switched-opamp stage is also shown.

and the on-resistance of the replaced series switch. R_{IN} must be large enough to sufficiently attenuate V_{in} during the charge-transfer clock phase, ϕ_2, without drawing too much current from V_{in}. R_{IN} must be small enough that the sampling of the input signal, V_{in}, onto C_{IN} can sufficiently settle during the sampling phase, ϕ_1.

For a capacitor, C, charged with a voltage source in series with a resistance, R, the transfer function from the voltage source to the voltage across the capacitor, $v_C(t)$,

is $H(s) = \frac{\frac{1}{sC}}{\frac{1}{sC}+R}$. If the voltage source is a unit step, u(t), then the voltage across the capacitor is

$$v_C(t) = u(t) * h(t).$$

Taking the Laplace transform,

$$\begin{aligned} V_C(s) &= \left(\frac{1}{s}\right) H(s) \\ &= \left(\frac{1}{s}\right)\left(\frac{\frac{1}{sC}}{\frac{1}{sC}+R}\right) \\ &= \left(\frac{1}{s}\right)\left(\frac{\frac{1}{RC}}{\frac{1}{RC}+s}\right) \\ &= \left(\frac{1}{s}\right)\left(\frac{\frac{1}{RC}+s-s}{\frac{1}{RC}+s}\right) \\ &= \frac{1}{s} - \frac{1}{\frac{1}{RC}+s}. \end{aligned}$$

Taking the inverse Laplace transform,

$$\begin{aligned} v_C(t) &= u(t)\left(1 - e^{\frac{-t}{RC}}\right) \\ &= u(t)\left(1 - e^{\frac{-t}{\tau_o}}\right), \end{aligned} \tag{4.7}$$

where the time constant of this RC system is $\tau_o = RC$.

Using the result of Eq. 4.7, the effect of large R_{IN} on the sampling of V_{in} is as follows: If C_{IN} is discharged to a constant value, V_{CIN0}, during the charge-transfer phase of each cycle, and the input signal is then sampled onto C_{IN} for a period of time, t, then the voltage on C_{IN} is

$$V_{CIN}(t) = V_{CIN0} + (V_{in} - V_{CIN0})\left[1 - e^{\left(\frac{-t}{R_{IN}C_{IN}}\right)}\right].$$

Because V_{in} is sampled onto C_{IN} for a fixed period of time per cycle, $(\frac{1}{2f_s})$, where f_s is the sampling frequency, then incomplete settling due to large R_{IN} only attenuates

the sampled input signal by a factor of

$$1 - e^{\left(\frac{-1}{2f_s R_{IN} C_{IN}}\right)}, \tag{4.8}$$

and add a constant offset of

$$V_{CIN0}\, e^{\left(\frac{-1}{2f_s R_{IN} C_{IN}}\right)}. \tag{4.9}$$

In an actual implementation, nonlinear parasitic capacitance can lead to nonlinear settling (see Sec. 7.8.2).

4.2.2 DC Reference Level at Input

In the topology of Fig. 4-3, a separate capacitor, C_{DC}, of size $C_{IN}/2$ is used to create a DC voltage shift at the input [18][19]. During the sampling phase, ϕ_1, while C_{IN} is connected between V_X and the series resistor at the input, C_{DC} is connected between V_X and V_{SS}. At the start of the charge-transfer phase, ϕ_2, the input side of C_{IN} is switched to V_{SS} while capacitor C_{DC} is switched from V_{SS} to V_{DD}. Just as in the conventional switched-capacitor integrator, the opamp is placed in a negative feedback topology, forcing the voltage at V_X to settle to the virtual ground reference voltage on its noninverting terminal. The change in charge on capacitor C_{FB} matches the change in charge on the combination of capacitors C_{IN} and C_{DC}:

$$\begin{aligned}
\Delta Q &= C_{IN}[(V_{SS} - V_{SS}) - (V_{SS} - V_{in})] + C_{DC}[(V_{SS} - V_{DD}) - (V_{SS} - V_{SS})] \\
&= C_{IN}(V_{in} - V_{SS}) + C_{DC}(V_{SS} - V_{DD}) \\
&= C_{IN}\left[V_{in} - \left(\frac{C_{DC}}{C_{IN}}\right) V_{DD} - \left(1 - \frac{C_{DC}}{C_{IN}}\right) V_{SS}\right]
\end{aligned} \tag{4.10}$$

Note that the charge-transfer of the switched-opamp integrator in Eq. 4.10 is the same as that for the conventional switched-capacitor integrator of Eq. 4.1 with a reference voltage, $V_{REF} = \left(\frac{C_{DC}}{C_{IN}}\right) V_{DD} + \left(1 - \frac{C_{DC}}{C_{IN}}\right) V_{SS}$. Assuming that the input signal must swing symmetrically around V_{REF}, the input signal swing is maximized

for a reference voltage equal to the mid-level voltage, $(V_{DD} + V_{SS})/2$, which occurs for $C_{DC} = C_{IN}/2$. For this value of C_{DC}, Eq. 4.1 becomes

$$\Delta Q = C_{IN}\left(V_{in} - \frac{V_{DD} + V_{SS}}{2}\right), \tag{4.11}$$

and therefore Eq. 4.2 becomes

$$\Delta V_{out} = \frac{\Delta Q}{C_{FB}} = \frac{C_{IN}}{C_{FB}}\left(V_{in} - \frac{V_{DD} + V_{SS}}{2}\right). \tag{4.12}$$

Thus, the use of capacitor C_{DC} maximizes the input signal swing by setting the input reference level to the mid-level voltage, without requiring a switch to conduct the mid-level voltage directly, which would not be possible under low power supply voltages[3].

A disadvantage of using capacitor C_{DC} is the increased noise gain from the opamp due to the increase in total capacitance at node V_X. With capacitor C_{DC}, the noise gain is

$$\begin{aligned} \frac{V_{out}}{V_X} &= \frac{\text{total capacitance at node } V_X}{C_{FB}} \\ &= \frac{C_{FB} + C_{IN} + C_{DC}}{C_{FB}} \end{aligned} \tag{4.13}$$

A higher noise gain means that the input-referred noise of the opamp has a larger effect on the output voltage, V_{out}. Note that due to noise-shaping, the more important effect of opamp noise is on the charge integrated on capacitor C_{FB}. This is explained in detail for ZCB integrators in Sec. 7.3.4, although the same argument also applies to opamp-based circuits.

Another disadvantage of using capacitor C_{DC} is that it adds to sampled thermal noise; if the thermal noise contributed by C_{IN} is $\overline{q^2_{C_{IN}}} = kTC_{IN}$ and the noise contributed by C_{DC} is $\overline{q^2_{C_{DC}}} = kTC_{DC} = kTC_{IN}/2$, then the total input-referred

[3]Except in the unusual case of $V_{tn} >> |V_{tp}|$ or $|V_{tp}| >> V_{tn}$.

mean-square thermal noise voltage due to C_{IN} and C_{DC} is

$$\begin{aligned}\overline{v_{in}^2} &= \frac{\overline{q_{C_{IN}}^2} + \overline{q_{C_{DC}}^2}}{C_{IN}^2} \\ &= \frac{kTC_{IN} + kTC_{IN}/2}{C_{IN}^2} \\ &= \frac{3}{2}\frac{kT}{C_{IN}}\end{aligned} \tag{4.14}$$

It should be noted that, just like their conventional switched-capacitor counterparts, switched-opamp topologies require high gain opamps, with the additional requirement that these opamps need to have outputs that can be disabled. Thus, although the switched-opamp technique alleviates the problem of series switches under low power supply voltages, it actually makes the challenge of designing a high gain opamp more difficult.

4.3 Zero-Crossing-Based Integrator

The following section describes the operation of an integrator created using the ZCB technique (see Ch. 2) as applied to the conventional switched-capacitor integrator of Fig. 4-1.

4.3.1 Operation

Just like the conventional switched-capacitor integrator, the ZCB integrator (Fig. 4-4) requires two non-overlapping clock phases, ϕ_1 and ϕ_2. During the first clock phase, ϕ_1, the input voltage is sampled onto capacitor C_{IN} (Fig. 4-5). At the start of the second clock phase, ϕ_2, the operation of the ZCB integrator deviates from the conventional by requiring a brief preset (Fig. 4-6) in which the output node is set to the maximum possible output value. Then a gated current source discharges the output voltage towards the other extreme (Fig. 4-7), causing the virtual ground node, V_X, to ramp towards virtual ground. When V_X reaches the virtual ground voltage, the crossing detector shuts off the gated current source, holding the output voltage

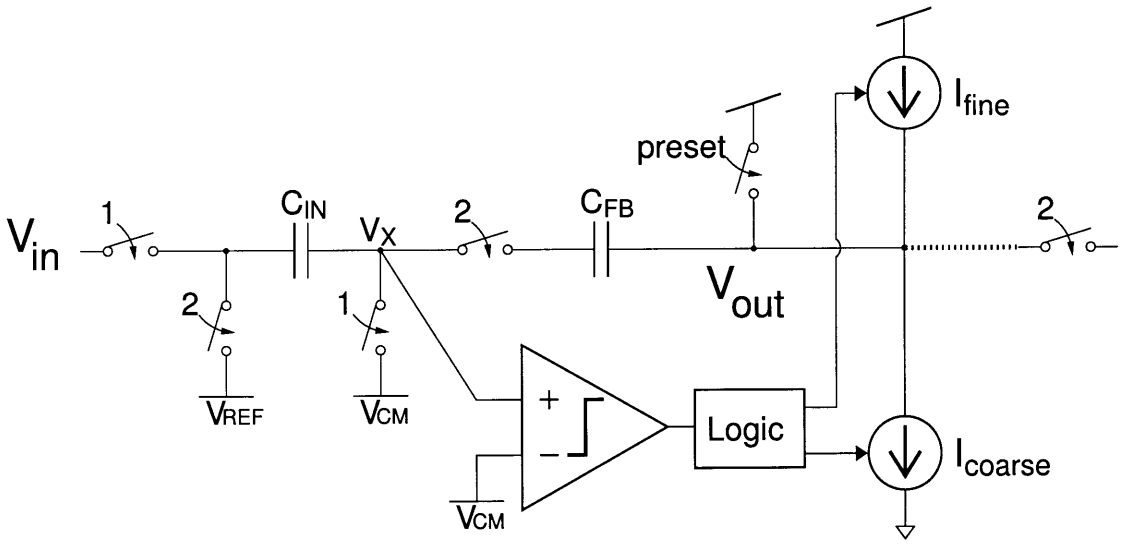


Figure 4-4: Zero-crossing-based switched-capacitor integrator. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase (preset + coarse + fine), ϕ_2 = "2". "Preset" is the first segment of the charge-transfer phase.

constant. Alternatively, the sampling switches for C_{FB} of the integrator and C_{IN} of the next integrator are turned off to sample the voltage at the zero-crossing instant.

Due to the finite bandwidth of the crossing detector and the propagation delay of the related logic, the voltage V_X may overshoot virtual ground. If necessary, a second (fine) gated current source can be used to reverse the effects of overshoot from the first (coarse) ramp (Fig. 4-8). Then, when the virtual ground condition is sufficiently satisfied, the output voltage is sampled by the next stage. Note that, unlike a conventional switched-capacitor circuit, this sampling of the output voltage does not occur on a clock transition but rather is asynchronous.

At the instant of output voltage sampling, the voltages of the nodes of a ZCB integrator correspond identically to those of the conventional SC integrator described in Sec. 4.1. Thus, ignoring overshoot error, the change in output voltage for a ZCB integrator is identical to that given in Eq. 4.2 for an identical signal at the input.

As can be seen in the operation of a ZCB circuit, the negative feedback loop around the virtual ground node uses a one-shot logic signal. In contrast, the opamp of a conventional switched-capacitor circuit uses a continuous-time analog control signal in its negative feedback loop. The advantage of the one-shot logic feedback is that it

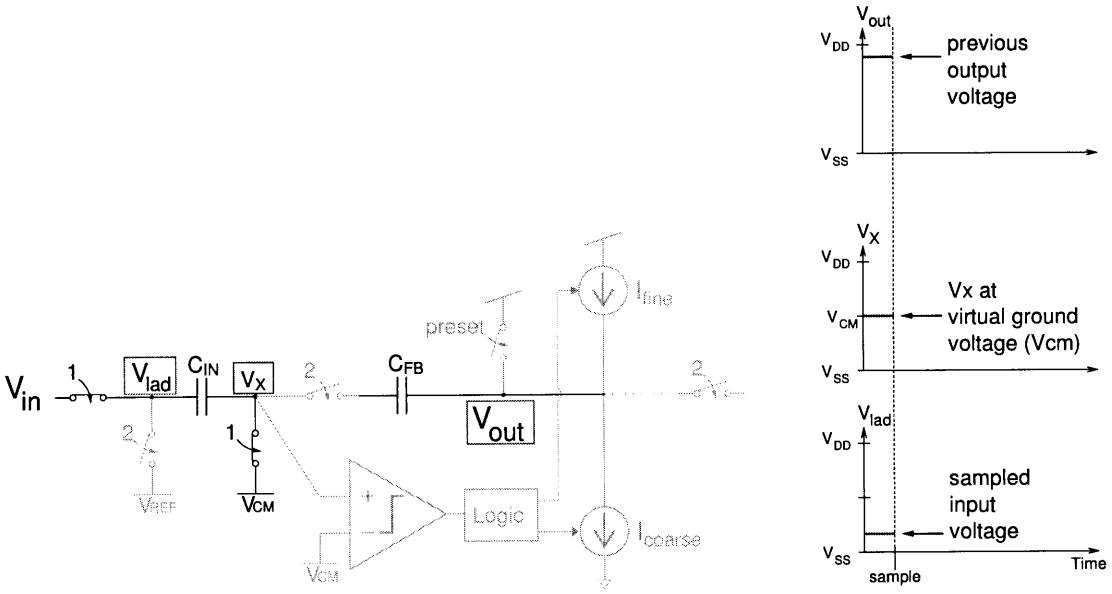


Figure 4-5: ZCB operation: Sample the signal at the input.

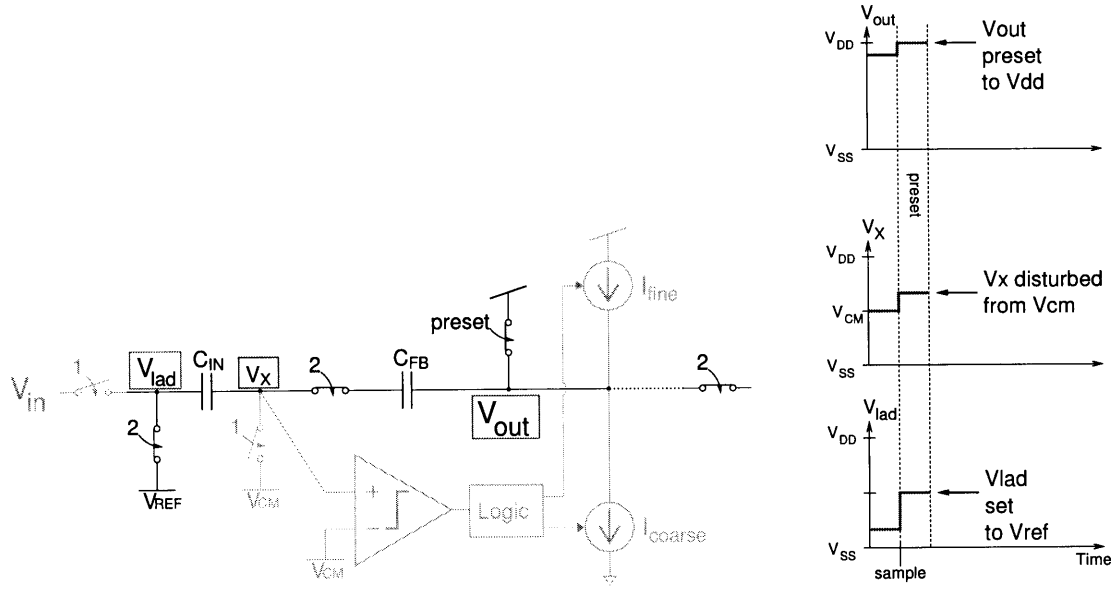


Figure 4-6: ZCB operation: Preset the output voltage to one extreme.

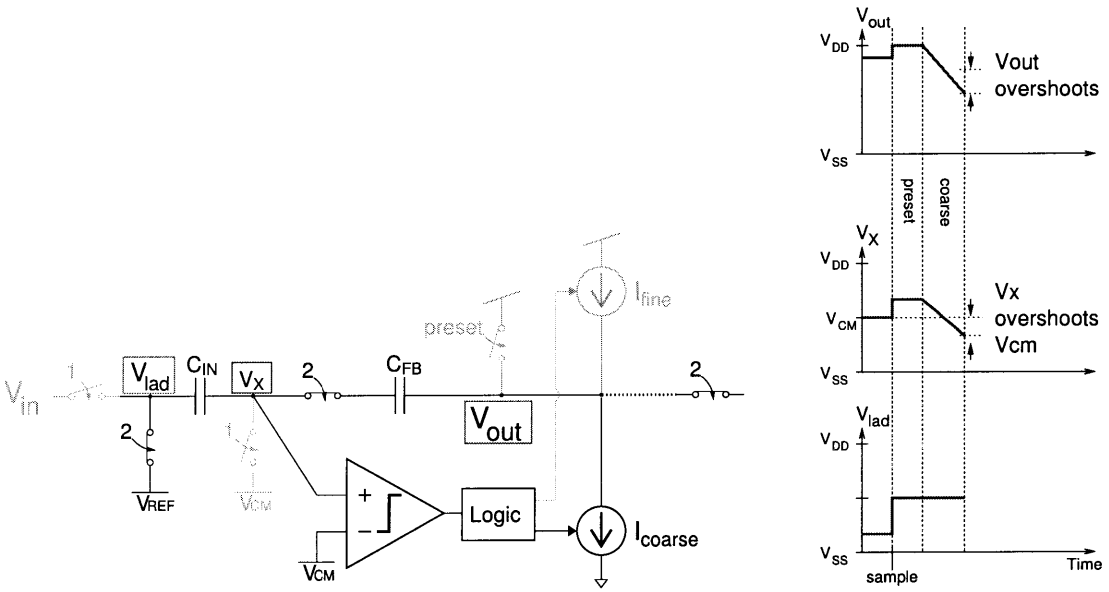


Figure 4-7: ZCB operation: Coarse charge-transfer phase.

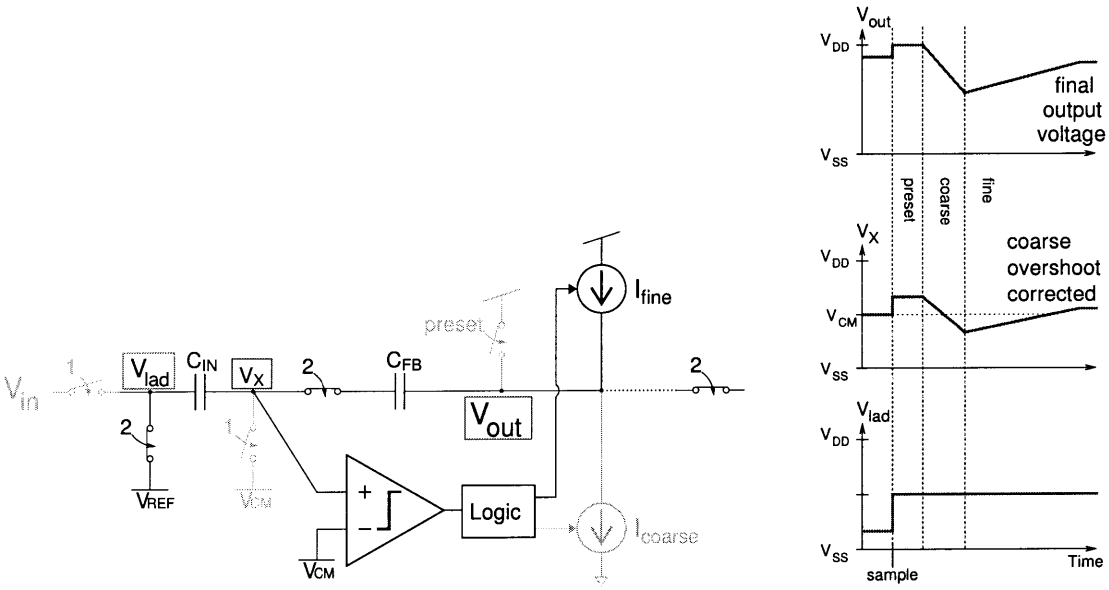


Figure 4-8: ZCB operation: Fine charge-transfer phase.

is inherently stable, therefore not requiring the bandwidth restricting compensation used to stabilize an opamp-based circuit.

A disadvantage of the ZCB technique is that a single-stage ZCB circuit can only accomodate a half-cycle delay.

4.3.2 Maximum Virtual Ground Reference Voltage

One potential complication of the ZCB integrator comes in the choice of virtual ground reference voltage (V_{CM} in Fig. 4-4). From the end of the preset, where $V_{out} = V_{DD}$, to the end of the charge-transfer phase, where $V_X = V_{CM}$, the charge transferred onto C_{IN} and C_{FB} by the gated current source(s) is

$$\begin{aligned} \Delta Q_{CFB} &= \Delta Q_{CIN} \quad \text{(capacitors in series)} \\ C_{FB}[(V_{out,f} - V_{CM}) - (V_{DD} - V_{X,preset})] &= C_{IN}[(V_{CM} - V_{REF}) - (V_{X,preset} - V_{REF})] \\ C_{FB}[(V_{out,f} - V_{CM}) - (V_{DD} - V_{X,preset})] &= C_{IN}[V_{CM} - V_{X,preset}], \end{aligned} \tag{4.15}$$

where $V_{X,preset}$ is the voltage at node V_X during the preset and $V_{out,f}$ is the voltage at node V_{out} at the end of the following charge-transfer phase. Note that any parasitic capacitance at node V_X will add to C_{IN} in Eq. 4.15. Rearranging terms, we get

$$C_{FB}V_{out,f} + (C_{FB} + C_{IN})V_{X,preset} = (C_{FB} + C_{IN})V_{CM} + C_{FB}V_{DD}. \tag{4.16}$$

Solving Eq. 4.16 for $V_{out,f}$, we get

$$V_{out,f} = \frac{C_{FB} + C_{IN}}{C_{FB}}(V_{CM} - V_{X,preset}) + V_{DD} \tag{4.17}$$

It can be seen from Eq. 4.17 that a maximum value of V_X at the end of the preset corresponds with a minimum value for V_{out} at the end of the following charge-transfer phase. If the allowed maximum value for V_X during the preset is V_{DD}, then the

minimum value of V_{out} can be calculated as

$$\begin{aligned} V_{out,f} &\geq \frac{C_{FB}+C_{IN}}{C_{FB}}(V_{CM}-V_{DD})+V_{DD} \\ V_{out,min} &= V_{CM}-\frac{C_{IN}}{C_{FB}}(V_{DD}-V_{CM}). \end{aligned} \tag{4.18}$$

For example, if $V_{CM}=\frac{V_{DD}+V_{SS}}{2}$, then for $V_{SS}=0$ V, $V_{DD}=1$ V, $C_{IN}=1$ pF, and $C_{FB}=2.7$ pF,

$$\begin{aligned} V_{out,min} &= \left(\frac{V_{DD}+V_{SS}}{2}\right)-\frac{C_{IN}}{C_{FB}}\left(\frac{V_{DD}-V_{SS}}{2}\right) \\ &= \left(\frac{1V+0V}{2}\right)-\frac{1\text{ pF}}{2.7\text{ pF}}\left(\frac{1V-0V}{2}\right) \\ &= 315\text{ mV}. \end{aligned} \tag{4.19}$$

Note that for $C_{FB}>C_{IN}$, which corresponds to an integrator gain less than unity[4] (see Eq. 4.12), Eq. 4.19 demonstrates that $V_{out,min}>V_{SS}$, that is, the integrator cannot have a rail-to-rail output without V_X exceeding V_{DD} during the preset. If rail-to-rail output swing is required, that is, $V_{out,min}=V_{SS}$, then the maximum virtual ground reference voltage which ensures that V_X will not exceed V_{DD} during the preset can be calculated by solving Eq. 4.18 for V_{CM} and substituting $V_{out,f}=V_{SS}$:

$$\begin{aligned} V_{CM}\left(\frac{C_{FB}+C_{IN}}{C_{FB}}\right) &\leq V_{out,f}+\frac{C_{IN}}{C_{FB}}V_{DD} \\ V_{CM} &\leq \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right)V_{out,f}+\left(\frac{C_{IN}}{C_{FB}+C_{IN}}\right)V_{DD} \\ V_{CM,max} &= \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right)V_{SS}+\left(\frac{C_{IN}}{C_{FB}+C_{IN}}\right)V_{DD}. \end{aligned} \tag{4.20}$$

For example, if $V_{SS}=0$ V, $V_{DD}=1$ V, $C_{IN}=1$ pF, and $C_{FB}=2.7$ pF, then Eq. 4.20 gives a maximum virtual ground reference voltage of 270 mV.

[4]The gain of integrators is usually less than 1 in delta-sigma modulators due to the consideration of voltage swing [20].

Chapter 5

Low-Voltage Zero-Crossing-Based Integrator

In this chapter, a new switched-capacitor technique which combines the switched-opamp and zero-crossing-based (ZCB) techniques is introduced.

Because the gated current sources at the output of a ZCB circuit are off outside of the charge-transfer phase, ϕ_2, the ZCB approach (Sec. 4.3) can be combined with the switched-opamp technique (Sec. 4.2) to create a low-voltage ZCB (LV-ZCB) design that does not require turning off active circuits such as opamps. An integrator demonstrating the combined technique is shown in Fig. 5-1.

5.1 Operation

The basic operation of the dual-ramp LV-ZCB integrator is similar to that of a dual-ramp ZCB integrator, having a sampling phase, ϕ_1, and a charge-transfer phase ϕ_2. Just as with the dual-ramp ZCB integrator, the charge-transfer phase begins with a preset segment, continues with a coarse charge-transfer, and ends with a fine charge-transfer.

Similar to the switched-opamp technique, the virtual ground reference voltage

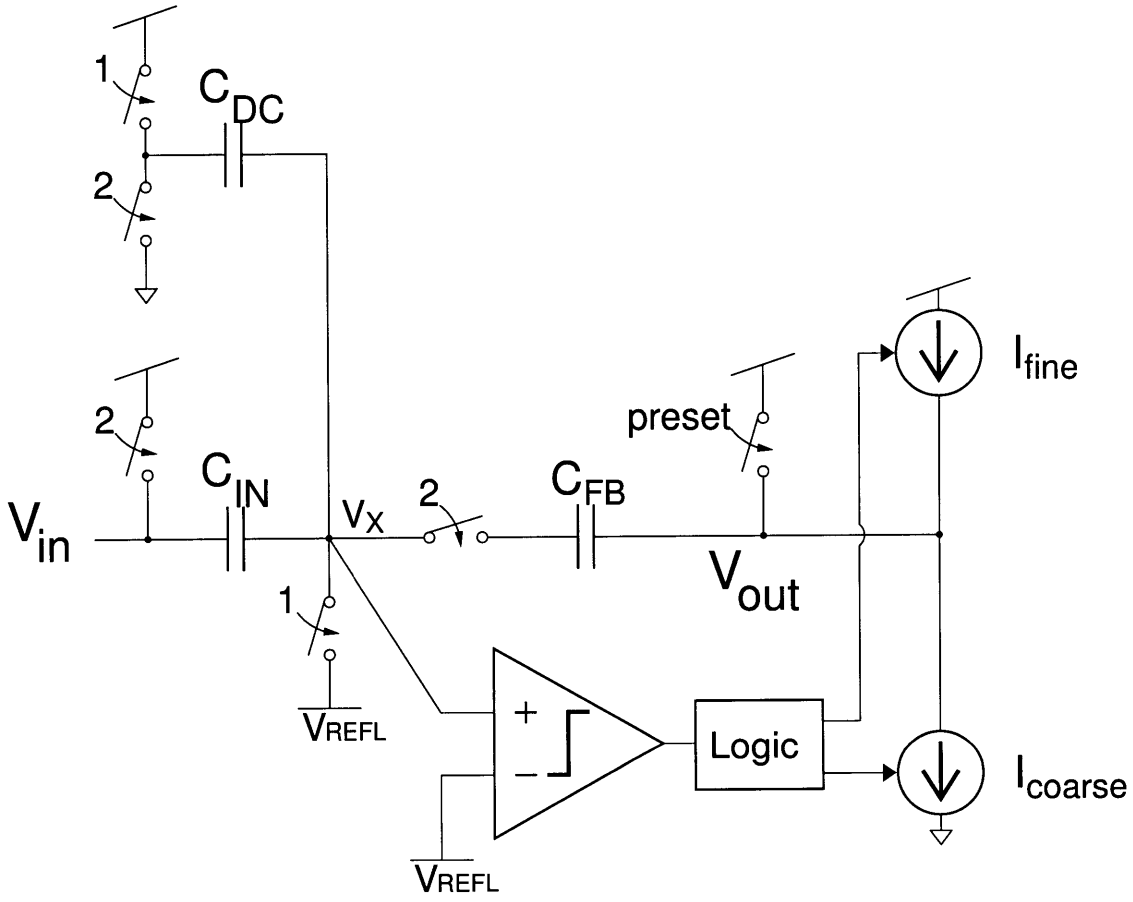


Figure 5-1: Single-ended low-voltage zero-crossing-based integrator. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase (preset + coarse + fine), ϕ_2 = "2".

V_{REFL}[1] is chosen to be close to but not equal to V_{SS}. Thus, both switches at node V_X are NMOS-only. Without some margin between the reference voltage and the power supply voltage, the voltage at node V_X might exceed (overshoot) V_{SS} during the coarse charge-transfer due to crossing detector delay. If V_X falls excessively below V_{SS}, the normally reverse-biased pn junction of the NMOS switch transistors connected to node V_X would become forward-biased, leading to inaccuracy through loss of charge. For this same reason, the preset switch pulls node V_{out} towards V_{DD} (and not V_{SS}) so that the effect of the preset voltage step on V_X is to move it away from V_{SS}.[2]

As with the switched-opamp integrator, a capacitor, C_{DC}, is used to adjust the reference level of the input to the LV-ZCB integrator. A slight modification has been made to the switching of C_{DC} and C_{IN} such that C_{IN} is switched to V_{DD} and capacitor C_{DC} is switched from V_{DD} to V_{SS} at the start of the charge-transfer phase. This swap allows the same transistor to be used as a preset switch at the output of one stage and the reference switch at the input of the subsequent stage. This change also ensures that C_{IN} always pulls V_X away from V_{SS} at the start of the charge-transfer phase, which is important because C_{IN} is larger than C_{DC} and therefore capable of putting a larger voltage step on node V_X in the case of large input voltages.[3]

The charge-transfer for one cycle of the single-ended LV-ZCB can be calculated analogously to that of the switched-opamp integrator:

$$\begin{aligned}
\Delta Q &= C_{IN}[(V_{\text{REFL}} - V_{DD}) - (V_{\text{REFL}} - V_{in})] + C_{DC}[(V_{\text{REFL}} - V_{SS}) - (V_{\text{REFL}} - V_{DD})] \\
&= C_{IN}(V_{in} - V_{DD}) + C_{DC}(V_{DD} - V_{SS}) \\
&= C_{IN}\left[V_{in} - \left(1 - \frac{C_{DC}}{C_{IN}}\right)V_{DD} - \left(\frac{C_{DC}}{C_{IN}}\right)V_{SS}\right]. \qquad (5.1)
\end{aligned}$$

[1]Note the distinction between V_{REFL}, which is a reference for virtual ground node, V_X, and V_{REF} of Fig. 4-1, which is a reference for the input node, V_{in}.

[2]A similar limitation exists in the switched-opamp integrator, as explained in [19].

[3]Although ideally C_{IN} and C_{DC} will switch simultaneously to their respective power supply voltages, this switch configuration makes the switch timing less critical in ensuring that V_X doesn't exceed V_{SS}.

Similarly, the change in output voltage is

$$\Delta V_{out} = \frac{\Delta Q}{C_{FB}} = \frac{C_{IN}}{C_{FB}} \left[V_{in} - \left(1 - \frac{C_{DC}}{C_{IN}}\right) V_{DD} - \left(\frac{C_{DC}}{C_{IN}}\right) V_{SS} \right], \tag{5.2}$$

which for $C_{DC} = C_{IN}/2$ gives us the same relationships specified in Eq. 4.11 and Eq. 4.12 for the switched-opamp integrator.

5.1.1 Maximum Virtual Ground Reference Voltage

In contrast to the ZCB integrator of Sec. 4.3, it is not possible to pull node V_X above V_{DD} during the preset. If V_{out} is pulled to V_{DD}, the maximum voltage that V_X can reach is $V_{DD} - V_{tn}$. Above this voltage, the NMOS series switch between V_X and C_{FB} will not conduct and capacitor C_{FB} is left floating.

A concern is that, during the preset, the voltage on the C_{FB} side of the series switch may exceed V_{DD}. The voltage on this node is $V_{out} - V_{CFB}$. To prevent this voltage from exceeding V_{DD} when $V_{out} = V_{DD}$ at the end of the preset, the following equivalent conditions must be met:

$$\begin{aligned} V_{out} - V_{CFB,preset} &\leq V_{DD} \\ V_{DD} - V_{CFB,preset} &\leq V_{DD} \\ V_{CFB,preset} &\geq 0 \\ \frac{Q_{CFB,preset}}{C_{FB}} &\geq 0 \\ Q_{CFB,preset} &\geq 0, \end{aligned} \tag{5.3}$$

where $V_{CFB,preset}$ and $Q_{CFB,preset}$ are the voltage and charge, respectively, on C_{FB} at the end of the preset.

From Eq. 4.15, the amount of charge transferred by the gated current source(s) from the end of the preset to the end of the charge-transfer phase for the LV-ZCB

integrator is

$$\begin{aligned} \Delta Q_{CFB} &= \Delta Q_{CIN} \quad \text{(capacitors in series)} \\ C_{FB}[(V_{out,f} - V_{REFL}) - V_{CFB,preset}] &= C_{IN}[V_{REFL} - V_{X,preset})]. \end{aligned} \tag{5.4}$$

Note that any parasitic capacitance at node V_X will add to C_{IN} in Eq. 5.4. We solve Eq. 5.4 for $V_{CFB,preset}$ and substitute the result into the conditions of Eq. 5.3:

$$\begin{aligned} V_{CFB,preset} &= V_{out,f} - V_{REFL} + \frac{C_{IN}}{C_{FB}}(V_{X,preset} - V_{REFL}) \\ &\geq 0. \end{aligned} \tag{5.5}$$

As stated above, the maximum value for $V_{X,preset} = V_{DD} - V_{tn}$. Thus, Eq. 5.5 becomes

$$V_{out,f} - V_{REFL} + \frac{C_{IN}}{C_{FB}}[(V_{DD} - V_{tn}) - V_{REFL}] \geq 0. \tag{5.6}$$

Solving Eq. 5.6 for V_{REFL} gives

$$\begin{aligned} V_{out,f} + \frac{C_{IN}}{C_{FB}}(V_{DD} - V_{tn}) &\geq \left(\frac{C_{FB} + C_{IN}}{C_{FB}}\right) V_{REFL} \\ V_{REFL} &\leq \frac{V_{out,f} + \frac{C_{IN}}{C_{FB}}(V_{DD} - V_{tn})}{\frac{C_{FB}+C_{IN}}{C_{FB}}} \\ &= \left(\frac{C_{FB}}{C_{FB} + C_{IN}}\right) V_{out,f} + \left(\frac{C_{IN}}{C_{FB} + C_{IN}}\right)(V_{DD} - V_{tn}). \end{aligned} \tag{5.7}$$

Just as with the ZCB integrator, the worst-case scenario for satisfying Eq. 5.7 during preset occurs for the minimum voltage on node V_{out} during the following charge-transfer phase. Thus, Eq. 5.7 becomes

$$V_{REFL} \leq \left(\frac{C_{FB}}{C_{FB} + C_{IN}}\right) V_{out,min} + \left(\frac{C_{IN}}{C_{FB} + C_{IN}}\right)(V_{DD} - V_{tn}). \tag{5.8}$$

For $V_{out,min} = V_{SS}$,

$$V_{REFL} \leq \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right) V_{SS} + \frac{C_{IN}}{C_{FB}+C_{IN}}(V_{DD} - V_{tn}). \tag{5.9}$$

For example, if $V_{SS} = 0$ V, $V_{DD} = 1$ V, $C_{IN} = 1$ pF, $C_{FB} = 2.7$ pF, and $V_{tn} = 350$ mV, then Eq. 5.9 gives $V_{REFL} \leq 176$ mV. Eq. 5.9 represents the condition on V_{REFL} for the LV-ZCB integrator to have a rail-to-rail output swing without having any nodes exceed V_{DD} during the preset[4]. Because $V_{SS} < V_{DD} - V_{tn}$, the condition of Eq. 5.9 is more strict than the simple condition that $V_{REFL} \leq V_{DD} - V_{tn}$, which is required for the series switch between V_X and C_{FB} to conduct the virtual ground reference voltage, V_{REFL}.

5.2 First LV-ZCB Stage

In the same manner as the switched-opamp integrator (Sec. 4.2), a resistor is used in place of a series switch at the input of a LV-ZCB integrator.

Fig. 5-2 demonstrates a two-stage version of the switched-opamp input of Fig. 4-3 which would be suitable for a switched-opamp or a LV-ZCB integrator. In this implementation, the attenuation of V_{in} during the charge-transfer phase, ϕ_2, is spread across two voltage divider stages. Cascading multiple voltage divider stages allows for lower total switch size and lower total R_{IN} because the attenuation compounds geometrically (multiply) while the sizes compound arithmetically (add)[5].

Note that the resistance of the first resistor, R_{IN1}, determines the amount of current which is pulled from V_{in} during ϕ_2. The larger the resistance, the less current draw.

In sizing the resistors and switches of the multistage attenuator, it is important to

[4]Note that Eq. 5.9 for the LV-ZCB integrator can be obtained by taking Eq. 4.20 for the ZCB integrator and replacing V_{DD} with $(V_{DD} - V_{tn})$.

[5]A limitation of increasing the number of attenuation stages comes from the parasitic capacitance of the resistors and switches. As the number of stages increases, parasitic capacitance begins to dominate and the settling of the attenuator becomes too slow.

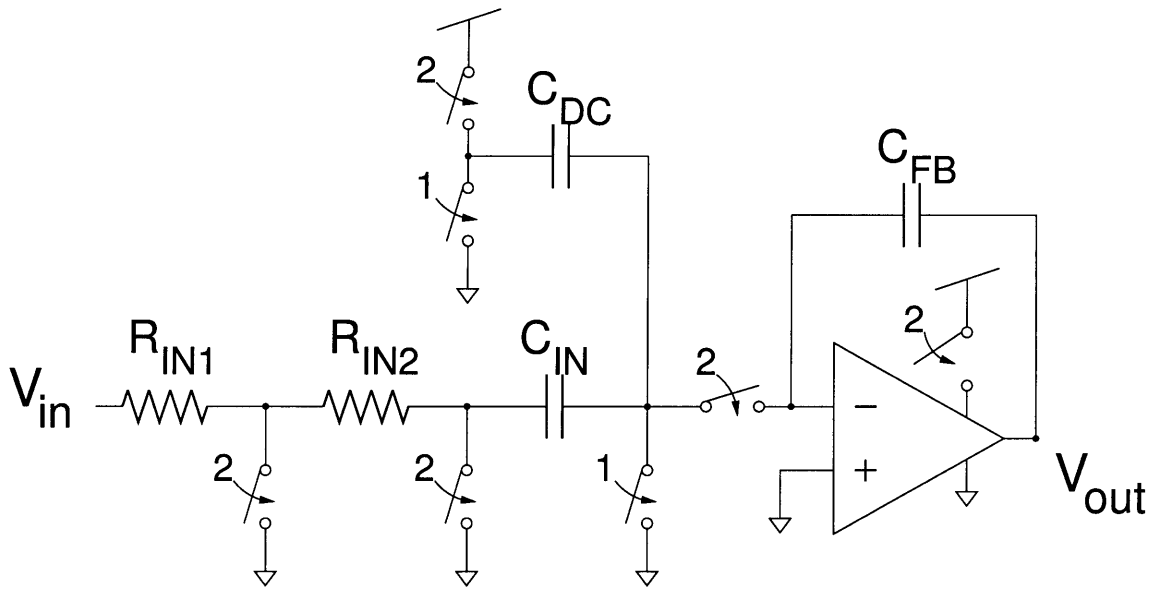


Figure 5-2: 2-stage switched-opamp input

remember that triode switch resistance increases with the voltage across the switch:

$$I_{DS,triode} = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right], \qquad V_{DS} \leq (V_{GS} - V_t), \quad V_{GS} > V_t$$

$$r_{ds} = \frac{dV_{DS}}{dI_{DS}} = \frac{1}{dI_{DS}/dV_{DS}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t - V_{DS})},$$

where V_{DS} is the voltage across the switch, r_{ds} is the resistance of the switch, and V_{GS} is the gate-source voltage (in this case equal to $V_{DD} - V_{SS}$) of the switch transistor. Note that the switches closer to the input will have larger voltages across them and thus will be the most susceptible to this input-dependent variation in resistance. Also, a higher attenuation in the early stages of a multistage attenuator reduces voltage across all later stages of the attenuator. Thus, to reduce dependence of the attenuation ratio on V_{in}, it is advantageous to have more attenuation in the first voltage divider stage than in the later stages. This optimization coincides with increasing the value of R_{IN1}, which reduces current draw from V_{in} as mentioned above. Note that, in an actual implementation, nonlinear capacitance can lead to distortion due to nonlinear

settling (see Sec. 7.8.2), which is exacerbated by larger $R_{IN} = R_{IN1} + R_{IN2}$.

5.2.1 1-bit DAC

If the LV-ZCB integrator is to be used in a delta-sigma modulator (see Ch. 6), the circuit of Fig. 5-2 can be modified for use as a 1-bit feedback DAC. As shown in Fig. 5-3, instead of shunting the voltage signal V_{in} to V_{SS} during every charge-transfer phase, ϕ_2, the input signal is shunted to V_{SS} or V_{DD} depending on the DAC logic level [21]. Also, there is no need for $C_{DC} = C_{IN}/2$. With these modifications, Eq. 5.1 becomes

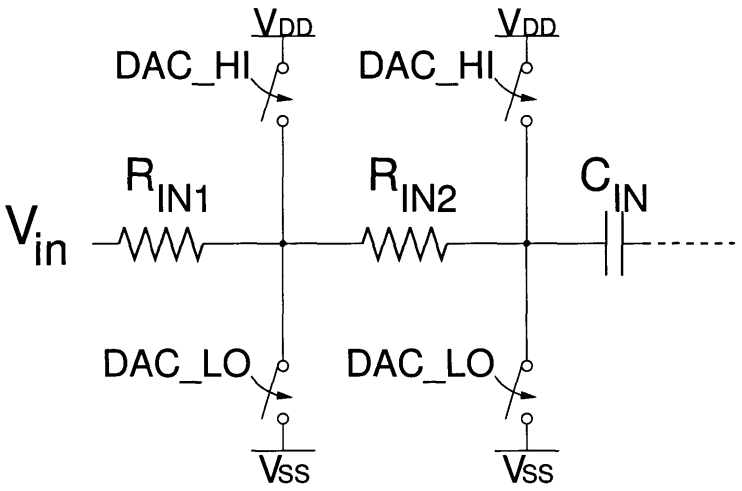


Figure 5-3: 2-stage switched-opamp input, as implemented in 1st stage LV-ZCB integrator.

$$\begin{aligned} \Delta Q &= C_{IN}\left[V_{in} - \left(1 - \frac{0}{C_{IN}}\right)V_{DAC} - \left(\frac{0}{C_{IN}}\right)V_{SS}\right] \\ &= C_{IN}(V_{in} - V_{DAC}), \end{aligned} \tag{5.10}$$

where V_{DAC} is V_{SS} or V_{DD} depending on the DAC logic level. Eq. 5.2 becomes

$$\Delta V_{out} = \frac{\Delta Q}{C_{FB}} = \frac{C_{IN}}{C_{FB}}(V_{in} - V_{DAC}). \tag{5.11}$$

An advantage of this configuration is that it avoids the extra sampled thermal noise contributed by C_{DC} (see Eq. 4.14).

To prevent interference between each sampled value and the previous DAC value, the charge on C_{IN} must be reset to a constant before each sample. In the implemented differential integrator, which will be discussed in Sec. 5.5, a form of return-to-zero sampling was used. Because switches could not be used to charge both V_{inp} and V_{inn} sampling capacitors to the mid-level voltage, V_{inp} was charged to V_{SS}, and V_{inn} was charged to V_{DD} just before each sampling phase. Thus, in Eq. 4.9, the prefactor for offset, $V_{CIN0} = V_{SS} - V_{DD}$. This offset decays exponentially, as indicated in Eq. 4.9.

5.3 Reset Operation

The integrators of a delta-sigma modulator must be initialized to zero at system startup and in case of modulator instability. The difficulty of zeroing a LV-ZCB integrator is that the output voltage needs to be set to the mid-level voltage, but it is not possible to conduct this voltage through a switch under low power supply voltages (as explained in Sec. 3.2). A method for setting the LV-ZCB integrator states to zero is shown in Fig. 5-4.

During the charge-transfer phase of the reset operation, a zero-crossing detector is used not to detect the virtual ground condition at node V_X (as during normal operation), but instead to detect when the output voltage, V_{out}, reaches the desired reset voltage, V_{RESET}, while V_X is held to V_{REFL}.

Note that because V_{RESET} will usually be the mid-level voltage, there can be no series switch between V_{out} and the input of the zero-crossing detector used for reset. Because the zero-crossing detector used for reset cannot be disconnected from V_{out}, separate zero-crossing detectors must be used for normal operation and reset operation. However, because the reset zero-crossing detector is only powered during startup and in the rare event of modulator instability, the use of an extra zero-crossing detector has negligible effect on power usage.

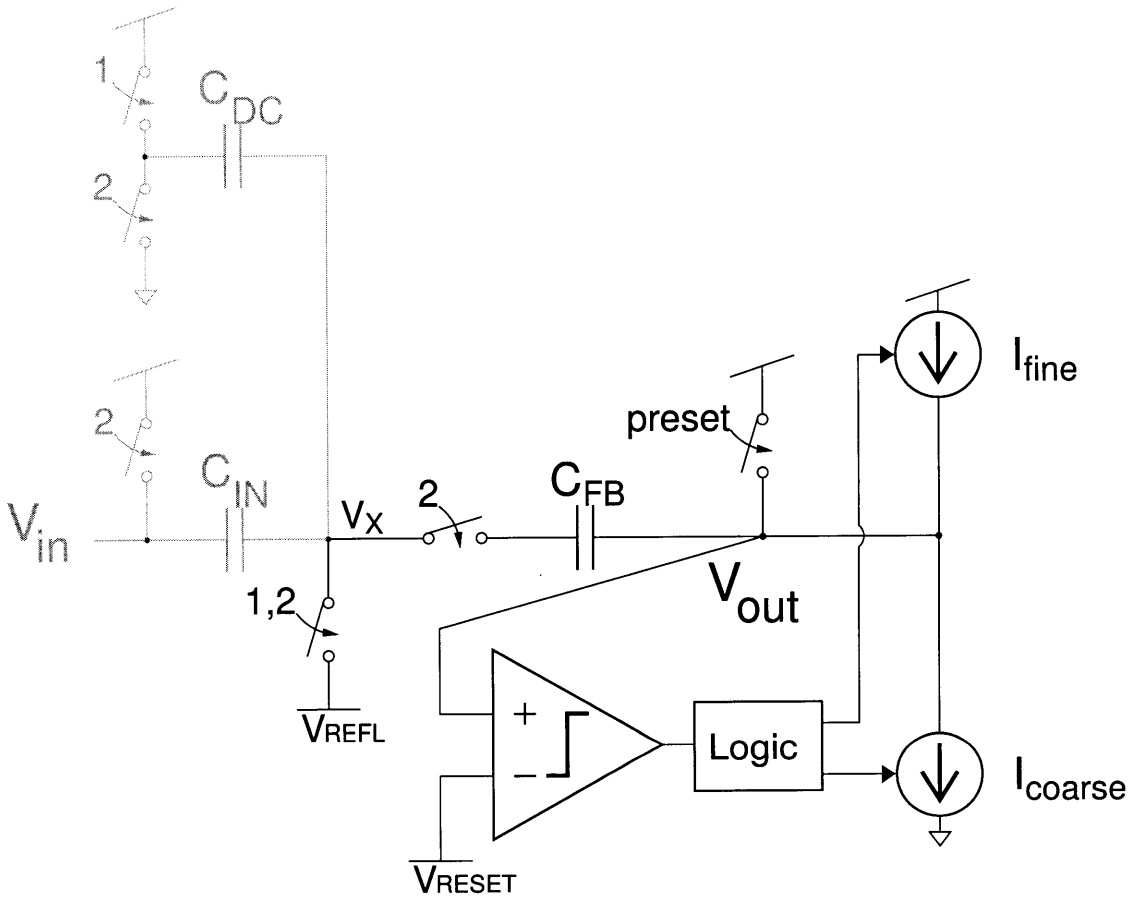


Figure 5-4: Single-ended low-voltage zero-crossing-based integrator in reset configuration

5.4 Gated Current Source Output Impedance

5.4.1 Voltage Drop Across Switches

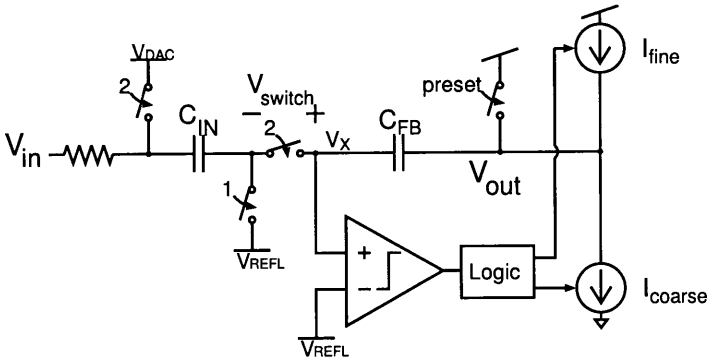
Unlike opamp-based switched-capacitor circuits, which settle to steady-state during the charge-transfer phase, current is still flowing through the switches of ZCB circuits at the instant the output voltage is sampled. Output-dependent variations in the voltage drop across these switches, whether from variations in switch resistance or current, lead to errors in the output voltage of the circuit. These variations are accentuated under low power supply voltages, where each switch has a higher resistance than at higher power supply voltages.

In [12] and [2], the voltage drop across the switch at the output of each ZCB pipeline stage is minimized through the use of "current source splitting". In this technique, each gated current source is divided into two separate sources, so that the drain and source of each switch can be charged separately with minimal current flowing through the switch itself. However, this solution is not applicable for a LV-ZCB integrator circuit because the switches that conduct during the charge-transfer are not at the output node.

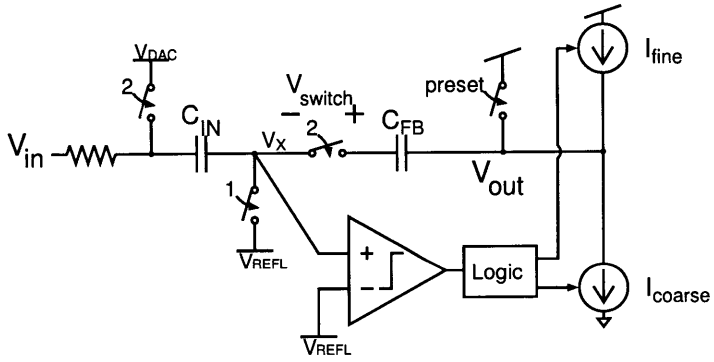
The series switch between C_{IN} and C_{FB} in Fig. 5-5 is always biased at virtual ground at the sampling instant at the end of each cycle's charge-transfer phase. Thus, the switch resistance does not vary from cycle-to-cycle[6]. However, due to the finite output impedance of current source I_{fine}, the current across the series switch is output-dependent, and so the voltage drop across the switch is also output-dependent. The effect of this output-dependent voltage drop depends on which node of the switch is connected to the crossing detector as the virtual ground node.

Compare the two possible implementations for an LV-ZCB integrator shown in Fig. 5-5. The implementation of Fig. 5-5(a) comes from applying the LV-ZCB technique directly to the conventional opamp-based switched-capacitor integrator of Fig. 4-1. In an opamp-based integrator, the inverting input of the opamp must be

[6]Note that in a differential implementation, the resistance can vary in response to a common-mode signal.



(a) LV-ZCB integrator based directly on switched-capacitor integrator topology (Fig. 4-1).



(b) LV-ZCB integrator as implemented with alternative crossing detector switch placement (functionally equivalent to Fig. 5-1).

Figure 5-5: Alternate locations around series switch for virtual ground node connection.

connected to the side of the series switch closer to C_{FB} because the opamp must stay in negative feedback during the sampling phase, ϕ_1. For an LV-ZCB integrator in this configuration, the amount of charge integrated onto C_{FB} (Eq. 5.10), becomes:

$$\Delta Q = C_{IN}\left(V_{in} - V_{DAC} - V_{\text{switch}}\right), \tag{5.12}$$

where V_{switch} is the voltage drop across the switch from C_{FB} to C_{IN}. The output voltage (Eq. 5.11) becomes:

$$\Delta V_{out} = \frac{\Delta Q}{C_{FB}} = \frac{C_{IN}}{C_{FB}}\left(V_{in} - V_{DAC} - V_{\text{switch}}\right).$$

Thus, the voltage drop across the series switch at virtual ground leads to an error in the integrator output voltage as well as in the charge integrated on C_{FB}. Because V_{switch} is output-dependent, these errors are also output-dependent.

In contrast with the implementation of Fig. 5-5(a), in the implementation of Fig. 5-5(b), the side of the series switch which is closer to C_{IN} is connected to the crossing detector as the virtual ground node. This configuration works for a ZCB integrator because the crossing detector doesn't use continuous feedback. In this implementation, the voltage drop across the switch only leads to an error in the sampled integrator output voltage, V_{out}, and causes no error in the amount of charge integrated on C_{FB}. Because the error is not integrated each cycle, it is attenuated by the integrator gain when input-referred. In a sigma-delta modulator (Ch. 6), the error is suppressed by first-order noise-shaping. In this sense, the configuration of Fig. 5-5(b) is superior to the configuration of Fig. 5-5(a).

5.4.2 Charge Integrated During Crossing Detector Delay

Another source of error caused by the finite output impedance of the gated current sources is the extra charge integrated onto C_{FB} each cycle due to the delay of the crossing detector and its related logic gates. Because the crossing detector has a finite bandwidth, and the logic that follows it has a nonzero propagation delay which

is further exacerbated by a low power supply voltage, there is a time, t_{delay}, at the end of the fine charge-transfer, between when the voltage at node V_X reaches virtual ground and when the crossing detector stops C_{FB} from being charged. Below we examine the effect of t_{delay} on the charge integrated onto C_{FB} for the case of a crossing detector with constant t_{delay}, as well as two cases (ideal integrator and steady-state) for crossing detectors with input-dependent delay.

Crossing Detector With Constant Delay

We model current source I_{fine} as an ideal current source of value I_{fine0} in parallel with a finite output impedance, r_o:

$$I_{fine} = I_{fine0} - \frac{V_{out}}{r_o}. \tag{5.13}$$

The negative sign before the $\frac{V_{out}}{r_o}$ term comes from the fact that as V_{out} gets higher, the voltage across current source I_{fine} gets smaller, and so I_{fine} gets smaller.

Because the change in V_{out} during t_{delay} is small compared to the full range of V_{out}, we consider I_{fine} to be relatively constant during t_{delay}. If t_{delay} is a constant, then the extra charge integrated onto C_{FB} during t_{delay} is

$$\begin{aligned} Q_{\text{overshoot}} &= I_{fine} t_{delay} \\ &= \left(I_{fine0} - \frac{V_{out}}{r_o} \right) t_{\text{delay}}. \end{aligned} \tag{5.14}$$

If we add this extra charge due to crossing detector delay to the result of Eq. 4.1, we get a total charge integrated onto C_{FB} of

$$\begin{aligned} \Delta Q &= C_{IN}(V_{in} - V_{REF}) + \left(I_{fine0} - \frac{V_{out}}{r_o} \right) t_{\text{delay}} \\ &= C_{IN} \left(V_{in} - V_{REF} - \frac{V_{out} t_{\text{delay}}}{r_o C_{IN}} \right) + I_{fine0} t_{\text{delay}} \end{aligned} \tag{5.15}$$

Eq. 5.15 shows that the nonzero delay of the crossing detector affects the charge integrated on C_{FB} by adding a constant term, $I_{fine0} t_{\text{delay}}$, as well as a term that

is proportional to the ratio of t_{delay} and the time-constant $r_o C_{IN}$. The ratio term is proportional to V_{out}, analogous to the finite opamp gain term in the comparable equation (Eq. 4.6) for the conventional switched-capacitor integrator. This shows that crossing detector delay, combined with the finite output impedance of the fine charge-transfer current source, has an effect in a ZCB integrator similar to finite opamp gain in a conventional switched-capacitor integrator.

Crossing Detector With An Ideal Integrator-Type Preamplifier

The analysis above assumes that the crossing detector and related logic have a constant delay, t_{delay}. In [22], a crossing detector with input-dependent delay is examined. In that analysis, the crossing detector consists of a single-stage preamplifier (transconductance G_M, output impedance R_o, total output capacitance C_o) followed by an infinitely fast threshold detector (threshold V_M) and infinitely fast logic gates. The delay of the crossing detector is then

$$t_{\text{delay}} = \begin{cases} \sqrt{\frac{2V_M C_o}{M_x G_m}}, & \text{Ideal integrator case (valid for } t_{delay} << R_o C_o), \\ \frac{V_M}{M_x G_m R_o}, & \text{Steady-state case (valid for } t_{delay} >> R_o C_o), \end{cases} \tag{5.16}$$

where M_x is the slope of the ramp at the input of the preamplifier, and t_{delay} is the time it takes between when the output of the preamplifier leaves a zero (clamp) voltage and when it reaches threshold V_M. Roughly speaking, for the same t_{delay}, the ideal integrator solution corresponds to a preamplifier with a lower bandwidth but higher gain, whereas the steady-state solution corresponds to one with a higher bandwidth but lower gain.

Repeating the same analysis used in the constant delay case, for the ideal integrator case, the extra charge added is

$$\begin{aligned} Q_{\text{overshoot,int}} &= I_{fine} t_{delay} \\ &= I_{fine} \sqrt{\frac{2V_M C_o}{M_x G_m}}. \end{aligned}$$

The slope of the ramp at the input of the preamplifier is $M_x = I_{fine}/C_{IN}$, and so

$$\begin{aligned} Q_{\text{overshoot,int}} &= I_{fine}\sqrt{\frac{2C_{IN}V_M C_o}{I_{fine}G_m}} \\ &= \sqrt{\frac{2I_{fine}C_{IN}V_M C_o}{G_m}}. \end{aligned}$$

Note that the delay of a crossing detector for the ideal integrator case is inversely proportional to I_{fine}, and so the dependence of $Q_{overshoot}$ on I_{fine} is partially cancelled. Substituting in the model given in Eq. 5.13 for I_{fine},

$$Q_{\text{overshoot,int}} = \sqrt{\frac{\left(I_{fine0} - \frac{V_{out}}{r_o}\right) 2C_{IN}V_M C_o}{G_m}}.$$

Assuming that $V_{out}/R_o << I_{fine}$ and using a Taylor series expansion to approximate,

$$\begin{aligned} Q_{\text{overshoot,int}} &= \sqrt{1 - \frac{V_{out}}{I_{fine0}r_o}}\sqrt{\frac{2I_{fine0}C_{IN}V_M C_o}{G_m}} \\ &\approx \left(1 - \frac{V_{out}}{2I_{fine0}r_o}\right)\sqrt{\frac{2I_{fine0}C_{IN}V_M C_o}{G_m}}. \end{aligned} \tag{5.17}$$

As we did for the case of a crossing detector with constant delay, we add this result to that of Eq. 4.1, and get a total charge integrated onto C_{FB} of

$$\begin{aligned} \Delta Q &= C_{IN}\left(V_{in} - V_{REF} - \frac{V_{out}\sqrt{\frac{2I_{fine0}C_{IN}V_M C_o}{G_m}}}{2I_{fine0}r_o C_{IN}}\right) + \sqrt{\frac{2I_{fine0}C_{IN}V_M C_o}{G_m}} \\ &= C_{IN}\left(V_{in} - V_{REF} - \frac{V_{out}}{r_o}\sqrt{\frac{V_M C_o}{2I_{fine0}C_{IN}G_m}}\right) + \sqrt{\frac{2I_{fine0}C_{IN}V_M C_o}{G_m}} \end{aligned} \tag{5.18}$$

Just like the solution for a constant delay in Eq. 5.14, the analysis of a crossing detector as an ideal integrator shows that the crossing detector delay causes the charge integrated onto C_{FB} to have a constant offset, as well as an error that is proportional to V_{out} and inversely proportional to r_o.

Crossing Detector With Preamplifier In Steady-State

For the steady-state case of Eq. 5.16, the extra charge added is

$$\begin{aligned} Q_{\text{overshoot,ss}} &= I_{fine}\frac{V_M}{M_x G_m R_o} \\ &= I_{fine}\frac{C_{IN}V_M}{I_{fine}G_m R_o} \\ &= \frac{C_{IN}V_M}{G_m R_o}, \end{aligned} \tag{5.19}$$

which is not a function of V_{out}. As the slope of the ramp at V_{out} changes due to the finite output impedance of I_{fine}, the crossing detector delay changes inversely and the two effects cancel [23]. Thus, the error caused by crossing detector delay in the charge integrated on C_{FB} is a constant offset which depends only on C_{IN} and parameters internal to the crossing detector.

As we did for the previous crossing detector cases, we add this result to that of Eq. 4.1, and get a total charge integrated onto C_{FB} of

$$\Delta Q = C_{IN}\left(V_{in} - V_{REF} + \frac{V_M}{G_m R_o}\right). \tag{5.20}$$

Comparing Eq. 5.20 to Eq. 4.6, we see that this case is similar to a conventional switched-capacitor integrator with an opamp that, just like the crossing detector preamplifier, has gain, $A = G_m R_o$, and has to reach a constant $V_{out} = -V_M$ each cycle.

Table 5.1 summarizes the results of comparing Eq. 4.6 with Eq. 5.15, Eq. 5.18, and Eq. 5.20. Note that in an actual implementation, the crossing detector and related logic gates would have a combination of constant and input-dependent delay.

For a typical current source, the output impedance, r_o, is inversely proportional to the bias current. Thus, the input-referred offset and output-dependent error are linearly dependent on I_{fine0} in the constant delay case, but dependent on the square root of I_{fine0} in the ideal integrator case. For both of these cases, input-referred offset

Table 5.1: Input-Referred Offset & Coefficient of Output-Dependent Error

topology	input-referred offset	output-dependence
switched-capacitor	$-V_{REF}$	$1/A$, A = finite opamp gain
ZCB, constant delay	$-V_{REF} + \frac{I_{fine0} t_{delay}}{C_{IN}}$	$\frac{t_{delay}}{r_o C_{IN}}$
ZCB, ideal integrator	$-V_{REF} + \sqrt{\frac{2 I_{fine0} V_M C_o}{C_{IN} G_m}}$	$\frac{1}{r_o}\sqrt{\frac{V_M C_o}{2 I_{fine0} C_{IN} G_m}}$
ZCB, steady-state	$-V_{REF} + \frac{V_M}{G_m R_o}$	0

and output dependence can be reduced by decreasing I_{fine}, the current of the gated current source in the final segment of the charge-transfer phase. This is an argument for using multiple ramps per charge-transfer phase.

5.4.3 Correlated Level-Shifting Technique

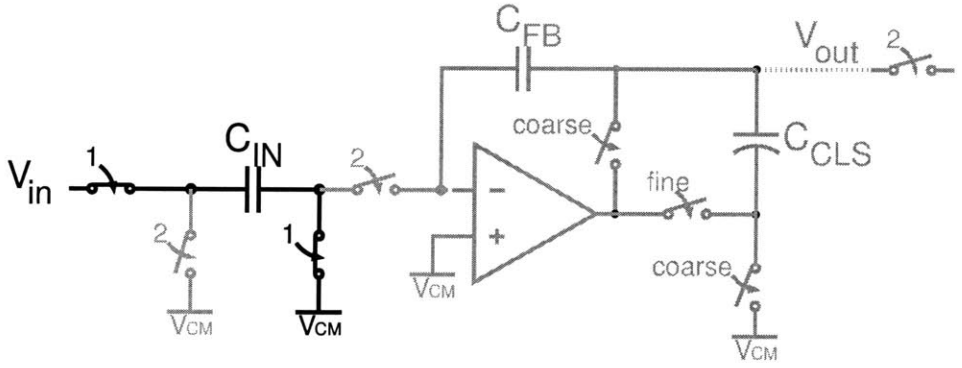
Correlated Level-Shifting in Conventional Switched-Capacitor Circuits

In [24], a switched-capacitor technique which reduces errors from finite opamp gain and limited opamp swing is presented. This technique is called correlated level-shifting (CLS) and is illustrated for a conventional switched-capacitor integrator in Fig. 5-6.

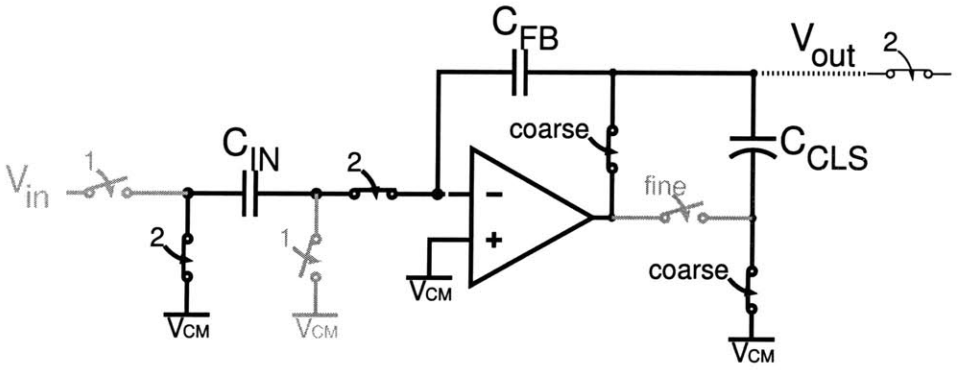
In the CLS technique, the sampling phase (Fig. 5-6(a)), ϕ_1, is identical to that for the non-CLS switched-capacitor integrator of Fig. 4-1. The difference between the CLS and non-CLS circuit occurs in the charge-transfer phase, ϕ_2, which is subdivided into coarse and fine charge-transfers for the CLS case.

During the coarse charge-transfer (Fig. 5-6(b)), the opamp settles as for the non-CLS switched-capacitor integrator. However, at the end of this settling, the output voltage, V_{out}, is sampled onto capacitor C_{CLS} as a coarse estimate of the final value of V_{out}.

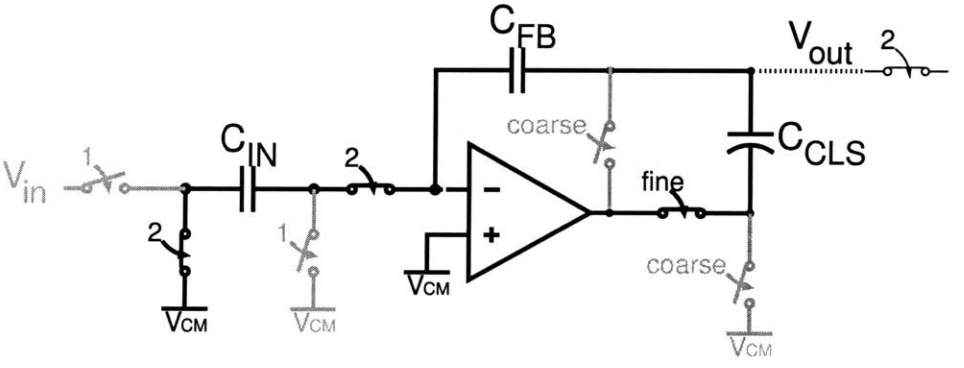
During the fine charge-transfer (Fig. 5-6(c)), the voltage sampled onto C_{CLS} is used as an offset between the output of the opamp and node V_{out}. Due to this correlated level-shifting, the voltage at the output of the opamp depends only on the difference between the coarse estimation of V_{out} and the final value of V_{out}. This decreased dependence on V_{out} reduces the effects of finite opamp gain, and potentially



(a) Sampling phase.



(b) Coarse charge-transfer.



(c) Fine charge-transfer.

Figure 5-6: Correlated level-shifting technique. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase (coarse + fine), ϕ_2 = "2".

increases the swing of V_{out} beyond the range possible if V_{out} was directly driven by the opamp.

Correlated Level-Shifting in ZCB Circuits

A level-shifting technique used to increase the linearity of the fine current source, I_{fine}, for a LV-ZCB integrator is similar to the CLS technique and is shown in Fig. 5-7. However, there is a significant additional benefit of combining this technique with ZCB circuits that use multiple ramps per charge-transfer phase, as will be explained later in this section.

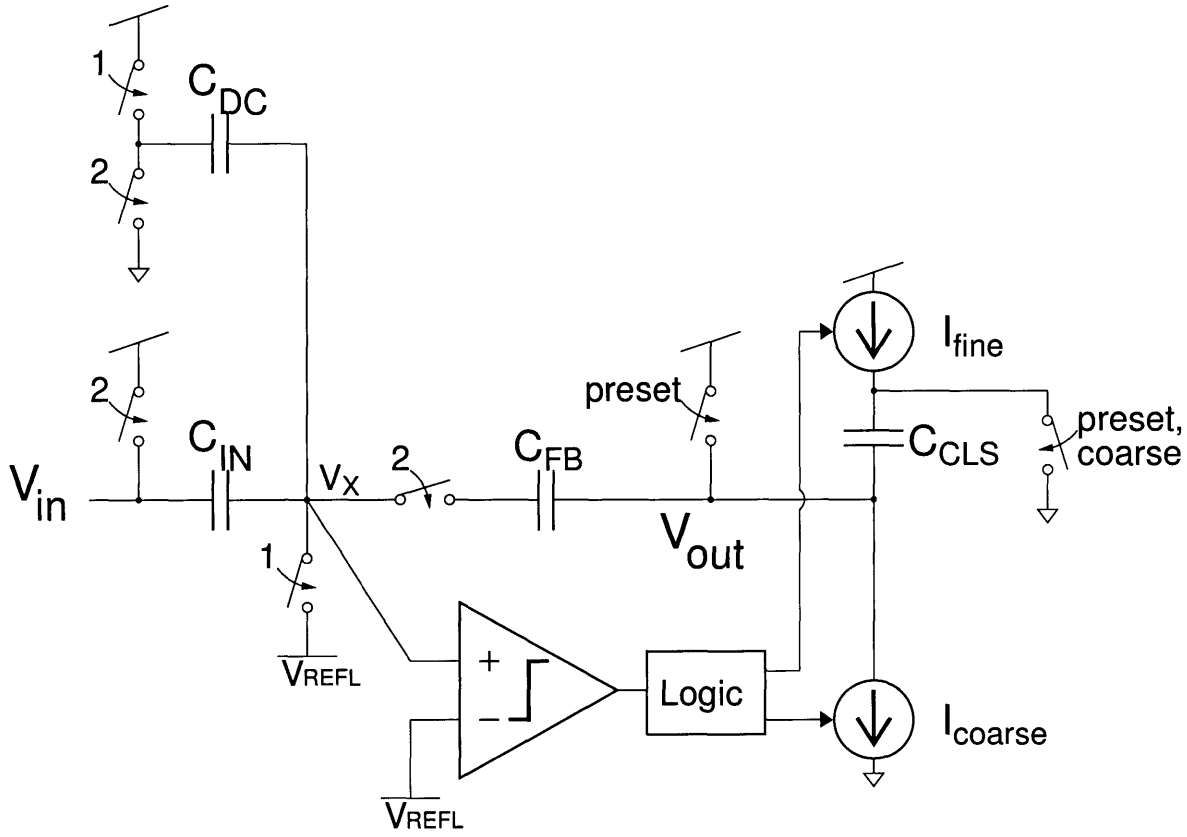


Figure 5-7: Single-ended low-voltage zero-crossing-based integrator showing use of correlated level-shifting for fine current source. Phase notation: sampling phase, ϕ_1 = "1"; charge-transfer phase (preset + coarse + fine), ϕ_2 = "2".

In this technique, I_{fine} is not directly connected to node V_{out} but instead is capacitively coupled via capacitor C_{CLS}. During the coarse charge-transfer, an extra

switch is closed, setting the voltage across C_{CLS} equal to the coarse approximation of V_{out}. This switch is then opened for the fine charge-transfer.

During the fine charge-transfer, when I_{fine} is used to drive V_{out}, the voltage seen by I_{fine} is level-shifted through C_{CLS} by a voltage equal to the coarse approximation of V_{out}. Thus, the voltage across current source I_{fine} at the start of the fine charge-transfer is $V_{DD}-V_{SS}$. The change in voltage across I_{fine} during the fine charge-transfer phase is only a function of the coarse overshoot, removing the dependence of current I_{fine} on the full value of V_{out}. Because the coarse overshoot is relatively constant, I_{fine} becomes much more constant. With this correlated level-shifting, the current I_{fine} at the end of the fine charge-transfer becomes (compare with Eq. 5.13)

$$\begin{aligned} I_{fine} &= I_{fine0} - (\text{voltage divider from } I_{fine} \text{ to } V_{out})^{-1} \left(\frac{V_{\text{overshoot,coarse}}}{r_o} \right) \\ &= I_{fine0} - \left(\frac{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}}{C_{FB}C_{CLS} + C_{IN}C_{CLS}} \right) \left(\frac{\frac{dV_{out}}{dt_{coarse}} t_{\text{delay,coarse}}}{r_o} \right), \end{aligned} \quad (5.21)$$

where $\frac{dV_{out}}{dt_{coarse}}$ is the ramp rate of V_{out} and $t_{\text{delay,coarse}}$ is the delay of the crossing detector during the coarse charge-transfer. If $t_{delay,coarse}$ is a constant, then the only dependence of I_{fine} on V_{out} now comes from $\frac{dV_{out}}{dt_{coarse}}$ which is given by

$$\begin{aligned} \frac{dV_{out}}{dt_{coarse}} &= \frac{I_{coarse}}{C_{CLS} + \frac{C_{FB}C_{IN}}{C_{FB}+C_{IN}}} \\ &= \frac{I_{coarse0} + \frac{V_{out}}{r_{o,coarse}}}{C_{CLS} + \frac{C_{FB}C_{IN}}{C_{FB}+C_{IN}}} \\ &= \frac{\left(I_{coarse0} + \frac{V_{out}}{r_{o,coarse}} \right) (C_{FB} + C_{IN})}{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}}, \end{aligned} \quad (5.22)$$

where $r_{o,coarse}$ is the output impedance of current source I_{coarse}. Substituting Eq. 5.22 into Eq. 5.21 gives

$$\begin{aligned} I_{fine} = I_{fine0} \\ - \left(\frac{C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN}}{C_{FB}C_{CLS} + C_{IN}C_{CLS}} \right) \left[\frac{\left(I_{coarse0} + \frac{V_{out}}{r_{o,coarse}} \right) (C_{FB} + C_{IN}) t_{\text{delay,coarse}}}{(C_{FB}C_{CLS} + C_{IN}C_{CLS} + C_{FB}C_{IN})\, r_o} \right] \end{aligned}$$

$$= I_{fine0} - I_{coarse0}\left(\frac{t_{\text{delay,coarse}}}{r_o C_{CLS}}\right) - \left(\frac{V_{out}}{r_o}\right)\left(\frac{t_{\text{delay,coarse}}}{r_{o,coarse} C_{CLS}}\right). \tag{5.23}$$

Assuming that $t_{delay,coarse}$ is a constant, the $I_{coarse0}$ term is a constant. The $\frac{V_{out}}{r_o}$ term represents the new output dependence of I_{fine} on V_{out}. We see from Eq. 5.23 that, through correlated-level shifting, the output impedance of I_{fine}, has effectively been multiplied:

$$r_{o,CLS} = r_o\left(\frac{r_{o,coarse} C_{CLS}}{t_{delay,coarse}}\right). \tag{5.24}$$

Another benefit of correlated level-shifting that is unique to ZCB circuits which use multiple ramps per charge-transfer phase is that, due to the decreased swing requirement on I_{fine}, techniques such as cascoding can be used to implement the I_{fine} current source, further improving the output impedance of I_{fine}. This benefit does not apply to the opamp case presented by [24], where the same opamp circuitry is used for both the coarse and fine charge-transfer phases. All of these improvements to output impedance reduce the errors explained in Sec. 5.4.1 and Sec. 5.4.2.

Note that for large values of C_{CLS}, I_{fine} is able to pull V_{out} beyond V_{DD}. However, not only would this reduce transistor reliability, but also this extended signal swing is limited by the fact that it is unidirectional, extending beyond V_{DD} but not beyond V_{SS}.

5.5 Differential LV-ZCB integrator

A low-voltage zero-crossing-based integrator which uses differential signaling is shown in Fig. 5-8. Just as in the single-ended LV-ZCB integrator of Fig. 5-7, the preset operation sets the differential output voltage to the maximum possible value, which for a differential signal is $(V_{DD} - V_{SS})$. Thus, during preset, V_{outp} is pulled to V_{DD}, and V_{outn} is pulled to V_{SS}.

To prevent the virtual ground nodes, V_{Xp} and V_{Xn}, from exceeding the power supply rails during preset, different virtual ground reference voltages, V_{REFL} and

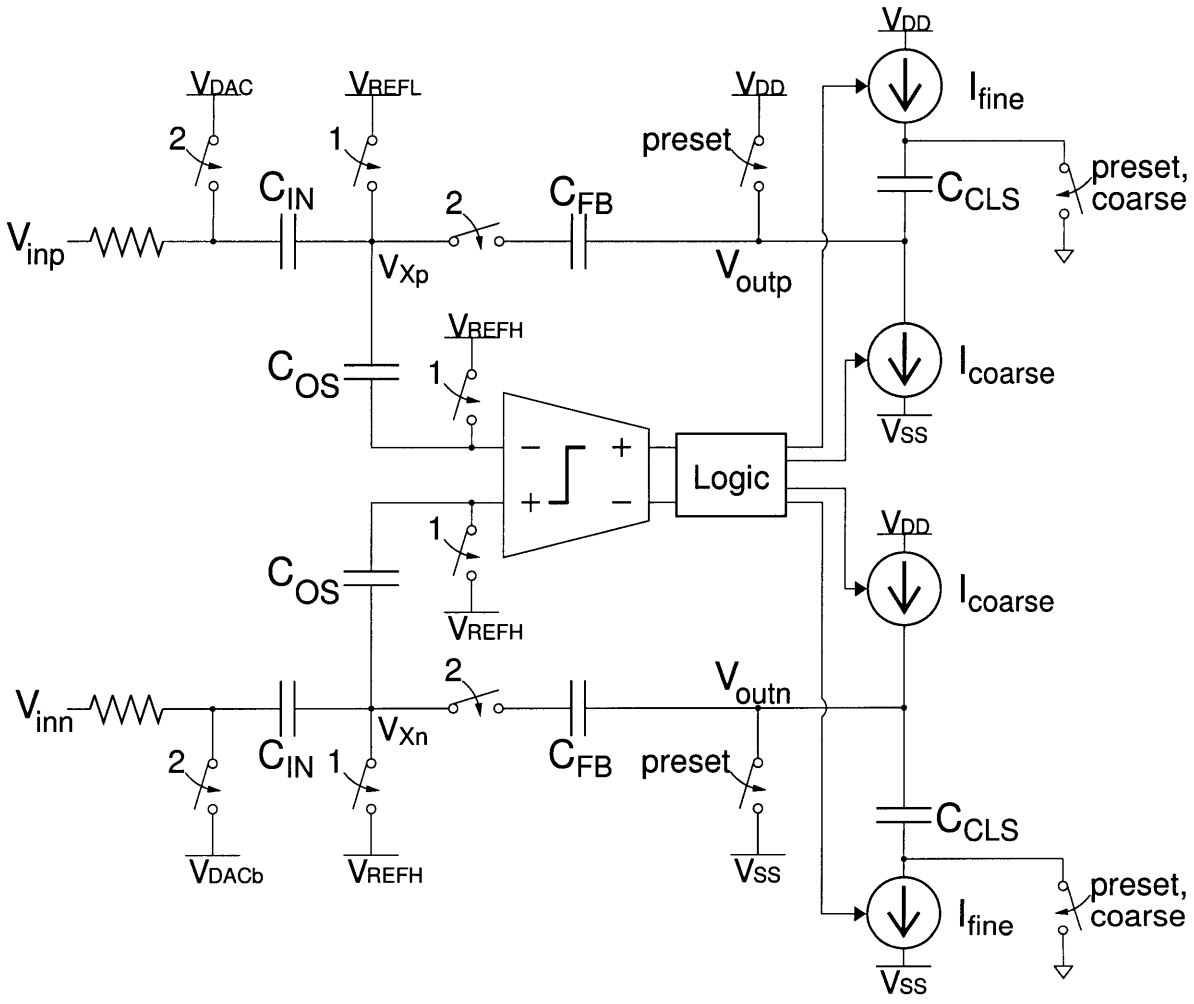


Figure 5-8: Differential low-voltage zero-crossing-based integrator showing use of correlated-level shifting for fine current source. V_{DAC} and its complement V_{DACb} are input reference levels set by an external DAC.

V_{REFH}, which are close but not equal to V_{SS} and V_{DD}, respectively, are used for the positive and negative differential signal paths. The margins between V_{REFL} / V_{REFH} and V_{SS} / V_{DD} prevent the voltages at the virtual ground nodes from exceeding the power supply due to crossing detector delay (overshoot) during the coarse charge-transfer.[7]

The difference in virtual ground reference voltages between the differential signal paths is adjusted for at the input to the crossing detector via a constant offset implemented with capacitors C_{OS}. These offset capacitors can be large because they are charged to the same voltage every cycle and are never discharged, and thus have little effect on power consumption or speed of operation. Note that the voltage across capacitors C_{OS} must be given time at system startup to settle to an accuracy of $\frac{V_{LSB}}{2}\frac{C_{IN}}{C_{IN}+C_{FB}}$, where V_{LSB} is the change in voltage of the input-signal corresponding to one least-significant bit at the output of the ADC. However, this requirement is not a significant disadvantage in a delta-sigma ADC because it can occur in parallel with the initialization of the integration capacitors, C_{FB}, which is already required for proper modulator operation (Sec. 5.3).

5.5.1 Reference Voltages and Signal Swing

The use of capacitors C_{OS} adds an additional restriction to the voltage at V_{Xp}. To avoid exceeding V_{DD} at the input to the crossing detector which corresponds with the positive signal path,

$$V_{Xp} + V_{REFH} - V_{REFL} \leq V_{DD} \tag{5.25}$$

[7]A possible variation would be to preset both differential outputs to the same power supply voltage, putting a common-mode offset on the output. However, it would be difficult to reduce this common-mode offset to zero at the same instant that the charge-transfer completes. Consider the case where the final value for the differential $V_{outp} - V_{outn} = 0$. In this case, the charge-transfer time would be zero, and the common-mode adjustment would have to be infinitely fast.

As explained in Sec. 5.1.1, the maximum possible voltage of V_{Xp} is $V_{DD} - V_{tn}$. Thus, Eq. 5.25 becomes

$$\begin{aligned}(V_{DD} - V_{tn}) + V_{REFH} - V_{REFL} &\leq V_{DD} \\ V_{REFH} - V_{REFL} &\leq V_{DD} - (V_{DD} - V_{tn}) \\ V_{REFH} - V_{REFL} &\leq V_{tn}. \end{aligned} \tag{5.26}$$

Eq. 5.8 can be used to write the conditions for the virtual ground reference voltages, V_{REFL} and V_{REFH}, such that nodes V_{Xp} and V_{Xn} do not exceed the power supply rails during preset:

$$V_{REFL} \leq \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right) V_{outp,min} + \left(\frac{C_{IN}}{C_{FB}+C_{IN}}\right)(V_{DD} - V_{tn}) \tag{5.27}$$

$$V_{REFH} \geq \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right) V_{outn,max} + \left(\frac{C_{IN}}{C_{FB}+C_{IN}}\right)(V_{SS} + |V_{tp}|). \tag{5.28}$$

The maximum negative swing of the differential output voltage, $V_{out} = V_{outp} - V_{outn}$, for which virtual ground reference voltages can be chosen to satisfy Eq. 5.26, Eq. 5.27, and Eq. 5.28, can be solved for by substituting Eq. 5.27 and Eq. 5.28 into Eq. 5.26:

$$\left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right)(V_{outn,max} - V_{outp,min}) + \left(\frac{C_{IN}}{C_{FB}+C_{IN}}\right)(V_{SS} + |V_{tp}| - V_{DD} + V_{tn}) \leq V_{tn}$$

$$\begin{aligned}(V_{outn,max} - V_{outp,min}) &\leq \frac{V_{tn} - \left(\frac{C_{IN}}{C_{FB}+C_{IN}}\right)(V_{SS} + |V_{tp}| - V_{DD} + V_{tn})}{\frac{C_{FB}}{C_{FB}+C_{IN}}} \\ &= \left(\frac{C_{FB}+C_{IN}}{C_{FB}}\right) V_{tn} - \left(\frac{C_{IN}}{C_{FB}}\right)(V_{SS} + |V_{tp}| - V_{DD} + V_{tn}) \\ &= V_{tn} + \left(\frac{C_{IN}}{C_{FB}}\right)(V_{DD} - V_{SS} - |V_{tp}|). \end{aligned} \tag{5.29}$$

For example, if $V_{SS} = 0$ V, $V_{DD} = 1$ V, $C_{IN} = 1$ pF, $C_{FB} = 2.7$ pF, and $V_{tn} = |V_{tp}| = 350$ mV, then $V_{outn,max} - V_{outp,min} = 591$ mV. If we assume that the common mode

for this value of V_{out} is $(V_{DD} + V_{SS})/2$, then $V_{outp,min} = 205$ mV and $V_{outn,max} = 795$ mV. Substituting these values back into Eq. 5.27 and Eq. 5.28 gives $V_{REFL} = 325$ mV and $V_{REFH} = 675$ mV.

By comparing the limitation on signal swing given by Eq. 5.26 to the full-scale range of $V_{DD} - V_{SS}$, it can be seen that

$$\begin{aligned} \frac{V_{outn,max} - V_{outp,min}}{V_{DD} - V_{SS}} &= \frac{V_{tn} + \left(\frac{C_{IN}}{C_{FB}}\right)(V_{DD} - V_{SS} - |V_{tp}|)}{V_{DD} - V_{SS}} \\ &= \frac{V_{tn} - \left(\frac{C_{IN}}{C_{FB}}\right)|V_{tp}|}{V_{DD} - V_{SS}} + \frac{C_{IN}}{C_{FB}}. \end{aligned}$$

Thus, as the power supply range, $V_{DD} - V_{SS}$, decreases, the maximum negative signal swing at the output of the integrator becomes a larger fraction of full-scale. For $V_{tn} = |V_{tp}| = V_t$ and $V_{DD} - V_{SS} = V_t$, the maximum negative signal swing, $V_{outn,max} - V_{outp,min}$, becomes equal to full-scale.

Although not tested in the implemented chip, if the condition given by Eq. 5.26 is too strict for the desired swing for V_{out}, an extra capacitor can be placed between the inputs of the crossing detector. Along with capacitors C_{OS}, this extra capacitor will serve as a voltage divider from the virtual ground nodes, V_{Xp} and V_{Xn}, attenuating the signal at the input of the crossing detector to prevent it from exceeding V_{DD}. Note that this will also have the detrimental effect of increasing the crossing detector noise when it is referred back to the integrator input. Thus this solution should be used only as a last resort (i.e. when it is impossible to choose a set of virtual ground reference voltages, V_{REFL} and V_{REFH}, that satisfy all required conditions).

5.5.2 Design Asymmetry

Although not illustrated in Fig. 5-8, the differential LV-ZCB integrator is asymmetrical with respect to the positive and negative differential signal paths. Without using clock boosting or gate bootstrapping, only a NMOS switch can conduct V_{REFL}, and only a PMOS switch can conduct V_{REFH}. Thus, the use of different virtual ground reference voltages forces the positive and negative signal paths to be NMOS/PMOS

complements; a transistor that is implemented with an NMOS in one path is implemented as a PMOS in the other and vice-versa.

5.5.3 Output Common-Mode Issues

Controlling the common-mode at the output of a low-voltage ZCB circuit is more difficult than for conventional ZCB circuits that operate under higher power supply voltages with no common-mode feedback. In the conventional ZCB circuit of [2], no common-mode feedback is required; the output common-mode level is set during the preset. During the charge-transfer phase, the common-mode level at the output is not disturbed because V_{outp} and V_{outn} nominally change at the same rate in opposite directions.

The difficulty of controlling the common-mode level at the output of a LV-ZCB circuit comes from the fact that, due to the low gate drive, the series switches between the virtual ground nodes, V_{Xp}/V_{Xn}, and C_{FB} capacitors are not continuously conductive during the charge-transfer ramp. Thus, the capacitive loads on the gated current sources, I_{coarse}, vary with time and are not guaranteed to be equal for the positive and negative signal paths.

As an example, consider the positive signal path of Fig. 5-8. During the preset, V_{outp} is pulled to V_{DD}, pulling the drain/source voltage of the NMOS series switch (between V_{Xp} and C_{FB}) above V_{REFL}. If this voltage is pulled above $V_{DD} - V_{tn}$, then the series switch stops conducting. During the coarse charge-transfer, V_{outp} is ramped down towards V_{SS} by I_{coarse}. While the series switch between V_{Xp} and C_{FB} is not conducting, C_{FB} is left floating. The capacitive load on I_{coarse} is then C_{CLS}. If I_{coarse} is implemented as a constant current source, the ramp rate of V_{outp} is

$$\frac{dV_{outp}}{dt} = \frac{I_{coarse}}{C_{CLS}}.$$

When the voltage at the drain/source of the series switch gets to $V_{DD} - V_{tn}$ or lower, the NMOS series switch begins to conduct, and the load on I_{coarse} becomes $C_{CLS} +$

$\frac{C_{FB}C_{IN}}{C_{FB}+C_{IN}}$. Accordingly, the ramp rate changes to

$$\frac{dV_{outp}}{dt} = \frac{I_{coarse}}{C_{CLS} + \frac{C_{FB}C_{IN}}{C_{FB}+C_{IN}}}.$$

A similar process happens in the negative signal path. During the coarse charge-transfer, the PMOS series switch between V_{Xn} and C_{FB} begins to conduct when the voltage at the drain/source of the switch gets to $V_{SS} + |V_{tp}|$ or higher. However, because $|V_{tp}|$ is not guaranteed to equal V_{tn} for any process, the changes in ramp rate of V_{outp} and V_{outn} are not guaranteed to occur simultaneously, leading to an error in the common-mode level at the output of the integrator.[8]

The common-mode error alone may not be detrimental if the integrator output is being sampled by a circuit with a high common-mode rejection ratio. However, for large integrator outputs, $V_{outp} - V_{outn}$, an output common-mode error may cause one of the I_{coarse} current sources driving V_{outp} or V_{outn} to enter the linear region. At that point, the differential ramp rate at the output, $\frac{d(V_{outp}-V_{outn})}{dt}$ will decrease, and therefore the coarse overshoot will decrease. Because the coarse overshoot affects the final voltage across the I_{fine} current sources (Eq. 5.21), the fine overshoot will increase. Thus, the constant portion of the fine overshoot will no longer be constant from cycle-to-cycle, affecting the accuracy of the integrator.

5.5.4 Voltage Ramp Generator

To address the issue of output common-mode control in the LV-ZCB integrator, each coarse gated current source is implemented as a voltage ramp generator [25].

The basic concept of the voltage ramp generator is illustrated in Fig. 5-9. The amplifier and capacitor, C_{RG}, in negative feedback act as an integrator for current

[8] An alternative topology for the differential LV-ZCB integrator could be made that does not suffer from this problem. One possibility would be to reduce the swing of the virtual ground nodes by putting a capacitor between V_{Xp} and V_{Xn}. However, the attenuation would increase the input-referred noise of the crossing detector. Alternatively, another coarse charge-transfer could be used in place of the preset, such that the charge-transfer phase consisted of two coarse and one fine charge-transfer. However, without the preset to reset the common-mode level at the output, additional circuitry would be required for common-mode feedback. Also, circuitry to control an extra charge-transfer ramp would almost certainly be more complex than to control the preset.

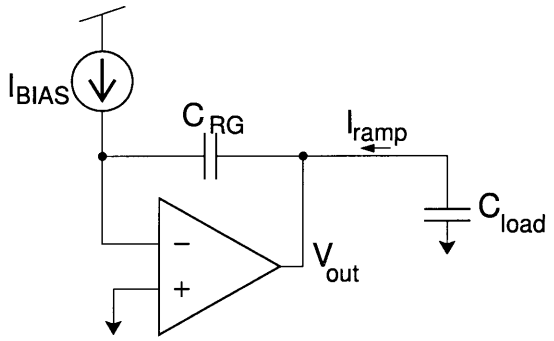


Figure 5-9: Voltage ramp generator concept

source I_{BIAS}. As I_{BIAS} charges C_{RG}, the voltage at the input to the amplifier is held constant by negative feedback through C_{RG}. Thus, the change in voltage across C_{RG} appears at V_{out}, which is the same as node V_{outp} or V_{outn} in the differential LV-ZCB integrator of Fig. 5-8. The ramp rate at V_{out} is

$$\frac{dV_{out}}{dt} = \frac{-I_{\text{BIAS}}}{C_{RG}}.$$

In performing the negative feedback, the amplifier also sinks current I_{ramp}, which is the variable amount of current required to charge variable C_{load} at a rate of $\frac{dV_{out}}{dt}$. C_{load} in this diagram represents the load on the corresponding I_{coarse} current source of Fig. 5-8.

A low-voltage compatible implementation of a voltage ramp generator is seen in Fig. 5-10. The design of Fig. 5-10 operates under two clock phases, a biasing phase and a voltage ramp phase, which correspond to the preset and coarse charge-transfer, respectively, of Fig. 5-8. During the coarse charge-transfer, M_2 provides the gain for the feedback loop with capacitor C_{RG}. As I_{BIAS} charges C_{RG}, the voltage at the gate of M_2 is held constant by negative feedback through C_{RG}. During the coarse charge-transfer, the ramp rate at the gate of M_1 and M_2 is given by

$$\frac{dV_{g1}}{dt} = \frac{I_{\text{BIAS}}}{C_g + (1 + A_{V2})C_{RG}},$$

where C_g is the parasitic capacitance at the gate of M_1/M_2 and $A_{V2} = g_{m2}Z_{out}$, where

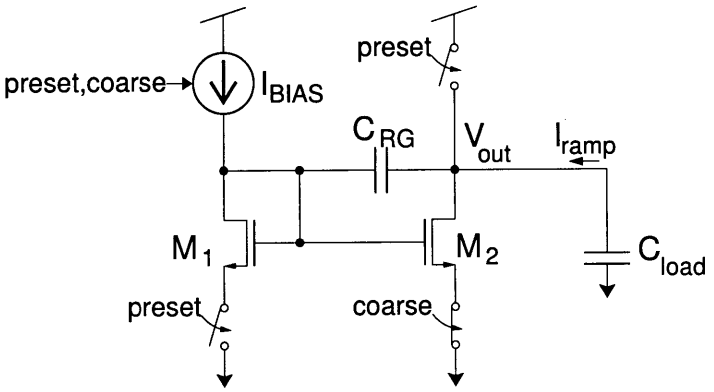


Figure 5-10: Possible implementation of voltage ramp generator. To minimize startup transients, $W_{M2}/W_{M1} = 1 + C_{\text{load}}/C_{RG}$.

Z_{out} is the impedance at V_{out}. The ramp rate at the output of M_2 is

$$\begin{aligned} \frac{dV_{out}}{dt} &= -A_{V2} * \frac{dV_{g1}}{dt} \\ &= \frac{-A_{V2} I_{\text{BIAS}}}{C_g + (1 + A_{V2}) C_{RG}} \\ &\approx \frac{-I_{\text{BIAS}}}{C_{RG}}, \end{aligned} \tag{5.30}$$

for large values of A_{V2}. Thus, regardless of change in capacitive load, C_{load}, the voltage signal at the output, V_{out}, is a linear ramp[9]. The common-mode for differential integrator outputs V_{outp} and V_{outn} in Fig. 5-8 is thus controlled by independently setting the magnitudes of the ramp rates for the coarse current sources (voltage ramp generators) of the positive and negative paths to the same constant.

The preset switch on V_{out} corresponds to the preset switch on either V_{outp} or V_{outn} of Fig. 5-7. M_1 is used to set the starting voltage across C_{RG} during the biasing phase (preset). A limitation for this particular topology is the long settling time for the voltage across C_{RG} during this phase. If faster operation is required, biasing of C_{RG} can take place during the sampling phase, ϕ_1, during which time the preset switch at V_{out} is also closed to provide a reference voltage for the subsequent stage (see Sec. 5.1).

To minimize startup transients at the transition from the biasing to voltage ramp

[9]Note that C_{load} affects Z_{out}, and if C_{load} gets large enough, A_{V2} becomes frequency-dependent.

phase, the widths of M_1 and M_2 should be ratioed such that

$$\frac{W_{M2}}{W_{M1}} = 1 + \frac{C_{\text{load}}}{C_{RG}}.$$

Because C_{load} is not constant, the above ratio should be chosen as a compromise between $C_{\text{load}} = C_{CLS}$ and $C_{\text{load}} = C_{CLS} + \frac{C_{FB}C_{IN}}{C_{FB}+C_{IN}}$, plus the capacitance of any other circuits which sample V_{out}.

The fine current sources, I_{fine}, are not voltage ramp generators, but instead use correlated level-shifting (Sec. 5.4.3). Voltage ramp generators are not required during the fine charge-transfer, because after the coarse charge-transfer is completed, $V_{Xp} \approx V_{REFL}$ and $V_{Xn} \approx V_{REFH}$. Thus the series switches between the virtual ground nodes, V_{Xp}/V_{Xn}, and C_{FB} capacitors are conductive during the fine charge-transfer ramp. Also, the change in V_{outp} and V_{outn} during the fine charge-transfer is small, so any change in common-mode voltage would also be small.

5.5.5 Maximum Common-Mode Swing at Input

Suppose a common-mode signal, $V_{in,cm} = (V_{inp} + V_{inn} - (V_{DD} + V_{SS}))/2$, is introduced at the input to the LV-ZCB integrator. This corresponds to a charge of $-C_{IN}V_{in,cm}$ on each of the sampling capacitors, C_{IN}. During the preset, this charge is shared between C_{IN} and C_{FB}, creating a common-mode shift at the virtual ground nodes of

$$V_{X,cm} = \frac{-C_{IN}V_{in,cm}}{C_{FB} + C_{IN}}.$$

Note that any parasitic capacitance at node V_X will add to the denominator of the above equation. Because the voltage ramp generators prevent a common-mode signal from developing at the output of the integrator, this common-mode shift remains on the virtual ground nodes for the duration of the charge-transfer phase. Thus, it is important to identify how this shift affects the operation of the integrator.

Switch Conductance at End of Charge-Transfer Phase

For a shift in the common-mode, $V_{X,cm}$, at the virtual ground nodes, the following conditions must be met for the series switch between V_{Xp} or V_{Xn} and the respective C_{FB} capacitor to be able to conduct at the end of the charge-transfer phase:

$$\begin{aligned} V_{REFL} + V_{X,cm} &\leq V_{DD} - V_{tn} \\ V_{REFH} + V_{X,cm} &\geq V_{SS} + |V_{tp}|. \end{aligned}$$

If either of these conditions are not met, then the charge transfer from C_{IN} to C_{FB} on one of the differential sides will be incomplete, leading to a differential error in the final output voltage. To avoid this error, the common-mode swing at V_{in} must be limited to

$$\begin{aligned} (V_{REFL} - V_{DD} + V_{tn}) \leq \quad & -V_{X,cm} \quad \leq (V_{REFH} - V_{SS} - |V_{tp}|) \\ (V_{REFL} - V_{DD} + V_{tn}) \leq \quad & \tfrac{C_{IN} V_{in,cm}}{C_{FB}+C_{IN}} \leq (V_{REFH} - V_{SS} - |V_{tp}|) \\ \left(\frac{C_{FB}+C_{IN}}{C_{IN}}\right)(V_{REFL} - V_{DD} + V_{tn}) \leq \quad & V_{in,cm} \quad \leq \left(\frac{C_{FB}+C_{IN}}{C_{IN}}\right)(V_{REFH} - V_{SS} - |V_{tp}|). \end{aligned}$$

For example, if V_{SS} = 0 V, V_{DD} = 1 V, C_{IN} = 1 pF, C_{FB} = 2.7 pF, V_{tn} = $|V_{tp}|$ = 350 mV, V_{REFL} = 325 mV, and V_{REFH} = 675 mV, then the limit on $V_{in,cm}$ is -1.203 V $\leq V_{in,cm} \leq$ 1.203 V.

Note that, in comparison to the differential LV-ZCB integrator, for a differential switched-opamp integrator, the virtual ground reference voltages for the positive and negative paths are typically the same (either both V_{REFL} or both V_{REFH}). Thus, for switched-opamp integrators, the requirement that the series switches conduct at the end of the charge-transfer phase leads to a one-sided limit on $V_{in,cm}$[10].

[10]The other side of the limit for the input common-mode level of a switched-opamp integrator is based on the condition that the virtual ground nodes not exceed the power supply rails during charge-transfer.

Node Voltages During Preset

The shift in the common-mode voltage at the virtual ground nodes will also affect the conditions given in Eq. 5.27 and Eq. 5.28 for V_{REFL} and V_{REFH} (the maximum V_{REFL} and minimum V_{REFH} such that no node voltages exceed V_{DD} during the preset). The modified conditions are

$$V_{REFL} - \frac{C_{IN}V_{in,cm}}{C_{FB}+C_{IN}} \leq \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right) V_{outp,min} + \frac{C_{IN}}{C_{FB}+C_{IN}}(V_{DD} - V_{tn})$$

and

$$V_{REFH} - \frac{C_{IN}V_{in,cm}}{C_{FB}+C_{IN}} \geq \left(\frac{C_{FB}}{C_{FB}+C_{IN}}\right) V_{outn,max} + \frac{C_{IN}}{C_{FB}+C_{IN}}(V_{SS} + |V_{tp}|).$$

The maximum negative swing of the differential output voltage of the integrator, $V_{outp,min} - V_{outn,max}$, is fully constrained by the above equations and by Eq. 5.26 for capacitor C_{OS}. Thus, to allow for a common-mode shift of $\pm V_{in,cm}$ at the input of the integrator, the maximum negative swing of the differential output voltage must be reduced by $2\,C_{IN}V_{in,cm}/C_{FB}$ to prevent any nodes from exceeding the power supply voltages during preset. For example, if $C_{IN} = 1$ pF and $C_{FB} = 2.7$ pF, to allow for a ± 50 mV swing in the common mode at the input of the integrator would require a reduction in $V_{outn,max} - V_{outp,min}$ of 37 mV.

Chapter 6

Delta-Sigma Modulator

This chapter briefly introduces the use of delta-sigma modulation in implementing analog-to-digital conversion. Next, the use of zero-crossing-based integrators in delta-sigma ADCs is compared to the more traditional use of opamp-based switched-capacitor integrators.

6.1 Basic Principle

6.1.1 Feedback

Signal Transfer Function

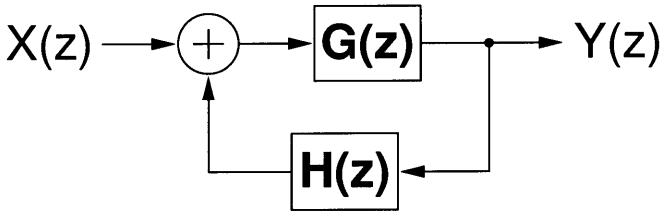


Figure 6-1: Generic feedback system.

The feedback system in Fig. 6-1 with forward path gain, $G(z)$, and feedback path

gain, $H(z)$, has a transfer function of

$$\begin{aligned} Y(z) &= X(z)G(z) + Y(z)G(z)H(z) \\ Y(z)[1 - G(z)H(z)] &= X(z)G(z) \\ \frac{Y(z)}{X(z)} &= \frac{G(z)}{1 - G(z)H(z)}, \end{aligned}$$

which for negative feedback systems ($H(z) < 0$), we get

$$\begin{aligned} \frac{Y(z)}{X(z)} &= \frac{G(z)}{1 + G(z)|H(z)|} \\ &\approx \frac{1}{|H(z)|} \quad \text{for large G(z).} \end{aligned} \tag{6.1}$$

Noise Transfer Function

Suppose a noise signal, $N(z)$, is introduced at the output of $G(z)$ as shown in Fig. 6-2. The transfer function from noise to the output is

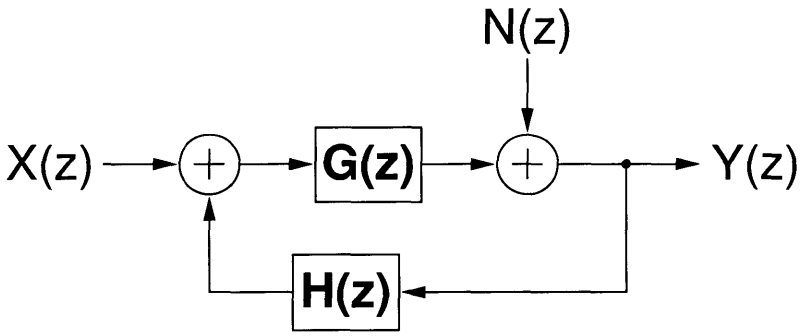


Figure 6-2: Generic feedback system with noise signal.

$$\begin{aligned} Y(z) &= N(z) + Y(z)G(z)H(z) \\ Y(z)[1 - G(z)H(z)] &= N(z) \\ \frac{Y(z)}{N(z)} &= \frac{1}{1 - G(z)H(z)}, \end{aligned}$$

which for a negative feedback system becomes

$$\begin{aligned} \frac{Y(z)}{N(z)} &= \frac{1}{1+G(z)|H(z)|} \\ &\approx 0 \quad \text{for large G(z).} \end{aligned} \tag{6.2}$$

6.1.2 Delta-Sigma Analog-to-Digital Converter

A delta-sigma analog-to-digital converter (Fig. 6-3) is a negative feedback system which has a large forward path gain in the signal band and a unity feedback path gain. According to Eq. 6.1 and Eq. 6.2, a large forward path gain leads to a transfer

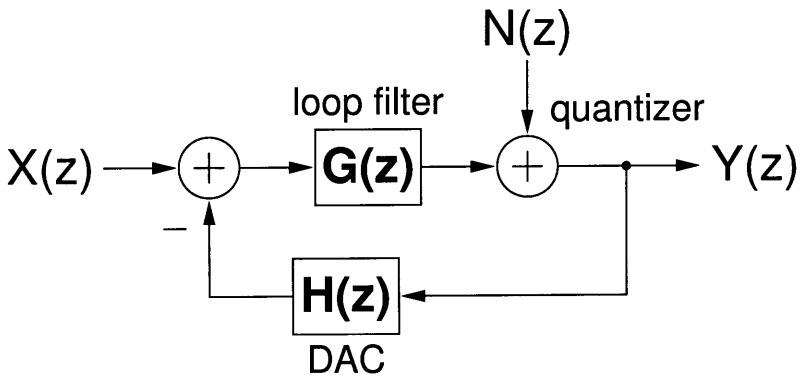
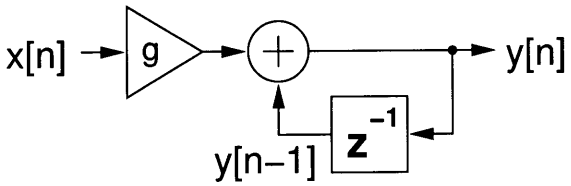


Figure 6-3: Generic delta-sigma loop.

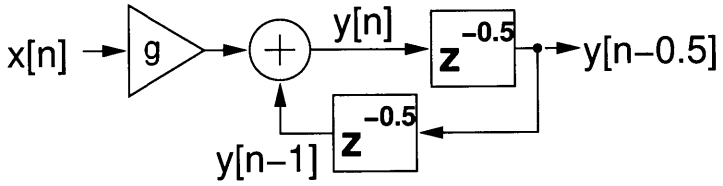
function of approximately 1 for the signal, and a transfer function of approximately 0 in the signal band for the noise added by the quantizer. In this manner, quantization noise is suppressed in the signal band. A digital decimation filter can then be used to remove the out-of-band quantization noise.

6.2 Integrator System Diagrams

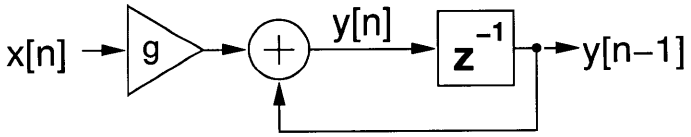
Fig. 6-4 shows system diagrams for delay-free, half-cycle delay, and full-cycle delay integrators. These system diagrams match with the switched-capacitor integrators in Fig. 4-2(a), Fig. 4-2(b), and Fig. 4-2(c), respectively. All three system diagrams implement the same system function, the distinction being where along the unit-delay



(a) Delay-free inverting integrator.



(b) Integrator with half-cycle delay



(c) Integrator with full-cycle delay.

Figure 6-4: System diagrams for different integrator timings.

feedback loop each output is tapped. Using the z-transform time-shifting property, $x[n-k] \overset{\mathcal{Z}}{\longleftrightarrow} z^{-k}X(z)$, we can see that the system function implemented in the diagram is

$$\begin{aligned} y[n] &= gx[n] + y[n-1] \\ Y(z) &= gX(z) + z^{-1}Y(z) \\ H(z) &= \frac{Y(z)}{X(z)} = \frac{g}{1-z^{-1}} \end{aligned} \tag{6.3}$$

which represents a discrete-time integrator (also known as an accumulator) with gain g. The impulse response of this system is a step function:

$$h[n] = gu[n].$$

6.2.1 Loop Filter Implemented Using One Integrator

Sec. 6.1.2 discussed the basic principle of the delta-sigma analog-to-digital converter. Consider the case of a delta-sigma ADC implemented using the full-cycle delay integrator of Fig. 6-4(c) as the loop filter. Using Eq. 6.3, the transfer function of this integrator is

$$G(z) = \frac{Y(z)z^{-1}}{X(z)} = \frac{gz^{-1}}{1-z^{-1}}$$

Suppose that the delta-sigma modulator has a unity feedback gain, $H(z) = 1$. Using Eq. 6.1, the signal transfer function (STF) of this modulator is

$$\begin{aligned} STF = \frac{Y(z)}{X(z)} &= \frac{G(z)}{1+G(z)H(z)} \\ &= \frac{\frac{gz^{-1}}{1-z^{-1}}}{1+\left(\frac{gz^{-1}}{1-z^{-1}}\right)(1)} \\ &= \frac{gz^{-1}}{1-z^{-1}+gz^{-1}} \\ &= z^{-1} \text{ for } g = 1, \end{aligned} \tag{6.4}$$

which is a unit delay. The noise transfer function (NTF) is

$$\begin{aligned} NTF = \frac{Y(z)}{N(z)} &= \frac{1}{1+G(z)H(z)} \\ &= \frac{1}{1+\left(\frac{gz^{-1}}{1-z^{-1}}\right)(1)} \\ &= \frac{1-z^{-1}}{1-z^{-1}+gz^{-1}} \\ &= 1-z^{-1} \text{ for } g=1, \end{aligned} \tag{6.5}$$

which is a discrete-time differentiator. The transfer function to input-refer the noise is

$$\begin{aligned} \frac{X(z)}{N(z)} &= \frac{NTF}{STF} \\ &= \frac{1}{G(z)} \\ &= \frac{1-z^{-1}}{gz^{-1}} \\ &= \frac{z-1}{g} \end{aligned} \tag{6.6}$$

We find the frequency domain equivalent of Eq. 6.6 by substituting $z = e^{j\omega T} = e^{j2\pi f/f_s}$, where $T = 1/f_s$ is the sampling period.

$$\begin{aligned} \frac{X(z)}{N(z)} &= \frac{e^{j2\pi f/f_s}-1}{g} \\ &= \left(\frac{e^{j\pi f/f_s}-e^{-j\pi f/f_s}}{2j}\right)\left(\frac{2j\,e^{j\pi f/f_s}}{g}\right) \\ &= \sin\left(\frac{\pi f}{f_s}\right)\left(\frac{2j\,e^{j\pi f/f_s}}{g}\right). \end{aligned}$$

The magnitude of this input-referred noise transfer function is

$$\left|\frac{X(z)}{N(z)}\right| = \left|\sin\left(\frac{\pi f}{f_s}\right)\left(\frac{2j\,e^{j\pi f/f_s}}{g}\right)\right| \tag{6.7}$$

$$= \frac{2}{g}\sin\left(\frac{\pi f}{f_s}\right) \tag{6.8}$$

Note that this magnitude is a high-pass function[1], equal to 0 for $f = 0$ and increasing monotonically as f goes to $f_s/2$. To understand this result in more detail, we examine the case of noise, $N(z)$, which is white (constant across all frequencies) with power spectral density S_N. Suppose the modulator oversamples the input signal, such that $f_s = (2f_B)\,\mathrm{OSR}$, where f_B is the signal bandwidth, and OSR is the oversampling ratio, that is, the ratio of the sampling frequency to the Nyquist sampling rate for the particular signal bandwidth. The input-referred noise which falls into the signal band[2] is[3]

$$\begin{aligned}
\overline{v_{in,N}^2} &= \int_0^{f_B} S_N \left|\frac{X(z)}{N(z)}\right|^2 df \\
&= \int_0^{f_B} S_N \left[\frac{2}{g}\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \\
&= \frac{S_N}{g^2}\left[2f_B - \left(\frac{f_s}{\pi}\right)\sin\left(\frac{2\pi f_B}{f_s}\right)\right] \\
&= \frac{S_N}{g^2}\left[\frac{fs}{\mathrm{OSR}} - \left(\frac{f_s}{\pi}\right)\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\right].
\end{aligned} \tag{6.9}$$

For OSR = 1 (no oversampling), Eq. 6.9 evaluates to

$$\begin{aligned}
\overline{v_{in,N}^2} &= \frac{S_N}{g^2}\left[\frac{fs}{1} - \left(\frac{f_s}{\pi}\right)\sin\left(\frac{\pi}{1}\right)\right] \\
&= \frac{S_N f_s}{g^2}
\end{aligned} \tag{6.10}$$

For OSR $>> \pi$, Eq. 6.9 simplifies using a Taylor series approximation to

$$\begin{aligned}
\overline{v_{in,N}^2} &= \frac{S_N}{g^2}\left[\frac{fs}{\mathrm{OSR}} - \left(\frac{f_s}{\pi}\right)\left(\frac{\pi}{\mathrm{OSR}} - \frac{\pi^3}{3!\,\mathrm{OSR}^3}\right)\right] \\
&= \frac{S_N}{g^2}\left(\frac{f_s}{\mathrm{OSR}} - \frac{f_s}{\mathrm{OSR}} + \frac{f_s\pi^2}{6\,\mathrm{OSR}^3}\right) \\
&= \frac{S_N}{g^2}\left(\frac{f_s\,\pi^2}{6\,\mathrm{OSR}^3}\right).
\end{aligned} \tag{6.11}$$

[1]Intuitively, this high-pass function is the reciprocal of the integrator transfer function, which is a low-pass function that is infinite at $f = 0$ and decreases monotonically as f goes to $f_s/2$.

[2]We only care about noise that falls into the signal band. Out-of-band noise will be removed using a low-pass decimation filter.

[3]For in-depth details of this derivation, see App. A.

Eq. 6.11 represents the equivalent noise at the input of the integrator which has the same effect on the output of the delta-sigma modulator as a white noise source of power spectral density S_N at the output of the integrator.

By comparing the result of Eq. 6.11 for large OSR with the result of Eq. 6.10 for no oversampling, it can be seen that the effect of oversampling with first-order noise-shaping is an attenuation of the input-referred noise of

$$\frac{\frac{S_N}{g^2}\left(\frac{f_s \pi^2}{6\,\mathrm{OSR}^3}\right)}{\frac{S_N f_s}{g^2}} = \frac{\pi^2}{6\,\mathrm{OSR}^3}. \tag{6.12}$$

In decibels, this is

$$\begin{aligned} & 10log_{10}\pi^2 - 10log_{10}6 - 10log_{10}\mathrm{OSR}^3 \\ = \; & 9.9dB - 7.8dB - 30log_{10}\mathrm{OSR} \\ = \; & 2.1dB - 30log_{10}\mathrm{OSR} \\ = \; & 2.1dB - \left(\frac{30}{log_{10}2}\right) log_2\mathrm{OSR} \\ = \; & 2.1dB - 9dB\, log_2\mathrm{OSR}, \end{aligned} \tag{6.13}$$

which represents an attenuation of 9 dB (1.5 bits) per doubling of the OSR with first-order noise-shaping. The reason for this attenuation of input-referred quantization noise is that, in the signal band, the modulator is much more sensitive to signals added at the input, $X(z)$, than to signals added at the output, $N(z)$, due to the discrete-time integration that occurs between the input and output.

6.2.2 Effect of Finite Opamp Gain on Integrator

Sec. 4.1.2 discusses the effects of finite opamp gain on the switched-capacitor integrator of Fig. 4-1. Continuing the analysis using discrete-time notation[4], Eq. 4.4

[4]The discrete-time notation used here assumes that each time period consists of two consecutive phases, ϕ_1 and ϕ_2, each of which spans half the period. However, the conclusions in this analysis also apply to systems where ϕ_1 and ϕ_2 are not equal in duration.

becomes:

$$V_{out}[n] = V_X[n] + V_{CFB}[n].$$

Substituting Eq. 4.3 to write V_X in terms of V_{out} and using the definition of capacitance (C = Q/V), we solve for V_{out} in terms of q_{CFB}:

$$\begin{aligned} V_{out}[n] &= \left(V_{CM} - \frac{V_{out}[n]}{A}\right) + \frac{q_{CFB}[n]}{C_{FB}} \\ V_{out}[n]\left(1+\frac{1}{A}\right) &= V_{CM} + \frac{q_{CFB}[n]}{C_{FB}} \\ V_{out}[n] &= \frac{V_{CM} + \frac{q_{CFB}[n]}{C_{FB}}}{\left(1+\frac{1}{A}\right)} = \left(\frac{A}{A+1}\right)\left(V_{CM} + \frac{q_{CFB}[n]}{C_{FB}}\right). \end{aligned} \quad (6.14)$$

Note that Eq. 6.14 shows a gain discrepancy between the charge integrated on capacitor C_{FB} and the voltage at V_{out}. We substitute Eq. 6.14 into 4.6 to find the charge on C_{FB} as a function of V_{in}:

$$\begin{aligned} q_{CFB}[n] - q_{CFB}[n-1] &= C_{IN}\left(V_{in}[n-1] - V_{REF}\left[n-\frac{1}{2}\right] - \frac{V_{out}[n]}{A}\right) \\ &= C_{IN}\left[V_{in}[n-1] - V_{REF}\left[n-\frac{1}{2}\right] - \left(\frac{1}{A+1}\right)\left(V_{CM} + \frac{q_{CFB}[n]}{C_{FB}}\right)\right] \\ &\updownarrow \mathcal{Z} \\ Q_{CFB}(z) - Q_{CFB}(z)z^{-1} &= C_{IN}\left[V_{in}(z)z^{-1} - V_{REF}(z)z^{-0.5} - \left(\frac{1}{A+1}\right)\left(V_{CM} + \frac{Q_{CFB}(z)}{C_{FB}}\right)\right] \end{aligned}$$

$$\begin{aligned} Q_{CFB}(z)\left(1 - z^{-1} + \frac{C_{IN}}{(A+1)C_{FB}}\right) &= C_{IN}\left[V_{in}(z)z^{-1} - V_{REF}(z)z^{-0.5} - V_{CM}\left(\frac{1}{A+1}\right)\right] \\ Q_{CFB}(z) &= \frac{C_{IN}\left[V_{in}(z)z^{-1} - V_{REF}(z)z^{-0.5} - V_{CM}\left(\frac{1}{A+1}\right)\right]}{1 - z^{-1} + \frac{C_{IN}}{(A+1)C_{FB}}}. \end{aligned}$$

Assuming $V_{CM} = 0$ and solving for the voltage across C_{FB}:

$$\begin{aligned} V_{CFB}(z) &= \frac{Q_{CFB}(z)}{C_{FB}} \\ &= \frac{C_{IN}}{C_{FB}} \frac{V_{in}(z)z^{-1} - V_{REF}(z)z^{-0.5}}{1 - z^{-1} + \frac{C_{IN}}{(A+1)C_{FB}}}. \end{aligned} \quad (6.15)$$

The remainder of this analysis assumes that $V_{REF} = 0$. A nonzero value for V_{REF} would act as an input-referred offset.

Because Fig. 4-1 is a non-inverting full-delay integrator, it corresponds to Fig. 6-4(c), with $x[n] = V_{in}[n]$, $y[n-1] = V_{CFB}[n]$, and $y[n] = V_{CFB}[n+1]$. We solve for the transfer function $\frac{Y(z)}{X(z)}$ by substituting these relationships into Eq. 6.15:

$$\begin{aligned}
\frac{Y(z)}{X(z)} &= \frac{V_{CFB}(z)z}{V_{in}(z)} \\
&= \frac{C_{IN}}{C_{FB}} \frac{z^{-1}z}{1 - z^{-1} + \frac{C_{IN}}{(A+1)C_{FB}}} \\
&= \frac{C_{IN}}{C_{FB}} \frac{1}{1 - z^{-1} + \frac{C_{IN}}{(A+1)C_{FB}}}
\end{aligned} \tag{6.16}$$

Note that the value of the transfer function at DC (z=1) is no longer infinite, but instead is

$$\begin{aligned}
\frac{Y(1)}{X(1)} &= \frac{C_{IN}}{C_{FB}} \frac{1}{1 - 1^{-1} + \frac{C_{IN}}{(A+1)C_{FB}}} \\
&= \frac{C_{IN}}{C_{FB}} \frac{(A+1)C_{FB}}{C_{IN}} \\
&= A + 1.
\end{aligned} \tag{6.17}$$

Because the DC gain[5] is no longer infinite, the integrator is considered to be "leaky" or "lossy".

To solve for the pole of the transfer function in Eq. 6.16, we rearrange it as follows:

$$\frac{Y(z)}{X(z)} = \frac{C_{IN}}{C_{FB}} \frac{1}{\frac{A+1+\frac{C_{IN}}{C_{FB}}}{A+1} - z^{-1}}.$$

[5]Not to be confused with the gain coefficient, g, in the transfer function of the generic integrator of Fig. 6-4.

We then multiply the numerator and denominator by $\frac{A+1}{A+1+\frac{C_{IN}}{C_{FB}}}$ to get:

$$\begin{aligned}\frac{Y(z)}{X(z)} &= \frac{C_{IN}}{C_{FB}} \frac{\frac{A+1}{A+1+\frac{C_{IN}}{C_{FB}}}}{1 - z^{-1}\frac{A+1}{A+1+\frac{C_{IN}}{C_{FB}}}} \\ &= \frac{C_{IN}}{C_{FB}} \frac{p}{1 - pz^{-1}}, \end{aligned} \tag{6.18}$$

where p is the pole of transfer function $\frac{Y(z)}{X(z)}$:

$$p = \frac{A+1}{A+1+\frac{C_{IN}}{C_{FB}}}. \tag{6.19}$$

We can see that finite opamp gain, A, causes the pole, p, to move away from z=1 (DC) and inside the unit circle. We can also see that if A is finite, then in the numerator of Eq. 6.18, $p \neq 1$, and the integrator has a gain error.

In summary, finite opamp gain has the following effects on the transfer function of a switched-cacitor integrator: 1) causes a gain discrepancy between the output voltage of the integrator and the voltage across the integration capacitor, 2) moves the pole in the transfer function away from the unit circle, which causes finite DC gain, and 3) causes an error in integrator gain[6].

6.2.3 Effect of Crossing Detector Delay on Integrator

The analysis of the pole, p, of the integrator transfer function, $\frac{Y(z)}{X(z)}$, for the case of a ZCB integrator is analogous to that of a SC integrator. Using Table 5.1 to substitute into Eq. 6.17 and Eq. 6.19, we find the DC gain and pole values for the ZCB integrators. The results are shown in Table 6.1. Because the frequency response of an integrator decreases with increasing frequency, the gain at DC for an integrator is also its maximum gain. Note that, because the DC gain depends on r_o for the constant delay and ideal integrator cases, DC gain can be increased (or the same DC gain can be realized with longer crossing detector delay, t_{delay}) using the correlated

[6]Similar but different solutions for Eq. 6.19 can be found in [26], [27]. A simplified solution is found in [21]

Table 6.1: Integrator DC Gain & Pole

topology	DC gain	pole location in z-plane
switched-capacitor	$A+1$ A = finite opamp gain	$\frac{A+1}{A+1+\frac{C_{IN}}{C_{FB}}}$
ZCB, constant delay	$\frac{r_o C_{IN}}{t_{\text{delay}}}+1$	$\frac{\frac{r_o C_{IN}}{t_{\text{delay}}}+1}{\frac{r_o C_{IN}}{t_{\text{delay}}}+1+\frac{C_{IN}}{C_{FB}}}$
ZCB, ideal integrator	$r_o\sqrt{\frac{2I_{fine0}C_{IN}G_m}{V_M C_i}}+1$	$\frac{r_o\sqrt{\frac{2I_{fine0}C_{IN}G_m}{V_M C_i}}+1}{r_o\sqrt{\frac{2I_{fine0}C_{IN}G_m}{V_M C_i}}+1+\frac{C_{IN}}{C_{FB}}}$
ZCB, steady-state	inf	1

level-shifting technique presented in Sec. 5.4.3.

6.3 Modulator System Diagram

Fig. 6-5 represents a 4th-order chain-of-integrators[7] feedforward delta-sigma modulator [21]. To simplify the design, quantization noise is attenuated in the signal

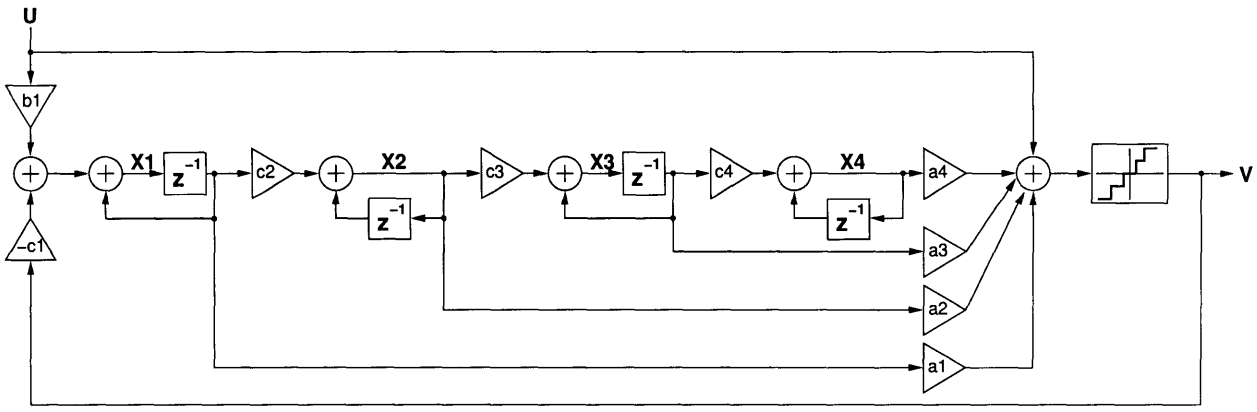


Figure 6-5: Conventional 4th-order chain-of-resonators feedforward (CRFF) delta-sigma modulator [21] (local feedback coefficients set to zero) implemented with a combination of delay-free and full-cycle delay integrators.

band using only DC (z=1) loop-filter poles. Thus local feedback between pairs of

[7]In [21], this topology is categorized as a "chain-of-resonators, feedforward" (CRFF). In the complete topology, local feedback loops between pairs of integrators (not shown in Fig. 6-5) move the loop-filter poles / NTF zeros to resonance frequencies, resulting in a flatter quantization noise floor in the signal-band.

integrators is not required.

The input to the quantizer is a weighted sum of the input signal and the outputs from each of the four integrators. The quantizer provides negative feedback to the first integrator only.

The advantage of the feedforward topology is that as the modulator goes unstable, saturating the outputs of later integrators, the loop filter gracefully degrades [28] to a lower order until it reacquires a stable state. For example, if the output of the fourth integrator saturates, the input to the quantizer becomes a weighted sum of the input signal, the first three integrator outputs, and a constant from the fourth integrator. Effectively, the modulator has become third order. This degradation to lower orders occurs until a stable state is reacquired.

Another advantage of choosing a feedforward modulator topology, as compared to a feedback topology (where the DAC output is subtracted from the input of each integrator) is that the integrators of a feedforward modulator only process the quantization noise and not the full input signal [29][30]. Because the inputs to the integrators become independent of the input to the modulator, the performance requirements for the integrators are reduced.

Comparing Fig. 6-5 with Fig. 6-3, we see that the loop filter of the delta-sigma modulator has been implemented with a chain (cascade) of integrators (Fig. 6-4). The basic conclusions stated in Sec. 6.1.2 assume that the gain of the loop filter is high in the signal band. However, as expressed in Table 6.1, the DC gain (and equivalently, the maximum gain) of the integrators is decreased by finite opamp gain (for switched-capacitor integrators) or finite gated current source output impedance (for ZCB integrators). Thus, the importance of high DC gain (and therefore high opamp gain / gated current source output impedance) for the integrators in the loop filter becomes clear.

Fig. 6-6 represents the same system diagram implemented with half-cycle delay integrators, as originally demonstrated for switched-opamp circuits in [19].

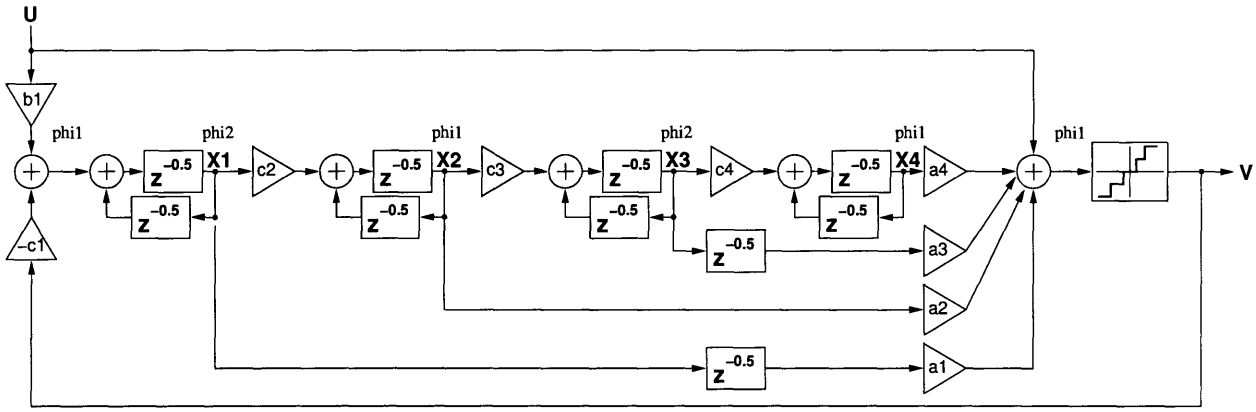


Figure 6-6: 4th-order CRFF delta-sigma modulator implemented with half-delay integrators. Signals are available at end of indicated clock phase.

Chapter 7

Test Chip

This chapter documents the design, fabrication, and test of a 4th-order single-bit delta-sigma ADC which uses LV-ZCB integrators to implement the loop filter.

Because the ADC is intended for audio applications, a signal bandwidth of at least 20 kHz is desired. Also, for comparison to other published low-voltage audio ADCs (such as [7] which achieves a peak SNDR of 82 dB, and [31] which achieves a peak SNDR of 81 dB), a 14-bit ENOB is desired.

7.1 Modulator Design

7.1.1 Loop Filter Coefficients

Fig. 7-1 represents the actual implemented delta-sigma modulator, which has a system function identical to that of the modulators in Fig. 6-5 and Fig. 6-6. Nodes "X1", "X2", "X3", and "X4" represent the outputs of integrators 1-4, respectively.

The difference between Fig. 7-1 and Fig. 6-6 comes from the desire to use the resistor-switch ladder (a.k.a. 1-bit DAC, Sec. 5.2.1) of the first integrator to sample the input signal both for the first integrator and for the modulator's summing node simultaneously. The purpose of reusing this circuitry is to avoid the extra power that would be required for a second resistor-switch ladder for the summing node. However, as a trade-off of sharing one resistor-switch ladder to sample the input signal for both

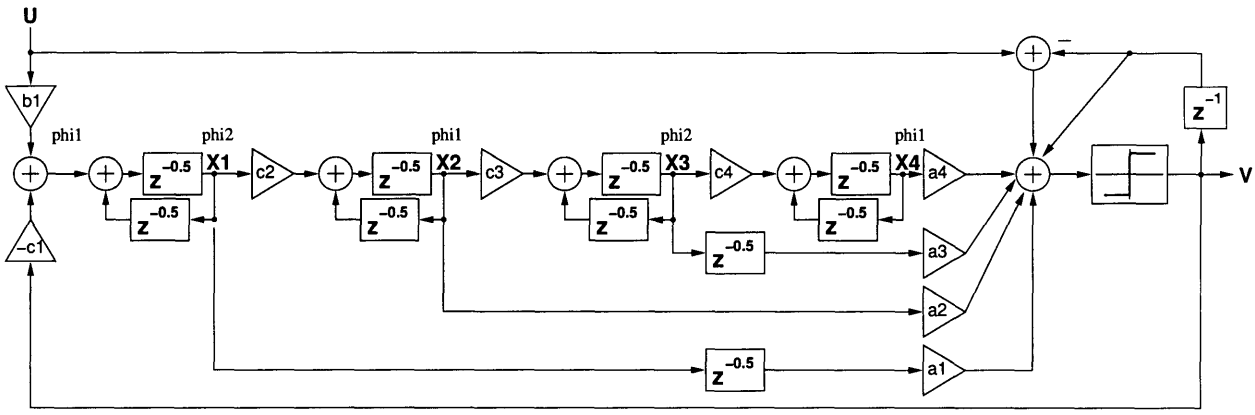


Figure 7-1: 4th-order CRFF delta-sigma modulator as implemented. Nodes "X1", "X2", "X3", and "X4" represent the outputs of integrators 1-4, respectively.

functions, the signal from the DAC which provides feedback to the first integrator has to be canceled at the summing node (see Sec. 7.1.4). Also, a danger is that kickback from the quantizer and capacitive coupling from the other summed signals could add noise to the input of the modulator. Thus, using separate resistor-switch ladders to sample the input signal for the first integrator and for the summing node is recommended for a future implementation.

The modulator coefficients of Table 7.1 were determined using Richard Schreier's Delta-Sigma Toolbox for Matlab [32][1].

Table 7.1: 4th-Order CRFF Delta-Sigma Modulator Coefficients

Coefficient	Calculated	Implemented	Purpose
a1	0.8233	5/6 = 0.8333	Weighted sum integrator 1
a2	1.0222	13/12 = 1.0833	Weighted sum integrator 2
a3	0.7804	3/4 = 0.7500	Weighted sum integrator 3
a4	0.6881	2/3 = 0.6667	Weighted sum integrator 4
b1	0.3711	1/2.7 = 0.3704	Input gain
c1	0.3711	1/2.7 = 0.3704	Integrator 1 gain
c2	0.1545	1/7 = 0.1429	Integrator 2 gain
c3	0.1325	1/7 = 0.1429	Integrator 3 gain
c4	0.0604	1/16 = 0.0625	Integrator 4 gain

[1]In determining the proper coefficients, the infinity-norm, the maximum gain of the NTF over all frequencies, was $||H_\infty|| = 1.2$. For coefficient scaling, each integrator output was limited to a magnitude of xlim = 0.9.

A pole-zero plot of the implemented NTF (assuming an effective quantizer gain of 1) is shown in Fig. 7-2. Note that all NTF zeros (loop-filter poles) are at DC (z=1).

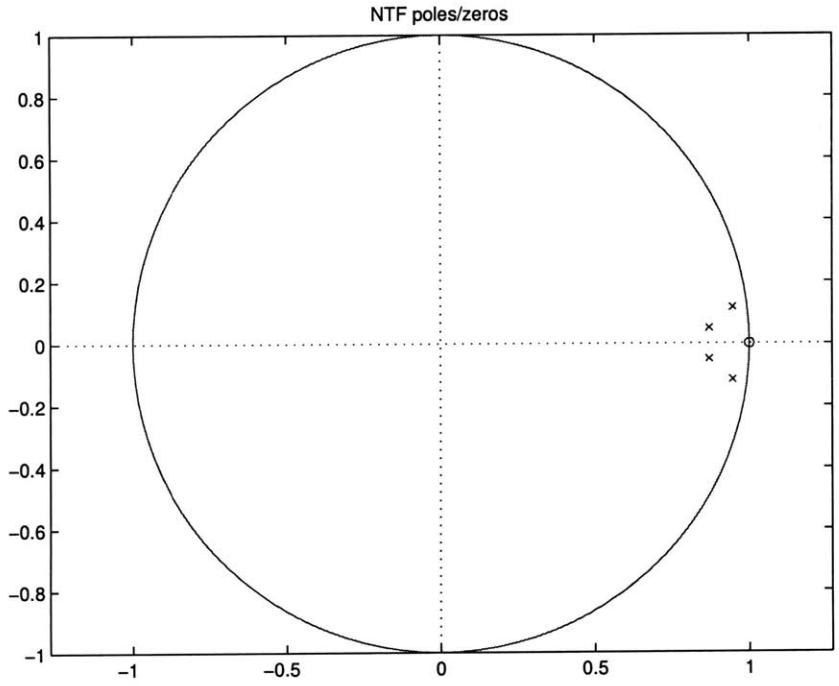


Figure 7-2: Plot of NTF/STF poles and NTF zeros for implemented 4th-order CRFF delta-sigma modulator.

7.1.2 Oversampling Ratio

A chart of peak SNR versus OSR for the ideal modulator as simulated in Matlab is shown in Fig. 7-3. Note that the SNR increases with OSR. For 14-bit (SNDR = 86 dB) accuracy, signal-to-quantization-noise ratio must be better than 86 dB, which is achieved for OSR = 128 or higher. For a conservative design, the chip was designed to achieve a higher oversampling ratio, OSR = 256. Fig. 7-4 shows an FFT of the ideal modulator's response to a sinusoidal input, as simulated in Simulink with a 1-bit quantizer.

An issue with high OSR is that data must be taken from a larger number of discrete cycles to get sufficient resolution in the signal band of an FFT, leading to a

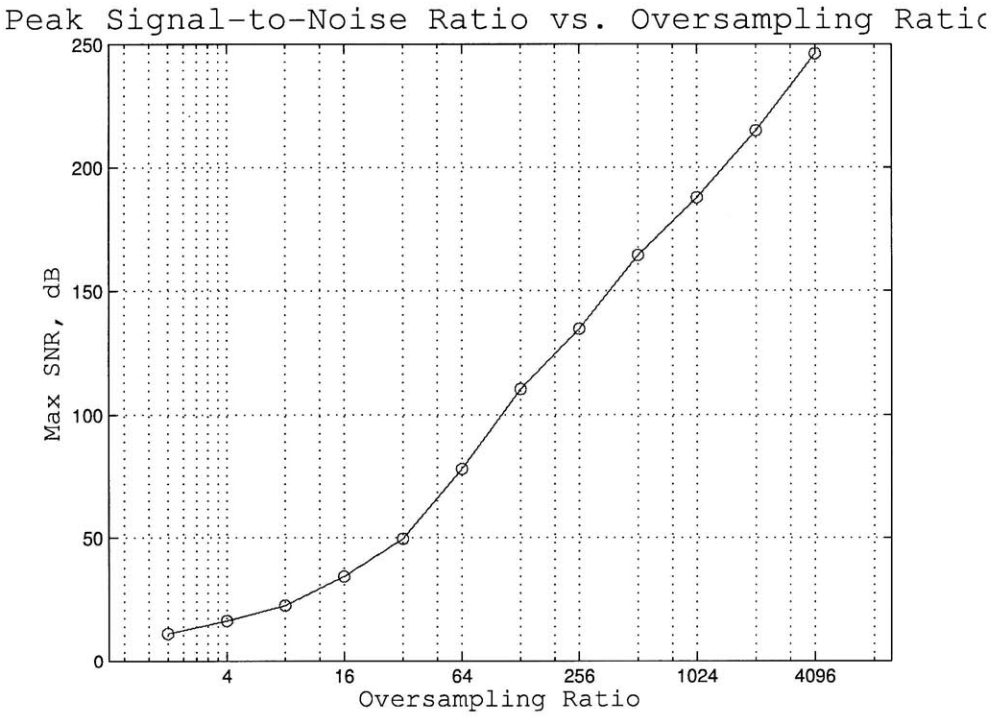


Figure 7-3: Peak SNR vs. OSR as simulated in Matlab for the modulator coefficients of Table 7.1.

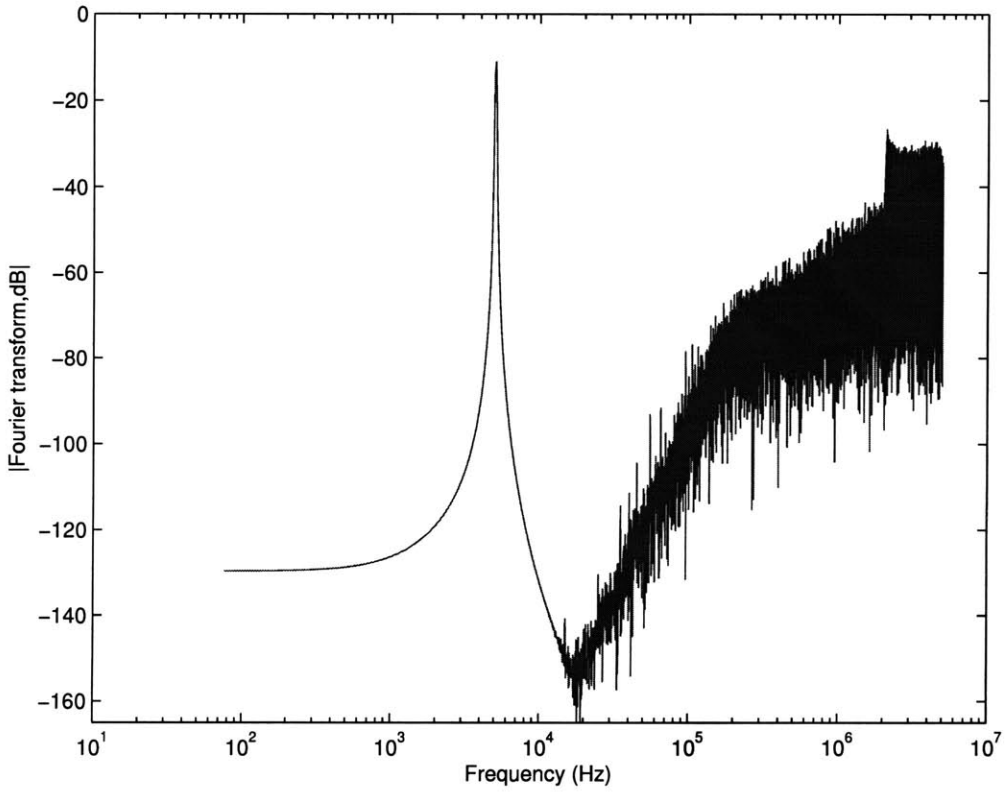


Figure 7-4: Ideal FFT of implemented modulator, simulated using MATLAB Simulink, for input of $\pm$ 800 mV differential at 5 kHz, $N = 2^{17}$ points. Hann window.

longer required simulation time. This can be a problem when the ADC is simulated at the transistor level.

Another disadvantage of a high OSR is that it increases the DC gain requirement for the integrators. The theoretical requirement for DC gain is explained in [21]:

> Linear analysis indicates that the attenuation offered by the NTF begins to degrade if its zero moves inside the unit circle by about π/OSR. Since finite op-amp gain shifts the pole of the first integrator by $C_{IN}/(A\,C_{FB})$, one might be tempted to conclude that $A = (OSR\,C_{IN})/(\pi\,C_{FB})$ would be adequate. However, this linear analysis neglects the nonlinear errors which result from slewing and nonlinear DC gain.

A rule-of-thumb presented by [33] and reiterated by [21] suggests that each integrator in a delta-sigma modulator should have a DC gain of at least OSR to maintain less than 0.2 dB drop in SNR compared to the same modulator built with infinite DC gain integrators. Simulation data from [26] shows that a 3rd-order modulator with OSR = 64 will experience a 3dB drop in SNR for integrators with an average DC gain of 43.

As an example, according to Table 6.1, for a ZCB integrator to achieve a DC gain of OSR = 256 with a sampling capacitor, C_{IN} = 1 pF, and a fine crossing detector delay of $t_{delay,fine}$ = 4 ns, the output impedance of the gated current source for the fine charge-transfer would have to be

$$\begin{aligned} OSR &= \frac{r_{o,fine}\,C_{IN}}{t_{delay,fine}} \\ r_{o,fine} &= \frac{OSR\,t_{delay,fine}}{C_{IN}} \\ &= \frac{(256)(4\text{ ns})}{1\text{ pF}} \\ &= 1\text{ M}\Omega. \end{aligned}$$

However, using the correlated level-shifting technique described in Sec. 5.4.3 with a level-shifting capacitor C_{CLS} = 1.75 pF and a coarse crossing detector delay of $t_{delay,coarse}$ = 0.8 ns, the gated current sources for the coarse and fine charge transfers

only need to have output impedances of

$$\begin{aligned} OSR &= \left(\frac{r_{o,coarse}\, C_{CLS}}{t_{delay,coarse}}\right)\left(\frac{r_{o,fine}\, C_{IN}}{t_{delay,fine}}\right) \\ r_{o,coarse} * r_{o,fine} &= \frac{OSR\, t_{delay,coarse}\, t_{delay,fine}}{C_{CLS}\, C_{IN}} \\ &= \frac{(256)(0.8 \text{ ns})(4 \text{ ns})}{(1.75 \text{ pF})(1 \text{ pF})} \\ &= 4.7 \text{ x } 10^8\ \Omega^2, \end{aligned}$$

which is met if the current sources have a geometric mean output impedance of $\sqrt{4.7 \text{ x } 10^8} = 21.6\ \text{k}\Omega$.

7.1.3 Modulator Stability & 1-Bit Quantizer

Fig. 7-5 shows the root locus of the NTF for the implemented 4th-order CRFF delta-sigma modulator, plotting the pole locations on the Z-plane as a function of the closed-loop gain. For large gain, the poles are inside the unit circle, indicating stability. The root locus shows that the poles move outside of the unit circle for small values of closed-loop gain, and so the modulator is conditionally stable, which is the norm for single-loop single-bit delta-sigma modulators of order higher than two.

Because the integrator gain coefficients are constant, the closed-loop gain is proportional to the quantizer gain. In the implemented delta-sigma ADC, a single-bit quantizer was chosen for linearity. If the quantizer is single-bit, and therefore has a constant magnitude at the output, its effective gain is inversely proportional to the magnitude of its input. Thus, the input to the quantizer must remain small to maintain stability.

A schematic of the implemented quantizer is shown in Fig. 7-6. This clocked comparator implementation is identical to the current-controlled latch sense amplifier of [34]. In this topology, the differential outputs are both precharged to V_{DD}. When the clock signal ("latch") rises, the positive feedback of two cross-coupled inverters causes one output to stay high and the other output to go low. The speed of each inverter, and hence the latched state, is determined by current set by V_{inp} and V_{inn},

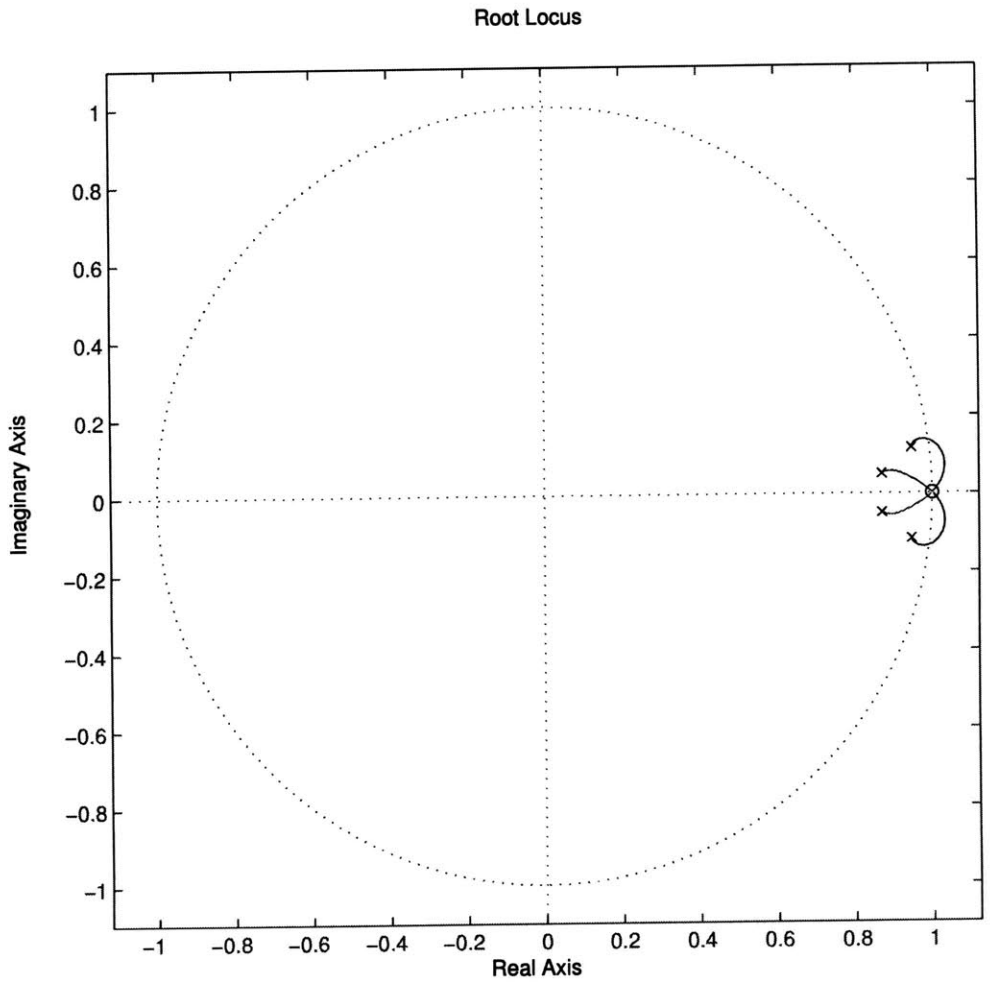


Figure 7-5: Root locus showing NTF/STF poles of implemented 4th-order CRFF delta-sigma modulator for effective quantizer gain, $k \leq 1$. Poles move toward NTF zeros as k decreases to 0.

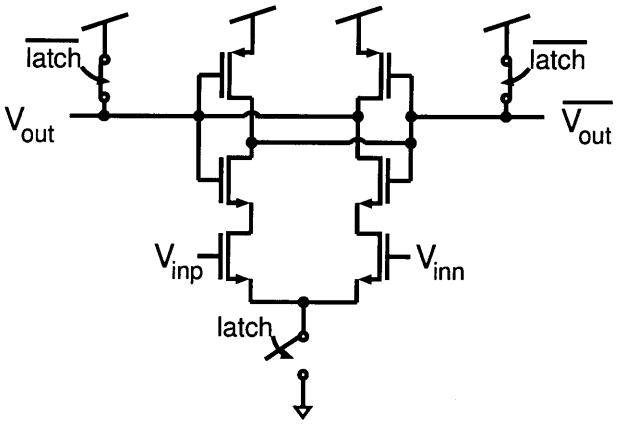


Figure 7-6: 1-bit quantizer.

respectively.

7.1.4 Summing Node

The signal that the quantizer evaluates is a weighted sum of the signals at the input of the modulator and the outputs of the integrators. Because of the timing of the signals to be summed, and the speed with which summing and quantizing must be accomplished, special attention must be paid to the coordination of this operation.

Challenges of Summing

Consider the modulator diagram of Fig. 7-1. Note that while integrators 1 & 3 are in their sampling phase, integrators 2 & 4 are in their charge-transfer phase, and vice-versa. Thus, a method is needed to delay the output signals from integrators 1 & 3 by a half-cycle before summing[2]. Although it would be possible to accomplish this delay using a unity-gain LV-ZCB buffer, such a solution would require extra power to bias the extra buffer stages. Another complication is that, because each integrator's charge-transfer is controlled asynchronously, even integrators that share the same clock phases, such as integrators 2 & 4, have outputs that are valid at

[2]The switched-opamp delta-sigma ADCs of [19], [35], [36], and [37] all use feedback modulator topologies, possibly to avoid summing multiple integrator outputs, as is required in a feedforward modulator. For a feedback topology, the half-cycle delay can be done in the digital domain.

different times[3].

Another point to note in the modulator of Fig. 7-1, is that the path from the output of integrator 2 (or 4), through the summing node and the quantizer, through the feedback path (DAC) towards the input of the modulator, and through integrator 1 only contains a half-cycle delay. Thus, after integrators 2 & 4 finish their charge-transfer phase, their outputs (through the quantizer and feedback DAC) must affect the charge-transfer of integrator 1 a half-cycle later. Because the output of a ZCB circuit does not settle like an opamp-based circuit, the input reference for a ZCB circuit (V_{DAC} and V_{DACb} in the differential LV-ZCB integrator of Fig. 5-8) must settle completely before charge-transfer begins. Thus, the weighted sum of the integrator outputs, the 1-bit quantization, and the settling of the DAC voltage must all be completed during the first integrator's preset. The speed with which these operations must occur severely limits the topologies that can be used to implement them.

Summing Implementation

In the implemented modulator, the weighted sum is accomplished by capacitively coupling the differential input of integrator 1 and the differential outputs of integrators 1-4 to differential summing nodes, which are the same nodes as the inputs to the 1-bit quantizer of Fig. 7-6. The sizes of the coupling capacitors are weighted according to coefficients a1-a4 of Table 7.1. As explained in Sec. 7.1.1, the input of integrator 1 contains a signal from the DAC which is not a desired component in the weighted sum. Thus, the inverse of the DAC voltage is also coupled to the summing nodes to cancel the unwanted term. This method for summing the integrator outputs is illustrated in Fig. 7-7. A related graph of signals is shown in Fig. 7-8.

As mentioned above, summation occurs a half clock cycle after the charge-transfer phases of integrators 1 & 3. To implement the half-cycle delay without requiring extra LV-ZCB stages, the outputs of integrators 1 & 3 are coupled to the summation nodes during the transition from the end of their charge-transfer phase through their next

[3]The ZCB delta-sigma modulator of [8] is limited to 2nd-order, thus avoiding the problem of summing asynchronous signals that share a charge-transfer phase.

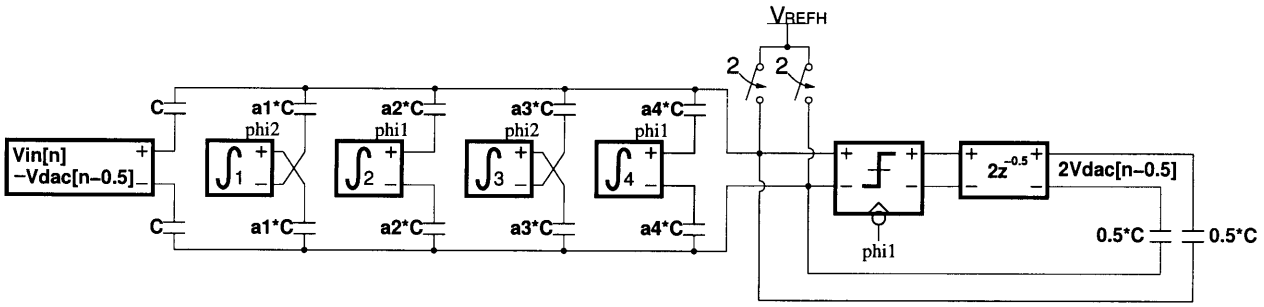


Figure 7-7: Connections for weighted sum of modulator input and integrator outputs at input of quantizer. For simplicity, capacitors for canceling DC offsets (see Sec. 4.2.2) are not shown. The sum is zeroed during ϕ_2, and quantized at the end of ϕ_1. Phase notation: ϕ_2 = "2".

sampling phase. As can be seen in Fig. 7-8, the change in V_{out} for an integrator during this transition is equal in magnitude but opposite in sign to the change in V_{out} during the previous charge-transfer phase, assuming that the preset is identical from cycle-to-cycle. The differential outputs of these integrators are crossed (inverted) before coupling to the summation nodes to create the proper signals for summing[4].

In Fig. 7-7, the effect of each integrator output, V_{outi}, where i=1, 2, 3 or 4, on the respective summing node (quantizer input) is

$$\Delta V = V_{outi} * \frac{a(i)C}{C_{sum}} \tag{7.1}$$

where a(i) is the weighting coefficient from Table 7.1 and $C_{sum} = C(1 + a1 + a2 + a3 + a4)$ is the total capacitance at the respective summing node.

The charge-transfer phase for each integrator finishes asynchronously; after an integrator completes its fine charge-transfer, the output nodes of the integrator are left floating when its sampling switches are opened. Thus, C_{sum} of Eq. 7.1 can vary slightly when the first integrator of each pair (1 or 3; 2 or 4) completes its fine charge transfer. However, the fine charge-transfer is longer in duration than the longest possible coarse charge-transfer; therefore no integrator can complete its fine charge-transfer before the paired integrator completes its coarse charge-transfer. Thus C_{sum}

[4]The implementation of a half-cycle delay by crossing the differential outputs of an integrator is shown for inverter-based integrators in [31].

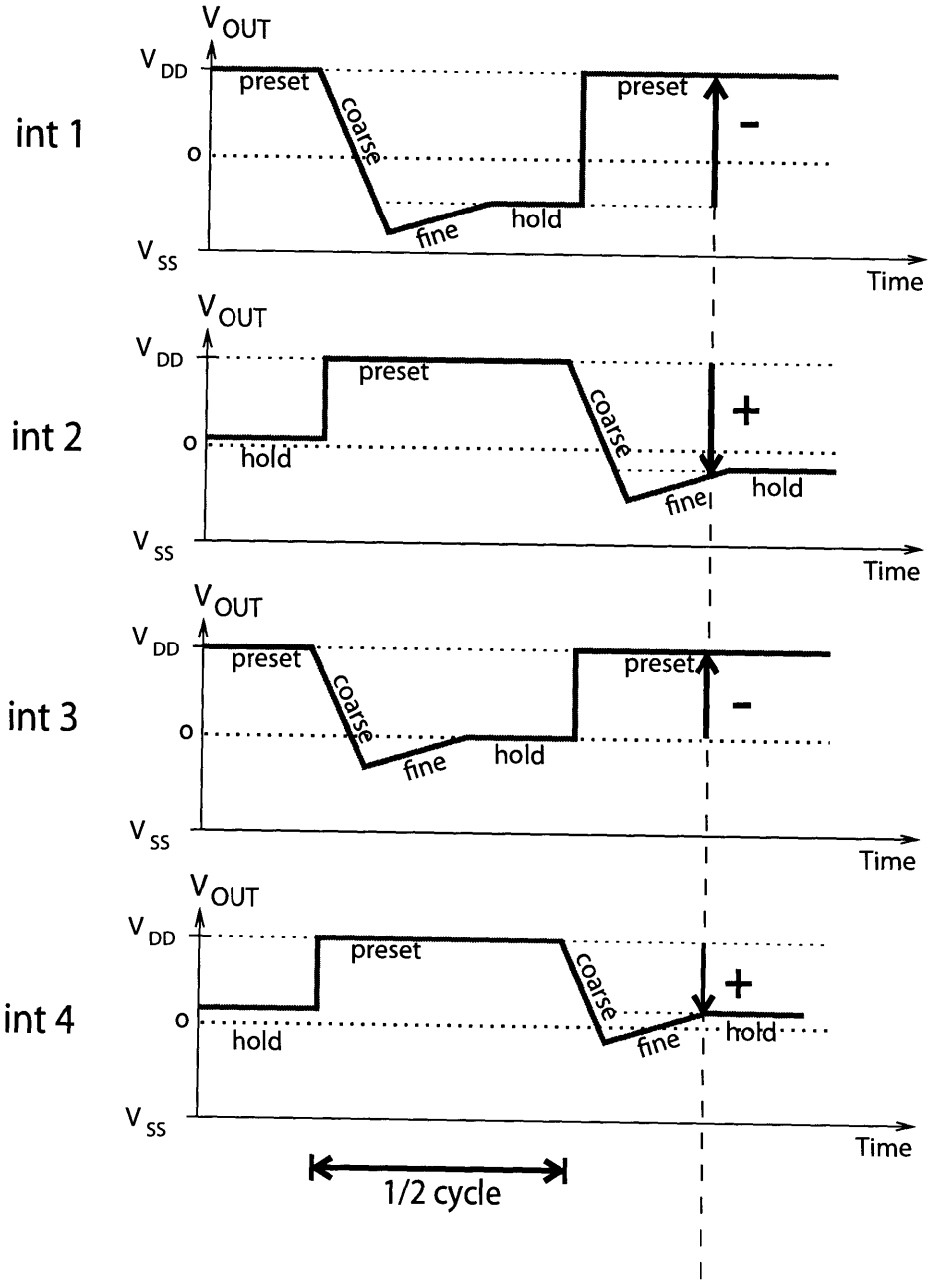


Figure 7-8: Graph demonstrating how signals which are half-cycle out-of-phase are summed.

is constant during each integrator's coarse charge-transfer. The weighted sum of these coarse values and partial fine values are good enough to achieve 1-bit accurate quantization.

Summation and Offset

The negative feedback of the modulator loop and the high DC gain of each integrator forces the effective mean of each integrator input to be zero[5]. If each integrator in the feedforward delta-sigma modulator of Fig. 7-1 has zero offset, then because the inputs to integrator stages 2-4 are simply the outputs of integrators 1-3, the means of these outputs must also be zero. The input to integrator 1 is the difference between the modulator input and the bitstream at the modulator output, thus this difference (quantization noise) must also have a mean of zero.

The main cause of offset in a LV-ZCB integrator stage is the delay of the crossing detector which causes overshoot at the integrator output, as summarized in Table 5.1. If an integrator has an input-referred offset, the mean output of the preceding integrator must cancel that offset. Thus, the means of the outputs of integrator 1-3 are constants that are determined by the input-referred offsets of integrators 2-4. The input-referred offset of integrator 1 becomes an offset at the input to the entire modulator.

As explained in Sec. 7.1.3, the input to the quantizer must remain small to maintain modulator stability. The input to the quantizer is the weighted sum of the modulator input and the outputs of integrators 1-4. Because the mean outputs of integrators 1-3 are set by the offsets of the subsequent integrators, the output of integrator 4 is the free variable that must roughly cancel the modulator input and the outputs of integrators 1-3 in the weighted sum. This requirement can increase the output signal swing of integrator 4.

Fig. 7-9 and Fig. 7-10 illustrate Simulink output for the modulator in response to a sinusoidal input. The integrators in this model have output overshoots of 1%

[5]Another way to think about it is that if the mean of an integrator input was not zero, then as time goes to infinity, the output of that integrator would saturate.

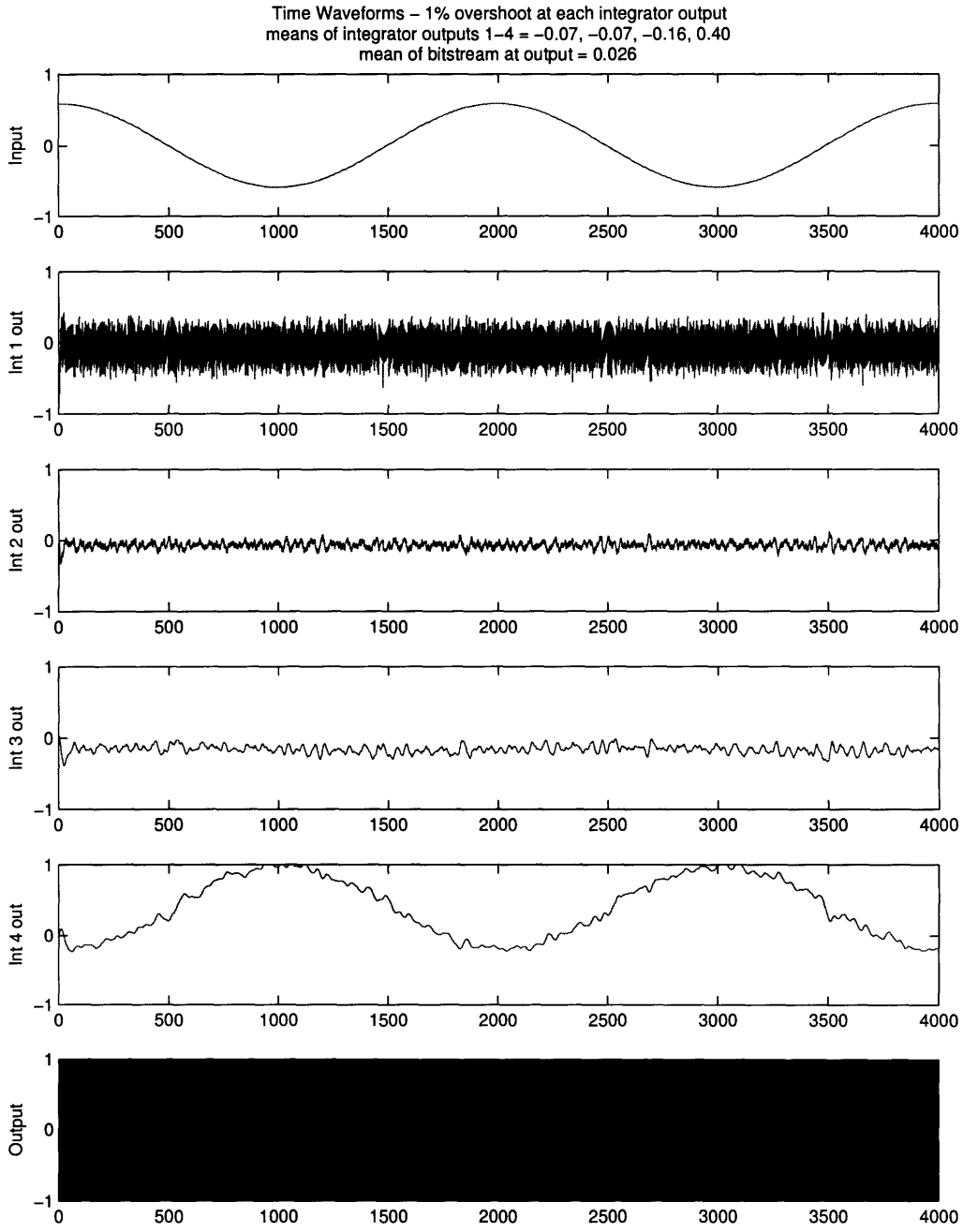


Figure 7-9: Sample modulator output from Simulink, first 4000 cycles. Overshoot at output = 1% of the full signal-swing.

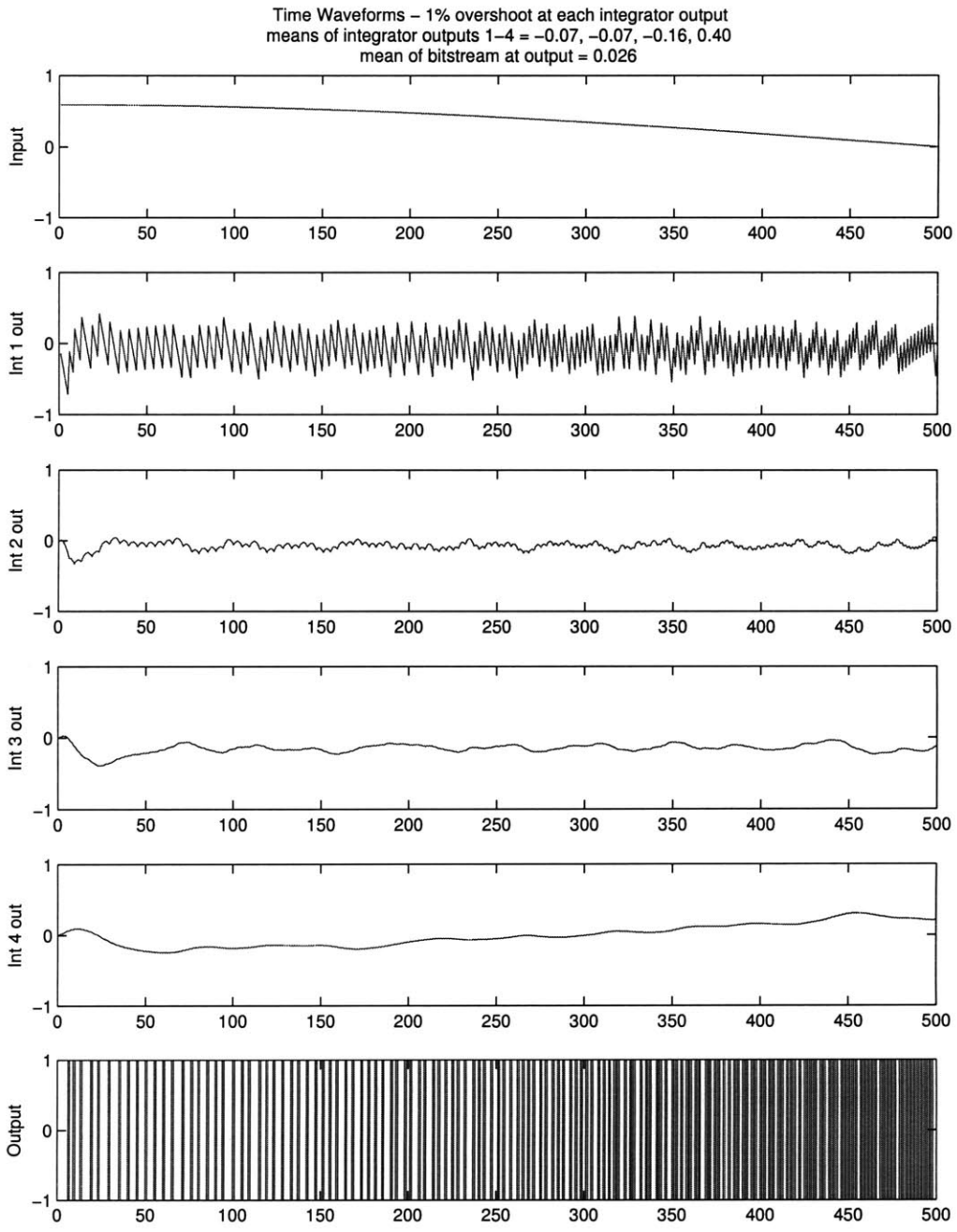


Figure 7-10: Sample modulator output from Simulink, first 500 cycles. Overshoot at output = 1% of the full signal-swing.

of the full signal-swing. Although the modulator coefficients were scaled to create a maximum 90% swing at each integrator output, Fig. 7-9 shows that offsets of the other integrator outputs push the output of integrator 4 close to saturation.

Because these offsets are not automatically accounted for by the delta-sigma toolbox [32], either a) the offsets must be kept small, or b) the signal swing at the output of integrator 4 must be adjusted by decreasing its gain. To keep the weighted sum the same, the decrease in integrator 4 gain must be accompanied by increasing the weighting of that signal in the sum. Alternatively, c) the offsets of integrators 2-4 can be cancelled by adjusting the reference voltages for the crossing detector offset capacitors (C_{OS} of Fig. 5-8). Another possible solution is that d) the charge-transfer ramps of some integrators can be done in opposite directions so that overshoots of some integrators cancel the overshoots of other integrators. The implemented circuit showed no saturation in integrator 4, most likely due to the unidirectional extension of signal swing which is a benefit of the correlated level-shifting technique (Sec. 5.4.3. However, it is recommended that a future design use a more robust solution such as the ones a)-d) mentioned above.

7.2 Differential Crossing Detector

7.2.1 Topology

The differential crossing detector of Fig. 7-11 consists of three cascaded stages: 1) a differential amplifier with resistive load (implemented using triode MOSFET) and binary-weighted capacitive load, 2) a differential-to-single-ended amplifier with active load, and 3) a dynamic crossing detector. The differential amplifier with resistive load is similar in design to the preamplifier of [22]. The differential-to-single-ended amplifier and dynamic crossing detector are similar to those used in [38].

The number of gain stages was chosen as a trade-off between crossing detector delay and power consumption for a given noise performance. This use of multiple gain stages highlights one of the advantages of the ZCB technique - extra stages can

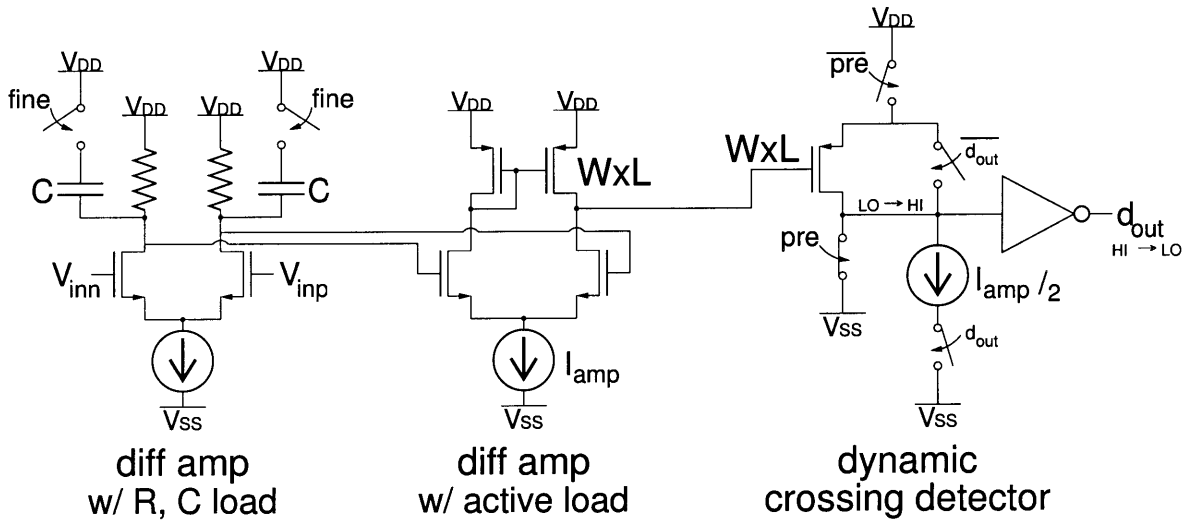


Figure 7-11: Differential crossing detector: differential amplifier, operational-transconductance amplifier, dynamic crossing detector.

be cascaded without the concern of destabilizing a feedback loop.

The differential amplifier with resistive load (stage 1) was chosen as the first stage of the crossing detector because its output impedance can be tuned off-chip (by controlling the voltage on the gate of the triode MOSFET). For similar flexibility, a configurable binary-weighted capacitor was placed at the output of this stage. The capacitor only loads the amplifier during the fine charge-transfer ramp and can be used to control the bandwidth of the amplifier. However, this capacitor was not used during final data collection because it reduces the noise performance of the implemented chip.

The dynamic crossing detector (stage 3) was chosen because it has little delay, and gives a rail-to-rail output signal. Another advantage of this topology is that it has low static power dissipation, only requiring a small current to counter the effects of leakage. A disadvantage of the dynamic crossing detector is that it is only single-ended, thus it must be preceeded by differential gain stages in a high accuracy ADC for adequate power supply noise rejection.

In the actual chip implementation, separate crossing detectors are used for controlling the coarse and fine charge-transfer ramps. Using separate crossing detectors

mitigates the challenge of designing a single crossing detector that is both fast and accurate. The coarse crossing detector consists of a differential-to-single-ended amplifier and a dynamic crossing detector (stages 2 & 3 of Fig. 7-11). The fine crossing detector consists of a chopper-stabilized differential amplifier (stage 1) which is attached to two coarse crossing detectors (stages 2 & 3) wired in parallel with opposite polarities. The two sets of stages 2 & 3 are required because the dynamic crossing detector only detects crossings in one direction. Note that only one of the two sets is used in each charge-transfer cycle, depending on the direction of chopping. The use of chopper stabilization for the implemented ADC is explained in more detail in Sec. 7.3.5.

7.2.2 Crossing Detector Delay

Plots of delay versus input ramp rate, as simulated in Cadence, for the coarse charge-transfer crossing detector (which is identically sized in all integrator stages), integrator 1's fine charge-transfer crossing detector, and the fine charge-transfer crossing detectors of integrators 2-4, are shown in Fig. 7-12.[6] As the slope of the input signal increases, the coarse crossing detector approaches a minimum delay of approximately 0.7 ns, and the fine crossing detectors approach a minimum delay of approximately 1.7 ns (integrators 2-4) and 2.5 ns (integrator 1). Note that this delay does not include some of the logic and switches associated with the gated current sources controlled by the crossing detectors.[7]

Approximately 13 ns is allocated for the coarse charge-transfer. For $V_{DD} - V_{SS} = 1V$, the coarse charge-transfer ramp rate is then 2V/13ns = 154 mV/ns. Reading from Fig. 7-12, the coarse crossing detector delay at that ramp rate is approximately 0.8ns.

[6]The input ramp was hard clamped from [0, 1.2V]. Ramp rates given are differential, $\frac{d(V_{inp}-V_{inn})}{dt}$. The size ratio between the fine charge-transfer crossing detectors of integrator 1 and integrators 2-4 is 6:1. For characterization purposes, the integrator 1 crossing detector was loaded with a 100 fF capacitor. The fine crossing detector of integrators 2-4 and coarse crossing detector was loaded with 20fF capacitors.

[7]The delay for very slow input ramps (< 1mV/ns) is affected by crossing detector offset. The offset varies with the common-mode level at the input of the crossing detector, which causes a change in bias current due to the finite output impedance of the tail current sources. This change in bias current creates an offset at the interface between the differential-to-single-ended amplifier and the dynamic crossing detector.

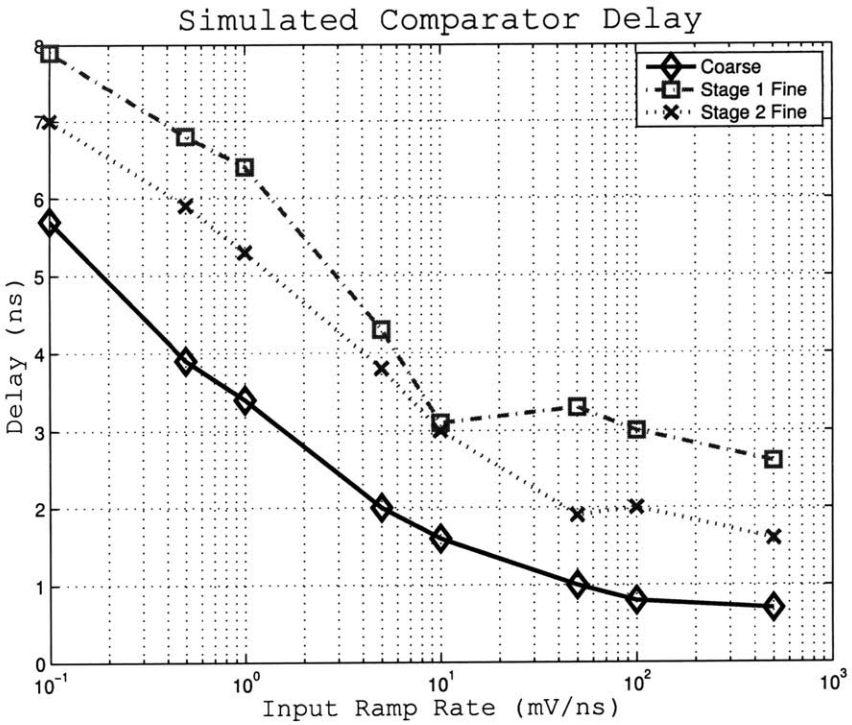


Figure 7-12: Differential crossing detector: delay vs. input ramp rate.

The expected overshoot is thus 0.8ns * 154 mV/ns = 123 mV. Cadence simulations show a coarse overshoot of approximately 140 mV for the integrators.

Approximately 30 ns is allocated for the fine charge-transfer. The fine charge-transfer ramp rate is then at least 140mV/30ns = 4.7 mV/ns. Reading from Fig. 7-12, the fine crossing detector delay at that ramp rate is approximately 4 ns. The expected overshoot for the fine charge-transfer is thus 4ns * 4.7 mV/ns, which is less than 20mV.

7.3 Noise Analysis

7.3.1 Signal Power

For an input of $V_{sin} = \frac{A}{2}\sin(2\pi ft)$, the mean-square value is[8]

$$\begin{aligned} \overline{V_{sin}^2} &= \frac{1}{f}\int_0^{1/f} |\frac{A}{2}\sin(2\pi ft)|^2\, dt \\ &= \frac{A^2}{8}, \end{aligned} \tag{7.2}$$

and the root-mean-square value is

$$\overline{V_{sin}} = \frac{A}{2\sqrt{2}}. \tag{7.3}$$

7.3.2 Allowed Noise

For an N-bit ADC, where A/2 is the amplitude of the full-scale sinusoidal signal, the quantization error is uniformly distributed in the range of $A\left(\pm\frac{1}{2}\right)\left(\frac{1}{2^N}\right) = \pm\frac{A}{2^{N+1}}$. The mean-square value of this error is

$$\begin{aligned} \overline{V_q^2} &= \left(\frac{1}{\frac{A}{2^{N+1}} - \frac{-A}{2^{N+1}}}\right)\int_{\frac{-A}{2^{N+1}}}^{\frac{A}{2^{N+1}}} x^2\, dx \\ &= \left(\frac{2^N}{A}\right)\frac{x^3}{3}\Bigg|_{\frac{-A}{2^{N+1}}}^{\frac{A}{2^{N+1}}} \\ &= \left(\frac{2^N}{A}\right)\left(\frac{1}{3}\right)\left(\frac{A^3}{2^{3N+3}} - \frac{-A^3}{2^{3N+3}}\right) \\ &= \left(\frac{2^N}{A}\right)\left(\frac{1}{3}\right)\left(\frac{A^3}{2^{3N+2}}\right) \\ &= \frac{(A/2^N)^2}{12}. \end{aligned} \tag{7.4}$$

[8]For in-depth details of this derivation, see App. A.

For N = 14 bits, and A = 1 V, this corresponds to a root-mean-square quantization noise voltage of[9]

$$\begin{aligned}\overline{V_q} &= \frac{(A/2^N)}{\sqrt{12}} \\ &= \frac{(1/2^{14})}{\sqrt{12}} \\ &= 17.6\mu V.\end{aligned}$$

Note that the results of Eq. 7.3 and Eq. 7.4 can be used to derive the conversion between signal-to-noise-and-distortion ratio (SNDR) and effective number of bits (ENOB):

$$\begin{aligned}\text{SNDR} &= 10\log_{10}\frac{\overline{V_{sin}^2}}{\overline{V_q^2}} \\ &= 10\log_{10}\frac{\frac{A^2}{8},}{\frac{(A/2^{\text{ENOB}})^2}{12}} \\ &= 10\log_{10}\frac{12(2^{2\,\text{ENOB}})}{8} \\ &= 10\log_{10}\frac{12}{8} + (2\ \text{ENOB})10\log_{10}2 \\ &= 1.76\ \text{dB} + (\text{ENOB})6\ \text{dB}. \qquad (7.5)\end{aligned}$$

7.3.3 Sampled Thermal Noise

When sampling a voltage across a capacitor, the thermal noise of any series resistance is also sampled. The power spectral density for the thermal noise of a resistor is $S_{VR}(f) = 4kTR$ V^2/Hz, where k is Boltmann's constant, and T is temperature in Kelvin. If V_{in} is the voltage across a capacitor, C, and resistor, R, in series, and V_C is the voltage across the capacitor, then the ratio $\frac{V_C}{V_{in}} = \frac{1}{sC}/(R + \frac{1}{sC}) = \frac{1}{sCR+1}$. Integrating across frequency, the mean-square voltage of the noise sampled onto the

[9]For a power supply of $V_{DD} - V_{SS} = 1$ V, the full-scale differential signal range is ± 1 V which corresponds to A = 2 V. However, in a high-order single-bit delta-sigma modulator, the stable input range is usually a few dB below full-scale [21].

capacitor is[10]

$$\begin{aligned}\overline{V_C^2} &= \int_0^\infty 4kTR\left|\frac{1}{sCR+1}\right|^2 df \\ &= \int_0^\infty \frac{4kTR}{(2\pi fCR)^2+1^2}\,df \\ &= \frac{kT}{C}. \end{aligned} \tag{7.6}$$

If this noise is sampled at frequency f_s, the noise power spectral density is $\overline{V_C^2}/(f_s/2)$. If the sampling frequency, f_s, oversamples a signal by a factor of OSR, then the portion of the power spectral density that falls into the signal band is 1/OSR. Thus, the mean-square noise voltage becomes

$$\overline{V_C^2} = \frac{kT}{C}\Big/\,\text{OSR}. \tag{7.7}$$

For sampled thermal noise (Eq. 7.7) to be less than quantization noise (Eq. 7.4),

$$\begin{aligned}\overline{V_C^2} &< \overline{V_q^2} \\ \frac{kT}{C}\frac{1}{\text{OSR}} &< \frac{(A/2^N)^2}{12} \\ C &> \frac{12\,(2^{2N})\,k\,T}{A^2\,\text{OSR}}. \end{aligned} \tag{7.8}$$

For a N = 14 bits, T = 300 K, A = 1 V, and OSR = 256,

$$\begin{aligned} C &> \frac{12\,(2^{2(14)})(1.38\text{x}10^{-23}\frac{m^2\,kg}{s^2K})300\text{K}}{(1)^2\,256} \\ &= 0.05\text{ pF}. \end{aligned}$$

If the signal is being sampled differentially across two capacitors in series, then the value of each capacitor should be 2C.

As a conservative design, sampling capacitors, C_{IN}, of size 1 pF were used in the first integrator stage. For OSR = 256, this corresponds to a root-mean-square

[10]For in-depth details of this derivation, see App. A.

sampled thermal noise voltage of

$$\begin{aligned}\overline{V_C} &= \sqrt{\frac{kT}{C}\frac{1}{\text{OSR}}} \\ &= \sqrt{\frac{(1.38\text{x}10^{-23}\frac{m^2\,kg}{s^2K})300\text{K}}{1\text{ pF}/2}\frac{1}{256}} \\ &= 5.7\mu V.\end{aligned}$$

Because the gain of an integrator is C_{IN}/C_{FB}, the size of C_{FB} was determined from C_{IN} and coefficient c1 of Table 7.1. The scaling for integrators 1-4 was 6:1:1:1, with the latter integrators made smaller in size to decrease power consumption. The limit on scaling for integrators 2-4 came from the sizes of binary-weighted components which came close to the minimum-size for the process.

7.3.4 Crossing Detector Thermal Noise

Power Spectral Density

We first examine the thermal noise for the first stage of Fig. 7-11, which is a differential amplifier with resistive load. The input pair is implemented with NMOS transistors and the resistive load is implemented with a pair of PMOS transistors in triode.

Let $S_{Vn,active}$ represent the power spectral density of the voltage noise of an NMOS in the forward-active region. Let $S_{Ip,triode}$ represent the power spectral density of the current noise of a PMOS in the linear region [15]. The input-referred power spectral density of the thermal noise of the differential amplifier with resistive load is[11]

$$\begin{aligned}S_{Vin,ampl,therm} &= 2(S_{Vn,active}) + 2\left(\frac{S_{Ip,triode}R_{o1}^2}{(g_{mn1}R_{o1})^2}\right) \\ &= 2\left(\frac{8}{3}\frac{kT}{g_{mn1}}\right) + 2\left(\frac{4kTg_{ds}R_{o1}^2}{(g_{mn1}R_{o1})^2}\right) \\ &= \frac{16}{3}\frac{kT}{g_{mn1}} + \frac{8kTg_{ds}}{g_{mn1}^2}. \qquad (7.9)\end{aligned}$$

[11]We ignore the noise of the tail current source, because it effects both sides of the differential amplifier equally and thus has negligible effect on the differential signal at the output.

The input pair has a transconductance of g_{mn1} and an output impedance of r_{on1}. The channel conductance of the triode load is g_{ds}. The total output impedance of the differential amplifier with resistive load is $R_{o1} = r_{on1}||\frac{1}{g_{ds}}$.

The input-referred power spectral density of the thermal noise of the differential-to-single-ended amplifier [15][39][21] (stage 2 of the crossing detector of Fig. 7-11) is[12]

$$\begin{aligned} S_{Vin,amp2,therm} &= 2(S_{Vn,active}) + 2\left(\frac{S_{Ip,active}R_{o2}^2}{(g_{mn2}R_{o2})^2}\right) \\ &= 2\left(\frac{8}{3}\frac{kT}{g_{mn2}}\right) + 2\left(\frac{\frac{8}{3}kTg_{mp2}R_{o2}^2}{(g_{mn2}R_{o2})^2}\right) \\ &= \frac{16}{3}\frac{kT}{g_{mn2}} + \frac{16kTg_{mp2}}{3g_{mn2}^2}. \end{aligned} \tag{7.10}$$

The input pair has a transconductance of g_{mn2} and an output impedance of r_{on2}. The active load pair has a transconductance of g_{mp2} and an output impedance of r_{op2}. The total output impedance of the differential amplifier with resistive load is $R_{o2} = r_{on2}||r_{op2}$.

We refer the noise of Eq. 7.10 to the input of the crossing detector by attenuating it by the gain of the preceeding stage, the differential amplifier with resistive load. Summing this result with that from Eq. 7.9, we get a combined input-referred power spectral density of the thermal noise of the crossing detector of

$$\begin{aligned} S_{Vin,ZCD,therm} &= S_{Vin,amp1,therm} + \frac{S_{Vin,amp2,therm}}{(g_{mn1}R_{o1})^2} \\ &= \frac{16}{3}\frac{kT}{g_{mn1}} + \frac{8kTg_{ds}}{g_{mn1}^2} + \frac{\frac{16}{3}\frac{kT}{g_{mn2}} + \frac{16kTg_{mp2}}{3g_{mn2}^2}}{(g_{mn1}R_{o1})^2} \\ &= \frac{16}{3}\frac{kT}{g_{mn1}}\left(1 + \frac{3g_{ds}}{2g_{mn1}} + \frac{1}{g_{mn2}\,g_{mn1}R_{o1}^2} + \frac{g_{mp2}}{g_{mn2}^2\,g_{mn1}R_{o1}^2}\right). \end{aligned} \tag{7.11}$$

[12]Although the output of this stage is single-ended, the noise contribution of the tail current source is still negligible and can be ignored [15]. Any noise current added by the current source is split evenly between the NMOS input pair, and roughly cancels at the output through the PMOS current mirror [21].

The voltage gain of the differential amplifier with resistive load (stage 1 of Fig. 7-11) is $g_{mn1}R_{o1}$, of which

$$1 << g_{mn1}R_{o1} = g_{mn1}\left(r_{on1}||\frac{1}{g_{ds}}\right) < \frac{g_{mn1}}{g_{ds}}.$$

It thus becomes clear that the last three terms of Eq. 7.11 are negligible compared to the first term. In other words, the thermal noise of the input pair to the first amplifier of the crossing detector dominates the input-referred thermal noise.

In the implemented circuit, with 10 μA bias current for the differential amplifier with resistive load, $g_{mn1} = 143.2$ μS, $r_{on1} = 1/6.6$ μS, and $g_{ds} = 2.0$ μS as measured in Cadence. This corresponds with a voltage gain, $g_{mn1}R_{o1} = 16.7$.

For simplicity, the noise of later stages of the crossing detector (specifically, the dynamic crossing detector, which is stage 3 of the crossing detector of Fig. 7-11) have been ignored; when referred to the input of the crossing detector, these noise sources will be attenuated by the gains of the amplifiers that preceed them and will also become negligible.

Crossing Detector Equivalent Noise Bandwidth

Using the input-referred power spectral density of the thermal noise of the crossing detector (Eq. 7.11), we now compare the equivalent input-referred noise bandwidth for two cases - a differential amplifier in steady-state (lower gain, higher bandwidth) and a differential amplifier acting as an ideal integrator (higher gain, lower bandwidth). In both cases, the thermal noise undergoes continuous-time filtering by the crossing detector's frequency response.

For the amplifier in steady state,

$$V_{out,amp1}(s) = V_{in,amp1}g_{mn1}\left(\frac{1}{\frac{1}{R_{o1}} + sC_{o1}}\right),$$

where C_{o1} is the capacitance at the output node of the differential amplifier with resistive load. The steady-state transfer function for the differential amplifier with

resistive load is then

$$H_{ampl}(s) = \frac{V_{in,ampl}}{V_{out,ampl}(s)} = \frac{g_{mn1}R_{o1}}{1 + sR_{o1}C_{o1}}. \tag{7.12}$$

We find the output-referred noise for the case of the differential amplifier in steady-state case by multiplying by the single-pole transfer function of Eq. 7.12 and integrating the noise power spectral density with respect to frequency. To refer this voltage back to the input of the amplifier, we divide by the amplifier gain in the signal band, which is approximately the same as the DC gain, $H_{ampl}(0) = g_{mn1}R_{o1}$. Thus,

$$\overline{V_{in,ampl}^2} = \int_0^\infty S_{Vin1,therm} \left| \frac{H(s)}{g_m R_o} \right|^2 df$$

Because $S_{Vin1,therm}$ is white noise and therefore not a function of frequency,[13]

$$\begin{aligned} \overline{V_{in,ampl}^2} &= S_{Vin,ampl,therm} \int_0^\infty \left| \frac{H(s)}{g_m R_o} \right|^2 df \\ &= S_{Vin,ampl,therm} \int_0^\infty \left(\frac{1}{1 + (2\pi f R_o C_o)^2} \right) df \\ &= S_{Vin,ampl,therm} \left(\frac{1}{4R_o C_o} \right) \\ &= S_{Vin,ampl,therm} \, \mathrm{NBW}_{\mathrm{ampl,ss}}. \end{aligned} \tag{7.13}$$

We see that the white thermal noise has been filtered by the differential amplifier, where $NBW_{ampl,ss}$ is the equivalent noise bandwidth of the differential amplifier in steady-state. $NBW_{ampl,ss} = \frac{1}{4R_oC_o} = \frac{1}{4\tau_{ampl}}$, where τ_{ampl} is the time constant of the differential amplifier. This equivalent noise bandwidth is valid for white noise filtered by any first-order (single-pole) system in steady-state with time constant τ_{ampl}.

The steady-state result given in Eq. 7.13 is a particular case of the general solution given in [22], and repeated in [1], and [40]. The analysis in [22] separates the crossing detector delay into two components,

$$t_{delay} = t_i + t_d. \tag{7.14}$$

[13]For in-depth details of this derivation, see App. A.

The integration response time, t_i, is the time it takes for the differential amplifier's output voltage to transition from the zero initial condition (clamp voltage) to a detection threshold, triggering the threshold detector that follows it. The propagation delay, t_d, occurs after the output of the differential amplifier reaches the detection threshold, until the output voltage of the circuit (e.g. integrator or multiply-by-two stage) is sampled and/or the gated current source is turned off. Using this distinction, the derivation of [22] gives the general noise bandwidth for a first-order system of time constant, τ_o, sampling white noise for a time, t_i. The result of the derivation is

$$\mathrm{NBW} = \frac{1}{4\tau_o} \coth\left(\frac{t_i}{2\tau_o}\right) u(t_i) \tag{7.15}$$

For large x, $\coth x \approx 1$. Thus for $t_i >> \tau_o$

$$\mathrm{NBW}_{ampl,ss} = \frac{1}{4\tau_o}, \tag{7.16}$$

which matches the result of the derivation above for the steady-state case. The solution of Eq. 7.15 for $t_i << \tau_o$ gives the equivalent noise bandwidth for a crossing detector comprised of an ideal integrator followed by an infinitely fast threshold detector and infinitely fast logic gates. Using the Taylor series approximation that $\coth x \approx 1/x$ for x close to zero, the equivalent noise bandwidth of the ideal integrator case is

$$\mathrm{NBW}_{ampl,int} \approx \frac{1}{4\tau_o}\frac{2\tau_o}{t_i} \tag{7.17}$$

$$= \frac{1}{2t_i}. \tag{7.18}$$

The steady-state case applies to opamp-based circuits, as well as to a ZCB circuit where the differential amplifier is fast enough for its output to have mostly settled when it reaches the threshold of the subsequent threshold detector. The case of the differential amplifier as an ideal integrator applies to the situation in a ZCB or LV-ZCB circuit where the differential amplifier has not yet reached steady-state, but the subsequent threshold detector has already reached its threshold. In comparing a ZCB

circuit that matches the ideal integrator (not steady state) case against an opamp-based circuit, if the two circuits have the same noise spectral density, the ZCB circuit offers superior noise performance if

$$\begin{aligned} 2t_i &> 4\tau_{ampl} \\ t_i &> 2\tau_{ampl}, \end{aligned} \tag{7.19}$$

the crossing detector's response time is longer than two of the comparable opamp's time constants.

As a conservative estimate for the time constant in a conventional switched-capacitor integrator, consider the case of a single-bit delta-sigma ADC with zero input. The magnitude of the quantization error in any given cycle is thus $(V_{DACp} - V_{DACn})/2$, where V_{DACp} and V_{DACn} are the positive and negative DAC reference voltages. According to Eq. 5.11, the change in voltage at the integrator output (also the opamp output) each cycle is

$$\begin{aligned} |\Delta V_{out}| &= \frac{C_{IN}}{C_{FB}} |V_{in} - V_{DAC}| \\ &= \frac{C_{IN}}{C_{FB}} \left(\frac{V_{DACp} - V_{DACn}}{2} \right). \end{aligned} \tag{7.20}$$

If the delta-sigma ADC is required to be N-bits accurate, then the maximum input-referred error is[14]

$$V_{in,err,max} = \frac{(V_{DACp} - V_{DACn})}{2^{N+1}}.$$

To find the acceptable error at the output of the integrator, we multiply by the integrator gain:

$$\begin{aligned} V_{out,err,max} &= \frac{C_{IN}}{C_{FB}} V_{in,err,max} \\ &= \frac{C_{IN}}{C_{FB}} \frac{(V_{DACp} - V_{DACn})}{2^{N+1}}. \end{aligned} \tag{7.21}$$

[14]Note that the error of an actual implementation would have to be smaller because this equation assumes a full-swing input signal, which would not be possible for most modulators due to stability issues.

Dividing Eq. 7.21 by Eq 7.20, we find the fraction of the charge-transfer which can remain incomplete due to finite settling, such that the ADC is N-bits accurate regardless of the linearity of the settling. If the opamp is dominant-pole compensated, exhibiting a first-order settling response characterized by time constant, τ_{ampl}, then

$$\begin{aligned} \frac{\frac{C_{IN}}{C_{FB}}\frac{(V_{DACp}-V_{DACn})}{2^{N+1}}}{\frac{C_{IN}}{C_{FB}}\left(\frac{V_{DACp}-V_{DACn}}{2}\right)} &= e^{\left(\frac{-t}{\tau_{ampl}}\right)} \\ 2^{-N} &= e^{\left(\frac{-t}{\tau_{ampl}}\right)}. \end{aligned}$$

The number of time constants over which the opamp must settle is

$$n = \frac{t}{\tau_{ampl}} = -\ln\left(2^{-N}\right) = N\ln 2 = 0.69N.$$

For N = 14 bits, this corresponds to $n = 9.7$ time constants of settling. This number of time constants must happen during the charge-transfer phase, which has a duration of $\frac{1}{2f_s}$, where f_s is the sampling frequency of the modulator. Thus,

$$\begin{aligned} n\tau_{ampl} &= \frac{1}{2f_s} \\ \tau_{ampl} &= \frac{1}{2f_s n} \\ \tau_{ampl} &= \frac{1}{2f_s N\ln 2}. \end{aligned}$$

For N = 14 bits and f_s = 10 MHz, τ_{ampl} = 5.15 ns. In accordance with Eq. 7.19, a ZCB circuit for which the crossing detector delay is allowed to be greater than $2\tau_{ampl}$ = 10.3 ns will have better thermal noise performance than the comparable opamp-based circuit.

Note that the crossing detector and the comparable opamp need not have the same time constant for a circuit of the same speed. The crossing detector doesn't need to reach steady-state and can therefore have lower bandwidth than the comparable opamp. For a ZCB integrator whose noise performance is dominated by the thermal noise of the first stage of its crossing detector, this flexibility could be used

to add an extra capacitor to increase C_o of the crossing detector's first differential amplifier stage, increasing t_i according to Eq. 5.16 and decreasing the noise bandwidth according to Eq. 7.18. Alternatively, for the same bias current, the input pair of the differential amplifier could be made wider, increasing $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$, lowering the noise power spectral density, and also increasing C_o due to the increased drain capacitance of the larger input pair.

Referral of Crossing Detector Noise to Input of Integrator

We now calculate the transfer function from the input of the crossing detector of Fig. 5-8 to the input of the integrator, $V_{inp} - V_{inn}$. Suppose an error voltage, $+\Delta V$, is applied as a differential offset to the input of the crossing detector, $V_{in,amp1}$. We assume that C_{OS} is large relative to the parasitic capacitance at the input to the crossing detector and thus the voltage drop across C_{OS} is constant. During the charge-transfer phase, when the crossing detector detects the virtual ground condition on the virtual ground nodes, $V_{Xp} - V_{Xn}$, the error in the crossing detector will result in an error on the virtual ground nodes of

$$V_{X,err} = -\Delta V. \tag{7.22}$$

During the charge-transfer phase, the change in voltage at the output of the integrator, $V_{outp} - V_{outn}$, is related to the change in voltage at the virtual ground nodes, $V_{Xp} - V_{Xn}$, by the voltage divider between capacitors C_{FB} and C_{IN}. The error on the virtual ground nodes thus causes an error in the integrator output voltage of

$$\begin{aligned} V_{out,err} &= V_{X,err} * \text{noise gain} \\ &= \frac{V_{X,err}}{\frac{C_{FB}}{C_{FB}+C_{IN}}} \\ &= \frac{-\Delta V(C_{FB}+C_{IN})}{C_{FB}}. \end{aligned} \tag{7.23}$$

Typically when referring noise to the input of a system, we find the effect on V_{out} and divide by the transfer function V_{out}/V_{in} of the system. In the case of an integrator,

that would mean dividing by the integrator transfer function, thus the noise becomes first-order noise-shaped when referred to the input.[15] To understand the significance of the first-order noise shaping, we consider the effect of referring this noise to the input of the integrator. If the input-referred noise of the crossing detector is $\overline{V_{in,ampl}^2}$, then the effect on the output of the integrator can be determined using Eq. 7.23 to be

$$\overline{V_{out}^2} = \overline{V_{in,ampl}^2}\left(\frac{C_{FB}+C_{IN}}{C_{FB}}\right)^2. \tag{7.24}$$

Although this noise has a low-pass-filtered spectral density, when it is sampled at the end of each charge-transfer phase, the resulting distribution is approximately white due to aliasing [21]. The power spectral density is then $S_{v,out} = \overline{V_{out}^2}/(f_s/2)$. The noise can then be referred to the input of the integrator using Eq. 6.11, which calculates the effect of first-order noise shaping, where $g = C_{IN}/C_{FB}$ is the gain of the integrator and the power spectral density of the white noise to be shaped is $S_N = S_{v,out}$:

$$\begin{aligned}
\overline{V_{in}^2} &= \frac{\overline{V_{out}^2}}{f_s/2}\left(\frac{C_{FB}}{C_{IN}}\right)^2\left(\frac{f_s\,\pi^2}{6\,\mathrm{OSR}^3}\right) \\
&= \frac{\overline{V_{in,ampl}^2}\left(\frac{C_{FB}+C_{IN}}{C_{FB}}\right)^2}{f_s/2}\left(\frac{C_{FB}}{C_{IN}}\right)^2\left(\frac{f_s\,\pi^2}{6\,\mathrm{OSR}^3}\right) \\
&= \overline{V_{in,ampl}^2}\left(\frac{C_{FB}+C_{IN}}{C_{IN}}\right)^2\left(\frac{\pi^2}{3\,\mathrm{OSR}^3}\right).
\end{aligned} \tag{7.25}$$

Similar to Eq. 6.13, which quantizes the effects of first-order noise shaping, the term on the right side of Eq. 7.25 for OSR = 256 is

$$\frac{\pi^2}{3\,(256)^3} = 1.96\text{x}10^{-7},$$

which represents an attenuation of $10\log_{10}(1.96\text{x}10^{-7})$ = -67 dB. This large attenuation shows that noise that only affects the voltage at the output of an integrator without affecting the charge integrated on capacitor C_{FB} has a negligible effect on the input-referred noise of the integrator.

[15]Note that noise on V_{out} is indistinguishable from noise at the input of the following integrator stage.

The more significant effect of the crossing detector noise is on the charge stored on C_{FB}, which is integrated each cycle and thus does not benefit from any noise-shaping. We thus examine the effect of the errors of Eq. 7.22 and Eq. 7.23 on the charge stored on integration capacitors, C_{FB} each cycle:

$$\begin{aligned}
\Delta Q_{CFB,err} &= C_{FB}(V_{out,err} - V_{X,err}) \\
&= C_{FB}\left(\frac{-\Delta V(C_{FB}+C_{IN})}{C_{FB}} + \Delta V\right) \\
&= C_{FB}\left(\frac{-\Delta V(C_{FB}+C_{IN})}{C_{FB}} + \frac{\Delta V C_{FB}}{C_{FB}}\right) \\
&= -\Delta V\, C_{IN}.
\end{aligned} \tag{7.26}$$

We then refer this error to the integrator input voltage, $V_{inp} - V_{inn}$, by dividing by the gain of Eq. 5.1:

$$\begin{aligned}
V_{in,err} &= \frac{Q_{CFB,err}}{\frac{d\Delta Q}{dV_{in}}} \\
&= \frac{-\Delta V\, C_{IN}}{C_{IN}} \\
&= -\Delta V.
\end{aligned} \tag{7.27}$$

Thus, in terms of the effect on the charge integrated onto C_{FB} each cycle, the magnitude of the gain from the input of the crossing detector, $V_{in,amp1}$, to the input of the integrator, V_{in}, is $\left|\frac{V_{in,err}}{V_{in,amp1}}\right| = 1$.[16]

Using Eq. 7.11 and Eq. 7.15, and using the same argument for oversampling presented in Sec. 7.3.3 for Eq. 7.7, the thermal noise of a crossing detector (input pair transconductance, $g_{mn1} = 143.2\mu S$; time constant, $\tau_{amp1} = 4.8$ ns) referred to the input of the corresponding ZCB integrator (oversampling ratio, OSR = 256) is

[16] An intuitive explanation for this is that there is no way to distinguish between an error on V_{in} during the sampling phase, ϕ_1, and an error of the same magnitude on V_X during the charge-transfer cycle. Either way, the charge on C_{IN} is disturbed by the same amount.

thus

$$\begin{aligned}
\overline{V_{in}^2} &= (S_{Vin,ZCD,therm}) \left| \frac{V_{in,err}}{V_{in,ampl}} \right|^2 (\text{NBW}) \left(\frac{1}{\text{OSR}} \right) \\
&\approx \left(\frac{16}{3} \frac{kT}{g_{mn1}} \right) 1^2 \left[\frac{1}{4\tau_{ampl}} \coth \left(\frac{t_i}{2\tau_{ampl}} \right) \right] \left(\frac{1}{\text{OSR}} \right) \\
&= \frac{16}{3} \frac{(1.38\text{x}10^{-23} \frac{m^2 kg}{s^2 K}) \, 300\text{K}}{143.2\mu S} \left[\frac{1}{4(4.8ns)} \coth \left(\frac{t_i}{2(4.8ns)} \right) \right] \left(\frac{1}{256} \right) \\
&= \begin{cases} 3\text{x}10^{-19}/t_i \quad V^2/\text{Hz} & \text{for } t_i << \tau_{ampl} = 4.8 \text{ ns} \\ 5.6\mu V & \text{for } t_i >> \tau_{ampl} = 4.8 \text{ ns} \end{cases}
\end{aligned} \tag{7.28}$$

The root-mean-square thermal noise voltage for various values of t_i is given is Table 7.2.

Table 7.2: Integration Response Time vs. Thermal Noise RMS Voltage

t_i (ns)	$\overline{V_{in}}$ (μV)
1	24.6
5	11.4
15	8.3
30	7.9

Note that the above derivation for the referral of crossing detector noise to the input of the LV-ZCB integrator ignores the effect of parasitic capacitance. It also does not take into account capacitor C_{DC} (see Sec. 4.2.2), which is not used in integrator 1, but is used in integrators 2-4 of the implemented ADC. For the general case of parasitic capacitance, C_p, at node V_X, and the use of capacitor C_{DC}, the noise gain is affected according to Eq. 4.13. Thus, Eq. 7.26 becomes

$$\begin{aligned}
\Delta Q_{CFB,err} &= C_{FB}(V_{out,err} - V_{X,err}) \\
&= C_{FB} \left(\frac{-\Delta V(C_{FB} + C_{IN} + C_{DC} + C_p)}{C_{FB}} + \Delta V \right) \\
&= -\Delta V(C_{IN} + C_{DC} + C_p),
\end{aligned}$$

and Eq. 7.27 becomes

$$V_{in,err} = -\Delta V \left(\frac{C_{IN} + C_{DC} + C_p}{C_{IN}} \right).$$

The factor of $\left| \frac{V_{in,err}}{V_{in,ampl}} \right|$ in Eq. 7.28 would then be increased accordingly.

7.3.5 Crossing Detector Flicker Noise

The power spectral density of flicker (1/f) noise is modelled as $S_{v,flick}(f) = \frac{K}{WLC_{ox}f}$, where K is device-dependent [15]. Because an ADC for audio frequencies must have high accuracy at relatively low frequencies, special care must be taken to mitigate the effects of flicker noise, which dominates at low frequencies.

As stated in Sec. 7.2, the differential amplifier of the crossing detector for the fine charge-transfer is chopper-stabilized [41]. In chopper stabilization, the differential input connections to the chopper-stabilized stage are swapped each cycle. To maintain the same system function, the differential outputs are also swapped each cycle. This multiplies the noise of the chopper-stabilized stage by a sinusoid at the chopping frequency, $f_s/2$. In the frequency domain, the noise of the chopper-stabilized stage is shifted to the chopping frequency. In this manner, low-frequency noise (e.g. flicker noise) is moved out of the signal band.

Implementing chopper-stabilization under low power supply voltages is not straightforward, because each added switch must be carefully considered. In the implementated differential LV-ZCB integrators (Fig. 5-8), it is possible to use PMOS switches to connect C_{OS} to each crossing detector input, because the crossing detector inputs are biased around V_{REFH}. Thus it is simple to swap these connections each cycle. However, the common-mode level at the output of the differential amplifier (stage 1 of the crossing detector of Fig. 7-11), is set by the bias current and resistive load of the differential amplifier. Since the bias current and resistive load are externally configurable, it was decided not to use switches to connect the differential amplifier with resistive load to the differential-to-single-ended amplifier (stages 1 & 2 of the crossing detector of Fig. 7-11) to avoid adding extra constraints on the current and

resistance values. Instead, a second set of differential-to-single-ended amplifier and dynamic crossing detector (stages 2 & 3 of the crossing detector of Fig. 7-11) is wired to the differential amplifier in parallel with the first set but with opposite polarity. The output of the crossing detector is then taken from alternate dynamic crossing detectors each cycle.

The differential-to-single-ended amplifier and dynamic crossing detector (stages 2 & 3 of the crossing detector of Fig. 7-11) do not benefit from chopper stabilization. However, they do benefit indirectly due to the fact that the noise between the two sets is uncorrelated. Thus, the contribution of their noise is reduced by 3 dB. Their noise contribution is also suppresed by the gain of the differential amplifier with resistive load (stage 1 of Fig. 7-11).

According to [41], the power spectral density of chopper-stabilized flicker noise is

$$S_{CS-1/f}(f) \approx 0.8525\, S_0\, f_k\, T \text{ for } |fT| < 0.5, \tag{7.29}$$

where S_0 is the power spectral density of the thermal noise, f_k is the noise corner frequency at which flicker (1/f) noise and thermal (white) noise contribute equally before chopping, and T is the chopping period.

From Eq. 7.29, the most important factor in implementing chopper stabilization is to be sure that the noise corner frequency is lower than the chopping frequency (plus the signal bandwidth) before chopping is implemented. Then when chopping is implemented and the noise is shifted to the chopping frequency, the flicker noise in the signal band will be negligible compared to the thermal noise.

The differential amplifier of the crossing detector of the first integrator in the implemented ADC uses NMOS transistors of W/L = 300μm / 0.2μm and PMOS transistors of W/L = 5μm / 1μm, all biased at I_d = 5μA. Fig. 7-13 illustrates the gate-referred noise simulated in Cadence for transistors of this size and biasing. For this size and biasing, the PMOS noise corner frequency is approximately 100 kHz. The NMOS noise corner frequency is approximately 1 MHz. For a clock rate of 10 MHz, the chopping frequency for a crossing detector that is chopped every cycle is 5 MHz.

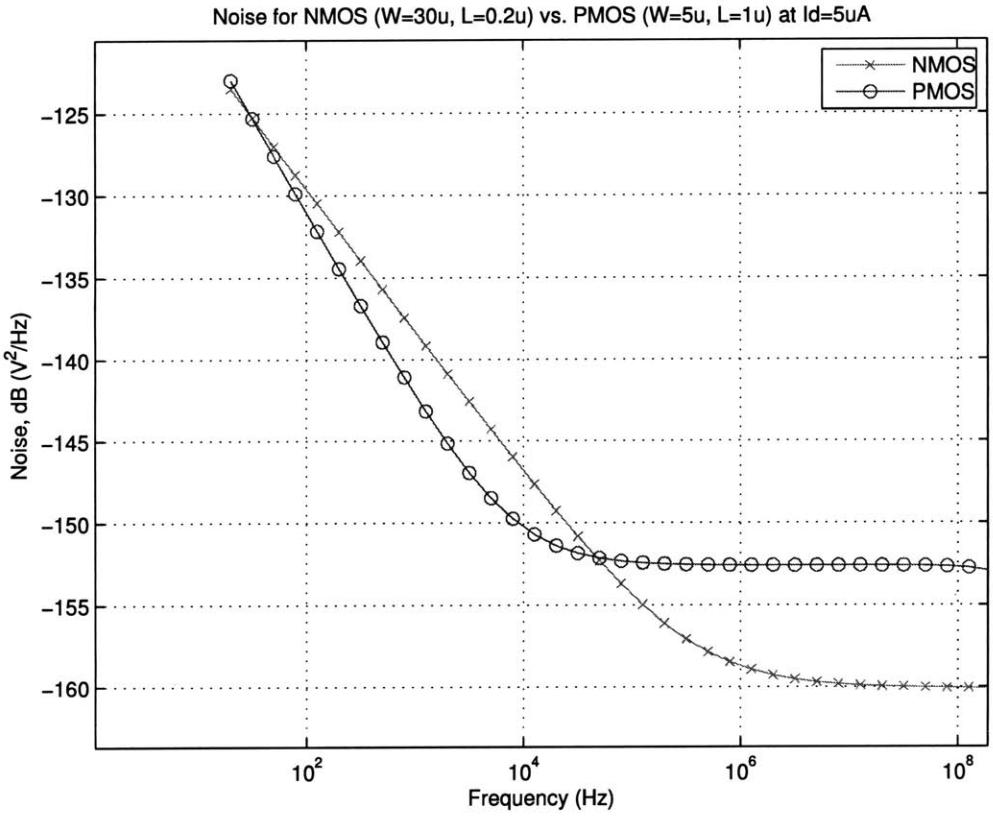


Figure 7-13: Gate-referred noise for NMOS (W=300μm, L=0.2μm), PMOS (W=5μm, L=1μm), I_d=5μA

Thus, both the NMOS and PMOS corner frequencies are safely below the chopping frequency. Note that the PMOS has less flicker (1/f) noise, but more thermal (white) noise.

7.3.6 Other Sources of Noise

A full analysis of noise in CBSC/ZCB circuits is given by [22]. Below is a summary of the results for less significant sources of noise.

Clamp Noise

Clamp noise comes from the variation in the starting voltage at the output of the differential amplifier (stage 1 of the crossing detector of Fig. 7-11) before the ramp signal at the input of the crossing detector begins to be integrated. The decay time-constant for this initial condition is

$$\begin{aligned} \tau_{amp1} &= R_o C_o \\ &= \frac{1}{g_{on1} + g_{ds}} (C_{ddn1} + C_{ddp1} + C_{gg2}) \\ &= \frac{1}{6.6\mu S + 2\mu S} (33 \text{ fF} + 7 \text{ fF} + 1 \text{ fF}) \\ &= 4.8 \text{ ns}, \end{aligned} \tag{7.30}$$

where R_o is the output impedance of the differential amplifier, and C_o is the total capacitance at the output of the differential amplifier. In the implemented circuit, C_{ddn1} and C_{ddp1} are the parasitic drain capacitances of the NMOS input pair and PMOS triode load, and C_{gg2} is the parasitic gate capacitance of the differential-to-single-ended amplifier (stage 2 of the crossing detector of Fig. 7-11). Note that any capacitance explicitly added to this node must also be counted when using Eq. 7.30 to calculate τ_{amp1}.

The pipeline ADC of [1] uses clamp circuitry to enforce an initial condition until the input to the comparator passes a threshold level. In contrast, the delta-sigma ADC of this work does not use clamp circuitry to hold the initial condition. Thus the

initial condition decays for most of the fine charge-transfer. For a fine charge-transfer duration, t_{fine} = 30 ns, the clamp noise experiences over 6 τ_{amp1} of exponential decay, corresponding to $20\log_{10}(e^{-30ns/4.8ns})$ = -54.3 dB of attenuation. Thus the clamp noise becomes negligible compared to other sources of noise in the ciruit.

Gated Current Source Shot Noise

According to [22], the mean-square voltage across a capacitor, C, charged for time, t_i, by a current source with one-sided white noise power spectral density, S_i is

$$\overline{v_C^2}(t_i) \approx \frac{S_i}{2C^2} t_i u(t) \tag{7.31}$$

Using Eq. 7.31, the thermal noise added to C_{FB} during the crossing detector delay, t_{delay}, is

$$\overline{V_{CFB}^2}(t_{delay}) = \frac{S_i}{2C_{FB}^2} t_{delay} u(t).$$

Referring this voltage to the input of the integrator by dividing by the gain specified in Eq. 4.12 gives

$$\begin{aligned} \overline{V_{in}^2}(t_{delay}) &= \frac{S_i}{2C_{FB}^2} t_{delay} u(t) \left(\frac{C_{FB}}{C_{IN}}\right)^2 \\ &= \frac{S_i}{2C_{IN}^2} t_{delay} u(t). \end{aligned} \tag{7.32}$$

For a gated current source with one-sided shot noise power spectral density, $S_i = 2qI_D$, Eq. 7.32 becomes

$$\overline{V_{in}^2}(t_{delay}) = \frac{qI_D}{C_{IN}^2} t_{delay} u(t). \tag{7.33}$$

The overshoot at the output of a ZCB circuit due to crossing detector delay is

$$\begin{aligned} V_{ov} &= \frac{I_D\, t_{delay}}{C} \\ &= I_D\, t_{delay} \frac{C_{IN} + C_{FB}}{C_{IN}\, C_{FB}}. \end{aligned} \tag{7.34}$$

The capacitance, C, in the above equation is the capacitive load on I_D. Note that the load capacitor, C_{IN} of the following stage, has been ignored because it is relatively small due to scaling between integrator stages. Using Eq. 7.33 and Eq. 7.34, and using the same argument for oversampling presented in Sec. 7.3.3 for Eq. 7.7, the equivalent input-referred root-mean-square voltage for gated current source shot noise can be written as

$$\begin{aligned}\overline{V_{in}} &= \sqrt{\left(\frac{1}{\mathrm{OSR}}\right)\left(\frac{qI_D}{C_{IN}^2}t_{delay}\right)\left(\frac{C_{IN}+C_{FB}}{C_{IN}C_{FB}}\right)\left(\frac{C_{IN}C_{FB}}{C_{IN}+C_{FB}}\right)} \\ &= \sqrt{\left(\frac{1}{\mathrm{OSR}}\right)\frac{qV_{ov}}{C_{IN}}\left(\frac{C_{FB}}{C_{IN}+C_{FB}}\right)}. \end{aligned} \tag{7.35}$$

For $C_{IN} = 1\mathrm{pF}$, and $C_{FB} = 2.7$ pF, Table 7.3 lists input-referred shot noise voltage for various overshoot voltages. As can be seen from Table 7.3, for overshoot voltages, V_{ov},

Table 7.3: Output Overshoot Voltage vs. Shot Noise RMS Voltage

V_{ov} (mV)	$\overline{V_{in}}$ (μV)
10	2.1
20	3.0
50	4.8
100	6.7
200	9.6

that are a reasonably small fraction of the differential full scale voltage, $(V_{DD} - V_{SS}) - (V_{SS} - V_{DD}) = 2\mathrm{V}$, the effect of gated current source shot noise is small compared to the thermal noise of the crossing detector (Sec. 7.3.4) seen in Table 7.2. For an overshoot of 20 mV, the shot noise RMS voltage is 3.0 μV.

In practice, the noise contributed by the gated current source of a ZCB circuit is smaller than that given by Eq. 7.35 and shown in Table 7.3. As explained in [22], during the integration response time, t_i, portion (defined in Eq. 7.14) of the crossing detector delay, t_{delay}, the shot noise of the gated current source creates jitter in the preamplifier of the crossing detector which cancels the effects of the shot noise. This results in complete cancellation of the shot noise for the case of a preamplifier in steady-state, and partial cancellation of the shot noise for the case of an ideal

integrator as a preamplifier.

Gated Current Source Flicker Noise

The flicker noise of the gated current sources for the fine charge-transfer can be decreased by making the transistors large. In this manner, the flicker noise is decreased until it becomes negligible within the signal band compared to other sources of noise. Although the flicker noise at frequencies below the signal band will be large, it will have minimal impact, being indistinguishable from offset in the ADC. Because sampling switches (as opposed to turning off the gated current sources) are used to define the sampling instant at the end the fine charge-transfer, the size of the gated current source transistors does not limit the speed of the system.

Switch Noise

According to [22], the thermal noise of switches can be made negligible by minimizing their equivalent noise resistance, $R_{neq,sw}$, compared to the equivalent noise resistance of the crossing detector, $R_{neq,ZCD}$. Using the thermal noise calculated in Sec. 7.3.4, and equalizing it with an equivalent noisy resistor, we get

$$\begin{aligned} 4kTR_{neq,ZCD} &= S_{Vin,ZCD,therm} \\ &\approx \frac{16}{3}\frac{kT}{g_{mn1}} \\ R_{neq,ZCD} &\approx \frac{4}{3\,g_{mn1}} \\ &= \frac{4}{3(143.2\mu S)} \\ &= 9.3k\Omega. \end{aligned}$$

From Fig. 3-1(b), a minimum-sized PMOS switch has a conductance of 0.05 mS at $|V_{gs}| = 0.8V$, which corresponds to a resistance of $1/0.05$ mS $= 20$ kΩ. A minimum-sized NMOS switch has an even larger conductance for the same V_{gs}. Since there are only 6 switches (2 shown per differential path, plus 1 for each fine gated current source) in the differential LV-ZCB integrator of Fig. 5-8 which are conductive during

the charge-transfer phase, and these switches are many times wider than minimum size, their thermal noise is negligible compared to the thermal noise of the crossing detector.

Another source of noise from switches, as described by [22], is the sampled thermal noise which occurs at the end of the charge-transfer phase at the output sampling instant. However, due to the fact that the gains of integrators in a delta-sigma modulator are typically less than one, the integration capacitor, C_{FB} is many times the size of the input sampling capacitor, C_{IN}, and thus its sampled thermal noise is negligible compared to the thermal noise sampled on C_{IN} at the end of the sampling phase.

7.4 Layout

The complete ADC was fabricated in an IBM 0.13 μm CMOS logic process through the Trusted Access Program Office. The die area was 2mm x 2mm. The ADC area was approximately 1.4mm x 1mm. A layout diagram is shown in Fig. 7-14.

7.5 Test Setup

A diagram of the test setup is shown in Fig. 7-15.

The 77-bit on-chip configuration register was initialized using a National Instruments PCI-6533 I/O card (PCI-DIO-32HS), which was controlled with LabVIEW 6.02 and NI-DAQ 6.93 software. Unstrobed I/O mode was chosen [42] with the original purpose of using open-collector output mode. However, due to debugging difficulties, this mode was not used in the final test setup.

An Audio Precision System One was used as the sinusoid source for testing. The source was controlled using an APIB PCI-WIN card using APWIN 2.24.1390 software. The source was connected to the PCB board using an XLR cable. The output was set to balanced (differential) with a floating ground [43]. The floating ground was biased using an external voltage supply.

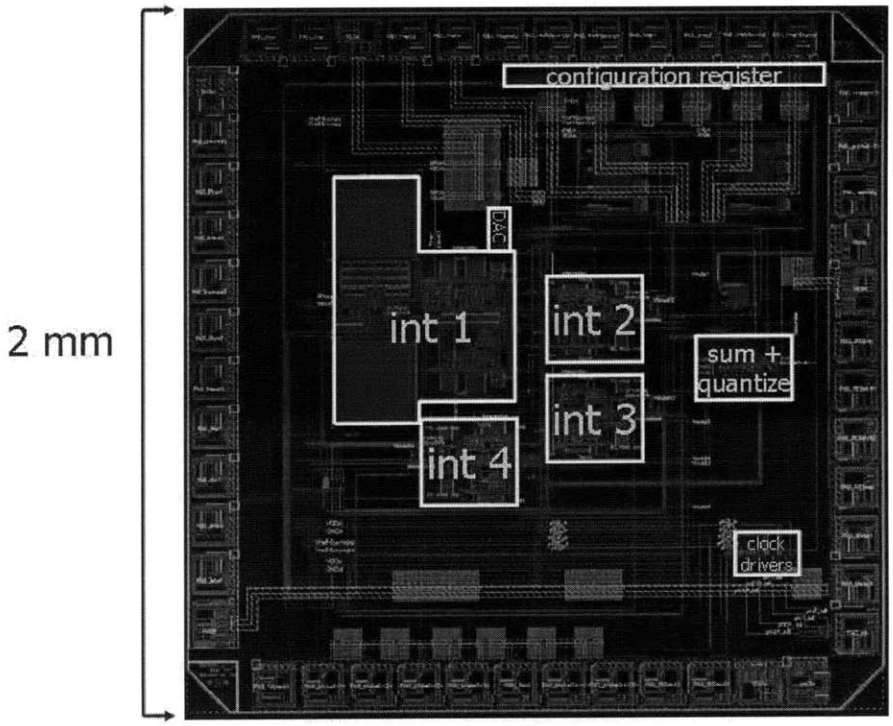


Figure 7-14: Layout of LV-ZCB delta-sigma ADC in 0.13 μm CMOS.

A Hewlett Packard 8112A Pulse Generator was used to generate the 10 MHz square wave master clock for the ADC chip. The generator was set in Fixed Transition mode, which has a rise/fall time of 4.5 ns [44].

Data was captured from the ADC using an Analog Devices ADC-HSC-EVAL FIFO board. The FIFOs have been upgraded from 32 KB to 256 KB. The board was controlled via USB connection using Visual Analog 1.8.14.6 software. The number of points captured per trial was 2^{17}, which at 10 MHz represents 13.1 ms of data.

The computer that contained the PCI-6533 I/O and APIB PCI-WIN cards ran Windows XP SP3.

The decimation of the ADC's output bitstream was processed in Matlab (no on-chip decimation filter).

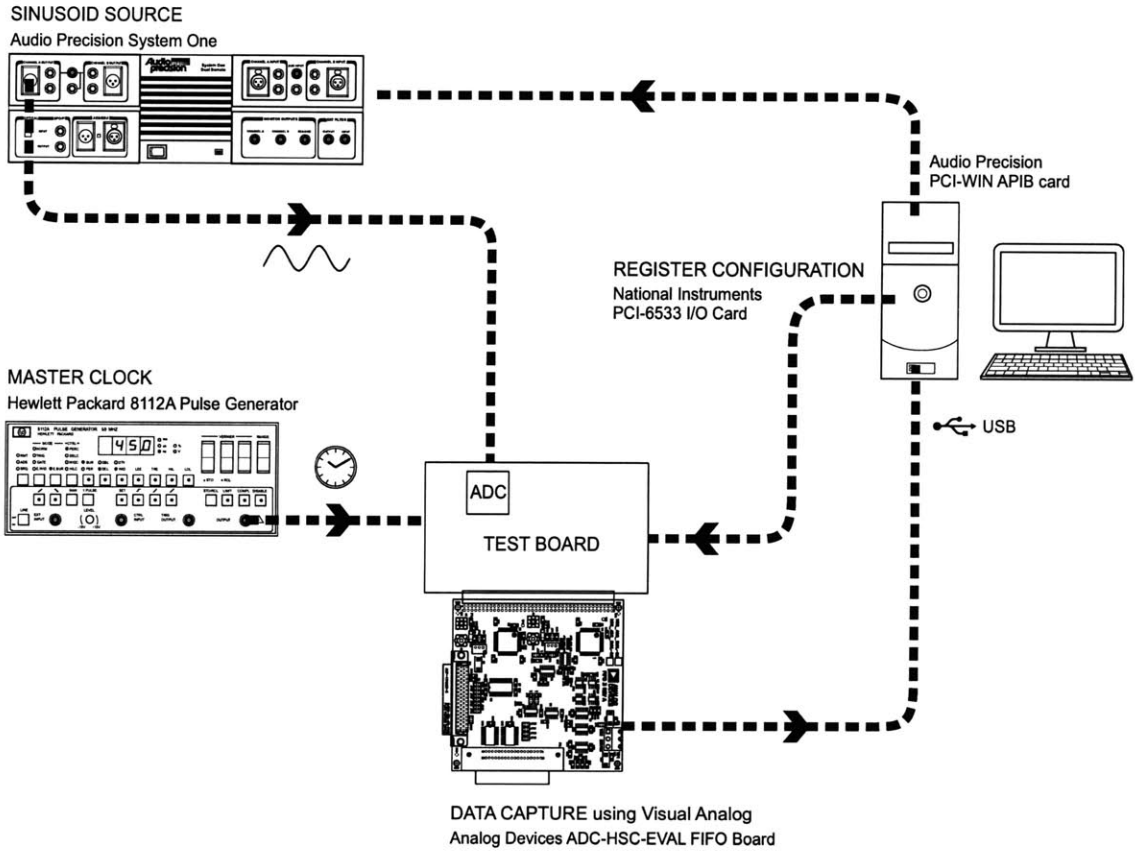


Figure 7-15: Test setup. Figure courtesy of Lingwei Lee.

7.6 Results

An FFT of the bitstream from the ADC chip in response to a sinusoidal input is shown in Fig. 7-16.

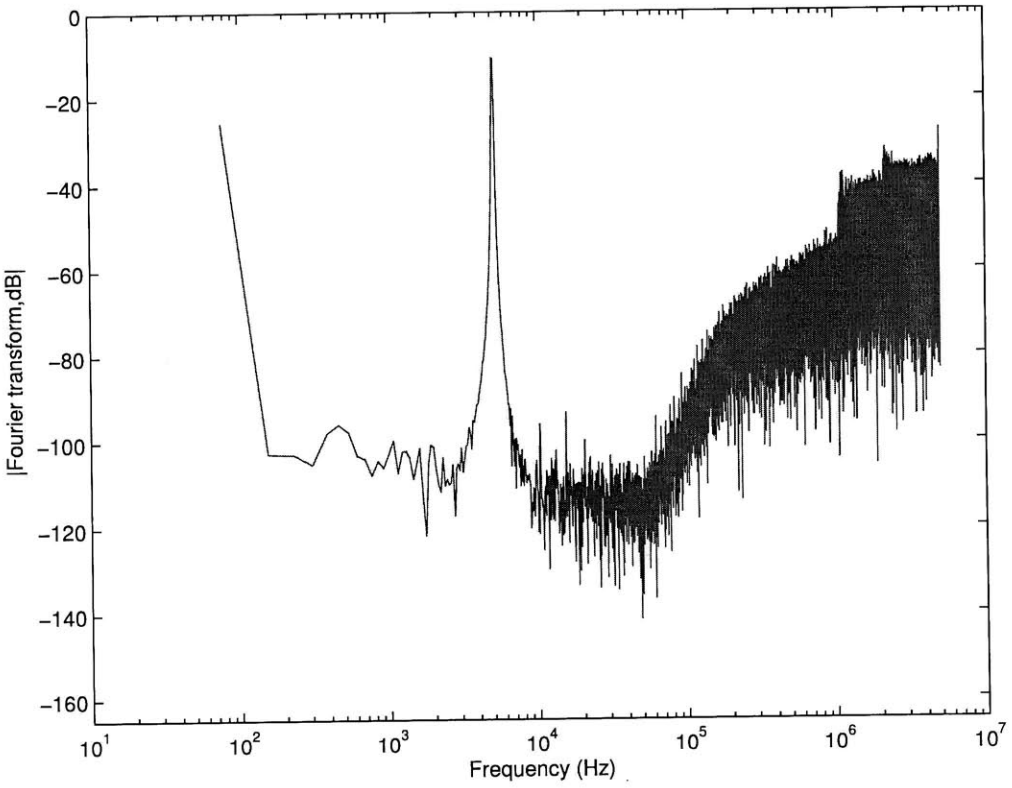


Figure 7-16: Measured FFT of implemented modulator, for input of ± 800 mV differential at 5 kHz, $N = 2^{17}$ points. Hann window.

Table 7.4 summarizes the performance of the fabricated chip. Figure of merit (FOM) [45][46] is

$$\text{FOM} = \frac{P}{2\, f_B\, 2^{\text{ENOB}}}, \tag{7.36}$$

where P is power, f_B is the signal bandwidth, and ENOB is the effective number of

Table 7.4: ADC Chip Performance Summary

Specification	**Value**		**Units**
technology	130		nm std. CMOS
ADC area	1.4		mm^2
supply voltage, V_{DD}	1		V
supply voltage, minimal	850		mV
sampling frequency	10		MHz
power, analog	798		μW
power, digital	388		μW
input amplitude	$\pm$ 800		mV, differential
input frequency	5		kHz
bandwidth	20	60	kHz
peak SNDR	75.6	73.0	dB
FOM	5.85	2.63	pJ/step

bits as taken from Eq. 7.5

$$ENOB = \frac{SNDR_{dB} - 1.76 \text{ dB}}{6.02 \text{ dB/bit}}, \tag{7.37}$$

where SNDR_{dB} = signal-to-noise-and-distortion ratio in dB.

7.6.1 Supply Voltage for Optimal Power

Ch. 3 motivated the need for low-voltage analog design by considering a mixed-signal system with a shared supply voltage where the total power consumption is dominated by digital circuits. Because the presented ADC topology contains both analog and digital circuits, it is worth finding the supply voltage at which power consumption is minimized for the same ADC resolution and bandwidth. A simplified analysis can be done with the following assumptions:

- Signal power is proportional to V_{DD}^2, according to Eq. 7.2.
- ADC resolution is dominated by the thermal noise of the analog circuits[17]. The gate-referred power spectral density for the thermal noise of a MOSFET

[17]This assumption assumes that the ADC performance is not limited by issues such as the interconnect problem of Sec. 7.8.1.

is proportional to $1/g_m$. Thus, assuming no change in noise bandwidth, to maintain SNR as signal power changes with V_{DD}, g_m must be proportional to $1/V_{DD}^2$. Assuming that transistor widths are scaled to maintain current density, g_m/I_D is constant, and so total analog current, I_{ana}, is also proportional to $1/V_{DD}^2$. Analog power, P_{ana}, is equal to $V_{DD}\, I_{ana}$ and thus is proportional to $1/V_{DD}$. Thus, analog power decreases with increased V_{DD}.

- Digital power, P_{dig}, is proportional to V_{DD}^2. Thus, digital power increases with increased V_{DD}. It is assumed that the speed of the digital circuits does not affect ADC operation, although this is not a valid assumption for lower values of V_{DD}.

With these assumptions, and given the measurements for analog and digital power of the ADC at $V_{DD} = 1$ V from Table 7.4, the total power consumption of the ADC is

$$\begin{aligned} P_{tot} &= P_{ana} + P_{dig} \\ &= \frac{798\mu W\, 1V}{V_{DD}} + \frac{388\mu W\, V_{DD}^2}{(1V)^2}. \end{aligned}$$

This power consumption reaches a minimum where

$$\begin{aligned} \frac{dP_{tot}}{dV_{DD}} &= \frac{-798\mu W\, 1V}{V_{DD}^2} + \frac{2\,(388\mu W)\, V_{DD}}{(1V)^2} \\ &= 0, \end{aligned}$$

which is satisfied for

$$\begin{aligned} V_{DD,opt}^3 &= \frac{798\mu W\,(1V)^3}{2\,(388\mu W)} \\ V_{DD,opt} &= \sqrt[3]{\frac{798\mu W\,(1V)^3}{2\,(388\mu W)}} \approx 1V. \end{aligned}$$

Thus, the discussed ADC topology was implemented at the supply voltage corresponding with minimum total power. Above this optimum supply voltage, total power consumption increases due to the digital circuits. Below the optimum supply voltage, total power consumption increases due to the requirements of the analog circuits.

7.7 Comparison With Other References

Table 7.5 compares the performance of this work with other low-voltage delta-sigma ADCs.

Table 7.5: Low-Voltage Delta-Sigma ADC Performance Comparison

Authors	**Publication**	**FOM** (pJ/step)	**Topology**	**BW** (khz)	**SNDR** (dB)
this work	'10	2.5	LV-ZCB	60	73
Musah [8]	CICC'09	1.9	ZCB switched-resistor	833	48
Chae [31]	JSSC'09	0.3	inverter	8	63
		0.1		20	81
Sauerbrey [37]	ESSCIRC'06	7.9	switched-opamp	312	65
Ahn [7]	JSSC'05	2.7	switched-RC	20	81
Wang [47]	JSSC'03	56.7	unity-gain reset opamp	25	61
Sauerbrey [36]	JSSC'02	2.7	switched-opamp	8	67
Cheung [48]	JSSC'02	287.8	switched-opamp	200	42
Keskin [35]	JSSC'02	22.1	unity-gain reset opamp	20	78
Peluso [19]	JSSC'98	1.2	switched-opamp	16	62

The work presented in [8] is a 2nd-order delta-sigma with less than 8-bit ENOB. Bootstrapped switches were used to ensure low switch resistance.

The work presented in [31] is a ZCB circuit that uses an inverter instead of a crossing detector. Thus the performance is highly dependent on the power supply voltages $V_{DD} - V_{SS}$. Clock-boosting is used to ensure low switch resistance.

The work presented in [47] is a bandpass delta-sigma. Note that, compared to a lowpass modulator, a bandpass modulator requires double the loop filter order for the same order of noise-shaping [21].

The work presented in [48] is also a bandpass delta-sigma.

The work presented in [19] is a third-order delta-sigma that shares one of the same authors as the original switched-opamp paper [5]. In this ADC, the input range is decreased so that a series NMOS switch can be used at the input of the first integrator.

7.8 Limitation of Performance

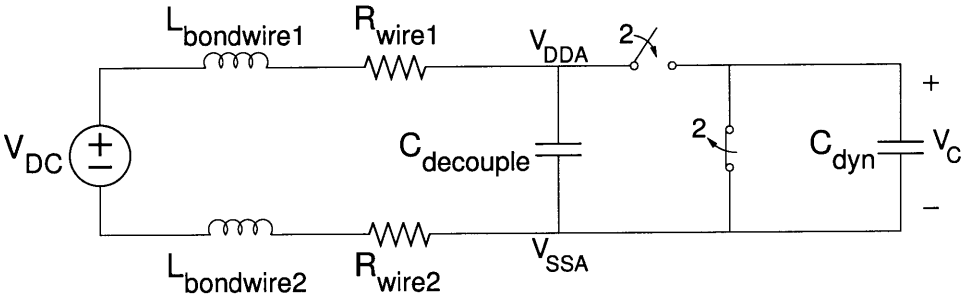
7.8.1 DAC Error Due to Power Supply Noise

The performance of the fabricated chip was limited by an interconnect oversight - a shared on-chip connection between the analog power supply and DAC reference voltages. Although the DAC reference voltages were intended to be the same voltage as the power supply voltages, they should be connected off-chip through separate pins rather than connected on-chip and using shared pins. If the DAC reference voltages are tied on-chip to the power supply voltages, then any fluctuation in the power supply voltages shows up as a DAC error. From Eq. 5.11, it is clear that errors in the DAC voltage, $V_{DAC} - V_{DACb}$, are indistinguishable from fluctuations at the input of the ADC. Thus the performance of the fabricated chip does not correspond with the performance limit or simulated results of the proposed design.

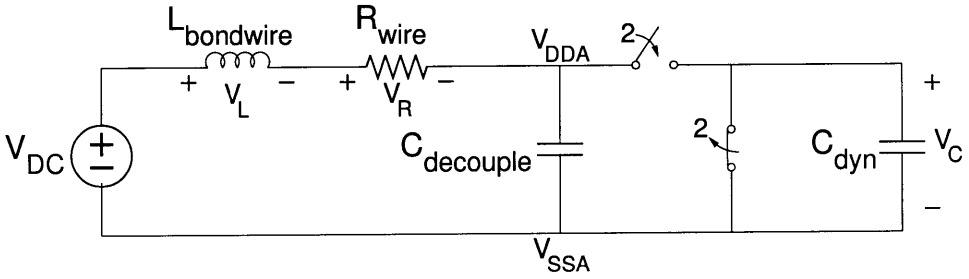
Power Supply Noise Model

To investigate the effect of this interconnect problem, a model of the external power supply, bondwire inductance, on-chip wiring resistance, decoupling capacitance, and the capacitive load corresponding with the dynamic power portion of the ADC is shown in Fig. 7-17(a). Capacitor $C_{decouple}$ represents the on-chip decoupling (bypass) capacitance[18] between the analog power supply voltages, V_{DDA} and V_{SSA}. Capacitor C_{dyn} models the dynamic power consumption of the delta-sigma ADC as a capacitor that is charged from V_{SSA} to V_{DDA} at the start of the first integrator's charge-transfer

[18]For simplicity, decoupling capacitors between node V_{SSA} and multiple off-chip reference voltages such as V_{REFH} have been neglected. These capacitors would effectively add additional RLC series paths in parallel with $L_{bondwire2}$ and R_{wire2}.



(a) Power supply model



(b) Simplified power supply model

Figure 7-17: Model of power supply, bondwire inductances, on-chip wiring resistance, decoupling capacitance, and ADC load capacitance.

phase, ϕ_2. Inductor $L_{bondwire1}$ and resistor R_{wire1} represent the bondwire inductance and on-chip wiring resistance from the external power supply to the analog power supply voltage V_{DDA}. Inductor $L_{bondwire2}$ and resistor R_{wire2} represent the bondwire inductance and on-chip wiring resistance from the power supply to the analog power supply voltage V_{SSA}. The model is further simplified in Fig. 7-17(b), where the series inductances and resistances have been combined.

The value for $C_{decouple}$ is taken from the process design kit to be 6 capacitor arrays * 24pF/array = 144 pF. The value for inductance, $L_{bondwire}$ is estimated using the 1nm/mm rule-of-thumb to be roughly $L_{bondwire}$ = 2nH total. The value for R_{wire} is estimated by counting squares of on-chip wiring on the layout and multipying by the resistance per square as given by the process design manual.

$$\begin{aligned} R_{wire1} &= 20 \text{ squares} * 0.0339\,\Omega/\text{square} = 0.678\,\Omega \\ R_{wire2} &= 73 \text{ squares} * 0.0339\,\Omega/\text{square} = 2.5\,\Omega \\ R_{wire} &= R_{wire1} + R_{wire2} = 3.178\,\Omega. \end{aligned}$$

The value for C_{dyn} is estimated from the dynamic power of the ADC. The analog power of the chip is 775μW at 10 MHz and 487μA at 5 MHz.[19] Dynamic power is proportional to CV^2f, but static power does not vary with clock frequency. Thus, the dynamic power at 10 MHz can be found by solving the following system of equations:

$$\begin{aligned} P_{dyn}(10 \text{ MHz}) + P_{stat} &= 775\mu W \\ P_{dyn}(5 \text{ MHz}) + P_{stat} &= 487\mu W \\ P_{dyn}(5 \text{ MHz}) &= \frac{1}{2}P_{dyn}(10 \text{ MHz}), \end{aligned}$$

where $P_{dyn}(10 \text{ MHz})$ is the dynamic power dissipation at 10 MHz and P_{stat} is the static power dissipation from the analog power supply. Solving for $P_{dyn}(10 \text{ MHz})$

[19]The analog power for 5 MHz has been corrected to account for a slight change in bias currents.

gives

$$\begin{aligned} P_{dyn}(10\text{ MHz}) &= 2(775\mu W - 487\mu W) \\ &= 576\mu W. \end{aligned}$$

We make the approximation that the dynamic power dissipation is evenly divided between each clock phase. Given that the power supply voltage, $V_{DC} = V_{DDA} - V_{SSA}$ = 1V, the dynamic capacitance, C_{dyn} can be estimated to be

$$\begin{aligned} C_{dyn}(V_{DDA} - V_{SSA})^2 f &= \frac{P_{dyn}(10\text{ MHz})}{2} \\ C_{dyn} &= \frac{P_{dyn}(10\text{ MHz})}{2(V_{DDA} - V_{SSA})^2 f} \\ &= \frac{576\mu W}{2(1V)^2 10\text{MHz}} \\ &= 28.8pF. \end{aligned}$$

Since this is only a rough approximation, we round down to C_{dyn} = 24 pF to simplify the later math.

Near the beginning of the first integrator's charge-transfer phase, ϕ_2, the capacitor C_{dyn}, which was previously discharged, is placed in parallel with capacitor $C_{decouple}$, which was previously charged to $V_{DC} = V_{DDA} - V_{SSA}$. As charge is shared between the two capacitors, the starting voltage across the capacitors in parallel becomes

$$\begin{aligned} V_C(0^+) &= \frac{Q_{decouple}(0_-) + Q_{dyn}(0_-)}{C_{decouple} + C_{dyn}} \\ &= \frac{(V_{DDA} - V_{SSA})C_{decouple} + 0\,C_{dyn}}{C_{decouple} + C_{dyn}} \\ &= \frac{1V\ 144pF}{144pF + 24pF} \\ &= 6/7V. \end{aligned} \tag{7.38}$$

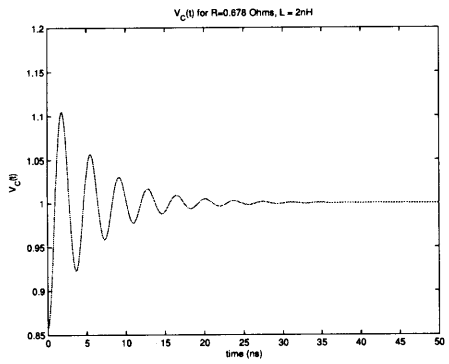
The voltage across a series RLC circuit is [49]

$$\begin{aligned} V_{DC}\,u(t) &= V_L(t) + V_R(t) + V_C(t) \\ &= L\frac{di(t)}{dt} + Ri(t) + \frac{\int_{0^+}^{t} i(t)\,dt + q(0^+)}{C}, \end{aligned}$$

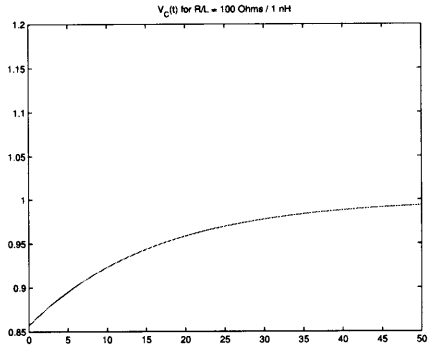
for all t, where u(t) is the unit step function, i(t) is the current through the circuit, and q(t) is the charge on capacitor C at time t. Using the stated values for V_{DC}, $L = L_{bondwire}$, $R = R_{wire}$, $C = C_{decouple} + C_{dyn}$, and $V_C(0^+)$ to solve this differential equation,[20]

$$V_C(t) = 1V - \frac{1}{7}e^{-\frac{Rt}{2L}}\left[\cos(\omega_o t) + \left(\frac{R}{\omega_o 2L}\right)\sin(\omega_o t)\right] \tag{7.39}$$

This equation represents the fluctuation of the on-chip analog power supply voltages due to the dynamic power dissipation. As can be seen from Eq. 7.39, the form of this fluctuation is a sinusoid inside an exponentially decaying envelope, an example of which can be seen in Fig. 7-18(a). Fig. 7-18(b) illustrates the effect of a disturbance



(a) $R_{wire} = 0.678\ \Omega$, $L_{bondwire} = 2$nH (underdamped).



(b) $R_{wire} = 100\ \Omega$, $L_{bondwire} = 1$nH (overdamped).

Figure 7-18: Transient of on-chip analog power supply voltage in response to dynamic disturbance.

to the power supply voltage for a higher value of R/L.

[20]For in-depth details of this derivation, see App. B.

Instant of Sampling

For the differential LV-ZCB integrator of Fig. 5-8, the charge-transfer phase, ϕ_2, consists of a preset, a coarse charge-transfer, and a fine charge-transfer, after which the voltage on the integration capacitors, C_{FB}, is sampled. From Fig. 4-8, which demonstrates the transient response of a single-ended ZCB integrator, it can be seen that the duration of the coarse charge-transfer, t_{coarse}, is output dependent, a property which also holds for the differential LV-ZCB integrator. In contrast, if the delay of the coarse crossing detector is constant, and the slope of the output voltage during the coarse and fine charge-transfers is constant, then the duration of the fine charge-transfer, t_{fine}, is constant from cycle-to-cycle.

At a clock frequency of 10 MHz, a clock period is 100 ns. For each 50 ns half-cycle, we approximate the coarse charge-transfer time as being in the range $t_{coarse} \in [0, 13 \text{ ns}]$ (depending on the output voltage), and approximate the fine charge-transfer time as $t_{fine} = 30$ ns (constant). We assume that the disturbance on the power supply voltage occurs each cycle during the preset of ϕ_2 and, for simplicity, set this time to be t = 0. Assuming that the coarse overshoot is small, then the differential integrator output voltage at the end of the coarse charge-transfer is approximately equal to the differential output voltage at the end of the fine charge-transfer:

$$V_{outp}(t_{coarse} + t_{fine}) - V_{outn}(t_{coarse} + t_{fine}) \approx V_{outp}(t_{coarse}) - V_{outn}(t_{coarse}). \quad (7.40)$$

Using these approximations, we can solve for sampling time as a function of the final integrator output voltage, $V_{outp}(t_{coarse} + t_{fine}) - V_{outn}(t_{coarse} + t_{fine})$:[21]

$$\begin{aligned} t &= t_{fine} + t_{coarse} \\ &\approx 30ns + \{(V_{DD} - V_{SS}) - [V_{outp}(t_{fine} + t_{coarse}) - V_{outn}(t_{fine} + t_{coarse})]\} \left[\frac{13ns}{2(V_{DD} - V_{SS})}\right]. \end{aligned} \quad (7.41)$$

This value for time, t, can be substituted into Eq. 7.39 to find the error on the DAC

[21] For in-depth details of this derivation, see App. B.

reference voltages at the moment the voltage on the integration capacitors, C_{FB}, is sampled[22].

Simulink Model Incorporating DAC Noise

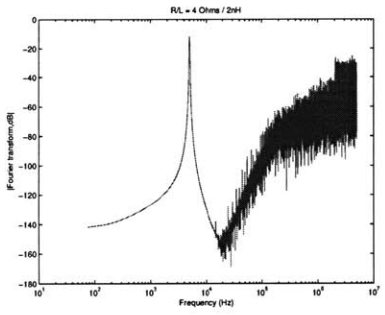
Using the result of Eq. 7.41 in Eq. 7.39, the effect on the delta-sigma modulator of the error of the DAC reference voltages was simulated in Simulink for various values of $R = R_{wire}$ and $L = L_{bondwire}$. The results of these simulations can be seen in Fig. 7-19.

Fig. 7-19(a) shows an ideal FFT, which represents the bitstream output of the ADC without any DAC noise.

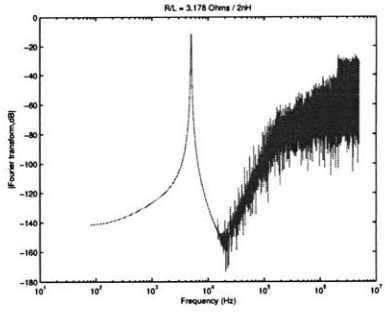
Fig. 7-19(b) shows the FFT for the estimated values of $R = R_{wire} = 3.178\Omega$ and $L = L_{bondwire} = 2nH$. The simulation does not show a significant increase in noise for these values. However, noise performance deteriorates drastically for only a slight decrease in the ratio of R/L. For example, if R_{wire2}, the series resistance from the power supply to V_{SSA}, is ignored, then power supply noise limits the SNDR of the ADC to 86 dB (14-bit ENOB), as seen in Fig. 7-19(c). If $L_{bondwire}$ is also doubled, the SNDR drops to 61 dB (less than 10-bit ENOB), as seen in Fig. 7-19(d). Because the values estimated for R and L are only rough approximations, and because the noise performance is highly sensitive to these values, it is strongly possible that DAC noise resulting from an interconnect oversight explains the high noise floor in the measured FFT of the implemented chip (Fig. 7-16). Also, this simple RLC model for the power supply assumes that the voltage fluctuations only occur during the preset and are identical from cycle-to-cycle; it is unlikely that the actual on-chip power supply voltage fluctuations are as ideally distributed.

Because the effect of DAC noise depends so strongly on the R/L ratio, one method to improve the performance of the fabricated ADC might be to add a small tunable resistor in series between the external power supply and the analog power supply pins, adjusting the value to minimize the effect of DAC noise.

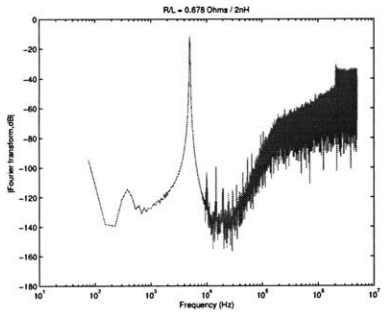
[22]An approximation has been made that the fluctuation of the power supply voltage, $V_C(t)$, is small, such that it does not recursively affect the time, t, to be substituted into Eq. 7.39.



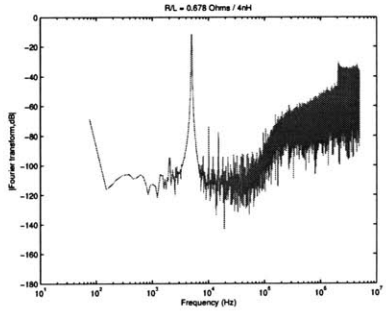
(a) Ideal (no DAC error).



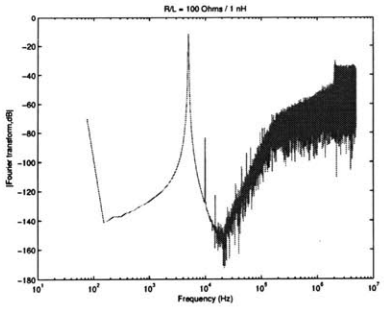
(b) R = 3.178Ω, L = 2nH (estimated from chip layout). SNDR = 115 dB. SNR = 115 dB.



(c) R = 0.678 Ω, L = 2nH. SNDR = 86 dB. SNR = 97 dB.



(d) R = 0.678Ω, L = 4nH. SNDR = 61 dB. SNR = 72 dB.



(e) R = 100Ω, L = 1nH. SNDR = 73 dB

Figure 7-19: FFT showing effect of power supply / DAC coupling error as simulated in Simulink. V_{in} = 588 mV differential at 5 kHz, $N = 2^{17}$ points. Hann window.

The way that power supply disturbances affect the output spectrum depends on the resonance frequency of the system. The damped resonance frequency of the RLC system (derived in Eq. B.3) for the estimated values of R, L, and C is

$$\begin{aligned}
\omega_o &= \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \\
&= \sqrt{\frac{1}{L_{bondwire}(C_{decouple} + C_{dyn})} - \left(\frac{R_{wire}}{2L_{bondwire}}\right)^2} \\
&= \sqrt{\frac{1}{2nH(144pF + 24pF)} - \left(\frac{3.178\Omega}{4nH}\right)^2} \\
&= 1.53 \text{ nrad/s}
\end{aligned}$$

This corresponds to a period of

$$\begin{aligned}
T_o &= \frac{2\pi}{\omega_o} \\
&= \frac{2\pi}{1.53 \text{ nrad/s}} \\
&= 4.1 \text{ ns}
\end{aligned}$$

For small values of L and C, it is clear that multiple periods of resonance occur during the coarse charge-transfer phase (for which 13 ns is allocated). If the system is also underdamped, as in the cases of Fig. 7-19(c) and Fig. 7-19(d), then $V_C(t)$, and therefore the error introduced by the DAC, is not strongly correlated with the output voltage of the first integrator. Thus the DAC error raises the white noise floor. In contrast, for the overdamped case, where the power supply voltage fluctuation decays monotonically, the error is correlated with the output voltage of the integrator, resulting in harmonic distortion, as seen in the FFT of Fig. 7-19(e).

During testing of the fabricated chip, it could be seen that the voltage / current parameter that most strongly lowered the noise floor was a decrease in I_{fine} for the first integrator. A decrease in I_{fine} decreases the slope of the fine charge-transfer and therefore increases t_{fine} in Eq. 7.41. According to the model presented for the effects of power supply noise (see Eq. 7.39), increasing t_{fine} results in a later sampling, giving

the oscillation of the power supply voltages more time to settle. Thus, the observation of the effect of I_{fine} on the noise floor corresponds with the presented model.

7.8.2 Distortion of Resistor-Switch Ladder

Another limitation of the performance of the fabricated chip came from the resistor-switch ladder (Fig. 5-3) used to sample the input voltage of the ADC.

The settling time constant for the resistor-switch ladder is

$$\begin{aligned} \tau &= RC \\ &= (R_{IN1} + R_{IN2})C_{IN} \\ &= (9336\Omega + 495\Omega)1pF \\ &= 9.831 \text{ ns} \end{aligned}$$

For a 10 MHz clock frequency, the duration of the sampling phase, ϕ_1, is 50 ns, which means that the sampled signal settles for over 5 time constants. The attenuation according to Eq. 4.8 is

$$\begin{aligned} & 1 - e^{\left(\frac{-1}{2f_s R_{IN} C_{IN}}\right)} \\ = \; & 1 - e^{\left(\frac{-1}{2(10MHz)9.83ns}\right)} \\ = \; & 0.9938, \end{aligned}$$

which should not be a problem for the ADC. However, the effect of incomplete settling indicated in Eq. 4.8, assumes a constant value for C_{IN}, resulting in a constant attenuation of the input signal.

In the implemented chip, the attenuation seen at a clock frequency of 10 MHz was 0.735, indicating a discrepancy between the predicted values for R_{IN} and C_{IN} and the fabricated values.

The effect of nonlinear parasitic capacitance in the resistor-switch ladder is harmonic distortion. An FFT of the sampled signal as simulated in Cadence for the implemented values of C_{IN} and R_{IN} is shown in Fig. 7-20. As seen in Fig. 7-20,

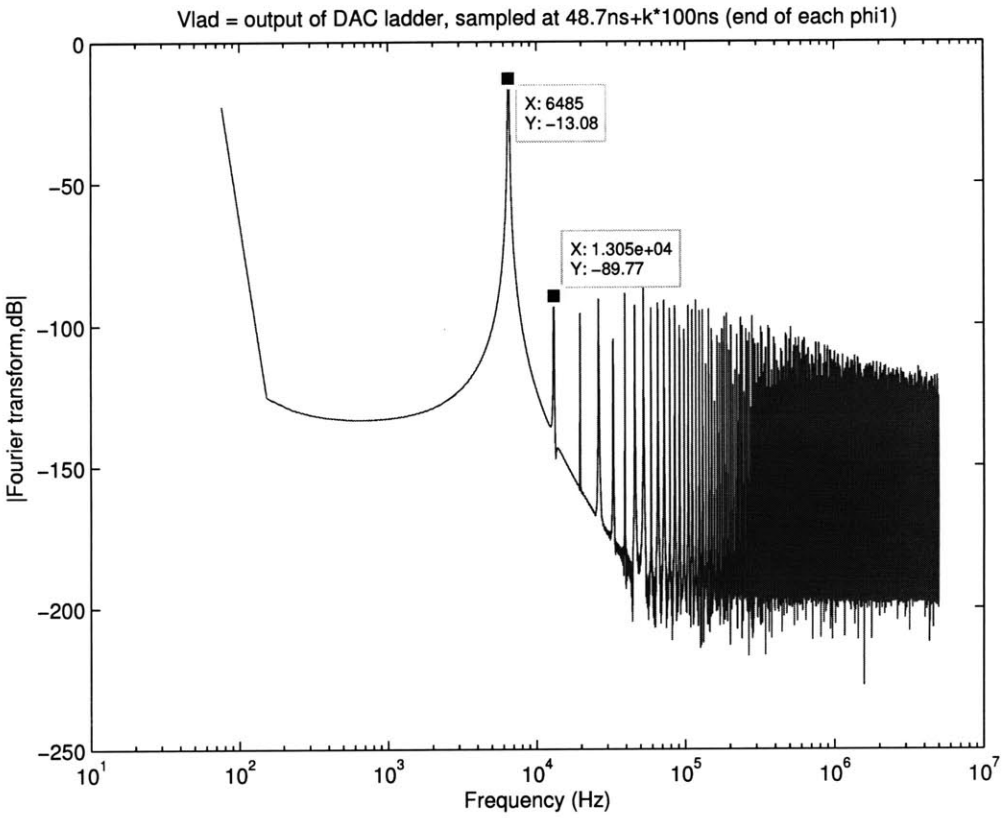


Figure 7-20: FFT of sinusoid sampled by resistor-switch ladder as simulated in Cadence. V_{in} = 500 mV differential at 6.5104 kHz, $N = 2^{17}$ points. Hann window. SFDR = 77 dB.

the nonlinear settling of the input voltage on C_{IN} limits spurious-free dynamic range (SFDR), and therefore SNDR.

Because the effects of finite settling are decreased by a longer settling time, the distortion due to parasitic capacitance in the resistor-switch ladder can be decreased by lowering the clock frequency.

It is important to note that the resistor-switch ladder is not a requisite component of a LV-ZCB circuit, but is only required when the circuit is not preceeded by a stage with an output that can be disabled. This same requirement is also true for switched-opamp circuits.

Chapter 8

Conclusion

8.1 Thesis Contributions

In this project, a technique for designing differential low-voltage ZCB circuits that do not require gate boosting was created, using elements from both the switched-opamp and ZCB techniques. The fabricated chip represents the first implementation of a voltage ramp generator to linearize the charge-transfer ramp in the presence of a changing load. The correlated level-shifting technique was developed and the effect on ZCB circuits was shown to effectively increase the output impedance of the gated current sources while simultaneously reducing the output swing requirement. In a ZCB circuit, this linearity benefit can also be traded off for a longer crossing detector integration time, which can be used to lower thermal noise, or to decrease power consumption.

The LV-ZCB concept was demonstrated with a 4th-order delta-sigma modulator for audio applications. In designing a delta-sigma methodulator with LV-ZCB integrators, the effect of ZCB overshoot and crossing detector delay was analyzed, and the results were compared to the offset and finite DC gain limitations encountered in traditional opamp-based designs. Also, a method for summing asynchronous ZCB signals was created, allowing the creation of delta-sigma modulators with higher-order feedforward loop filters implemented using ZCB circuits. This method does not require extra ZCB stages and can function under the time-constraints of ZCB

circuits.

8.2 Future Work

As shown in Ch. 5, for the LV-ZCB integrator, the preset of the output voltage at the start of the charge-transfer phase significantly limits the choice of virtual ground reference voltages and the allowable common-mode range at the input of the integrator. In a ZCB circuit, the purpose of presetting V_{outp} and V_{outn} to voltage extremes (V_{DD} and V_{SS}) is to ensure that they are beyond the range of possible output voltages at the start of the charge-transfer phase, so that the virtual ground condition will be met at some point during the charge-transfer ramps. However, for an integrator with a gain, $C_{IN}/C_{FB} < 1$ (as is true for all the integrators of the implemented modulator, as seen in c1..c4 of Table 7.1), the range of possible output values in any given cycle is less than full-scale and depends on the output voltage of the previous cycle.

One way to reduce the preset limitation for a LV-ZCB integrator would be to do an "intelligent" preset, where a different preset voltage is chosen based on the output voltage of the previous cycle. It would be a challenge to implement this customized preset under low power supply voltages due to the limited range of preset voltages that can be conducted by switches.

For switched-capacitor integrators with very low gain, the possible change in output voltage from cycle-to-cycle is very small. Thus, for ZCB circuits that use multiple ramps in each charge-transfer phase, it may be faster to skip the preset phase altogether and to replace it with an extra charge-transfer ramp. Note that, without the preset to reset the common-mode level at the output each cycle, common-mode feedback circuitry would have to be implemented.

Glossary

ADC Analog-to-Digital Converter

back-end-of-line a.k.a. BEOL. The phase of integrated circuit fabrication in which metal interconnect wires are created.

channel length modulation The decrease in MOSFET inversion channel length due to an increase in drain voltage, leading to increased drain current.

cascode A series combination of common-source and common-gate amplifiers. The common-gate transistor serves as a current buffer to the common-source transistor, isolating the common-source drain from the output voltage and effectively increasing the output impedance of the amplifier.

CBSC Comparator-Based Switched Capacitor

CMOS Complementary (n-channel & p-channel) Metal-Oxide-Semiconductor

CMOS scaling The decrease in feature size seen in each generation of CMOS integrated circuits. Scaling results in increased speed and power efficiency for digital circuits, but requires more power and often topological changes to maintain performance in analog circuits.

device voltage gain a.k.a. intrinsic gain = $g_m r_o = g_m / g_{ds}$

digitally-controlled current source A current source that is either fully on or fully off depending on the value of a digital control input.

ENOB Effective number of bits. $(SNDR_{dB} - 1.76)/6.02$.

FOM Figure Of Merit. (analog + digital power) / (2*bandwidth * 2^{ENOB})

f_B signal bandwidth.

f_s sampling frequency. For Nyquist sampling, $f_s = 2f_B$.

g Integrator gain coefficient. Not the same as DC gain of the integrator, which is the value of the integrator transfer function for z=1.

gate overdrive voltage $V_{gs} - V_t$

ground a constant reference voltage which may be equal to V_{SS}

I_{coarse} gated current source current for coarse (first-pass) charge-transfer phase

I_{fine} gated current source current for fine (second-pass) charge-transfer phase

k Boltmann's constant = 1.38 x 10^{-23} J/K

mid-level voltage $(V_{DD} + V_{SS})/2$

mid-range voltages voltages close to mid-level voltage

NTF Noise Transfer Function. Gain of quantization noise from quantizer to modulator output.

opamp operational amplifier

OSR OverSampling Ratio = $f_s/(2f_B)$.

pole (as opposed to zero) value of a variable which causes the denominator of an equation to go to ∞.

q charge of an electron = 1.6 x 10^{-19} C

SFDR Spurious-Free Dynamic Range. Ratio of signal to largest distortion harmonic.

SNDR, a.k.a. SINAD Signal-to-Noise-and-Distortion Ratio. Ratio of signal power to the power of noise plus distortion. Used to determine the effective number of bits (ENOB) for an analog-to-digital converter.

STF Signal Transfer Function. Gain of signal from modulator input to modulator output.

t_d propagation time. The portion of crossing-detector delay after the voltage at the output of the preamplifier passes a specified threshold.

t_{delay} Crossing-detector delay. $t_{delay} = t_d + t_i$

t_i integration response time. The portion of crossing-detector delay before the voltage at the output of the preamplifier passes a specified threshold.

V_{CM} virtual ground reference voltage, usually corresponding to the mid-level voltage

V_{DD} maximum power supply voltage

$V_{in,cm}$ common-mode signal at the input to a differential circuit

V_{REF} voltage that controls the reference level at the input of an integrator

V_{REFL} a contant reference voltage that is approximately equal to V_{SS}

$\mathbf{V}_{\mathrm{REFH}}$ a contant reference voltage that is approximately equal to V_{DD}

V_{SS} minimum power supply voltage. Equivalent to ground in a single-supply circuit.

V_t threshold voltage

V_{tn} NMOS threshold voltage. When $V_{gs} \geq V_{tn}$, a NMOS switch turns on.

V_{tp} PMOS threshold voltage. When $V_{sg} \geq |V_{tp}|$, a PMOS switch turns on.

V_T thermal voltage = kT/q = 25.85 mV @ 300 K

virtual ground When an opamp uses negative feedback to force the voltage at its inverting input to be equal to the voltage at its noninverting input such that the inverting input node acts as a constant voltage supply.

V_X Virtual ground node in a single-ended circuit.

$V_{X,cm}$ common-mode signal on virtual ground nodes V_{Xp} and V_{Xn} in a differential circuit.

V_{Xn} virtual ground node for the negative signal path in a differential circuit.

V_{Xp} virtual ground node for the positive signal path in a differential circuit.

white noise noise whose power is constant across all frequencies

ZCBC Zero-Crossing-Based Circuits

zero (as opposed to a pole) value of a variable which causes the numerator of an equation to go to ∞.

Appendix A

Extended Equation Derivations

Eq. 6.9:

$$
\begin{aligned}
\overline{v_{in,N}^2} &= \int_0^{f_B} S_N \left|\frac{X(z)}{N(z)}\right|^2 df \\
&= \int_0^{f_B} S_N \left[\frac{2}{g}\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \\
&= S_N \int_0^{f_B} \frac{4}{g^2}\sin^2\left(\frac{\pi f}{f_s}\right) df \\
&= \frac{S_N}{g^2}\int_0^{f_B} 4\left[\frac{1-cos\left(\frac{2\pi f}{f_s}\right)}{2}\right] df \\
&= \frac{S_N}{g^2}\left[2f - 2\left(\frac{f_s}{2\pi}\right)\sin\left(\frac{2\pi f}{f_s}\right)\right]\Bigg|_{f=0}^{f_B} \\
&= \frac{S_N}{g^2}\left[2f_B - \left(\frac{f_s}{\pi}\right)\sin\left(\frac{2\pi f_B}{f_s}\right)\right] \\
&= \frac{S_N}{g^2}\left[\frac{fs}{\mathrm{OSR}} - \left(\frac{f_s}{\pi}\right)\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\right].
\end{aligned}
$$

Eq. 7.2:

$$\begin{aligned}
\overline{V_{sin}^2} &= \frac{1}{f}\int_0^{1/f} |\frac{A}{2}\sin(2\pi f t)|^2\, dt \\
&= \frac{(A/2)^2 f}{(2\pi f)}\int_0^{2\pi} \sin^2 x\, dx \\
&= \frac{A^2}{8\pi}\int_0^{2\pi} \frac{1-cos(2x)}{2}\, dx \\
&= \frac{A^2}{8\pi}\left(\frac{x}{2} - \frac{sin2x}{4}\right)\Big|_0^{2\pi} \\
&= \frac{A^2}{8\pi}\left(\frac{2\pi}{2} - 0\right) \\
&= \frac{A^2}{8},
\end{aligned}$$

Eq. 7.6:

$$\begin{aligned}
\overline{V_C^2} &= \int_0^{\infty} 4kTR\left|\frac{1}{sCR+1}\right|^2 df \\
&= \int_0^{\infty} \frac{4kTR}{(2\pi fCR)^2 + 1^2}\, df \\
&= 4kTR\int_0^{\infty} \frac{1}{(2\pi fCR)^2 + 1^2}\, df \\
&= \frac{4kTR}{2\pi CR}\int_{2\pi 0 CR}^{2\pi\infty CR} \frac{1}{x^2+1}\, dx \\
&= \frac{2kT}{\pi C} tan^{-1}x|_0^{\infty} \\
&= \frac{2kT}{\pi C}(\frac{\pi}{2} - 0) \\
&= \frac{kT}{C}.
\end{aligned}$$

Eq. 7.13:

We use the trigonometric substitution

$$\begin{aligned} 2\pi f R_o C_o &= \tan\theta \\ 2\pi R_o C_o df &= \sec^2\theta d\theta \\ df &= \frac{\sec^2\theta}{2\pi R_o C_o} d\theta \end{aligned}$$

$$\begin{aligned} \overline{V_{in,ampl}^2} &= S_{Vin,ampl,therm} \int_{\tan^{-1}(2\pi 0 R_o C_o)}^{\tan^{-1}(2\pi\infty R_o C_o)} \left(\frac{1}{1+\tan^2\theta}\right)\left(\frac{\sec^2\theta}{2\pi R_o C_o}\right) d\theta \\ &= S_{Vin,ampl,therm} \int_0^{\pi/2} \cos^2\theta \left(\frac{\sec^2\theta}{2\pi R_o C_o}\right) d\theta \\ &= S_{Vin,ampl,therm} \int_0^{\pi/2} \left(\frac{1}{2\pi R_o C_o}\right) d\theta \\ &= S_{Vin,ampl,therm} \left(\frac{1}{2\pi R_o C_o}\right)\left(\frac{\pi}{2}-0\right) \\ &= S_{Vin,ampl,therm} \left(\frac{1}{4R_o C_o}\right) \\ &= S_{Vin,ampl,therm}\, \mathrm{NBW}_{\mathrm{ampl,ss}}. \end{aligned}$$

Appendix B

Extended Derivation for Series RLC Circuit

Eq.7.39:

The voltage across a series RLC circuit is [49]

$$\begin{aligned} V_{DC}\,u(t) &= V_L(t) + V_R(t) + V_C(t) \\ &= L\frac{di(t)}{dt} + Ri(t) + \frac{\int_{0^+}^{t} i(t)\,dt + q(0^+)}{C}, \end{aligned}$$

for all t, where u(t) is the unit step function, i(t) is the current through the circuit, and q(t) is the charge on capacitor C at time t. Taking the derivative of both sides with respect to t, and dividing through by L,

$$\begin{aligned} V_{DC}\,\delta(t) &= L\frac{d^2q(t)}{dt^2} + R\frac{dq(t)}{dt} + \frac{q(t)}{C} \\ \frac{V_{DC}\,\delta(t)}{L} &= \frac{d^2q(t)}{dt^2} + \frac{Rdq(t)}{Ldt} + \frac{q(t)}{LC}, \end{aligned} \tag{B.1}$$

where $\delta(t)$ is the unit impulse function. If the general solution of Eq. B.1 is $q(t) = Ae^{st}$,

then for $t > 0$,

$$\begin{aligned} 0 &= s^2 Ae^{st} + \frac{RsAe^{st}}{L} + \frac{Ae^{st}}{LC} \\ 0 &= s^2 + \frac{Rs}{L} + \frac{1}{LC}, \end{aligned}$$

which has solutions of

$$s = \frac{-\frac{R}{L} \pm \sqrt{\left(\frac{R}{L}\right)^2 - \frac{4}{LC}}}{2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}.$$

Thus

$$\begin{aligned} q(t) &= A_1 e^{s_1 t} + A_2 e^{s_2 t} \\ &= A_1 e^{\left(-\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}\right)t} + A_2 e^{\left(-\frac{R}{2L} - \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}\right)t} \\ &= e^{-\frac{Rt}{2L}} \left(A_1 e^{\left(\sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}\right)t} + A_2 e^{-\left(\sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}\right)t} \right) \\ &= e^{-\frac{Rt}{2L}} \left(A_1 e^{j\left(\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\right)t} + A_2 e^{-j\left(\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\right)t} \right), \end{aligned} \tag{B.2}$$

where A_1 and A_2 are complex numbers. If the term in the square-root, $\frac{1}{LC} - \left(\frac{R}{2L}\right)^2 = 0$, the RLC system is critically damped. For the estimated values for inductance (L = $L_{bondwire}$ = 2 nH) and capacitance (C = $C_{decouple} + C_{dyn}$ = 144pF + 24pF), critical damping occurs for a series resistance of

$$\begin{aligned} \frac{1}{LC} - \left(\frac{R}{2L}\right)^2 &= 0 \\ R &= \sqrt{\frac{4L}{C}} \\ &= \sqrt{\frac{4(2\text{ nH})}{144pF + 24pF}} \\ &= 6.9\,\Omega. \end{aligned}$$

For the estimated value for resistance (R = R_{wire} = 3.178 Ω), the square-root term is greater than zero, and so the RLC system is actually underdamped and therefore

oscillates. We can use Euler's formula, $e^{j\theta} = \cos\theta + j\sin\theta$, and the related identity, $e^{-j\theta} = \cos\theta - j\sin\theta$, to get

$$q(t) = e^{-\frac{Rt}{2L}}\left[(A_1+A_2)\cos\left(t\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right) + j(A_1-A_2)\sin\left(t\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)\right].$$

Knowing that charge, q(t), is real, we know that A_1 and A_2 are complex conjugates, such that $A_1 + A_2$ is real and $A_1 - A_2$ is imaginary. We can thus write the voltage across capacitor C as

$$\begin{aligned} V_C(t) &= \frac{q(t)}{C} \\ &= V_f + e^{-\frac{Rt}{2L}}\left[B_1\cos\left(t\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right) + B_2\sin\left(t\sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}\right)\right] \\ &= V_f + e^{-\frac{Rt}{2L}}[B_1\cos(\omega_o t) + B_2\sin(\omega_o t)] \end{aligned} \tag{B.3}$$

where V_f, B_1, and B_2 are real constants, and $\omega_o = \sqrt{\frac{1}{LC}-\left(\frac{R}{2L}\right)^2}$, is the damped resonance frequency of the system. The solution, V_f, has been added to account for the discontinuity at t = 0.

We solve for V_f of Eq. B.3 using the knowledge that $V_C(\infty) = V_{DC}$:

$$V_C(\infty) = V_f = V_{DC} = 1V. \tag{B.4}$$

We solve for B_1 of Eq. B.3 using Eq. B.4 and the value of $V_C(0^+)$ given in Eq. 7.38:

$$\begin{aligned} V_C(0^+) &= V_f + B_1 \\ B_1 &= V_C(0^+) - V_f \\ &= 6/7 - 1V \\ &= -1/7. \end{aligned} \tag{B.5}$$

Using Eq. B.3, we solve for $i(t) = C\frac{dV_c(t)}{dt}$:

$$\begin{aligned} i(t) &= (C_{decouple} + C_{dyn})\frac{dV_C(t)}{dt} \\ &= (C_{decouple} + C_{dyn}) * \\ &\quad \left\{ \left(\frac{-R}{2L} \right) e^{-\frac{Rt}{2L}} \left[B_1 \cos(\omega_o t) + B_2 \sin(\omega_o t) \right] + e^{-\frac{Rt}{2L}} \omega_o \left[-B_1 \sin(\omega_o t) + B_2 \cos(\omega_o t) \right] \right\}. \end{aligned}$$

We solve for B_2 using the knowledge that $i(0) = 0$:

$$\begin{aligned} i(0) = (C_{decouple} + C_{dyn}) \left[\left(\frac{-R}{2L} \right) B_1 + \omega_o B_2 \right] &= 0 \\ B_2 &= \frac{B_1}{\omega_o} \frac{R}{2L} \\ &= \frac{-1/7}{\omega_o} \frac{R}{2L} \end{aligned} \tag{B.6}$$

Substituting the results of Eq. B.4, Eq. B.5, and Eq. B.6 into Eq. B.3, we get:

$$V_C(t) = 1V - \frac{1}{7} e^{-\frac{Rt}{2L}} \left[\cos(\omega_o t) + \left(\frac{R}{\omega_o 2L} \right) \sin(\omega_o t) \right] \tag{B.7}$$

Eqn 7.41:

During the coarse charge transfer, the differential integrator output voltage is

$$\begin{aligned} V_{outp}(t) - V_{outn}(t) &= V_{preset} - t \left[\frac{2(V_{DD} - V_{SS})}{13ns} \right] \\ &= (V_{DD} - V_{SS}) - t \left[\frac{2(V_{DD} - V_{SS})}{13ns} \right]. \end{aligned} \tag{B.8}$$

Rearranging Eq. B.8 and using the approximation of Eq. 7.40,

$$\begin{aligned} t &= \{(V_{DD} - V_{SS}) - [V_{outp}(t) - V_{outn}(t)]\} \left[\frac{13ns}{2(V_{DD} - V_{SS})}\right] \\ t_{coarse} &= \{(V_{DD} - V_{SS}) - [V_{outp}(t_{coarse}) - V_{outn}(t_{coarse})]\} \left[\frac{13ns}{2(V_{DD} - V_{SS})}\right] \\ &\approx \{(V_{DD} - V_{SS}) - [V_{outp}(t_{coarse} + t_{fine}) - V_{outn}(t_{coarse} + t_{fine})]\} \left[\frac{13ns}{2(V_{DD} - V_{SS})}\right]. \end{aligned} \tag{B.9}$$

The time at which the fine charge-transfer ends and the final voltage is sampled onto the integration capacitors, C_{FB}, is $t = t_{coarse} + t_{fine}$. Using Eq. B.9, we can solve for this time as a function of the final integrator output voltage, $V_{outp}(t_{coarse} + t_{fine}) - V_{outn}(t_{coarse} + t_{fine})$:

$$\begin{aligned} t &= t_{fine} + t_{coarse} \\ &\approx 30ns + \{(V_{DD} - V_{SS}) - [V_{outp}(t_{fine} + t_{coarse}) - V_{outn}(t_{fine} + t_{coarse})]\} \left[\frac{13ns}{2(V_{DD} - V_{SS})}\right]. \end{aligned} \tag{B.10}$$

Appendix C

Rationale for Choosing the Delta-Sigma Topology

Fig. C-1 documents the performance of ADCs presented at the International Solid State Circuits Conference from 1997-2010 and at the Symposium on VLSI Circuits from 1997-2009 [50][1]. The radius of each dot is a function of FOM, which is defined in Eq. 7.36. Larger dots indicate better performance (lower FOM).

Fig. C-2 marks the approximate areas where each ADC topology had the best FOM for a given SNDR and bandwidth. As can be seen in Fig. C-2, for audio band ADCs of 20 kHz bandwidth and 14-bit ENOB ($SNDR_{dB}$ = 86dB), the delta-sigma topology historically has the best FOM.

[1] This ADC data is freely available online.

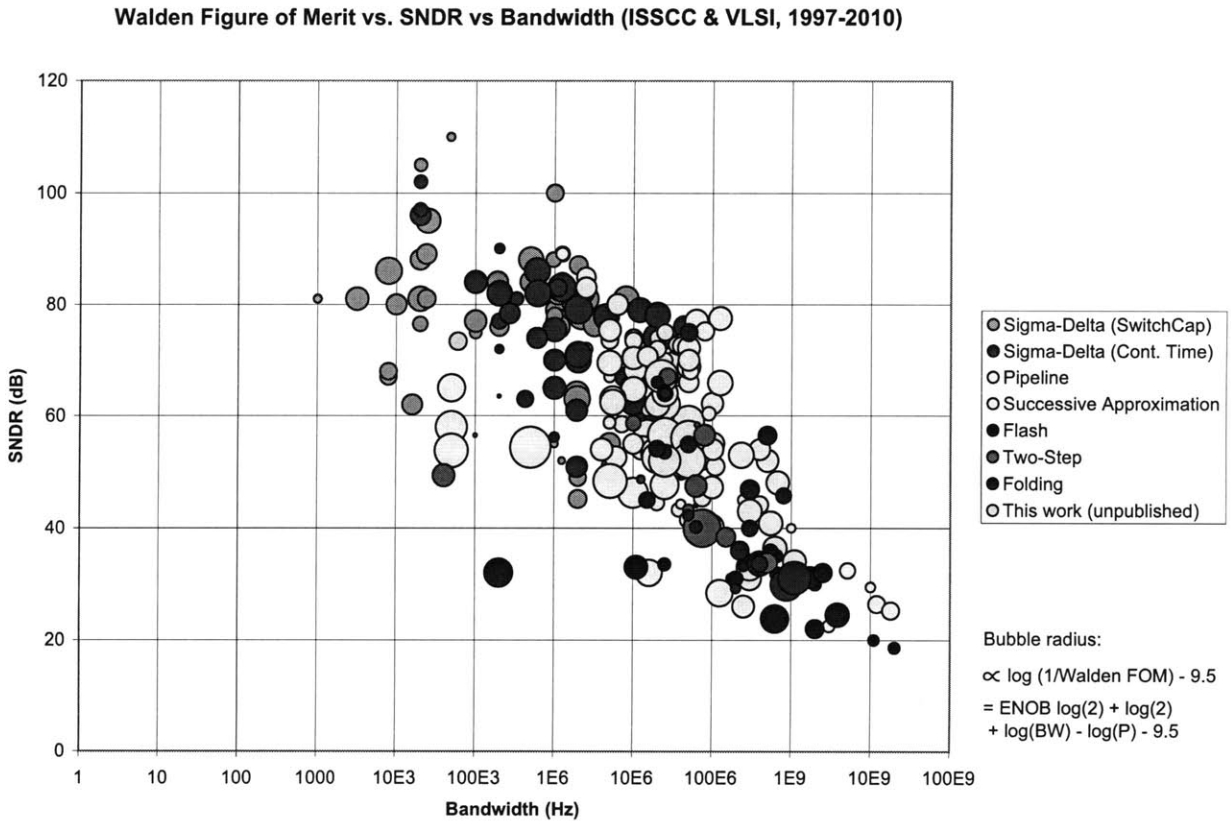


Figure C-1: Chart of ADC papers presented at ISSCC (1997-2010) and VLSI Symposium (1997-2009). Larger bubbles indicate better figure of merit.

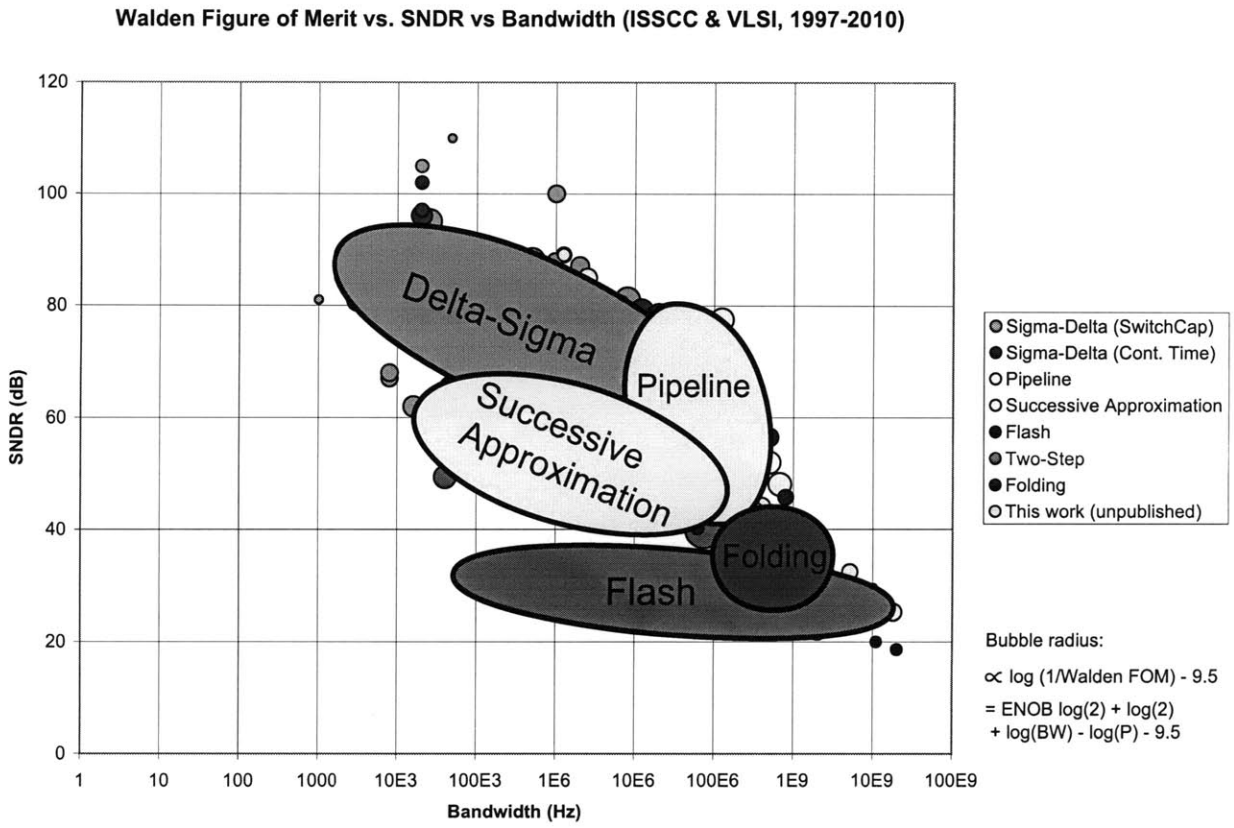


Figure C-2: Chart of ADC papers presented at ISSCC (1997-2010) and VLSI Symposium (1997-2009). Dominant areas for each topology identified.

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