Membrane Technology for the Fabrication of Three-Dimensional Photonic Crystals

by

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Abstract

Three-dimensional photonic crystals hold tremendous promise toward the realization of truly integrated photonic circuits on a single substrate. Nanofabrication techniques currently limit the ability to create the multilayer structure of dielectric materials. Past investigators have approached the problem using the layer-by-layer fabrication method; this method leverages the planar processes that have been developed by the semiconductor industry. Ultimately, the result from this path offered a small area with low yield and exorbitant costs in terms of time and resources.

We introduce large-area membrane stacking as a new approach for three-dimensional nanofabrication. Silicon-nitride membranes are pre-patterned with the two-dimensional photonic crystals. The membranes can then assembled in a serial manner on a substrate to generate the three-dimensional photonic crystal. The efficacy of this method is founded upon the ability to inspect membranes before assembly; it also requires a large yield for stacking.

This thesis is concerned with addressing the key challenges of the membrane-stacking-nanofabrication architecture. We develop a process for generating large-area-silicon-nitride membranes and investigate emerging lithography techniques for patterning them: nanoimprint lithography and coherent diffraction lithography. We demonstrate the ability to reliably bond these membranes to a new substrate. Finally, we address the novel problem of releasing the membrane from its frame. This is accomplished by designing stress-engineered cleavage points that detach the membrane while leaving behind defined edges and a particle-free surface. We will show the stacking of two large-area membranes on a patterned substrate for a total of three functional layers

Thesis Supervisor: Henry I. Smith
Title: Professor of EECS

Acknowledgments

Where do I begin? That is the first question that emerges when you pursue a novel research endeavor. I must confront the same question when given the impossible task of acknowledging those who have guided me to this point in life. My enjoyment and success at MIT is truly owed to the people that I have been privileged to call colleagues and friends.

I first thank Professor Hank Smith for the opportunity to work with him all these years. I have always admired his sincere and passionate pursuit of technology and innovation. I have come to appreciate both the joy and deep frustration that goes hand-in-hand with the freedom to pursue interesting technical challenges. I didn't think I would feel more accomplished after the Ph.D. (because I didn't feel it after the Masters degree). Fortunately, I have gained a new confidence after over seven years of resera ch experience. The confidence comes from an exposure to an incredibly diverse set of projects, ranging from software architecture within zone-plate-array lithography to three-dimensional nanofabrication. Hank trusted me to creatively to attack and solve these challenges. And I firmly believe that creativity is useless in a vacuum. Hank has engendered a uniquely collaborative culture at the NSL, one of teaching and knowledge sharing. That has been the key to past success and will be the bedrock to innovation moving forward.

Professor Karl Berggren contributed a great deal of time and ideas as a thesis reader. His feedback during my early committee meetings really helped organize ideas and contributions. He forced me to put my research into the context of the greater nanofabrication community. Doing so helped me realize the significance of this work. He is also responsible for the continued growth of the NSL community which has improved the probability of learning and starting collaborations.

In the day-to-day grind of the lab, I owe a great debt to the lab manager, James Daley. He is the foundation that allows us to continue building and making progress. Through my journey, he provided solutions to problems or provided new functionalities in the lab so that I could overcome a hurdle. He is an exceptional colleague,

always going above and beyond so that others may succeed. And when not greasing the wheels of my project, he made spending hours and hours in the sterile yellow light of the cleanroom enjoyable.

Mark Mondol was a great asset when it came to utilizing the scanning-electron-beam facility. He did the exposures on the VS-26 and helped with training when I migrated over to the Raith.

Euclid Moon and Tim Savas have continued to provide their leadership and expertise to the challenges that current students are addressing. I have been the greatest beneficiary of their wisdom and experience.

Tom O'Reilly was instrumental in keeping the Lloyd's-Mirror tool robust and repeatable. I really appreciated his guidance in the mechanical engineering aspects of my work. He was always willing to sit down and give an impromptu lecture to a humble electrical engineer. His library of textbooks came in handy to say the least.

One of the hallmarks of a great project (in my opinion) is a collaborative nature. I had the fortune of working in a team where ideas were constantly produced and shared. Many points of inspiration came from working with Corey Fucetola, Martin Deterre, Will Arora, and Tony Nichol. Corey was a great source of moral support. I hope to see the same enthusiasm that has guided him this far next time I stop by for a visit.

So many NSL members and staff have supported me through this endeavor: Trey Holzwarth, Tymon Barwicz, Orit Shamir, Cindy Lewis, Alicia Akins, Donny Winston, Joel Yang, and Bryan Cord. My officemates, Feng Zhang, Sidney Tsai and David Chao, made going to work very enjoyable. I wish Sidney the best as she moves into a leadership role with our group. I wish to thank Thomas Reisinger for the opportunity to work with him on finding the Poisson spot for molecules.

I have been very fortunate enough to make a core group of friends inside and outside of lab: David Chao, Vikas Anant, Tyrone Hill, Kerry Cheung, Brian Taff, Justin Harper (my first MIT friend) and Karen Wong. It's nice that MIT does the heavy legwork in making sure quality individuals join the community. Investing in these relationships was really easy.

Of course I had great times with the family from Berwick: Shawn Kuo, Mengmeng Ding and Yi Zhang.

My time at MIT wouldn't have been possible without the support and love of my family: mom, dad and brother Jason. Many times along the way they didn't understand what I was up to, but they had the patience to stick with me until the end.

I finally end with the best thing that I earned during my time at MIT, my dear Chhandasi. She gave me the confidence and encouragement to stay on course when they were the toughest. With MIT finally in my back pocket and with her by my side only great things will happen. So where do we begin?

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Chapter 1

Nanofabrication of Three-Dimensional Photonic Crystals

1.1 Photonic Crystals

Nanofabrication is a curious field. The continual push for progress has not been the end goal in itself. Instead, the field is driven forward by applications. Nanofabrication is the quintessential "enabling technology". For example, research pushing modalities of lithography to the limits [57, 10, 42] or research venturing into new methods of nanolithography [41, 50, 37] are interesting because of the multidisciplinary challenges they encompass. However, their relevance comes when you place them in the context of an application. While microelectronics has been the historical benefactor of nanofabrication innovations, they are now opening a conduit toward solving critical problems in emerging areas like renewable energy production, optical communication, and biotechnology. The field is a symbiotic feedback loop where applications drive new nanofabrication technology and new nanofabrication technology drives new applications.

The goal in this body of work is to push out the frontier of nanofabrication tech-

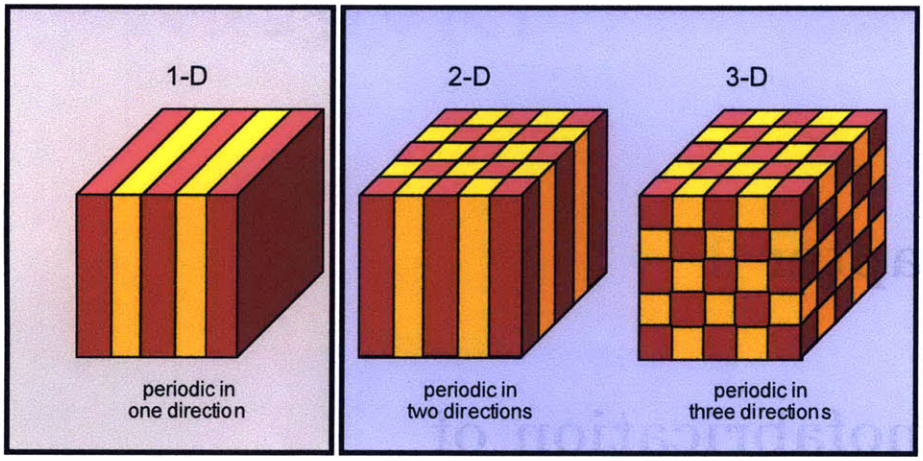

Figure 1-1: Simple illustration of photonic crystals of the 1-D, 2-D and 3-D variety. An N-D crystal can control the wavefunction in N-directions. A dielectric mirror (an example of a 1-D photonic crystal) reflects light in one direction.

nologies to create the Three-Dimensional Photonic Crystal (3DPC). The innovations presented here are a function of the specific application, but are general enough to open up other applications.

1.1.1 The 2D Photonic Crystal

Photonic crystals of different dimensionality are shown in Figure 1-1. The intuition of operation of the photonic crystal is most easily understood in the 1D scenario on the left. The 1DPC, otherwise known as a dielectric mirror, is a periodic stack of dielectric materials of contrasting index n_1 and n_2. From classical electromagnetic wave theory we know that there is a reflection at every interface because of impedance mismatch. When the reflections are in phase, they constructively interfere to cancel the transmitted wave and transfer all power to the reflected wave.

We characterize a bandgap material as one in which a selective band of wavelengths are reflected, and wavelengths outside this band transmit. Photonic crystals are metamaterials. It is the shaping of materials into a specific periodic structure rather than the inherent bulk material properties that provides the photonic functionality. The band of wavelengths that transmit versus reflect are a function of the materials

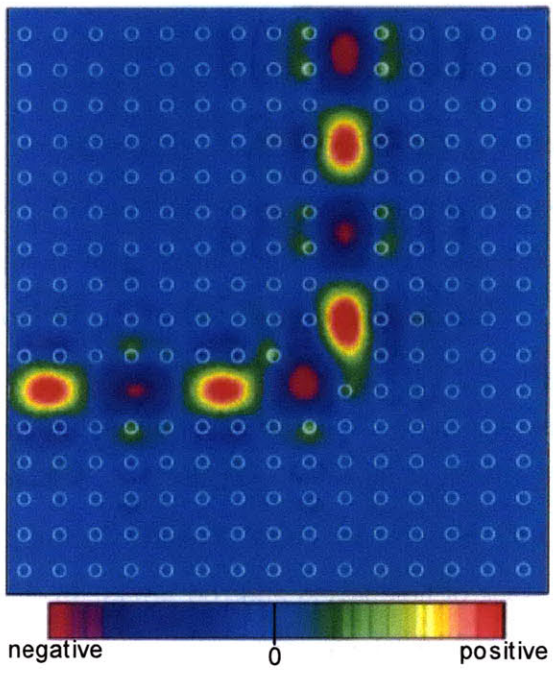

Figure 1-2: A simulation of a 2DPC with a 90 degree bend waveguide. We notice a periodic arrangement of rods except where the L-shaped waveguide is carved out. The period of the rods is proportional to the wavelength of the mode, $p = \frac{\lambda}{n}$ The band structure prevents modes from existing in the periodic region. However, modes readily propagate down the defect mode. Here the designers achieve a sharp bend with no loss. Taken from reference [4]

chosen and their respective thicknesses. Figure 1-2 shows the plan view of a 2DPC with square symmetry[4]. The periodic structure looks like a mirror to optical modes propagating inplane. However, paths (known as defect states) can be carved into the lattice which allows the radiation to propagate, yielding a functional waveguide. A 90^0 lossless turn cannot be achieved with traditional waveguide structures. The sharp bends give us a platform to build a fully integrated photonic chip[26].

1.1.2 The 3D Photonic Crystal

The 2DPC is a concrete way for theoreticians to design devices and test ideas. However, their capability as real devices is far more limited. The simulation in Figure 1-2 does not account for loss due to coupling to out-of-plane modes. In such a case we would not experience one-hundred percent transmission. Including this reality limits the potential of 2DPCs.

The solution is to sandwich the 2DPC within a three-dimensional lattice. This 3D lattice serves as a perfect mirror which extinguishes out-of-plane modes[5]. Figure 1-3 is an example of a 3DPC designed by David Roundy during his tenure at MIT[18]. One notes that it is a stack of hole layers and rod layers. In this specific instance the designer created a summation of planar structures so that is amenable to fabrication and device design. Yablonovite is a 3DPC that makes no concessions for device design and existing nanofabrication capabilities [20]. Let us enumerate the key physical characteristics of our selected structure, shown in Figure 1-4.

1. 660nm pitch features for a crystal built in silicon/air (n=3.4/n=1.0) and designed to operate with telecom wavelengths of λ = 1550nm. The structure is also square symmetric.

2. Multilayer structure with better than 20nm overlay requirements. Johnson states that a cavity must have two periods above and below it for sufficient confinement. That requirement yields a total of 8 hole layers and 8 rod layers.[5]

3. Periodic geometry in three dimensions. The only deviations occur for the device defect states which can be created by removing rods.

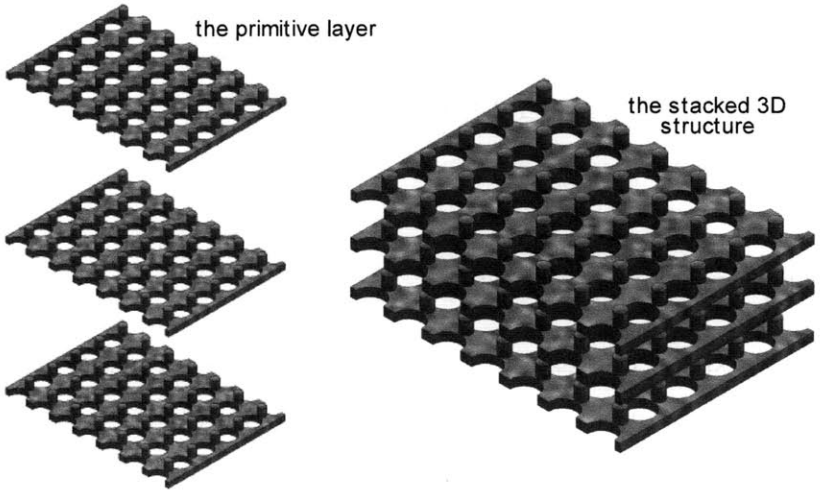

Figure 1-3: The photonic crystal is a stack of hole and rod 2DPCs with square symmetry that extend out over large area. The primitive layer is a layer of holes and rods. Over each primitive layer is another primitive layer with a half-pitch phase offset in x and y.

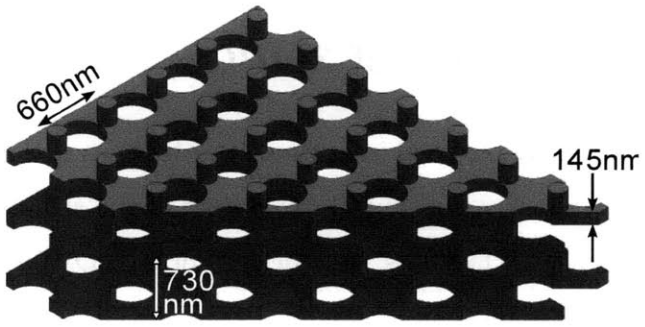

Figure 1-4: A cross sectional slide of the Roundy 3DPC along with dimensional measurements. One vertical period in z consists of two primitive layers.

4. Envisioned area of 10mm $\times$ 10mm for large-scale integration

This combination of characteristics is a significant departure from other nanostructure devices. The fabrication obstacles encountered when using traditional planar processes is discussed in Section 1.2.1. Our response to these challenges is at the core of this thesis (Section 1.3).

1.1.3 Application of 3DPCs

The theoretical existence of exotic nanostructures are not a justification enough to build them. We must question whether this platform gives us a unique solution to a difficult problem. The answer is yes. Specifically, 3DPCs will enable us to realize coupled resonator optical waveguides (CROWs). Figure 1-5 is a cartoon depiction of a CROW. This basic device is a series of point defect cavities that are weakly coupled. The cavities serve as resonators with long lifetime (high Q). Modes in this waveguide experience large dispersion, which in turn slows the group velocity. We can therefore precisely time events using slowed light. Doing so in ordinary silicon fiber would take many kilometers of line, which is highly impractical for many portable applications, such as phased-array antennas.

1.2 Nanofabrication of 3DPCs

The physical characteristics outlined in Section 1.1.2 leave us with a daunting fabrication challenge. The large-area and multilayer nature of the structure are outside the standard bounds of research facilities. In order to obtain a Q of at least 10^6, a device layer of a photonic crystal must be surrounded by eight layers (two vertical periods) above and below[5]. The solution to the problem requires creativity. Materials scientists have taken approaches involving holographic lithography in thick resist[46, 13] or self assembly of colloids[?]. These bulk methods have their advantages; however, even at their best, they can only produce perfectly periodic lattices. The functional device layer is not possible.

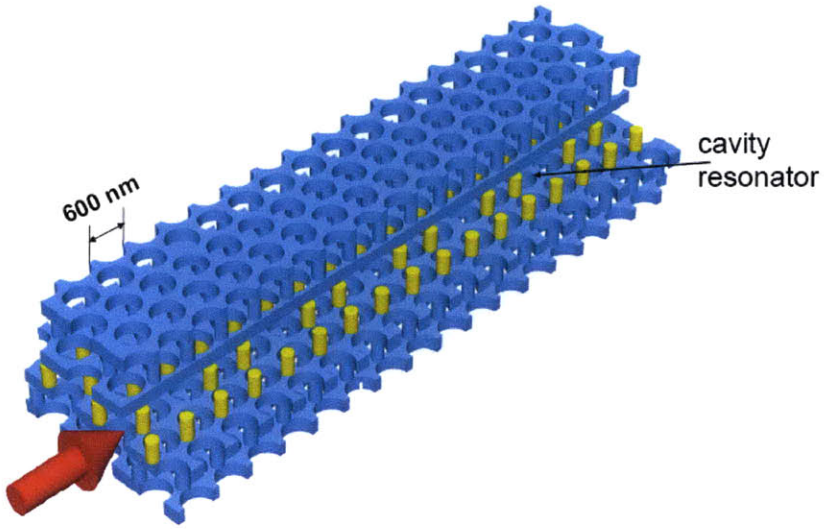

Figure 1-5: This is the coupled resonator optical waveguide implemented in a 3DPC. The device layer is in yellow. Every missing rod signifies a cavity resonator. Photons couple between the cavities by tunneling. The 3D confinement prevents photons from radiating away.

1.2.1 Layer-by-Layer with Planar Processes

The 3DPC depicted in Figure 1-3 is designed as a stack of 2DPCs. Therefore, one can take advantage of mature planar processes used by the semiconductor industry such as lithography, material deposition and anisotropic plasma etching[?]. In contrast to bulk fabrication methods, we can readily insert the functional device layer in the center of the crystal.

Researchers at the NanoStructures Laboratory understood this and proceeded to fabricate a seven-layer segment of the 3DPC with lateral dimensions of 100μm $\times$ 100μm (one field of an electron-beam lithography tool) [39]. They specifically worked with the MIT Crystal [27], which is similar to the Roundy Crystal in its planar hole/rod configuration (see Figure 1-6). However, it has triangular symmetry and a very large possible bandgap of 25%. The fabrication process cycle to fabricate two hole layers and one rod layer is outlined in Figure 1-7. The process flow includes typical planar processes such as lithography, liftoff and reactive-ion-etching. However, it also includes substrate planarization and material deposition, two processes that have lower probabilities of success. These processes are so unwieldy that most researchers

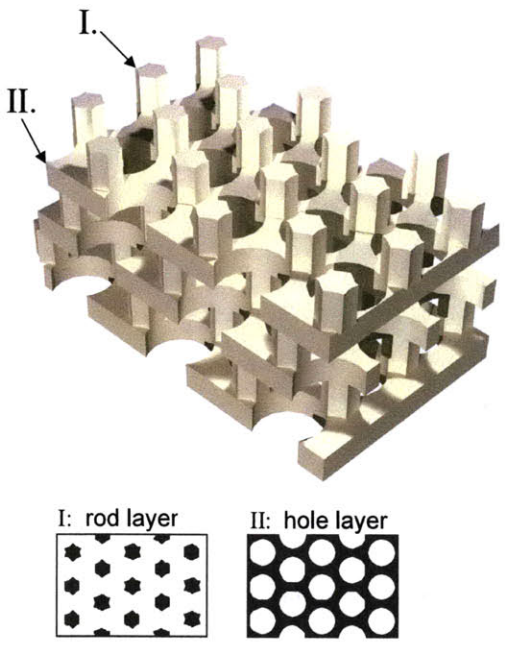

Figure 1-6: The MIT Crystal is a stack of 2DPCs, alternating between hole and rod layers. The plan view clearly shows the triangular symmetry. It was designed for layer-by-layer fabrication. Figure from reference [27].

attempt to design around them or make compromises to avoid them.

The exercise conducted by past researchers showed that the realization of a 3DPC is possible using planar processes, but it is extremely onerous. The process suffers from long fabrication times(on the order of four to six months), large costs, and very poor yield. The traditional layer-by-layer approach is not compatible with low volume runs in a research environment.

An analysis with a model elucidates the inherent problem. The yield of a process (i.e. the probability of success), Y, for a device chip is the product of the respective yields for all the subprocesses as is noted in Equation 1.1.

$$Y(N) = (P_A \cdot P_B \cdot P_C \cdot P_D \cdot P_E \cdot)^N \tag{1.1}$$

The equation highlights the key steps in Figure 1-7. P_A represents yield for lithography, P_B is the yield for lift-off, P_C is the yield for etching, P_D is the yield for planarization, and P_E is the yield for material deposition. These key processes

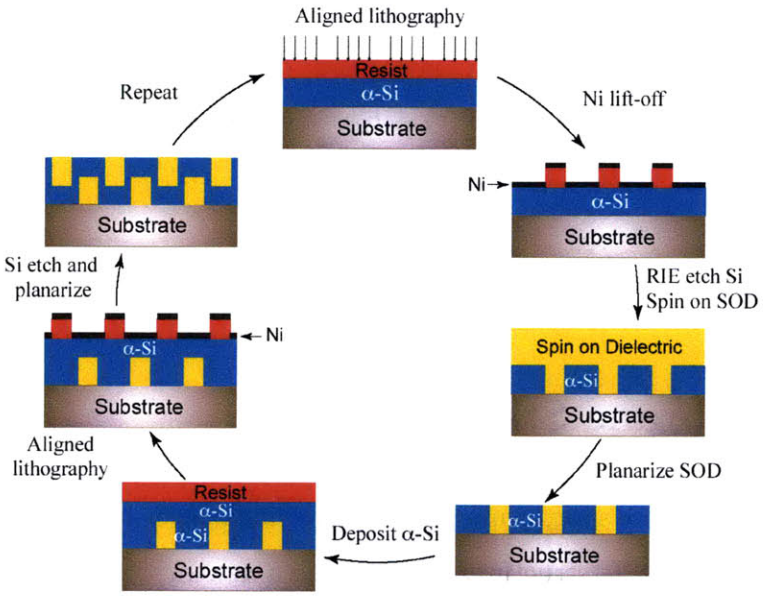

Figure 1-7: The first layer-by-layer process used to fabricate the MIT crystal(Figure 1-6). The process cycle highlights fabrication methods such as lithography, lift-off, planarization and material deposition. This single cycle for two hole layers and one rod layer is extremely difficult and low yield. Figure from reference [39].

can be broken down with finer granularity. For example P_A is the product of spinning resist, baking, and alignment. N represents the number of layers. Even if we plug in very optimistic numbers, the yield approaches zero for the total 3D structure,$Y = (0.95 \cdot 0.95 \cdot 0.95 \cdot 0.5 \cdot 0.5)^{16}$.

The time and cost of production (Equation 1.2 and Equation 1.3, respectively) are linear with the number of layers. N layers means N costly runs of lithography, etching, etc. Nothing can be done in parallel. One cannot build the 10th layer until layers one through nine are soundly underneath.

$$t(N) = N \cdot (t_A + t_B + t_C + t_D + t_E) \tag{1.2}$$

$$x(N) = N \cdot (x_A + x_B + x_C + x_D + x_E) \tag{1.3}$$

1.3 Membrane Stacking

In order to overcome the shortcomings of the traditional layer-by-layer approach to the nanofabrication of 3DPC structures, we propose a new method based on membrane technology. Figure 1-8 shows a cross-sectional view of our novel membrane stacking architecture. 2DPCs are fabricated as freestanding membranes, the membranes are inspected for accuracy, and then the membranes are stacked onto a substrate. As the figure also shows, we are able to fabricate many layers in parallel on a single substrate. This radical shift in multilayer production changes the math behind yield, cost and lead time in our favor.

While the membranes may be fabricated in parallel on a single substrate, their yields are uncoupled from one another. If there is a defective membrane layer, it does not determine the yield of the entire structure. This is because we inspect the membranes before committing them to the final stack. Any membranes that fail inspection are swapped for a good layer. The membranes are only coupled together during the stacking and therefore the yield is described by Equation 1.4, where P_S is

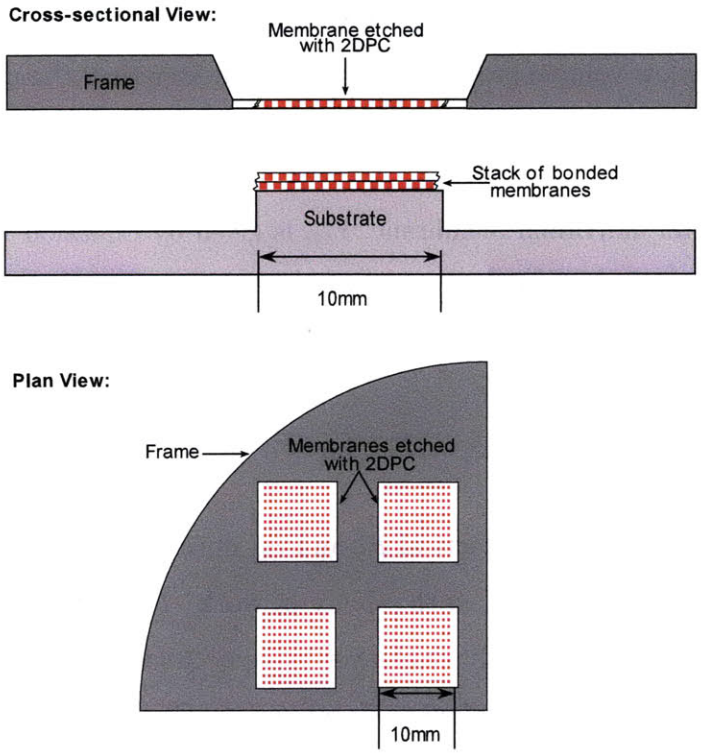

Figure 1-8: The membrane stacking architecture. [Top] Cross-sectional view of the membrane stacking concept. Membranes with 2DPCs are fabricated on a frame. The membranes are bonded to a substrate and then released from the frame. The vision is for large-area substrates. [Bottom] Plan view of multiple membranes fabricated in parallel on a single substrate. A quarter wafer is depicted because that is the substrate utilized in the body of this work.

the yield of stacking.

$$Y(N) = P_S^N \tag{1.4}$$

Assuming that we can achieve stacking with a 95% yield, our device yield for 16 layers is 44%. We will show that half the number of stacks are required by forming rods and holes on a single layer. In this case, the yield jumps to 66%. This is sufficient for our low volume production and much better than the near zero yield of the traditional layer-by-layer process.

The yield of an individual membrane, Y_M, is given by Equation 1.5, where, P_A is the yield of lithography, P_B is the yield of liftoff, P_C is the yield of etching, and P_Q is the yield of membrane release(a process unique to membrane processing).

$$Y_M = (P_A \cdot P_B \cdot P_C \cdot P_Q) \tag{1.5}$$

For membrane stacking to be practical P_S and P_Q must be reasonably high. Demonstrating this is a central theme to this body of work. It must be pointed out that not only do we beat out the traditional layer-by-layer model in terms of yield, but we also dramatically reduce time and cost of production. Equation 1.2 and Equation 1.3 are a function of the number of layers. However, for our stacking technique, the cost and time models, Equation 1.7 and Equation 1.6, are constant because many layers can be fabricated in parallel. In Equation 1.6, the additional constant, K, refers to the time required to stack. Because stacking can be done quickly, the scale of the problem does not scale exponentially or even linearly for additional layers.

$$t = t_A + t_B + t_C + t_Q + K \tag{1.6}$$

$$x = x_A + x_B + x_C + x_Q \tag{1.7}$$

1.4 Thesis Contributions and Organization

The focus of this work is to develop solutions for the key challenges inherent to membrane stacking. As was shown in Equation 1.4 and Equation 1.5, the individual yields for membrane release and membrane stacking must be sufficiently high for this nanofabrication architecture to be viable. Achieving this lofty goal means addressing a myriad of challenges that include:

- Developing large-area lithography for the 2DPC with overlay potential.
- Releasing large-area free-standing membranes patterned with 2DPC with aspect ratios of 10mm $\times$ 10mm $\times$ 300nm.
- Efficient and repeatable bonding of large-area membranes to substrates
- Controlled and particle-free release of a membrane from its frame
- Ancillary membrane processing, cleaning and handling techniques to improve yield

Chapter 2

Large-area Free-standing Photonic Crystal Membranes

2.1 Introduction

Our ultimate vision is to create a technology for multilayer nanofabrication over large areas (more than 10mm $\times$ 10mm). Because 3DPCs are a very promising vehicle for realizing an integrated optical circuit, large areas are requisite. The first question that one must ask is whether one can fabricate 2DPCs membranes with dimensions of 10mm $\times$ 10mm $\times$ 300nm. This problem is on a different scale than we have seen in other multilayer-membrane fabrication processes such as NanoOrigami. There typical structures have aspect ratios on the order of 100μm $\times$ 100μm $\times$ 300nm[7, 36]. This chapter addresses this issue by discussing processes and techniques developed to fabricate large area free-standing photonic structures in low-stress silicon nitride. The inspiration comes from work done by Tim Savas[47]. He fabricated free-standing gratings with a 100nm pitch on a 100nm-thick membrane of silicon nitride. Silicon nitride offers a unique platform upon which we can create large area membranes and use robust batch processing for membrane release.

2.1.1 Lessons from X-ray Lithography

Large-area silicon nitride membranes were utilized as amplitude masks for X-ray proximity lithography. Circular membranes with diameters at 31mm and thickness of 1μm were routinely fabricated. These membranes are quite strong when pressure was applied to the face of the membrane [14]. The material, by nature of its thinness, is transparent to the X-ray radiation. The dark regions are defined by a gold absorber (exceeding 100nm in thickness). This is relevant to our discussion because this gold absorber is patterned after the membrane has been released. In other words, the creators of X-ray masks must pattern and process directly on these fragile substrates. As one can imagine this is a potential nightmare and a true test of patience. The reasons for doing it this way are manifold.

Because X-ray masks are patterned with scanning-electron-beam lithography (SEBL), writing on a membrane is advantageous over writing on solid substrate because back-scattered electrons contribute less to the point-spread function of the beam, largly doing away with pattern-dependent proximity effects. Second, X-ray masks are heterogenous material systems including silicon nitride, gold absorber, and sometimes polyimide protective layers[14]. These layers do not withstand the wet etch process used to etch the silicon handle and release the membrane (see Section 2.4.1). It also comes down to cost. Patterning the X-ray masks using SEBL is very expensive in terms of time and money. One didn't want to spend a great deal patterning a wafer only to have it burst during the release. Using membranes that yield after release is built-in quality control. Finally, patterning on membranes after the release give us better control over distortion.

Given that we will also utilize silicon nitride membranes, a question of strategy is posed: should we release the membrane and then process or conversely, process and then release. We bucked the convention set by X-ray lithography and selected the latter method. As will be discussed in Section 2.2, interference lithography will be utilized for patterning. Optical exposure on a solid substrate is well understood, while patterning on a transparent membrane would require extra measures to prevent

spurious backside reflections from disrupting the pattern. The more a membrane is handled and processed, the greater the probability of it failing. In this chapter we show that the strategy of patterning and then processing pays off with high yield and efficient processing.

2.2 Interference Lithography

At the NanoStructures Laboratory we are uniquely suited to patterning large-area periodic nanostructures because of the availability of interference lithography (IL) [54]. There are three platforms: the Lloyd's mirror setup ($\lambda = 325$nm), the Mach-Zender ($\lambda = 351$nm), and the achromatic interference lithography tool ($\lambda = 193$nm)[47]. For this specific project the Lloyd's-Mirror interference lithography tool was utilized. A diagram demonstrating the basic concept is shown in Figure 2-1. This tool is particularly appropriate for the prototype membranes because it can pattern areas as large as a quarter of a 10cm wafer. Additionally, the stage of the tool rotates relative to the incident beam, changing the incident angle and the pitch of the interference intensity modulation. The relationship between period and angle is stated in Equation 2.3. The modulation in the x-direction is obtained by taking the intensity of the two plane waves (an approximation) at the substrate surface, Equation 2.2.

$$E(x) = E_1(x) + E_2(x) = e^{ik_x x} + e^{-ik_x x} \tag{2.1}$$

$$I(x) = \frac{cn\epsilon_0}{2}|E(x)|^2 = \frac{cn\epsilon_0}{2}(2e^0 + 2e^{-i2k_x x} + 2e^{i2k_x x})$$

$$I(x)\frac{2}{cn\epsilon_0} = 2 + 2cos(2k_x x) = 2 + 2cos(2\pi sin(\theta)\frac{x}{\lambda}) \tag{2.2}$$

$$P = \frac{\lambda}{2 \cdot sin(\theta)} \tag{2.3}$$

This method of IL has been utilized in the fabrication of 2DPC devices such as

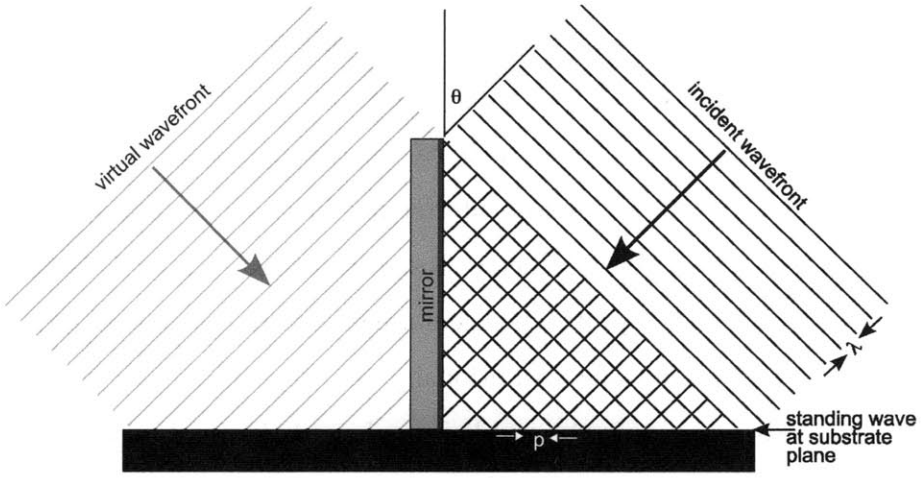

Figure 2-1: Illustration of the Lloyd's-Mirror interference lithography tool. A spatially-filtered incident is simultaneously incident on a substrate plane and mirror plane. The reflected beam from the mirror interferes with the beam at the substrate plane. The pitch of the standing wave is determined by the source wavelength and the angle of rotation of the mirror relative to the incident wavefront. A single exposure forms gratings. A double exposure, where the substrate is rotated 90^o between exposures, results in a grid.

the supercollimater and superprism [43, 52]. The tradeoff for the tool's flexibility and ease of use is the inability to lock the pitch from wafer to wafer. Overcoming the compromise is detailed in Section 3.5. However, for the prototype free-standing membranes, pitch reproducibility is not a primary concern.

The Lloyd's mirror can cover a 3.75cm $\times$ 3.5cm area with a grid pitch of 600nm. A detailed description of the tool design is found in Mike Walsh's thesis [54].

2.2.1 Resists System

Patterning on a silicon nitride substrate (n=2.06 at λ = 325nm) is done with a trilayer stack of AZ BarLi (n=1.55-i0.14 at λ=325nm) antireflection coating(ARC), 20nm of oxide (n=1.48), and PFI88 positive photoresist (n=1.79-i0.02) (or PS4 negative photoresist). The index for silicon is 4.68-i2.03.The ARC thickness is a function of the silicon-nitride film thickness underneath and the illumination angle of the beam. For periods between 500nm and 600nm, 270-300nm of BarLi is spun. The ARC has two functions. One, it attenuates the beam. Second, the thickness is tuned such that the incident beam and the reflected beam tend to cancel each other at the ARC/resist interface.

1. Ash SiN-coated Si wafers in O2/He plasma after removing from fluoroware (plastic casing)

2. Spin BarLi (ARC) and bake 90 seconds at 175^{o}C on hotplate

3. Evaporate 20-30nm of SiO_2

4. Apply HMDS by puddling for 60 seconds, spinning for 5 seconds, wiping down bowl and waiting 4 minutes

5. Spin PFI88 (or PS4) at 3800RPM for 200nm coat and bake at 90^{o}C on hotplate

6. Put sample in fluoroware and cover with foil until exposure

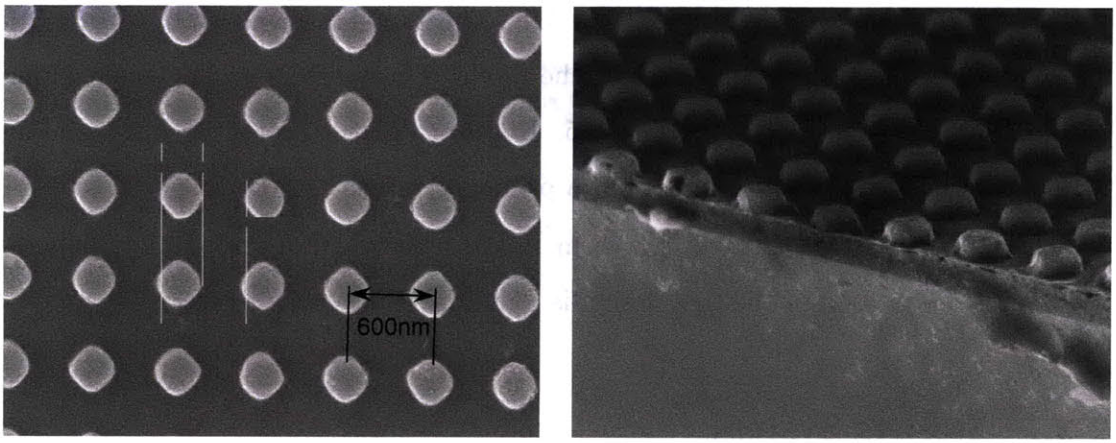

Figure 2-2: [Left] PFI88 posts after exposure and development. In order to create a geometry with square symmetry, the sample was exposed at full dose, rotated 90 degrees (using the wafer flats as a reference) and exposed again. [Right] A cross sectional micrograph of the resist after exposure. The resist sits on an ARC layer. The post pattern will be transferred into the ARC with RIE.

2.2.2 IL Exposure

High quality and repeatable results require calibrating the Lloyd's mirror exposure tool before each exposure. The illumination optics for the tool are straight forward. The beam from the source, HeCd laser operating at $\lambda = 325$nm, is guided by steering mirrors to a spatial filter where spatial frequencies contributing to noise are filtered out. After the pinhole, the beam is allowed to expand freely for about two meters until it intersects the substrate. The power must be measured directly out of the laser. Additionally, the power at the substrate plane must be measured for intensity and uniformity. The beam is also qualitatively inspected prior to exposure to ensure a round Gaussian profile. Tracking these metrics allows for repeatable and uniform results. Since we are interested in exposing photonic crystals with square symmetry, the wafer is exposed at full dose, rotated 90^o and exposed again. Since there is no rotation stage for the substrate to pivot on, the rotation is done by hand using the wafer flat as a reference. After exposure PFI88 wafers are developed in CD-26 developer for 45 seconds and then thoroughly rinsed with DI water and dried with nitrogen. PS4 requires a post hotplate bake at 110°C shortly after exposure and before

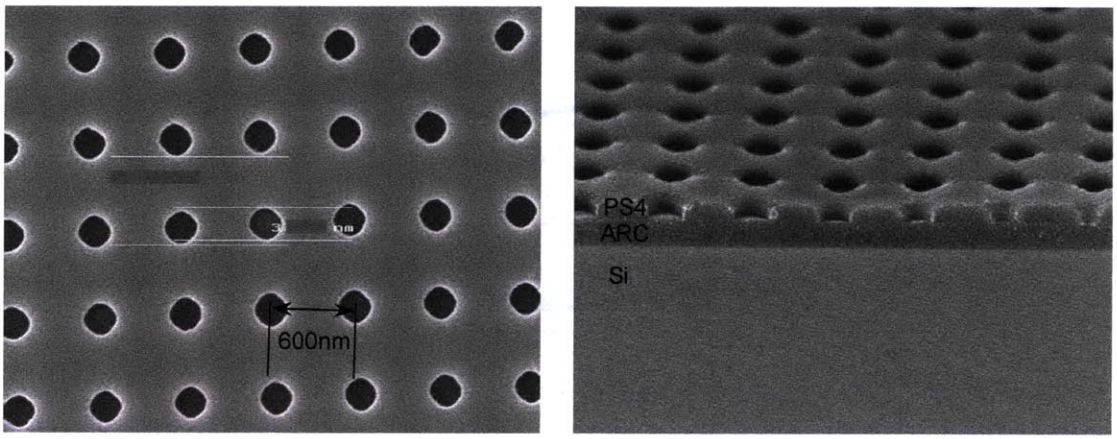

Figure 2-3: [Left] 600nm pitch holes in PS4 that were exposed in the Lloyd's mirror. PS4 has sufficient contrast to create a layer of holes and PF88 has sufficient contrast to create posts. [Right] A cross sectional view. The ARC layer clearly contrasts with the resist and silicon substrate.

development. Figure 2-2 shows a top down and cross-sectional view of a successful IL exposure with PFI88. Figure 2-3 shows a cross-sectional view of of the trilayer stack with a hole pattern in exposed PS4. The double exposure technique allows us to cover nearly an entire quarter wafer with a pattern. Both resists have a long history at the NSL and exhibit robustness and a long shelf life if refrigerated. This characteristic cannot be taken for granted in a research fabrication facility.

2.2.3 Trilayer Etch

As shown in Figure 2-4, the pattern in resist is transferred into the SiO_2 interlayer and then the ARC using reactive ion etching (RIE). The photoresist holds up well to the short CF_4 etch required to etch through the oxide. The oxide has very high selectivity with the O_2/He plasma used to anisotropically etch the ARC. Highly vertical sidewalls are achievable with this process, which are essential for liftoff. There is also good tolerance in this process to overetching, making it very forgiving. Figure 2-5 shows the final product of a trilayer etch when starting with a post pattern in PFI-88.

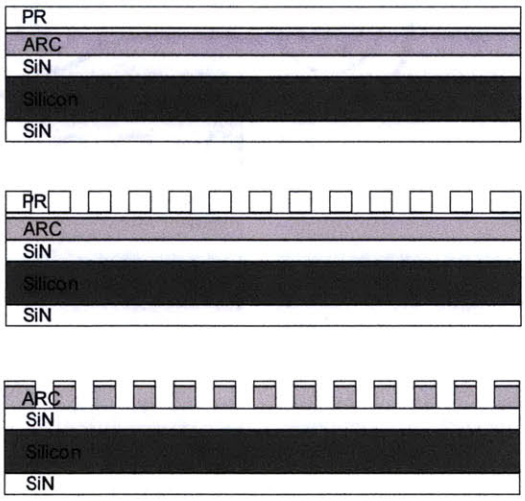

Figure 2-4: [Top] The starting substrate is a double polished 4" wafer that is coated with low-stress SiN. Trilayer is spun on top. [Middle] Gratings are exposed in resist using the Lloyd's mirror. [Bottom] RIE is used to transfer the pattern in resist to the ARC.

2.3 Pattern Transfer

2.3.1 Liftoff

The grid pattern which starts in PFI88 must be ultimately transferred to the silicon-nitride layer as is depicted in Figure 2-9. Pattern transfer into silicon nitride is accomplished with anisotropic RIE. High-fidelity-pattern-transfer via RIE requires a highly selective etch mask. ARC can suffice as an etch mask for short etch depths ($<$ 100nm); however, it is best to employ a metal mask for the etch depths required in our substrates ($>$ 300nm). In this work, both chromium and nickel were employed as etch masks. In both cases the metal is evaporated on the ARC posts and then the ARC is lifted off. Figure 2-5 shows how things look after a relatively thick metal evaporation.

After metal evaporation, the sample is soaked in a solvent or acid that will dissolve or liftoff the underlying polymer (ARC in this case). ARC's are typically difficult to remove because of their chemistry. When lifting off BarLi ARC, EKC-265 is employed. This viscous liquid is heated to 65^{o}C. This temperature, where the fluid becomes less viscous, is critical in obtaining a good liftoff. Figure 2-6 shows the result of liftoff

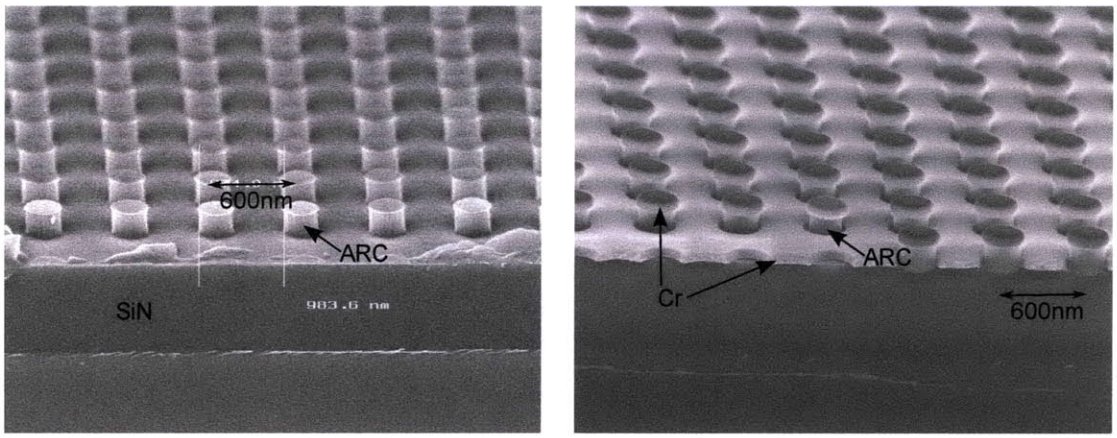

Figure 2-5: [Left] 600nm pitch posts of ARC with an oxide cap that remains after the trilayer RIE etch. [Right] A look at the posts after a thick metal evaporation.

after 3 minutes. Eliminating the redeposition of the metal caps can be solved by using ultrasonic agitation of the wafer. The typical process is to soak the wafer in hot EKC-265 for 90 seconds and then transfer the beaker to an ultrasonic bath for an additional 90 seconds. The wafer is then rinsed with isopropyl alcohol(IPA). Post liftoff, samples are transitioned to an RCA clean because EKC-265 residue typically remains. It must be noted that EKC-265 is caustic to nickel. Immersion of 30nm films in EKC-265 for more than 3 minutes leads to deterioration. Chrome is robust to long exposures to EKC-265.

2.3.2 Reactive-Ion Etching of Silicon Nitride

RIE is an effective way to transfer the pattern in metal into silicon nitride. Table 2.1 summarizes the gas and mask combinations attempted. The only chemistry with poor results is CF_4 with a nickel mask. This combination leads to the formation of a flourinated polymer as is shown in Figure 2-7. This additional scum increases the surface roughness, which will have deleterious effects for membrane bonding. The recipe that was utilized the most for it's combination of etch anisotropy and etch rate was CHF_3/O_2. At 300V and 10mTorr we obtained about a 25nm/min etch rate. Makers of photonic devices prefer the nickel mask because it can achieve finer grains

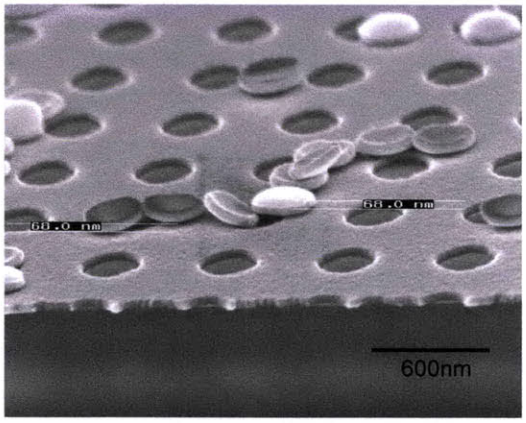

Figure 2-6: A hole pattern in metal after lifting off the ARC posts. The liftoff process inverts the original posts in resist to holes in metal. This particular sample suffers from redeposition of the lifted off metal caps onto the surface. This result is remedied by using ultrasonic agitation [1].

Table 2.1: RIE etch results for silicon nitride.

Gas/Mask	Etch Rate	Bias/Pressure	Quality	Sputtering
CF_4/Ni	22 nm/min	300V/10mTorr	poor	low
CHF_3-O_2/Ni	25 nm/min	300V/10mTorr	good	low
CF_4/Cr	22 nm/min	300V/10mTorr	good	low
CHF_3-O_2/Cr	25 nm/min	300V/10mTorr	good	low

and thus superior side-wall roughness[12]. This is not as critical for our photonic-band-gap research [5]. While both masks were utilized, chrome is preferred because of its resistance to EKC265.

After RIE, the metal mask is removed with a wet etch. CR-7 is used to strip chrome and TFB etchant is used for the nickel. Figure 2-8 shows the final pattern. The substrate is ready for release.

2.4 Membrane Release

As was stated in Equation 1.5, releasing the membrane is a key processing step. P_Q must be near 1.0 for membrane stacking to be a viable technology. This section addresses the hurdles we overcame to achieve nearly a perfect yield.

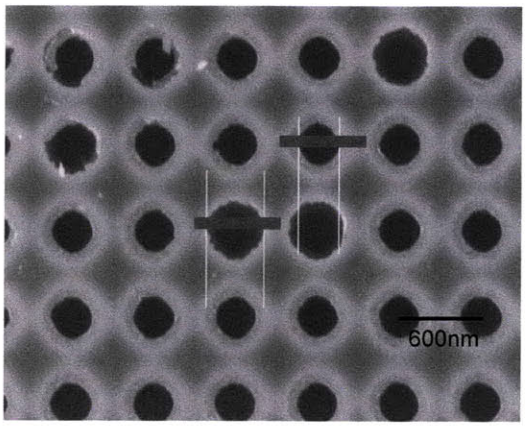

Figure 2-7: A view of silicon nitride substrate after RIE in CF_4 and nickel hardmask removal. There is a fluorinated polymer that remains at the openings. Flakes of this polymer flake off and generated particles. This problem is solved by moving to a CHF_3 and oxygen (16:3) mixture during RIE.

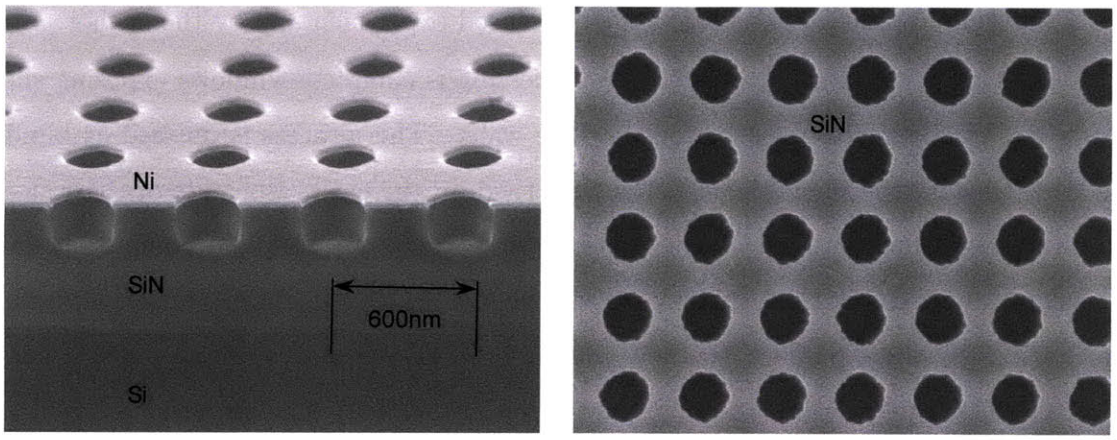

Figure 2-8: [Left] Mask on SiN after partial dry etching. We note good anisotropy and good mask integrity. [Right] View of SiN substrate after RIE and mask removal. Surface is smooth and particle free.

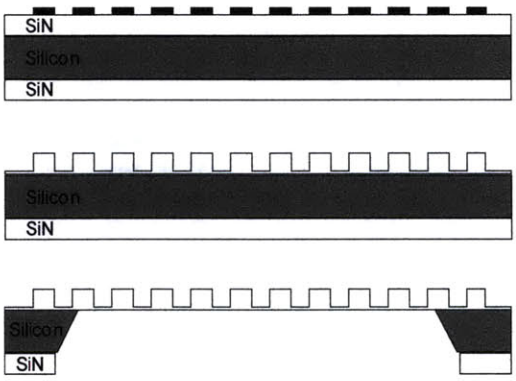

Figure 2-9: Low yield membrane release .[Top] Metal mask after liftoff of ARC [Middle] Pattern is transferred across entire wafer via RIE. The etch should be stopped before going completely through the SiN [Bottom] SiN window is opened with RIE and Si is etched in KOH bath to release membrane. This structure was ultimately found to be weak.

2.4.1 Blind Release

The initial approach taken to releasing patterned membranes follows the process outlined by Tim Savas [51, 2] and shown in Figure 2-9. He recommended that the photonic-crystal pattern be etched only 90% of the way through the nitride film to prevent the silicon etch from occurring on the front side, generating gas byproducts and bursting the membrane This was experienced experimentally by the author.

After frontside (the patterned side) processing is complete windows exposing silicon must be etched on the backside of the wafer. This process is dubbed as blind release because the photonic region is patterned on the entire frontside of the wafer and no alignment is required with the backside windows. This is accomplished by masking the frontside with a thick resist, Shipley 1813. Then the backside is spun, and windows are exposed with the Tamarac or OAI exposure tools at $\lambda = 400$nm. In this work, square windows ranging from 10mm to 15mm were patterned. Circular windows were attempted successfully, however, the etch forms a jagged circle. With square windows, multiple windows can be packed together on a quarter-wafer sample.

The windows of silicon nitride are etched through to the silicon. This wafer is ready for release in a 20% potassium hydroxide (KOH) bath set at 85°C [55]. The silicon will etch at 100μm per hour for a total etch time of about 5 hours. A resulting

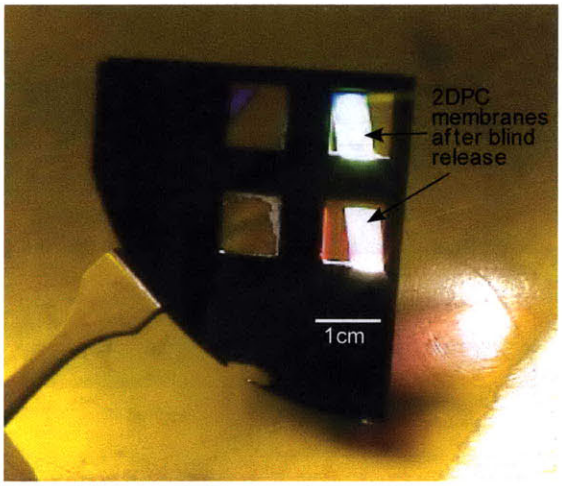

Figure 2-10: Wafer after the blind release. Half of the windows burst after the cleaning process.

wafer is shown in Figure 2-10. The yield for these large-area photonic patterns after cleaning and drying was only 50%. Savas was able to achieve a better yield because he created small-area membranes measuring 200μm $\times$ 5mm.

2.4.2 Post-etch cleaning

Wafers that have gone through KOH etch remain contaminated with salt. Therefore, the finished wafers must be soaked in DI Water overnight. It should be noted here that large area membranes should always sit vertically in any bath. They should be placed within or pulled out of the bath with slow and smooth vertical motion. After the water soak the wafers can be dried by blowing gently with a nitrogen gun. They are then put in a pirhana bath (3 Sulfuric Acid H_2SO_4: 1 Hydrogen Peroxide H_2O_2). The wafers are transferred to a water bath to soak for at least ten minutes before being placed in an RCA clean. The wafer should be soaked in DI Water and then carefully dried with a variable pressure nitrogen gun set to a soft pressure.

2.4.3 Perfect Yield With An Aligned Release

The patterned membrane is weak at the membrane and frame border. The structure is bolstered by leaving a buffer of unpatterned membrane between the edge of the

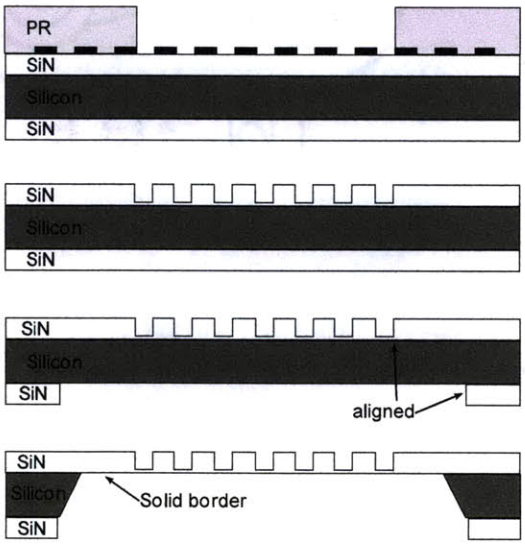

Figure 2-11: High-yield-release process.[One] Photoresist windows are aligned to a reference. These are the regions where the PCs are selectively etched. [Two] Wafer after selective RIE. Etch is only 90% of the way through. [Three] Resist is spun on backside and window is exposed after aligning to reference. [Four] The final free-standing membrane structure with improved integrity.

membrane and the photonic region as is shown in Figure 2-11. We cannot do a blind release if we want this border region. Rather than etching the photonic crystal pattern into the entire frontside of the wafer, we selectively etch square regions of photonic crystals where the membranes will be released. The windows in the backside must be larger than the square regions on the front side so that there is an unpatterned border. Alignment between two sides of the wafer imposes a significant challenge because no exposure tool is equipped to image the front and backside of a wafer simultaneously.

Figure 2-12 depicts the alignment scheme employed. The cleaved edges of the quarter wafer serve as the reference between frontside and backside. Special technique is required to obtain straight cleaves that ensure a 90^o corner on the quarter wafer. The wafer can be aligned in lateral dimensions and rotationally with reference to the orthogonal rail alignment marks (on the lower right corner of the mask in Figure 2-12. It is best to make the patterns symmetric about the $x = y$ line so that no handedness errors occur between the front and backside patterns. Using this method on the OAI contact aligner, $\pm 200\mu$m of registration was achieved consistently. This number

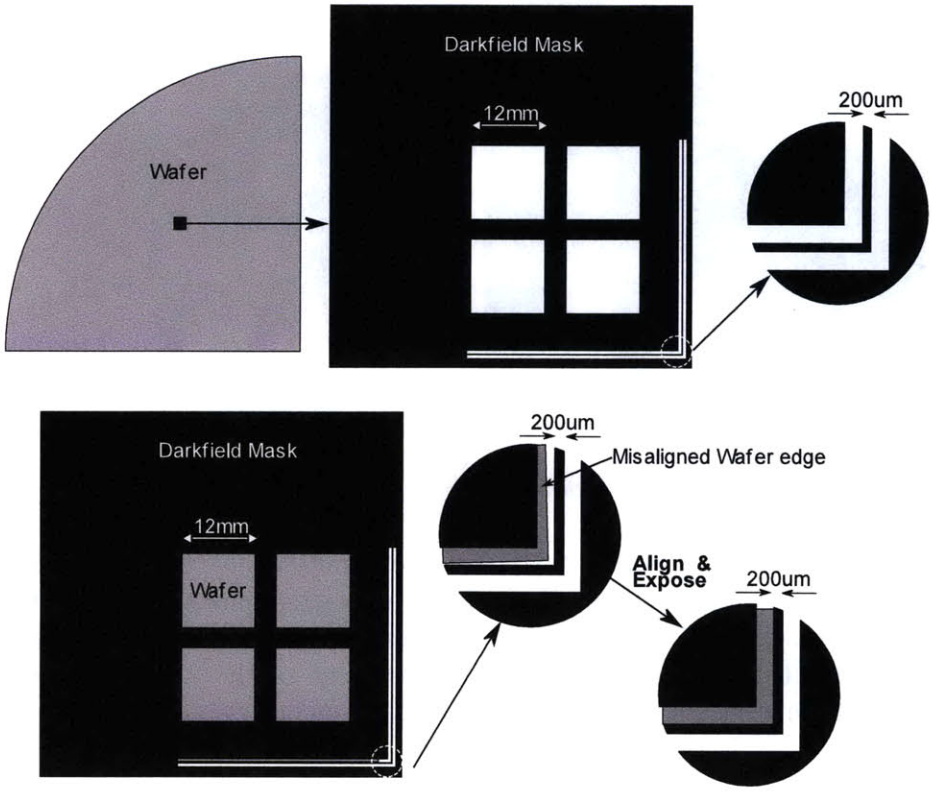

Figure 2-12: The cartoon shows the scheme devised to align frontside features with window features on the backside of a quarter wafer. Exposures were done with the NSL OAI aligner. This scheme enabled alignment within 200μm. Accuracy is dependent on the quality of the cleave of the quarter wafer. This technique is crucial for the process where membrane is processed before release.

sets the tolerance for how small the border region can be made. Ultimately, this is wasted area, so we are interested in minimizing it. We cover the alignment mark with aluminium during exposure because we do not want it to be transferred into the wafer.

2.5 Results and Applications

Employing the aligned release dramatically improved the yield for large-area patterned membranes from $P_Q = 50\%$ to a consistent 100%. Figure 2-13 shows a 15mm $\times$ 15mm $\times$ 350nm freestanding membrane[38]. We notice that there is a unpatterned

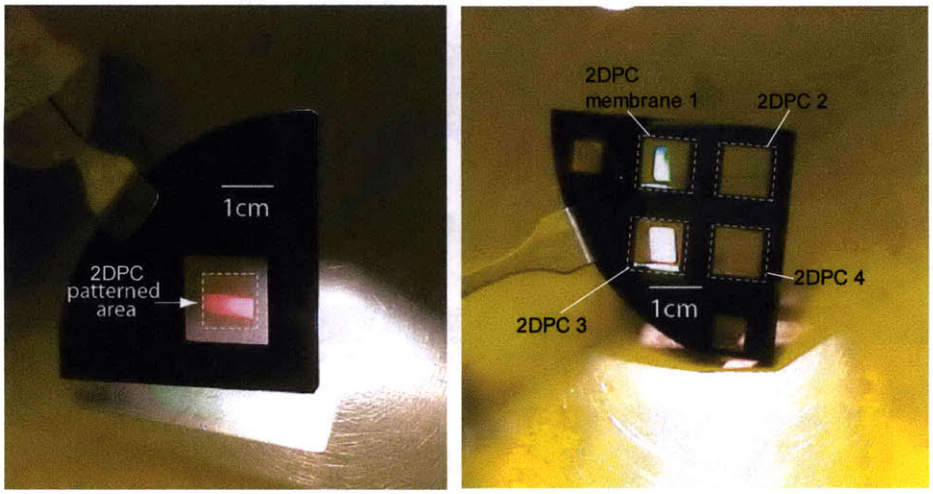

Figure 2-13: Large-area patterned membranes that are viable for photonic-chip integration. [Left] Light diffracts from a 2DPC membrane measuring 15mm × 15mm × 350nm. Note the solid border that separates the edge of the frame and the edge of the 2DPC pattern. [Right] We were able to demonstrate that many layers can be processed in parallel.

border around the patterned region, which does not diffract the light. This is the largest membrane fabricated in this thesis work, and it was also the largest membrane attempted. This is the largest free-standing membrane with photonic pattern published to date. The area demonstrated is sufficient for our intended application; larger membranes are potentially feasible. The ability to pattern and release several membranes in parallel on a single wafer was demonstrated. Figure 2-13 shows four photonic layers created together on one wafer. This is a key requirement to making the stacking architecture practical.

Later in the thesis we explore patterning additional features on the membranes to assist with membrane stacking. While our intention is to use these 2DPC membranes for a photonic device, there are other interesting applications for this device. One idea involves using the membrane as a template for evaporations which could be potentially used for the fiducial grid for Spatial-Phase-Locked E-beam Lithography [23]. Also the the large area structure can readily be used as a diffractive optical element, which we briefly explore in Section 3.5.

Chapter 3

Fabrication of the Primitive Layer with Next Generation Lithography

3.1 Introduction

In this chapter we address the interesting and challenging lithography issues that surface as we tackle the problem of photonic crystals via membrane assembly. As was described in the introduction, the 3D photonic crystal design by Roundy (Figure 1-3)is an alternating stack of hole layers and rod layers. In Chapter 2 we showed that a membrane etched with a periodic array of holes can be fabricated. However, how do we form a membrane of disconnected rods? It is not possible unless the rod layer is fabricated on a very thin (sub 50nm-thick) supporting membrane. A careful look at the plan view of the primitive structure (Figure 3-1) shows that the rods sit on top of solid regions with respect to the hole layers below; therefore, it is possible to fabricate both layers onto a single membrane. The question is whether we can do it at high yield.

While this two-level structure is not as onerous as a multilayer photonic crystal, it still forces us to confront material deposition and planarization processes that compromised the success of the traditional layer-by-layer process. The idea of putting the hole layer and rod layer on a single membrane only makes sense if the structure can be done at high yield.

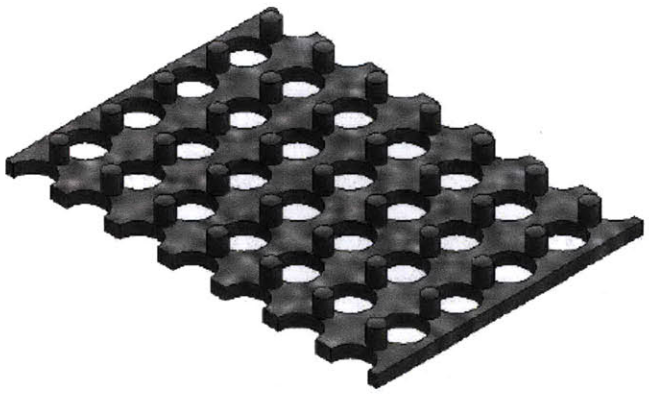

Figure 3-1: The primitive structure of the 3DPC. Rods sit on the solid spaces of the hole layer. The focus of this chapter is the nanofabrication of this structure.

3.2 Dual-Hard-Mask Process

Multilevel nanostructures are avoided in the research environment because the traditional method for creating multilayer structures is onerous. However, researchers at the NSL have often focused on fabricating two-level photonic structures such as the polarizer-splitter and rotator and the Bragg-filter waveguide[11, 30]. These devices were fabricated with good yield using a dual-hard-mask process that requires no new material deposition and no planarization via chemical mechanical polishing. The primitive layer is another candidate to benefit from this process.

Figure 3-2 summarizes the fabrication processes incorporated to build the layer. The process takes advantage of strong etch selectivity between chrome and nickel. The chrome (20-30nm) etch mask used to define the rods is put down first using interference lithography and PS4 (process delineated in Chapter 2). Because the chrome is so thin, the surface is readily planarized with the spin of the ARC for the second lithography step. For the second lithography step a thicker ARC layer is preferred to minimize the intensity modulation of the reflection caused by the chrome mask below. The process presented here does not adddress the alignment required for the holes and rods to be patterned with appropriate spatial offset and coherence. However, for this proof of concept development, this requirement is circumvented by

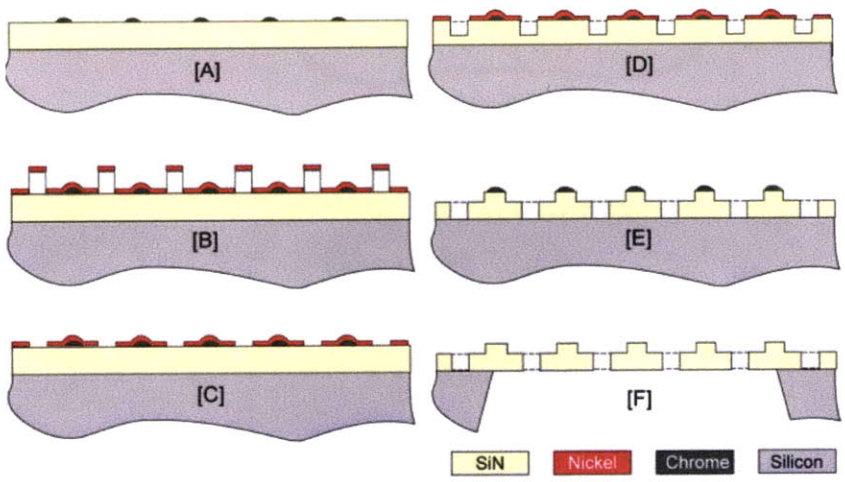

Figure 3-2: [A] Chrome dots on surface after lithography in negative resit and liftoff. [B] Lithography in positive resist and nickel evaporation. [C] Liftoff leaves us with two masks on a planar surface. Figure 3-3. [D] RIE hole layer to specification. [E] Remove nickel and RIE rod layer to specification. [F] Membrane release.

doing the second exposure in the Lloyd's mirror with the same period but rotated with an offset. This results in a regular beating between the two layers where the holes are aligned with respect to the rods. Figure 3-3 shows the two sets of masks sitting on the silicon nitride substrate.

After the masks are put down, the pattern is dry etched in two phases. The nickel mask is first used to etch the hole level while the chrome mask sits idle underneath. The most difficult part of the process is timing the etch so that the etch depth is consistent with what is needed. Barwicz and Qi showed that this is possible with the fabrication of the Polarization-Splitter Rotators [11][40]. The nickel mask is removed with a wet etch exposing the chrome mask underneath. Another anistropic RIE etch is done to define the rod layer. Finally the chrome mask can be removed with CR7. Figure 3-4 shows the final results of the process. There are no significant obstacles preventing this process from becoming high yield.

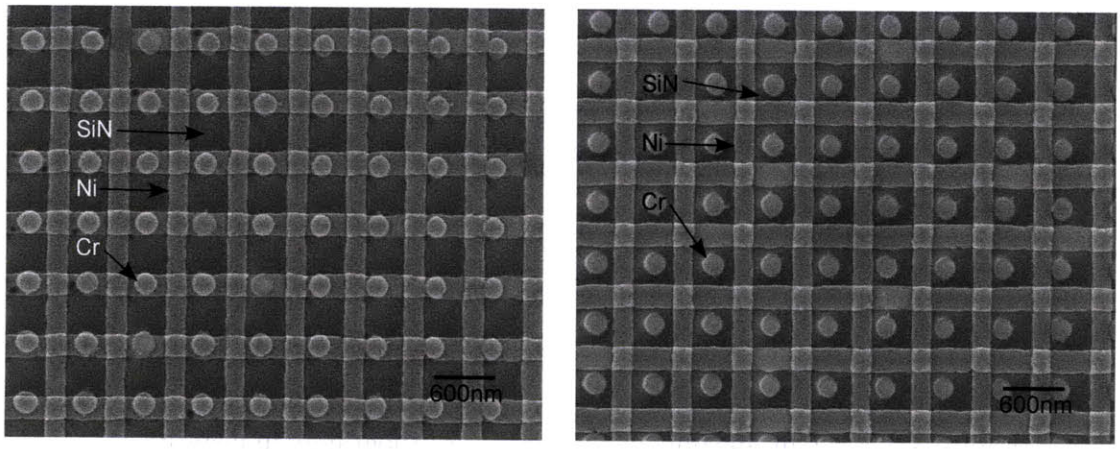

Figure 3-3: Nickel and chrome masks sitting on a planar nitride surface. Both images are taken from the same sample. On the left, the hole and rod masks are aligned. Lithography was done with IL.

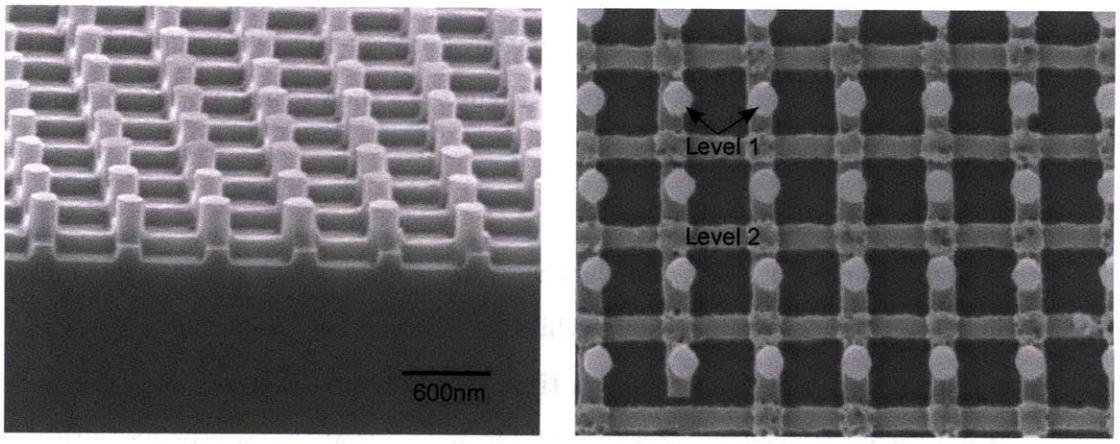

Figure 3-4: The two-level primitive structure created with the dual-hard-mask process. No planarization or material deposition is required to achieve this structure; this structure can be fabricated with high yield and very low overhead.

3.2.1 Discussion

The innovation of using a dual-hard-mask process to fabricate a hole and rod on a single membrane has a significant consequence in the context of membrane technology. We reduce the number of membranes and stacks required by a factor of two which dramatically improves yield for the final device. According to the models outlined in the Introduction, each membrane should contain the maximum number of levels it can accommodate at a high yield. We have successfully shown that number is two layers.

This process requires a patterning modality with the following characteristics:

1. Large-area patterning of 2DPC photonic crystals

2. Registration and Overlay

3. Efficiency in cost and time.

A lithography modality encompassing the breadth of these specifications is not available in the NanoStructures Laboratory. SEBL achieves the overlay required, but it is very expensive, slow, and covers small areas [40]. The Lloyd's mirror, which is employed several times in the course of this work, cannot meet the registration and overlay commitments. Optical steppers utilized in the semiconductor industry to manufacture the current generation of microprocessors potentially fit the bill, however they can cost over twenty million dollars and are not accessible to the research community. Section 3.4 and Section 3.5 investigate new modalities for lithography that can potentially capture the list of requirements.

3.3 Interferometric-Spatial-Phase Imaging

The first question that people ask when they hear the details of this project is: "How will you align the layers?". The 3DPC requires very tight tolerances not typically addressed in university research. The alignment requirements are within the bounds of SEBL. The initial fabrication attempt of the MIT Crystal utilized SEBL for the

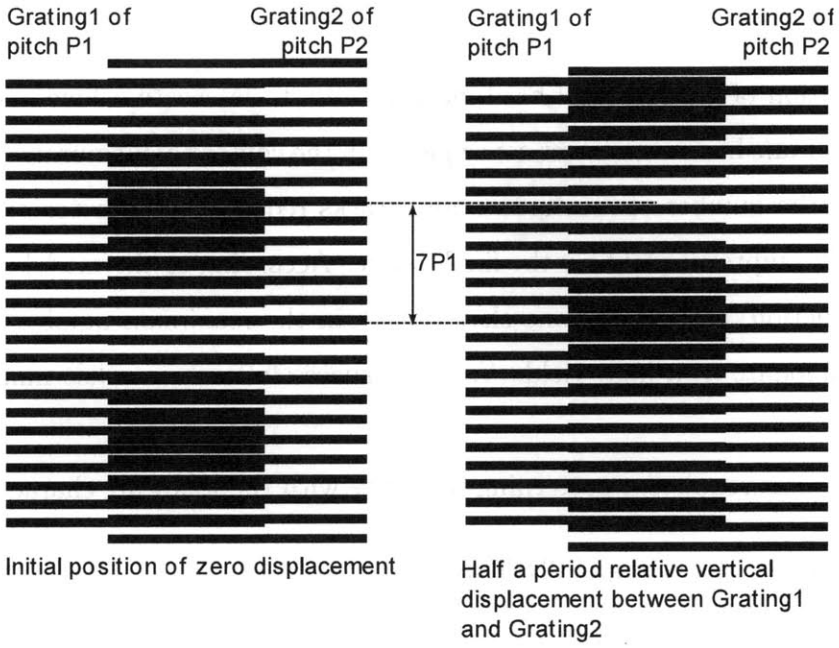

Figure 3-5: Moirè patterns and ISPI [Left] Two gratings of slightly different pitches overlap. We observe a beat pattern called moirè fringes. [Right] Grating 2 is displaced by one-half of a period. The fringes are displaced by a factor of 7×P1. This is a 14× amplification.

lithography and required overlay, which was sufficient for small-area exploration (i.e. within a single write-field). However, when we move toward large-area fabrication, the problems of alignment and overlay become one to two orders of magnitude more difficult.

The alignment requirement inspires us to explore a mask-based lithography approach over interference lithography. Here, we investigate two mask-based, high-resolution-lithography techniques and discuss their ability to address the core challenge. The task of aligning the mask relative to the substrate is accomplished with Interferometric-Spatial-Phase Imaging (ISPI). The core technical details of ISPI are comprehensively discussed in works by Euclid Moon [34, 35, 21]. ISPI, another offshoot of research in X-ray proximity lithography, offers the ability to detect 1nm lateral displacements and at least 50nm displacements in gap. While the details are discussed elsewhere, the intuitive grasp of this method is illustrated in Figure 3-5. When two gratings of slightly different period are overlayed, a moirè pattern with a

larger pitch is observed. A small displacement between the two gratings is amplified by a large (and thus more visible) shift in the moirè fringes. Absolute positions and relative offsets can be ascertained by a combination of P1 and P2 marks. ISPI builds on the moirè and offers off-axis illumination; this improves the signal-to-noise.

3.4 NanoImprint Lithography

NanoImprint lithography(NIL) is a candidate to replace optical projection lithography at the end of the semiconductor roadmap. Its merits include simplicity and high resolution patterning that is not limited by diffraction [31, 50]. On paper, NIL has the attributes to cover the objectives outlined in Section 3.2.1. While there is no dedicated commercial tool in the NSL like those sold by Molecular Imprints Inc (Austin, TX) and NanoNex (Princeton, NJ), there exists an experimental tool used once to fabricate a zone-plate array [21]. The experimental tool is inspired from the step and flash mode of NIL (SFIL). Figure 3-6 shows the simplicity of SFIL process.

1. Spin substrate with X-HRIC to serve as a transfer layer. This polymer is used as an ARC in optical lithography. It can be anisotropically etched with a helium/oxygen plasma.

2. Coat the template with a release layer that reduces the surface energy (the imprint resist should preferentially adhere to the X-HRIC). We used a proprietary blend from Molecular Imprints.

3. Parallelize the template with respect to the substrate using green-light interferometry (highlighted in the Chapter 5). The gap must be below 50μm for fringes to be visible.

4. Apply a 30nL drop of imprint fluid. This volume is sufficient to over the area of a 38mm diameter template.

5. Bring the template into contact with the substrate so that the imprint fluid can fill the voids. The only pressure applied is the weight of the template (pressure

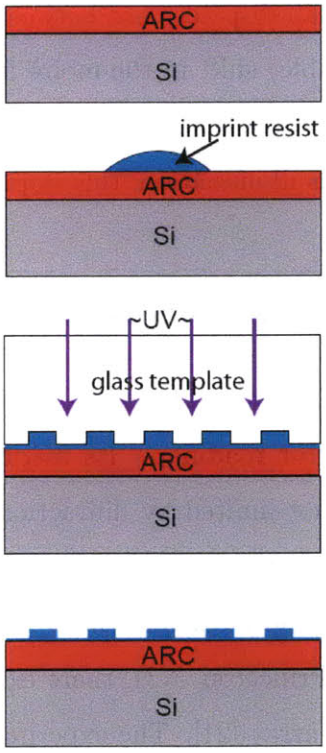

Figure 3-6: [1] Si wafer is coated with an ARC transfer layer. [2] After the template and substrate are parallel, swing out the wafer and apply droplet of imprint resist. [3] Bring the template into contact. [4] Remove the template. The pattern can be transferred using dry etch processes.

may improve results; it was not attempted).

6. Cure with UV radiation for four minutes.

7. Lift away template. Because of the pressure required, this was done manually.

The resist and nanopatterned template are the key technical components of SFIL. The resist is an organosilicon solution. It has very low viscosity and crosslinks when exposed to UV radiation. We used a solution containing 44% 3-Acryloxypropyl Tris silane, 37% of Tert-Butyl Acrylate, 15% of Ethylen glycol–diacryalte and 4% of Darocur 1173 Photoinitiator. It was mixed at the NSL and kept in the fridge [21, 16]. This solution etches in a CF_4 plasma, giving it good selectivity to the ARC transfer etch. Studies of the etch profiles can be found elsewhere[21].

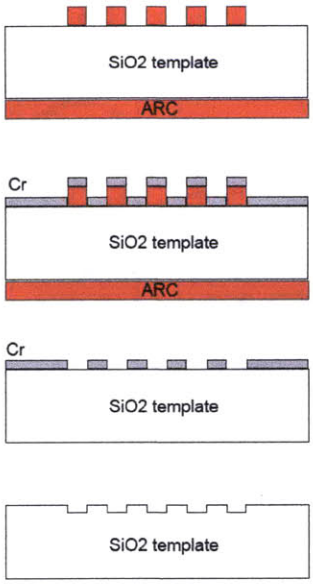

Figure 3-7: The process to fabricate the imprint template. The crucial feature is the backside ARC to prevent reflections. All solvent bakes are done in the oven to ensure uniformity.

3.4.1 SFIL Template

The standard template is a thick optical flat with a diameter up to 50mm. The pattern to be imprinted can be etched into the glass or grown on top. In line with the latter method, Mathias Galus [21] used SEBL to fabricate a template of zoneplates in HSQ negative e-beam resist. The zone plates covered an area less than one square millimeter. In order to better characterize the capabilities for SFIL, the first template fabricated in this work consists of gratings etched into the glass template. As is shown in Figure 3-7 the backside of the template must be coated with ARC to prevent backside reflections from distorting the pattern in resist during exposure. Then we continue with evaporation and liftoff, and RCA clean. The backside ARC goes away with the liftoff in EKC-265 and the RCA clean. RIE into the glass for a depth of 125nm using CHF_3 for vertical sidewalls.

Working with thick glass substrates is challenging because they need to handled firmly for processing but also cannot be contaminated with particles at the edges. We used wide teflon tongs to pick up the templates.

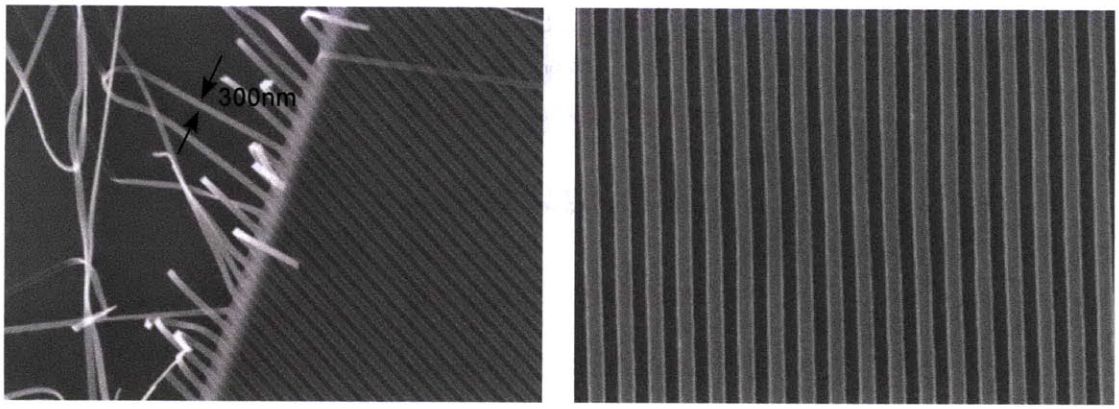

Figure 3-8: Scanning-electron micrograph of imprint resist after SFIL. Excellent replication of the mask is observed. On the left we observe some adhesion problems of the gratings to the substrate.

3.4.2 SFIL Results

Figure 3-8 shows a top view of gratings printed in the imprint fluid. We observe good pattern replication of the mask onto the substrate. We were able to print a grating covering the entire area of the template; this is a key strength of SFIL. Figure 3-9 shows cross-sections of the gratings formed in imprint fluid. It reveals the greatest shortcoming of large area patterning using SFIL. The resist thickness is not uniform over a large area. The residual-layer that sits underneath the pattern can vary greatly across the wafer, which ultimately prevents one from transferring the pattern into our device layer. The variation in thickness ultimately is linked to a variation in the gap between the mask and the substrate. The variation in gap results from many sources, including:

1. Particles on the mask and/or the substrate. The rigid surfaces cannot conform to accommodate the particles.

2. The fluid mechanics of the imprint fluid. We applied no pressure on the template to drive the fluid to spread uniformly.

Many of these challenges are being addressed by commercial NIL tools. One detrimental source of particles we observed was imprint fluid sticking to the template, as shown in Figure 3-10. The fact that the template can be compromised by the

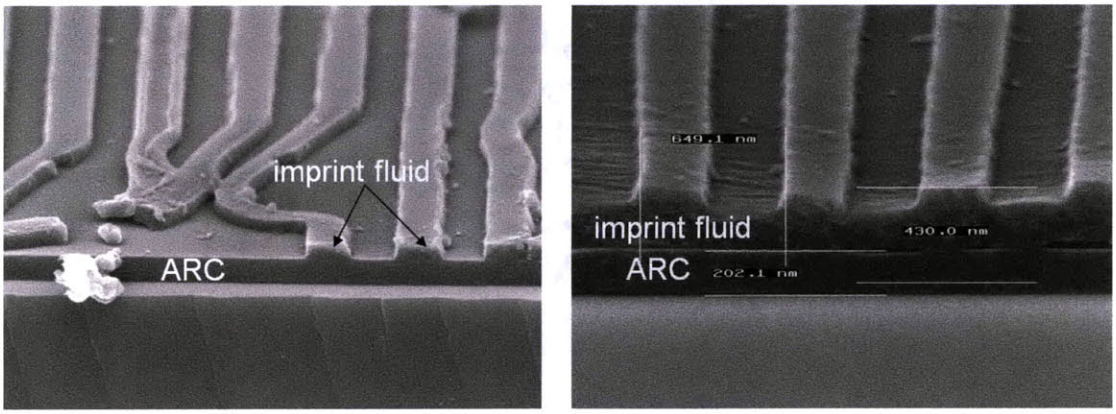

Figure 3-9: Scanning-electron micrograph of gratings in imprint resist. The residual layer is not constant thickness across the wafer. Both images are from the same sample but separated by roughly 3mm. Obtaining a very uniform gap is the key to resolving this discrepancy.

imprint process itself was the ultimate motivation to seek an alternative lithography modality. This problem may be addressed by commercial products and processes that were not available to the author.

3.4.3 SFIL Discussion

Ultimately, the decision was made to abandon SFIL development to concentrate on more pressing technical challenges. Many of the engineering hardships encountered are being addressed by commercial firms. However, there were two main shortcomings of this technology from our research perspective. First, the imprint resist contained too much uncertainty for long term success. Robust chemicals such as PFI88 and PMMA are requisite for quality and reproducible patterning. Imprint resist, with no technical support, was too much of a variable to worth betting on. If SFIL receives greater acceptance in the research environment more information will be available about the robustness of the chemicals.

But ultimately, particles between the template and the substrate are a major nuisance to achieving large-area and highly reproducible photonic features. Controlling particles across the full area of the template is difficult to pull off. This particular

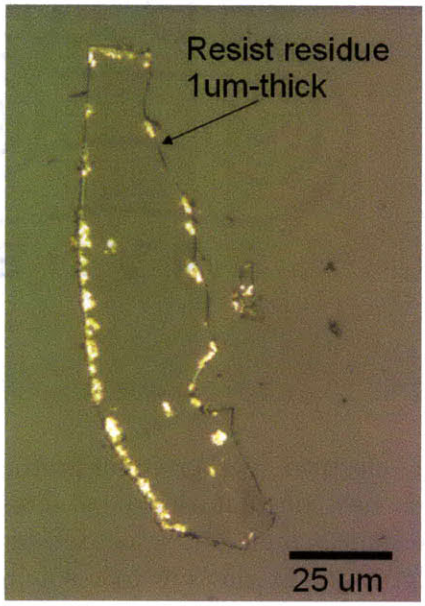

Figure 3-10: Imprint fluid on the mask template that stays behind after an imprint. It is 1μm-thick and cannot be removed with an RCA clean. Only physically scraping the residue removed it. The reason for contamination may come from poor application of the template release layer or the resist not functioning properly because it has expired.

fact motivated us to look in another direction.

3.5 Coherent Diffraction Lithography

After preliminary results from NIL proved disappointing, we took a deeper look at Coherent Diffraction Lithography(CDL) to see if we could overcome the main deficiencies of NIL. In the past, it was shown that hexagonal-close-packed periodic photonic structures could be replicated with high fidelity using a mask via the Talbot effect[58]. In simple terms, CDL is a mask-based interference lithography approach. A periodic pattern on a mask is illuminated with a monochromatic and collimated source(i.e. a flat phase front). This generates well-defined diffracted orders which combine downstream to reproduce the mask pattern. The planes at which the image reproduction occurs are called Talbot planes. The distance, Z_T between even and odd Talbot planes is determined by Equation 3.1.

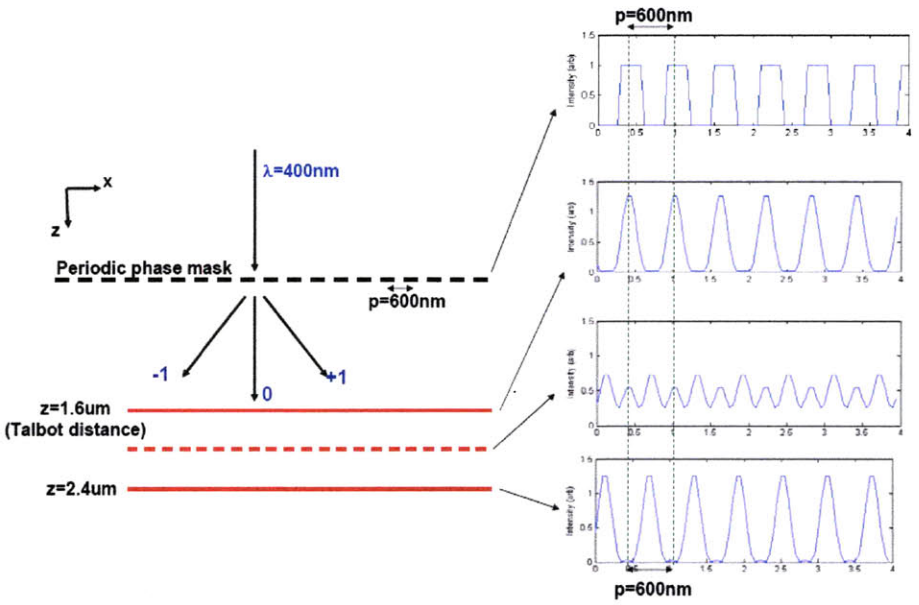

Figure 3-11: Schematic of CDL with accompanying simulation on the right. For the wavelength and master pitch selected in the example, only the -1,0,+1 orders propagate. Higher order modes become cut off (evanescent). The simulations clearly show how the intensity modulation changes with changes in gap. There are even, odd, and frequency doubling planes.

$$Z_T = \frac{1}{2}\frac{p^2}{\lambda}\left(1+\sqrt{1-\left(\frac{\lambda}{p}\right)^2}\right) \tag{3.1}$$

In Equation 3.1, p represents the pitch of the features on the mask, and λ represents the wavelength of the illuminating radiation. Figure 3-11 illustrates the periodic imaging from a grating amplitude mask with simulation results. The first Talbot plane is even and in-phase with the master grating. The second Talbot plane is out-of-phase. In between these two distances is a frequency doubling region which suffers from lower contrast.

3.5.1 CDL Tool Development

Our recent contribution has been to develop a dedicated CDL prototype tool that integrates the mask illumination optics and phase mask with ISPI gap control. The fabrication of a basic grating CDL mask follows the process for developing the SFIL Template in Section 3.4.1. The gratings were patterned with the Lloyd's Mirror (Section 2.2). A mix and match scheme was utilized to fabricate the ISPI gapping marks. After the gratings were selectively etched into a 1cm $\times$ 1cm square on the mask, a layer of chrome was evaporated and PMMA was spun on. The ISPI marks were designed by Euclid Moon and written using the VS-26. The subsequent processing is detailed in Section 7.4.

The prototype tool is depicted in Figure 3-12. A diode laser operating at $\lambda =$ 405nm and 60mW (procured from Power Technologies, Inc.) is directed into a spatial filter to remove noise and then collimated with a lens. The beam expands to a diameter of 25mm before collimation. The intensity profile is Gaussian. Ideally, one would expand the beam more so that the mask samples a flatter intensity profile. After collimation the beam travels downstream until it illuminates the mask, which has been leveled and set to the desired gap. While the tool is simple in terms of optical design, packaging it within the laboratory constraints required innovative mechanical and optical design. This engineering problem was attacked by Corey Fucetola. The exposing beam had to be completely confined for the safety of the NSL cleanroom

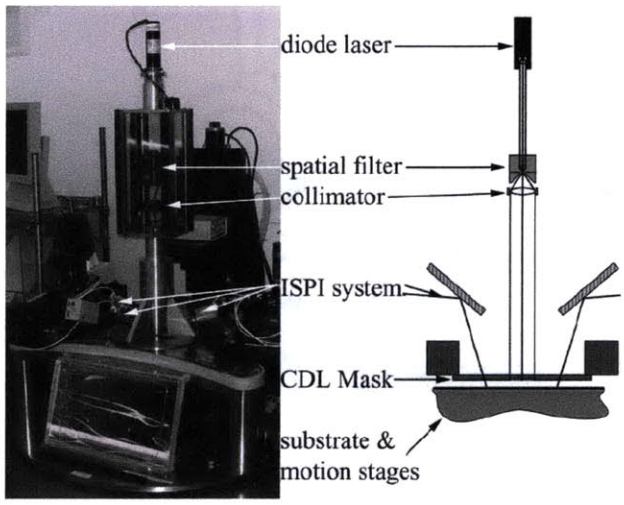

Figure 3-12: The CDL tool is designed by Corey Fucetola. This optical path consists of a source, spatial filter, collimating lens, the phase mask and the substrate.

users. Additionally, the optics had to be mounted on to an ISPI platform, which constrained the location of mirrors, sources, etc.

We demonstrated that CDL can overcome the problems faced by NIL. Because CDL is an optical interference lithography method, one can use the robust processes that are used with Lloyd's-mirror IL. Additionally, we show that CDL can work at large gaps well beyond any risk of interference from particles [17].

3.5.2 Exposure Results

The tool and mask were used to expose wafers coated with the PFI88 trilayer stack described earlier. We first conducted a wedge exposure where the mask was tilted at 5mrad with respect to the substrate. This allowed us to capture the 1st to the 52nd Talbot planes (a gap range from 1.55μm to 40.16μm). Figure 3-13 shows the transitions between different imaging planes as the gap changes. There is a gap progression of 772nm between the dark bands which represent the frequency doubling regions. Within this band we obtained a depth of focus $> 50\%$.

We also performed a uniform-gap exposure at 2μm, which is shown in Figure 3-14. The absolute gap was obtained using the transverse-chirp gapping marks, printed on

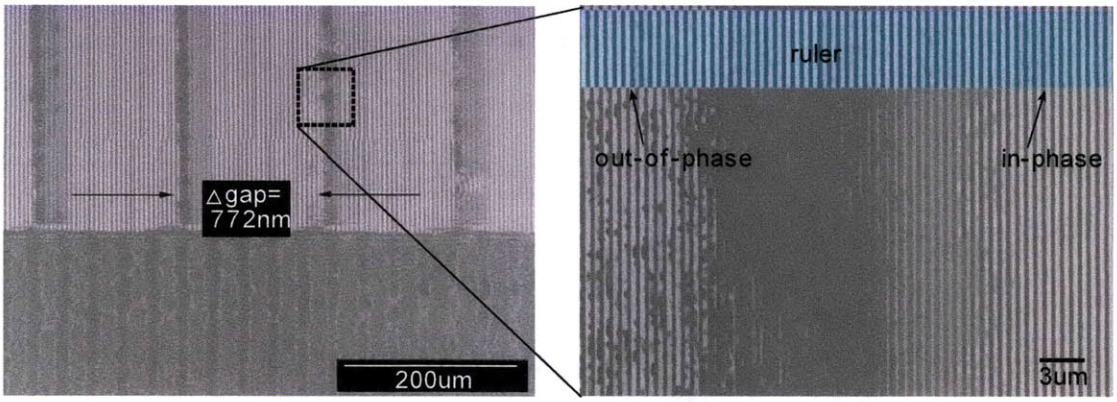

Figure 3-13: Evidence of Talbot imaging. The mask is tilted relative by 5mrad to the substrate and illuminated. This enables us to observe Talbot planes in resist. [Right] We see an even Talbot plane and odd plane separated by an unresolved frequency doubled region. The change in gap between the two regions is 772nm.

the mask. We are currently pursuing more experiments to test the repeatability of the ISPI gapping marks. Figure 3-14 also shows the first demonstrated replication of patterns with square symmetry. The mask used for this exposure was a membrane containing a 2D photonic-crystal pattern, fabricated in Chapter 2.

3.5.3 CDL Discussion

We have obtained very promising results for CDL. The current focus is on improving uniformity of the exposure across a large area. There are several avenues to pursue. First we want to improve the beam profile in terms of phase and intensity flatness. The current tool constraints have limited our exposing beam to only 25mm in diameter. A 100mm beam would provide a more uniform dose over our 25mm region-of-interest.

Next, we must improve the design of the phase mask. The early masks were not fabricated with optimal phase steps. Simulations can help us obtain this goal. Furthermore, a new fabrication process for phase zone plates is being developed so that a very precise etch depth can be achieved using RIE.

Finally, a significant challenge is mask handling during fabrication. Because we use the zero order for imaging, spatial-frequency components that arise from scratches

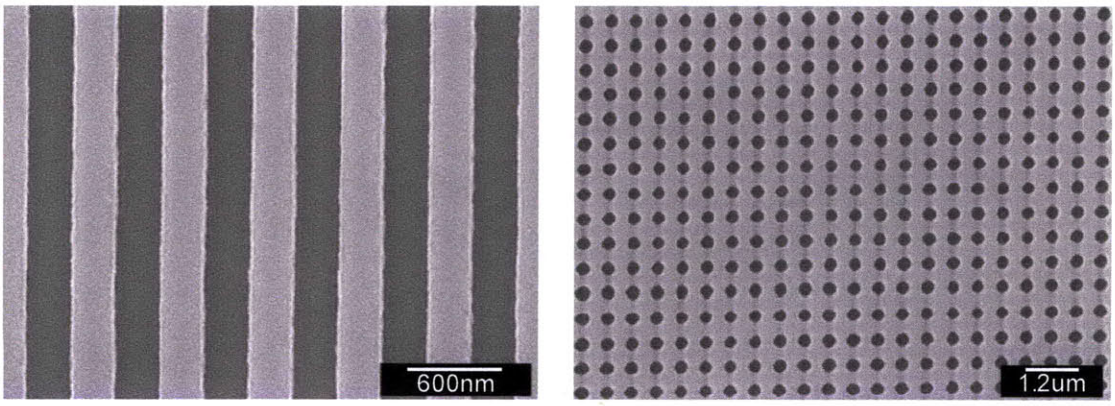

Figure 3-14: [Left] Gratings exposed in PFI88 using a CDL mask. [Right] Grid pattern in PFI88 that was generated from a SiN-membrane mask.

on the bottom side of the template can distort the image. It is very difficult to protect the bottom size of the template during processing. One potential solution that was alluded to, is the use of large-are membranes etched with the photonic pattern. In this case, the backside surface is never handled and it is very near the exposing plane; a defect will only affect a small area.

3.6 Conclusion

We developed the dual-hard-mask process to pattern the hole and rod primitive structure without material deposition and planarization.

We looked into new modes of lithography that enable the overlay requirement we need. We investigated SFIL and CDL, whose merits are summarized in Table 3.1. We strongly feel that CDL offers a path toward realizing our goal. We were successful in pattering gratings and square symmetric patterns. The focus now is to scale up the area by improving tool and mask design.

Table 3.1: Summary of the capabilities of next generation lithography modes investigated for 2DPC patterning.

Modality	robust resist	one mask	ISPI compatible	resolution (p=600nm)	non-periodic?
CDL	√	√	√	√	-
SFIL	-	-	√	√	√

Chapter 4

Bonding Membranes to a New Substrate: Part I

4.1 Introduction

This chapter is the first of two parts that deals with the challenge of bonding a free-standing membrane that has been prepatterned with a photonic crystal onto another substrate. Part I introduces the area of membrane transfer, sets the foundational architecture and presents the first success in membrane transfer. Part II improves repeatability and presents analysis of our results.

We will rely on van der Waals interatomic forces to provide adhesion between the film and the substrate. The membrane stacking architecture is designed so that the stacked structure is complete after the final stack. It will not require any more processing. So while van der Waals forces are relatively weak they are sufficient to keep the structure in tact.

This chapter should be read through the lens of our goal for realizing the 3DPC. At the time of the publication of this thesis there does not exist a membrane bonding technology that achieves the goals we require for 3DPCs. We desire to have a technique for membrane bonding that allow for multilayer nanostructure fabrication. In conjunction to the construction of a multilayer structure, we require overlay between layers. Because the focus is on large integrated photonic systems such as the CROW,

we need a large area solution ($> 1\text{cm}^2$). Finally, materials must be compatible for optical devices. Ideally, we should build a homogenous materials system of dielectrics. The introduction of metals will introduce loss.

4.2 Review of Work in the Field

4.2.1 X-ray Lithography

The NanoStructures Laboratory has a trailblazing history in the development of X-ray proximity lithography. A membrane amplitude mask is brought within 5μm of a substrate coated with PMMA. The PMMA is then exposed with X-ray radiation, which cuts up the long polymer chains making them soluble in developer. The spatial resolution using this technique is a function of the minimal achievable gap, G.

$$G = \alpha \frac{w^2}{\lambda} \tag{4.1}$$

The finest sub-50nm resolution is only achievable via intimate contact with the substrate [25]. The theme of achieving these small gaps is one of the core technical challenges that resonated within the NanoStructure Lab during the 1990s. We present three of the most successful variations here.

Backside Air Pressure

Isabel Yang had to transfer features from a quartz mask onto a resist-coated membrane. In her configuration, the X-ray mask sits at 5μm gap relative to the mask. The fixed gap is achieved by aluminum studs that circle the outside edge of the x-ray mask. The gap is reduced below 1μm by applying pressure from the backside [56]. The membrane stretches to accommodate the pressure. While this method does reduce the gap, it does not enable uniform contact across the entire membrane region. We repeated the experiment with an X-ray mask and the result is presented in Figure 4-1. The quality of the bond is poor. In fact Yang was able to unbond the surfaces by removing the pressure. It is inconsistent across the region and particles

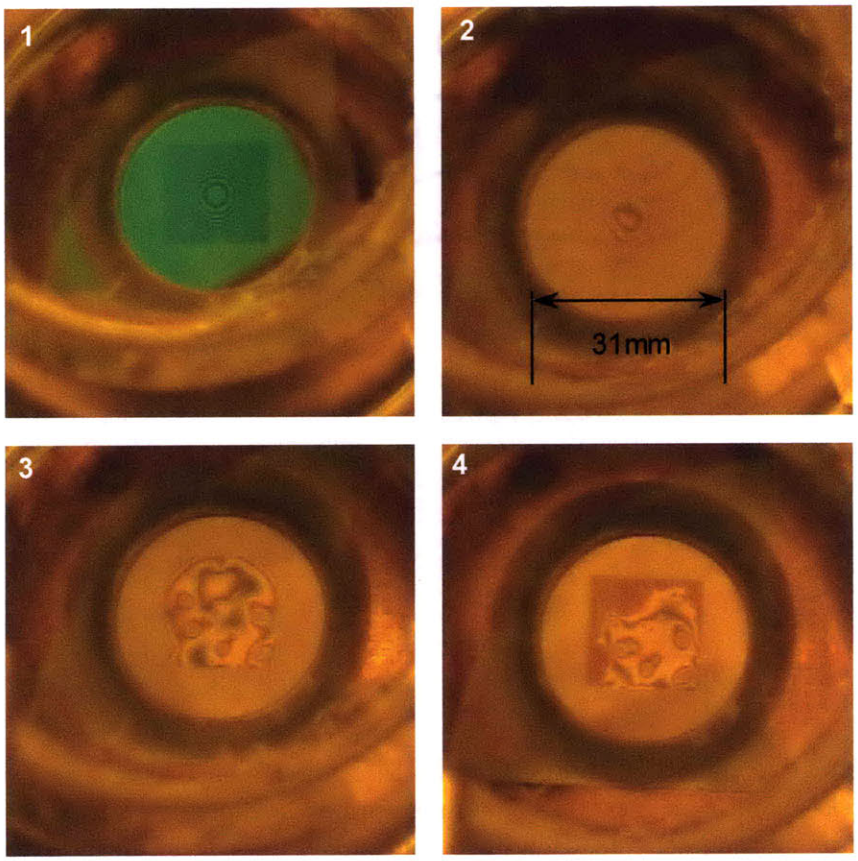

Figure 4-1: The backside pressure experiment. [1] Pressure is applied within a special box covering the X-ray mask. We observe bow in the membrane via interference fringes. [2] Center region comes into close proximity. [3] while light interference fringes over square substrate. [4] Final bond after two hours.

cause large disruptions in the contact region. The viability of this technology for 3DPCs is hindered by the fact that air pressure creates distortion in the membrane which will counter the desire to achieve overlay. The squeeze film of air between the two surfaces hinders a bond from propagating.

Suck and Puff Method

David Carter also attacked the problem by using a pressure differential between the front side and back side of the membrane to drive into contact with the substrate. However, he understood that the squeeze film between the mask and substrate played a large role in preventing intimate contact. Therefore, he applied a vacuum between

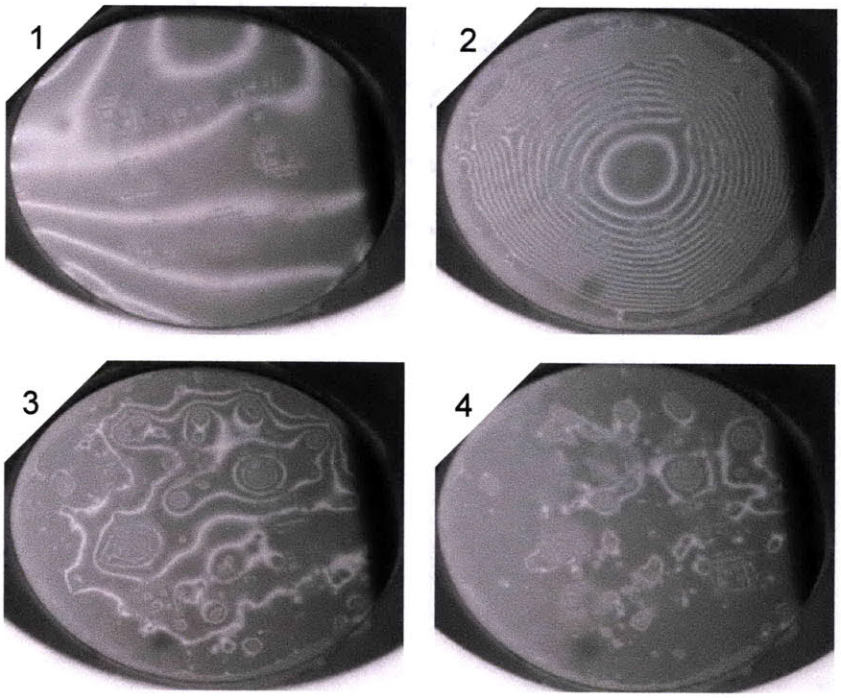

Figure 4-2: The suck and puff method. [1] Interference fringes as X-ray mask sits at 5μm gap. [2] Vacuum is applied between the surfaces and the membrane deflects. Bonding occurs from the edges. [3] Intermediate bond. [4] Final bond. Figure taken from reference [14]

the two surfaces to force contact. Figure 4-2 shows images taken from his experiments showing the evolution and quality of the bond [14]. In this configuration the outside edges feel the vacuum first and therefore are the first to contact. This leaves an air bubble in the central region. He uses shallow grating channels that are patterned on the membrane surface. This gives the air an escape path and slowly the membrane comes into contact with the surface. The settling time is on the order of 60 minutes. The membrane is pulled out of contact by applying pressure slowly to the same line that vacuum was applied. This method achieves a better result than the Yang method but we still observe large regions of poor bonding.

Electrostatic Potential

Reza Ghanbari and Bill Chu ventured away from pressure differentials and applied electrostatic potentials between the substrate and mask[22, ?]. The X-ray mask has

a plating base layer that serves as one of plates of the capacitor. When the two surfaces are in close proximity a voltage of 40-100V is applied, which drives the membrane into contact. Van der Waals attraction keeps the substrates attached even after the potential is removed. Catastrophic membrane failure is the glaring disadvantage of this method [14]. There often is arcing of charge between the surfaces which lead to breakage of the membrane. This is ultimately a low yield membrane bonding technique. In addition the metal material system required is ultimately not compatible for our photonic application. We seek a homogenous dielectric material systems.

4.2.2 Silicon Nanomembranes

Silicon-on-Insulator (SOI) technology has been a key development for the semiconductor industry in its efforts to battle leakage currents in shrinking devices. The quality of SOI wafers has dramatically improved in the last decade. It offers a very uniform crystalline silicon membrane. This, in turn, has led to new research into free-standing silicon nanomembranes. The buried oxide of the SOI wafer serves as a natural sacrificial layer enabling easy release of membrane structures. Here we explore two methods used for transferring silicon membranes to other substrates.

Wet Release

Researchers at the University of Wisconsin at Madison have developed a wet release technique for transferring silicon membranes to flexible polymer substrates [29]. Access holes are etched into a silicon membrane along with a square border. The SOI wafer is then placed within a hydrofluoric acid solution (HF) so that the oxide is undercut and a membrane is completely released from its frame in the solution. The floating membrane is then picked up from below by another substrate. The maximum area achieved with this technique is 4mm $\times$ 4mm [3]. While this method would potentially allow one to prepattern the substrate with a 2DPC pattern (which would also provide access holes), there is no available method for alignment and overlay since the

membrane release and transfer takes place in solution. Therefore they have limited their research to single layer devices such as transistors on flexible. The majority of processing is done after the membrane transfer.

Membrane Stamping

John Rogers is a proponent of the PDMS soft lithography approach initiated by George Whitesides at Harvard. In this scheme,free-standing silicon membranes are released from the sacrificial layer, but remain attached to the frame (as opposed to the Wisconsin method). The membranes are picked up with a polydimethylsiloxane (PDMS) stamp via adhesive forces. The membranes are then transferred to another substrate. The PDMS is released from the silicon with an optimized peel-back method. While this technique is powerful in transferring silicon structures to flexible substrates and the like, it does not provide the possibility for overlay because the PDMS stamp is not rigid. The area of the pickup is limited because of the peel back method. Rogers group succeeded in peeling back large areas of isolated islands. However, large-area continuous membranes, required for 3DPCs, fracture in this process[3, 32].

4.2.3 NanoOrigami in Silicon Nitride

There has been an initiative at the NanoStructures Laboratory toward building 3D structures by folding silicon nitride membranes. The folding is actuated by stress engineered "hinges". Actuation is done by a bi-layer metal stress [7], ion implantation [8](see Figure 4-3), or magnetic force [36]. This method, named NanoOrigami because of its relation to the Japanese art of paper folding, creates a simple method for building multilayer stacks of 3D NanoStructures without the typical constraints of wafer planarization and material deposition. Taking advantage of planar processing, all the layers can be processed in parallel on a single membrane and then folded together to form a 3D structure. To date they have demonstrated only two-layer stacks; however, there is potential to quickly build a multilayer structure in a matter

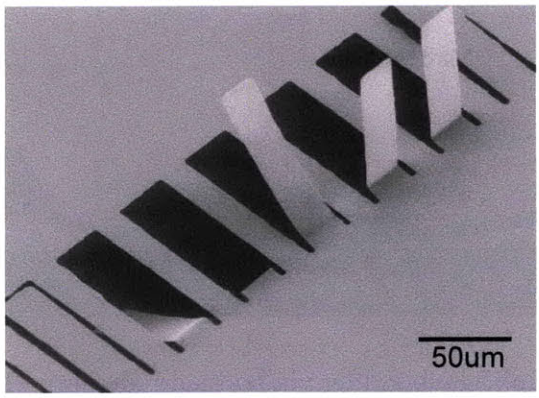

Figure 4-3: SiN cantilevers that have been induced to fold by ion implantation. The implantation creates local stress gradients. The depth of implantation determines the folding angle. No path for large area has been demonstrated using the NanoOrigami technique. Taken from reference [8].

of seconds. The folding regime has been limited to areas on the order of 100μm $\times$ 100μm. Additionally, the approach depends on nanomagnets for adhesion and alignment. This requirement further limits the usable area for photonic applications. While NanoOrigami may have interesting niche applications, it does not provide a comprehensive solution toward the goal of 3DPC nanofabrication.

4.3 SiN Membrane Bonding: Iteration One

The experiment discussed in this section is depicted in Figure 4-4. The 2DPC silicon nitride membranes, fabricated earlier, are the samples used here. The membrane wafer is manually brought face-to-face with the substrate. While we desire for the membrane to go into contact with the new substrate, there inevitably is a nonzero gap. There are several reasons for the gap:

1. There is squeeze film of air trapped between the two surfaces. Often the two surfaces will slide against each other.

2. There are particles on the surfaces that prevent intimate contact between wafers. Particles are typically generated during wafer cleaving and handling with tweez-

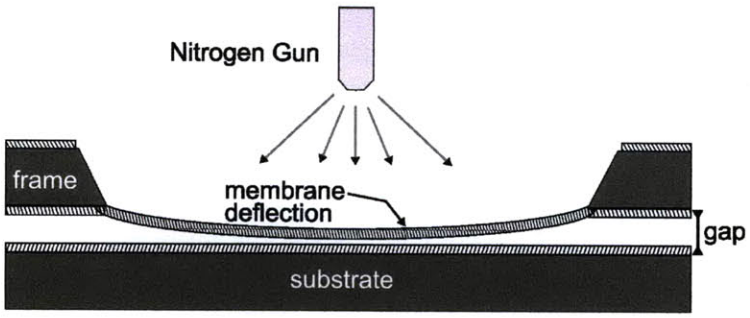

Figure 4-4: Membrane bonding via backside pressure. The samples are brought together manually. Any gap between the surfaces is compensated for by blowing nitrogen from the back and forcing the membrane to stretch. This is not the ultimate solution presented in this body of work.

ers. It is nearly impossible to keep the edges of a sample particle free. A quarter of a 10cm wafer is the used for efficiency. Whole wafers could be more effective because we avoid cleaving; they are more difficult to process.

3. Wafers have a natural bow. This curvature of surface results in small contact areas between wafers. Figure 4-5 is a map of wafer curvature for a typical 10cm wafer.

The gap is closed by applying a pressure on the backside of the membrane with a nitrogen gun as was done by Yang[56]. The membrane will stretch and go into contact to accommodate the pressure from the backside. If the pressure is removed, the membrane will spring back out of contact. Silicon nitride membranes have a remarkable resilience to handling pressure loads normal to the surface (they are used as vacuum windows). X-ray mask membranes are strong enough to withstand pressure manually applied by a Q-tip. In fact, the Q-tip shaft will break before the membrane gives[14].

However, membranes are weak to shear force. If there is relative lateral displacement between the handle wafer and the substrate while the membrane is in contact with the substrate, the membrane will shatter.

Section 4.4 and Part II discuss methods for gap reduction without applied pressure.

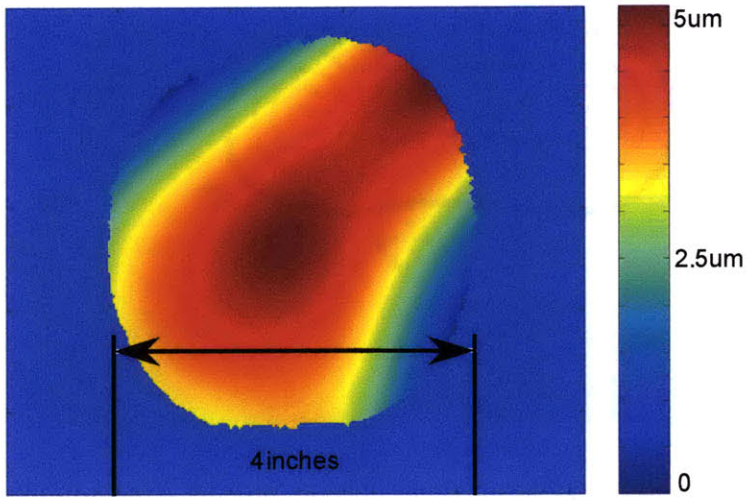

Figure 4-5: The Wyko surface profilometer measures a 5μm amplitude in the bow across an entire 10cm wafer in its resting state (no vacuum chuck).

4.3.1 Surface Preparation

The quality of the interfacial bond is a function of surface roughness and freedom from organic surface contamination. After the membrane has been released, the wafer must be cleaned in Pirhana (3 H_2SO_4: 1 H_2O_2) and RCA as described in Section 2.4.2. Typically, a sample may sit in fluoroware packaging for hours or even weeks waiting for bonding. This leads to the accumulation of organic contamination. Surfaces (i.e. face to be bonded on membrane and substrate) must undergo a plasma ash right before bonding. Settings for the plasma ash are as follows: 200W for 5 minutes with 350mTorr of He/O_2.

The steam-nucleation test is used to visually verify that a surface is free from contamination [48]. A shallow beaker with DI water is placed on a hotplate. Set the hotplate such that a gentle steam emanates from the surface. The surface in question must be held perpendicular a few centimeters above the water bath. Contamination is indirectly observed if a layer of microscopic water beads forms on the surface (the surface will appear dull). The steam will form a continuous film on a clean sample, evident by white-light-interference fringes spanning the entire surface. If one uses this test to confirm that a surface is contamination free, that surface should be ashed

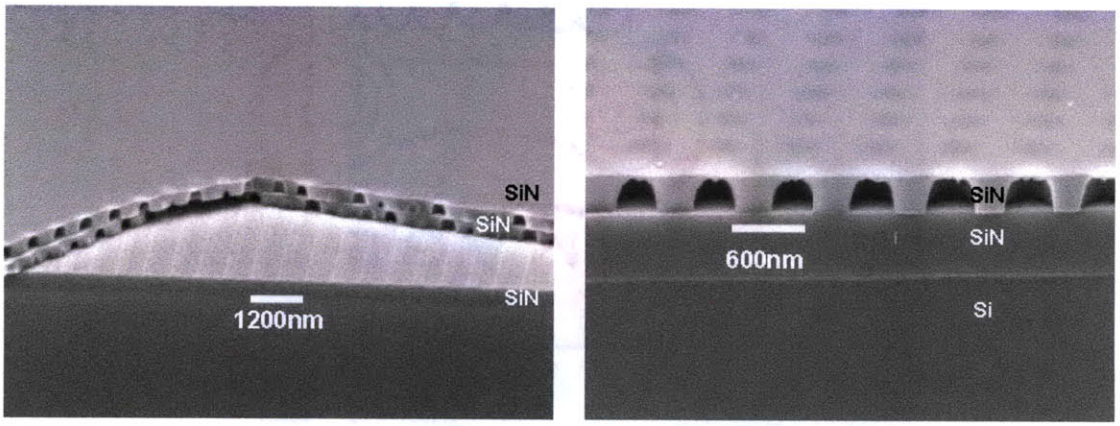

Figure 4-6: SiN membranes bonding via van der Waals forces. They were brought into contact by backside pressure. [Left] Two membranes on top of a patterned substrate, forming three layers. [Right] Cleave of a patterned membrane on a plain substrate. The maximum usable area is about 2mm $\times$ 2mm.

again to removed water saturated on the surface.

4.3.2 Results

Figure 4-6 shows patterned membranes stacked on substrates demonstrating three- and two-layer stacking [38]. From the manner in which the cleave propagates, we observe that van der Waals attraction between the two surfaces is sufficient for our application. The deficiency of this result is the small area, which is caused by nonzero gaps. The next section discusses how that can be overcome.

4.4 Mesa-Enabled Membrane Stacking

Because of the nonzero gap complications that arose during the bonding experiments described in Section 4.3, we propose an improved architecture for membrane stacking. Rather than using whole-wafer substrates, smaller area substrates that are elevated more than 100 μm above a baseline level are used. Figure 4-7 highlights this concept.

There are an impressive number of advantages that come from using raised substrates:

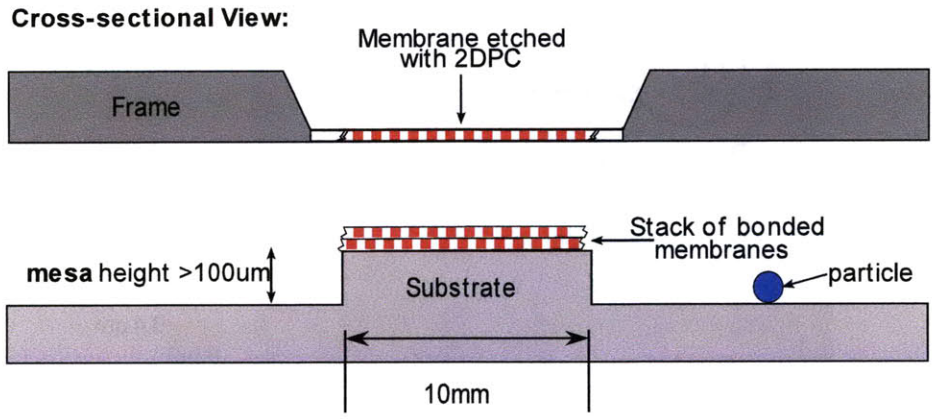

Figure 4-7: Membrane stacking with a raised substrate. The highlighted particle does not prevent a zero gap. The lower edge of the mesa is a safe region for handling the substrate.

1. Particles that are not in the region of interest no longer prevent a zero gap.

2. The challenge of wafer handling is solved. Tweezers generate particles at the wafer edge. However, the lower part of the mesa is a safe region for handling.

3. Wafer bow is negligible with the reduced area. Figure 4-8 shows that we are able to achieve a bow under 200nm without a pinchuck.

4. We dramatically reduce the path required for the trapped air to escape.

5. The deep mesa provides sufficient space to maneuver during the parallelization process.

6. We can stack a layer onto a substrate without affecting the other membrane layers on the frame. If we used a whole wafer as the substrate, all the membranes on the frame would be transferred simultaneously.

4.4.1 Mesa Fabrication Process

Figure 4-10 shows the process employed to generate high quality particle-free mesas. The first functional photonic layer is patterned on the mesa. However, a mesa can be created without a pattern. The dimensions of the mesa can be precisely controlled

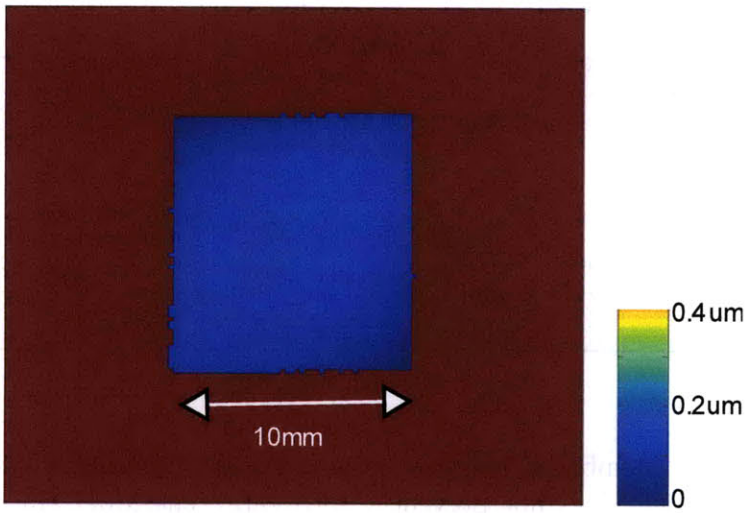

Figure 4-8: Wyko measures a 150nm peak wafer bow for a mesa on a quarter wafer sample not held with a pin-chuck. The interferogram was produced on the Wyko profilometer.

with a photomask. Because KOH etching of Silicon is preferential to the crystallographic planes, the mesa mask should be aligned to the crystal of the wafer. This can be achieved using the alignment scheme described in Figure 2-12 in Chapter 2.

Figure 4-9 shows micrographs of finished mesas after cleaning. These surfaces are free of particles and contamination. The edges will remain clean and free from tweezer scratches. This condition is necessary for proper bonding.

4.4.2 Result with Mesa-Enabled Membrane Stacking

The first large-area and particle free membrane stack was obtained using raised substrates to minimize the gap in conjunction with application of backside pressure with a nitrogen gun. The membrane bonded within minutes. The mesa helped us achieve a very small gap; the membrane did not recoil when the backside pressure was removed. The membrane was then detached from the frame using a razor. Figure 4-11 is a picture of light diffracting off this two level photonic crystal. The bonded region is 10mm $\times$ 10mm. Figure 4-12 shows close up images of the freestanding cross grating structure. As we can see in Figure 4-12, a large contact region is achieved without significant interference from particles. This result sets up the work in Chapter 5 and

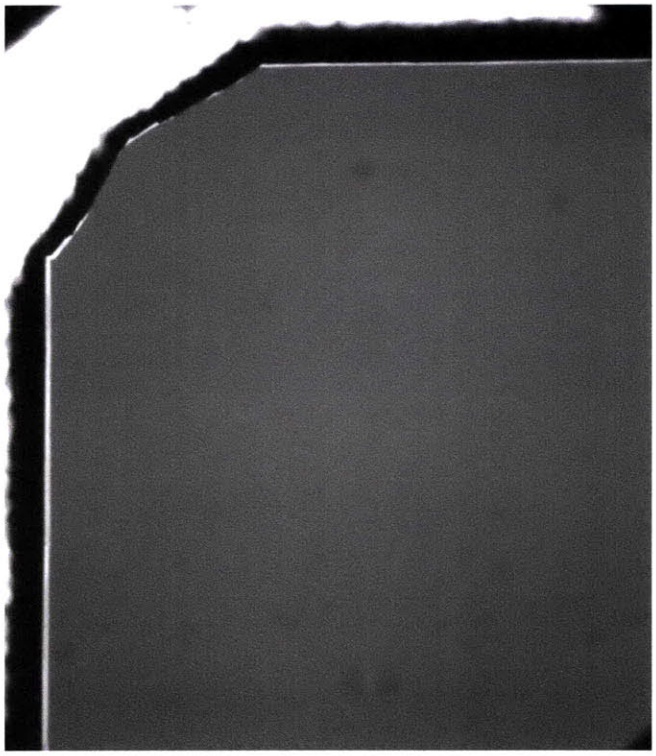

Figure 4-9: The corner of a mesa remains particle free, ensuring close gaps.

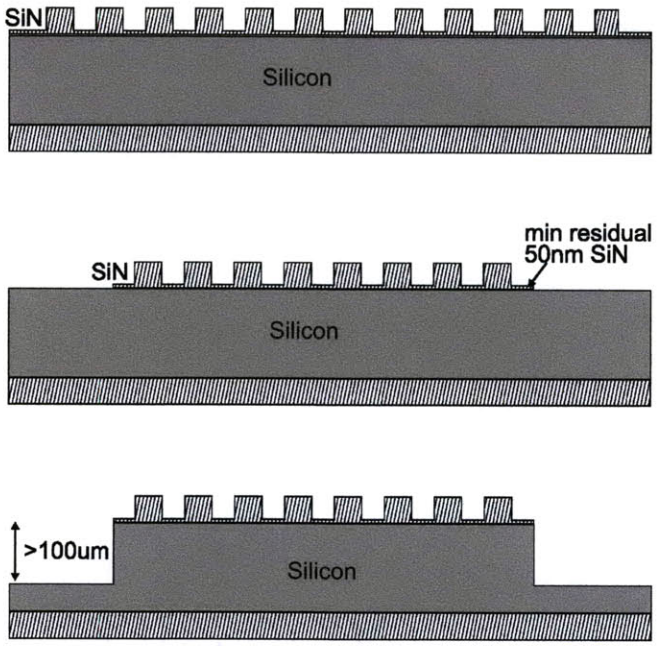

Figure 4-10: Fabrication process for mesa substrates. [1] Assume that we start with a plane SiN wafer or one patterned with a grating. In the patterned case,the features should not be etched completely through the SiN. [2] Mask off mesa region with thick resist. RIE SiN outside this region until it clears. [3] KOH etch for 1-2 hours to form mesa. Standard cleaning should be done post KOH.

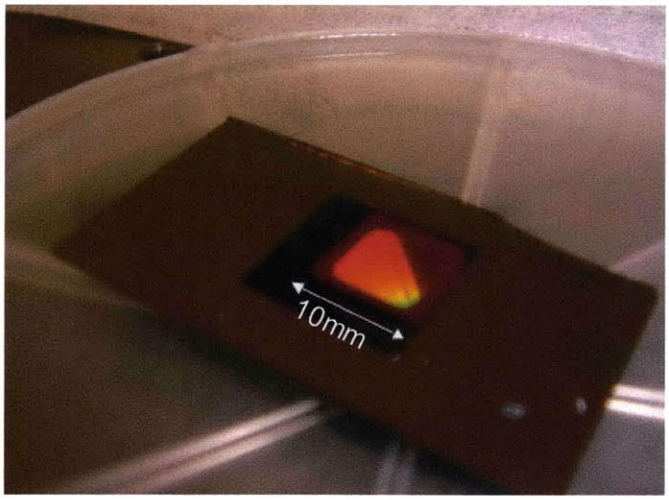

Figure 4-11: The first large-area, two-level silicon nitride structure fabricated by membrane stacking. 10mm × 10mm using a mesa and backside pressure. There were only five particles present in the device region, implying success of new handling techniques. The membrane was cut by razor, which causes poorly defined edges and particles at edges.

Chapter 6. The first goal is to make this success robust and repeatable because only one out of ten membranes yielded. The second challenge is addressing the detachment of the membrane from the frame. We also observe poorly defined edges and the existence of particles because we detached the membrane with a razor. Chapter 6 discusses the solution to this problem so that we may stack multiple layers on top of each other.

4.4.3 The Case for Membrane Stacking

The result in Figure 4-12 nicely elucidates the advantage of the membrane stacking approach over traditional layer-by-layer fabrication. In the former, the mesa and the membrane were fabricated in parallel, inspected for defects with optical microscopy and assembled in a matter of minutes to form a complex freestanding two-level structure.

Can this structure be fabricated using the standard process in a research facility such as the Microsystems Technology Laboratory at MIT? Assuming the first layer grating is complete, we must do the following processing to get the result presented

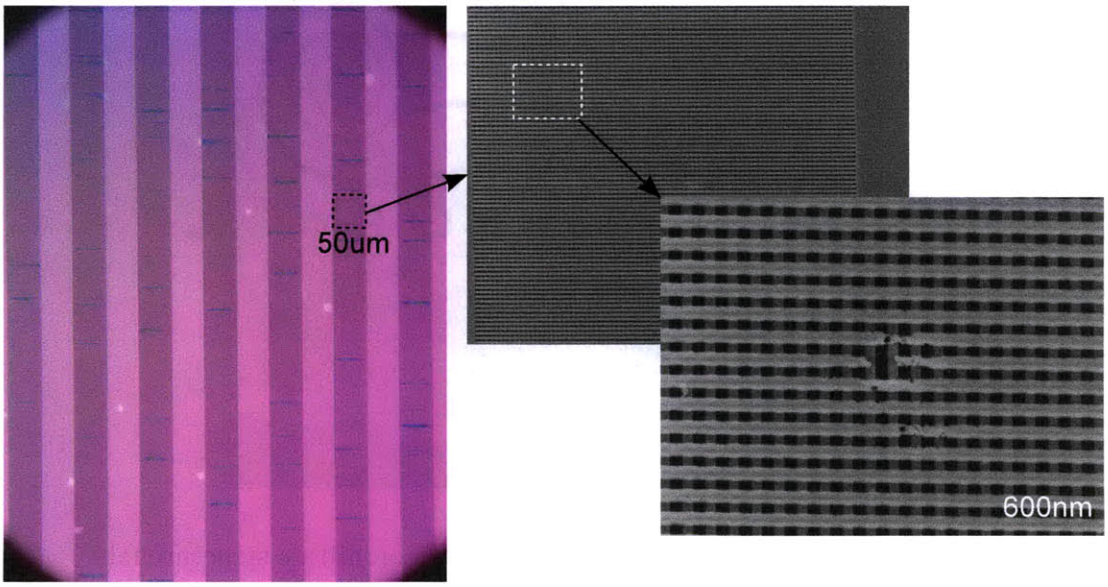

Figure 4-12: Micrographs of the transferred membrane in Figure 4-11. In this example a cross-grating structure was fabricated rather than the 2DPC.

in Figure 4-12:

1. Fill back the structure with oxide and chemical mechanical polish (CMP) the surface.
2. Low pressure chemical vapor deposition of a new layer of silicon nitride
3. Spin photoresist stack and expose grating with interference lithography
4. Evporate metal mask and liftoff photoresist
5. RCA clean
6. Dry etch the silicon nitride
7. Wet release of sacrificial oxide in HF

An optimistic estimate for the execution of these processing steps is one week. This compares with an execution time of minutes for membrane stacking. What about quality and yield? The traditional route requires many 'high risk' processes.

CMP at MTL is not reliable for the film thickness desired. Deposition accuracy for the second level of SiN can vary ±10nm from the target thickness. The dry etch process is also high risk because there is no etch stop. We can easily overetch into layer one, altering the structure. Ultimately, there is an increase in processing time and total cost of the final structure. There is also less of a guarantee that the result is the one we want. In membrane stacking we can inspect the layers for dimensional accuracy and unwanted defects to increase our chance for yielding a good device.

This analysis for one a two-layer structure. What happens when we extrapolate this to a ten layer structure? The math tells us that the traditional fabrication model is low yield indeed.

Chapter 5

Bonding Membranes to a New Substrate: Part II

5.1 Introduction

In Part I we successfully bonded a large-area photonic crystal membrane on a mesa substrate and discussed how the stacking method prevails over the traditional layer-by-layer process. We build on this significant result and establish two goals to this chapter. First, we will make the stacking process more repeatable and reliable in order to have a good stacking yield, P_S. The key here is to integrate stacking with ISPI gap control. The second is to better understand the bonding mechanism by attempting a variety of bonding experiments with different types of membranes and substrates. We will then do some analysis to understand the bonding results in the context of bonding theory.

5.2 Gap Control with ISPI

The key to repeatable membrane stacking is the controlled leveling and gap reduction between the membrane and the receiving substrate. As we have already introduced in earlier sections, we use the ISPI tool available in the NanoStructures Laboratory. Figure 5-1 shows a schematic for the coarse gapping capability used for membrane and

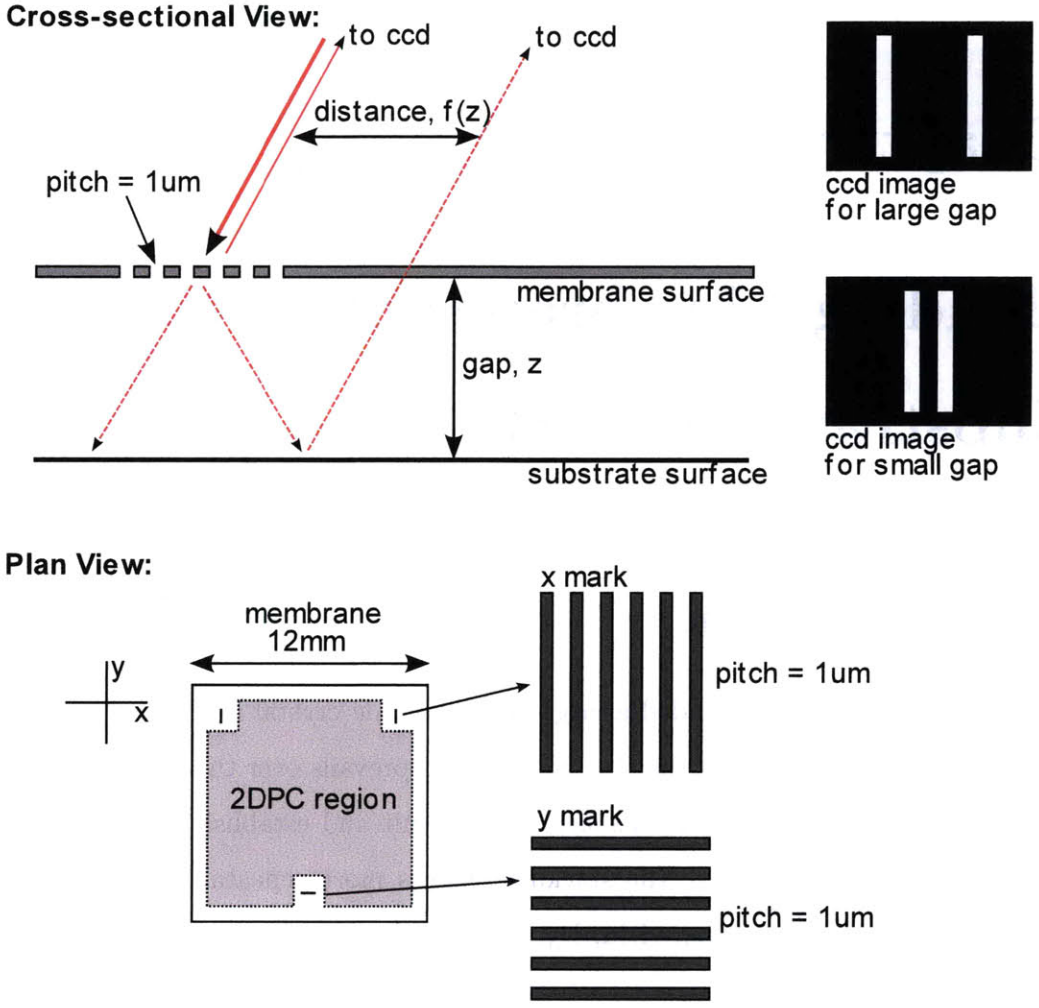

Figure 5-1: The coarse gapping ISPI scheme used to level membranes relative to mesa. In the plan view we see the layout of the 3 alignment marks relative to the 2DPC (see Figure 5-6). Three gapping points establish the plane of tilt, and we use these points to parallelize the membrane relative to the wafer within 5μm gap variation across the wafer. This gapping scheme can work up to 500μm where wafer maneuverability is unhindered. The cross-sectional view shows how a grating is used to collect gap information. We illuminate the mark at the Litrow angle and image the back diffracted order and the first-order which reflects off the substrate. The mark can distinguish gaps from zero gap to over 500μm.

substrate parallelization. ISPI allows us to capture quantitative information of the gap at three points. We map the gap information into tip and tilt stage movements until the gap is uniform over the three points (each gapping mark is spaced by 10mm from the others).

Because ISPI relies on a coherent source illumination of $\lambda = 632$nm, we can receive gap feedback at gaps exceeding 500μm. The ability to level at such a large gaps gives us space to maneuver the membrane wafer without crashing into the substrate at the far edges.

The ISPI coarse gapping marks enable us to get the two surfaces approximately parallel (within 5μm gap deviation). Further discrimination is beyond the resolution of the marks. However, at a close gap under 50μm we can utilize monochromatic-green-light illumination to track tilt of the membrane relative to the substrate. The tip and tilt actuation is done with human feedback from the green-light fringes. Once parallelized, the gap is slowly reduced. As the proximity of the membrane to the substrate falls under 3μm the contrast of the interference fringes of the green light increases (to a time scale of one to five seconds). Also the time constant for the air to displace increases. This is a qualitative way to discriminate that the surface are nearly in contact, and at this point the stage steps are lowered to only 100-200nm displacements.

Figure 5-2 shows the interference fringes between a membrane that has been leveled and brought in very close proximity to the substrate. White-light fringes appear when the gap falls below two microns (Figure 5-5).

5.2.1 Mounting Membrane Frame within the ISPI tool

The ISPI system was built for X-ray lithography exposures. Special trays and mounts were designed to hold and manipulate X-ray masks. One of the key innovations was to make membrane stacking compatible with the legacy constraints. We decided to mount the quarter wafers containing the membranes to Pyrex X-ray mask blanks. These are 0.25"-thick plates with a 1.25" square cut in the middle. This window is large enough to fit four 12mm membranes. We originally tried gluing the membrane

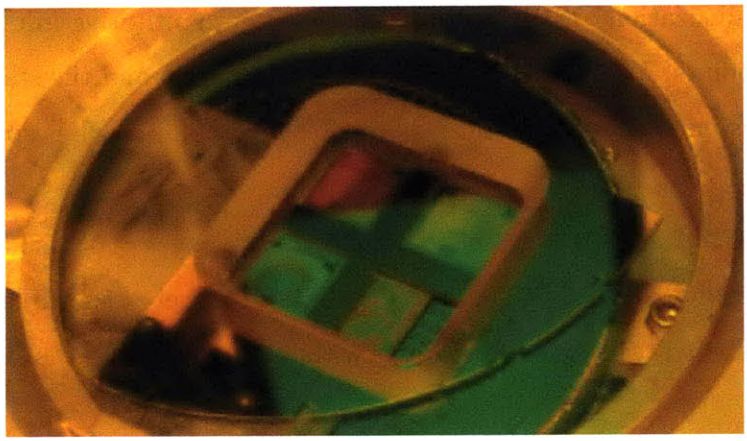

Figure 5-2: Green light interferometry is used for final parallelization after ISPI marks are taken to their limit. The coherence length of the source requires the gap be less than 50μm. Here, the single fringe indicates good flatness in the membrane and substrate. At gaps less than 5μm, the settling time for the fringes can be up to a few seconds. At this point, the stage steps are decreased to be $<$ 200nm.

wafer to the Pyrex with PMMA. This method has suffered from two shortcomings. First, it was not flexible. Once a wafer was mounted, it became difficult to remove. Second, the wafer distorted to fit the non-uniform layer of PMMA glue.

Our final solution was to use square gel pads to connect the wafer and Pyrex at three points. The pads (cut to 5mm $\times$ 5mm) provides sufficient adhesion to hold the wafer in place. It also cleanly detaches from both surfaces. The three-point-contact method did not distort the wafer. Figure 5-3 is an interferogram of the wafer after it has been mounted. The surface map is consistent with the map of the wafer before being mounted. While the whole wafer is bowed, the trend within each membrane window is flat.

5.3 Membrane Bonding Results

The ISPI tool gives us the tools for repeatable experiments. The key result we seek is bonding of a large-area-2DPC membrane to a patterned substrate. We are interested in comparing this result with three other variations: plain membrane bonding to a patterned substrate, plain membrane bonding to a plain substrate, and a patterned

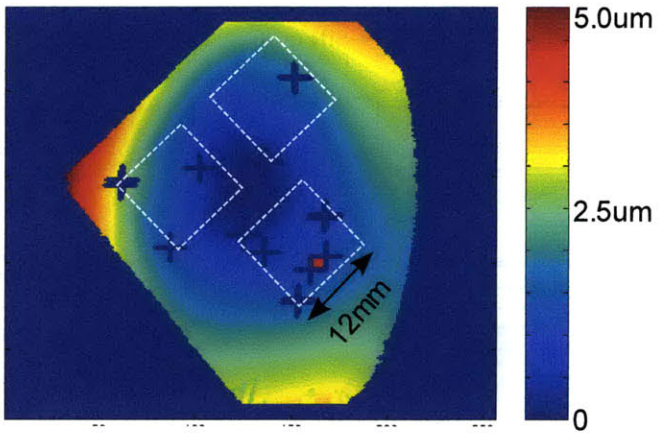

Figure 5-3: Image taken from Wyko interferometer showing wafer curvature after it has been mounted to the Pyrex X-ray mask frame with small gel squares. The highlighted membrane regions measure 12mm per side. These subregions are flat.

membrane bonding to a plain substrate. Figure 5-4 is a cartoon highlighting the variations. The results of these experiments will allow us to draw conclusions about conditions and mechanisms that allow us to bond large-area membranes. For all the following results, membranes are simply brought into close proximity of the substrate. The experiment takes place in atmosphere, and there is no differential pressure applied via backside pressure or vacuum.

5.3.1 Plain Membrane Bonding to Plain Substrate

Figure 5-5 shows how well a membrane can be brought to close proximity with a substrate using the mesa architecture and ISPI gap control. We notice that while the leftmost membrane is near contact, the other membranes on the frame remain unperturbed. This is a significant product of moving to the mesa architecture. After stacking of the first membrane we can imaging moving the substrate underneath the subsequent membrane layer. Any membranes that did not pass inspection can be avoided.

In this example, both surfaces are unpatterned save for the ISPI gapping marks,

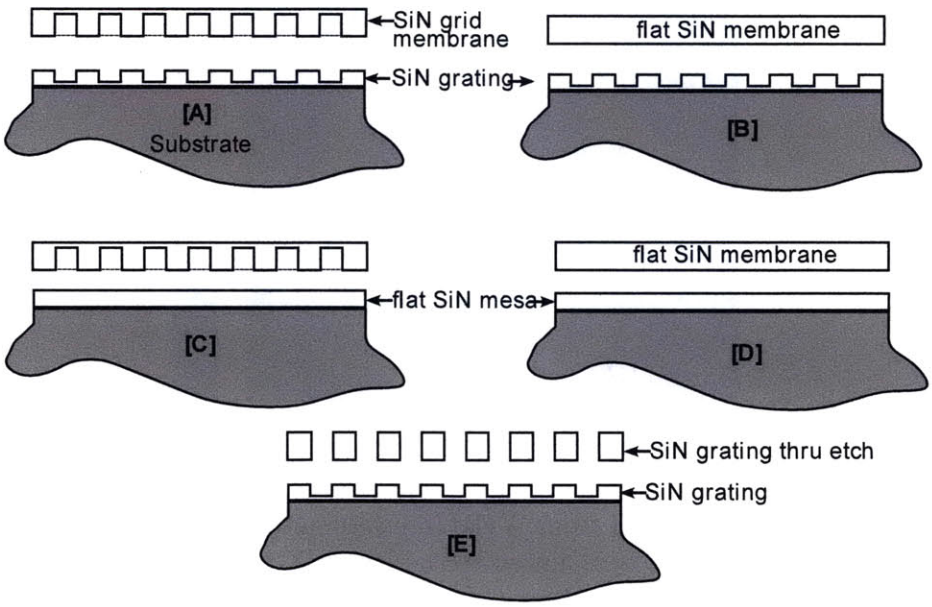

Figure 5-4: Cartoon of the different types of surfaces we attempted to bond in our study. [A] The key scenario for our 3DPC structure. [E] This case is presented as the key result in Chapter 4.

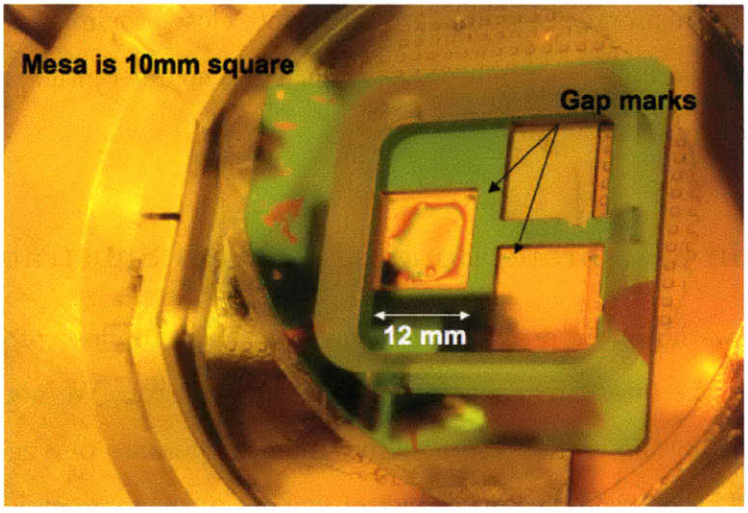

Figure 5-5: A plain membrane with ISPI gapping marks is brought into close proximity with a plain mesa. The observation of white light interference fringes confirms gaps of less than 1μm. Over a 24-hour period the fringes flattened but no bond every propagated.

cartoon [D] in Figure 5-4. Even though a very close gap is achieved between the surfaces, the film of air in the gap has difficulty dissipating, preventing contact initiation. After 24-hours of observation no contact was achieved.

We also tried the derivative experiment of using a patterned membrane (holes not completely etched through) with a plain mesa. The result of the experiment was the same as observed with the plain membrane and plain substrate, Figure 5-5. Again, the squeeze film cannot easily dissipate.

5.3.2 2DPC Membrane bonding to Grating Substrate

Here we present one of the key results of this work. We were able to show a large-area patterned silicon nitride membrane (holes not completely etched through) initiating contact and rapidly bonding to a substrate patterned with a grating. Figure 5-7 shows how a bond front propagates to cover the entire mesa substrate. The bond takes 25 seconds to complete. We can also compare Figure 5-2 and Figure 5-6. After bonding there are no interference fringes visible; the surface becomes reflective. As the good result implicitly implies, surfaces are clean from particles and contamination. Again, the surfaces are kept clean through proactive handling and cleaving techniques, RCA cleans and plasma ashing prior to bonding.

The exceptional quality of the van der Waals bond between the two surfaces is observed when we attempt to peel back the membrane in gradual steps. Figure 5-8 is composed of slides that show the change in contact area as the stage is slowly raised (at a rate less than 5μm per minute). This experiment was done with mesas that are smaller than the membrane windows as shown in Figure 5-7. However, the same experiment was done with mesas larger than the membrane windows (see Figure 5-9). In the former case, there is enough stage motion freedom to get complete mesa coverage, the latter can prevent us from obtaining complete coverage. Therefore, we choose to mesas that are smaller than the membrane window. This fact has implications for the method in which we cleave the membrane from its frame. This is discussed in detail in Chapter 6.

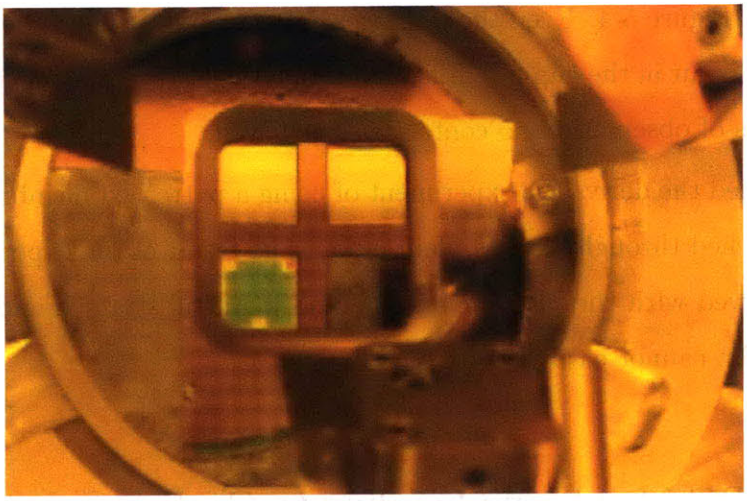

Figure 5-6: After the membrane bonds to the mesa the surface becomes highly reflective. The absence of interference fringes signifies a complete contact.

5.3.3 Plain Membrane bonding to Grating Substrate

The final combination we attempted stacking was a plain membrane with a grating substrate. Figure 5-10 shows that we were successful in bonding the two surfaces to together. The slowly propagating bond was complete in a time of nearly two hours. This is much slower than the case presented in Section 5.3.2. Additionally, the image shows that the bond is patchy and not complete. We also note that the membrane has difficulty conforming around particles as evidenced by the large air bubbles at the edges. Contrast this with with the very strong conformation of the patterned membranes to particles. In this case, air voids are only observable with a microscope.

5.4 Analysis of Membrane Bonding

In the previous sections of this chapter we successfully bonded a patterned membrane to a patterned surface. We were less successful with the other three combinations, as Table 5.1 summarizes. We look at three distinctive characteristics to explain the bonding dynamics observed in experiment: squeeze film presence, membrane stiffness, and surface roughness.

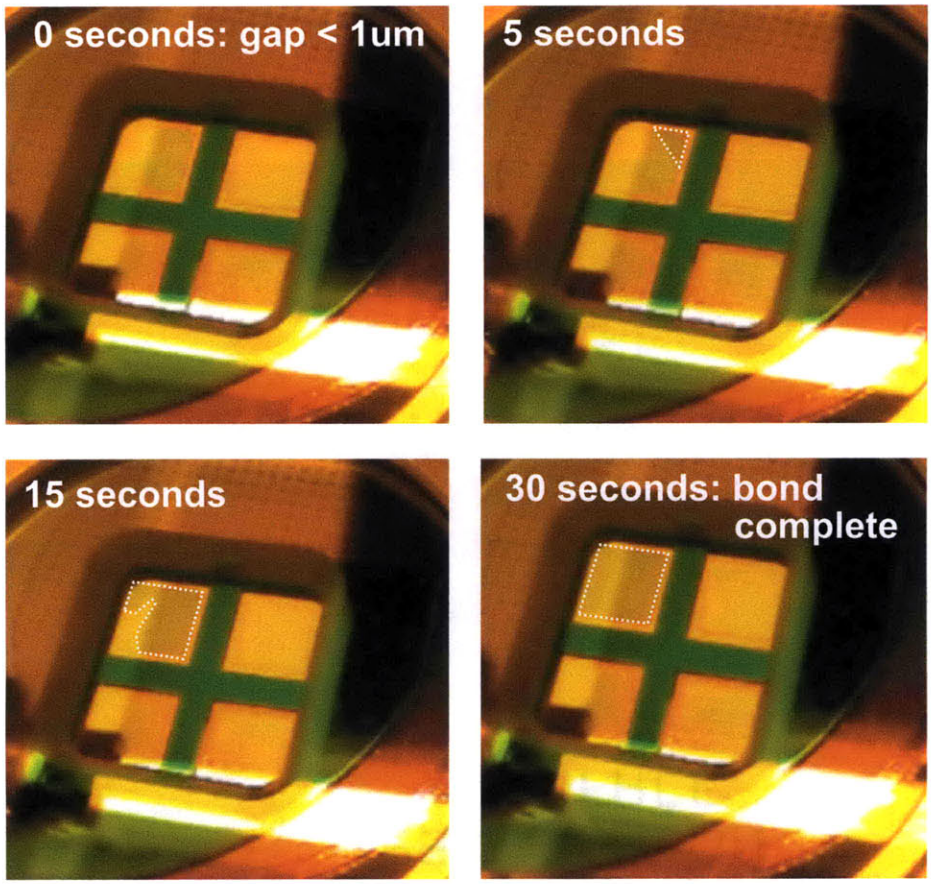

Figure 5-7: A patterned membrane (12mm × 12mm) bonds with a mesa substrate (10mm × 10mm). The upper left membrane is the one to track in these slides. The bond propagates from the top right corner and moves across the sample. After 30 seconds the bond is complete. We also take note that the membranes in the other quadrants are unperturbed by the stacking in the first quadrant.

Table 5.1: Bonding results for four different surface combinations. Cross reference this table with Figure 5-4

Membrane	Mesa	Squeeze Film (absent)	Reduced Stiffness	Bond Speed	Bond Quality
pattern	pattern	√	√	Fast	Good
pattern	plain		√	-	-
plain	pattern	√	-	Slow	Poor
plain	plain			-	-

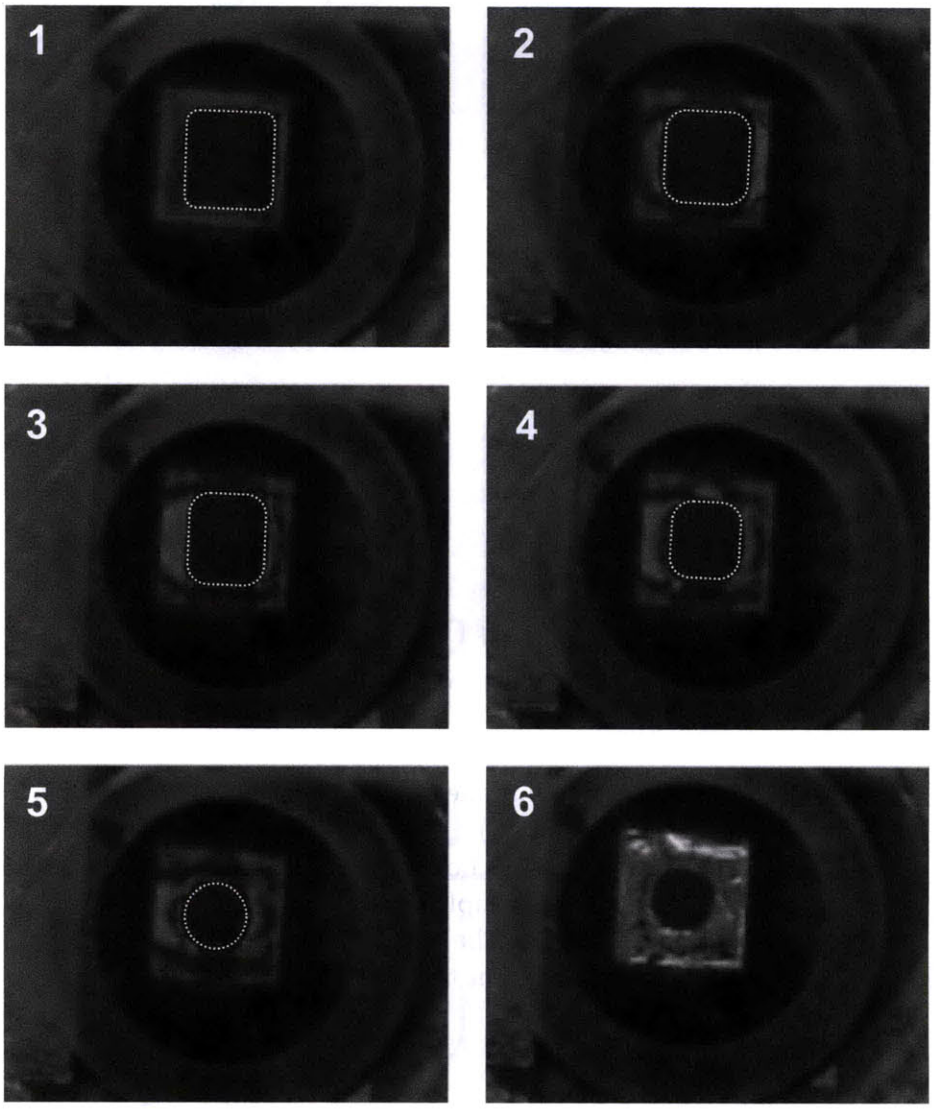

Figure 5-8: A patterned membrane in contact with the substrate is raised slowly, allowing the surfaces to go out of contact. The evolution of the contact area corroborates the quality and strength of the van der Waals forces that serve as the adhesion mechanism.

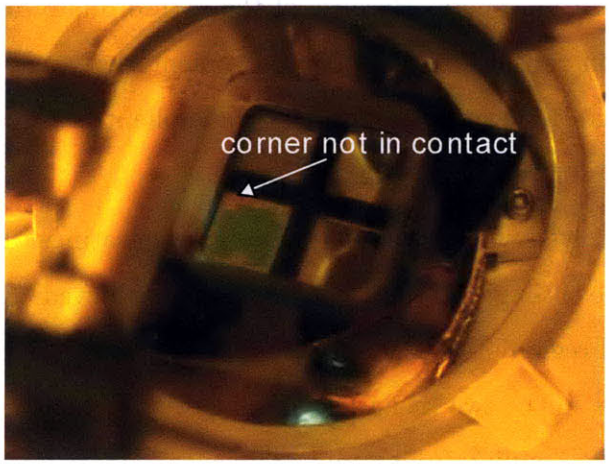

Figure 5-9: Patterned membrane bonded to patterned surface. In this scenario, the mesa measures larger than the membrane window. This limits stage movement; the membrane cannot go below the mesa. We notice that the corner of this sample is not in contact.

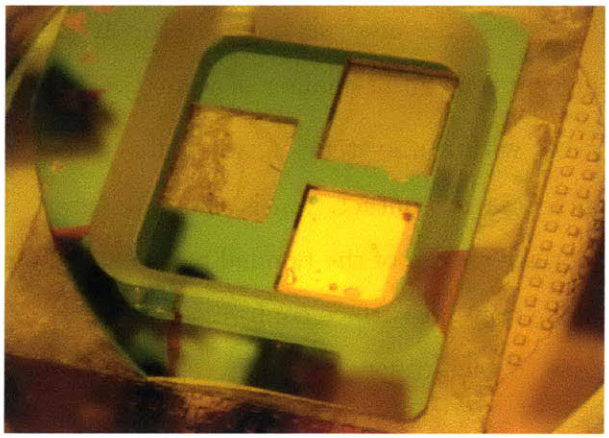

Figure 5-10: A plain membrane is bonded to a mesa with an etched grating. The bonding time was nearly two hours and the quality is poor. There is a patchy complexion to the bond, a symptom of air voids. We also notice that large tents form around particles because the membrane cannot comply around them.

As was discussed earlier, the squeeze film naturally exists when we bring two surfaces together in atmosphere. Because of the extraordinary aspect ratios characterized by submicron gaps and centimeter range membrane widths, the air has great difficulty evacuating. Because the membrane is compliant, it cannot sufficiently push out the trapped air, and contact is not initiated.

The problem is solved when we use substrates with gratings. The air has capillary channels to evacuate through, so that zero gap can be achieved. Even if an air bubble forms in the central region of contact surface it will quickly dissipate through the air channels. Therefore, in the two scenarios where we utilized patterned mesas, contact was initiated and the bonding front could propagate.

One could imagine doing the experiment in a vacuum system; however, this creates many more complications. The fact that we were able to achieve good bonding in atmosphere is a significant advantage our results versus prior work.

Given that bonding is only initiated when there is a mechanism for the squeeze film to escape, we must still account for the difference in bond quality in the plain membrane(Figure 5-10) and the patterned membrane(Figure 5-6 and Figure 5-7). For an intuitive answer we access the analysis done by Kevin Turner in his PhD thesis which explored the mechanisms and behavior of wafer/wafer bonding.

The total energy U_T within a system of two plates bonding is given by Equation 5.1. A represents area in contact, A_T is the total area, γ represents surface energies, γ_{12} is the interface energy of the bonded region and U_E represents the strain energy induced when one non-flat surface conforms to another. Figure 5-11 diagrams how the variables relate to each other.

$$U_T = U_E + (\gamma_1 + \gamma_2)(A_T - A) + \gamma_{12}(A) \tag{5.1}$$

The work that is achievable by adhesion is defined by Equation 5.2. It is a function of surface energies. Surface roughness reduces the surfaces energies and reduces the work available by adhesion. If we rearrange Equation 5.1 and differentiate with respect to area, A, we find that Equation 5.3 is true. The term $\frac{dU_E}{dA}$ is the strain

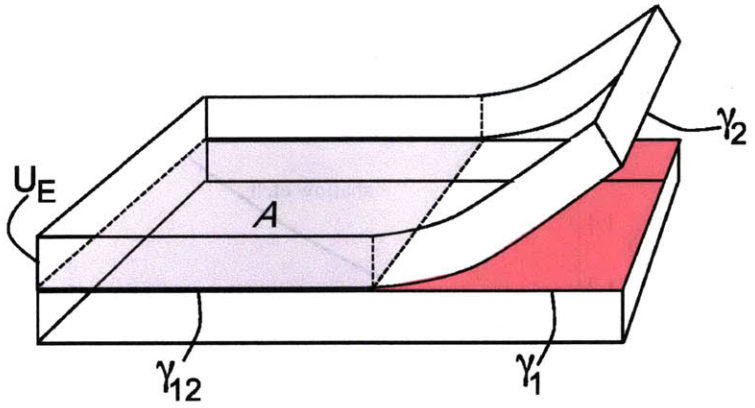

Figure 5-11: Diagram defining the parameters for wafer bonding analysis. γ represents the surface energies of the free and bonded regions. U_E is the strain energy potential within the top membrane that is generated from bonding and conforming to the bottom plate.

energy accumulation rate.

$$W = \gamma_1 + \gamma_2 - \gamma_{12} \tag{5.2}$$

$$\frac{dU_E}{dA} = W = \gamma_1 + \gamma_2 - \gamma_{12} \tag{5.3}$$

If a bond has been initiated locally, then it will propagate as long as the strain energy accumulation rate is less than the work of adhesion (see Equation 5.4).

Now how does this explain the difference in bonding we observed for the patterned and unpatterned membrane surfaces. A stiffer surface requires more strain accumulation and therefore more energy for a bond to advance. A more compliant surface, such as our patterned membranes, requires less strain for it to conform to a surface.

$$\frac{dU_E}{dA} < W \tag{5.4}$$

Now we must also offset the gain we make in reduced stiffness with loss in bondable area. In general, more area available for bonding results in greater adhesion potential. Turner ran simulations to understand which factor dominates during wafer bonding. He derived the graph in Figure 5-12[53]. In the case where shallow features are etched into the surface (no reduction in wafer stiffness), he found that the loss in

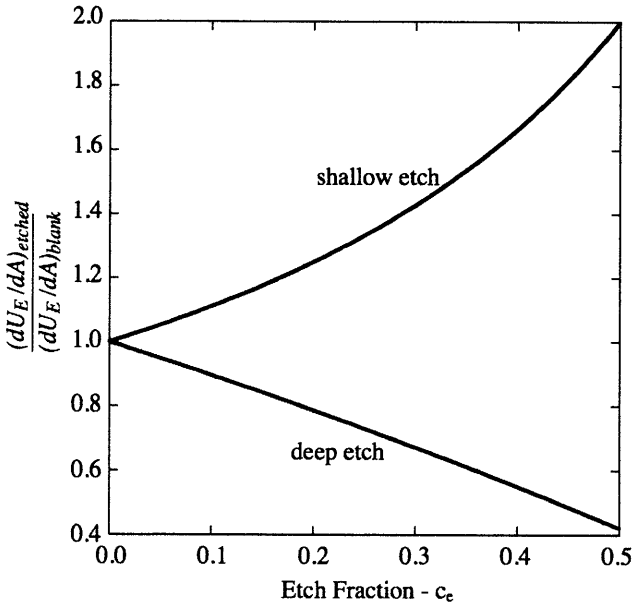

Figure 5-12: Turner plots the normalized strain energy acculumlation rate as a function of etch fractions. As the etch fraction increases, the bondable area falls. As the bottom curve shows, the reduction in stiffness cased by deep features facilitates bonding. Figure from reference [53].

area dominates and bonding becomes more difficult; the strain energy accumulation rate increases as the etch fraction increases. In the case where the same features were etched deeply into the wafer (resulting in a reduction in stiffness), he finds that the reduction in stiffness dominates the loss in area and bonding becomes easier. This conclusion is consistent with the improved bonding results there were obtained with our membranes which exhibit deeply etch features.

Another possible explanation for the discrepancy between the two runs is surface roughness differences. Equation 5.2 equates the work of adhesion to the surface energies of the system. Smoother surfaces have higher surface energies available for adhesion. For this factor to play a role, the patterned membrane surface must be smoother than the plain membrane surface. However, atomic force microscope (AFM) measurements validate the intuition that a patterned surface (which has undergone more processing) has a rougher profile. Figure 5-13 shows a roughness of 0.8nm on an AFM scan; this compares to values less than 0.3nm for a plain membrane. From the

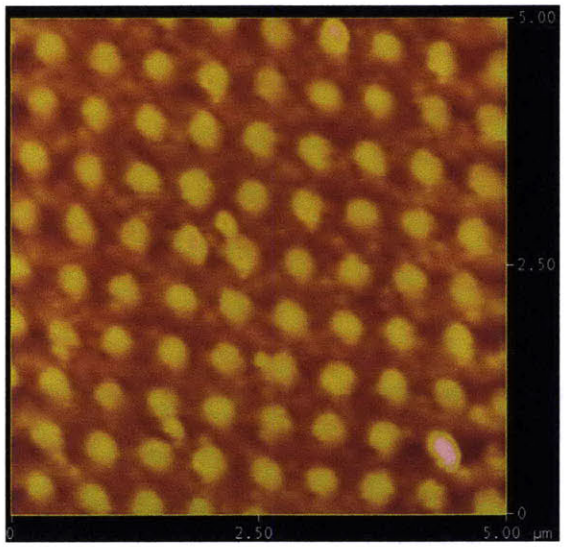

Figure 5-13: Membranes that have been patterned with the 2DPC have a rougher surface (0.8nm) than plain membranes (0.2-0.3nm). In this AFM scan we observe shallow posts that emanate from the trilayer etch.

surface profile, we know that the profile is created from sputtering during the trilayer etch process.

5.4.1 Distortion

One of the concerns for membrane stacking is distortion in the membrane after it has gone into contact with the surface. We can imagine that the sheet may contort in an irregular fashion to destroy the spatial coherence of the photonic structure. However, our stacking results have allowed us conclude that the stacking process preserves long-range spatial coherence of the lattice. It is even robust to particle interference. Figure 5-14 is an optical micrograph of the moirè pattern that is observed when two grids with 600nm pitch are laid on top of one another. The fringe period of 40μm can be used to calculate the rotational displacement by using Equation 5.5. Equation 5.5 simplifies to Equation 5.6 for the special case where the pitch for both grids is the same and the rotation angle is small. Using Equation 5.6, we find that $\alpha = 0.015\text{rad} = 0.85^o$ when the grid pitch is 600nm and the measured moirè pitch is 40μm.

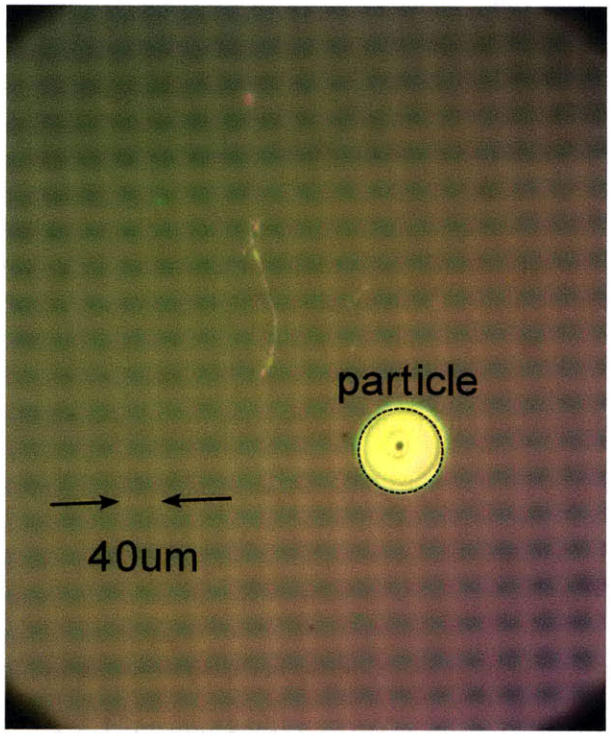

Figure 5-14: Optical micrograph of moirè fringes coming from 2DPC membranes in contact. The coherence of the fringes indicates the long-range coherence of the lattice. Note the lack of distortion in the vicinity of the particle.

$$P_M = \frac{p_1 p_2}{\sqrt{p_2^2 sin^2\alpha + (p_2 cos\alpha - p_1)^2}} \tag{5.5}$$

$$P_M = \frac{p}{2sin\alpha} \tag{5.6}$$

$$P_{beat} = \frac{p_1 p_2}{|p_1 - p_2|} \tag{5.7}$$

Moirè techniques are extremely sensitive to small displacements. In fact, strain measurements are conducted on physical samples using this technique. Local non-uniformities are readily revealed in the fringe pattern.

One possible mode of distortion would be a kink between two regions that results in a small rotational shift. If there was simply a 2% rotation shift in angle between two regions, $\alpha_{shifted} = .0153$rad, then $P_M = 39.2\mu$m in the shifted region. This would result in a beat period of 1960μm, which would be visible within the field of view in Figure 5-14. The absence of shifts in the fringes indicate there are no distortions caused by rotational errors.

The second possible mode of distortion would be a pitch variation between two regions. Since the membrane is compliant we can imagine one region could potentially stretch, changing the pitch of the grid. Assume the bottom layer remains unperturbed. The top membrane bonds with two distinct regions. One in which the fundamental period is matched to the bottom layer. The second region experiences a 1% increase in pitch from membrane stretching. Equation 5.5 tells us that in a new moirè pitch of 33μm emerges in the stretched region. The fringes from the stretched region and the normal region would beat at a 200μm.

5.5 Contributions and Conclusions

In summary, we have demonstrated repeatable and high-yield membrane stacking of patterned 2DPC membranes. These results are the largest-area bonding published to date in any material system. The figures in this chapter show 12mm $\times$ 12mm coverage; however we have succeeded in bonding a 14mm square membrane to a

substrate. The only limitation at the moment is the size of the membrane. Competing bonding techniques explored in Chapter 4 are limited by other factors.

We have shown a very intriguing and powerful application for ISPI, whose heritage dates back to X-ray lithography.

We have shown a variety of experiments with various membrane and substrate types. This has enabled us to match the bonding mechanisms with intuitive theory that has been in place for wafer bonding. The experiments have concluded that the mesa should be smaller than the membrane window. This has implications for our next chapter which deals with releasing the membrane from its frame.

Chapter 6

Controlled Fracture of a Membrane from its Frame via Stress Engineering

6.1 Introduction and Prototype

The first successful large-area stacking of photonic crystal membrane is demonstrated in Chapter 4. One prominent shortcoming was the inability to remove the membrane from the frame in a controlled manner. Because we physically cut out the membrane after bonding we observe poorly defined edges and silicon nitride shards. This chapter is focused on the most significant hurdle in the realization of membrane stacking as a manufacturable technology. After the membrane has been bonded to the substrate, we must detach the membrane from its frame while satisfying the following requirements:

1. Predictable control the cleave line so that stacked layer has well defined edges
2. Particle-free surface after detachment to enable multiple layer stacking
3. The integrity of the region of interest remains in tact
4. Efficient actuation so that the stacking yield is high and the stacking time is negligible

This problem statement is extremely challenging when we take into account the catastrophic manner in which silicon nitride shatters. Figure 6-1 shows how cracks in a silicon nitride propagate. Controlling the propagation of the cracks in this material system is extremely complex. There are four potential avenues that we have identified that can potentially solve this novel research challenge. We list them here along with their merits and potential flaws:

1. Razor-blade cut - Because of its simplicity this method was utilized in earlier results (see Chapter 4). However, this method does not control edge definition and leaves particles behind.

2. Laser cutting with a focused spot - This method requires large capital investment and modification of our ISPI bench. Cutting with a spot will lead to membrane puncture which rapidly devolves into the scenario shown in Figure 6-1. It is also not clear if the cut can be made without the generation of particles.

3. Reactive-Ion Etching - Has the potential to define clean and particle-free edges. However, it is unclear how the region of interest can be masked off. In addition, this method requires taking the membrane and frame out of the alignment tool for etching. This will slow down the process and lead to lower yields

4. Stress-engineered cleaving - The method selected for this thesis.

We selected the fourth method, stress-engineered cleaving, because of its potential to comprehensively meet the requirements while also being an elegant solution. The price we pay is additional mechanical design and an extra lithography step to define the cleave structures. Additionally, the alteration of the membrane with a non-periodic pattern can lead to distortion. The plan view of a complete membrane for the membrane stacking architecture is captured in Figure 6-2. The perimeter of the photonic crystal region is lined with tethers that are strong enough to support the membrane structure during routine handling and designed to cleave with a force actuation.

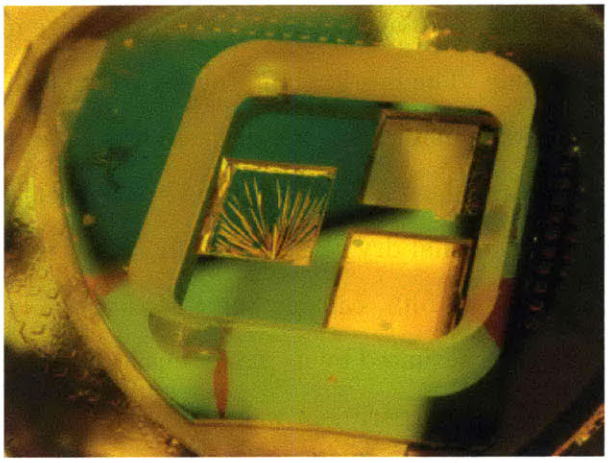

Figure 6-1: A 12mm-silicon-nitride-membrane window (350nm thick) catastrophically shatters after it is punctured. We see that the cracks propagate without any preferential direction as this is an amorphous material. SiN membranes are particularly sensitive to shear forces and punctures. Controlling the fracture is the topic of this chapter.

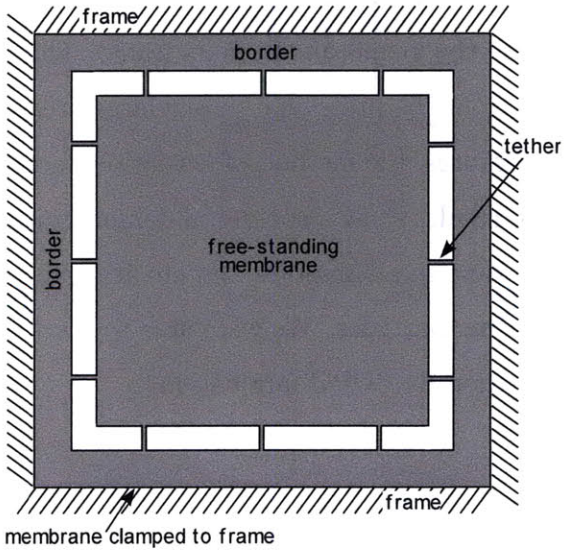

Figure 6-2: Cleave structures are incorporated in the edges of the membrane for release. The device region is at the center of the membrane and the cleave occurs only during an applied force actuation.

We tested the merits of the stress-concentration method by building a prototype in silicon nitride. The prototype consisted of a 400μm-per-edge membrane supported by three tethers on each side. The fabrication process, which utilizes SEBL, is similar to that of the Poisson spot membrane discs discussed in Chapter 7. We attempted two tether designs: a rectangular bar and a notched bar. Figure 6-3 shows the free-standing membrane after the final dry release via RIE. The tethers were too weak to suport the stress in the nitride film, causing some of them to become unhinged. In other words, the tethers were actuated by in-plane tensile stress (depicted in Figure 6-4). While the tethers failed, the experiment was a success because it allows us to make some important strategic conclusions.

1. The membrane will fracture at the point of highest stress first
2. The fracture lines can be controlled such that the region of interest (the central membrane) is not damaged
3. No fragments of silicon nitride are left behind by these very clean cleaves

We decided to move forward with the engineered stress-concentration structures as the method for releasing the membrane from its frame. This chapter discusses how we scale up the problem from the prototype to our large-area membranes. We cover the design of the break features, the method of actuation and the fabrication process developed. Experimental results show a successful demonstration of the concept. We are able to bond a membrane to a substrate and cut it away from its frame, leaving behind squared edges and no particles. We were able to stack another membrane on top; this is a scalable solution for 3DPC fabrication.

6.2 Mechanical Design

We must design weak points in the silicon-nitride membrane that are strong enough to support the membrane from the residual stress of the nitride and the forces applied through routine handling; they must be weak enough to readily fracture when a specifically designed force is applied.

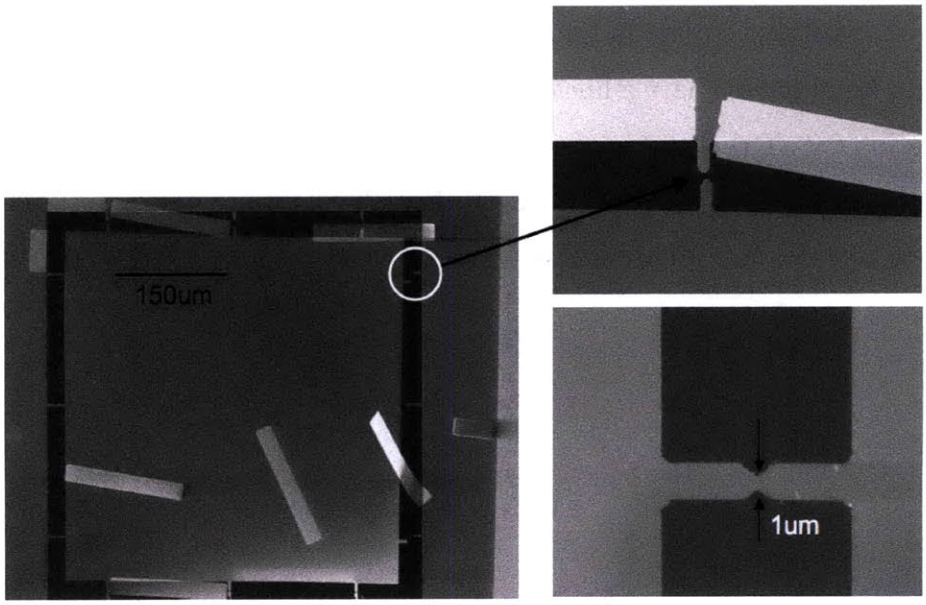

Figure 6-3: The prototype of stress-engineered cleaving using notched tethers in silicon nitride. The membrane area was released with an RIE etch. Failures in the tethers occurred because of overwhelming tensile stress. We note that 50% of the breaks occurred at the notch, the points of highest stress. There are no particles nor are there cracks which propagate onto the region of interest.

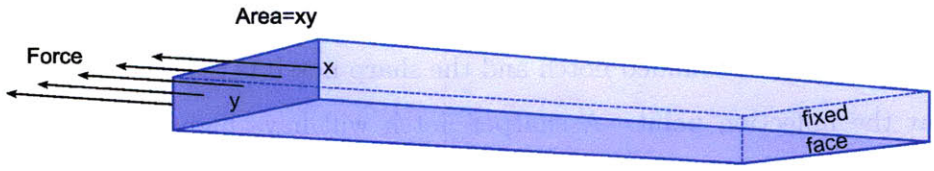

Figure 6-4: Cartoon demonstrating tensile stress being applied to the face of a bar. The other end is clamped, which will cause the bar to stretch and undergo uniform strain. SiN has a residual stress of 150MPa.

Low-stress silicon nitride has a residual stress. Etching features into the membrane allows us to concentrate stress loads in a desired fashion. Stress is a force acting on the cross section, as is stated in Equation 6.1 and shown in Figure 6-4. The stress and the strain Equation 6.3 have a linear relationship, whose slope is the elastic modulus, E, Equation 6.2. The strain in an elastic material is a ratio of the change in length caused by the stress to the relaxed length. For silicon nitride, literature values for E and σ are 200GPa and 150MPa, respectively [15, 28].

$$\sigma = \frac{F}{A} \tag{6.1}$$

$$\epsilon E = \sigma \tag{6.2}$$

$$\epsilon = \frac{\Delta L}{L} \tag{6.3}$$

Our starting set for tether structures is shown in Figure 6-5. The simple bar has an even distribution of stress. The prototype we fabricated with bar-shaped tethers experienced fractures only along the tethers since these were regions of highest stress concentration. However, the fracture point is not deterministic along the length of the bar. We contrast this with the prototype with notched tethers (Figure 6-3), where over 50% of the fractures occurred at the design locations. The notch configurations allow us to create a stress concentration at the waist of the notch. The notch geometry determines the weakness of the structure. The other consideration that separates the the rounded notch and the sharp notch is the stress multiplication factor at the inflection point. A sharper notch will have higher concentrations of stress at the corners, making it more vulnerable to fracture. In Section 6.2.1 we will show simulations that elucidate the effect of radius of curvature on stress focussing.

The final design is the simple tapered or trapezoidal bar. Discussions with Professor Martin Culpepper (Department of Mechanical Engineering) illuminated the simplicity of this design and its prevalence in metal stamping processes[49]. This shape has three primary advantages over the other three designs. First, the shape

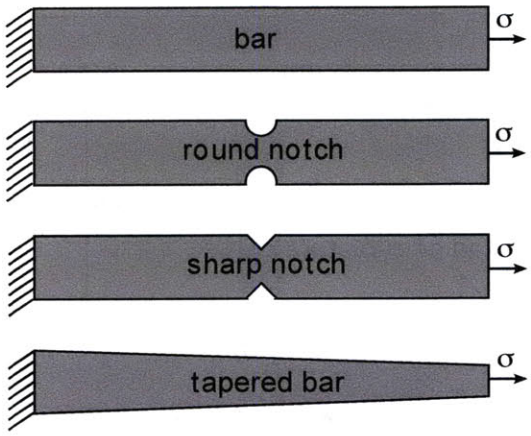

Figure 6-5: The four basic tether shapes investigated. The tapered bar was ultimately selected for fabrication and testing. There is a tensile stress applied by the membrane it connects to.

is very simple to pattern lithographically. Consider that the the sharp notch design is only possible using SEBL. Second, the cleavage point, the point of highest stress concentration, occurs at the extreme of the bar, allowing us to cleave at the edge of the membrane, not leaving behind vestigial bars. Finally, the design is conservative, making it an excellent starting point. As the antithesis, the sharp notch is the least conservative because of its ability to multiply stress and make the structure weaker.

6.2.1 Design Parameters and Simulations

Figure 6-6 shows how the tapered tethers will sit at the edge of the membrane. The figure highlights the parameters we have in designing the cleavage structure: namely, tether width, tether pitch, tether length, and corner radius of curvature.

Notes on FEA Simulations

Finite-element analysis was conducted to better understand the stress profiles within various tether geometries and boundary conditions. The following assumptions were made in our models: silicon nitride is an isotropic elastic material (E=200GPa) and its Poisson ratio is 0.23. Using two-dimensional plane-stress elements, our simulations covered in-plane stresses and actuation forces. The residual stress in the membrane

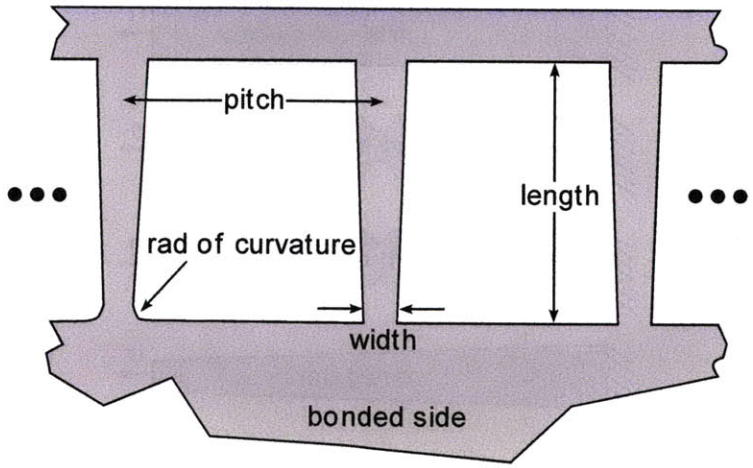

Figure 6-6: Shows the basic layout of the tapered bar tethers. The cleave point is adjacent to the region of interest. The four design parameters are: pitch, width, length, and radius of curvature at the boundary. The goal is to make the system robust to handling while susceptible to an actuation.

was assumed to be between 120-150MPa. The modeling package utilized is Adina, version 8.5.4 [6]. We only present simulations of tethers. The problem of modeling the entire membrane system with 2DPC and tethers is ignored because it is computationally difficult. The extreme aspect ratios make modeling with a reasonable number of elements difficult.

Radius of Curvature

The radius of curvature at the tether boundary is one of the variables that determines the relative weakness the membrane system. There can be very large concentrations of stress at the corners if they come to a sharp point. When initial designs were breaking prematurely, we shored up the design by increasing the radius of curvature. The physical concentrations of stress as they relate to the radius of curvature were shown by John Rogers group in the context of their PDMS silicon membrane stamping process [33]. They showed that sharper corners concentrate stress more and are more susceptible to fracture when actuated. Simulations in Figure 6-8 and Figure 6-7 show that we can reduce the maximum stress at the boundary by 33% when we increase the radius of curvature from 1μm to 3μm.

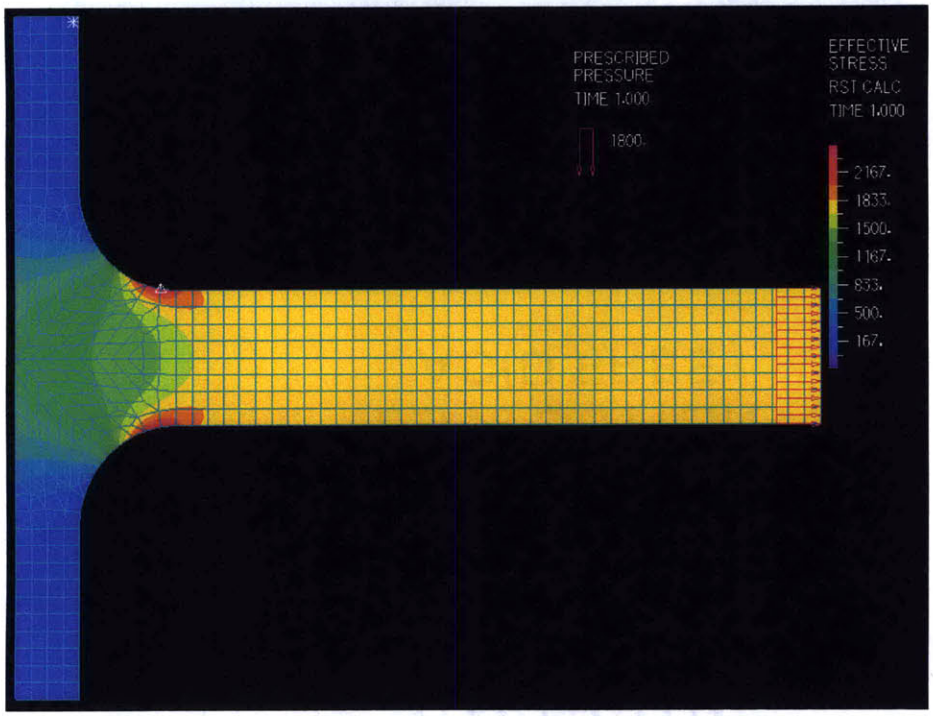

Figure 6-7: Simulation of a tether with corner radius of curvature of 3μm experiences a tensile stress. The maximum stress in the corner is 2000MPa.

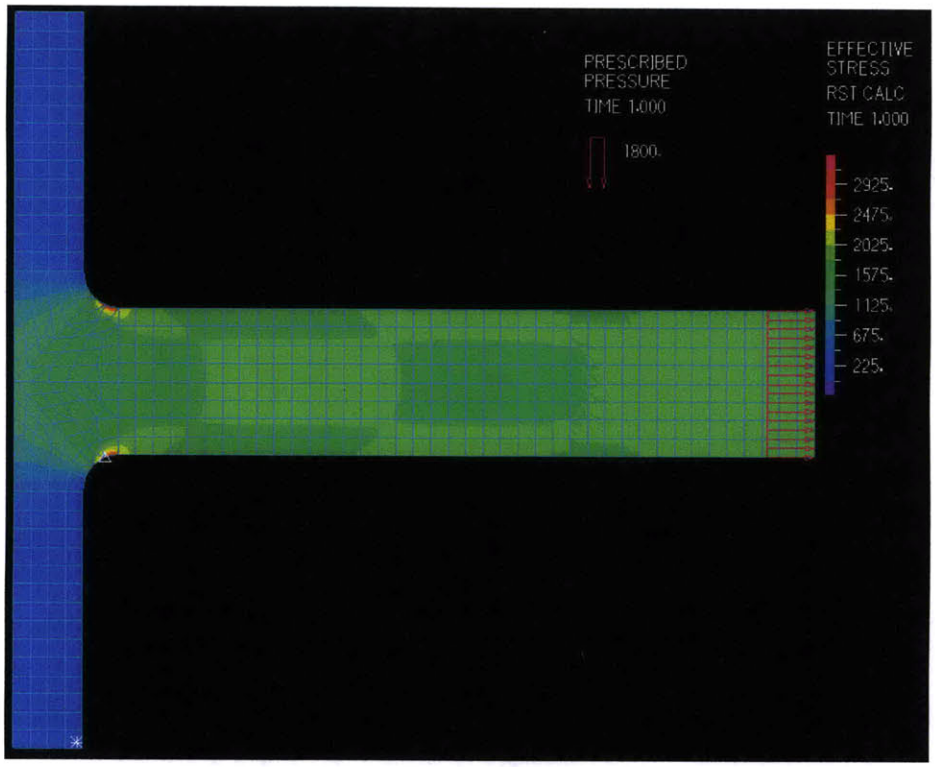

Figure 6-8: Simulation of a tether with corner radius of curvature of 1μm experiences a tensile stress. The maximum stress in the corner is 3000MPa.

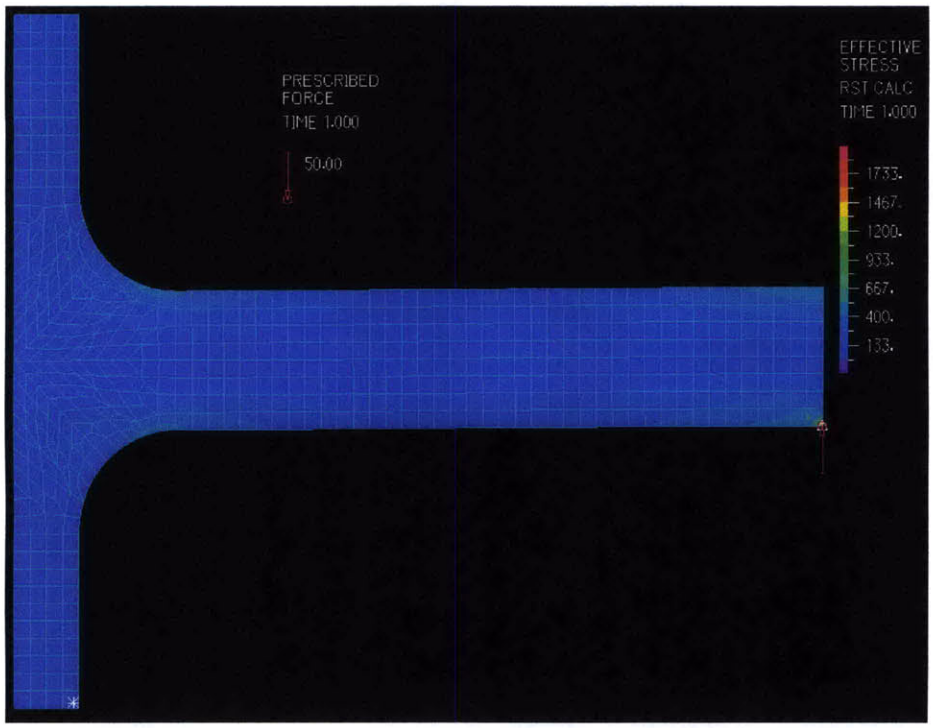

Figure 6-9: Simulation of a tether with corner radius of curvature of 3μm experiences a shear force. The maximum stress is 500MPa.

The improvement in strength is more pronounced when we talk about sensitivity to an applied torque. There is a $4\times$ reduction in the maximum stress at the boundary when we increase the radius of curvature from 1μm to 3μm. Figure 6-9 and Figure 6-10 are simulations.

Tether Width and Pitch

The radius of curvature gives us a small "dial" in refining the tether strength. The largest lever we have is the width and pitch of the tethers. Because of the large-area nature of the project, we need many tethers to keep the central membrane structure in tact and free of distortions. Therefore, we require many tethers along each edge. We fixed the pitch at 50μm, which yields 200 tethers per side for a 10mm square membrane. This pitch gives us very good flexibility for lithography. A very tight pitch may require only high-resolution lithography methods.

Once the pitch is fixed we vary the width of the individual tethers. We fabricated

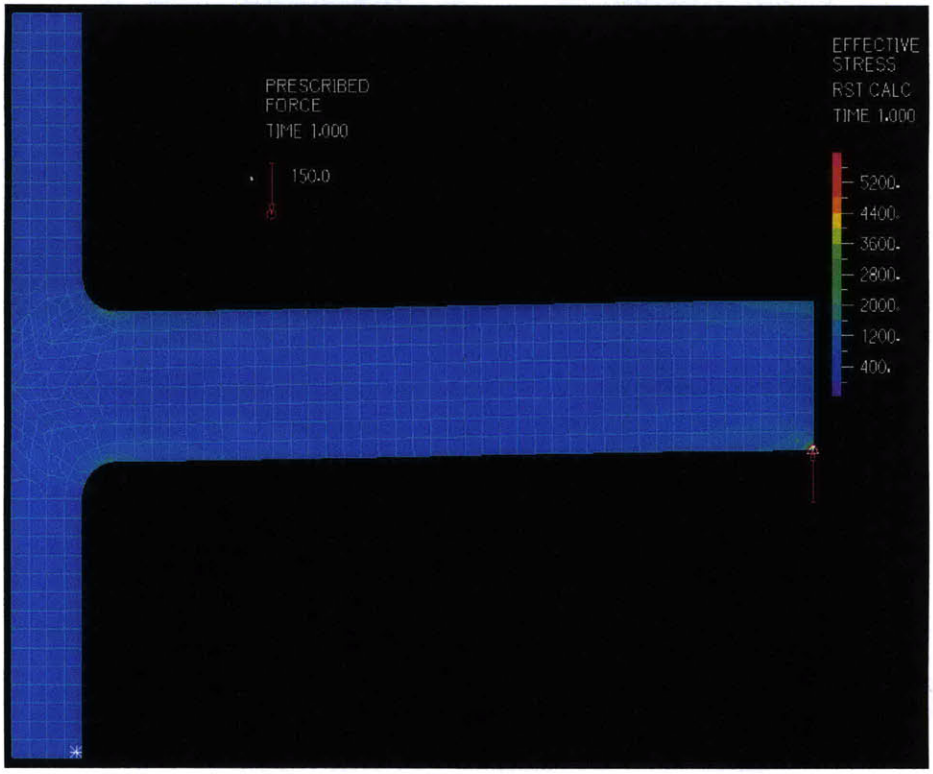

Figure 6-10: Simulation of a tether with corner radius of curvature of 1μm experiences a shear force. The maximum stress is 2000MPa.

tethers with widths at 2μm, 4μm, 6μm and 10μm. The highest yields we obtained were with 6μm and 10μm widths at the tapered end. We cannot make the tether too wide or we risk cracks propagating into the region of interest. A long and narrow aspect ratio, as we created in the prototype, ensures that cracks are localized within the tether.

The load experienced by a tether at its weakest point is given by the following equation, where σ_t is the stress on the tether, σ_m is the stress along the length of the membrane, A_m is the cross-sectional area of the membrane and A_t is the cross-sectional area of the tether at narrowest point, and n is the number of tethers.

$$\sigma_t = \sigma_m \frac{A_m}{A_t \cdot n}$$

Because both the tether and the membrane have the same thickness, the equation simplifies to a ratio of effective widths, Equation 6.4. The simulation in Figure 6-11 and Figure 6-12 show how the load increases after we remove tethers. We must have enough tethers such that the maximum stress never exceeds the fracture strength of silicon nitride.

$$\sigma_t = \sigma_m \frac{w_m}{w_t \cdot n} \tag{6.4}$$

In the case where five tethers (width of 2 units) support the load along a membrane (60 units total width), the stress in the tethers is $6\times$ the stress in the membrane. When we replace the five tethers with only two, the max stress in the tether is $15\times$ that of the membrane. Simulations Figure 6-11 and Figure 6-12 confirm the analytical model.

Tether Length

In Figure 6-12 we see how two tethers distribute a uniform load applied along the membrane. The maximum load in the tether is constant with respect to length. For example, if were to double the length of the tethers and apply the same load, the maximum stress at the focal spot would be the same. The tether length becomes

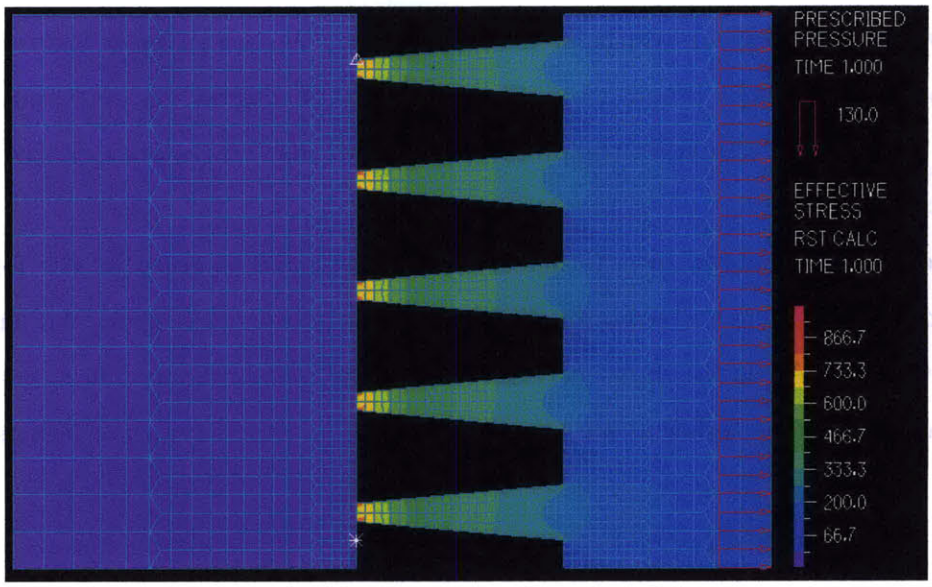

Figure 6-11: The stress along the membrane is distributed among five tethers. As is predicted by Equation 6.4, the maximum stress on the tether is six times the stress along the membrane.

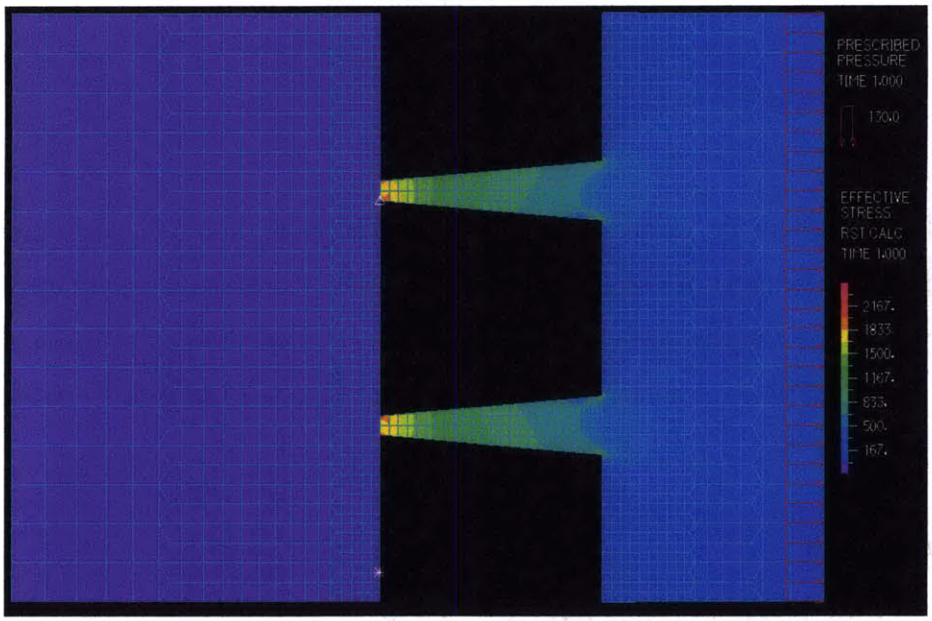

Figure 6-12: The stress along the membrane is distributed among five tethers. As is predicted by Equation 6.4, the maximum stress on the tether is 15 times the stress along the membrane.

important if we consider the fact that the membrane applying the load can relax. If we have two tethers, A and B, with respective lengths L_A and $L_B = 0.5L_A$ as shown in Figure 6-13. For tether A to experience the same stress as tether B, it must stretch twice as much. In other words, the longer tether can give more before it experiences the same stress as a shorter tether. The distance stretched by the tether is also the same distance by which the membrane relaxes. Stress in the system is reduced when the membrane relaxes. This is especially true for silicon nitride, which has a residual stress. The same may not be true for stress free silicon membranes. If we take into account the relaxation of the membrane, a longer tether will hold lower stress (and thus be stronger) than a shorter tether.

The drawback of using a long tether is the reduction in stiffness. The membrane will relax more and undergo more distortions. Holding the shape of the photonic crystal together requires a stiffer tether structure. We fabricated tethers with lengths of 30, 50, and 100μm. The final design used tethers with a length and pitch of 50μm.

6.3 Actuation

The break features are designed to be strong enough to withstand processing and handling. They must also be strong enough to survive the bonding action. Then we apply a force that exaggerates the stress concentrations and cleaves the structure. There are a few ideas for actuation that we contemplated.

1. Rotational shear
2. One-dimensional shear (along x or y)
3. Exaggerating the tensile stress by stretching

The first two force actuation are attractive because shear forces are not experienced by the membrane during normal handling. An explicit motion of the substrate stage would be required to exploit the weakness in the tethers. However, the rotational shear force is only attractive if we were to use circlular membranes and mesas

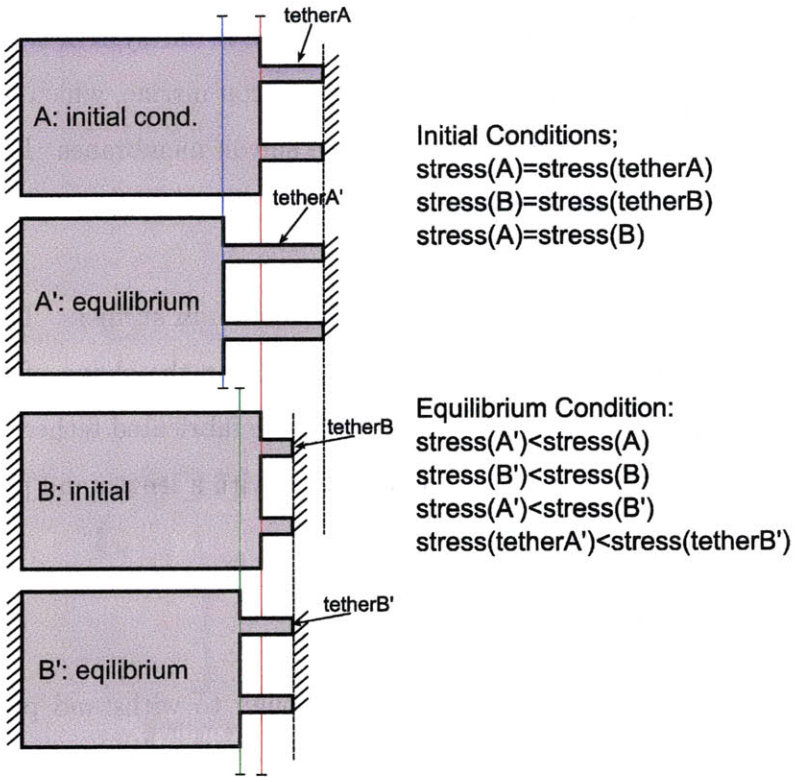

Figure 6-13: Tether length as a design parameter. We have illustrated two membrane/tether systems in a 1D scenario. The tether and the membrane are clamped on both sides but possess a residual stress. In order to go to equilibrium, the tethers stretch (experience more stress) while the membrane relaxes (experiences less stress). The equilibrium position occurs when the effective stress along the length of the membrane is equal to the effective stress along the widths of the tethers. There are different equilibrium points for both systems. Tether A has a lower stress because the membrane relaxes more.

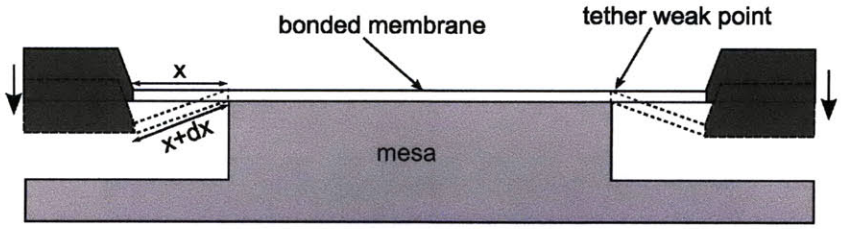

Figure 6-14: Pressing the frame down increases the length of the tethers which lie off the mesa edge. The stretching of the tether results in an increased stress; this stress will cause the tether to fail once the fracture stress is reached.

rather than the square shapes we pursued in this work. The membrane must be exactly at the center of rotation of the stage, and the complication of aligning the centers is not trivial. We considered applying a shear in only one direction. However, that would require the tethers parallel to the shear force to be redesigned or removed all together.

The most attractive method for actuation based on our membrane stacking architecture is a stress applied by stretching. Here, our decision to make the mesa smaller than the membrane window becomes a boon. After the membrane has been bonded to the mesa, we push the membrane frame down, forcing the tethers to stretch. The stretching of the tether results in an increased stress; this stress will cause the tether to fail once the fracture stress is reached. Figure 6-14 shows how this works. This method is attractive because it is symmetric, a uniform stress is applied to all the tethers in parallel. We must ensure that the mesa depth is larger than this figure.

6.4 Fabrication Process

The basic fabrication of the system with 2DPCs and the tether features is similar to the large-area membrane process flow described in Chapter 2. The additional fabrication steps required to place the break features is shown in Figure 6-15. There are unique and interesting problems in lithography that surface.

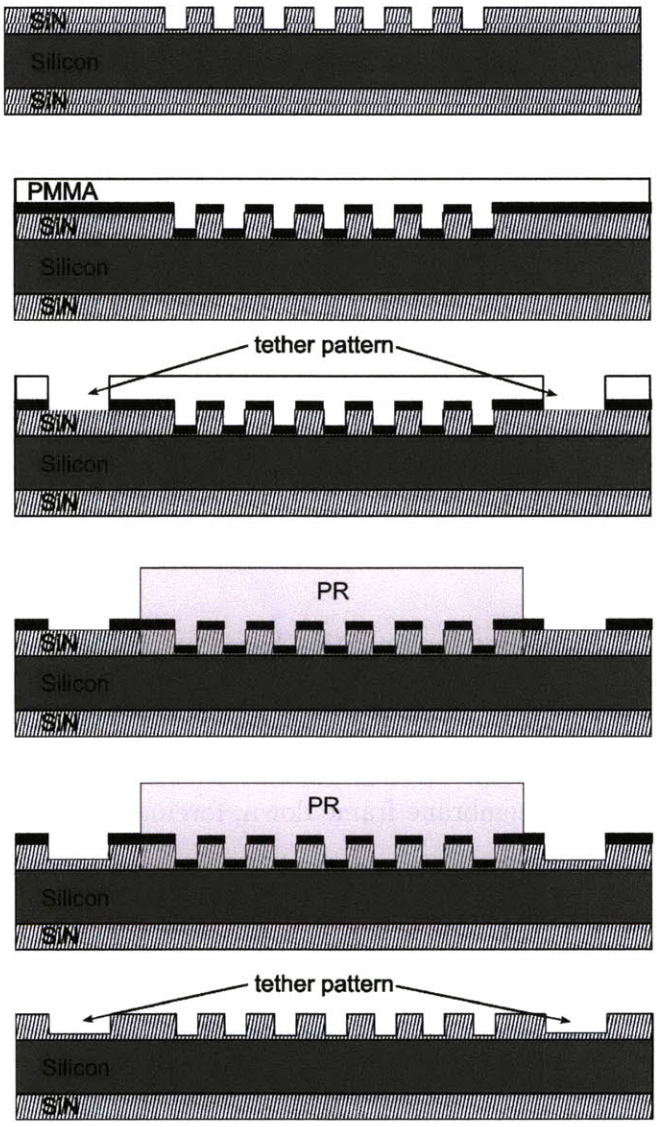

Figure 6-15: The process for etching the break structures into the 2DPC substrate. After the substrate has been patterned with the photonic crystal, the break structures are patterned into PMMA or resist and transferred into chrome via a wet etch. Before, we can RIE the structures into the silicon nitride, the 2DPC region must be masked off to ensure that it does not etch more.

6.4.1 Lithography

There are interesting lithography issues that follow from the challenge of patterning the break features. As has been a common theme in this thesis, there is no perfect lithography mode. We must choose a compatible with the application in mind. And at times we shape the application to better suit the capabilities of the lithography chosen. The case is true here. In general we are interested in patterning uniformly over a perimeter of 160mm (4 membranes $\times$ 4 sides $\times$ 10mm per side). We can get away with features as large as 3μm or as small as 50nm, depending on the tether shape employed.

We investigated scanning-electron-beam lithography (SEBL) and a masked-based exposure tool as the candidates to address our requirements.

Scanning-Electron-Beam Lithography

Maskless lithography tools such as SEBL give us the greatest flexibility for tether design. If we want 50nm feataure, as is required by a sharp notch tether design, then SEBL is our only option. Pattern uniformity is very good across the entire wafer because SEBL has a large depth of focus and laser-feedback stages. We patterned the tethers with simple rectagular geometries (400nm maximum width). Circles are not easily done with the tool, which limits are ability to control the radius of curvature. The writing time is about 25min for 8mm $\times$ 8mm membrane sizes. If one wanted to test new designs with rapid turn around, this is the tool of choice. However, in practice, the tool is expensive and booked at least two weeks in advance. It's key advantage of flexibility is tarnished a bit. And if a final design is established, the turn-around time with SEBL does not improve.

OAI Mask Aligner

Mask-based tools give us a cheap and high throughput method once the mask has been fabricated. We used Advanced Reproductions of Massachusetts to produce our masks. They were able to deliver 5inch by 5inch quartz masks (minimum feature

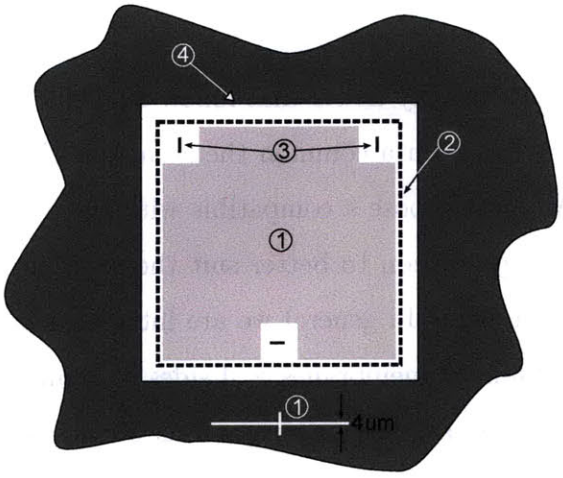

Figure 6-16: The alignment scheme for the respective lithographic steps. Pattern [1] shapes (2DPC and cross alignment mark) are aligned to the wafer flat as described in Chapter 2, Figure 2-12. Pattern[2] (tethers) are aligned relative to the cross mark placed in [1] ($\pm 20\mu$m achieved). Pattern[3] (ISPI marks) are written with SEBL and aligned to reference flat ($\pm 200\mu$m placement achieved). Pattern[4] (backside window) is aligned to the wafer flat ($\pm 200\mu$m placement achieved)

of 3μm) in 5 business days for 800 dollars. Quartz is necessary to utilize shorter wavelength illumination. We were easily able to place circles with 3μm radius to round corners. Using the OAI mask alignment exposure tool, we could readily place our features. Figure 6-16 summarizes the layout of a membrane and how features are aligned with respect to one another.

We employed two resists during the research phase, Shipley 1813 and PMMA. We ultimately selected PMMA; however the discussion of their merits is warranted. In both cases, they were used to pattern the chrome hard mask via a wet etch. The chrome is ultimately used to etch the tether features into the silicon nitride (see Figure 6-15). Shipley 1813 is a positive photoresist that is sensitive to $\lambda = 400$nm (developed in 321 developer). It was spun at 3000RPM for a 1.5μm-thick layer on the wafer. 1813 is difficult to spin on quarter wafers because of its thick viscoscity. Because we are etching a wafer that already has etched features, uniform coverage is paramount. In addition, poor spins result in edge beads which hinder good contact when vacuum is applied between the mask and the substrate. Poor contact prevents

uniform patterning. Dimensions of the critical feature of the tether would change along the wafer. This can lead to stress gradients which will ultimately lead to a failure of the membrane during release.

In addition to a lack of uniformity, 1813 outgasses during exposure. While we did short exposures, leaving long intervals (3-5min) for gas to trickle out, instead of one straight shot, we witnessed blisters in the resist. Again, these are not tolerable since there are features already on the wafer that can be corrupted.

The solution to these problems was to shift to PMMA which exposes at $\lambda = 220$nm (develops in MIBK:IPA 1:2). A detailed process flow for PMMA is in Chapter 7. PMMA was spun to 100nm; we were able to get complete quarter wafer coverage. The lack of edge beads enabled larger areas of contact when vacuum was applied between the mask and the substrate. Moving to a shorter wavelength makes the exposure less sensitive to gap variations than the 400nm exposures in 1813. We were able to get very uniform critical dimensions across the entire quarter wafer using PMMA.

The one drawback of PMMA is the possibility of slow to no development of a fine film (sub 20nm) in certain regions of the wafer. The problem surfaces because of a low field at the chrome/PMMA interface. Longer exposures help reduce this effect. Plasma ashing in oxygen also solves the problem. The ash must be well timed. A blind ash will remove the features. We used monitor wafers to test tolerance of the PMMA to ashing. Because we are working with large features, changes in dimension are negligible for such a thin resist.

6.5 Results

Figure 6-17 shows images of the final membranes on a frame. The sample successfully incorporates three modes of lithography, an exceptional case for the NanoStructures Laboratory. The layout of the since membrane device layer and alignment schemes utiliized are illustrated in Figure 6-16. Each type of lithography was exploited for it's strengths, be it large-area, resolution, cost, or speed. This theme must be carried

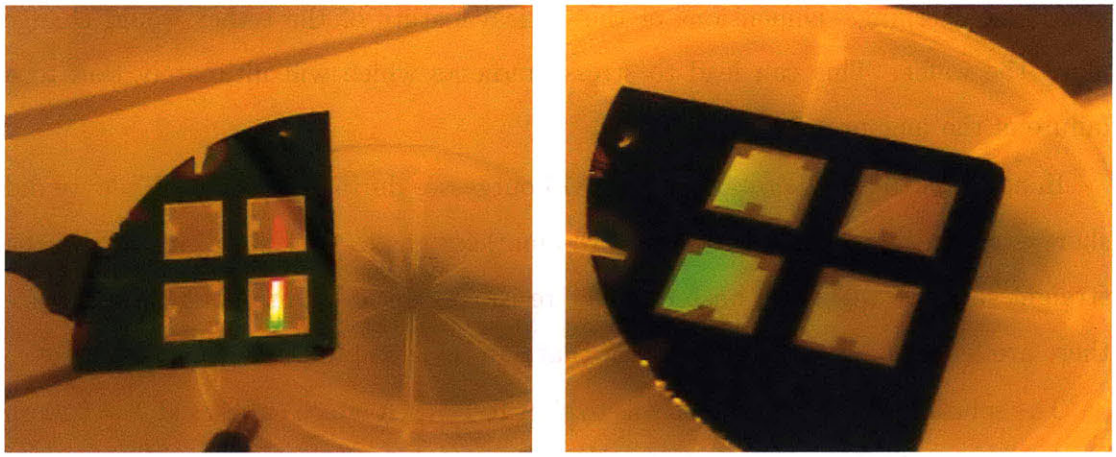

Figure 6-17: Final membranes with 10μm-wide tethers and ISPI gapping marks. We were able to manage high yield in the final batch of wafers. 11 out of 12 membranes survived over three substrates. Earlier runs suffered from around fifty-percent yields.

forward for the full realization of photonic crystals via membrane stacking. The final design consisted of tethers that were 50μm in length, with a spacing of 50μm (pitch), width of 6μm at the end of the taper, and a radius of curvature of 3μm. In the future it may be beneficial to reduce the radius of curvature and the width to improve cleave consistency. Also, we note that the etch to define the tethers was only 90 percent complete, as was done for the 2DPC in Chapter 2. Attempts to remove this residual layer after the membrane release lead to membrane failures. This residual layer did not hinder the cleaving of the structures.

The membranes were brought into contact with mesas measuring 9.8mm $\times$ 9.8mm in the procedure described in Chapter 5. The mesa was aligned within the boundaries of the tethers using a 3$\times$ camera to image the substrate plane. After the membrane was completely bonded, the frame was lowered in 200nm increments until fracture was initiated (at 6μm). Figure 6-18 is a photograph of the wafer after a successful transfer of a membrane to the mesa. We notice a smooth reflective surface with well-defined edges. Figure 6-19 and Figure 6-20 show closeup images of the final wafer.

The resulting wafer is free from particles. The tethers remain behind on the frame as is shown in Figure 6-21. The frame holds the excess margin of membrane that is

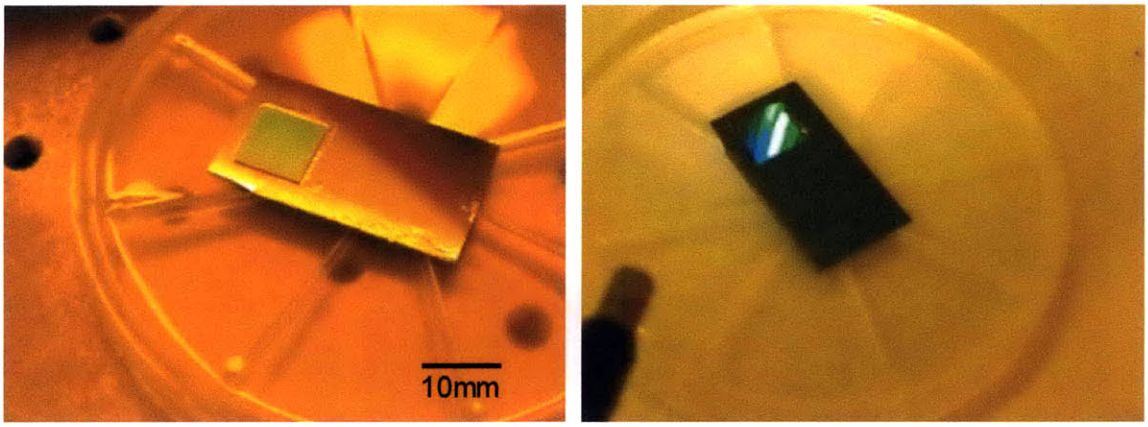

Figure 6-18: Successful stack of a 10mm × 10mm membrane onto a mesa via bonding and controlled release via stress engineering. Microscope images are shown in Figure 6-19 and Figure 6-20.

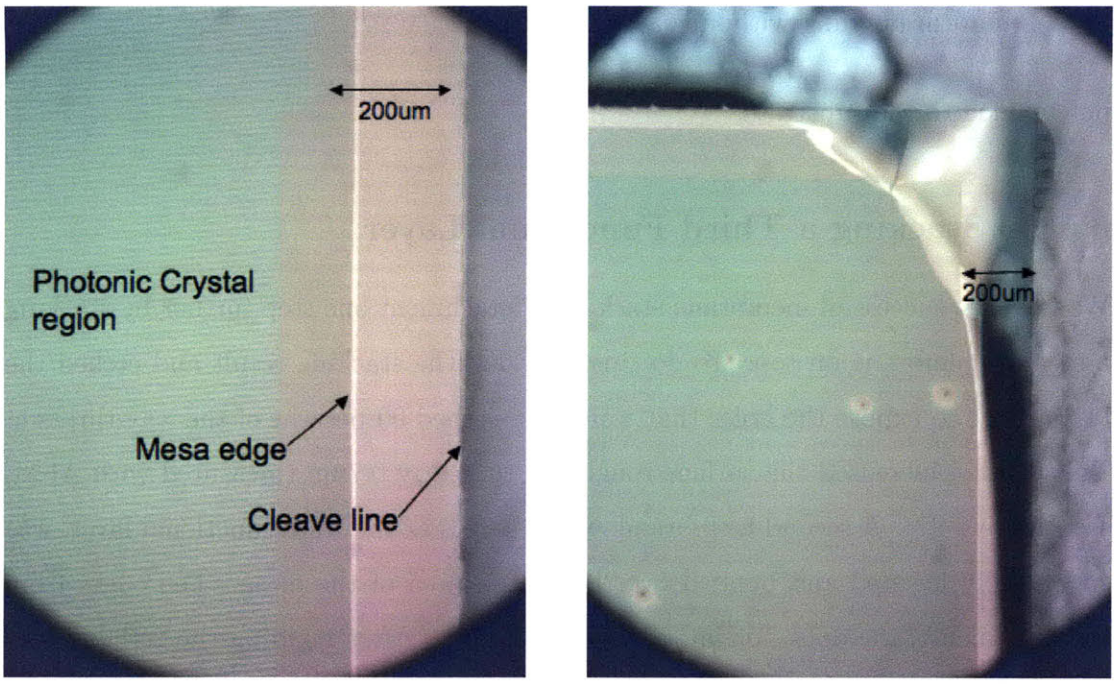

Figure 6-19: Membrane stacked on a mesa. There is a small area of margin that hangs over the mesa. The cleave line is well defined and there are no particles on the substrate. This sample is viable for additional layers.

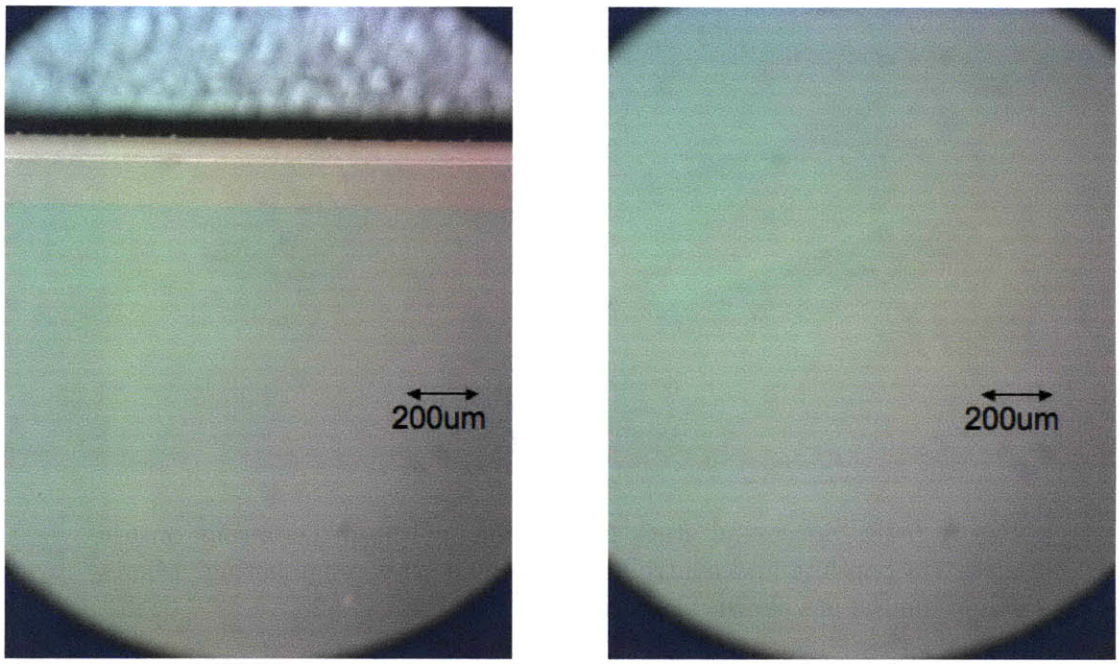

Figure 6-20: [Left] Controlled cleave along an edge. [Right] Large area, uniform bonding without particles.

not bonded to the substrate.

6.5.1 Stacking a Third Functional Layer

We take the successful membrane stack and detachment one step further by stacking a second membrane on top. To do this, we took the stacking result and etched the top surface to expose the holes that were only etched 90 percent of the way through. This etching increased the surface roughness to nearly 0.7nm (measured with AFM, see Figure 6-22). A second membrane, which serves as the third functional layer, was successfully lowered and bonded over the entire area of the mesa. The edges from the first membrane does not impede with bonding. After bonding the tethers were actuated with a 10μm drop. The result is shown in Figure 6-23.

The quality of the cleave is not as good as the first layer because the second layer overlaps the first. The overlap and potential contact of these regions can prevent the weak points from being exposed. A future scheme will require finger alignment between layers and perhaps a nesting method where, the area of each additional layer

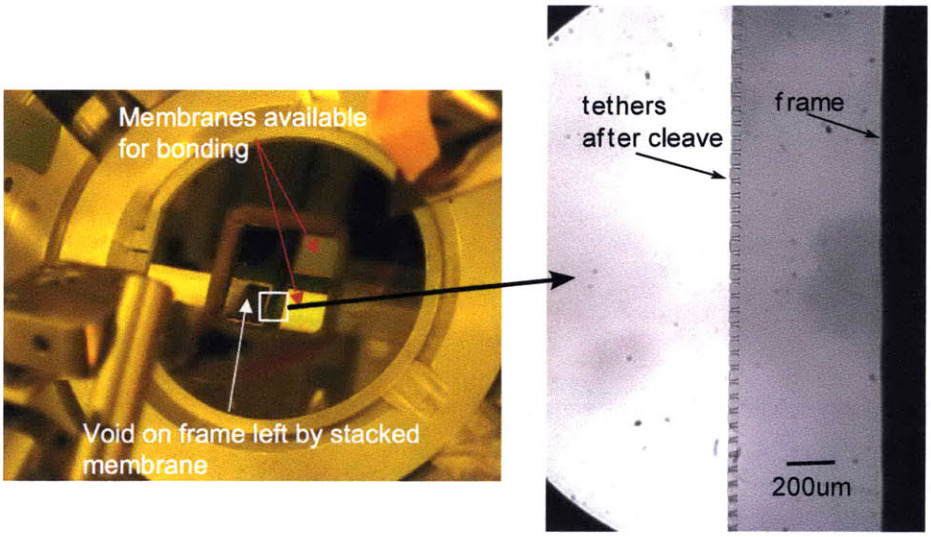

Figure 6-21: We observe the void left behind on the frame after the membrane has been bonded and detached. The excess membrane that does not bond to the substrate remains on the frame. On the right the tethers remain on the frame, which means that they do not contribute to particles to the sample.

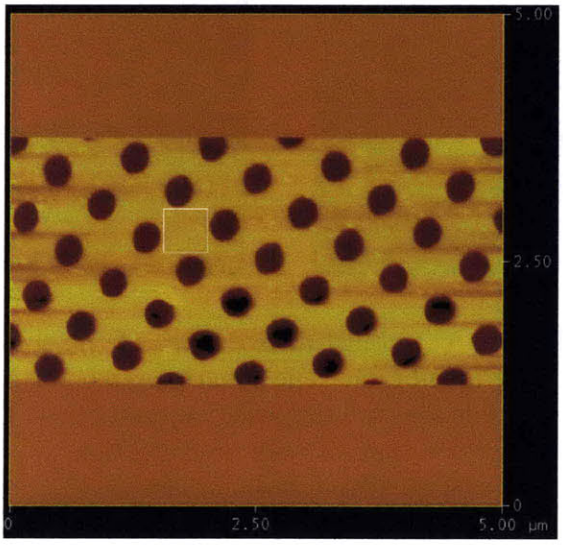

Figure 6-22: An AFM scan of the membrane surface after stacking and an RIE etch to open up the holes. Before the RIE, we measured the nitride to have an exceptional roughness of 0.11nm. This is the side that intimately touches the polished silicon surface during deposition. After RIE, the roughness increases to 0.7nm, which is also visible in this scan. Despite the increased roughness, we were able to observe bonding of an addtional layer.

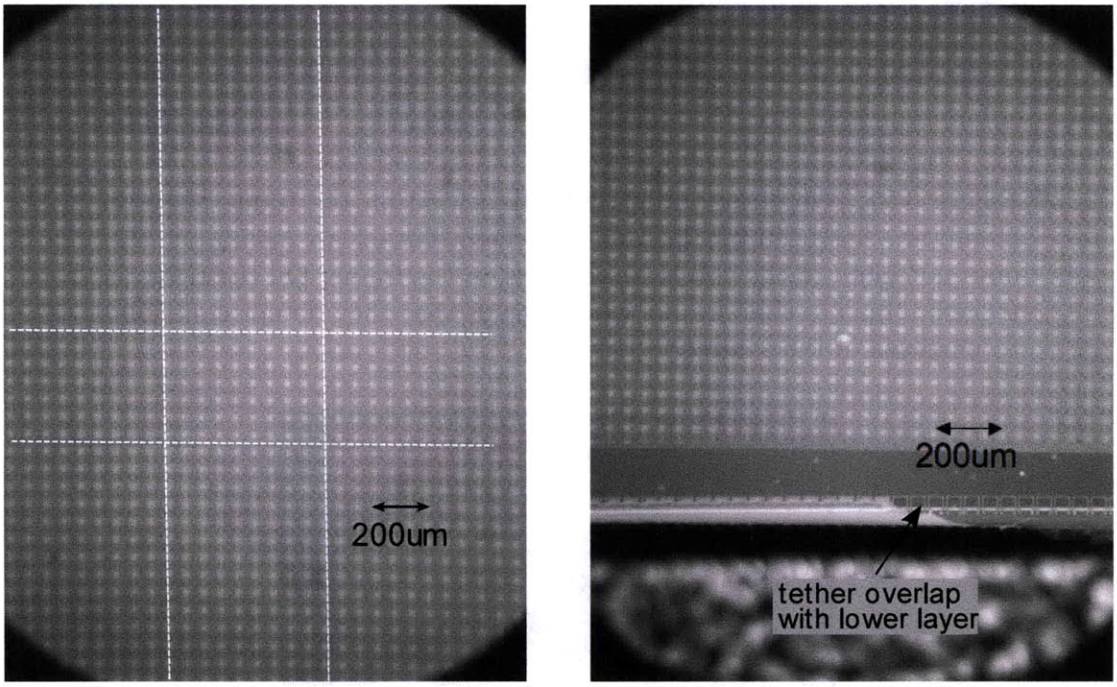

Figure 6-23: Large area optical micrographs of the second membrane stacked on the first membrane. The square moireè pattern comes from the fact that two grids are superimposed on each other. Guide lines are included to demonstrate that there is no distortion.

is slightly larger than the previous layer to ensure there is no overlap at the tether locations.

6.6 Conclusion

We have shown that stress-engineered cleaving is an effective way to detach a membrane from its frame. This technique satisfies our requirements:

1. Predictable control the cleave line so that stacked layers have well defined edges
2. Particle-free surface after detachment to enable multiple layer stacking
3. The integrity of the region of interest remains in tact
4. Efficiency so that the stacking yield is high and the stacking time is negligible

We have validated these qualities by successfully stacking a second membrane on top of the existing stack. In addtion, the device quality membranes created in this chapter utilized three modalities of lithography. This is an exceptional result because of the integration of alignment schemes and the duration of the process cycle.

Chapter 7

Fabrication of Free-standing Membrane Disc

7.1 Introduction

This chapter details other fabrication processes and techniques developed for the production of free-standing membrane devices. Specifically, we fabricated the suspended membrane disc shown in Figure 7-1. Ultimately, discs of 100μm and 60μm diameters centered within a 400μm aperture were fabricated. The discs are supported by four 3μm-wide support bars. This device is then used to demonstrate the quantum interference of deuterium (D_2) molecules via the Poisson Spot.

7.2 A History Lesson

In the early 19th century, the fundamental nature of light propagation stood on trial. The camps were divided between those believing in the corpuscular theory of light propagation and those who believed that light was a wave phenomenon. Intellectual heavyweights, Isaac Newton and Siméon-Denis Poisson believed that light was composed of particles that obeyed the laws of classical mechanics. Representing the antagonistic view, Augustin-Jean Fresnel postulated that light exhibited wave behavior. The debate came to a climax in 1818 when the French Academy hosted a

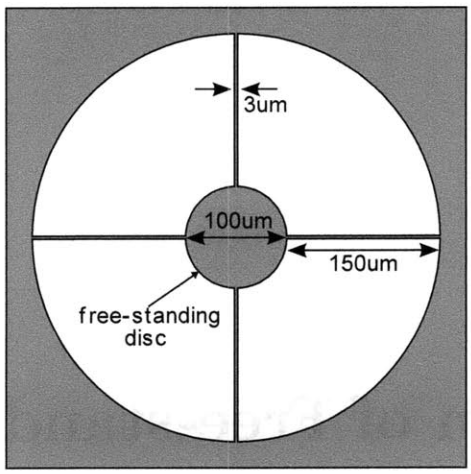

Figure 7-1: The free-standing membrane disc designed by Reisinger to conduct the Poisson Spot experiment with neutral particles. The thickness of the device is $< 1\mu$m.

competition to bring a resolution to the debate.

If the wave theory were true then there should be a bright spot of intensity in the shadow of a circular object. Obviously, this idea was counterintuitive. However, the French physicist Dominique Arago performed an experiment where a circular disc of 2mm was attached to a glass plate and illuminated from behind. He did indeed observe a bright spot, laying groundwork for the wave theory of light to evolve.

Professor Bodil Holst and her student Thomas Reisinger of the University of Bergen, Norway (formerly of TU Graz, Austria) desired to show the Poisson Spot experiment with molecules of deuterium. As we know from quantum mechanics, matter is described by a wave function. Because of the sub nanometer wavelengths, a smooth disc with less than 50nm of side-wall roughness is required.

7.3 Experimental Setup

Figure 7-2 shows the layout for the experiment. A supersonic beam of deuterium expands from a source. This beam is sampled with a skimmer to reduce the size and collimate the beam. The beam of molecules then sees the free-standing disc obstacle and diffracts off its edges. The beam of neutral particles is then ionized so they can

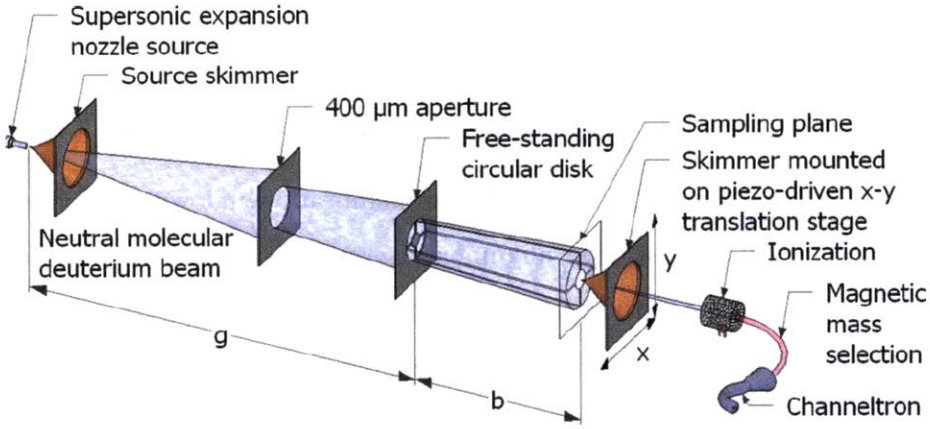

Figure 7-2: From left to right. A beam of deuterium expands out of a nozzle. The beam is sampled to a small area with a skimmer. The "collimated" beam illuminates the free-standing disc. The shadow of the disc is scanned. The experiment was done at TU Graz.

be detected. The detector is raster-scanned in the imaging plane to create a 2D map of intensity. The focus of our work at MIT was the fabrication of the free-standing disc to the specifications of the designer.

7.4 First-Generation Membrane Disc

In Chapter 2 we discussed the merits of patterning a membrane before it is released. For the large-area photonic crystal, this proved to be a worthy path because it resulted in efficient processing and high yield. However, for the fabrication of these smaller membrane devices, we chose to process the pattern after the membrane had already been released. This is the strategy also implemented in NanoOrigami [?, 36].The reasons are manifold, and they center around the lithography.

The layout is most effectively patterned with scanning-electron-beam lithography (SEBL). While the beam diameter can be on the order of a few nanometers, the resist experiences a much larger point spread function due to backscattered electrons[10]. This effect is a function of the substrate material and its thickness. Working on a membrane dramatically reduces backscattered electrons. The beam's point-spread function becomes less blurred. This allows us to achieve a higher fidelity pattern

with a more forgiving dose window. Additionally, proximity effect correction is not required.

Second, since we are fabricating a relatively small device, we prefer to work with smaller membranes($500\mu m \times 500\mu m$). If the membrane windows are defined before the lithography then no backside alignment is required. Membrane windows are readily detected in the exposure tool using the backscatter electron detector. As was discussed above, the yield in backscattered detectors falls dramatically when transitioning from a bulk substrate to a membrane.

Finally, an exposure on the SEBL tool is expensive in terms of cost and time. We maximize yield by reducing the number of steps that occur after exposure. Taking care of the membrane release early results in the best yield for written devices. If one were to release after processing, we can easily imagine a scenario where the aperture and the backside membrane are misaligned rendering a zero yield and wasted hours on the SEBL tool.

The fabrication process for the first generation is shown in Figure 7-3. We start with a $1\mu m$-thick silicon nitride membrane. We use e-beam evaporation to put down 30nm of chrome. The thickness is optimized to minimize compressive stress while still serving as a sufficient dry etch mask. The chrome also serves as a conductive layer during the lithography. Above the chrome, we spin on 100nm of PMMA. Membranes are tricky to process because they are not compatible with the vacuum chucks required for spinning. Essentially, one never wants to put a pressure differential between the two faces of the membrane. We circumvent this limitation by taping the membrane sample at the corners to a whole wafer which is held by the vacuum chuck. This allows us to safely spin on the sample.

7.4.1 SEBL

The exposure was done on the IBM VS-26 SEBL tool[9, ?]. This tool can only fill rectangular geometries. The round aperture geometry was approximated into rectangles with software written by Chris Dames. It generates a .kic file of boxes from an arbitrary polygon input[19]. The tool can also write the entire pattern in a

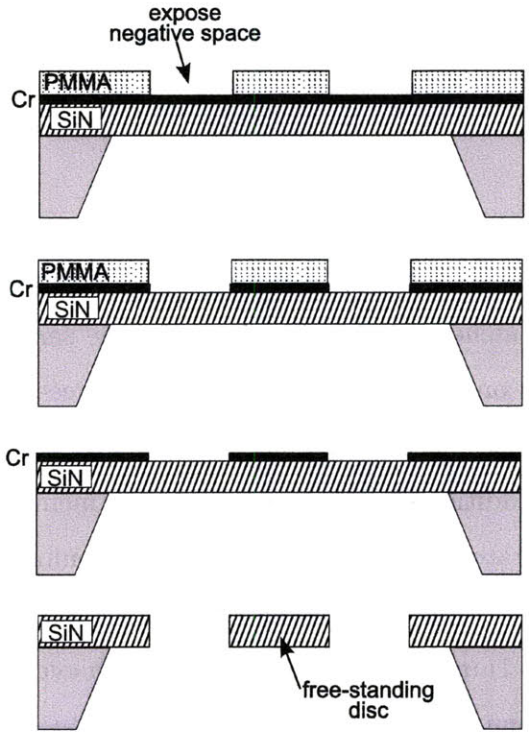

Figure 7-3: The first generation process for fabricating free-standing discs. Patterning of void regions is done directly on the membrane Chrome serves as the hard mask and the conduction layer. The pattern transfer from PMMA to chrome is done through wet etching. The chrome layer is slowly sputtered away during the SiN etch. No wet processing is done after the structure is free-standing.

single field (25nm × 25nm pixels with 409.6μm field).

Ultimately, we want to etch away the negative space of the device (reference Figure 7-1). Because we use a positive resist and direct transfer to the metal mask, we expose these regions in the tool. After exposure, the PMMA is developed in 2:1 MIBK:IPA (at a temperature of 21°C) for 90 seconds and subsequently rinsed in IPA for 30 seconds. The exposed chrome is etched in CR7 diluted 3:1. Because the etch is nonlinear, a monitor wafer (taken from the same chrome evaporation batch) is etched first to determine the etch rate.

7.4.2 RIE

After transferring the pattern into chrome, the PMMA is ashed away in an O_2 plasma. The negative space is etched away with RIE using the same chemistry explored in Section 2.3.2. There is one key subtlety when etching free-standing structures. The samples should be raised on glass slide stilts so that there is a large gap for air to evacuate and vent. Additionally, heat buildup on a membrane during an etch in vacuum can alter etch rates. In order to prevent gross nonlinearities, the etch process consisted of etching for 5-7 minutes, venting, inspecting and then continuing the etch. For a thick SiN film of 1μm, there were typically 6 etch cycles.

After the etch is complete and the structure stands on its own, there is no additional processing done. Wet processes at this point would destroy the structure. The chrome mask sputtered away slowly during the long etch. Figure 7-4 shows the completed freestanding discs in silicon nitride. It should be noted that the yield of this process was well over 80%. While the structural integrity is sound, we observe large sidewall roughness on the order of 250nm peak-to-peak. The next section discusses two modifications to the process to bring the the roughness down to specification.

7.5 Second-Generation Membrane Disc

Sidewall roughness in the first generation devices emanate from two sources. The first is the lithography in PMMA. The second is webbing that is the result of etching

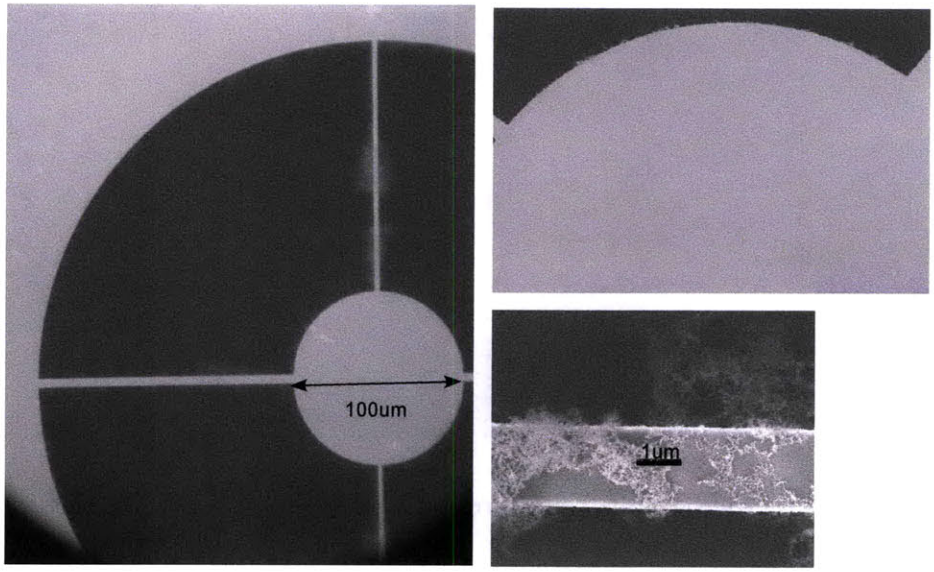

Figure 7-4: Micrographs of the first generation aperture. The glaring flaw in this series is the side-wall roughness. The roughness emanates from too coarse a pixel during SEBL patterning and large-area membrane etching. The picture on the lower-right clearly shows a mesh of unetched SiN membrane.

large areas of free-standing membrane material.

The roughness that comes from the SEBL tool is addressed by moving to a 10nm step size from 25nm. This requires that the write field is scaled accordingly to 160 μm, which means that our device will not fit into a single write field. We must, therefore, stitch multiple fields together. SEBL stitching introduces distortion into the pattern. A discussion about the causes and magnitude of stitching errors is explored in Todd Hastings' thesis [24]. This is solved by writing the key feature, the central disc (whose size is smaller than the write field), within a single write field and stitching the other fields around it. This allows us to utilize finer beam. Figure 7-5 clearly shows the marked improvement.

RIE of membranes works similarly to bulk materials up until the final few nanometers of material. At this point the etch becomes a mesh of material that is not easily cleared. After discussions with NanoOrigami team members, Tony Nichol and Will Arora, it was determined that the mesh can be eliminated by reducing the area that is etched. This is accomplished by etching a 1μm outline of the negative space rather

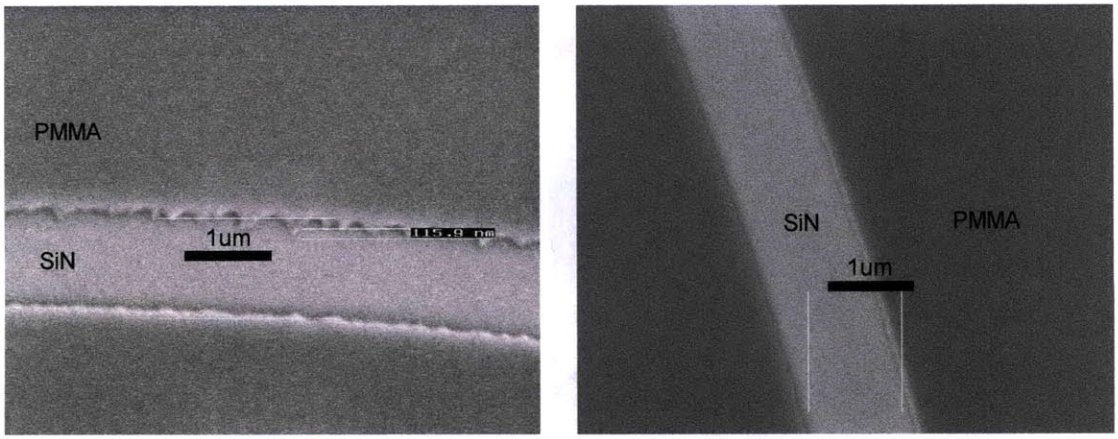

Figure 7-5: Micrographs taken from arc of aperture. On the left we see the roughness that comes from the coarse 25nm pixel. On the right we see a significant reduction in roughness by moving to a 10nm pixel. Exposures were on the VS-26 tool at MIT.

than the entire area. A side benefit is a dramatic reduction in write times proportional to the square root of the area of the device. Figure 7-6 summarizes the changes in processing to yield a better disc.

The final device incorporating the processing improvements is shown in Figure 7-7. We obtained a marked improvement in side-wall roughness with this generation (see Figure 7-8). There is one tradeoff in using the new process; we observed a reduction in device yield. This occurs because the material in the void regions does not always fall out when the etch is through the material. Instead, these flaps of material can stray onto the functional area of the device (see Figure 7-9). On a chip of 9 devices, 2 were functional. There is the potential to improve the yield by changing the width of the outline.

7.6 Experimental Results

The devices from both generations were shipped to TU Graz and inserted into the experimental setup (note their position in Figure 7-2). Holst and Reisinger successfully demonstrated the Poisson Spot phenomenon with Deuterium[45]. Figure 7-10 is a 2D image showing a measured bright spot in the shadow of the aperture. Figure 7-11

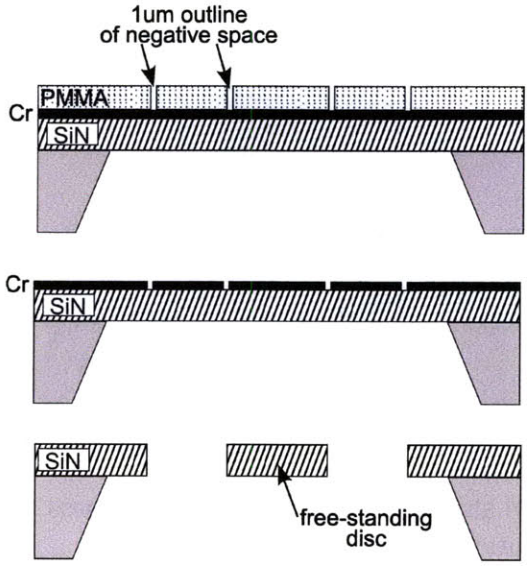

Figure 7-6: The final process used for disc fabrication.

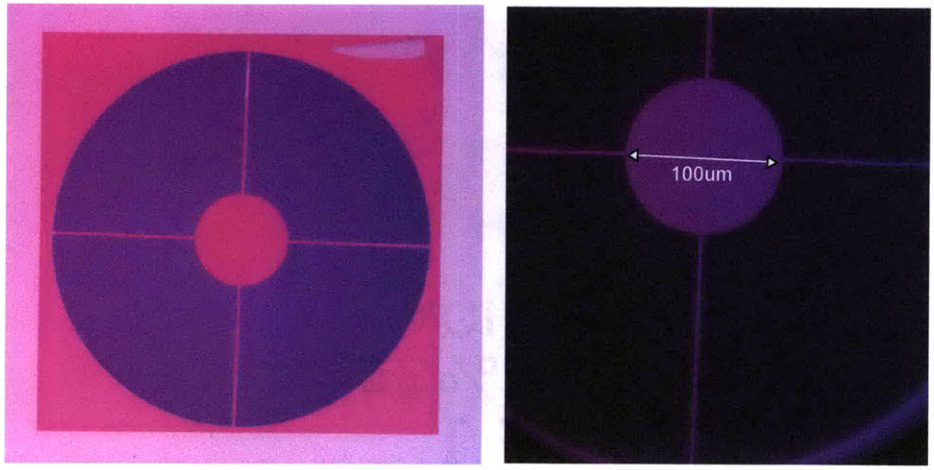

Figure 7-7: Second-generation aperture sits in a membrane window that is 450μm $\times$ 450μm. There is no mesh residue on this final device.

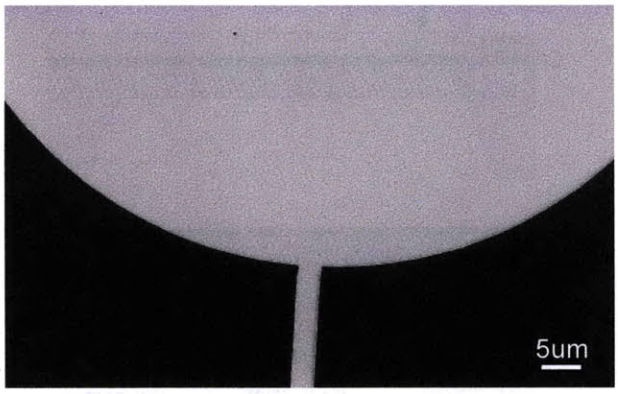

Figure 7-8: SEM showing 50nm side-wall roughness achievement using the modified fabrication process.

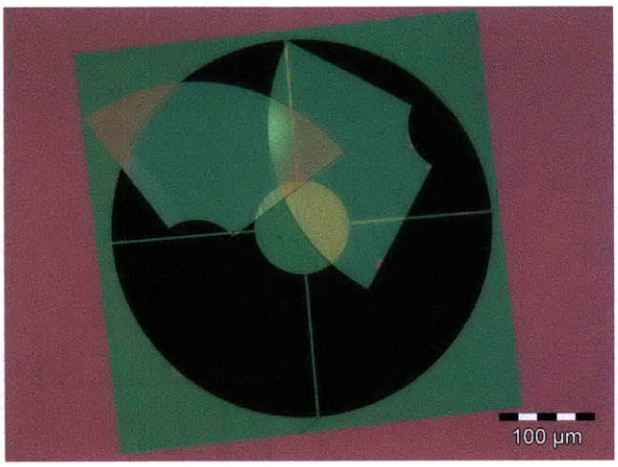

Figure 7-9: Flaps from the negative region do not always fall away as is shown here.

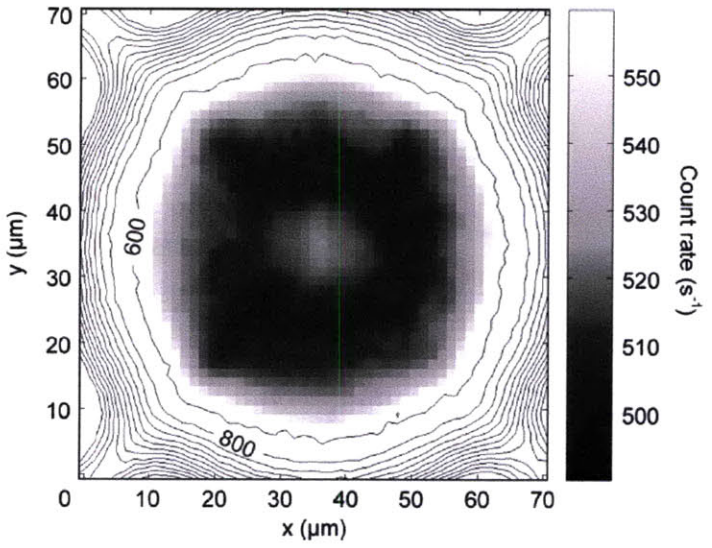

Figure 7-10: An image of the Poisson spot using molecules. The position of the support bars are featured in the corners of the image. The outer region is contour map of the count rate and the inner region is a gray-scale image. There is a clear intensity peak caused by the diffraction off the disc edge. For this image the sampling distance was 321mm behind the disc. Taken from [45]

are cross-sectional slices of intensity at three different sampling planes behind the aperture. They are compared with simulated values.

The experiment was successful because physicists were able to confirm a hypothesis about the laws of nature using experimental observation. In addition new nanofabrication techniques were developed for the processing of membrane devices. These techniques were taken as the foundation for the fabrication of free-standing-zone plates used in neutral particle imaging [44].

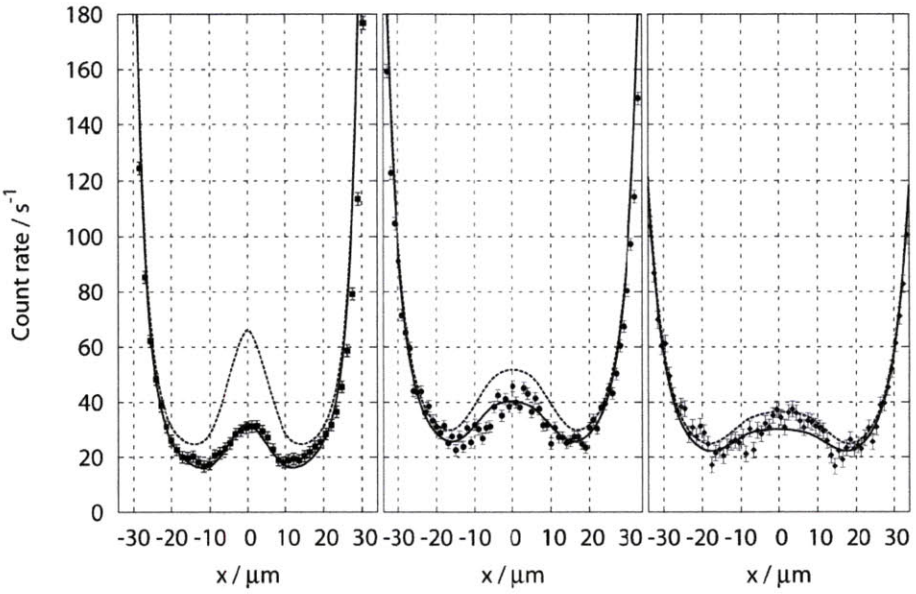

Figure 7-11: The Poisson Spot at three different sampling planes: (a) 321mm, (b) 641mm, (c) 801mm. The dashed line comes from simulations of an ideal circular disc. The simulation results represented by the continuous line take the sidewall roughness of the disc. The roughness was approximated as a sinusoidal variation with a period of 1μm and peak-to-peak amplitude of 300nm. Taken from [45]

Chapter 8

Conclusion and Future Work

The membrane stacking approach to three-dimensional nanofabrication is a compelling alternative to the layer-by-layer methodology. Membrane stacking offers higher yield, lower production costs, and shorter fabrication times. The fruition of this vision depends upon a high stacking yield. There are two significant challenges to the stacking problem, large-area membrane bonding and membrane detachment from the host frame. In order to solve the former we applied the mesa architecture and along with precise six-axis control using ISPI; We achieved very small and uniform gaps between the membrane and the substrate. The result was very rapid and repeatable bonding.

Detaching the membrane from its frame is the most prominent challenge we address in this work. Once the membrane has been bonded, stress-engineered cleavage allows us to detach the membrane from its frame in an efficient manner. The result is a clean and well defined surface upon which a another membrane can be bonded. The efficiency of this method was demonstrated by stacking two membranes on a patterned mesa (three total functional layers) within a few hours. The alternative processing methodology would require at least a two to four weeks of additional processing with a lower probability of success.

Achieving the final multilayer result required incorporating three modes of lithography into a single device layer. This is a very unique characteristic of this research. They key to high-resolution lithography is using the method that is most aligned to

the application at hand. Here, myriad requirements encouraged the mix and match approach.

8.0.1 Future Work

There is a great deal of interesting work to pursue looking forward. While we had great success with silicon nitride, it will be interested to see how the platform works with silicon membranes. Releasing patterned-silicon membranes with high yield using silicon-on-insulator is one of the challenges we are currently tackling. We desire the same batch processing and large yield that silicon nitride enabled. The hope is that we can create membranes with the same area as we saw with silicon nitride.

Coherent diffraction lithography has the potential to solve the needs of three-dimensional photonic crystal development. However, this lithography technique will enable new applications. For example, frequency doubling gratings will be enabled by the registration. Immediately, the priority is to push the tool to create uniform patterning exceeding 10mm $\times$ 10mm, and apply registration using ISPI. This will enable the generation of holes and rods on a single membrane. Here, we used 2DPC with holes to demonstrate the proof of concept. Integrating holes and rods together with large-area membranes is a difficult challenge remaining.

More design work is necessary for stress-engineered cleavage of membranes. The current designs can be tuned in order to achieve superior fracture rates. The designs will change when the platform is moved over to silicon since it does not have the same residual stress as nitride. We must also incorporate better alignment schemes through the process to reduce excess membrane margins and prevent the cleave structures from overlapping with the layer below it.

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