A fabrication method for integrated filter elements with inductance cancellation

Citation: Pierquet, B.J., T.C. Neugebauer, and D.J. Perreault. "A Fabrication Method for Integrated Filter Elements With Inductance Cancellation." Power Electronics, IEEE Transactions on 24.3 (2009): 838-848. © 2009 IEEE.

As Published: http://dx.doi.org/10.1109/TPEL.2008.2011638

Publisher: Institute of Electrical and Electronics Engineers

Persistent URL: http://hdl.handle.net/1721.1/60232

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

A Fabrication Method for Integrated Filter Elements With Inductance Cancellation

Brandon J. Pierquet, *Student Member, IEEE*, Timothy C. Neugebauer, *Member, IEEE*, and David J. Perreault, *Senior Member, IEEE*

***Abstract*—This paper outlines a fabrication method for integrated filter elements. An integrated filter element is a three- (or more) terminal device comprising a capacitor and coupled air-core magnetic windings, in which the magnetic windings cancel the effects of capacitor parasitic inductance. This provides greatly enhanced filtration performance over a capacitor alone. Methods for designing and forming cancellation windings are described, along with means for repeatable interconnection with the capacitor and encapsulation of the filter element. The high performance and repeatability of filter elements fabricated with the proposed method are demonstrated with several examples.**

***Index Terms*—Capacitors, electromagnetic interference (EMI), inductance, interference suppression, power quality.**

I. Introduction

FILTERS designed to suppress electromagnetic interference (EMI) often play a critical role in meeting requirements for device compatibility. Component parasitics, such as the equivalent series inductance (ESL) of capacitors and the equivalent parallel capacitance of inductors, often limit the size and performance of these filters [1]–[14]. Recent work has addressed methods to compensate for these parasitics, thereby increasing filter performance [5]–[15] The use of coupled magnetic windings has been shown to be effective in compensating for the effects of capacitor parasitic inductance, increasing its attenuation performance and reducing the filter volume and cost [5]–[7], [14].

Consider the low-pass filter in Fig. 1(a), shown with the first-order capacitor parasitics of equivalent series resistance (ESR) and ESL. At high frequencies, the equivalent series inductance of the capacitor causes an increase in the capacitor's impedance, greatly reducing the filtration performance in this region, where it is often most desired. The solid trace in Fig. 2 shows the effect of this increased impedance on the attenuation performance of the simple filter. To compensate for the parasitic effects of the capacitor, additional capacitors providing better high-frequency performance are normally connected in parallel with the main capacitor, increasing the circuit size and cost.

Manuscript received July 14, 2008. First published March 4, 2009; current version published April 8, 2009. This work was supported in part by the Office of Naval Research Grant N00014-02-1-481 and by the Air Force Research Laboratory through a National Defense Science and Engineering Graduate Fellowship. Recommended for publication by Associate Editor B. Ferreira.

B. J. Pierquet and D. J. Perreault are with the Laboratory for Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: pierquet@mit.edu).

T. C. Neugebauer is with Charles Stark Draper Laboratory, Cambridge, MA 02139-3563 USA.

Digital Object Identifier 10.1109/TPEL.2008.2011638

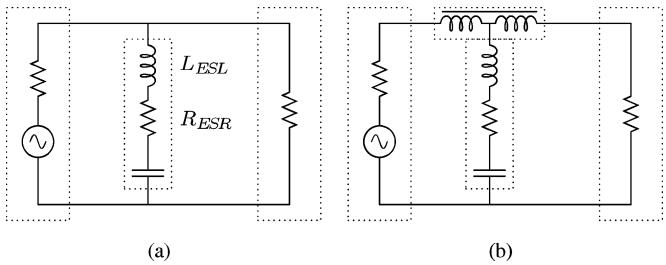

Fig. 1. Single-capacitor low-pass filter models with first-order capacitor parasitics. (a) Standard filter. (b) Filter with inductance cancellation.

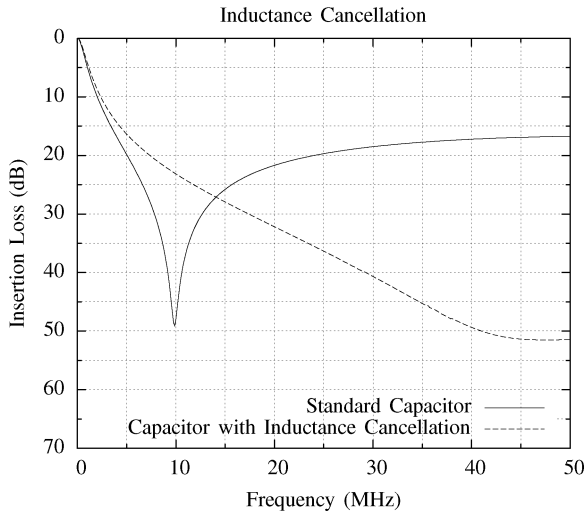

Fig. 2. Measured results from the low-pass filters in Fig. 1 showing the difference in performance between a circuit with a 4700 pF ceramic capacitor and one with the addition of inductance cancellation. The insertion loss is measured with 50 Ω source and load impedances. The capacitor has an approximate ESL of 50 nH.

An alternative to adding additional capacitors is to try to reduce the effects of the device parasitics. An example of the performance that can be achieved with reduced parasitic inductance can be seen in the dashed second trace of Fig. 2. To achieve this performance, a coupled inductor structure can be inserted into the circuit to induce a voltage that counteracts the voltage due to capacitor ESL [5]–[7], [14], as illustrated in Fig. 1(b). The designed cancellation effect can be achieved using the mutual coupling of magnetic flux between coupled inductor windings, illustrated in Fig. 3. Fig. 4 shows an equivalent two-port T model. When combining the models of the coupled inductor with that of the capacitor, the model in Fig. 5 results. To completely suppress the effects of the capacitor ESL, the residual shunt inductance L'_{12} is designed to be zero. An advantage

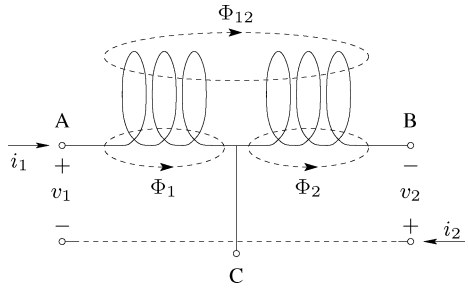

Fig. 3. Flux linkage in "center-tapped" magnetically coupled windings.

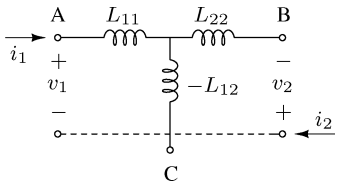

Fig. 4. Equivalent two-port "T" model of the coupled-winding structure shown in Fig. 3.

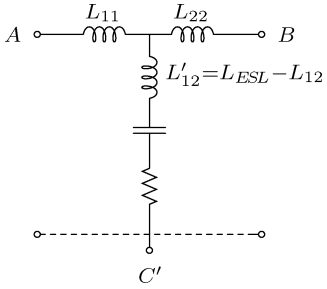

Fig. 5. Equivalent inductive "T" model of an integrated filter element, additionally showing shunt capacitance and resistance. Inductance cancellation is achieved by matching the winding mutual inductance L_{12} to the capacitor parasitic inductance L_{ESL}.

of this technique is that the coupled magnetic windings used to achieve cancellation can be very small, with inductances of the order of the parasitic inductance, typically 5–25 nH, being cancelled.

As developed in a previous work, a filter with inductance cancellation can be implemented with conventional capacitors and an air-core inductance cancellation winding printed on a circuit board [5]–[7], or discretely constructed [14]. These approaches are both highly effective, but each necessitates significant effort on the part of the circuit designer to design and implement the inductance cancellation winding in the context of a particular application. Another approach considered here is the development of an integrated filter element that can be provided to the circuit designer as a basic building block. An integrated filter element is one or more inductance cancellation windings packaged together with a capacitor to form a three- (or more) terminal device that provides greatly enhanced filter attenuation. Integrating the capacitor and windings creates a self-contained filter element that can easily be used in a wide range of circuit designs.

Repeatability is a primary concern when implementing inductance cancellation. Deviation in the final shunt inductance

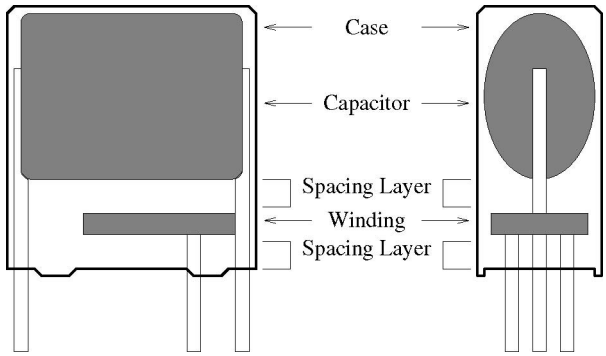

Fig. 6. Basic structure of an integrated filter element, where the magnetic winding is integrated with a capacitor into a single package.

can have a significant impact on the realized performance [6]. Printed circuit board (PCB) windings provide a consistent, repeatable structure that results in a very small variance, but can require a significant board footprint and must be redesigned for each circuit. For an integrated filter element, the design must be completed only once, but requires a repeatable fabrication method to ensure consistent performance for each device.

This paper develops a method to fabricate a cancellation winding and integrate it with a capacitor within the capacitor casing. The method is validated experimentally, and the performance and repeatability of the method are evaluated. Section II outlines the general design and fabrication process for an integrated filter element. Section III details the implementation of the developed process for two EMI filter capacitors. Section IV presents the performance characterization and design validation for the two constructed integrated filter elements. Section V concludes the paper.

II. Integrated Filter Element Design Process

An integrated filter element contains two primary components packaged together: the capacitive element and the magnetically coupled winding. Constraints are placed on the physical size and orientation of the magnetic winding to achieve the desired filtering performance, minimize sensitivity to variations in external conditions (e.g., ground plane proximity [6]), and provide spacing to meet voltage breakdown and clearance requirements. Fig. 6 illustrates a cutaway view of how these elements may be oriented and combined into a single package.

The maximum desirable outline size for the magnetic winding is limited by the capacitor cross-sectional area. However, it can be designed to have any number of layers and be constructed from any conductor thickness to obtain the appropriate inductance and series path resistance.

The fabrication process for the integrated filter element considered here is composed of two primary tasks: first, the design and construction of the coupled magnetic winding and second, electrically connecting and encapsulating the capacitor and winding into a single physical package. The resulting integrated filter elements are tested and characterized to validate the design and fabrication process.

Fig. 7. Example layout relationship for a winding footprint within the capacitor footprint.

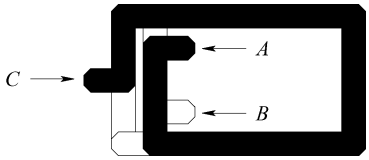

Fig. 8. Example two-layer inductance cancellation winding design to be used as a starting point for winding designs. The top layer is represented in solid black and the bottom layer in white. The two layers are mirror images of each other and electrically connected at point C.

A. Winding Design and Fabrication

Guidelines for the design of inductance cancellation windings on PCBs are given in [6] and [7], and more thoroughly developed in [15]. However, the windings designed for integration can have a significantly smaller footprint than those used in the PCB designs, due to the increased thickness of the conductor that can be employed as compared to the thin traces on a PCB. In both cases, the winding should be designed with a mutual inductance equal to that of the ESL of the capacitor of interest, including the contribution from any spacing layers.

For the winding designs considered here, an outer footprint is chosen to allow adequate clearance of the capacitor terminals and package edges. Both capacitors considered in this paper have a footprint shape similar to the one shown in Fig. 7, where the positioning of the winding relative to the capacitor footprint and terminals is illustrated by the dashed outline.

Analytical solutions for some geometries of coupled magnetic coils exist [16]–[18]; however, the use of a computer-aided design (CAD) package such as FastHenry [19] greatly simplifies the process of calculating the inductance and resistance for arbitrary winding designs. While no rules of thumb have been developed to instantiate the design process, over the course of this study, it has been found that a two-layer winding design is adequate for a wide range of capacitor package sizes from various manufacturers. Fig. 8 shows a typical two-layer winding pattern that can be used as a starting point for a design.

The greatest benefit of a two-layer design comes from its relative simplicity and ease of fabrication. The winding can be inexpensively fabricated from a single-layer pattern that can be constructed from a sheet of conductive material with the appropriate thickness. The desired pattern can be formed in a number of ways: stamping, chemical etching, mechanical milling, or cutting with an abrasive jet (water jet). This single-layer design can then be folded or joined into its final form. Fig. 9 shows a single-layer winding pattern that can be folded into the two-layer design illustrated in Fig. 8.

Additional leads must be attached to the winding at its endpoints to ensure that they extend outside of the final encapsulation. This can be done by soldering or otherwise joining short

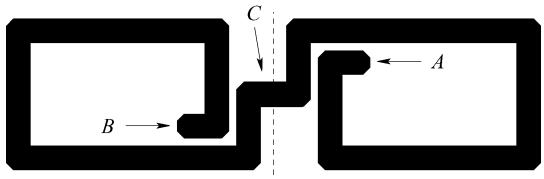

Fig. 9. Example of inductance cancellation winding design shown in a single-layer pattern, which can be of folded into the design of Fig. 8.

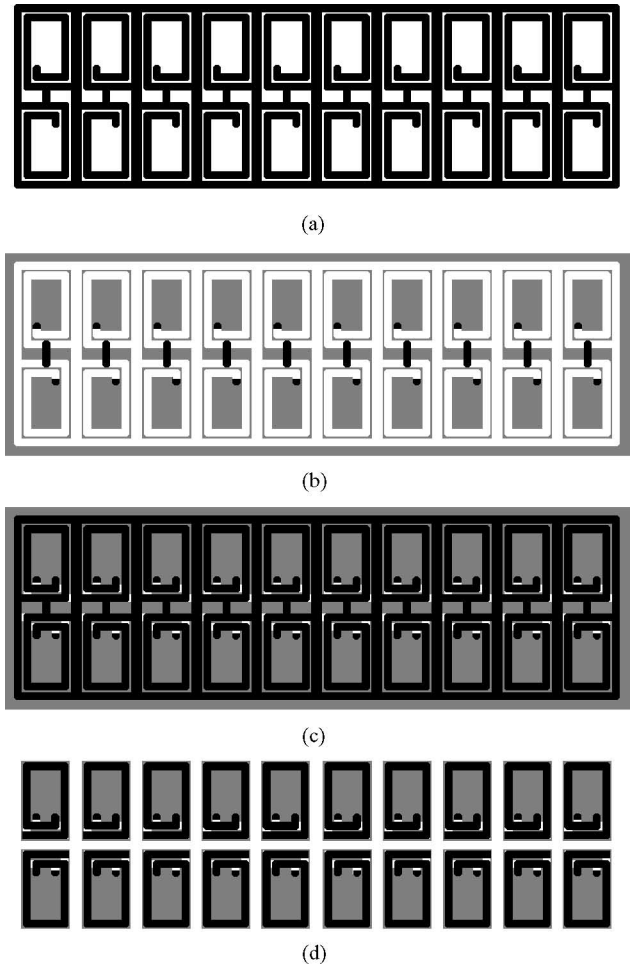

Fig. 10. Steps to create a batch of windings from two sheets of a symmetrical single-layer pattern. Black represents the exposed conductor, gray is the insulating mask, and white represents the masked conductor. (a) Original single-layer sheet. (b) Electrical insulation/solder-mask. (c) Two sheets aligned. (d) Detabbed and separated.

wires perpendicular to the winding. Alternatively, the two external terminal leads can be constructed as part of the original winding pattern and bent appropriately to extend outward.

In a controlled manufacturing process, the forming and folding of the windings can be automated to provide a consistent, repeatable result. However, folding the windings individually by hand for prototyping purposes does not necessarily provide the same consistency. For this reason, an alternative process for constructing windings has been developed, which is suitable for either manual or automated fabrication.

The method depicted in Fig. 10 is ideal for forming many identical cancellation windings at a time. One can cut a number

of single-layer patterns on a metal sheet such that they are held in by a number of cut tabs (e.g., as done with lead frames), an upper and a lower sheet can be overlaid to align any number of windings simultaneously. If a symmetrical winding design is used, as is done here, a single pattern can be used for both the top and bottom sheets, with one of the two flipped to provide the mirrored pattern. This ensures that each winding is aligned identically to the others on the sheet, greatly reducing the part-to-part variation. The sheet of windings, as shown in Fig. 10(a), produces a total of 20 windings; the number of windings can be easily adjusted to scale from prototyping to volume production. The full process can be separated into three main steps: insulation masking, soldering and alignment, and detabbing to separate the windings from the sheet.

The two sheets are electrically insulated with a thin material, such as adhesive-backed polyimide tape, which can withstand temperatures used for joining. Mask holes are cut in the insulating material where the joints between layers will exist, and then, solder paste is applied. To join the two sheets together, the top sheet is aligned over the lower one, then placed on a hot plate or in a solder reflow oven. The sheets should be fixed in place to avoid any movement as the solder paste wets and solidifies. After the joining of the two sheets, the windings can be removed from the sheet by cutting at the tabs. The windings are then ready to be integrated with capacitors.

B. Integration and Encapsulation

The process of integration involves electrically joining the cancellation winding with the capacitor and exposing the external terminals. One electrode of the capacitor remains as an external lead for the filter element, whereas the other is connected to the winding; the two endpoints of the winding become external leads of the filter element, forming a three-terminal filter component.

Attaching the winding to the capacitor electrode should be done in a manner that can be precisely repeated, as the attachment location on the capacitor electrode impacts the effective shunt inductance of the filter element, which, in turn, influences the inductance cancellation performance. If the inductance cancellation winding is to be integrated as part of the initial capacitor fabrication process, the winding can be attached to the capacitor lead a specific distance from the metalized film roll a number of ways before encapsulation: placing insulating spacers between the capacitor–winding and winding–environment interfaces, forming detents in the filter casing to position the winding relative to the capacitor and case surface, setting the desired spacing by potting each device in separate stages, or controlling the insulator thickness of the winding. Multiple methods can be combined to achieve more complex insulation requirements.

If the capacitor is already potted, as shown in the cutaway capacitor of Fig. 11, the winding can be positioned at a fixed distance from the bottom of the capacitor case instead, as the winding cannot be positioned directly against the potting compound at the bottom of the capacitor due to the inconsistent potting height, which varies measurably between capacitors. To position the winding relative to the bottom of the case, a small

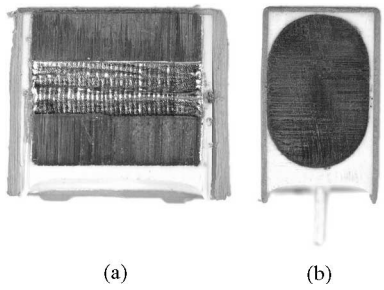

Fig. 11. Cutaway photographs of a Vishay BCcomponents Series MKP338 2222-338-24334 330 nF X2 film capacitor. (a) Side cut. (b) End cut.

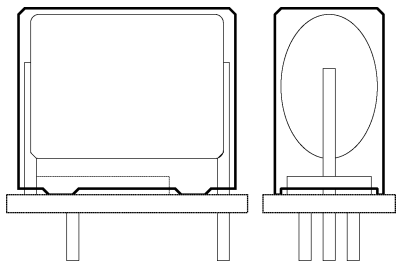

Fig. 12. Example fixture used to position the winding flush with the bottom of the capacitor casing for repeatable alignment and joining with the capacitor.

alignment fixture, shown in Fig. 12, is used to hold the winding, allowing it to be repeatably positioned on the capacitor for soldering.

With the capacitor and winding electrically connected and external leads brought out, the final step is to encapsulate the filter element. The encapsulation provides mechanical stability as well as electrical and environmental isolation. For prototyping purposes, it can also be used to tune the final filter element performance. The mechanical and electrical characteristics can be controlled by using different sized enclosures, adjusting the positioning of capacitor and winding, or using specialized potting compounds. In particular, an appropriate clearance from external conductive elements (e.g., the metalized capacitor film or an underfoot copper pour) should be ensured as the winding may induce eddy currents in these nearby materials, impacting the inductance cancellation performance.

To provide adequate clearance between the winding and the bottom of the filter element in prototype designs, the height of the original capacitor may need to be extended. In the prototyping stage, the height may be increased by wrapping adhesive tape around the capacitor, leaving a small overhang at the bottom of the casing extending past the cancellation winding, then filling this cavity with a potting compound. In production, the capacitor and winding would simply be placed in a more appropriately sized case.

When setting the final filter element height using encapsulant, as shown in Fig. 13, the residual shunt inductance of the filter can be controlled: increasing the height to add additional inductance or decreasing the height to reduce the inductance. For prototyping work, this allows a fine tuning of the filter element performance at the encapsulation stage without the need to change the winding design or alignment fixture.

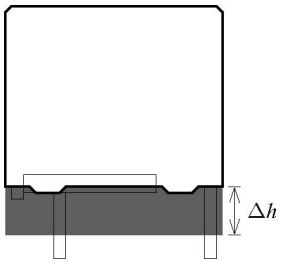

Fig. 13. Illustration of how the potting process can be used to control the filter element residual shunt inductance by modifying the height of the filter element, using the method shown in Fig. 16.

C. Validation and Testing

Two measurement methods are used to validate the proper tuning and operation of the inductance cancellation for the integrated filter elements: a method based on multiple two-terminal impedance measurements, and a two-port insertion loss measurement. The impedance measurements are used to calculate the residual shunt inductance of the integrated filter, and insertion loss allows the frequency response of the filter element to be measured directly.

1) Two-Terminal Impedance Measurements: Measuring the residual shunt inductance of the filter element provides a single value that can be used to compare devices and to verify that the fabrication method is providing consistent results. The measurement results can also be used to determine the parameter values of the filter T model for use in circuit simulation packages such as SPICE.

Measurements of the inductance between terminals AB, BC', and AC' are required to determine the inductance parameters in the T model of Fig. 5. These three measurements can be written as

$$L_{AB} = L_{11} + L_{22} \tag{1}$$

$$L_{BC'} = L_{22} - L'_{12} \tag{2}$$

$$L_{AC'} = L_{11} - L'_{12} \tag{3}$$

where L'_{12} is the residual shunt inductance, representing the sum of the cancellation winding mutual inductance, the capacitor equivalent series inductance, and any secondary effects due to inductive coupling between the winding and capacitor. The value of L'_{12}, L_{11}, and L_{22} can be found from the three measurements, using

$$L_{11} = \frac{L_{AB} + L_{AC'} - L_{BC'}}{2} \tag{4}$$

$$L'_{12} = \frac{L_{AB} - L_{BC'} - L_{AC'}}{2} \tag{5}$$

$$L_{22} = \frac{L_{AB} + L_{BC'} - L_{AC'}}{2}. \tag{6}$$

Ideally, the residual shunt inductance L'_{12} is zero; if the residual is less than zero, there is too much cancellation, and if the residual is greater than zero, too little. However, practical mounting considerations on an impedance analyzer may not accurately reproduce the mounting on a PCB, and thus, the residual inductance measured using an impedance analyzer is most useful to evaluate the *relative* variance between filter elements in the fabrication process, and not strictly as a measure of general filter element performance, as the following insertion-loss measurement is meant to provide.

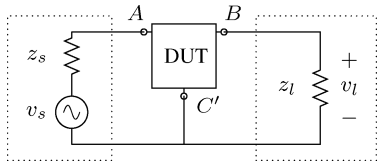

Fig. 14. Measurement setup for two-port insertion-loss measurements. Impedances z_s and z_l are 50 Ω.

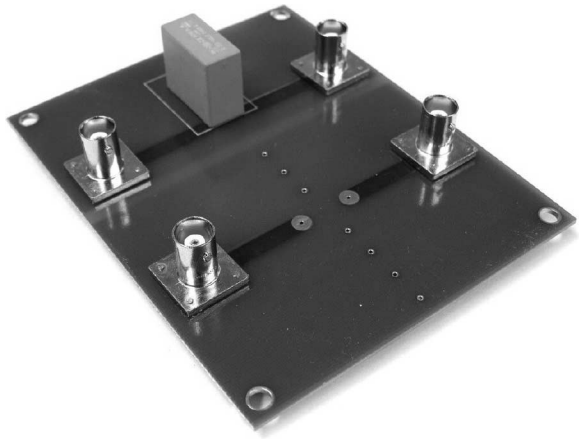

Fig. 15. Photograph of PCB measurement fixture used in the two-port network measurement shown in Fig 14. The mounted capacitor is used for the reference measurement, whereas the near mounting location is for the device under test. Both halves of the PCB contain an independent solid-copper bottom layer that is electrically connected to the shield of their respective Bayonet Neill Concelman (BNC) connectors.

2) Two-Port Insertion-Loss Measurement: Insertion loss is a measurement of the attenuation of a filter, and is a common method for evaluating the performance of EMI filters [20]. In the most simplistic arrangement, the measurement is made with a sinusoidal input source and series impedance driving the input port of the filter, while a load impedance is placed across the output port. The ratio between the magnitude of the source voltage and the output terminal voltage measured across the load impedance is the filter insertion loss, reported in decibels. The insertion-loss measurements are most easily taken using a network analyzer that provides the 50 Ω source and load impedances internally. Fig. 14 illustrates this type of measurement setup. Measurements in this paper are made in accordance with those used to evaluate inductance cancellation performance in [5] and [15] to allow for direct performance comparison. The filter responses presented in [6] are not those of insertion loss unfortunately, and thus, are not directly comparable; proper insertion-loss measurements for these filters appear in [15].

The use of a single PCB measurement fixture (with a bottom-layer ground plane), as shown in Fig. 15, attempts to mimic one of many possible realistic filter element mounting scenarios.

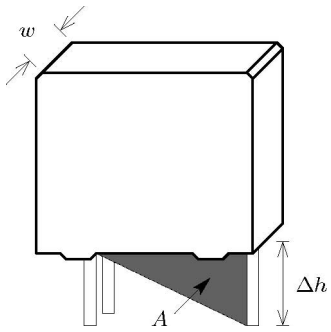

Fig. 16. Effective shunt inductance of an integrated filter element can be increased by lifting the capacitor off the testing fixture to increase loop area.

A more complete testing setup might provide a number of reference circuit test fixtures to evaluate the impact of various usage scenarios. For specific applications or to obtain maximum effectiveness, a manufacturer may chose to provide recommended PCB footprint and layout information for the circuit designer, as is common for many high-performance circuit components.

With the PCB measurement fixture and a three-terminal filter element, the filter performance can be interactively modified by raising and lowering the element with respect to the circuit board, then observing the change in frequency response. When the filter element is raised, the length of terminal C' is increased, thereby increasing the effective shunt inductance of the filter element, shown in Fig 16. The change in inductance can be approximated [3] by

$$\Delta L = \mu_0 \frac{A}{w} \tag{7}$$

where A and w are illustrated in Fig 16. This approximate relationship is valid for $\Delta h \ll w$, which should hold for many common sizes of integrated filter elements, and provide an intuitive tool for fine tuning prototype winding inductances. Once the clearance of a specific filter element design is determined, this would be applied for all fabricated parts.

This method of adjusting the filter element shunt inductance can be used to determine how close the filter element inductance cancellation is to "optimal." While it ideally seems that the optimal output response would occur when the residual shunt inductance is zero, it is often advantageous for a small positive inductance to remain. The proper residual shunt inductance allows the resonant frequency of the filter to be positioned near the highest frequency of interest; the insertion loss is increased near the resonance due to the reactive cancellation in the shunt path.

III. Implementation Examples

Using the design, fabrication, and measurement methods developed in Section II, two separate integrated filter element designs are presented here. The two selected capacitors are representative of capacitors used in many EMI filters. Vishay BCcomponents Series MKP338 capacitors in 330 nF and 1.0 μF, part numbers 2222-338-24334 and 2222-338-24105, respectively, are X2-rated polyester-film capacitors, indicating that they are approved for both line-to-line and line-to-ground configurations. The two capacitors differ primarily in their capacitance ratings and physical package size; Fig. 17 shows a photograph of the two capacitors. The size difference between the capacitors is indicative of their relative ESLs; the 1.0 μF capacitor is larger, and has a larger average inductive loop area and ESL. The capacitance ratings of the capacitors are illustrative of their use: the 1.0 μF capacitor is more likely to be used in filters with a higher current rating than the 330 nF capacitor.

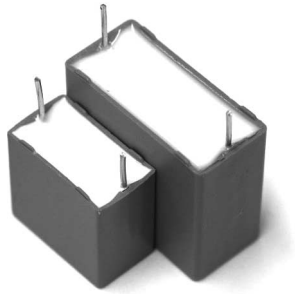

Fig. 17. Photograph of two Vishay BCcomponents Series MKP338 capacitors in 330 nF and 1.0 μF values. Figs. 18 and 22 contain the outer dimensions of each respective capacitor.

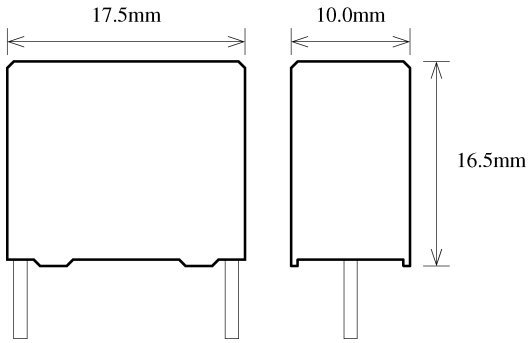

Fig. 18. Dimensioned illustration of Vishay BCcomponents 2222-338-24334 capacitor.

For both capacitors, 20 integrated elements were fabricated to determine the repeatability of the fabrication method. The windings were constructed using the methods described in Section II-A for fabricating multiple windings simultaneously.

In this section, all simulated inductance values are generated using the FastHenry [19] 3-D inductance extraction program. Measured inductance values are taken using an Agilent 4395A in Network/Impedance/Spectrum Analyzer impedance analyzer mode at 30 MHz, the same frequency as the simulations. The Agilent 4395A is also used in network analyzer mode for the two-port network measurements of insertion loss, which provides the 50 Ω source and load impedances.

A. Vishay BCcomponents 2222-338-24334 330 nF

This capacitor outline and dimensions are shown in Fig. 18. The measured ESL is 9.9 nH.

1) Winding Design: The filter winding is designed to carry series current of up to 5 A, with a loss of no more than 0.01% of

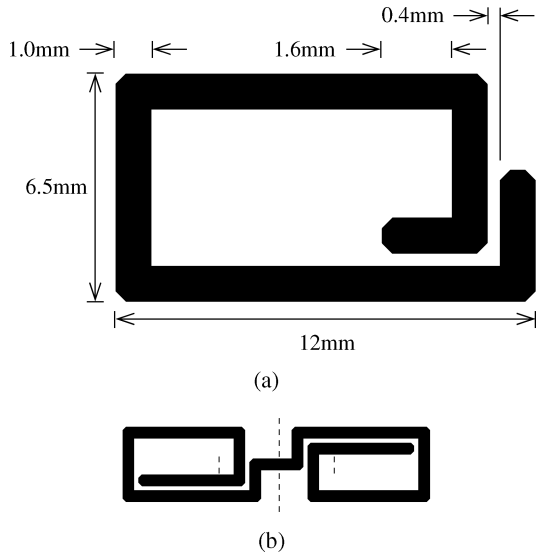

Fig. 19. Inductance cancellation winding design for use with the Vishay BCcomponents 330 nF capacitor. Both the two-layer folded and single-layer unfolded designs are shown. The winding is fabricated from 1-mm-thick copper. (a) Two-layer folded. (b) Single-layer unfolded.

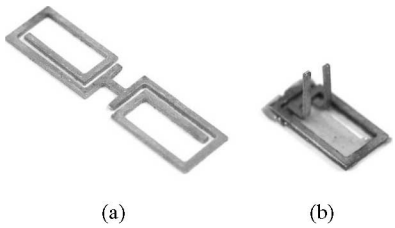

Fig. 20. Inductance cancellation winding photographs of single-layer pattern and final two-layer construction for the 330 nF integrated filter element. (a) Cut pattern. (b) Final assembly.

the power at 240 V. This corresponds to a series path resistance of less than 4.8 mΩ.

The winding inductance is designed to offset the capacitor ESL of 9.9 nH. Using the basic design of the example coil in Fig. 8 as a starting point, the final two-layer coil design shown in Fig. 19 was developed. The single-layer pattern, fabricated from a 1-mm-thick copper sheet using an abrasive-jet cutter, is marked to indicate where the pattern is folded to create the external leads. Fig. 20 shows both the single-layer windings as originally cut and the winding after the structure has been insulated, folded, and joined into its final two-layer form.

Simulation of the winding at 30 MHz results in an inductance matrix

$$L_{\rm sim} = \begin{bmatrix} 14.8 & 11.2 \\ 11.2 & 14.8 \end{bmatrix} \text{nH}$$

and a simulated winding resistance of 2.5 mΩ at 60 Hz. The measured winding inductances at 30 MHz (of one winding selected at random) result in the inductance matrix

$$L_{\rm meas} = \begin{bmatrix} 26.0 & 8.5 \\ 8.5 & 25.1 \end{bmatrix} \text{nH}$$

and a measured winding resistance of 3 mΩ at 60 Hz.

Fig. 21. Photograph of a completed 330 nF integrated filter element with inductance cancellation. The resulting package height is 1.75 mm taller than the original capacitor casing.

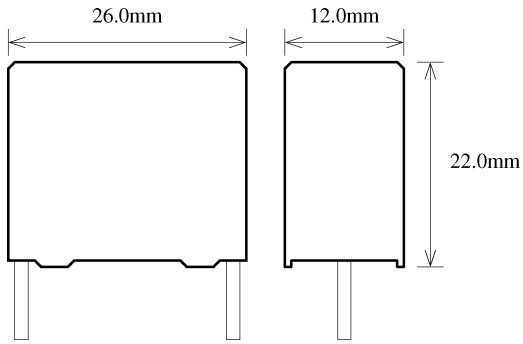

Fig. 22. Dimensioned illustration of Vishay BCcomponents 2222-338-24105 capacitor.

The self-inductance terms in the measured inductance matrix shows a significant departure from the simulation results. This is primarily due to the 6.5 mm interconnect length required to mount the C terminal of the winding on the impedance analyzer fixture, which is not reflected in the simulation results. The simulated and measured mutual inductance values are sufficiently close, however, to justify the use of FastHenry for initial estimation purposes. As always, the designer should takes into account the (consistent) variation between the simulation and real-world results regardless of simulation package.

2) Integration and Encapsulation: The final filter element potting height is experimentally determined by the desired residual shunt inductance, which determines the filtering characteristics of the device. This height is determined experimentally using the two-port insertion-loss measurements method described in Section IV. A randomly selected capacitor and magnetic winding from each batch were paired and used to determine the optimal potting height that resulted in the highest insertion loss; this same height was used for all subsequent elements in the batch. The final fabrication result for the 330 nF integrated filter element is shown in Fig. 21. The three-terminal device is 1.75 mm taller than the original capacitor casing.

The performance of this integrated filter design is investigated in Section IV.

B. Vishay BCcomponents 2222-338-24105 1.0 μF

This capacitor outline and dimensions are shown in Fig. 22. The measured ESL is 13.3 nH.

1) Winding Design: The filter winding is designed to carry a series current of 10 A, with a loss of no more than 0.01% of the power at 240 V. This corresponds to a series path resistance of

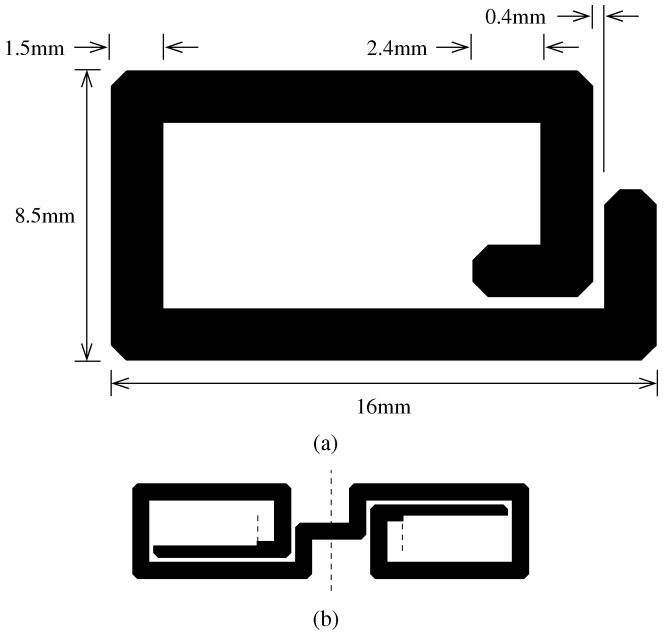

Fig. 23. Inductance cancellation winding design for use with the Vishay BCcomponents 1.0 μF capacitor, shown in both the two-layer folded and single-layer unfolded designs. The winding is fabricated from 1-mm-thick copper. (a) Two-layer folded. (b) Single-layer unfolded.

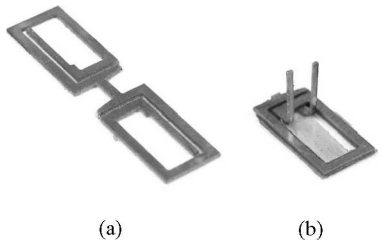

Fig. 24. Inductance cancellation winding photographs of single-layer pattern and final two-layer construction for the 1.0 μF integrated filter element. (a) Cut pattern. (b) Final assembly.

less than 2.4 mΩ. The winding inductance is designed to offset the capacitor ESL of 13.3 nH. Using the basic design of the example coil in Fig. 8 as a starting point, the final two-layer coil design shown in Fig. 23 was developed. The single-layer pattern, fabricated from a 1-mm-thick copper sheet using an abrasive-jet cutter, is marked to indicate where the pattern is folded to create the external leads. Fig. 24(a) shows the single-layer winding as originally cut, and Fig. 24(b) shows the winding after the structure has been insulated and joined into its final two-layer design.

The simulated winding inductances at 30 MHz result in an inductance matrix

$$L_{\rm sim} = \begin{bmatrix} 18.6 & 14.8 \\ 14.8 & 18.6 \end{bmatrix} \text{nH}$$

and a simulated winding resistance of 2.0 mΩ at 60 Hz. The measured winding inductances at 30 MHz (of one winding selected at random) result in the inductance matrix

$$L_{\rm meas} = \begin{bmatrix} 34.0 & 12.7 \\ 12.7 & 32.6 \end{bmatrix} \text{nH}$$

and a measured winding resistance of 2 mΩ at 60 Hz.

Fig. 25. Photograph of a completed 1.0 μF integrated filter element with inductance cancellation. The resulting package height is 1.2 mm taller than the original capacitor casing.

Again, the variation between the simulated and measured self-inductance matrices is primarily due to the 8 mm of interconnect required to connect terminal C of the winding to the impedance analyzer; however, the mutual inductance term L_{12} remains reasonably close for the purposes of initial estimation.

2) Integration and Encapsulation: The final filter element potting height is determined by the methods described in Section IV. A randomly paired capacitor and magnetic winding were used to determine the optimal potting height, providing the best performance in the test fixture; this height was used on all subsequent elements in the batch. The final fabrication result for the 1.0 μF integrated filter element is shown in Fig. 25. The three-terminal device is 1.2 mm taller than the original capacitor casing.

The performance of this integrated filter design is investigated in Section IV.

IV. Fabrication Results

To determine the relative precision of the filter element construction, each batch of 20 filter elements fabricated in Section III was characterized using measurements of the residual shunt inductance and insertion loss, as described in Section II-C.

The residual shunt inductance of each filter was found by applying (5) to the three two-terminal impedance measurements, then offset by the geometric mean of all 20 filter elements in the batch to provide a zero-centered measurement. Centering the residual inductances around zero eliminates the offset introduced by the component lead lengths and their connection to the impedance analyzer inductance of the measurement apparatus and illustrates the error *relative* to the other elements, not necessarily to a specific target residual shunt inductance. It is the *relative* values that are of interest for this measurement, as they indicate the repeatability of the fabrication process; actual filter performance is best described by the insertion-loss measurements. Histograms of the residual shunt inductance are presented in Figs. 26 and 27 for the 330 nF and 1.0 μF devices, offset by 1.89 and 5.09 nH, respectively. This illustrates a maximum variation of 0.88 and 0.68 nH, with corresponding standard deviations of 0.24 and 0.19 nH, for the 330 nF and 1.0 μF filter element batches, respectively. Additionally, it may be useful to consider this data in a normalized form, scaled by the magnitude of the initial capacitor ESLs to allow a comparison between designs. This results in maximum part-to-part

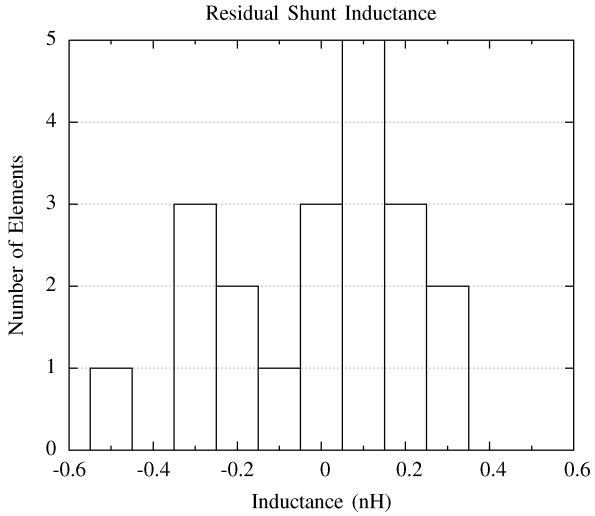

Fig. 26. Zero-centered histogram of measured residual shunt inductance values of twenty 330 nF integrated filter elements.

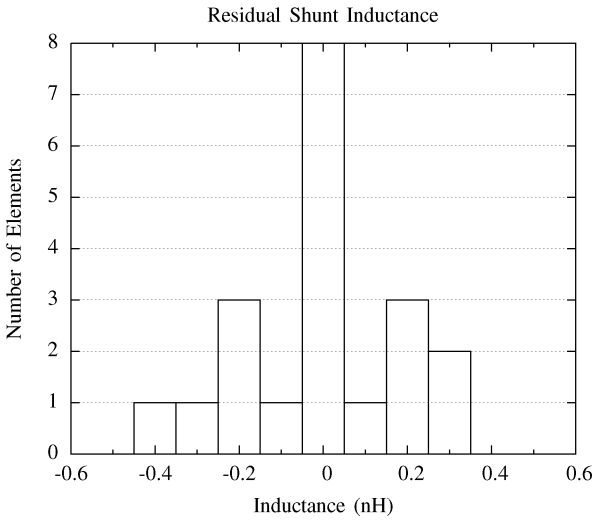

Fig. 27. Zero-centered histogram of measured residual shunt inductance values of twenty 1.0 μF integrated filter elements.

variation measurement of 8% and 5%, and standard deviations of 2.4% and 1.9% for the 330 nF and 1.0 μF filter elements, respectively.

To asses the attainable filtering performance for the integrated filter elements, the two-port insertion-loss measurements were taken for each device. Fig. 28 plots the frequency response of each element, grouped by design, along with the unmodified capacitor responses. Both integrated filter element designs show a significant improvement in performance over their capacitor-only equivalents, gaining more insertion loss at the higher frequencies where the ESL would normally dominate. At 30 MHz, the upper bound of the conducted EMI specification [2], the 330 nF and 1.0 μF filter elements, both show a minimum improvement of 20 dB. An interesting result in both filter element responses is the unveiling of the resonance located in the low- to mid-frequency range of the figures. This small resonance results from the distributed nature of the capacitor [21], and is normally insignificant relative to the dominating interconnect inductance.

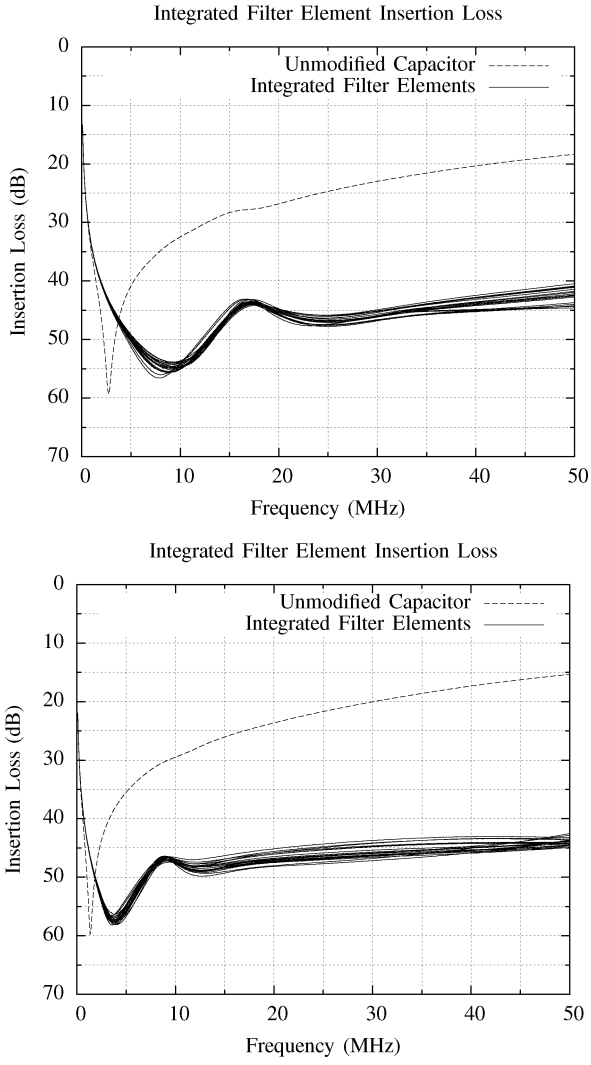

Fig. 28. Insertion-loss measurements for twenty 330 nF (top) and 1.0 μF (bottom) integrated filter elements.

A plot of the difference between the largest and smallest insertion-loss values for both filter designs is given in Fig. 29, illustrating the maximum variation between filter elements. The maximum variation across the frequency range is 4.1 dB for the 330 nF device and 3.5 dB for the 1.0 μF one. This variation can be considered acceptable, especially given the greater than 20 dB minimum improvement in insertion loss obtained at high frequencies. Additionally, the insertion-loss measurements of the 330 nF integrated filter elements can be compared directly with the results presented in [15] for the 330 nF capacitor with inductance cancellation implemented using PCB windings. The use of PCB windings for inductance cancellation appears to offer only a slight decrease in the maximum insertion-loss variation when compared to the *hand-fabricated* integrated filter elements presented here.

V. Conclusion

This paper has presented an implementation of inductance cancellation where the coupled magnetic winding is copackaged

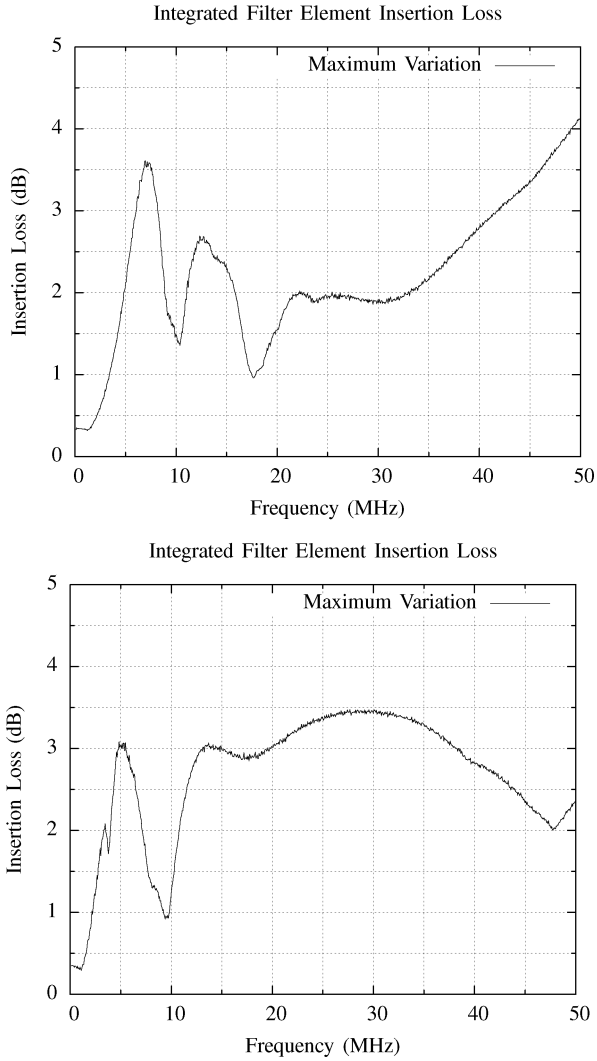

Fig. 29. Maximum variation of insertion-loss measurements for twenty 330 nF (top) and 1.0 μF (bottom) integrated filter elements.

with the capacitor to form a self-contained integrated filter element. A design methodology and fabrication procedure were presented, and the integrated filter elements constructed using this fabrication method have been shown to have substantial performance improvements over standard capacitors with a low part-to-part variation.

The resulting filter element characteristics and performance measurements validate the feasibility of fabricating devices with repeatable performance results using low-cost construction methods. Additional gains in device repeatability can be expected with a refined process and/or mechanized fabrication and assembly. The approach presented here offers a compelling combination of substantial performance improvements, repeatability, and ease of manufacture.

REFERENCES

[1] T. K. Phelps and W. S. Tate, "Optimizing passive input filter design," in *Proc. 6th Nat. Solid-State Power Convers. Conf.*, May 1979, pp. G1-1–G1-10.

[2] H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd ed. New York: Wiley, 1988.

[3] C. R. Sullivan and A. M. Kern, "Capacitors with fast current switching require distributed models," in *Proc. IEEE Power Electron. Spec. Conf.*, Vancouver, BC, Jun. 2001, vol. 3, pp. 1497–1503.

[4] T. Uchida, T. Y. Katsuyuki, K. Sugitani, and K. Masami, "LC filter with capacitor electrode plate not interfering with flux of two coils," U.S. Patent 6 476 689, Nov. 5, 2002.

[5] T. C. Neugebauer, J. W. Phinney, and D. J. Perreault, "Filters and components with inductance cancellation," *IEEE Trans. Ind. Appl.*, vol. 40, no. 2, pp. 483–491, Mar./Apr. 2004.

[6] T. C. Neugebauer and D. J. Perreault, "Filters with inductance cancellation using printed circuit board transformers," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 591–602, May 2004.

[7] D. J. Perreault, J. W. Phinney, and T. C. Neugebauer, "Filter having parastic inductance cancellation," U.S. Patent 6 937 115, Aug. 30, 2005.

[8] S. Wang, F. C. Lee, D. Y. Chen, and W. G. Odendaal, "Effects of parasitic parameters on EMI filter performance," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 869–877, May 2004.

[9] S. Wang, F. C. Lee, and W. G. Odendaal, "Using a network method to reduce the parasitic parameters of capacitors," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2004, vol. 1, pp. 304–308.

[10] S. Wang, F. C. Lee, W. G. Odendaal, and J. D. van Wyk, "Improvement of EMI filter performance with parasitic coupling cancellation," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1221–1228, Sep. 2005.

[11] T. C. Neugebauer and D. J. Perreault, "Parasitic capacitance cancellation in filter inductors," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2004, vol. 4, pp. 3102–3107.

[12] R. Chen, J. D. van Wyk, S. Wang, and W. G. Odendaal, "Improving the characteristics of integrated EMI filters by embedded conductive layers," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 611–619, May 2005.

[13] S. Wang, R. Chen, J. D. Van Wyk, F. C. Lee, and W. G. Odendaal, "Developing parasitic cancellation technologies to improve EMI filter performance for switching mode power supplies," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 4, pp. 921–929, Nov. 2005.

[14] B. J. Pierquet, T. C. Neugebauer, and D. J. Perreault, "Inductance compensation of multiple capacitors with application to common- and differential-mode filters," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1815–1824, Nov. 2006.

[15] T. C. Neugebauer, "Advanced filters and components for power applications," Ph.D. dissertation, Massachusetts Inst. Technol., Cambridge, Jun. 2004.

[16] F. W. Grover, *Inductance Calculations: Working Formula and Tables*. New York: Dover, 1946.

[17] C. M. Zierhofer and E. S. Hochmair, "Geometric approach for coupling enhancement of magnetically coupled coils," *IEEE Trans. Biomed. Eng.*, vol. 43, no. 7, pp. 708–714, Jul. 1996.

[18] W. G. Hurley and M. C. Duffy, "Calculation of self and mutual impedances in planar magnetic structures," *IEEE Trans. Magn.*, vol. 31, no. 4, pp. 2416–2422, Jul. 1995.

[19] A. Kamon, L. Silveira, C. Smithhisler, and J. White, *FastHenry USER'S GUIDE*, 3rd ed. Cambridge, MA: MIT Research Laboratory of Electronics, Nov. 1996.

[20] *CORCOM Product Guide Catalog 1654000*, Tyco Electron., Libertyville, IL, Mar. 2004.

[21] C. R. Sullivan and Y. Sun, "Physically-based distributed models for multilayer ceramic capacitors," *2003 Elect. Perform. Electron. Packaging*, pp. 185–188, Oct. 2003.

Brandon J. Pierquet (S'03) received the B.S. degree in electrical engineering from the University of Wisconsin, Madison, in 2004 and the S. M. degree from the Massachusetts Institute of Technology (MIT), Cambridge, in 2006.

He is currently a Doctoral Candidate in the Laboratory for Electromagnetic and Electronic Systems at MIT. His current research interests include the design and control of high-efficiency grid-connected power converters.

Timothy C. Neugebauer (M'04) received the B.S. degree in electrical engineering from Union College, Schenectady, NY, in 1997, and the M.S. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, in 1999 and 2004, respectively.

He is currently with Draper Laboratories, Cambridge, MA.

David J. Perreault (S'91–M'97–SM'06) received the B.S. degree from Boston University, Boston, MA, in 1989, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, in 1991 and 1997, respectively.

In 1997, he joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate, and became a Research Scientist in the laboratory in 1999. In 2001, he joined the MIT Department of Electrical Engineering and Computer Science, where he is currently a Associate Professor of electrical engineering. His research interests include design, manufacturing, and control techniques for power electronic systems and components, and in their use in a wide range of applications.

Dr. Perreault received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society, an ONR Young Investigator Award, and the SAE Ralph R. Teetor Educational Award, and is coauthor of four IEEE prize papers.