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17.6 An Efficient Piezoelectric Energy-Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor

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Energy harvesting is an emerging technology with applications to handheld, portable and implantable electronics. Harvesting ambient vibration energy through piezoelectric (PE) means is a popular energy harvesting technique that can potentially supply 10 to 100's of µW of available power [1]. One of the limitations of existing PE harvesters is in their interface circuitry. Commonly used full-bridge rectifiers and voltage doublers [2] severely limit the electrical power extractable from a PE harvesting element. Further, the power consumed in the control circuits of these harvesters reduces the amount of usable electrical power. In this paper, a bias-flip rectifier that can improve upon the power extraction capability of existing full-bridge rectifiers by up to 4.2× is presented. An efficient control circuit with embedded DC-DC converters that can share their filter inductor with the bias-flip rectifier thereby reducing the volume and component count of the overall solution is demonstrated.

Figure 17.6.1 shows a conventional full-bridge rectifier circuit together with the implemented bias-flip rectifier circuit. The PE element when excited by sinusoidal vibrations can be modeled as a sinusoidal current source in parallel with a capacitance C_P and resistance R_P [1]. The output capacitor C_{RECT} is large compared to C_P. The main limitation of the full-bridge rectifier is that, *even when ideal diodes are considered*, most of the current available from the harvester does not go into charging the output capacitor C_{RECT} at high values of V_{RECT}. At every half-cycle, when I_P changes direction, current first has to go into the capacitor C_P to charge it up from $-V_{RECT}$ to $+V_{RECT}$, or vice-versa, before it can flow into the output. The shaded portion of the current waveform in Fig. 17.6.1 shows the time spent in charging or discharging C_P every half-cycle. This loss in charge limits the amount of electrical power that can be extracted using the full-bridge rectifier.

The bias-flip rectifier consists of an inductor L_{SHARE} which is connected in parallel with the PE harvester. The switches M_1 and M_2 are turned ON for a brief time when I_P crosses zero in either direction. When the switches are ON, the inductor helps in flipping the voltage V_{BF} across C_P. The series resistance along the L_{SHARE}, C_P resonant path limits the magnitude of this voltage inversion. After the switches open, the PE current I_P needs to supply a smaller amount of charge to C_P to bring it up to $\pm V_{RECT}$. This significantly improves the power extractable from the harvester. The output power that can be obtained with the bias-flip rectifier is dependent on the PE harvester being used and can be given by,

$$P_{RECT} \approx 2C_P V_{RECT} f_P (2V_P - V_{RECT}(1 - e^{-\pi/2Q_L} + \pi/Q_P)) \quad (1)$$

where $V_P = I_P/\omega_P C_P$, $Q_P = \omega_P C_P R_P$ and Q_L is the Q-factor of the L_{SHARE}, C_P resonant network. Eq. (1) shows that there is an optimal value of V_{RECT} for maximal power transfer. A non-linear assessment of using an inductor to improve the power output of PE harvesters in a macro scale is given in [3]. A further advantage of the bias-flip rectifier scheme is that it pushes the optimal voltage for power extraction to be higher than that obtained using only a full-bridge rectifier, thereby reducing the effect of the losses which occur when diode non-idealities are introduced. In systems where it is prohibitive to use an inductor to improve power output, a switch-only rectifier scheme where L_{SHARE}, M_1 and M_2 are replaced by a single switch, can give up to 2× improvement in the extracted power.

Figure 17.6.2 shows the architecture of the bias-flip rectifier system. The output voltage of the rectifier V_{RECT} needs to be regulated at its optimum point for maximal power transfer. A buck DC-DC converter is used to regulate V_{RECT} and efficiently pass on the energy obtained to a storage capacitor C_{STO} or a rechargeable battery. A boost DC-DC converter is used to generate a high volt-age V_{HIGH} (~5V) which is used to power the switches of the bias-flip rectifier. Both the buck and boost DC-DC converters employ an inductor-based architecture for improved efficiency. The arbiter block is used to control access to the inductor L_{SHARE}, which is shared between the bias-flip rectifier, buck and boost DC-DC converters.

Figure 17.6.3 shows the control circuitry that determines the timing control of the switches M_1 and M_2 in the bias-flip rectifier. The switches need to be turned ON when I_P crosses zero. The zero-crossing in I_P is detected by comparing (depending on the direction of current) either V_{HAR_P} or V_{HAR_N} with a reference voltage V_{DIODE_REF}. When they go high, a request to access L_{SHARE} is sent to the inductor arbiter through the REQ_RECT signal. The arbiter grants access through the ACK_RECT signal which triggers a pulse generator whose width can be controlled by the signal $DELAY<0:7>$. The delay is adjusted to achieve zero-current switching of the inductor current. The switched capacitor circuit shown in the bottom of Fig. 17.6.3 allows the transistors M_1 and M_2 to have a gate-overdrive of V_{HIGH} when they are ON irrespective of the value of V_{RECT}.

Figure 17.6.4 shows the buck DC-DC converter that is used to regulate V_{RECT} and transfer the energy obtained to C_{STO}. The converter is a synchronous rectifier buck regulator and employs a pulse frequency modulation (PFM) mode of control [4] which enables inductor sharing. The buck converter is designed to regulate V_{RECT} from 2V to 5V with 4 bits of precision ($V_{REF}<0:3>$). When V_{RECT} goes above the reference voltage, a REQ_BUCK signal is sent to the arbiter to request access to the shared inductor. Once the arbiter grants access through the ACK_BUCK signal, the Pulse Width Control block turns the PMOS and NMOS power transistors ON sequentially with suitable pulse widths to achieve approximate zero-current switching [4]. The boost converter is designed similar to the buck converter and generates a 5V output voltage to drive the switches of the bias-flip rectifier. Figure 17.6.4 shows the measured efficiency of the buck converter with change in V_{RECT} when the rectifier provides a 20µA current input into C_{RECT}. The inductor sharing leads to a compact system with only a small drop (2 to 3%) in efficiency.

Figure 17.6.5 shows oscilloscope waveforms of the output voltage of the PE harvester and Fig. 17.6.6 shows the measured power obtained at the output of the rectifier for the different rectifier scenarios measured with off-chip diodes. The switch-only rectifier improves upon the extractable power by 1.9× compared to the conventional full-bridge rectifier. The effectiveness of the bias-flip rectifier improves as the inductance is increased. This increases the Q of the resonant network (Q_L), thereby improving the bias-flip magnitude and hence the extracted power. An 820µH inductor provides a 4.2× improvement in power extracted. When on-chip diodes are used, the improvement in power extracted increases as expected to above 7×. On connecting the rectifier to the buck DC-DC converter and using a 47µH inductor, a total output power of 32.5µW is obtained at the output of the buck converter, which takes into account, the loss in the buck and boost regulators and the power consumed by the control circuitry.

Figure 17.6.7 shows the die micrograph of the test chip fabricated in a 0.35µm CMOS process. The active area of the PE harvester interface circuitry together with the DC-DC converters is 4.25mm².

References:
[1] S. Roundy, P. K. Wright and J. Rabaey, *Energy Scavenging for Wireless Sensor Networks with Special Focus on Vibrations*, Kluwer Academic Press, 2003.
[2] T. T. Le, et al., "Piezoelectric Micro-Power Generation Interface Circuits," *IEEE J. Solid-State Circuits,* pp. 1411-1420, June 2006.
[3] D. Guyomar, et al., "Toward Energy Harvesting Using Active Materials and Conversion Improvement by Nonlinear Processing," *IEEE Trans. Ultrasonics, Ferroelectrics, and Frequency Control,* pp. 584-595, Apr. 2005.
[4] Y. K. Ramadass and A. P. Chandrakasan, "Minimum Energy Tracking Loop with Embedded DC-DC Converter Delivering Voltages down to 250mV in 65nm CMOS," *ISSCC Dig. Tech. Papers,* pp. 64-65, Feb. 2007.
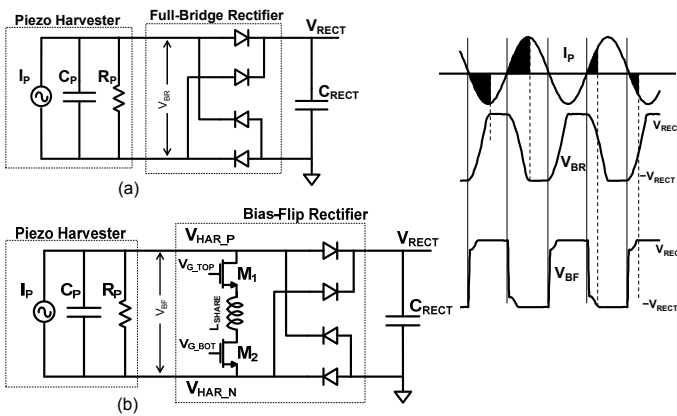
Figure 17.6.1: (a) Conventional full-bridge rectifier, (b) Bias-flip rectifier. The right-hand side shows simulated input current and voltage waveforms for the different scenarios. The shaded portions of the current waveform depict the amount of charge not delivered to the output capacitor C_{RECT}.
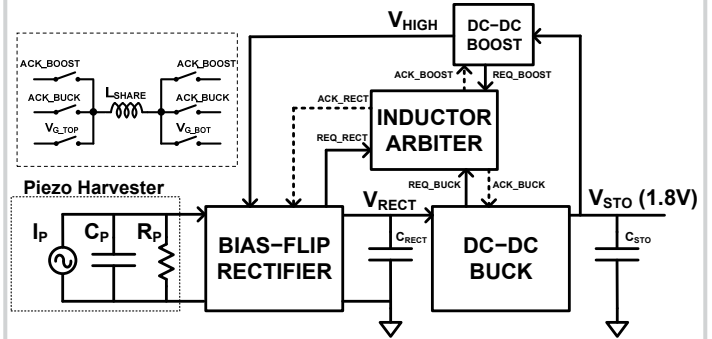

Figure 17.6.2: Architecture of the bias-flip rectifier system. The inductor arbiter controls access to the shared inductor L_{SHARE}.
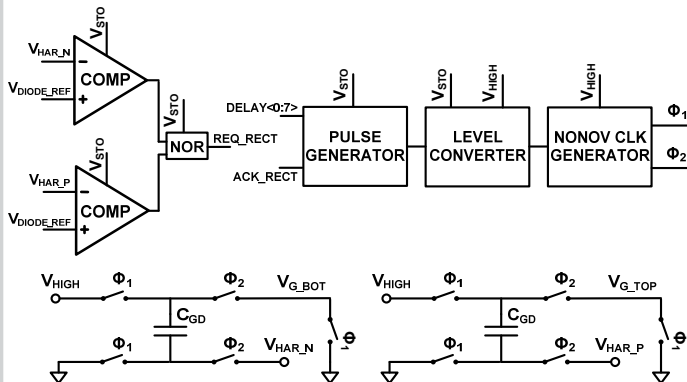

Figure 17.6.3: Control circuit for timing and gate-overdrive control of the bias-flip rectifier. The ACK_RECT signal triggers the Φ_2 pulse which makes V_{G_TOP} and V_{G_BOT} go high, thereby turning on the transistors M_1 and M_2 of the bias-flip rectifier.
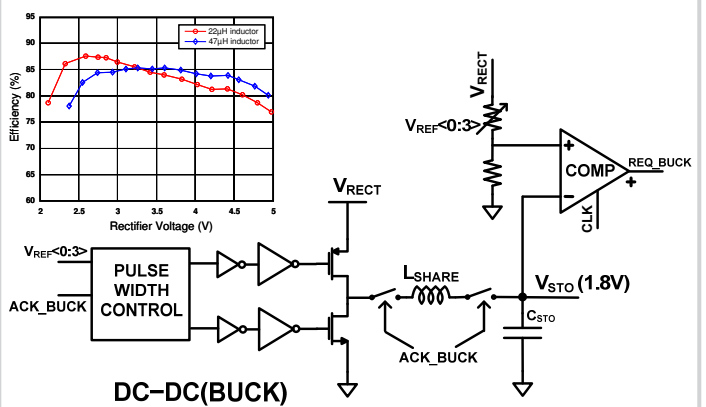

Figure 17.6.4: Architecture of the buck DC-DC converter for regulating V_{RECT}. The measured efficiency of the buck regulator with change in the rectifier voltage (V_{RECT}), when a current of 20μA is fed into V_{RECT}, is shown for two different values of L_{SHARE}.
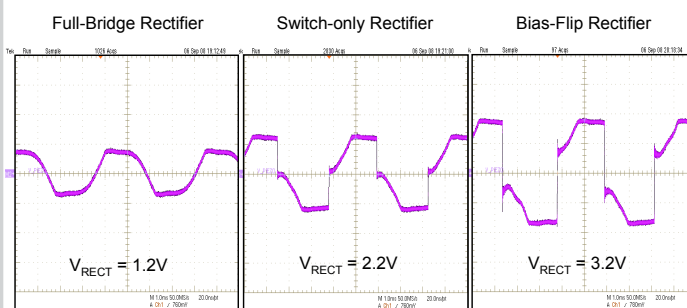

Figure 17.6.5: Oscilloscope waveforms of the output voltage of the piezoelectric harvester for a) full-bridge rectifier, b) switch-only rectifier, and c) bias-flip rectifier.
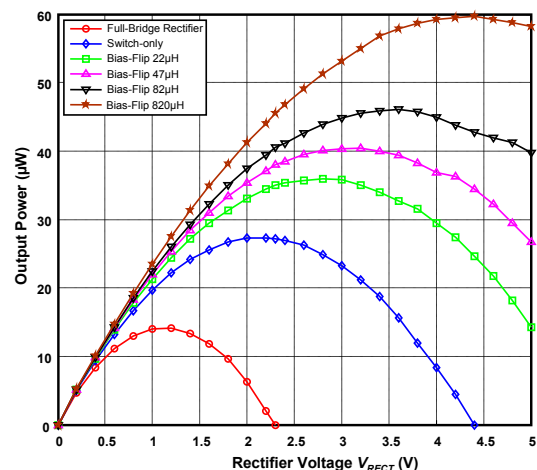

Figure 17.6.6: Measured electrical power output by the piezoelectric energy harvester with off-chip diodes. The optimal value of V_{RECT} for maximal power transfer increases with the switch-only and bias-flip rectifier schemes. Measurements with on-chip diodes further increases the improvement in power extracted.
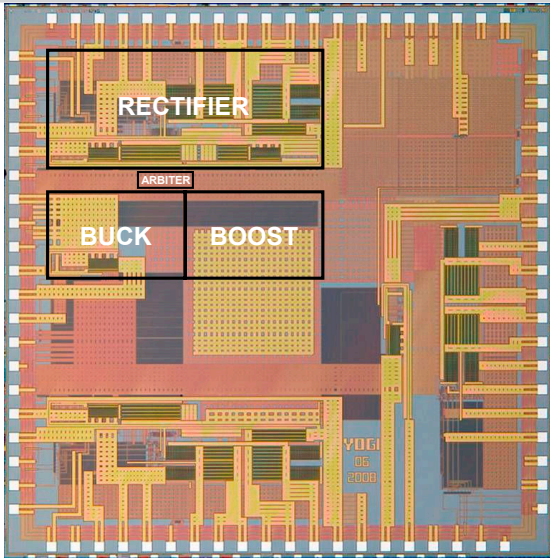
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Figure 17.6.7: Die micrograph of the bias-flip rectifier system.