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A Fractionally Spaced Linear Receive Equalizer with Voltage-to-Time Conversion

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Abstract

Based on voltage-to-time conversion technique, a pseudo-differential two-way-interleaved adaptive linear receive equalizer with two 2x-oversampled feed-forward taps has been designed in a 90 nm CMOS process. It integrates equalization and phase interpolation functions into one unit to simultaneously address inter-symbol-interference (ISI) cancellation and phase synchronization in a link receiver. It operates at 4 Gbps with 8 mW power consumption, and linearity of 4.3 effective bits at 1.2 V supply.

Keywords: fractionally spaced receiver equalizer

Introduction

Intersymbol-interference (ISI) is becoming an increasingly severe issue as target data rates increase in link applications, challenging both the equalization and synchronization sub-systems. Traditionally, adaptation loops in these two sub-systems derive the error information from different performance metrics (voltage errors at data sampling points and error information at edge crossings). This discrepancy results in sub-optimal link performance due to the interaction of the two loops, especially in situations where received signals are significantly asymmetrical and distorted by ISI [1,2] (e.g. loop-unrolled decision-feedback equalizers).

Fractionally spaced equalizers enable controlled ISI reduction at arbitrary sampling phase with a single adaptation loop [3]. In this paper we describe an implementation of a two 2x oversampled feed-forward taps receiver equalizer structure. Apart from oversampling speed challenges, implementation of linear receiver equalizers has been a difficult problem due to process mismatch and speed-power-nonlinearity trade-offs in current-mode implementations in scaled, low-supply voltage CMOS processes [4].

Architecture

To overcome these issues with good energy-efficiency, and achieve 4~5 bit linearity required by the adaptive algorithm the FSE design is based on voltage-to-time and time-to-voltage conversion techniques [5]. Due to the process speed limitation, half-rate time interleaving technique is also applied, Fig. 1. Four sampling phases (Φ_1- Φ_4) with 25% duty cycle are generated locally from Φ and $\Phi\_$ and another pair of quadrature clocks. A voltage-to-time (V2T) block converts the sampled signal into a delayed digital signal, transferring the sampled information into time-domain. All four V2T converters are followed by a time-to-voltage (T2V) stage to realize summing, subtraction and multiplication.

Equalizer tap weights are implemented as two programmable reference currents I_1, I_2 biasing T2V blocks. Two slicers with tunable thresholds are added to sense the signs of the input signal and output error of the FSE, respectively, and enable tap weight adaptation with external adaptive engine.

Implementation

A. V2T Converter

The V2T converter is shown in Fig. 2. When clock $\Phi\_$ is low, nodes V_S+/V_S- are pre-charged to VDD. Simultaneously, the sampling capacitors C_S+/C_S- track the input signals. The following edge of $\Phi\_$ pulls the sampled voltages on nodes V_X+/V_X- down by the same amount so that they are lower than the threshold voltage at the initial state. Afterwards, two identical currents $I_{charge}+/-$ charge V_X+/V_X- respectively. The nodes V_X+/V_X- will reach the threshold of N+/- at different times and trigger two pairs of edges ($E_{1r}+/-$ and $E_{1f}+/-$). To shorten the decision time, P+/P- provide positive feedback, improving the design speed by roughly 30%, for target time dynamic range. The timing Δt between $E_{1r}+/E_{1f}+$ and $E_{1r}-/E_{1f}-$ is proportional to the differential input V_{in1}.

B. T2V Converter

The T2V converter operation is shown in Fig. 3, with waveforms for $I_2=0$ for simplicity. When $\Phi\_$ is low, output nodes V_O+/V_O- are pre-charged to VDD. After the rising edge of $\Phi\_$, nodes V_O+/V_O- are discharged with current I_1 since E_1f+/E_1f- are high and E_1r+/E_1r- are low. After the arrival of E_1f+/E_1r+ edges, the discharge current by M_1+ switches from V_o+ to V_o-. Therefore, the discharge current of V_O+ becomes zero and that of V_O- is doubled. Thus, the difference between V_O+ and V_O- increases from zero till the arrival of E1f-/E1r- edges. Afterwards, the current by M_1- is rerouted to V_o+ and the discharge currents for both are I_1 again, and $V_o+/-$ decrease with the same slope until the falling edge of $\Phi\_$. The voltage output ΔV_O is proportional to $V_{diff,in1}xI_1$ and $V_{diff,in2}xI_2$, implementing the multiplication and summing operations. Changing the sign multiplexer control will realize a subtraction. T2V integrator has significantly improved linearity over the traditional GmC stage since its inputs are always full swing signals.

Measurements

The design is fabricated in a 90 nm CMOS process. The chip layout is shown in Fig. 4, with additional support blocks like scan chain and high-speed data snapshots to enable link tuning and in-situ performance characterization. The FSE receiver area is 65 μm x 130 μm.

At 4 Gbps rate, tuning the tap weights guarantees a flat open eye within +/-5% for any delay between data and clock, compared to the eyes visible by symbol-spaced slicers, Fig. 5b. Due to larger than predicted parasitic capacitance at the V_X node in the V2T converter, the design exhibits about 2x attenuation at V_O with respect to the input signal, Fig. 5a, but achieves target linearity of 4.3 effective bits with monotonic gain in tap weights, Fig. 6.

Conclusion

Leveraging the speed of advanced digital processes, a voltage-to-time conversion techniques provide an effective way to overcome the linearity issues in high-speed link receive filters and enable the implementation of fractionally-spaced filters that simultaneously address the phase synchronization and equalization tasks with good energy-efficiency.

References

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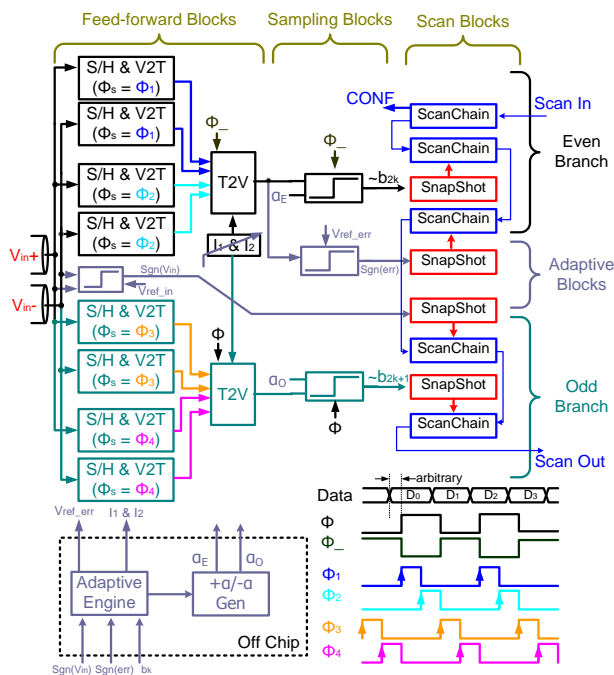
Fig. 1 Block diagram of 2-tap 2xoversampled two-way time interleaved architecture. Scan-chain and snapshot are applied for *in-situ* link characterization.
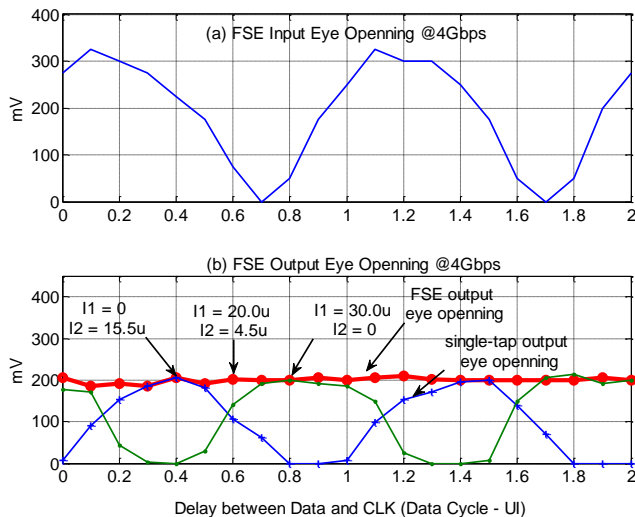

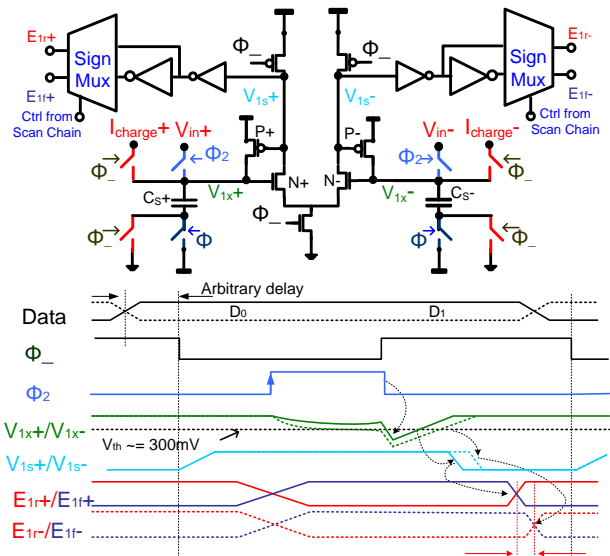Fig. 5 Input (a), and FSE output (b) eye opening vs. sampling phase.

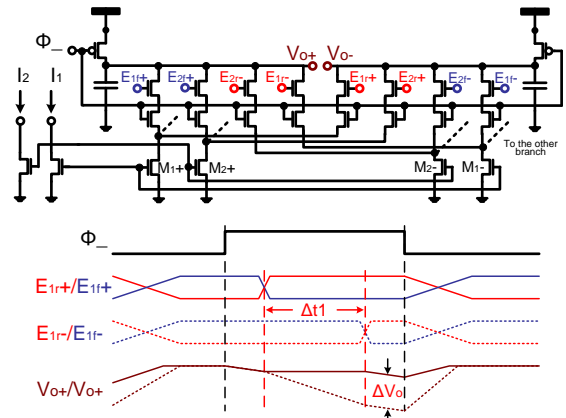Fig. 2 Schematic and time diagram of V2T converter

Fig. 3 Schematic and time diagram of T2V converter when $I_1 > 0$ and $I_2 = 0$. M_1+, M_1-, M_2+ and M_2- are shared by even/odd branches.
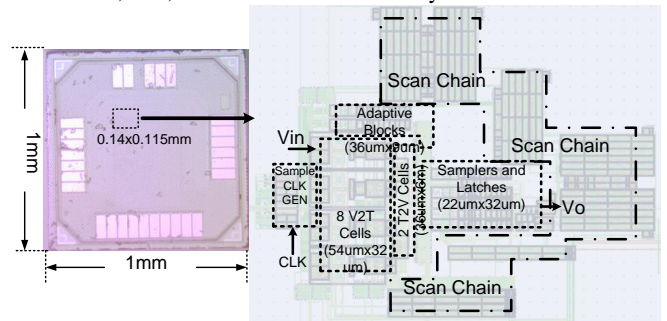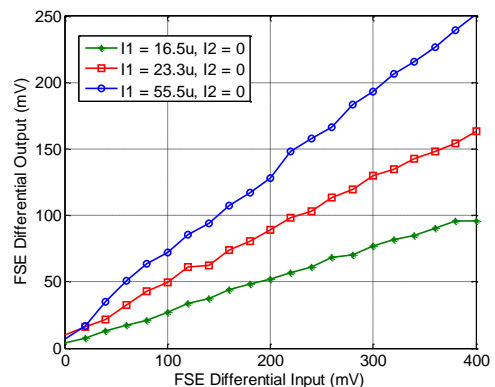

Fig. 4 Die photo and chip floor plan.

Fig. 6 Linearity of the FSE for different tap weights.