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**Citation:** Chung, SungWon and Joel L. Dawson. "A 73.1dB SNDR Digitally Assisted Sub-sampler for RF Power Amplifier Linearization Systems." 6th International Symposium on VLSI Technology, Systems and Applications (2009 VLSI-TSA), 27-29, April 2009, Hsinchu, Taiwan. © 2009 VLSI-TSA.

**As Published:** <http://vlsitsa.itri.org.tw/2009/General/>

**Publisher:** VLSI-TSA

**Persistent URL:** <http://hdl.handle.net/1721.1/60412>

**Version:** Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

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# A 73.1dB SNDR Digitally Assisted Sub-sampler for RF Power Amplifier Linearization Systems

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## Abstract

We present a digitally assisted subsampler, designed to serve as the downconversion path in adaptive predistorters for 800MHz–5.8GHz RF power amplifiers. We use digital averaging to overcome the noise folding problems of subsampling, obtaining a final SNDR of 73.1dB for signals centered about a 2.4GHz carrier. Using quadrature subsampling, we obtain both the I and Q samples from the same physical path and thereby eliminate IQ gain mismatch. When used as part of an adaptive predistortion system, the subsampler enables an EVM improvement of 3.2% and distortion products suppression of up to 7.6dB for 802.11g signals. The subsampler IC, designed in a 90nm CMOS process, consumes 6.0mW from a 1.2V supply.

## Introduction

Subsampling is recognized as an energy-efficient signal processing technique for highly digital transceivers [1]–[3]. However, subsamplers are notorious for low SNR performance due to noise folding, and for stringent requirements for anti-aliasing prefilters. This combination of faults has largely undermined their use in high performance receivers. In transmitters, however, the situation is *fundamentally* different. The signal environment has fewer extreme aggressors, such as blockers, and the transmitted data is often known in advance of actual transmission. This last fact enables the use of averaging and other signal processing techniques to overcome the noise folding problem.

In this paper we describe a subsampler IC for an adaptive predistortion system. Fig. 1 shows the architecture of the overall system. A set of training symbols are transmitted, and the PA output is sampled using the subsampler. The digitally processed subsampler output is used to populate the look-up table (LUT). Placing this LUT in the feedback path of  $\Delta\Sigma$  modulators accomplishes the inversion of the PA nonlinearity, as well as the interpolation between LUT entries [4]. In the remaining paragraphs, we describe the details of the subsampler IC, the digital signal processing used to obtain a high SNDR, and present measured results.

## Digitally Assisted Sub-sampler Architecture

Fig. 2 illustrates the architecture and the operation of the subsampler. For linearity, we limit the subsampler input to less than 150mVpp. As a result, SNDR at the subsampled output is limited to 18–24dB (3–4bits) by the large subsampling noise. To significantly reduce the subsampling noise, we apply digital averaging to the ADC output. To reduce IQ mismatch in gain and phase, quadrature subsampling is implemented with a single path. The principle behind quadrature sampling is that I and Q samples can be obtained serially from the same RF signal path if their corresponding sampling instants are offset by a  $T_c/4$ , where  $T_c$  is the period of the RF carrier. For the necessary clock phase generation, a frequency reference at twice the carrier frequency is necessary.

The subsampling operation is performed by charge integration with a transconductance amplifier (TA) whose current output is accumulated onto an integration capacitor  $C_{int}$ . For better linearity, a pseudo-differential topology is chosen for the TA. Cascode transistors are used to minimize corruption in the charge integration by providing higher output impedance. The AC coupling capacitor  $C_c$  helps to suppress the low-frequency artifacts of even-order distortion from both the PA and the TA.

A subsampling downconversion path has one difficulty that a

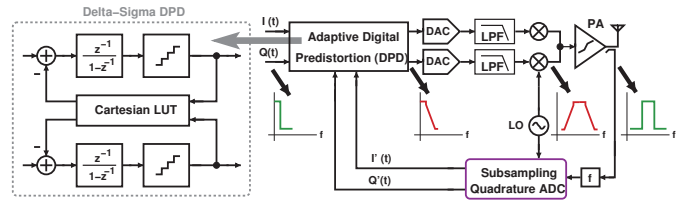


Fig. 1. Adaptive predistortion transmitter architecture with low-power training using RF subsampling. For the prototype, the A/D converter was an EVAL-AD7766-2 test board, all digital signal processing was done in MATLAB, and the D/A conversion was performed by an AFG3102 arbitrary waveform generator.

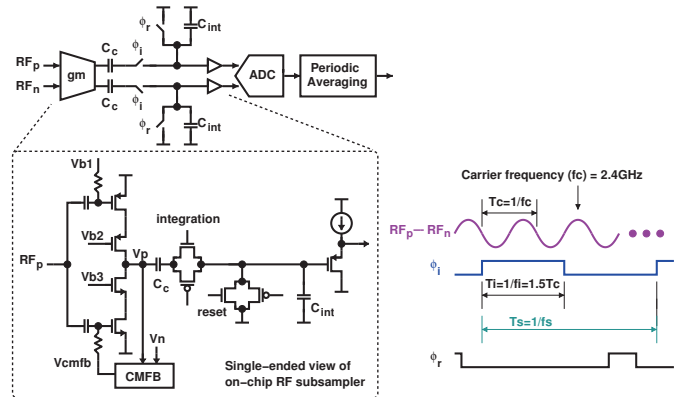


Fig. 2. Digitally assisted subsampler architecture. Quadrature sampling is employed (i.e., Q samples are offset from I samples by  $T_c/4$ ), allowing both the I and Q samples to be obtained from the same physical signal path.

mixer-based approach does not. Even-order nonlinearity in the PA can result in low-frequency products that corrupt the feedback data stream. Baseband digital predistortion cannot compensate for even-order nonlinearity in the PA, so in any predistortion training system it is desirable to reject or ignore these artifacts. A mixer naturally does this by modulating any low-frequency output of the PA back up to the carrier frequency, where it is easily filtered out. In the case of our system, we first modulate the training signals with a 4kHz sinusoid. Then, after subsampling, we process the samples with the averaging operation shown in Fig. 3(a). Samples are collected over a half-period of the 4kHz sinusoid, and samples from many successive half-period windows are averaged to construct a single half-period. This averaging operation requires that, before summation, alternate half-period windows are first inverted. The result is that the random noise is reduced, and even-order distortion products are cancelled out. The distorted I or Q value is then simply the peak value of the resultant half-period.

For our system, four samples are taken for each half-period. With that number of samples, the averaging operation can be viewed as the discrete-time FIR filter shown in Fig. 3(b). The magnitude response of this filter with seven delay elements (representing 8x averaging) is shown in Fig. 3(c).

## Measured Results

Fig. 4 shows the measured noise floor of the subsampler prototype chip, which is sampling at 50MSPS for 4kHz sinusoid training signals modulating a 2.4GHz carrier. Low-frequency spurious tones and a high noise floor limit the SNDR of the subsampler to under 22.9dB, providing an ENOB of 3.5, which is insufficient for most applications, including WLAN systems. With the 16384x averaging

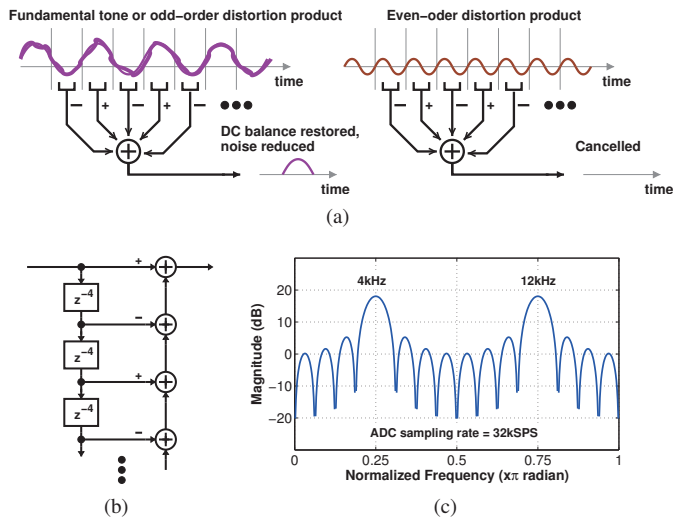


Fig. 3. Digital filtering for subsampling noise reduction: (a) DC filtering and even-order harmonic cancellation (b) FIR filter equivalent representation, and (c) digital-domain frequency response.

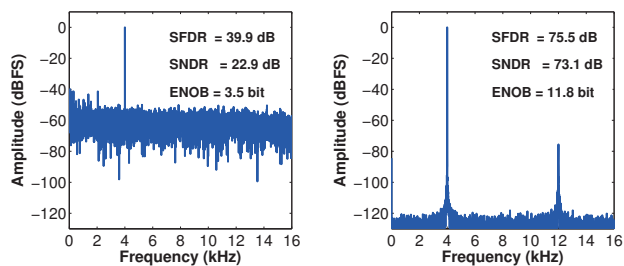


Fig. 4. Measured subsampling noise floor enhancement with a 4kHz sinusoid modulating 2.4GHz carrier: The ENOB is increased from 3.5 to 11.8 after using 16384x averaging.

TABLE I  
PERFORMANCE SUMMARY

Supply voltage	1.2 V
Power dissipation (excluding buffer)	6.0 mW
Sampler input frequency	800MHz – 5.8GHz
Gain (for 2.4GHz carrier)	-14.2 dB
SNDR (w/ 16384x avg., for 2.4GHz carrier)	73.1 dB
SFDR (w/ 16384x avg., for 2.4GHz carrier)	75.5 dB
ENOB (w/ 16384x avg., for 2.4GHz carrier)	11.8 bit
Max. subsampling rate	75 MSPS
Max. input	150 mVpp
Process technology	90nm digital CMOS

applied, the SNDR increases to 73.1dB, providing an ENOB of 11.8.<sup>1</sup> Fig. 5 shows that the subsampler provides an ENOB of higher than 10 with digital averaging for carrier frequencies between 800MHz and 5.8GHz.

Fig. 6 shows the transmitted spectrum with a SiGe SE2528L PA for a WLAN 802.11g/OFDM signal, which has a 6dB peak-to-average power ratio (PAPR). With digital predistortion trained using the subsampler chip, the transmit spectral mask margin is additionally increased by as much as 7.6dB. The measured EVM improves from 7.67% to 4.44%.

Fig. 7 shows the microphotograph of the prototype subsampler chip, which includes on-chip subsampling clock generation circuitry. The active area is 0.12mm<sup>2</sup> and the chip dissipates 6.0mW when subsampling at 50MSPS for 2.4GHz carriers. An on-chip source follower consumes 20mW, and it is used to drive the off-chip, 24bit, 32KSPS, 8.5mW ADC. Table I summarizes the performance of the subsampler chip.

<sup>1</sup>Theory predicts an ENOB improvement of 7 due to 16384x averaging. Our filter's cancellation of even-order distortion products accounts for the additional ENOB boost of 1.3.

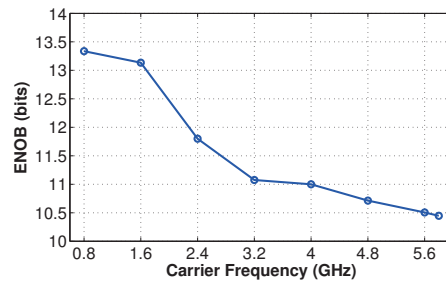


Fig. 5. Measured subsampler ENOB using 16384x averaging with a 4kHz sinusoid modulating carrier frequency between 800MHz and 5.8GHz.

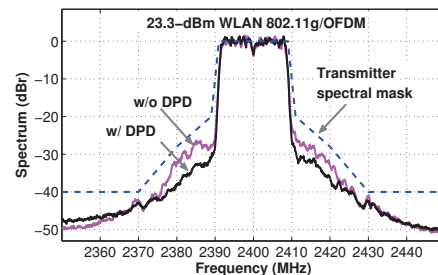


Fig. 6. Measured spectrum of WLAN 802.11g adaptive digital predistortion transmitter whose LUT is trained by the subsampler.

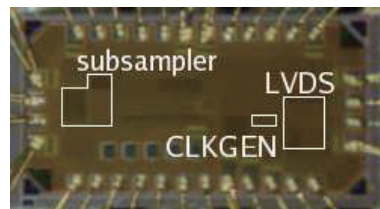


Fig. 7. Prototype chip with the active area of 0.12mm<sup>2</sup>. The die measures 1mm x 2mm.

## Conclusion

A digitally assisted subsampler chip for training adaptive predistortion transmitters is implemented. To reduce the noise folding and attenuate low-frequency spurious tones at the subsampler output, digital averaging is proposed. The digital averaging is equivalent to a multiband FIR filter whose passbands center on the training signals and the resultant odd-order distortion products. Additionally, quadrature sampling is employed to eliminate IQ gain mismatch errors in the feedback path. The subsampler chip provides 73.1dB SNDR for 4kHz training signals with 16384x averaging, which corresponds to an ENOB of 11.8 and is sufficient to train adaptive predistortion transmitters for most standards such as 3G and WLAN.

## Acknowledgment

This work was funded in part by the FCRP Focus Center for Circuit & System Solutions (C2S2).

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