LOW TEMPERATURE TRANSIENT LIQUID PHASE BONDING FOR ELECTRONIC PACKAGING

by

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Submitted to the Department of Materials Science and Engineering on May 8, 1992
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ABSTRACT

Electronic packages are increasingly limited by the ability to extract heat from the components. By optimizing solder interconnections, specifically 52wt.%In-48wt.% Sn Low Temperature Transient Liquid Phase (LTTLP) bonds between the chip carrier and the component, the temperature differential can be reduced so that the residual stress is decreased.

Bond strength is analyzed to ascertain why certain materials systems perform better than others as characterized by measuring remelt temperatures of the bond. Motorola, Inc. requirements of manufacturing are evaluated for the Au/In-Sn/Cu system with solder temperature (ST) at 180°C, a bondline thickness of 25μm, and heat treatment temperature (HT) of 145°C to form an LTTLP bond. At HT times (t) of 0.5-13 hours, remelt temperatures (RT) hover around 120°C. An alternative solution is to increase thermal strength through eliminating Au from the system to produce a Cu/In-Sn/Cu bond. The Cu/In-Sn/Cu system using a ST at 180°C, HT at 145°C exhibits RT >470°C, which is about four times the RT of the Au/In-Sn/Cu system. Composition profiles and scanning electron micrographs show Cu/In-Sn/Cu samples consisting of two Cu-rich phases which exhibit RT >470°C as opposed to Au/In-Sn/Cu samples which contain an In-rich phase and exhibit RT at 120°C. The bond formed in the LTTLP process is achieved at a time of 2.25 hours. Moreover, chemical activity profiles show that Au lowers the activity of In and Sn and inhibits diffusion, thus causing long bonding times and low remelt temperatures. In the Au/In-Sn/Cu system, In and Sn preferentially diffuse to the Au interface due to a strong decrease in chemical activity.

Thermal cycling has been used to understand the mechanical strength of the interconnection. Mechanical strength of the Cu/In-Sn/Cu system did not decrease significantly after 2500 cycles.

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1. INTRODUCTION

With the advent of today's demanding, product driven electronics market, semiconductor industries are focusing on meeting market needs through advanced microelectronic products. These products must be able to integrate multifunctionality into very miniaturized structures as well as increase component reliability in long term performance. This production of increasingly complex advanced microelectronics is made possible by the emergence of innovative high technology manufacturing processes. Therefore, the concern for manufacturing feasibility with respect to the requirements of volumetric product yield at cost-effective rates and quality performance is constantly being refined. The drive to increase the lifetime of semiconductor components in electronic products, especially in computers, are addressed by 1) maintaining process control during operations along the assembly line, 2) utilizing material selection, and 3) optimizing process parameters.

Maintaining process control during operations is characterized by the efficiency of equipment, such as automation by on-line computers. Ideally, to prolong the lifetime of computers, they should operate in environments that are tightly maintained and controlled. Realistically, potentially harmful outside influences, such as temperature variances, humidity, and contaminants, affect the lifetime of the computer through deterioration of its semiconductor components. For many applications, the quality of environmental ranges from business office environments (BOE) to extremely harsh, low technology processing environments [1]. These environmental concerns emphasize the importance of protecting semiconductor components through proper materials selection within the assembly that are less susceptible to deterioration over time. However, no material available satisfies all requirements for all applications. A compromise is usually made between required properties and available materials [3].

Another continuing issue of electronic packaging is to extend the specifications of high power semiconductor components through the optimization of process parameters. There is an ensuing need to compatibly produce components that handle very high power consumption while also allowing adequate heat dissipation during operations.

A packaging limitation to these types of components occur because of the mismatch in the thermal properties of materials. This mismatch in thermal properties can be characterized by the Coefficient of Thermal Expansion (CTE). The stress caused by different CTE of materials during attachment must be addressed for reliable operation [2] over time. Solder bonds provide excellent heat dissipation. At the point of heating the solder for the bond attachment, all components and interfaces involved respond thermally at different rates. Each material involved in bonding contracts at a different rate while the bond solidifies. The difference in thermal expansion and contraction of various materials causes a buildup of residual stress, contributing to component interconnection failure after a number of thermal cycles. Thus, minimization of CTE mismatch (the differential in CTE), component, size, or use of low temperature bonding processes to reduce thermal stresses "enhances the reliability of the attachment process" [3].

Innovative bond attachment processes have evolved as a result of the drive to make high power rating/high heat dissipation assemblies. Radical attachment processes are being used to alleviate the stress factors caused by CTE mismatch between chip and heatsink assembly.

New cost-effective attachment (joining) processes that maintain most of the advantages of existing processes while also addressing manufacturing issues have evolved. These processes are revolutionary in that the joining process occurs at low temperatures. "The ideal process would be to attach a component at low temperature thereby minimizing the level of entrained stress, but would withstand higher temperatures to allow higher level of assembly [3] or permit high temperature operations which may be

necessary for other components attachment. Low Temperature Transient Liquid Phase (LTTLP) bonding has the possibility of meeting all the requirements of an "ideal process".

LTTLP is a spinoff of the TLP bonding process. TLP joints are formed when a melting point depressant in the interlayer diffuses into the surrounding bulk and isothermal solidification results [4] before cooling the bond. The bond will not remelt until heated at a much higher temperature. LTTLP bonding, the main process between chip carrier and component attachment in this thesis, occurs at a much lower temperature. [LTTLP differs from TLP bonding] in that it is the dissolution of the base metal into the joining alloy which causes isothermal solidification of the joint [3]. The low temperature range involved lies in LTTLP bonding between 60°C-160°C.

Other current chip bonding technologies are Au-Sn eutectic bonding and epoxy bonding. Au-Sn eutectic is favorable because of its high heat dissipation capability. However, its high processing temperature contributes to a high buildup of residual stresses. Moreover, although epoxy bonding exhibits low heat dissipation capability, it is advantageous because of its ability to be processed at low bonding temperatures and to exhibit low residual stress. LTTLP bonding is the only technology among these attachment processes that has all the desired characteristics.

Thus, LTTLP bonding is compatible with the prior packaging operations and results in a joint possessing high strength and low residual stresses combined with excellent heat dissipation (see Table 1).

Table 1: Comparing Processing Parameters of Three Current Bonding Technologies

Chip Bonding Technologies	Au-Sn Eutectic	Epoxy	LTTLP
Heat dissipation capability	<u>high</u>	low	<u>high</u>
Processing temperature	high	<u>low</u>	<u>low</u>
Residual stresses	high	<u>low</u>	<u>low</u>

**underline represents desired feature.

Note: Only LTTLP bonding has all the desired characteristics.

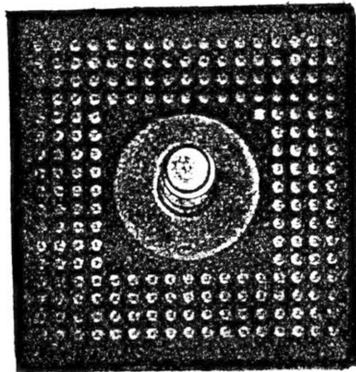
2.2 MIT PROPOSED WORK WITH MOTOROLA

2.21 Satisfying Motorola's Manufacturing Requirements

Electronic packages are increasingly limited by the ability to extract heat from their semiconductor components. Motorola, Inc. is interested in developing higher power rating packaging assemblies capable of dissipating heat as efficiently as possible. A possible assembly is comprised of three parts: 1) device and die (ie.chip and chip carrier) (see figure 2), 2) components (heatsink or source), and 3) substrate (ie. board).

The focus of this thesis with Motorola, Inc., is to understand the chip carrier to component attachment (see figure 1) by studying the electroplated metal interlayer on the carrier to the copper heatsink using 52%-48% In-Sn solder paste. This thesis addresses the development of relevant process parameters using LTTLP bond attachment technique to satisfy Motorola's manufacturing requirements. Although no one material can satisfy all the requirements, proper materials selection is important for optimizing the strength of attachments by alleviating residual stress and increasing time until bond failure.

Specifically, LTTLP bonding is implemented to reduce bonding times and to accomplish processing at low heat treatment temperatures (HT<165°C). Motorola has specified HT at 145°C and a remelt temperature of RT>215°C. This RT allows subsequent attachments to the package without affecting the chip carrier to heatsink attachment. 25μm is the desired bonding thickness . Bonding time to achieve these parameters needs to be configured and reduced to as short a time as possible. The chip carrier dimensions are specified as 0.8"x0.8"x.06" (2.03cm x 2.03cm x 0.15cm). The copper heatsink is specified as .25"x.25"x.03" (0.64cm x 0.64cm x 0.08cm). The LTTLP bond attachments are required to withstand 2500 cycles of thermal cycling under commercial specifications from 0°C to 70°C.



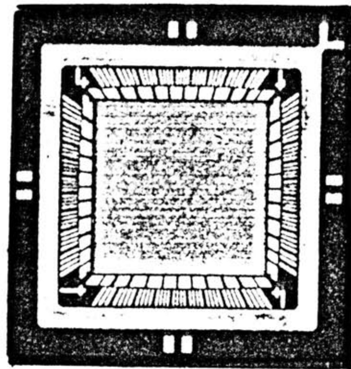


Figure 1: (top) Motorola, Inc.'s Controlled Collapse Flip Chip carrier with component attachment.

Figure 2: (bottom) Motorola, Inc.'s carrier for chip attachment.

2.22 Development: Process Parameters (see Table 2)

By using 52%-48% In-Sn solder interconnections, LTTLP bonds can be made between chip carrier and component, and the differential between the bonding temperature and room temperature can be reduced so that residual stress is minimized. Thermal strength is characterized by the its minimization of residual stress. Parameters that affect thermal strength are the following:

1. Materials system: Different solders affect the rate of heat dissipation; different base materials affect the differential CTE, and thus low heat dissipation and high differential CTE increases the amount of residual stress.
2. Solder mass: The amount of solder determines the rate of solder flow and LTTLP bonding time. Too much solder causes bonding times to be too long. Higher temperatures are then needed to melt solders at short bonding times, causing an increase in the residual stress.
3. Soldering temperature: High soldering temperatures cause buildup of residual stress.
4. Heat treatment temperatures: Low processing temperatures decrease the amount of heat buildup and thus minimizes residual stresses.
5. Remelt temperatures: Low remelt temperatures characterize a bond that will fail by creep at low temperatures.

Table 2: Process Parameters for 52%-48%In-Sn LTTLP Bond Attachment

MOTOROLA'S PROPOSAL

Parameters	
1. Materials Selection	Au/In-Sn/Cu Chip Carrier: 100μm" electroplated Au 0.8"x0.8"x0.06" Alumina Ceramic Component: Cu spacer 0.25:x0.25"x0.032" Solder Paste: 52-48%In-Sn, RMA-F flux
2. Cleaning Preparation	Acetone
3. Bond Mass	
4. Solder Temperature	136°C(liquidus)
5. Flux	RMA-F Type
6. Fixturing	P=1lbs./.25 sq.in.=16psi
7. HT Temperature	T=145°C
8. Bondline Thickness	Th=.001"=.25μm
9. Remelt Temperature	RT>215°C
10. Composition Profile	See attached graphs
11. Thermal Cycling	2500 cycles, 0° C to 70°C commercial specifications

3. THEORETICAL BACKGROUND

3.1 OVERVIEW

The topic of this thesis focuses on using LTTLP bonding as an attachment process to satisfy Motorola's requirements (see section 2) between their controlled collapse flip chip carrier and a copper heatsink (spacer). The concept of LTTLP bonding can be derived from that of TLP bonding. "The term LTTLP is chosen to reflect a more general definition of the term TLP to mean the process where an intermediate liquid layer is formed but then solidifies at or near the joining temperature. Therefore, the dissolution of base metals into the joining alloy causes the isothermal solidification of the joint. TLP, on the other hand, has a more specified definition meaning the process where isothermal solidification takes place when one or more constituents of liquid interlayer diffuse into the base metal."[3]

Although LTTLP is a more general case of TLP, much work has been accomplished on TLP bonding so that some of its high temperature characteristics can be used to describe LTTLP bonding at lower temperatures. Generally speaking, LTTLP bonding is a process in which isothermal solidification occurs at less than 160°C.

3.2 TRANSIENT LIQUID PHASE (TLP) BONDING

TLP has been defined by MacDonald and Eagar [4], who have described its stages, its advantages, and disadvantages.

A TLP bond is formed when a melting point depressant (MPD) in the interlayer diffuses into the surrounding bulk material and results in isothermal solidification. Thus, it is solid state diffusion that is the driving force for the interlayer to come to solidification.[4]

The TLP process has been divided into four stages by Tuah-Poku et al[5]: 1) dissolution, 2) bond widening, 3) isothermal solidification, and 4) homogenization (see figure 3). Step three is the most significant stage in TLP bonding as it is dependent on the width of the liquid interlayer and rate of [MPD] diffusion into the bulk. This step requires

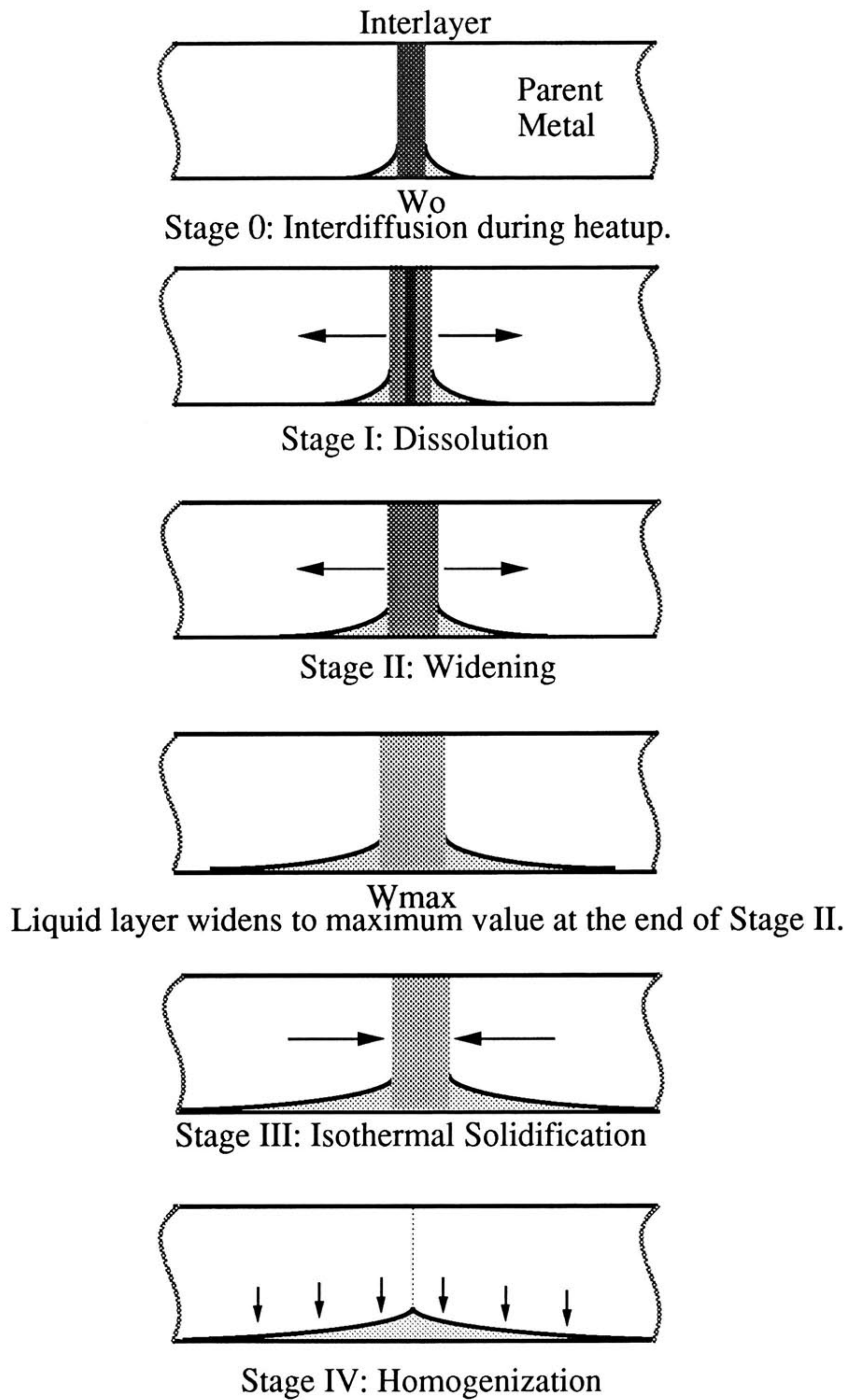


Figure 3: Schematic of TLP/LTTLP Bonding [4]

the longest time. An interesting characteristic of this stage is the existence of a temperature that leads to a minimum solidification time (see figure 3).

TLP allows many large complex shapes to be bonded in one operation rather than several smaller bonds. The advantages of the TLP bonding process are the following: 1) base metal properties at the joint, 2) no interface remains after bonding, 3) low joint pressure required, and 4) minimum surface preparation. However, the disadvantages are 1) long bonding times (hours) and 2) its restriction to processing at high temperatures.

3.3 Low Temperature Transient Liquid Phase Bonding

LTTLP bonding differs from TLP in that it is the dissolution of the base metal into the joining alloy which causes isothermal solidification of the joint. If such bond attachments can be reasonably produced in the 60°C to 160°C temperature range, semiconductor components can be bonded at temperatures near their operating temperatures, resulting in much lower residual stresses. [3]

Roman [3] states that the design of the experiment is important in producing an adequate LTTLP bond. Fixturing should be used to produce a thin uniform bondline. Initially, an excess of solder alloy should be used to produce a joint which is well wetted and void free. Then the bond is fixtured with a light pressure to expel the excess solder and produce a bondline of a minimum thickness. This procedure controls the dissolution of the base metal by limiting the amount of solder alloy in the bondline and also minimizes the distance for diffusion and /or metallic growth to occur across the bondline.[3]

Furthermore, cleaning procedures such as mechanical agitation, aid in wetting the component and chip carrier surfaces and thus shorten bonding times. Also, if no precaution is made to prevent the liquid from leaking out of the joint, then the mass balance is altered, which may significantly reduce the bonding time.[3]

Thus, LTTLP bonding is being investigated for industrial applications because it has the advantages of relatively short bonding times and low processing temperatures

whereas TLP bonding may require very long bonding times (many hours) and high processing temperatures. Moreover, thermal strength testing is characterized by the remelt temperature. The LTTLP bond has been shown to be four times stronger as the solder bond before the LTTLP heat treatments. This allows LTTLP bonds to provide excellent electronic package component attachments.

3.4 RELIABILITY OF BONDS

In order for an interconnection in an electronic package to function properly and exhibit long-term reliability, it should be designed to operate as close to ambient temperatures as possible. Higher temperatures of operation will magnify the thermal stresses and will normally result in shorter lifetime of the bond in the package. The main problem is not heat dissipation within the material but rather the temperature difference between the dissimilar materials. Large differentials result in excessive stress eventually causing the interconnection to fail. Thus, thermal management invariably involves management of stress in the assembly.[6]

3.41 Thermal and Stress Management

Thermally induced mechanical stresses in electronic interconnections result primarily from the difference in CTE of the different materials involved. There are two ways to reduce thermally induced stress during packaging assembly: Stress reduction by CTE matching of material surfaces and stress reduction by decreasing the temperature differential created during the process. For Motorola's Inc. particular application, LTTLP minimizes the stresses by reducing the temperature differential used in the process to approximately 100°C.

3.42 Thermal Cycling

Thermal cycling is used to test the long term reliability of the interconnection in terms of the mechanical strength of the bond. Because electronic packages are exposed to wide ranges of environmental conditions, bond attachments need to be tolerant to variations in environmental conditions. Whether such extremes as the environment of an office or the harsh environment of a factory, the attachment must perform reliably over long periods of time. Thermal cycling testing is used to understand how environmental influences like temperature variances, humidity, and contaminants, affect the lifetime of the bond interconnection.

4. EXPERIMENTAL DESIGN

4.1 OVERVIEW

LTTLP bonding uses conventional soldering techniques at low temperatures. Materials selection is important in attaining the desired bond properties. Samples are prepared by fixturing and heat treating for various times and temperatures to form LTTLP bonds (see also section 3.3). The temperature at which the bond detaches is determined by finding its remelt temperature. Microscope analysis is performed to determine bondline thicknesses and bond structure. The microprobe is used to determine compositional profiles and elemental distributions over bond thicknesses. By measuring the shear stress of the bond before and after thermal cycling, the change in mechanical strength over time (rate of degradation) is used to determine the reliability of the interconnection. All procedures are performed at ambient temperature and laboratory environments.

4.2 SYSTEM DEVELOPMENT: ESTABLISHING PROCESSING PARAMETERS

4.21 Materials System

For Motorola, Inc.'s flip chip carrier, Au/In-Sn/Cu was chosen as the initially proposed system. In this thesis, the Cu /In-Sn/Cu system is proposed as an alternative to Motorla, Inc.'s Au/In-Sn/Cu system. LTTLP bonding investigations are performed using both systems of 100μm" (2.54μm) Au electroplated on metallized alumina ceramic and 250μ" (6.35μm) Cu electroplated on metallized alumina ceramic. Both systems are then attached to Cu spacers by LTTLP bonding (see Figure 4a and4b). The Au or Cu electroplated ceramic has the dimensions of 0.8"x0.8"x0.06" (2.03cm x 2.03cm x .15cm). The Cu spacer dimensions are 0.25"x0.25"x.032" (.64cm x .64cm x .08cm). Specifications of surface area to weight distribution as well as size are chosen by Motorola, Inc. to allow heat dissipation between chip carrier and heatsink.

Figure 4a: Original Thicknesses of Au/In-Sn/Cu samples before heat treatments

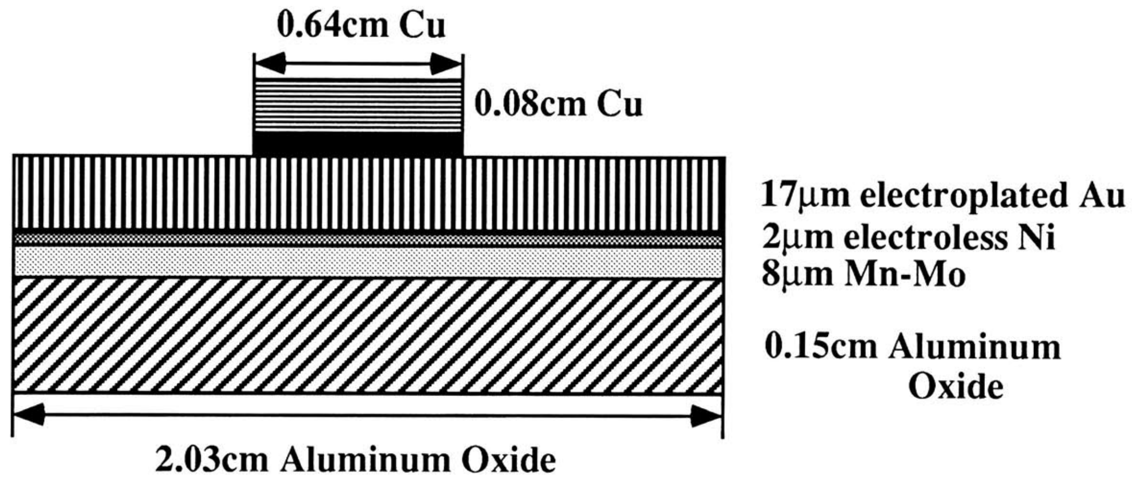
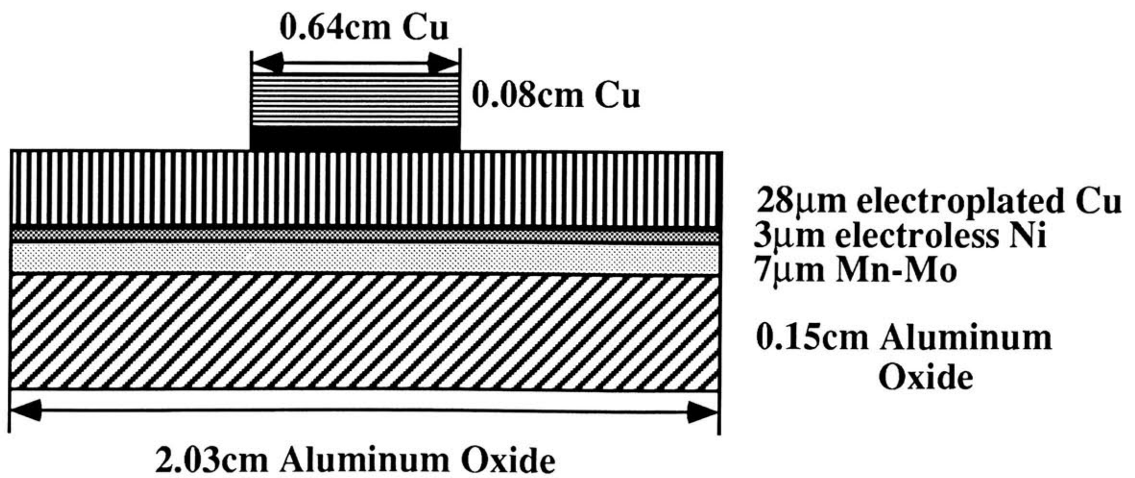


Figure 4b: Actual Original Thicknesses of Cu/In-Sn/Cu samples before heat treatments



Presently Sn-Pb is commonly used as the bonding material . With the recent surge of environmental concerns, use of Sn-Pb has become an issue because of its lead content. 52%In-48%Sn is being investigated for its ability to undergo LTTLP bonding at low temperatures and fast bonding times while maintaining bonding strength many times its original bond strength before heat treatment. Because of its reasonable bonding time and extraordinary remelting temperature, LTTLP bonding using In-Sn solder can become integrated in to manufacturing attachment processes of existing semiconductor components.

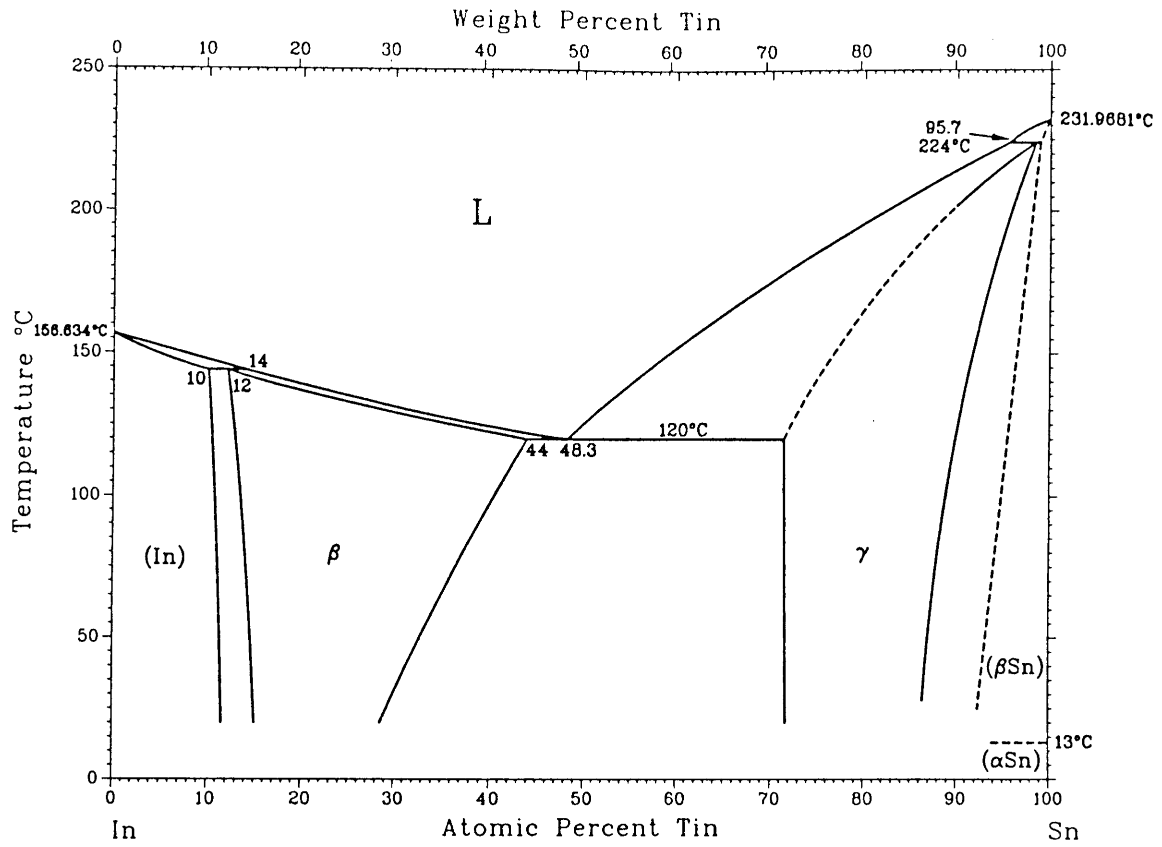
4.22 Materials Preparation

Removing impurities from the sample surface is significant for reducing bonding time and improving bond strength. Sample cleaning by mechanical agitation aids in surface wetting and shortened bonding times. Au/In-Sn/Cu samples were cleaned with acetone; Cu samples are cleaned with a dilute sulfuric acid and nitric acid solution.

Samples were manually soldered using 52%In-48%Sn RMA-F flux in the solder temperature ranges, ST=136°C-150°C (LTTLP range) and ST=180°C-205°C (see figure 5). The lower temperature range is near the In-Sn eutectic, the second range, which allows solder flow within one to three seconds, occurs when In-Sn is in the center of the liquidus phase (see figure 4). Application of solder to the samples works best if the diameter of the solder paste syringe has approximately 0.5cm of paste extruded out of the syringe. Subsequently, solder is heated and melted until it drops to the substrate. The mass of solder used is approximately 0.025g.

Considerations for good solderability requires good wettability. Wettability demands molten solder to wet and flow on samples within a short time period without dewetting. Also, components must be able to be soldered at temperatures required without disturbing other attachments. Therefore, good solderability results in good wetting, which means the formation of a uniform, smooth, unbroken, adherent coat of

In-Sn Phase Diagram



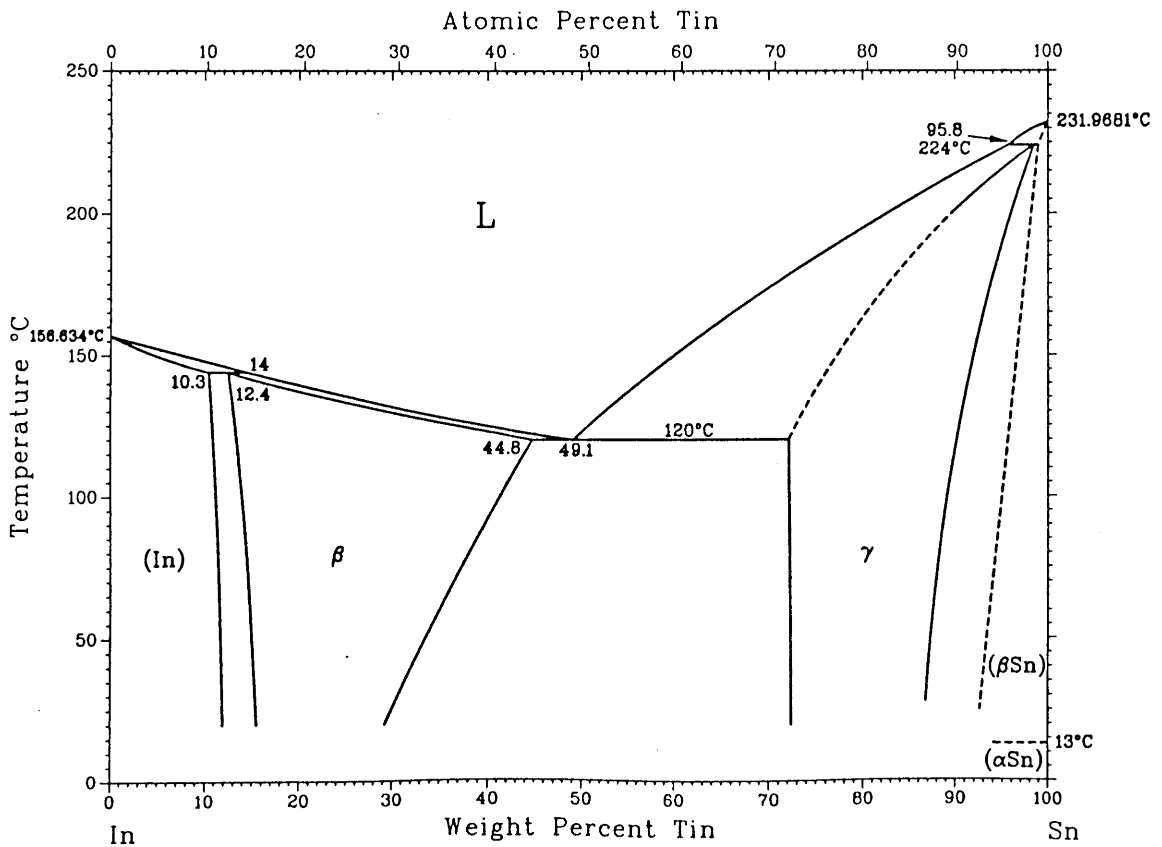


Figure 5: Binary Phase Diagram of In-Sn [8]

solder on the base metal, without the use of highly active flux and without impairing the function of the parts soldered [7]. Thus, good soldering techniques are a prerequisite and affect the success of the entire bonding process. Moreover, since the flux in the solder paste deteriorates over time, proper storage is needed. Therefore, careful methods need to be employed, such as establishing a controlled environment by refrigeration, to delay solder degradation.

In-Sn paste requires refrigeration when not in use. Soldering paste is brought to room temperature before application to avoid condensation residues. Samples were weighed to determine the mass of paste in the bond.

4.23 Heat Treatment

Prior to heat treatments, all samples are fixtured with a 16 psi (1 lb./.25 sq.in.) of pressure to produce a uniform bondline. Thus, the excess of paste during soldering is initially used to produce a joint which is well wetted and void free. These samples are now fixtured to expel excess solder and produce a bondline of approximately 25μm to 40μm thickness.[3]

The Au/In-Sn/Cu was heat treated at HT=145°C at bonding times t=0.5-13 hours to determine the LTTLP bond formation time. The Cu/In-Sn/Cu system and Au/In-Sn/Cu system were then heat treated at HT=145°C, 149°C, 153°C, and 157°C for a solder temperature (ST)=136°C-150°C (near eutectic temperature) and ST=180°C-205°C (liquidus phase). For LTTLP bonding, sufficient heat treatment temperatures and times are needed so that complete dissolution can occur to produce maximum bond width, then isothermal solidification, and finally homogenization so that the bond is directed toward a Cu-rich phase material.

An Omegalux box furnace was used for heat treatments. Heat energy transfer is by natural convection and conduction. Thermocouples are attached to the sample and the outside borders of the samples to gauge the temperature gradients. The furnace is

preheated to the heat treatment temperature before heat treatment starts. Also, temperatures must settle to the designated temperature before bond time consideration begins.

4.24 Temperature Testing (Remelt Test)

Temperature testing is used to determine at what temperature the bond will remelt after it has been heat treated. Remelt temperature is an indication of the thermal strength of the bond and how compatible it is when other components using different materials are soldered and heat treated.

The following is a schematic of the remelt temperature apparatus (see figure 6). The set-up is comprised of a Watlow temperature controller with a programmer, Omegalux chart recorder, and the remelt temperature furnace. The apparatus vertically positions the sample while a 16psi pressure is applied. The furnace heats the specimen from T=0°C to 500°C with the help of the programmer. The Omega RD-103-AR strip chart recorder provides a hard copy of all three thermocouple readings at atmoshphere, furnace, and sample temperatures when the bond remelts.

4.25 Microscopy Analysis

4.251 Metallographic Analysis

Samples are polished up to 0.03μm with aluminain preparation for the scanning electron microscope (SEM) and microprobe analysis. Because of the relative difference of hardness between alumina ceramic, electroplated metal, bond, and Cu metal, polishing is difficult. Quality of polished finish is checked using an optical microscope.

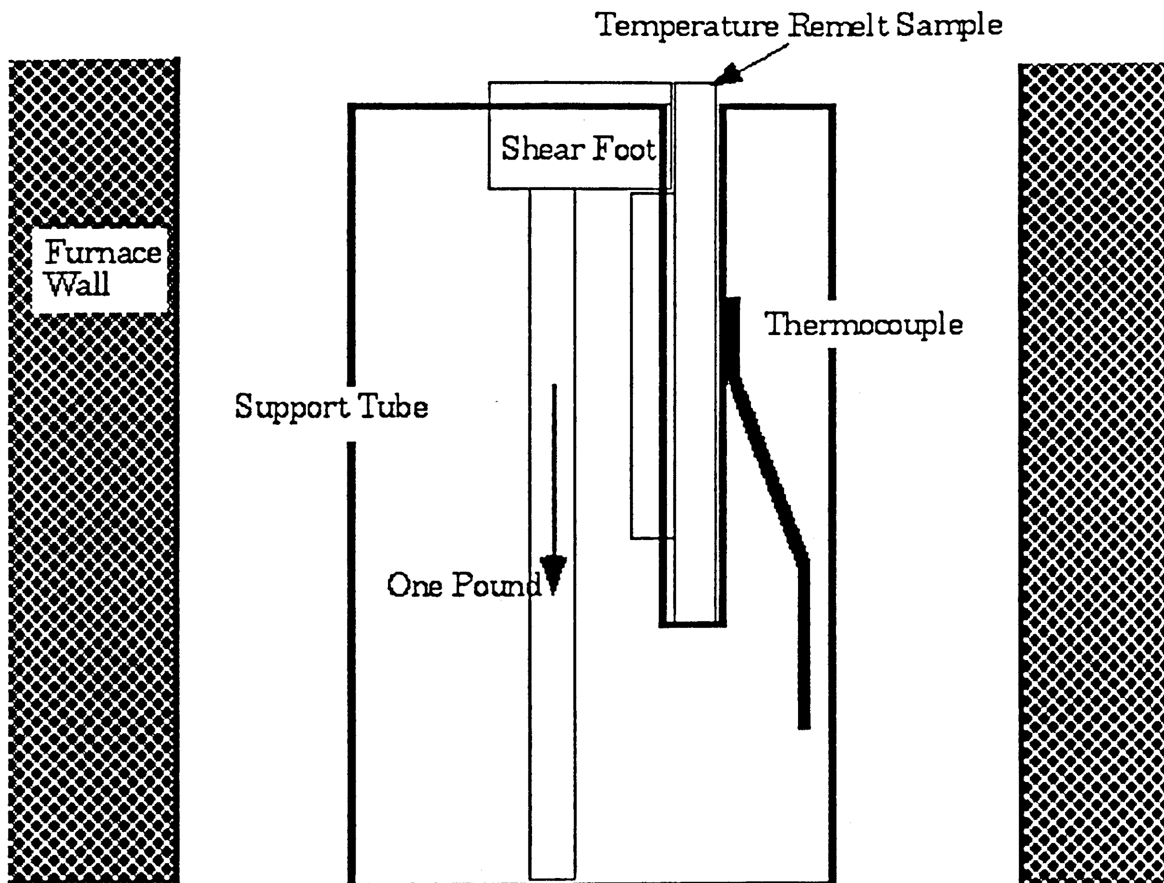


Figure 6: Drawing of the top portion of the remelt temperature test fixture showing shear foot loading the sample. This portion is in the furnace with the loading spring placed externally [3].

4.252 Scanning Electron Microscope (SEM) Analysis

The SEM is used as a tool to gauge bond definition. The microstructure of the bond and thickness of the bond is determined. Micrographs also illustrate the different phases present so that bond quality could be ascertained on a microscale level. The phases presented are also an indication of which stage of LTTLP bonding the sample progresses through completion over time.

4.253 Microprobe Analysis

The microprobe is used to determine the composition profile and elemental distribution with bond thickness for each heat treatment and solder temperature at a given bonding time. In other words, the bond composition across the joint was compared. These trends indicate which constituent is the diffusion limiting species, which constituent phases are present, and the relative amounts of the constituents.

4.26 Macroscale Analysis

4.261 Thermal Cycling

Thermal cycling with the FTS PAC-70-10 model was used to determine how the temperature variances affect the samples. Samples were thermal cycled up to 2500 cycles from 0°C-70°C.

4.262 Shear Testing (see figure 7)

Shear tests were performed to test the mechanical strength of the bond before and after thermal cycling and to indicate bond reliability over time.

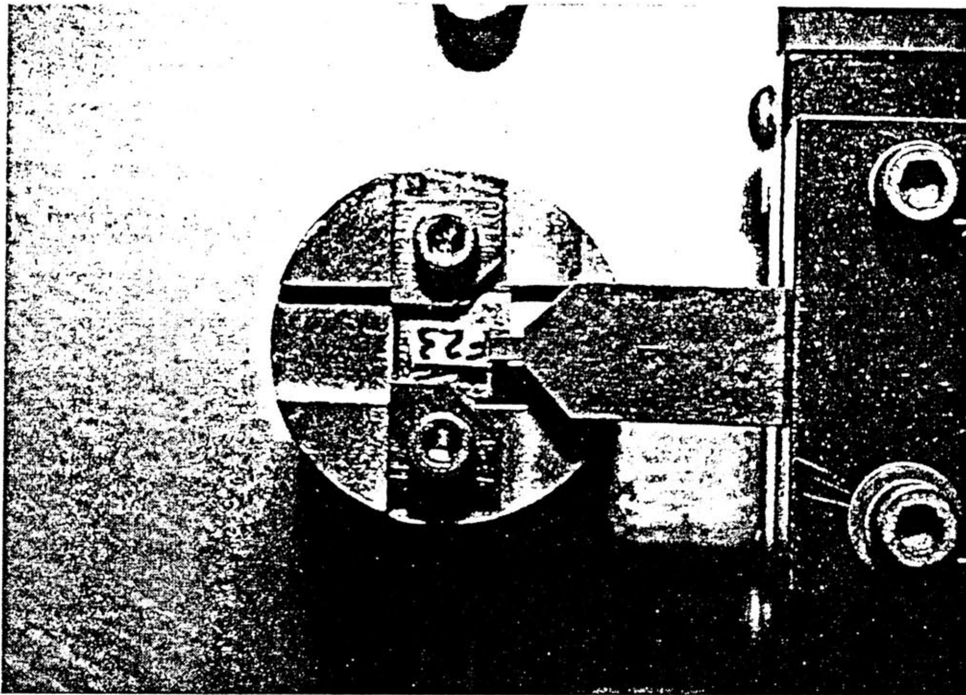


Figure 7: Close-up photograph of a shear sample in the shear test fixture. [3]

5. RESULTS AND DISCUSSION

The Cu/In-Sn/Cu system, which exhibits a remelt temperature of 470°C (HT=145°C) is proposed as an alternative solution to Motorola's Au/In-Sn/Cu system which has a remelt temperature of 120°C after a 2.25 hour heat treatment.

5.1 BOND STRENGTH

Bond strength is primarily controlled by the remelt temperature. For the Au/In-Sn/Cu system, the RT was 120°C. For the Cu/In-Sn/Cu system, the RT was greater than 470°C and the shear strength was greater than 2000psi after a HT of 2.25 hours. There were no significant changes in shear stress after thermal cycling samples up to about 2500 cycles.

A RT of 120°C equates to the eutectic of the In-Sn phase diagram. For the Au/In-Sn/Cu samples during heat treatment, In-Sn did not stay in the liquid stage long enough to go to complete dissolution.

5.2 BOND STRUCTURE

Figure 8 illustrates the Cu/In-Sn/Cu LTTLP bond after completion of the LTTLP bond at HT of 145°C. The black material in the lower portion of the figure is the aluminum oxide substrate. This is followed by a layer of manganese and molybdenum used to metallize the ceramic substrate and a nickel electroless plate. Next, is the plated copper layer followed by the Cu-In-Sn LTTLP bond. The original thickness of the copper plate was 28μm. After the heat treatment, it is approximately 7μm after LTTLP bonding. Finally, the top shows the second copper piece.

Figure 9 shows a similar bond made at 157°C. There are no essential differences between this bond and the bond made at 145°C.

Figures 10 and 11 show similar bonds made in the Au/In-Sn/Cu system. The original gold plate adjacent to the manganese molybdenum had a nickel underplate,

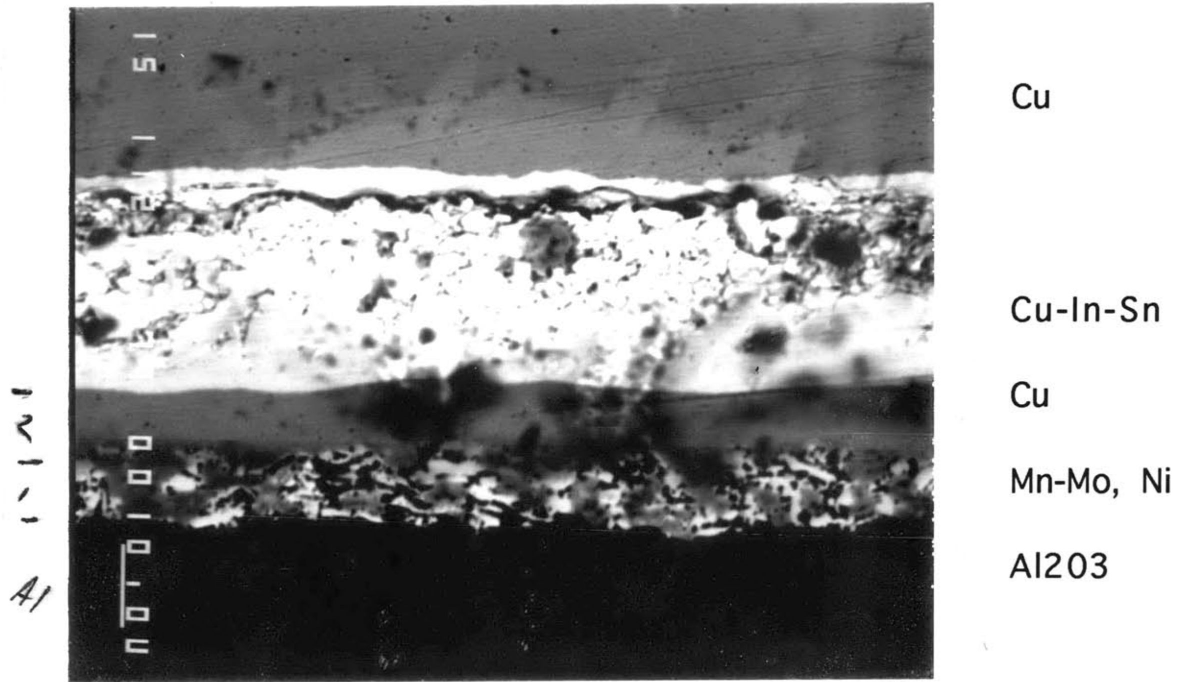


Figure 8: Cu/In-Sn/Cu LTTLP bond,
HT=145°C, ST=180°C, t=2.25hrs., RT>470°C

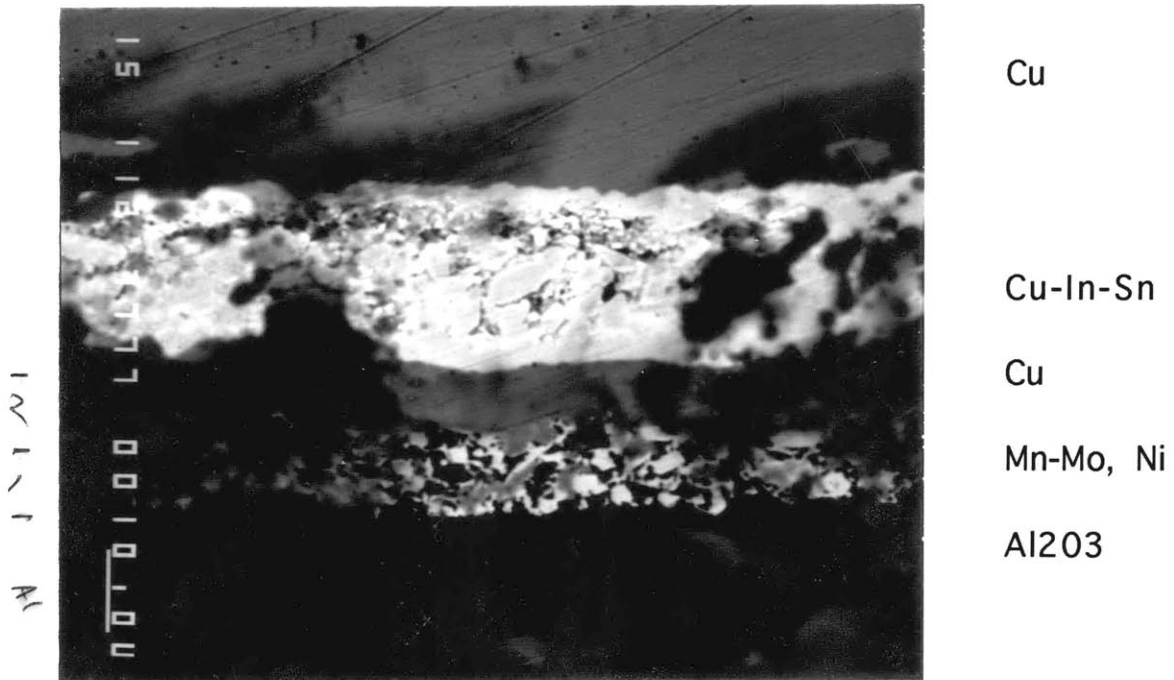


Figure 9: Cu/In-Sn/Cu LTTLP bond,
HT=157°C, ST=180°C, t=2.25hrs., RT>470°C

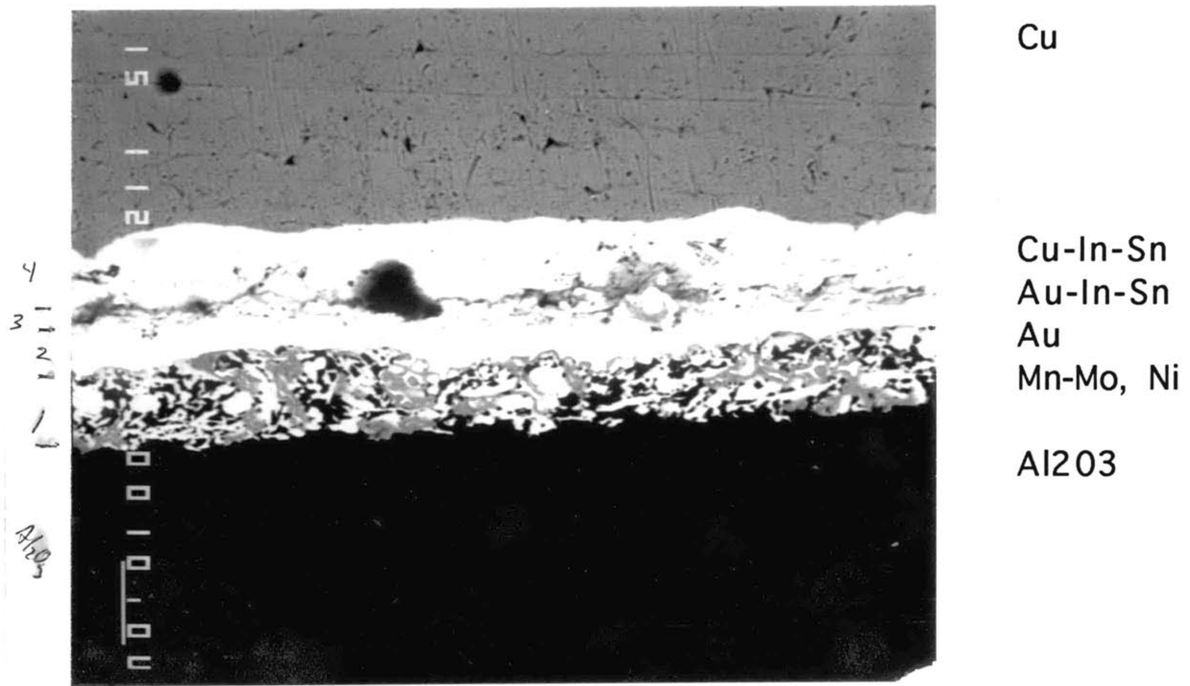


Figure 10: Au/In-Sn/Cu LTTLP bond,
HT=145°C, ST=180°C, t=2.25hrs., RT=120°C

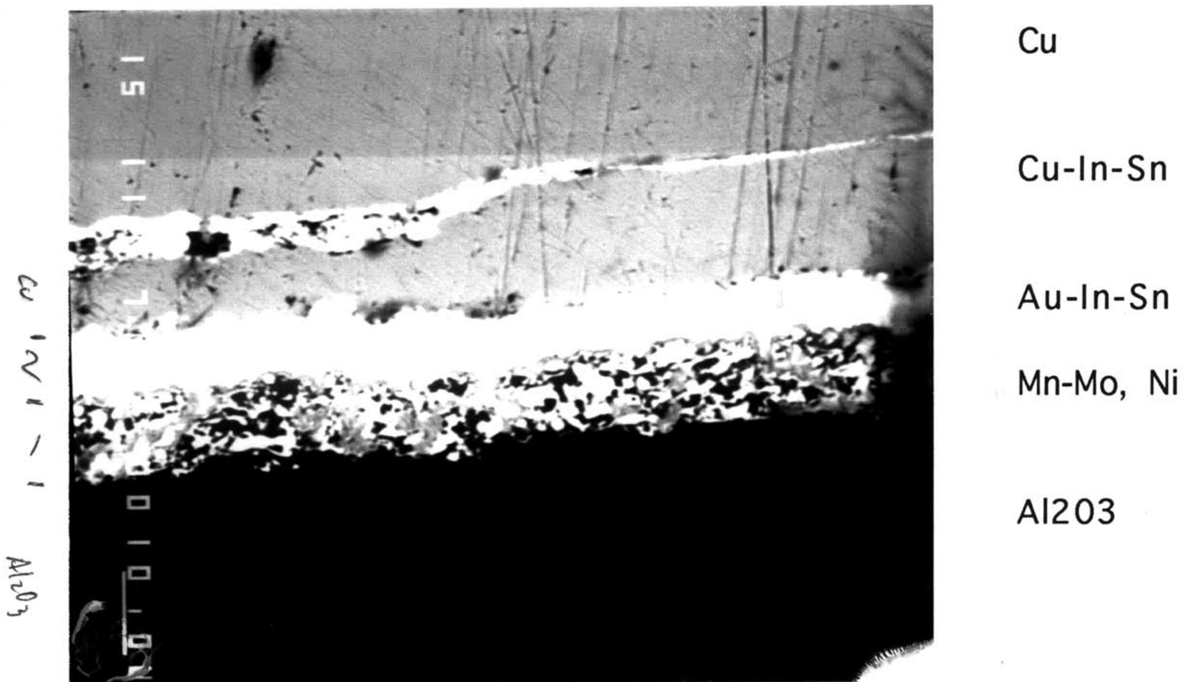


Figure 11: Au/In-Sn/Cu LTTLP bond,
HT=157°C, ST=180°C, t=2.25hrs., RT=120°C

however, very little of the gold plate and the underplate is present after LTTLP. It appears that the In-Sn solder has a strong tendency to dissolve the gold plating.

This is confirmed by the microprobe traces. Figures 12 and 13 show the results for the Cu/In-Sn/Cu system bonded at 145°C while figures 14 and 15 show the same system bonded at 157°C. It is seen that there are two intermediate Cu-In-Sn phases present between the solid copper adherends.

Figures 16 and 17 show the microprobe results of the Au/In-Sn/Cu system after LTTLP at 145°C while figures 18 and 19 show the same system bonded at 157°C. Although there is more scatter in the data, comparison of this data with similar samples processed at 149°C and 153°C show that three phases are present. Phases A and B are essentially the same as those found in the Cu/In-Sn/Cu system; however, phase C is an In rich phase containing approximately 25% gold. It should be noted in Figure 19, that the gold-nickel binary eutectic has also formed at one edge of the Au/In-Sn/Cu system.

The differences between these two bond system can be understood by considering the diffusion tendencies of In and Sn in both Au and Cu substrates.

5.3 DIFFUSION TRENDS

Figure 20 shows the Au/50%In-50%Sn/Cu system's composition profile at t=0 seconds. If diffusion is dependent on composition gradients, at t>0 diffusion occurs until a composition of 50%In50%Sn is reached in the Au and Cu phases on either side of the joint. But in fact, the driving force for diffusion is not a composition gradient, but is a chemical potential gradient.

Figures 21(a-d) shows the activities of the Au-In, Au-Sn, Cu-In, and Cu-Sn binary systems with the activities which were given in [9] except for In-Cu. For In-Cu, only the ΔH's were given. Activities of In-Cu were calculated based on a regular solution [10]. It is clear from these graphs that gold greatly decreases the activity of In and Sn while the

Figure 12: Composition Profile: Bond Composition vs. Bond Distance; Cu/In-Sn/Cu System, Solder T=180-205°C, t=2.25hr., T=145°C

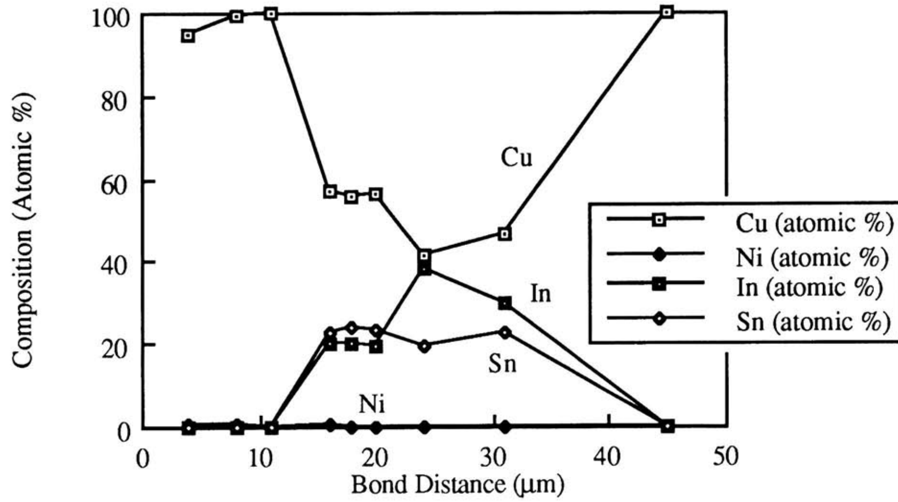


Figure 13: Composition Distribution of Figure 12

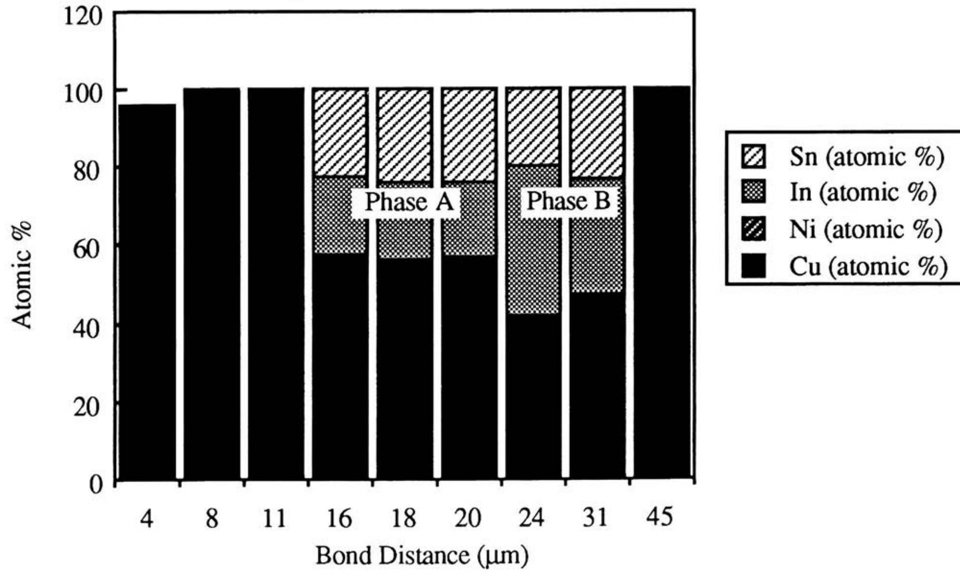


Figure 14: Composition Profile: Bond Composition vs. Bond Distance; Cu/In-Sn/Cu System, Solder T=180-205°C, t=2.25hr., T=157°C

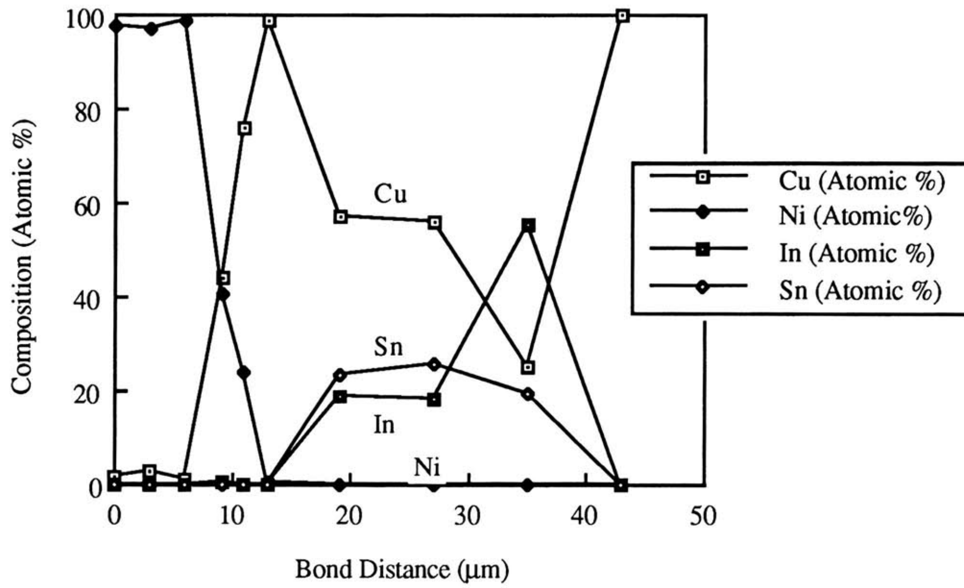


Figure 15: Composition Distribution of Figure 14

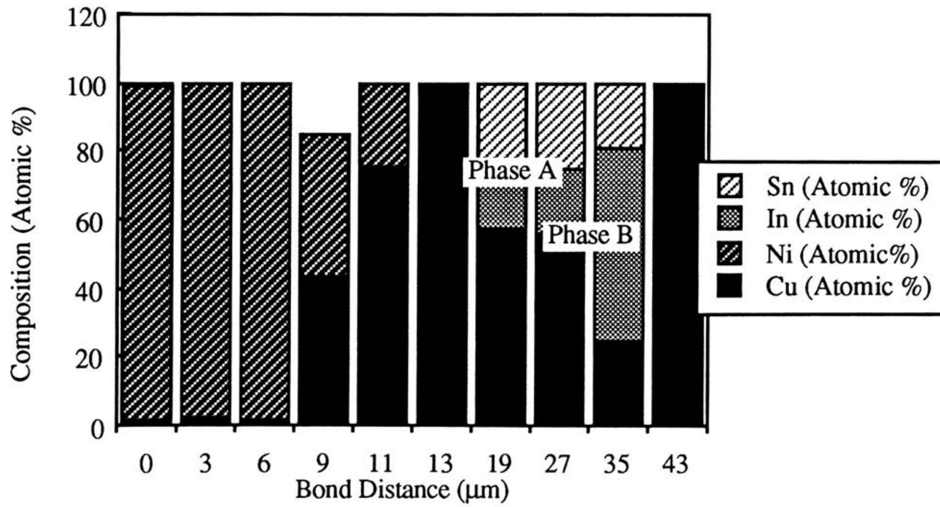


Figure 16: Composition Profile: Bond Composition vs. Bond Distance; Au/In-Sn/Cu System, Solder T=180-205°C, t=2.25hr., T=145°C

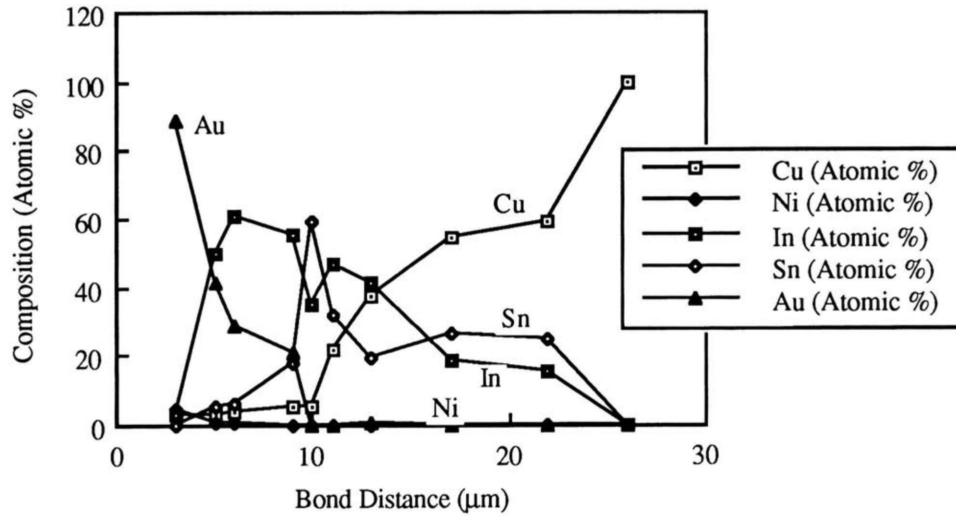


Figure 17: Composition Distribution for Figure 16

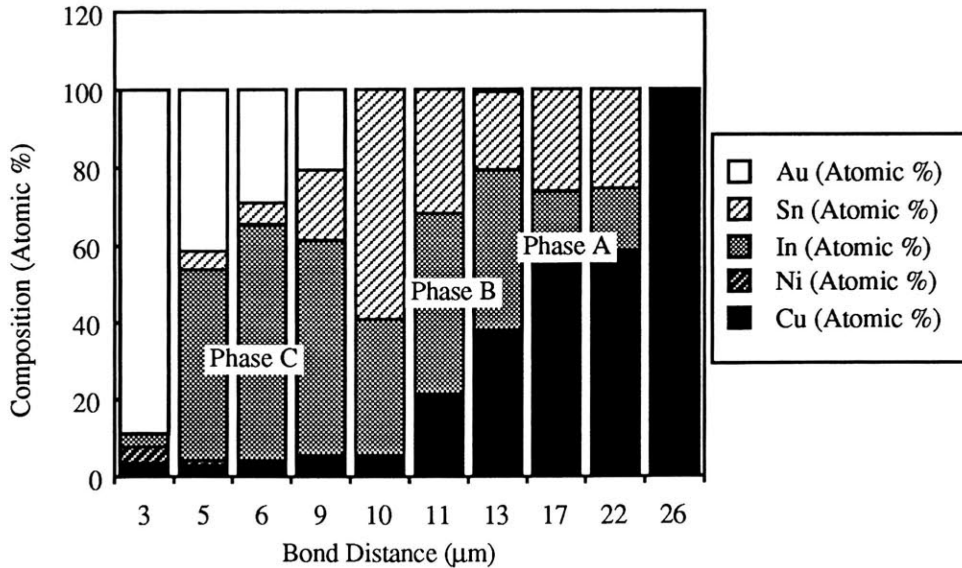


Figure 18: Composition Profile: Bond Composition vs. Bond Distance; Au/In-Sn/Cu System, Solder T=180-205°C, t=2.25hr., T=157°C

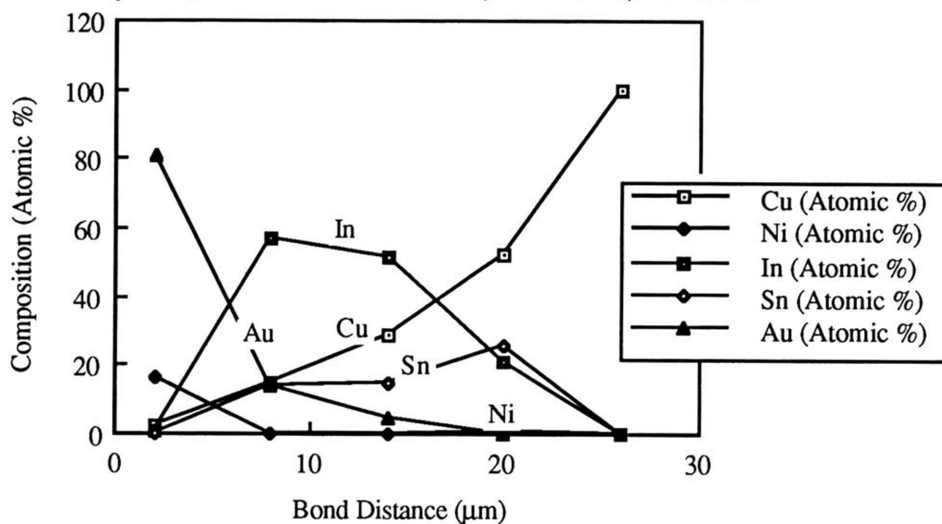


Figure 19: Composition Distribution of Figure 18

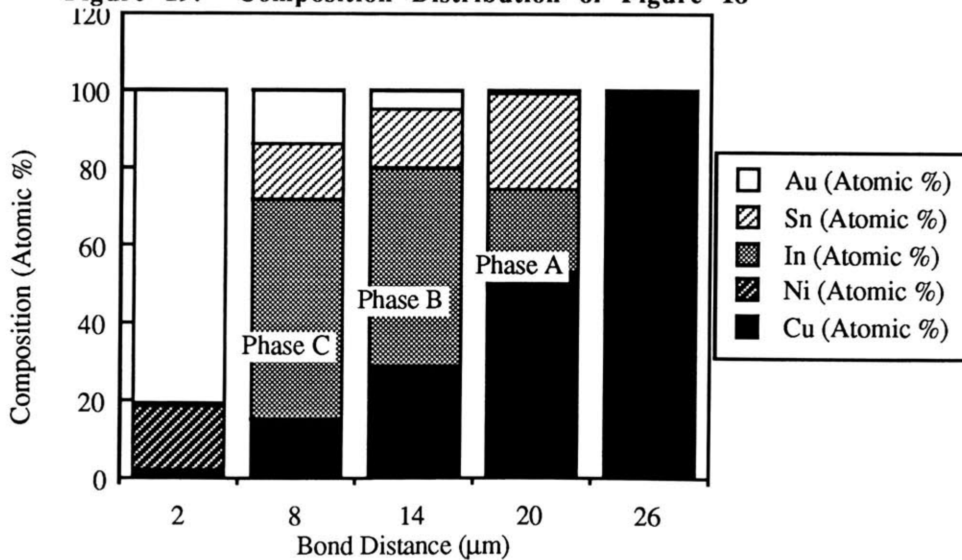


Figure 20: Composition Profiles of 50%In-50%Sn in Au/In-Sn/Cu system at t=0 and t>0

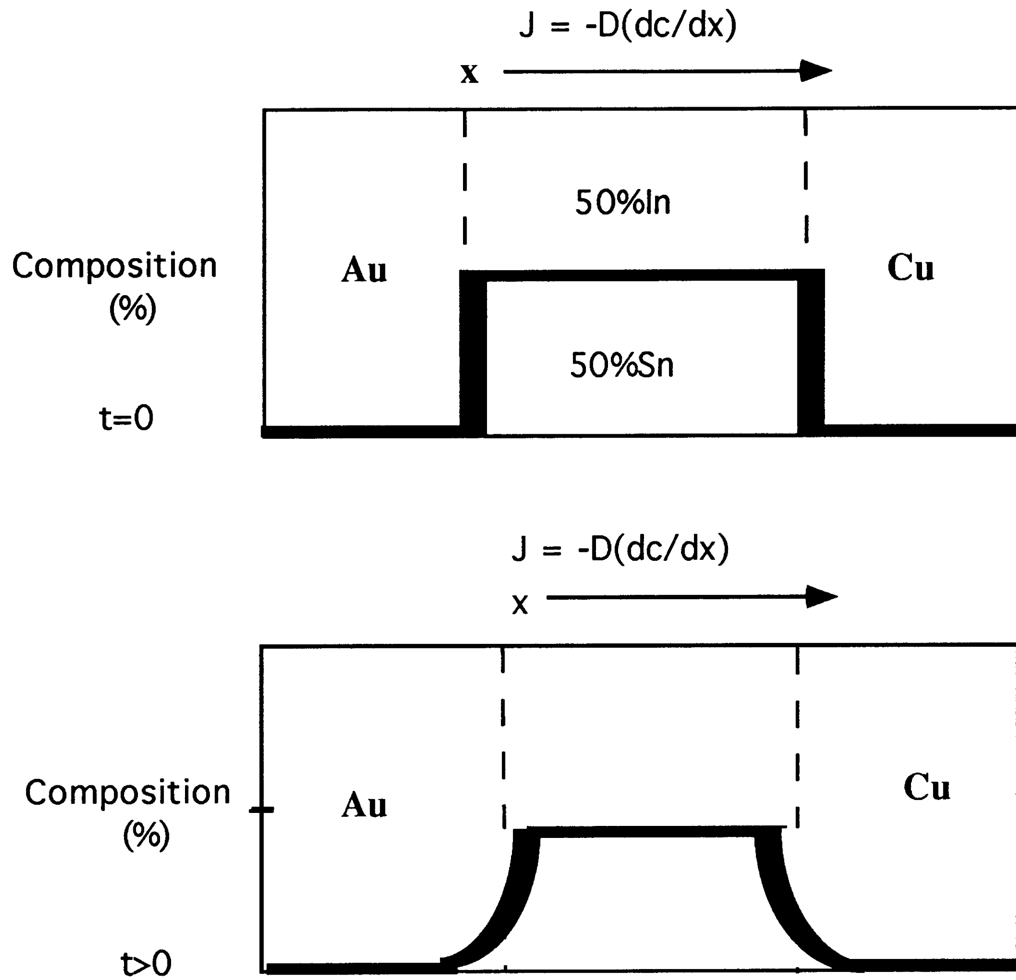


Figure 21a: Activity of In in Au versus Mole Fraction of In in Au at T=723K

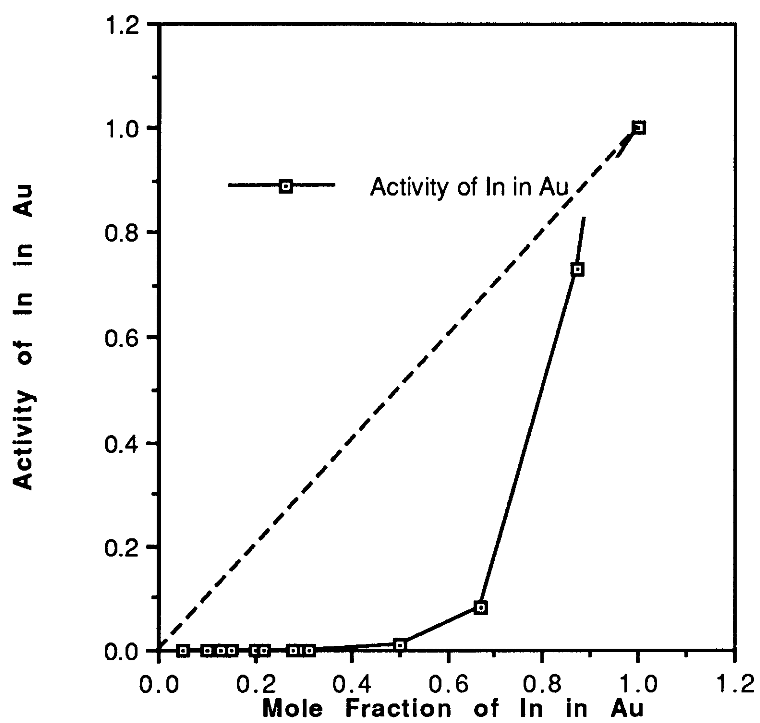


Figure 21b: Activity of Sn in Au versus Mole Fraction of Sn in Au at T=823K

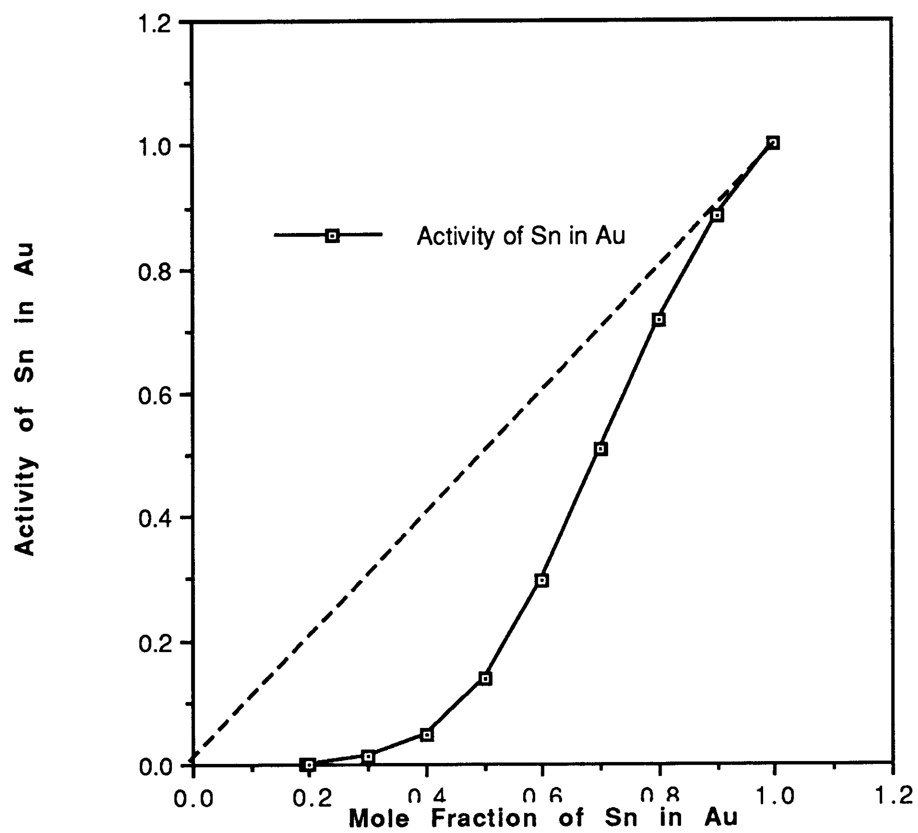


Figure 21c: Activity of In in Cu versus Mole Fraction of In in Cu at t=1013K

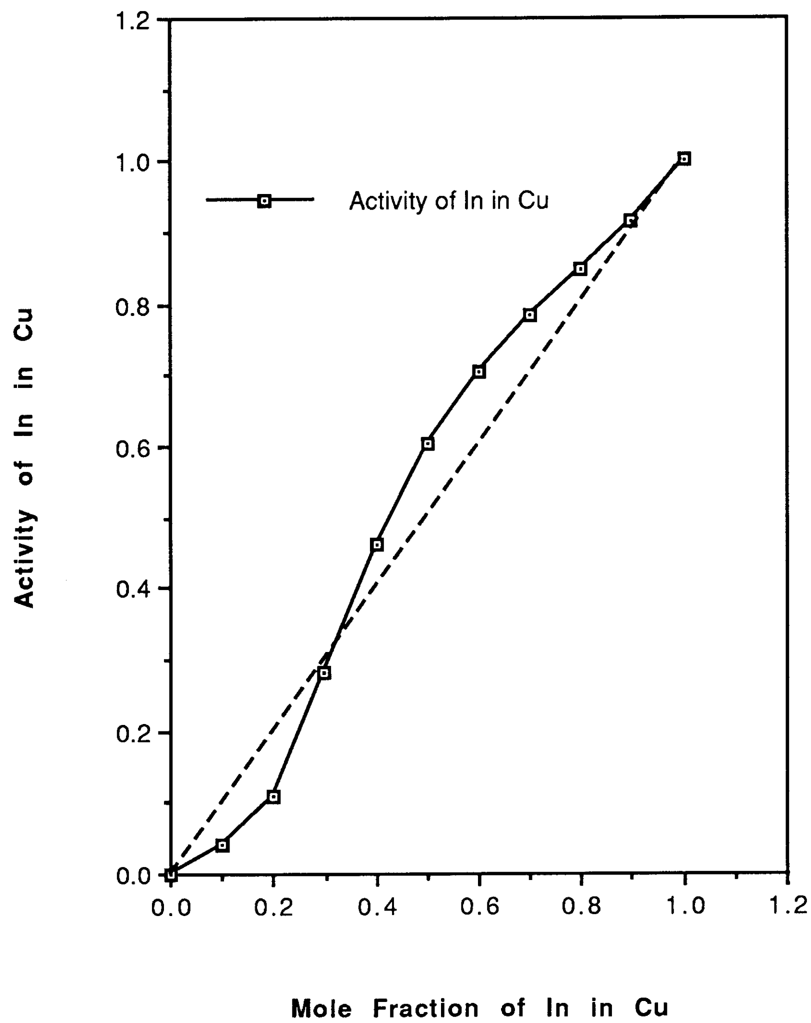


Figure 21d: Activity of Sn in Cu versus Mole Fraction of Sn in Cu at 1400K

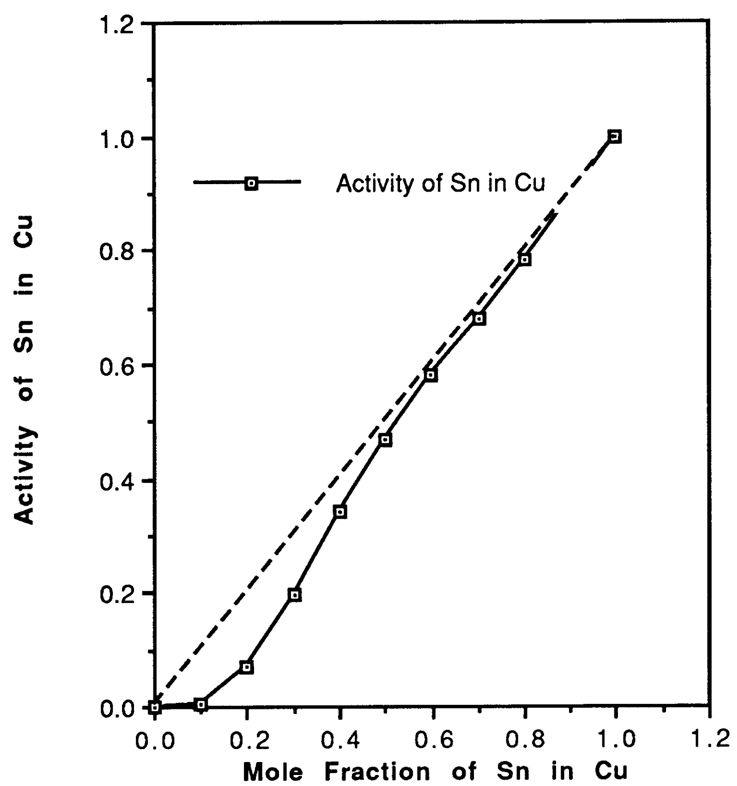
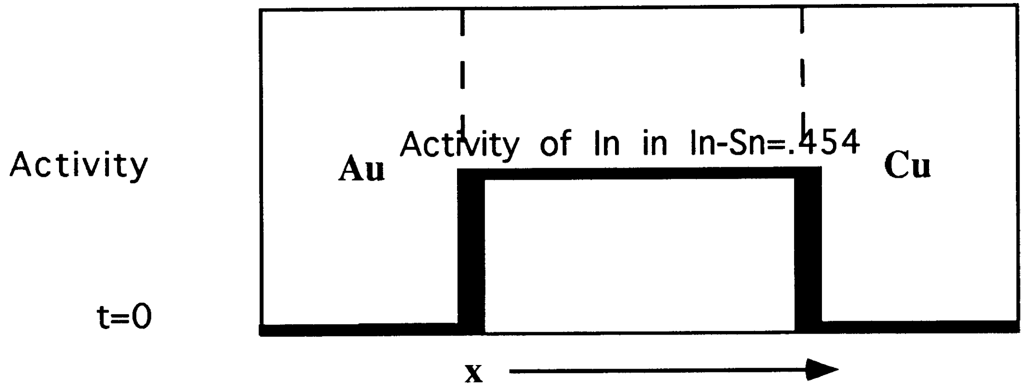


Figure 22a: Activity Profiles of In in Cu and Au at t=0 and t>0

$$J = -\mu(d\mu/dx)$$



$$J = -\mu(d\mu/dx)$$

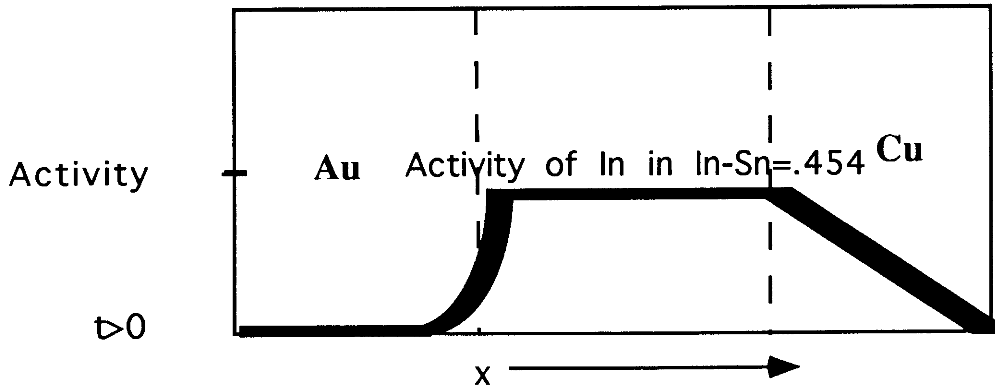
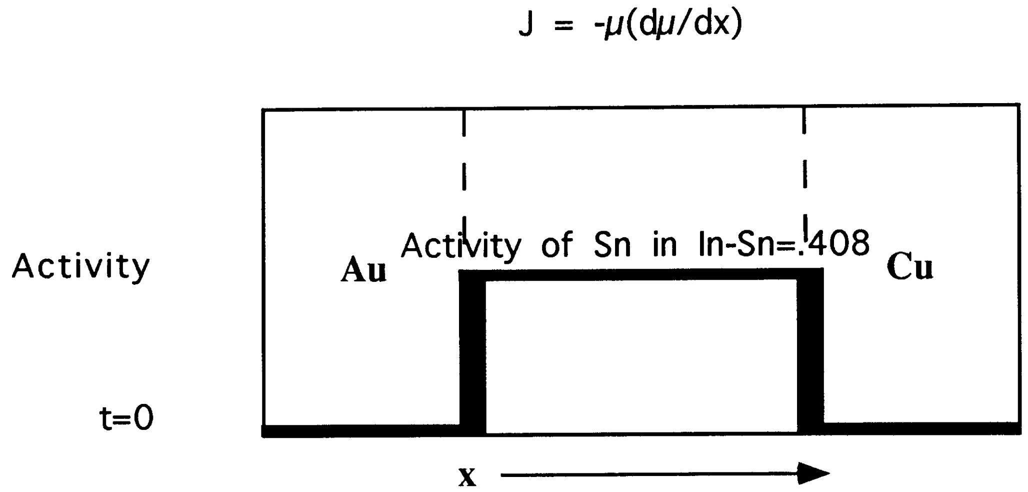
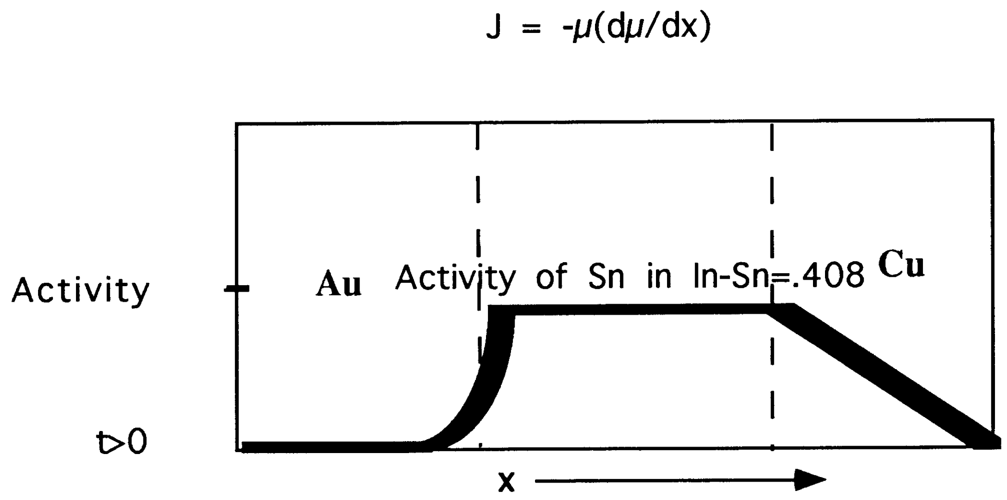


Figure 22b: Activity Profiles of Sn in Cu and Au at t=0 and t>0





activity of these alloying elements in copper is much closer to an ideal solution. If the diffusivities of In and Sn in the Cu and Au systems were equal and were controlled by the composition gradients, a symmetric dissolution profile such as Figure 20 would result. In fact, the driving force for diffusion is the activity gradient which, as shown in Figures 22a and 22b is much steeper on the Au side of the joint. As a result the In-Sn alloy dissolves all of the Au layer present on the substrate, forming a low melting (120°C) phase of 25% Au, 60%In, 8%Sn, 7%Cu.

The In and Sn have such low activities in this phase that there is insufficient activity gradient to diffuse the In and Sn into the adjacent Cu-rich phase. Thus diffusion is essentially stopped before isothermal solidification occurs.

This activity pattern suggests that In and Sn in In-Sn ,which are at a higher energy state, is preferentially diffusing towards the Au interface, which contains the In and Sn in a much lower energy state. Because the presence of Au alloyed with In and Sn, presents a more stable state, diffusion of In and Sn to the Cu interface is much slower. The bonding times are many times longer for the Au-In-Sn to diffuse the entire bond width, and then attain an equivalent activity of In or Sn in Cu.

6. Conclusions

The LTTLP bond process for Cu/In-Sn/Cu joints at HT=145°C and t=2.25 hours bonding time exhibit remelt temperatures greater than 470°C and thus greater bond strengths than the Au/In-Sn/Cu system, which forms a stable low melting Au-In-Sn-Cu phase. In and Sn, originally at a high energy state, preferentially diffuse to the lower activity state created at the Au interface. Au traps the In and Sn so that bonding times for the In-Sn-Au intermetallic to diffuse across the entire bond distance and attain an equivalent low activity in Cu are very long. The Cu/In-Sn/Cu system is more advantageous due to its ability to produce high melting intermetallics at short bonding times.

7. SUMMARY Table 3: Development of Process Parameters for 52%-48%In-Sn LTTLP Bond Attachment in Comparison with Motorola's Manufacturing Requirements

INITIAL PROPOSAL

Parameters		Comments
1. Materials System	Au Chip Carrier: 100µm" electroplated Au 0.8"x0.8"x0.06" Alumina Ceramic Component: Cu spacer 0.25:x0.25"x0.032" Solder Paste: 52-48%In-Sn, RMA-F flux	-Unable to produce RT>215°C due to multiphase bond -Stress buildup, bondline too thin(.001"=25µm)
2. Cleaning Preparation	Acetone, Mechanical Agitation	-Supposedly aids in wettability during soldering
3. Bond Mass	0.025g-0.03g	-Based on surface area and weight distribution of chip carrier and spacer
4. Solder Temperature	180°C or 136°C(liquidus)	-Solderability not sufficient -Au does not wet as well with paste so that bonding time is too long. -RT=120°C for all Au system samples.
5. Flux	RMA-F Type	-Storage: Refrigeration -Use: in laboratory environment
6. Fixturing	P=1lbs./.25 sq.in.=16psi	-Allows uniform, minimum bondline
7. HT Temperature	T=145°C	-But t=13+hrs. to achieve a RT>215°C

8. Bondline Thickness	Th=.001"=25µm	-Bondline too thin -Stress buildup so that RT=120°C for all samples
9. Remelt Temperature (RT)	RT=120°C	
10. Composition Profile	See attached graphs	-Varied, multiphase -LTTLP Bond has dissolution without widening of bond
11. Activity Profile	a(Sn/Cu)>a(Sn/Au) a(In/Cu)>a(In/Au)	-In or Sn preferentially diffuses to Au -Diffusion in 1 direction -Diffusion tends toward lower energy state
11. Thermal Cycling	2500 cycles	
12. Tensile Stress after HT	1760psi	
13. Tensile Stress after 2500 cycles	936-1464psi	

(Table 3 continued)

ALTERNATIVE SOLUTION PROPOSED

Parameters		Comments
1. Materials System	Cu Chip Carrier: Cu electroplated on 0.8"x0.8"x0.06" Alumina Component: Cu spacer 0.25"x0.25"x0.032" Solder Paste: 52-48% In-Sn	-At HT=145°C has attained RT>470°C -Th>42μm without build up of stress -Bonding time=2.25hrs.
2. Cleaning Preparation	-Cu Cleaner with Sulfuric Acid, Nitric Acid, and Water	-Aids in wettability of surface
3. Bond Mass	0.025g-0.030g	-Based on surface area to weight of spacer to chip carrier distribution
4. Solder Temperature	180°C	-Solder flow by t=1-3sec -HT=145°C produces RT>470°C
	136°C	-produces RT>470°C, but HT must be at 157°C
5. Flux	RMA-F Type	-Storage: Refrigeration needed -Use: in laboratory environment
6. Fixturing	P=1 lb/.25 sq.in.=16psi	-Necessary to make uniform bondline
7. Heat Treatment Temperature (HT)	145°C	-t=2.25hrs., bonding time decreased by 11+hrs. -RT>470°C

8. Bondline Thickness	Th=42-52μm	-Allows RT>470C without buildup of stress
9. Remelt Temperature (RT)	RT>470C	
10. Composition Profile	see attached graphs	-Single phase -Cu at 40%, In little less than 40%, Sn=20% -Cu composition must be greater than In -HT=145C, dissolution, allowing widening of bond up to Th=42μm -HT=157C, beginning of homogenization, Th>42μm -Diffusion in 2 directions
11. Thermal Cycling	2500 cycles	-LTTLP bond still intact
12. Tensile Stress after HT	>2000psi	
13. Tensile Stress after 2500 cycles	>2000psi	

8. References

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