A Fourth Order $\Sigma\Delta$ Bandpass Modulator

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

A fourth order bandpass $\Sigma\Delta$ modulator is proposed to digitize signals from a MEMS gyroscope. The modulator samples the amplitude-modulated signal at eight times the carrier frequency and achieves an SNR of 82dB with a sampling frequency of 640kHz and a bandwidth of 1.6kHz. This document shows that bandpass $\Sigma\Delta$ modulation offers the advantage of a high oversampling rate without the need to demodulate the signal for lowpass $\Sigma\Delta$ modulation.

Thesis Supervisor: Charles G. Sodini
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Chapter 1

Introduction

Encouraged by developments in semiconductor manufacturing, the use of micro-electro-mechanical systems(MEMS) allows the construction of small sensors that can be integrated with supporting electronics [7]. In popular point-and-shoot digital cameras, a resonating capacitive gyroscope can be used as a sensor for camera movement while the shutter is open; the corresponding information gathered by the MEMS sensor allows image blur resulting from hand shake to be alleviated. Given the micro-scale of the sensing gyroscope and the small position variants to be detected, challenges of the system include small signal strength and sensitivity to noise.

Analog-to-digital conversion is required to digitize measurements from the capacitive gyroscope sensor. The input signal characteristics and requirements to be met by the $\Sigma\Delta$ modulator are shown in Table 1.1. The maximum input signal range of 150mV stems from the minute scale of the sensor and is of particular note because the quantization and thermal noise levels must be minimized to achieve the desired accuracy despite the weak input signal strength. The specifications given indicate that the desired analog-to-digital converter (ADC) should focus on accuracy rather than conversion speed. The signal carrier frequency is a relatively low 80kHz, and a dynamic range of 72dB (approximately 12 bits) corresponds to an LSB of 36.6μV as shown in Equation 1.1.

$$\text{LSB voltage } = \frac{V_{FS}}{2^N} = \frac{150mV}{2^{12}} = 36.6\mu V \tag{1.1}$$

Table 1.1: Input Signal Characteristics and Target Specifications

Carrier Frequency	80kHz
Signal Bandwidth	100Hz
Input Signal Range	150mV
Desired Dynamic Range	>72dB

This emphasis on accuracy indicates that a $\Sigma\Delta$ converter should be used because $\Sigma\Delta$ converters are well-suited to high accuracy and low frequency applications [3].

1.1 Organization of Thesis

The thesis first discusses the basics of $\Sigma\Delta$ modulation in Chapter 2. Chapter 3 discusses the reasoning behind the design choices and shows that bandpass modulation is the logical choice for this application. Behavioral simulation results are discussed in Chapter 4. The thesis concludes with suggestions for future work in Chapter 5.

Chapter 2

$\Sigma\Delta$ Analog-to-Digital Conversion

The following chapter introduces the basic operation of and theory behind $\Sigma\Delta$ conversion. In addition, the chapter introduces possible $\Sigma\Delta$ modulator loop behaviors.

2.1 Basic $\Sigma\Delta$ Conversion

Commonly used for high-resolution but lower speed applications, $\Sigma\Delta$ A/D converters ease the necessity for precise component matching and sharp analog filters through oversampling and noise-shaping [3]. The main blocks of $\Sigma\Delta$ A/D converters are anti-aliasing filters, an analog modulator, and digital demodulation filters; a block diagram of $\Sigma\Delta$ modulation is shown in Figure 2-1. This thesis focuses on the analog modulator, which is outlined in Figure 2-2. The sections below discuss $\Sigma\Delta$ modulation with respect to oversampling and noise-shaping.

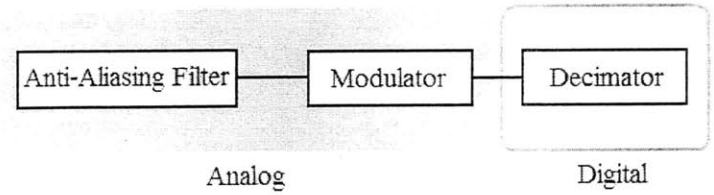


Figure 2-1: Block diagram of a $\Sigma\Delta$ A/D converter.

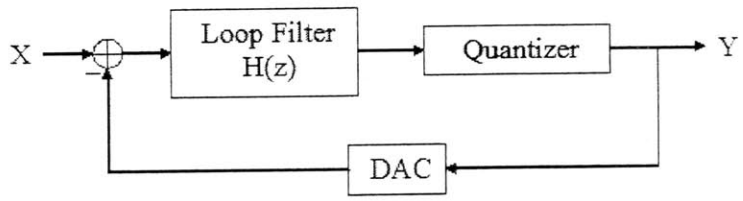


Figure 2-2: Block diagram of a $\Sigma\Delta$ modulator.

2.1.1 Quantization

Quantization converts an analog input into a digital signal by assigning an output value to a range of sampled inputs. The ideal quantizer transfer function in Figure 2-3 shows that quantization does not produce a one-to-one relationship between input and output values. The behavior of the quantizer results in quantization error, or quantization noise, because each analog input incurs an error when assigned an output value. The quantization error is shown by the shaded areas in Figure 2-3 that represent the difference between the analog input value and the output quantized value.

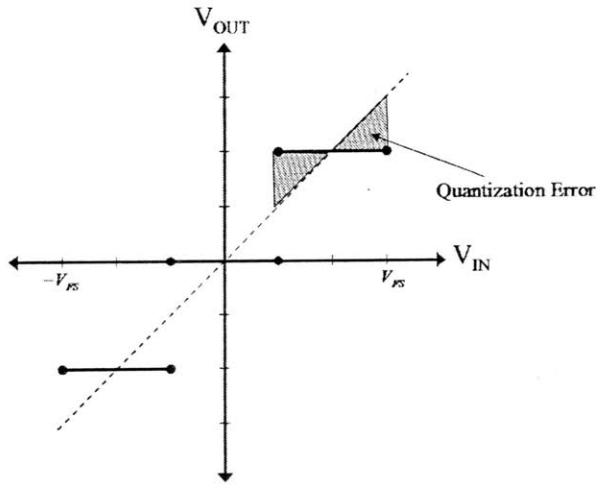


Figure 2-3: Ideal quantizer transfer function

While quantization error is derived from the input signal, quantization noise power can be approximated as a uniformly distributed white noise source given the following assumptions [4]:

- The quantizer does not saturate.

- The difference between successive samples of the input signal is large enough to ensure that the quantizer output cannot be predicted.
- The input signal shows no periodic or harmonic behavior and is not constant.

In a system with a full-scale voltage of V_{FS} and N bits and assuming that quantization noise can be modeled as a uniform noise source, the RMS value of the quantization error is given by Equation 2.1.

$$V_{Q(RMS)} = \frac{LSB}{\sqrt{12}} = \frac{V_{FS}}{2^N\sqrt{12}} \tag{2.1}$$

Given the above assumptions, the quantization error, Q, can be incorporated into the linearized $\Sigma\Delta$ modulator model shown in Figure 2-4. The white noise approximation thus eases the analysis of $\Sigma\Delta$ ADCs by allowing quantization error to be linearly added into the model as an independent noise source. $H(z)$ is the forward loop transfer function responsible for noise-shaping and will be discussed in Section 2.1.3.

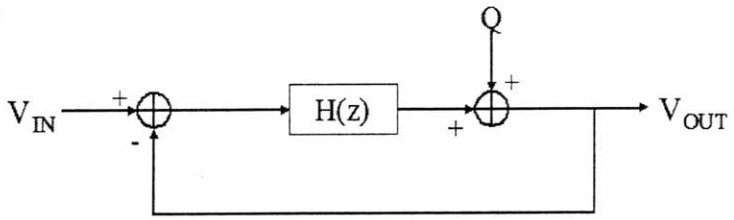


Figure 2-4: Linear model of a first-order $\Sigma\Delta$ modulator.

The performance of the converter is measured with respect to the signal-to-noise ratio (SNR); the SNR is determined by the ratio between the input signal power, P_s, and the inband noise signal power, P_e. P_s can be found by assuming the input to be a sine wave with peak-to-peak amplitude V_{FS}; the input signal power is then:

$$P_s = \frac{(\frac{V_{FS}}{2})^2}{2} = \frac{V_{FS}^2}{8} \tag{2.2}$$

Simplifying the analysis so that P_e is derived only from quantization noise and assuming that the sampling rate is approximately the Nyquist frequency ($2f_b$), P_e is

equal to $V^2_{Q(RMS)}$, the quantization noise power shown in Equation 2.1. The effect of quantization noise on the SNR of a Nyquist-rate converter is shown in Equation 2.3 where N is the number of bits. This shows that each additional bit decreases quantization noise by a factor of 2 and increases the SNR by about 6dB. Further discussion of multi-bit quantizers will be discussed below.

$$\begin{aligned} SNR &= 10\log(\frac{P_s}{P_e})\ \text{dB} \\ &= 10\log(\frac{2^{2N}12}{8}) \\ &= 10\log(2^{2N}) + 10\log(\frac{3}{2}) \\ &= 6.02N + 1.76\ \text{dB} \end{aligned} \tag{2.3}$$

2.1.2 Oversampling

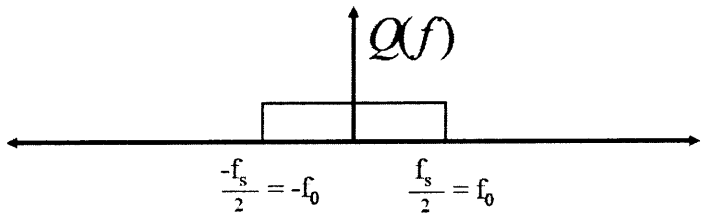
The previous section discussed quantization noise for converters that sampled around the Nyquist frequency. For all types of ADCs, the Nyquist Theorem states that the sampling frequency of a converter f_s must be at least twice the signal bandwidth f_b, or the Nyquist frequency, to prevent aliasing. Aliasing causes interference between images of the signal and prevents the signal from being reconstructed fully [3]. The front-end anti-aliasing filters of $\Sigma\Delta$ converters serve to band-limit the input signal and reduce the effect of out-of-band signals that fold back into the baseband.

However, oversampling converters, such as $\Sigma\Delta$ converters, sample above the input signal at a frequency above the Nyquist frequency to decrease inband quantization noise. The oversampling rate (OSR) is given by Equation 2.4 and is a measure of the sampling frequency, (f_s) with respect to the signal bandwidth (f_b) [9].

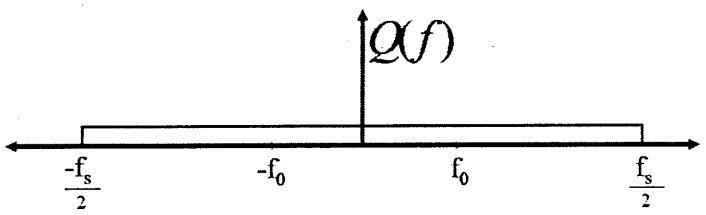
$$OSR = \frac{f_s}{2f_b} \tag{2.4}$$

In the previous subsection, the total quantization noise power, $V^2_{Q(RMS)}$ was approximated as a uniform white noise source dependent on V_{FS} and N, the number of bits [4]. This white noise can be represented as a uniform probability density ranging

from $\frac{-f_s}{2}$ to $\frac{f_s}{2}$. When the sampling frequency is increased to create an oversampling converter, the quantization noise power spreads over a greater frequency spectrum as seen in Figure 2-5. Figure 2-5 compares quantization noise spectral densities given two different sampling frequencies, f_s, and shows that high oversampling frequencies considerably decrease noise power between $-f_0$ and f_0.



(a) Spread of quantization noise power if the sampling frequency is equal to the desired bandwidth.



(b) Spread of quantization noise power if the sampling frequency is greater than the desired bandwidth.

Figure 2-5: Comparison of quantization spectral noise density with respect to sampling frequency.

Since the total quantization noise is equal to $V^2_{Q(RMS)}$, the height of each spectral density must be equal to $\frac{V_{FS}}{2^N\sqrt{12}}\frac{1}{\sqrt{f_s}}$ [3]. The inband quantization noise can then be calculated by integrating from $-f_b$ to f_b as shown in Equation 2.5.

$$P_e = \int_{-f_b}^{f_b} (\frac{V_{FS}}{2^N\sqrt{12}}\frac{1}{\sqrt{f_s}})^2 df = \int_{-f_b}^{f_b} \frac{V^2_{Q(RMS)}}{f_s} df = \frac{V^2_{Q(RMS)} 2f_b}{f_s} = \frac{V^2_{Q(RMS)}}{OSR} \qquad (2.5)$$

This shows that the larger spread of $V^2_{Q(RMS)}$ at higher sampling frequencies results

in lower quantization noise within any particular frequency band, and the decrease in inband quantization noise improves the SNR by reducing the noise floor. Using the same sine wave input from above, Equation 2.6 shows that doubling f_s results in an approximately 3dB increase in SNR for a modulator due to the decrease in inband quantization noise.

$$\begin{aligned} SNR &= 10\log\left(\frac{P_s}{P_e}\right) \text{ dB} \\ &= 10\log\left(\frac{2^{2N}12}{8}\cdot OSR\right) \\ &= 10\log\left(2^{2N}\right) + 10\log\left(\frac{3}{2}\right) + 10\log\left(OSR\right) \\ &= 6.02N + 1.76 + 10\log\left(OSR\right) \text{ dB} \end{aligned} \tag{2.6}$$

An additional advantage of oversampling involves the relaxation of requirements on the analog anti-aliasing filters. As shown in Figure 2-6, the anti-aliasing filter limits the input signal to prevent out-of-band noise from aliasing the input signal. Assuming that f_b is less than the $f_s/2$, higher sampling rates allow the anti-aliasing filters to be constructed with more gradual roll-offs because any signal greater than $f_s/2 - f_b$ will be attenuated.

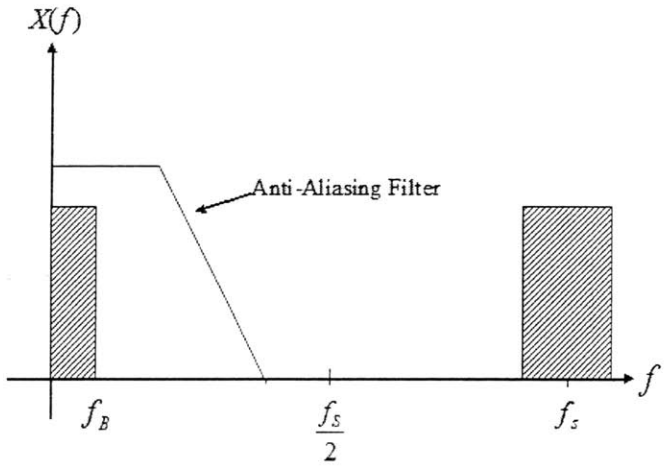


Figure 2-6: Anti-aliasing filter roll-off with respect to sampling frequency.

2.1.3 Noise-Shaping

$\Sigma\Delta$ A/D converters further reduce inband quantization noise by shaping quantization noise out-of-band using negative feedback. The desired goal of noise-shaping is to pass the input signal and attenuate quantization noise at frequencies within the baseband. Decreasing the inband quantization noise increases the SNR of the modulator by lowering the inband noise floor.

Noise-shaping thus requires a forward loop filter, $H(z)$, that has high gain in the signal band [4]. $H(z)$ can be analyzed with respect to the signal transfer function (STF) and noise transfer function (NTF) shown in Equations 2.7 and 2.8 [3].

$$\text{STF} = \frac{V_{out}}{V_{in}} = \frac{H(z)}{1 + H(z)} \tag{2.7}$$

$$\text{NTF} = \frac{V_{out}}{Q} = \frac{1}{1 + H(z)} \tag{2.8}$$

In the signal band, $|H(z)| \gg 1$ results in STF ≈ 1 and NTF ≈ 0; this ensures that the input signal is perfectly passed while the noise signal is shaped out of the signal band. Noise-shaping can be further examined through the linearized noise-transfer loop of a single-bit modulator shown in Figure 2-7. The output quantization noise is given by the difference between the current quantization error and a loop-filtered quantization error; however, the loop-filtered quantization error is shaped by the inverse of the $H(z)$. Therefore, within the signal band, this noise is small due to the high inband gain of $H(z)$.

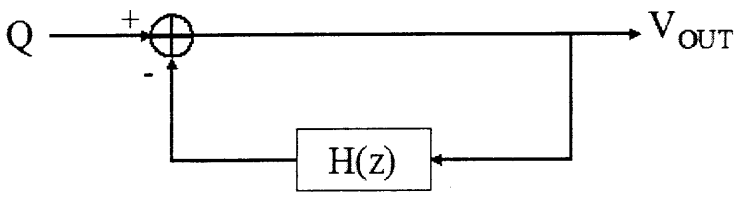


Figure 2-7: Linear model of the NTF of a $\Sigma\Delta$ modulator.

The effect of noise-shaping on SNR can be examined using a lowpass $\Sigma\Delta$ modulator example. For a first-order low-pass modulator, the forward loop filter, $H(z)$ is

an integrator and the NTF is given as:

$$\text{NTF} = (1 - z^{-1}) \tag{2.9}$$

The magnitude of the NTF in this example is equal to $\sin(\frac{\pi f}{f_s})$ and can be approximated as $\frac{\pi f}{f_s}$ [3]. The inband quantization noise power, P_e, can then be calculated by integrating the noise-shaped quantization noise as follows [3]:

$$P_e = \int_{-f_b}^{f_b} \frac{V_{Q(RMS)}^2}{f_s} |NTF(f)|^2 df = \int_{-f_b}^{f_b} \frac{V_{Q(RMS)}^2}{f_s} (\frac{\pi f}{f_s})^2 df = \frac{V_{Q(RMS)}^2}{OSR^3} \frac{\pi^2}{3} \tag{2.10}$$

Using the same sine wave input as defined above, the SNR of an oversampled and noise-shaped converter is shown in Equation 2.11.

$$\begin{aligned} SNR &= 10\log(\frac{P_s}{P_e}) \text{ dB} \\ &= 10\log(\frac{2^{2N}12}{8} \cdot \frac{3}{\pi^2} \cdot OSR^3) \\ &= 10\log(2^{2N}) + 10\log(\frac{3}{2}) + 10\log(\frac{3}{\pi^2}) + 30\log(OSR) \\ &= 6.02N + 1.76 - 5.17 + 30\log(OSR) \text{ dB} \end{aligned} \tag{2.11}$$

Comparison of Equation 2.6 and Equation 2.11 shows that noise-shaping boosts the SNR of a system without the need to increase the OSR. The 5.17dB decrease in SNR shown in Equation 2.11 stems from the slight amplification of quantization noise by the forward loop. As shown above, oversampling decreases inband quantization noise to increase the SNR but may result in high power consumption due to the higher sampling frequency. The increase in SNR from noise-shaping thus relaxes the need for high oversampling rates.

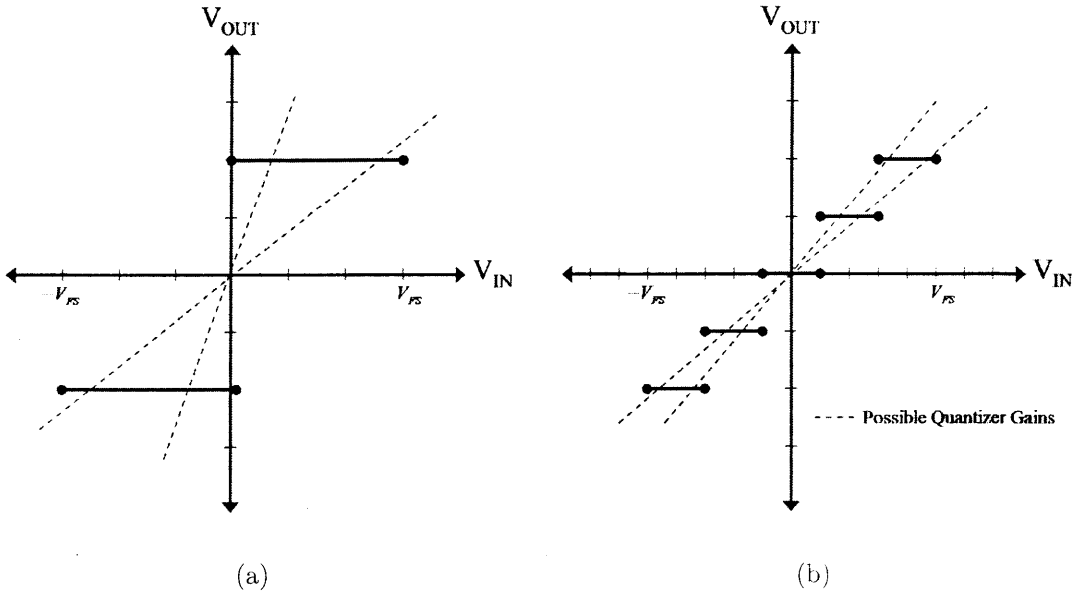
2.2 $\Sigma\Delta$ Conversion Enhancements

The following section expands on the basic theory presented in Section 2.1 and shows the need for more complex $\Sigma\Delta$ converters. Higher-order converters will be presented

along with the differences between lowpass and bandpass $\Sigma\Delta$ converters. In addition, the section also discusses multi-bit quantization.

2.2.1 Multi-Bit Quantization

In multi-big quantization, the output of the quantizer consists of more than 2 levels; Figure 2-8(b) shows an example of a multi-bit quantizer. Multi-bit quantization improve performance by decreasing quantization error; each output signal incurs less error because the full-scale input range is divided between smaller sized ranges. The increase in SNR is quantified in Equation 2.6 and Table 2.1 and shows that the SNR increases by approximately 6dB for every additional bit. In addition to lower quantization noise, multi-bit quantizers increase the stability of the modulator because the range of possible gains for multi-bit quantizers is smaller than that of single-bit quantizers. As shown in Figure 2-8, the gain through a single-bit quantizer is uncertain and could be many values. In contrast, the multi-bit quantizer shown in Figure 2-8(b) has a smaller range of possible gain values.



(a) (b)

Figure 2-8: Example of possible gains in single-bit quantizer

The main disadvantage of multi-bit quantization occurs in the nonlinearity of the

Table 2.1: Effect of noise-shaping on a lowpass modulator [3]

Noise-Shaping Order	SNR (dB)
0	$SNR = 6.02N + 1.76 + 10log(OSR)$
1	$SNR = 6.02N + 1.76 - 5.17 + 30log(OSR)$
2	$SNR = 6.02N + 1.76 + -12.9 + 50log(OSR)$

feedback DAC shown in Figure 2-2. Since the error of the DAC is in the feedback loop of the modulator, the noise-shaping properties of the loop filter does not affect the error from the DAC. This indicates that DAC nonlinearity directly affects the input signal and cannot be minimized through noise-shaping. The performance of a multi-bit $\Sigma\Delta$ modulator thus must also take into consideration the precision of the feedback DAC. In contrast, single-bit quantization has the advantage of complete linearity as the output of the quantizer only switches between two values.

2.2.2 Higher-Order Loop Filters

Higher-order loop filters use more than one integrator or resonator to increase the noise-shaping capability of a $\Sigma\Delta$ modulator. Using the lowpass $\Sigma\Delta$ modulator example and the sine wave input presented in the initial discussion of noise-shaping, Table 2.1 shows the derived SNR equations for higher-order modulators [3]. The derivation for the first-order $\Sigma\Delta$ modulator is shown in Section 2.1.3. This shows that quantization noise is pushed more aggressively out of the signal band as the order of the loop filter increases. Increased noise-shaping also magnifies the effect of oversampling on quantization noise. For example, doubling the OSR in a first-order noise-shaped increases the SNR by approximately 9dB; doubling the OSR in a second-order system increases the SNR by approximately 15dB. Higher-order modulators can thus achieve higher performance at lower oversampling rates.

The predicted SNR equations in Table 2.1, however, do not take into the stability of the modulator. Practically, the increased complexity of higher-order architectures decreases the stability of the modulator and limits the SNR to less than the predicted value [9]. High-order converters are also used to decrease the effect of idle tones in first-order modulators. Tones occur when the DC component of the input signal

causes the white noise approximation presented above to fail because quantization noise can no longer be assumed as a random and independent noise source. However, high-order converters consist of multiple integrators or resonators in the loop filter. Noise from each successive stage serves to randomize quantization noise and breaks the periodic pattern that causes idle tones. Therefore, although a first-order single-bit lowpass $\Sigma\Delta$ modulator can achieve over 12 bits of accuracy using an OSR of 256, higher-order modulators are preferred because they reduce the presence of idle tones.

2.2.3 Noise-shaping Loop Topologies

The discussion thus far has concentrated on lowpass $\Sigma\Delta$ modulators. An alternative noise-shaping loop that is relevant to this thesis is the bandpass modulator, which requires resonators rather than integrators in the forward loop filter. The following subsections describe and contrast lowpass and bandpass $\Sigma\Delta$ modulators.

Lowpass $\Sigma\Delta$ Conversion

Lowpass $\Sigma\Delta$ modulators shape quantization noise out-of-band up to a desired frequency and is generally used for signals concentrated at low frequencies. The forward loop filter therefore must have high gain beginning from DC to some higher frequency. An example of a lowpass $\Sigma\Delta$ modulator's behavior is shown in Figure 2-9(a); the input signal to the lowpass $\Sigma\Delta$ modulator is passed while the inband quantization noise is shaped to higher frequencies. The plot shows the behavior of a single-bit 3rd order low pass modulator with an OSR of 128 and an 8MHz sampling frequency.

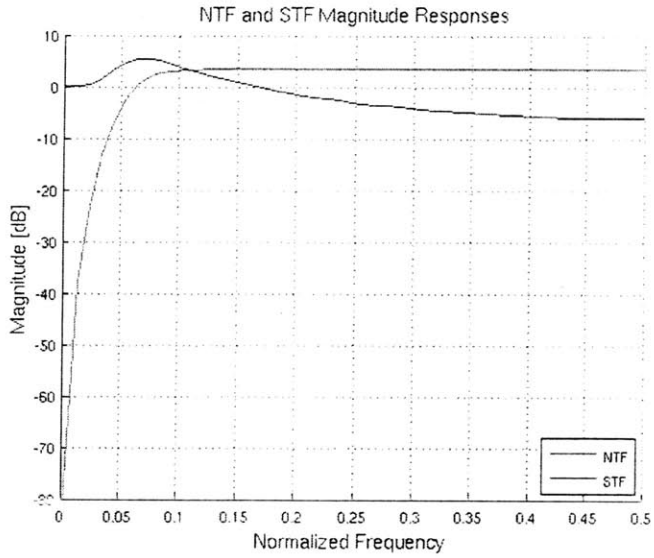
Bandpass $\Sigma\Delta$ Conversion

A bandpass modulator shapes the quantization noise out of a notched band and is well-suited for applications with a modulated signal. An example of a bandpass modulator's NTF and STF is shown in Figure 2-9(b). It should be noted that the bandwidth of a bandpass modulator is different from the bandwidth of the input signal.

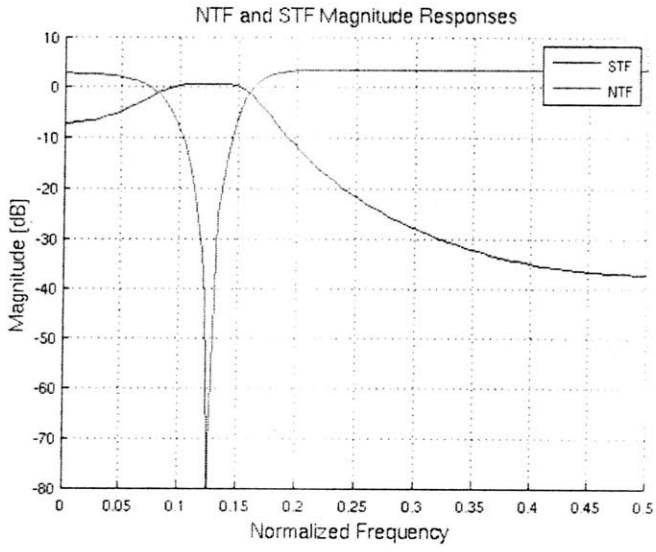
In bandpass $\Sigma\Delta$ modulation, the forward loop filter only has a high gain within a specific frequency band, which requires the use of resonators rather than integrators. Resonators will be discussed in more detail in Chapter 3. Additionally, the sampling frequency for bandpass modulators is a multiple of the carrier frequency; this property allows the sampling frequency to be much lower in bandpass $\Sigma\Delta$ modulation than in a corresponding lowpass $\Sigma\Delta$ modulator.

2.3 Summary

The basics of $\Sigma\Delta$ conversion were outlined in this section. The effects of oversampling and noise-shaping on SNR was presented and expanded into multi-bit quantization and higher-order modulators



(a) Lowpass NTF and STF



(b) Bandpass NTF and STF

Figure 2-9: Comparison of lowpass and bandpass behaviors.

Chapter 3

Bandpass $\Sigma\Delta$ Modulation Analysis

Chapter 3 outlines the design of a discrete-time bandpass modulator by analyzing the NTF and STF with respect to dynamic range, modulator order, sampling frequency, and stability. The transfer function analysis is followed by a discussion of the reasons for choosing a Lossless Discrete Integrator (LDI) resonator and the chosen topology. Results from MATLAB and SIMULINK conclude the chapter.

3.1 Signal and Noise Transfer Function Analysis

The signal and noise transfer functions of the system were determined with respect to the trade-off between resolution, robustness, and stability. The section describes how the desired specifications are fulfilled and shows that bandpass modulation is more suited to the MEMS application.

3.1.1 Bandpass Noise-Shaping

A bandpass modulator is more suitable for the given application because the input signal is a narrow-band signal (100Hz) modulated to a carrier frequency (80kHz). A lowpass converter would require modulating the input signal down to DC or using a high sampling frequency. However, the disadvantages of bandpass $\Sigma\Delta$ modulation are:

- Increased complexity

- Difficulty constructing reliable resonators

In addition to the differences discussed in Section 2.2.3, the sampling frequency of bandpass $\Sigma\Delta$ modulation differs slightly from the analysis presented in Chapter 2. In bandpass $\Sigma\Delta$ modulation, the sampling frequency is a multiple of the carrier frequency rather than the input signal bandwidth; the proposed modulator uses a sampling frequency 8 times the carrier frequency for an f_s of 640kHz. As discussed below, the ratio between the carrier and sampling frequencies also determines the placement of poles in the resonators.

An Lth order lowpass modulator corresponds to a 2L order bandpass modulator as can be seen by the conventional z to z^2 transformation [4]. In this thesis, the order of bandpass $\Sigma\Delta$ modulation will be referred to as twice the noise-shaping capabilities of the converter; for example, a 2nd order noise-shaping loop ($L = 2$) corresponds to a 4th-order bandpass modulator.

3.1.2 Dynamic Range

The dynamic range (DR) describes the ratio between the maximum input amplitude and the input amplitude where the signal becomes equal to the noise floor [10]. In a $\Sigma\Delta$ converter, the maximum dynamic range possible of a modulator is estimated by Equation 3.1 where R is the oversampling rate, L is the noise-shaping order, and N is the number of bits.

$$DR_{max} = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 R^{2L+1} \tag{3.1}$$

The desired dynamic range of 72dB corresponds to approximately 12 bits of resolution.

3.1.3 Quantization

A single-bit modulator was chosen to take advantage of the inherent linearity of single-bit quantizers [9]. The output of the comparator is responsible for only two values, and the feedback DAC nonlinearity is eliminated. The disadvantages of single-bit modulation were addressed by limiting the out-of-band gain of the NTF to ensure stability and by analyzing the trade-off between oversampling rate and multi-bit quantization. The stability issues caused by the nonlinearity of the quantizer are discussed below. Multi-bit quantization was not needed to achieve the 12-bit resolution because the quantization noise could be decreased sufficiently using a moderate OSR. Therefore, since multi-bit quantization introduces additional error due to the feedback DAC, single-bit quantization is most suited for the specified requirements.

3.1.4 Loop Order and OSR

Figure 3-1 shows the relationship between maximum dynamic range and OSR for a single-bit modulator. L denotes the modulator order with respect to a lowpass modulator. As described in Section 3.1.1, this thesis uses L to describe the noise-shaping order but 2L to denote the order of the bandpass $\Sigma\Delta$ modulator. As shown in Figure 3-1, a 12-bit resolution can be easily achieved with a first-order noise-shaping loop. However, the presence of idle tones makes this solution undesirable. Examination of a second-order noise-shaping loop ($L = 2$) shows that the desired resolution can be achieved at oversampling rates above 100.

Using Equation 2.4, a sampling frequency of 640kHz and a signal bandwidth of 100Hz will result in an OSR of 3200. This shows that bandpass $\Sigma\Delta$ modulation is advantageous in this situation because the oversampling rate can be increased dramatically using relatively low sampling frequencies without the need to modulate to DC. Similarly, bandpass $\Sigma\Delta$ modulation has greater conversion efficiency over lowpass modulation because bandpass $\Sigma\Delta$ modulation eliminates the need to convert signals from DC to the edge of the baseband.

However, while a high oversampling rate can increase performance by reducing

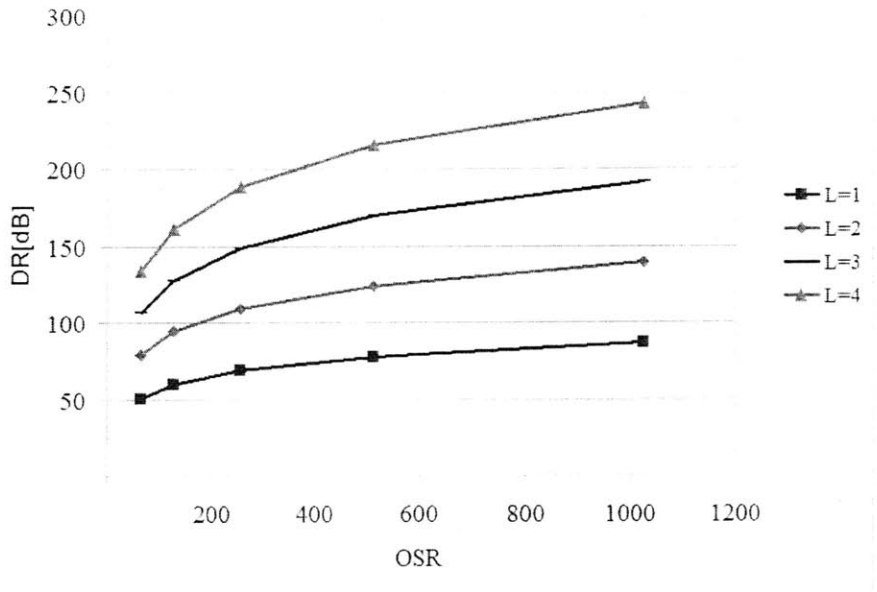


Figure 3-1. The relationship between maximum dynamic range and OSR.

the inband quantization noise, the small width of the resulting NTF stopband is impractical and difficult to achieve with great precision. An OSR of 3200 would result in an NTF stopband width of 100Hz; as will be shown below, the NTF stopband width is determined by the resonators in the forward loop. This narrow bandwidth is difficult to acheive so a lower OSR is chosen to alleviate the necessity for very high-performance resonators while still meeting the given specifications.

A 2nd-order noise-shaping loop ($L = 2$) with an OSR of 200 was chosen to result in a maximum DR of 103dB. This corresponds to a fourth-order bandpass $\Sigma\Delta$ modulator with an NTF stopband width of 1.6kHz. While higher-order modulators can achieve better performance at lower oversampling rates, a fourth-order modulator reduces complexity and increases stability when compared to higher-order loops.

3.1.5 Stability

The stability of $\Sigma\Delta$ modulators depends not only on the linear models presented in Chapter 2 but also on the nonlinear behavior of the quantizer. Linear stability depends on the placement of poles and zeros as determined by the loop filter [2] but is also affected by the gain of the quantizer. As shown in Chapter 2, the gain of

a single-bit quantizer is difficult to precisely define due to the piece-wise behavior of the quantizer. In addition, a quantizer is inherently a nonlinear function. This indicates that the exact stability of the modulator depends on a variable gain and the input signal and no longer follows a linear behavior as predicted by the simplified models [4].

The uncertainty caused by the nonlinear elements indicates that the modulator can be unstable under certain conditions and result in quantizer overload and runaway states. The modulator can be stabilized by constraining the input to the quantizer through limitations on the out-of-band gain of the NTF [1]. According to [1], $|NTF(z)| < 2$ limits quantizer overload and the accumulation of error to stabilize single-bit $\Sigma\Delta$ modulators. The NTF synthesized for this design satisfies this condition by limiting the $|NTF(z)|$ to be less than 1.6 or 4.08 dB:

$$|NTF(z)| < 4.08 \text{ dB} \tag{3.2}$$

3.1.6 Proposed Noise Transfer Function

A MATLAB toolbox [8] was used to generate the NTF given the desired specifications discussed in this chapter. The calculated NTF of the system is shown in Equations 3.3 and plotted in Figure 3-2. The pole/zero plot of the ideal NTF is shown in Figure 3-3. The maximum out-of-band NTF is 4.08dB for stability.

$$NTF = \frac{(z^{-2} - 1.42z^{-1} + 1)(z^{-2} - 1.41z^{-1} + 1)}{(0.438z^{-4} - 1.5z^{-3} + 2.6z^{-2} - 2.28z^{-1} + 1)} \tag{3.3}$$

The sections below describe the realization of the loop topology and discuss the choice of resonators and loop filter architecture.

3.2 Resonators

The following section introduces the need for resonators and analyzes the choice of discrete-time Lossless Discrete Integrator(LDI) resonators. Resonators amplify

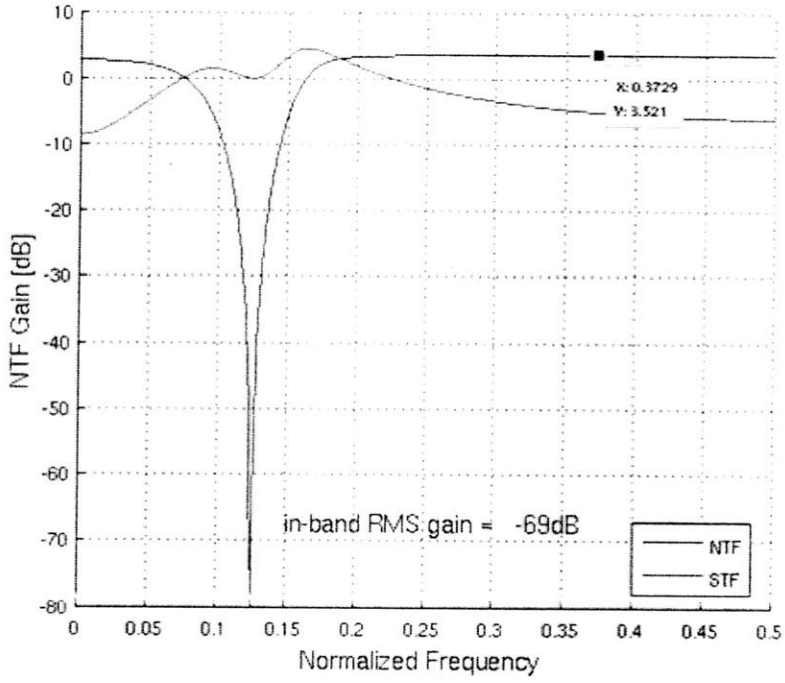


Figure 3-2: NTF and STF of proposed bandpass $\Sigma\Delta$ modulator.

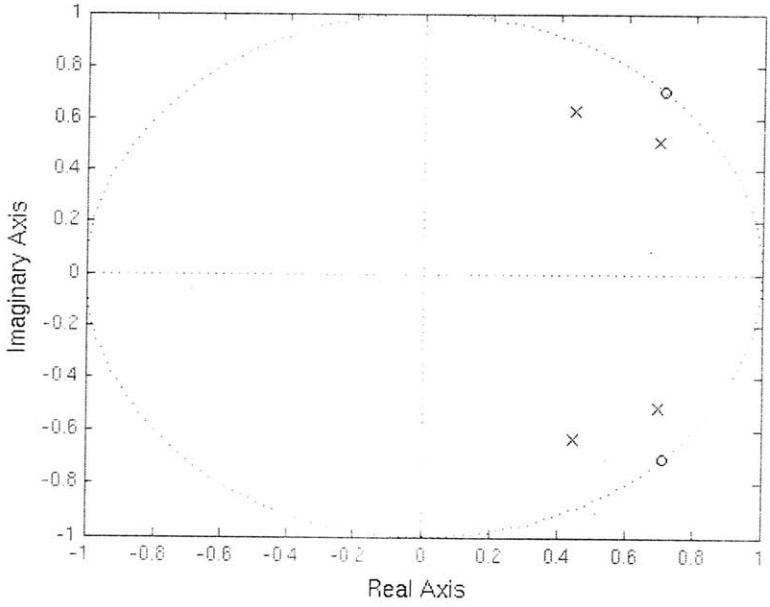


Figure 3-3: P/Z plot of the noise transfer function.

signals within a specific passband and are characterized by Q, the quality of the peak, and the resonant frequency [6]. Bandpass modulators use resonators in place of integrators to create a passband around the carrier frequency. The chosen OSR and sampling frequency indicate that the resonator should have a relatively narrow passband of 1.6kHz; the desired resonator thus requires a high Q-value as well as a fairly accurate resonant frequency. A block diagram of a discrete-time LDI resonator is shown in Figure 3-4.

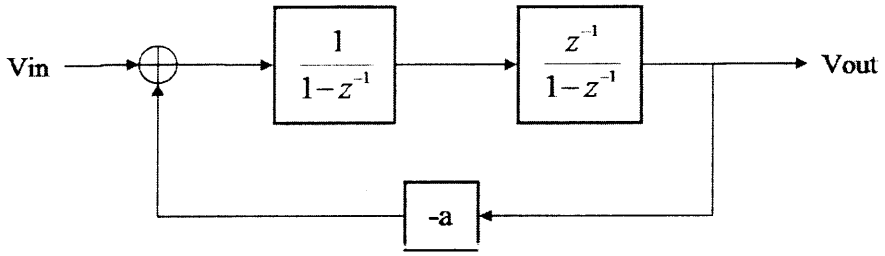


Figure 3-4: Block diagram of LDI resonator.

A resonator has a pair of poles that are responsible for the peak characteristic plotted in Figure 3-6. For discrete-time resonators, the transfer function is represented in Equation 3.4 where r is the magnitude of the poles, ϕ is the resonant frequency, and A is the resonator gain [6]. As shown in [6], the Q-value is mainly dependent on the value of p_2; therefore, r is ideally one for the poles to be placed on the unit circle for a deep notch. The resonant frequency is affected by both poles.

$$H_{res}(z) = \frac{z^{-2}}{1 - 2rcos(\phi)z^{-1} + r^2z^{-2}} = \frac{Az^{-2}}{1 - p_1z^{-1} + p_2z^{-2}} \tag{3.4}$$

The ideal transfer function of an LDI resonator is shown in Equation 3.5. The poles of an ideal LDI resonator can thus be placed directly on the unit circle for maximum notch depth as $r = 1$ for LDI resonators. The parameter a determines the resonant frequency according to Equations 3.6 - 3.7 [6].

$$H_{LDI} = \frac{z^{-1}}{1 + (a-2)z^{-1} + z^{-2}} \tag{3.5}$$

$$(a-2) = -2rcos(\phi) \tag{3.6}$$

$$a = -2rcos(\phi) + 2 \tag{3.7}$$

Deviations from ideal behavior stems from mismatch and amplifier gain for a switched capacitor resonators. Assuming an amplifier error (e), the effect of capacitor mismatch can be seen in Equations 3.8 [6]. The Q-value of the LDI resonator is not affected by gain error but e has a greater effect on the resonant frequency. As shown below, the range of capacitor mismatch does not strongly effect the resonant frequency. Therefore, LDI resonators were chosen to maximize the depth of the NTF notch.

$$H_{LDI} = \frac{(1+e)^2 z^{-1}}{1 - (2 + (1+e)^2 a) z^{-1} + z^{-2}} \tag{3.8}$$

3.2.1 Realized Resonator

The LDI resonators used in the modulator are realized with two amplifiers and a single delay in the forward path. The poles of the resonator are located at $\pm\phi = \frac{\pi}{4}$ to realize a resonant frequency at $\frac{1}{8}$ of the clocking frequency (or sampling frequency). According to Equation 3.7, this results in $a = 0.586$. The pole-zero plot of an ideal LDI resonator is shown in Figure 3-5. The frequency response of a switched-capacitor LDI resonator simulated in ADICE is shown in Figure 3-6. The effects of nonidealities such as capacitor mismatch and amplifier gain are discussed in the following chapter.

3.3 Proposed Loop Topology

The following section discusses the choice of modulator topology using LDI resonators and concludes with the calculated gain coefficients needed to realize the NTF shown in Equation 3.3.

3.3.1 Feedforward Loop Topology

A feedforward topology was used to reduce power consumption by minimizing the amount of signal added back into the feedforward path. The single feedforward path

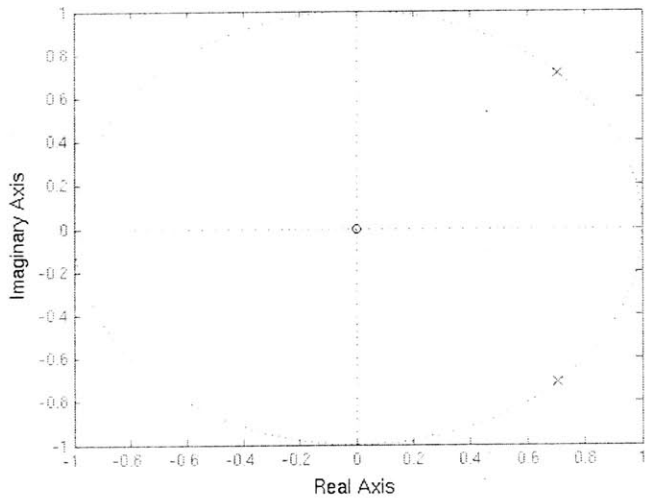


Figure 3-5: Pole/zero plot of discrete time LDI resonator.

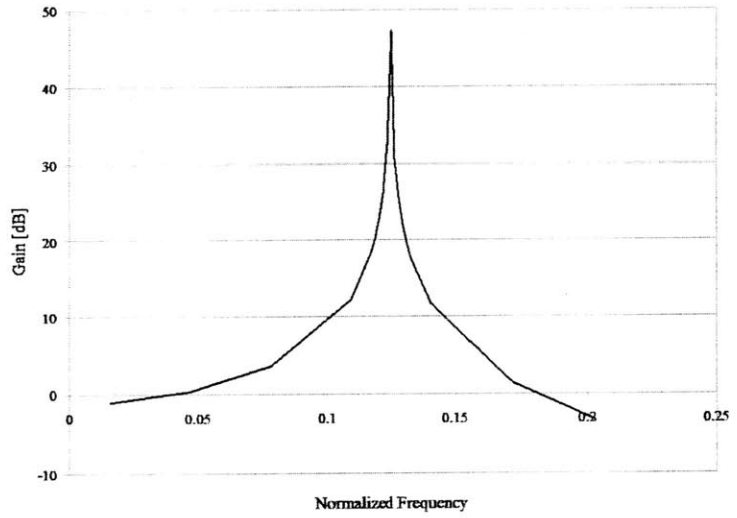


Figure 3-6: Simulated frequency response of implemented LDI resonator.

Table 3.1: Numeric Gain Coefficients

	Original Coefficient	Scaled Coefficient
a1	1	1.67
a2	-0.13	-0.27
c1	0.556	0.336
c2	1	1

is drawn from the output of the first resonator and includes a $1 - z^{-1}$ term to allow the modulator zeros to be placed correctly. However the chosen topology results in a modulator with only 2 independent coefficients for a fourth-order system. While this does not allow full control over the loop, the desired behavior can be achieved with the chosen topology. Increased flexibility of the loop can be achieved by tapping the output of every integrator because the system would have 4 independent coefficients. The proposed modulator topology is shown in Figure 3-7. The calculation of gain coefficients is described in the subsection below.

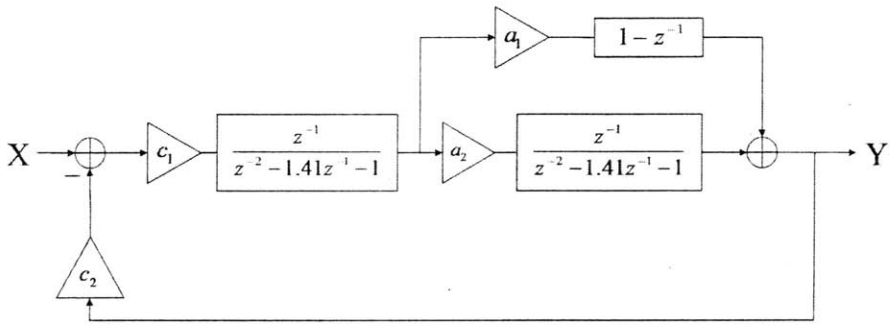


Figure 3-7: Block diagram of proposed $\Sigma\Delta$ bandpass modulator.

3.3.2 Gain Coefficients

Table 3.1 shows the calculated and rescaled coefficients of the modulator. The coefficients were scaled to equalize the outputs of the resonators. In addition, the gain coefficients were rounded during the switched capacitor implementation to allow capacitor sizes to be discretized into scalable units. The relationship of each coefficient to the NTF is shown in Table 3.2.

Table 3.2: Gain Coefficient Equations

Variable	Coefficient
z^{-4}	$1 - c_1 a_1$
z^{-3}	$2(a-2) + c_1 a_1 - c_1 a_1 (a-2)$
z^{-2}	$(1 + (a-2)^2 + 1) + c_1 c_2 a_2 + c_1 a_1 (a-2) - c_1 a_1$
z^{-1}	$2(a-2) + c_1 a_1$
z^0	1

3.4 SIMULINK Results

This section describes results from a SIMULINK model. Simulations of an ideal system resulted in an SQNR of 87dB. Figure 3-8 show the output PSD when nonidealities such as $\frac{kT}{C}$ noise from the input and feedback capacitors and nonideal amplifiers are included. The models simulated noise at 300K with 1pF sampling capacitors.

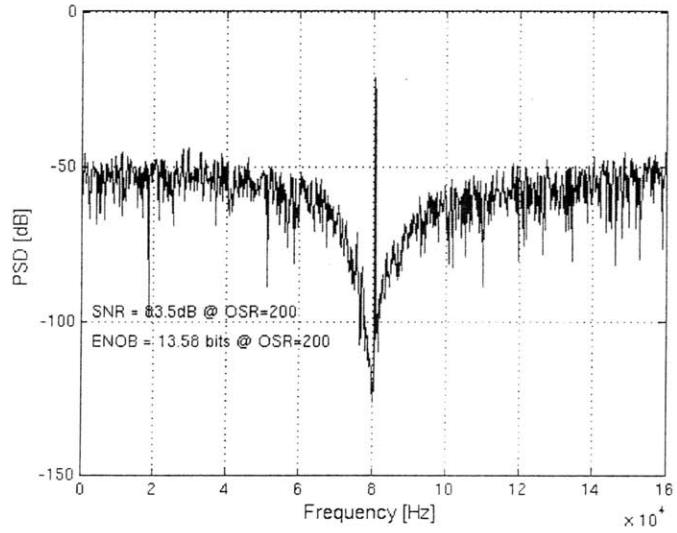


Figure 3-8: Output amplitude of LDI resonators in SIMULINK model.

The final gain coefficients were also shifted to ensure that the output amplitude of signals from each resonator were roughly equal to distribute the signal power. Figure 3-9 shows the range of output signals from both resonators.

The dynamic range of the modulator is shown in Figure 3-10. The modulator has a maximum SNR of 86dB at -2 dbFS. At -6dbFS, the SNR of the modulator is approximately 83dB.

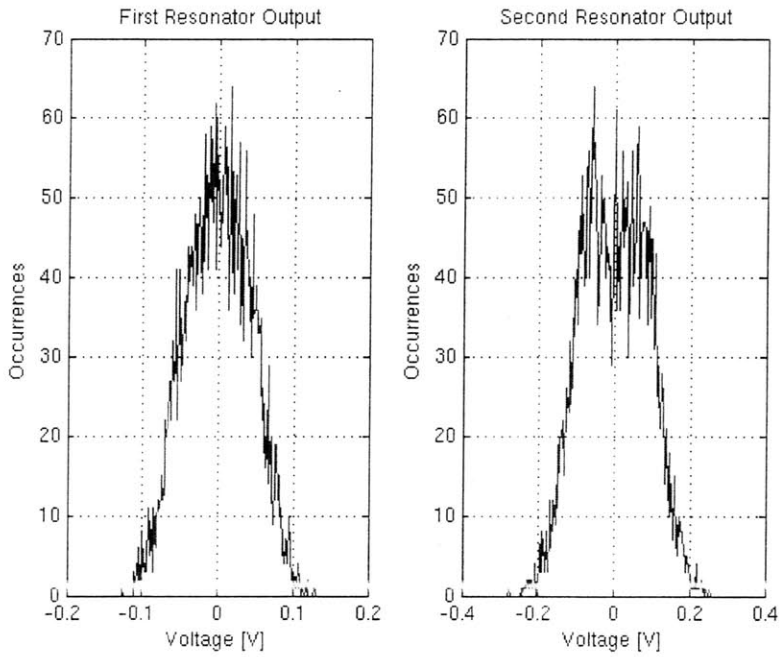


Figure 3-9: Output amplitude of LDI resonators in SIMULINK model.

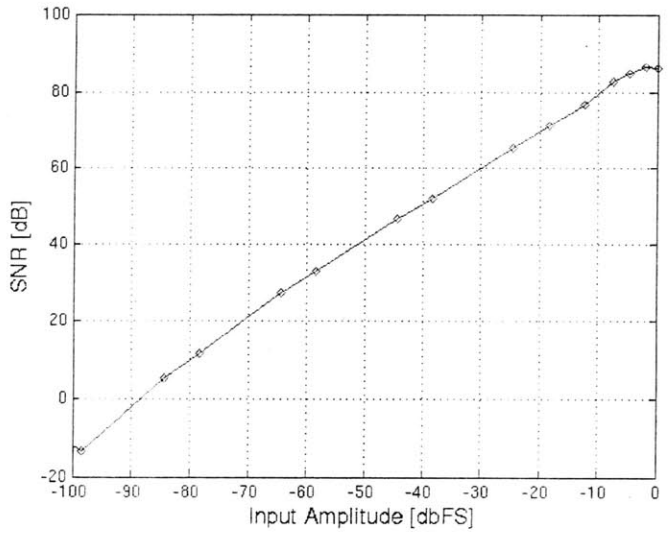


Figure 3-10: SNR vs. Input Amplitude of SIMULINK model.

3.5 Summary

This chapter analyzed the NTF and STF of the proposed discrete time modulator with respect to dynamic range, sampling frequency, and OSR. A feedforward topology using LDI resonators was proposed and simulated in SIMULINK. The following section presents results from behavioral simulations in ADICE.

Chapter 4

Discrete Time $\Sigma\Delta$ Bandpass Modulator Results

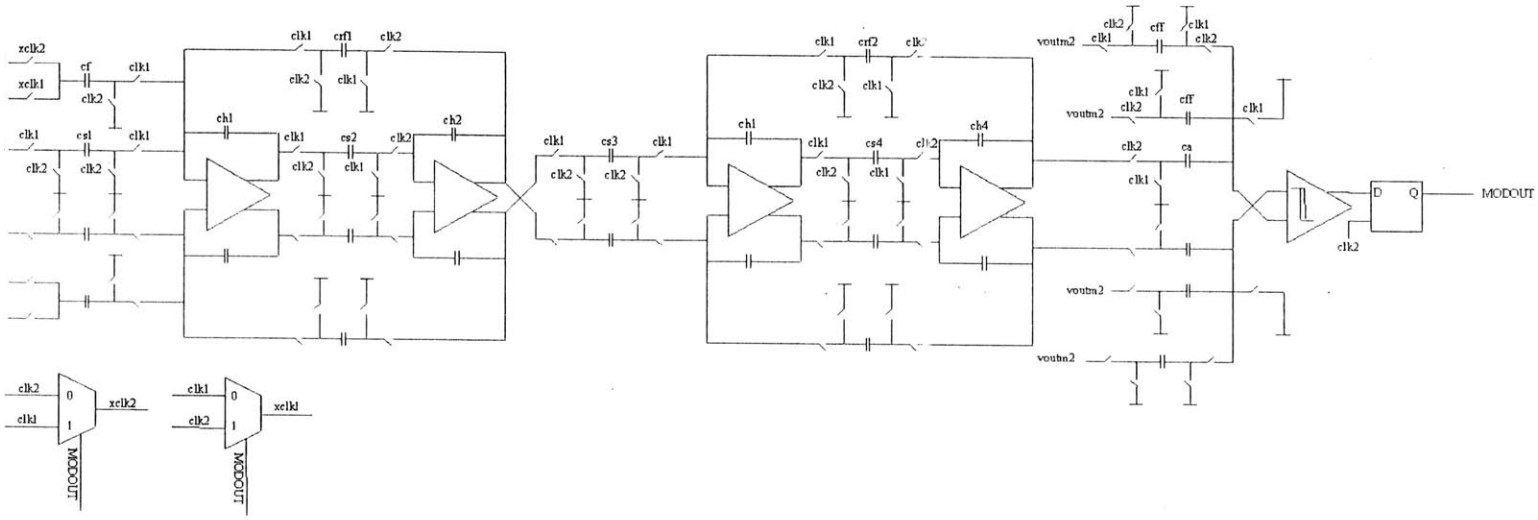
Chapter 4 presents results from a behavioral model simulated in ADICE, a proprietary Analog Devices simulator. The section analyzes the noise sources in the modulators and describes the effect of nonideal resonators.

4.1 Behavioral Model

The behavioral model is presented in Figure 4-1; the switched capacitor circuit is driven by two nonoverlapping clocks, $clk1$ and $clk2$, and uses passive summing nodes. Simulation of the model included switch resistance as well as amplifier limitation such as slew rate and finite gain. The ratio of capacitors that realizes the transfer function is shown in Table 4.1, and the effect of resonator capacitor mismatch is discussed below.

Table 4.1: Modulator Capacitor Ratios

a1	a2	c1	c2
$\frac{cff}{ca}$	$(\frac{cs1}{ch1})(\frac{cs2}{ch2})$	$(\frac{cs3}{ch3})(\frac{cs4}{ch4})$	$\frac{cf}{cs1}$


xclk2
xclk1
cf
clk1
clk2
crf1
ch1
ch2
cs1
cs2
cs3
cs4
crf2
ch4
voutm2
cff
ca
D
Q
MODOUT
xclk2
xclk1
0
1
MODOUT

4.1.1 Quantization and Thermal Noise

As shown in Equation 2.3, the achievable SNR of the modulator depends on the inband noise in the modulator and the anticipated input signal amplitude. While each stage contributes thermal noise, noise from the first stage of the modulator is the least noise-shaped and has the largest impact on SNR. Both switch thermal noise ($\frac{kT}{C}$) and amplifier thermal and flicker noise contribute to the noise in the first stage.

$\frac{kT}{C}$ noise of a switched capacitor circuit results from the series combination of the on-resistance of a switch and the sampling capacitor. The effect of $\frac{kT}{C}$ noise on SNR is largely dependent on the size of the first sampling capacitor; the thermal noise from the first sampling capacitor is injected directly into the first stage and only marginally noise-shaped. Since $\frac{kT}{C}$ noise is inversely proportional to the size of the capacitor, the desired SNR sets a lower bound on the size of the first sampling capacitor. An upper bound is determined by the settling time requirements and area specifications because large capacitors increase the load on the amplifiers and consume more area. The size of the initial capacitor is also dependent on the maximum input amplitude of the signal because the strength of the signal affects the ability to distinguish signal from noise.

Mathematically, the size of the initial sampling capacitor can be calculated by selecting the minimum capacitor size that allows the desired SNR to be reached. Equation 4.1 describes the inband noise of the modulator with respect to the sampling $\frac{kT}{C}$ noise and the power of the input signal is described in Equation 4.2 [5]. As the input amplitude decreases, SNR decreases for a particular sampling capacitor size because the input signal decreases below the noise floor. Figure 4-2 plots the expected SNR for various capacitor sizes given an expected input peak-to-peak amplitude of 150mV.

$$V^2_{inband(RMS)} = \frac{4KT}{C_S OSR} \tag{4.1}$$

$$V^2_{input(RMS)} = \frac{V^2_{FS}}{8} = 0.00281V^2 \tag{4.2}$$

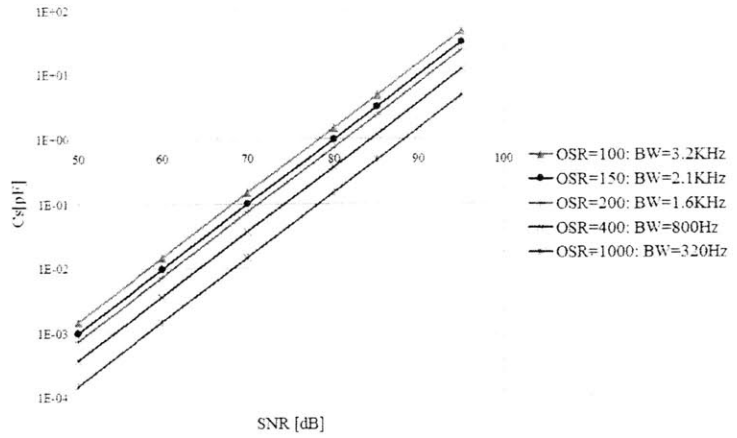


Figure 4-2: Sampling Capacitor vs. SNR

Table 4.2: Noise Contributions

	Inband RMS Noise $[\mu V]$
Quantization Noise	1.88
kT/C Noise	9.1

A sampling capacitor value of 1pF was chosen for an RMS noise of $9.1\mu V$. This value includes the noise contributions from both sampling capacitors of the differential circuit.

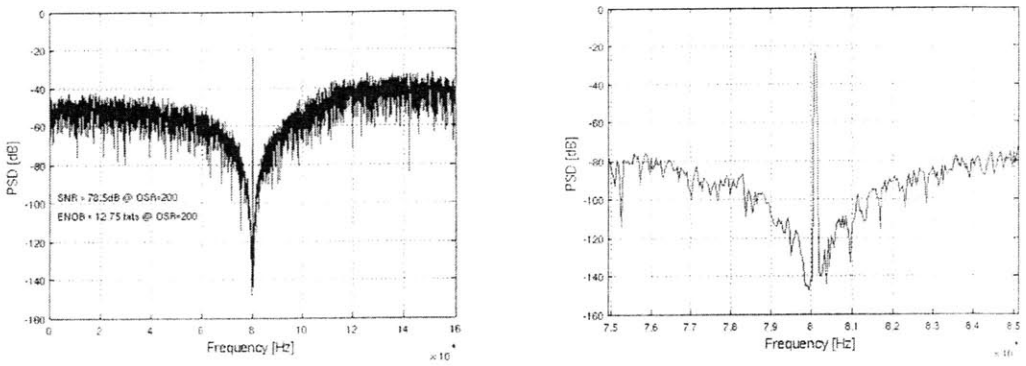
The quantization noise contribution was calculated as follows using an SQNR of 89dB and the input signal power shown in Equation 4.2:

$$SQNR = 10\ log(\frac{V^2_{input(RMS)}}{V^2_{Q(RMS)}}) \tag{4.3}$$

$$V^2_{Q(RMS)} = \frac{V^2_{input(RMS)}}{10^{(\frac{89}{10})}} \tag{4.4}$$

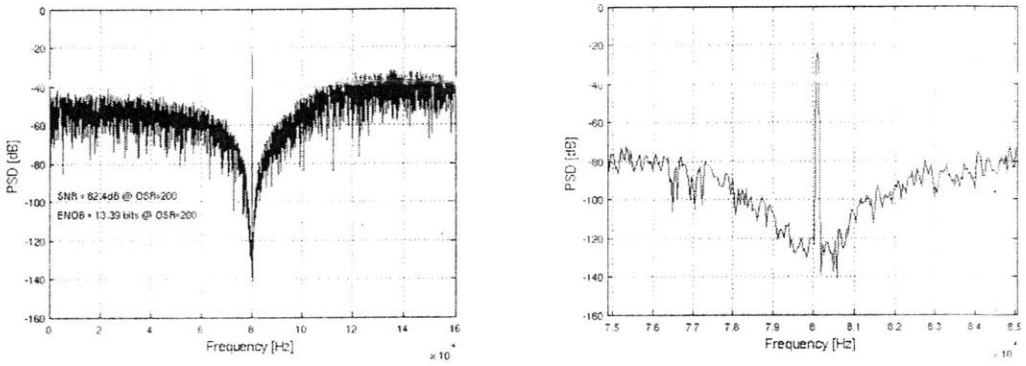
Table 4.1.1 shows the calculated inband noise contributions of the first sampling capacitor and quantization noise. Given the high OSR value chosen, the quantization noise floor is below that of the sampling capacitor. This indicates that noise from the sampling capacitors rather than quantization noise limits the resolution of the modulator.

Figure 4-3 shows the output PSD and notch detail of the proposed modulator. An SNR of 78dB was achieved assuming no capacitor mismatch. An 8192 point



(a) (b)

Figure 4-3: Output PSD of Non-optimized Modulator



(a) (b)

Figure 4-4: Output PSD of Modulator with Optimized Zeros

Hanning window was used. The performance of the modulator can be increased by optimizing the zeros of the NTF to decrease inband RMS gain. In a bandpass modulator, this corresponds to adjusting the notches of each resonator as shown in Figure 4-4. Rather than placing both resonator notches at the same frequency, optimization of zeros widens the NTF stopband notch by placing each resonator notch at a different frequency within the desired bandwidth. Comparison of the notches in Figures 4-3 and 4-4 shows that optimizing zeros decreases the depth of the notch at the carrier frequency (80kHz) but also decreases the average inband gain. In Figure 4-4(b), the stopband notch is both flatter and wider than the corresponding notch in Figure 4-3(b). Optimizing zeros results in a 4dB increase in SNR to 82dB.

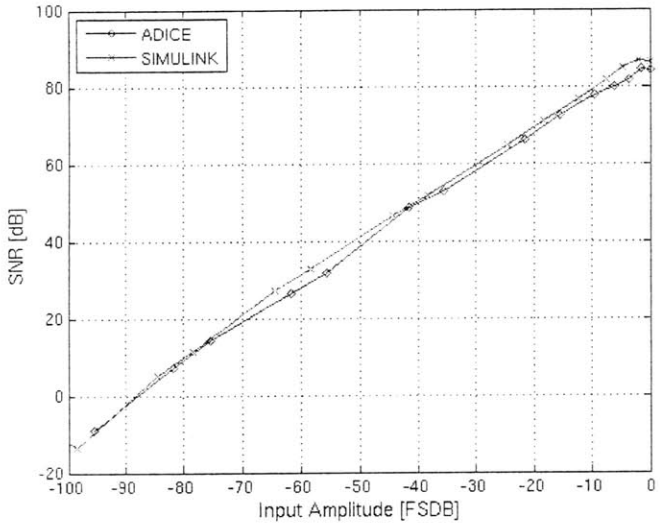


Figure 4-5: SNR vs. Input Amplitude

Table 4.3: LDI Resonator Capacitor Ratios

	Gain	a
Capacitor Ratio	$(\frac{cs1}{ch1})(\frac{cs2}{ch2})$	$(\frac{cs2}{ch2})(\frac{crf}{ch1})$

Figure 4-5 plots the SNR with respect to input amplitude using a modulator with optimized zeros and compares the results from SIMULINK and ADICE. The modulator has a max SNR of approximately 85dB at -3dBFS and a dynamic range of 85dB.

4.2 Effect of Resonator Capacitor Mismatch and Finite Amplifier Gain

Capacitor mismatch in the resonator affects the notch frequency and Q-value of the resonator and is dependent on the amplifier gain. The ratios of capacitors that represent the gain and notch frequency of the resonator are shown in Table 4.3. As calculated in Chapter 3, a notch frequency that is $\frac{1}{8}$ of the sampling frequency is satisfied by $a = 0.586$.

Figure 4-6 shows the effect of capacitor mismatch on the notch frequency. $\pm 1\%$

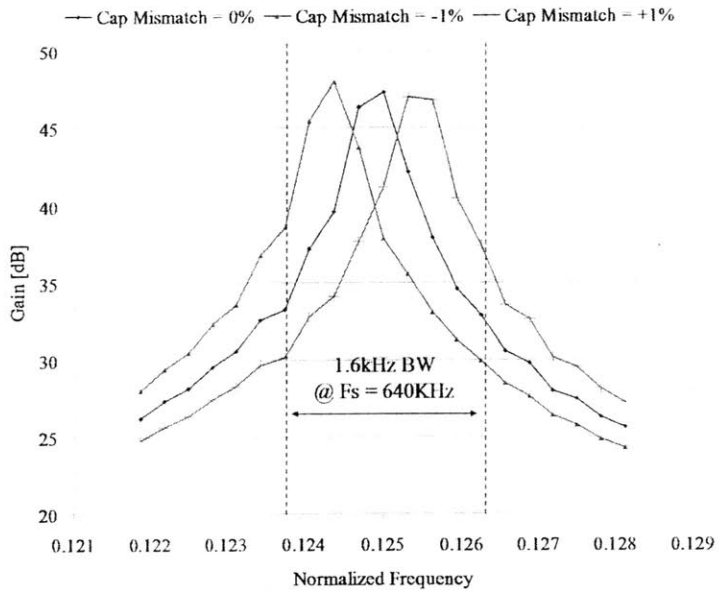


Figure 4-6: Effect of Capacitor Mismatch on Notch Frequency

capacitor mismatches were approximated by assuming a 1% error in the value of crf; an amplifier gain of 60dB was used during simulations. The notch frequency of the resonator moves a considerable amount given the simulated mismatch but the notch stays within the 1.6kHz band. This displacement of resonator notches, however, affects the SNR of the modulator as shown in Figure 4-7.

The decrease in SNR can be attributed to an increase in NTF inband RMS gain. As shown in Figure 4-7, the capacitor ratios must show less than 0.5% mismatch to realize the desired SNR. Figures 4-8 and 4-9 show the output PSD of simulations with mismatched capacitors; SNRs of 71dB and 72dB were achieved, respectively. The details of the notches show that although the notch frequency of the resonators are within the desired 1.6kHz bandwidth, the inband RMS gain increases and causes the SNR to decrease.

The accuracy of the switched capacitor modulator is also dependent on the gain of the amplifiers within the resonators. High gain amplifiers reduce error in charge to aid the achievable resolution of the modulator. The decrease in resonator notch gain as amplifier gain decreases is shown in Figure 4-10.

Figure 4-11 shows the output of the modulator when all amplifiers have a gain of

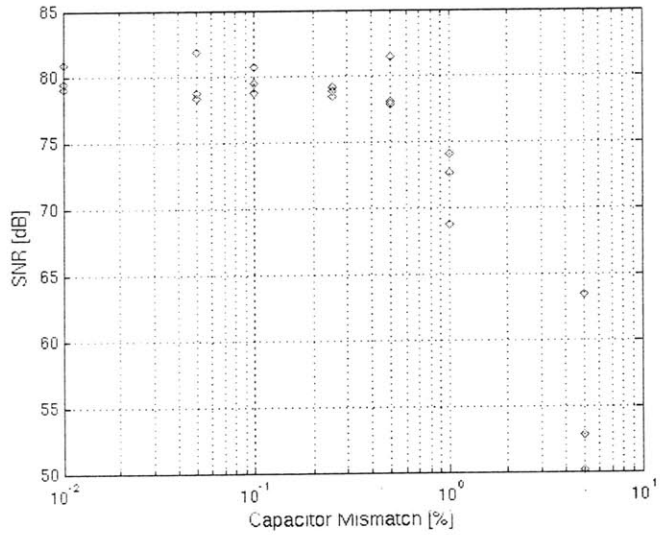
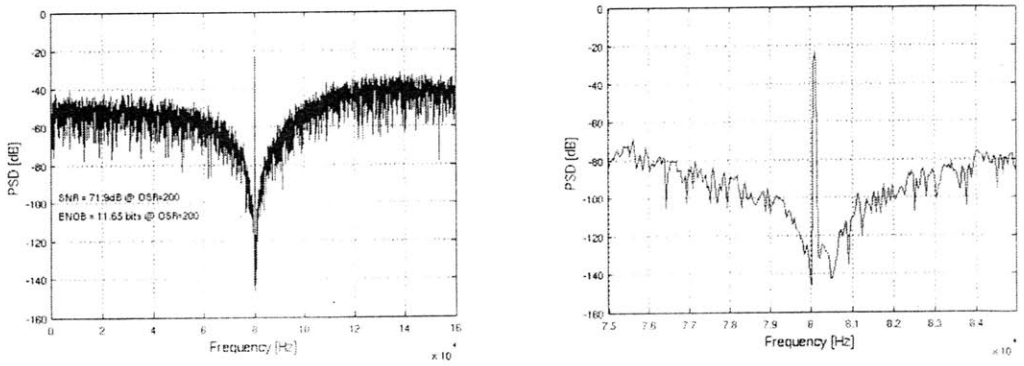
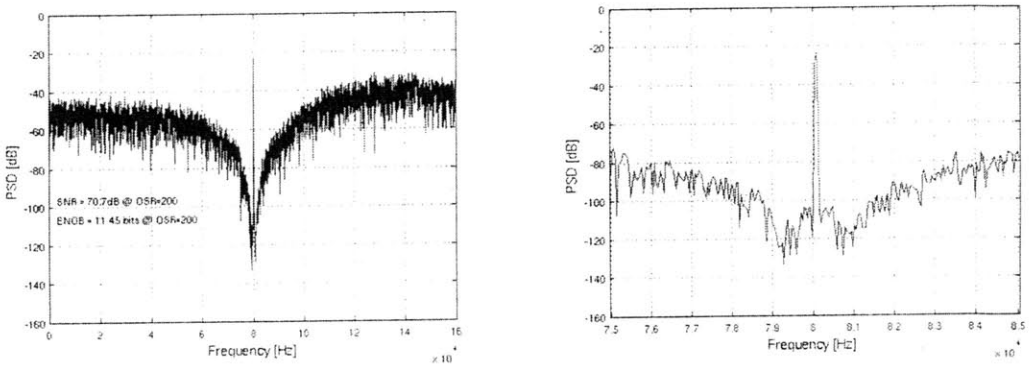


Figure 4-7: Effect of resonator capacitor mismatch on SNR.



(a) (b)

Figure 4-8: Output PSD of Modulator with Resonator Capacitor Mismatch



(a) (b)

Figure 4-9: Output PSD of Modulator with Resonator Capacitor Mismatch

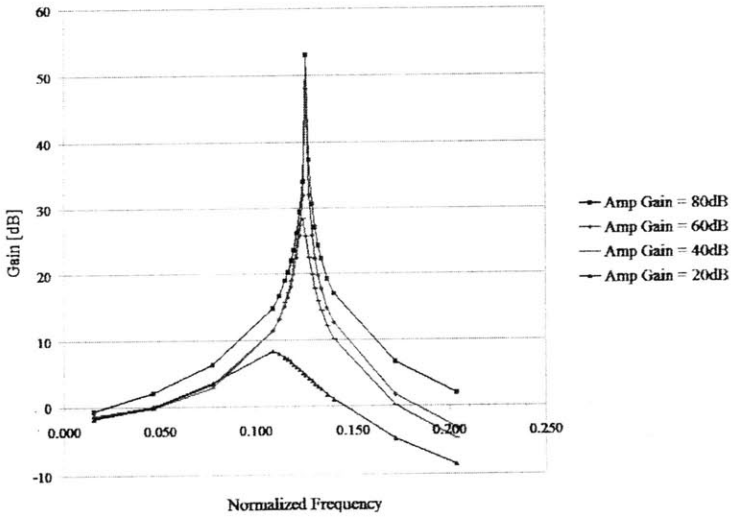


Figure 4-10: Effect of Amplifier Gain on Notch Depth

40dB; the notch is essentially filled in and the SNR drops to 59dB. As shown in Figure 4-12, the amplifiers in the modulator must have gains of at least 60dB to achieve the desired resolution.

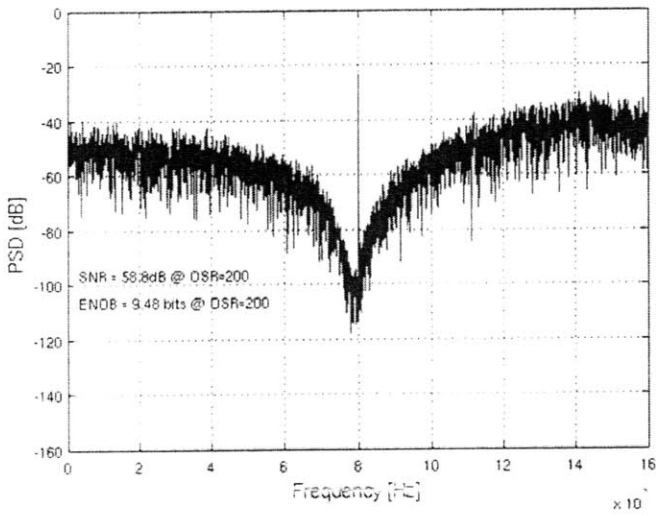


Figure 4-11: Output PSD where Amplifier Gain is 40dB

4.3 Summary

This chapter presented the parameters used to construct a behavioral model of the modulator and ADICE simulation results. The modulator achieves an SNR of 82dB and a dynamic range of 85dB with optimized zeros.

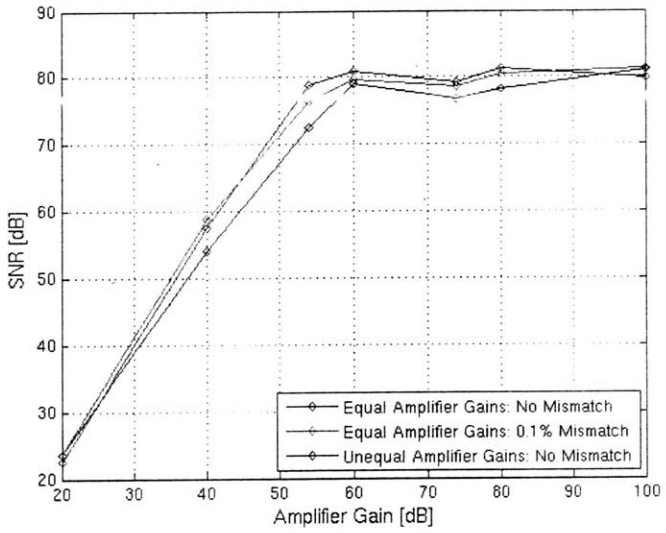


Figure 4-12: Effect of amplifier gain on SNR.

Chapter 5

Conclusion and Future Work

A fourth-order bandpass $\Sigma\Delta$ modulator was presented. The 100Hz-wide input signal modulated up to a carrier frequency of 80kHz can be converted by a bandpass modulator without the need to demodulate the signal to DC. However, in contrast to the relative ease with which switched capacitor integrators can be constructed, resonators increase the complexity of bandpass modulation and are more difficult to construct robustly. The proposed modulator thus traded simplicity for power and efficiency. An optimized modulator achieves an SNR of 82dB at half full scale and has a dynamic range over 80dB.

Further work should investigate the decoupling of gain coefficients in the modulator [11] as mentioned in Chapter 3. Full controllability over the loop can potentially eliminate the dip in the STF passband and smooth the gain in this region. This would require shifting the zeros in the feedforward path but can help performance by increasing the signal strength passed through the modulator. Independent coefficients can potentially be obtained by tapping the output of each integrator.

In addition, analog implementation of the modulator should carefully consider the flicker and thermal noise of the amplifiers. Since the LDI resonators use two amplifiers, a greater power and noise budget should be given to the first resonator because the noise of the first stage is minimally shaped. Pre-amplification of the input signal should also be investigated; this will ease the requirements on the initial sampling capacitor while easing noise specifications on the circuit components.

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