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*Fully monolithic cellular buck converter
design for 3-D power delivery*

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cycle, where $\lceil \dots \lceil \lceil N/r \rceil / r \rceil \dots / r \rceil = \lceil N/r^n \rceil = 1$. Then from $N/r^n \leq \lceil N/r^n \rceil = 1$, we have $N/r^n \leq 1 \Rightarrow n \geq \log_r N$.

If $0 < N/r^{n-1} \leq 1$, then $\lceil N/r^{n-1} \rceil = 1$. This means only $n - 1$ cycles are needed and this contradicts our original assumption that n cycles are required. Therefore, $N/r^{n-1} > 1 \Rightarrow n < \log_r N + 1$ and $\log_r N \leq n < \log_r N + 1$, so that

$$n = \lceil \log_r N \rceil. \quad (6)$$

This represents the exact time complexity of the i th channel of the residue arithmetic process shown in Fig. 5. Because all the N channels run in parallel, $\lceil \log_r N \rceil$ is also the exact time complexity of the scaling scheme constructed on r -input LUTs.

It can also be proven that the exact space complexity of each channel is $\lceil (N - 1/r - 1) \rceil$ such that the exact space complexity of the whole arithmetic process is $N \lceil (N - 1/r - 1) \rceil$, which is at the level of $O(N^2)$.

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Fully Monolithic Cellular Buck Converter Design for 3-D Power Delivery

Jian Sun, David Giuliano, Siddharth Devarajan, Jian-Qiang Lu, T. Paul Chow, and Ronald J. Gutmann

Abstract—A fully monolithic interleaved buck dc-dc point-of-load (PoL) converter has been designed and fabricated in a 0.18-mm SiGe BiCMOS process. Target application of the design is 3-D power delivery for future microprocessors, in which the PoL converter will be vertically integrated with the processor using wafer-level 3-D interconnect technologies. Advantages of 3-D power delivery over conventional discrete voltage regulator modules (VRMs) are discussed. The prototype design, using two interleaved buck converter cells each operating at 200 MHz switching frequency and delivering 500 mA output current, is discussed with a focus on the converter power stage and control loop to highlight the tradeoffs unique to such high-frequency, monolithic designs. Measured steady-state and dynamic responses of the fabricated prototype are presented to demonstrate the ability of such monolithic converters to meet the power delivery requirements of future processors.

Index Terms—3-D integration, dc-to-dc converters, monolithic power conversion, power delivery, power management, voltage regulator.

I. INTRODUCTION

FUTURE microprocessors and high-performance integrated circuits (ICs) will require multiple, dynamically scalable, sub-1-V supply voltages with total current exceeding 100 A/chip [1]. Conventional power delivery methods employing a voltage regulator module (VRM) mounted on the motherboard have several limitations in meeting future IC technology needs. One critical problem of this 2-D power delivery architecture is the long interconnect between the VRM and the processor, which creates an impedance bottleneck for dynamic power delivery and forces the use of decoupling capacitors at various locations along the power delivery path. Another problem of 2-D power delivery is the large number of power and ground pins required by the processor, which consumes expensive board area around the processor and/or increases packaging complexity. Meeting the power delivery requirements of future microprocessors and high-performance ICs requires a paradigm shift in power delivery system design and integration.

3-D power delivery [2]–[5], in which the power supply is vertically integrated with the processor in a 3-D stack, offers a possible solution to the problems of 2-D power delivery by dramatically reducing the interconnect parasitics. In addition, this ultimate point-of-load (PoL) converter configuration reduces the number of power pins and facilitates the delivery of multiple supply voltages. Of the different 3-D architectures discussed in the literature, the wafer-level 3-D approach proposed

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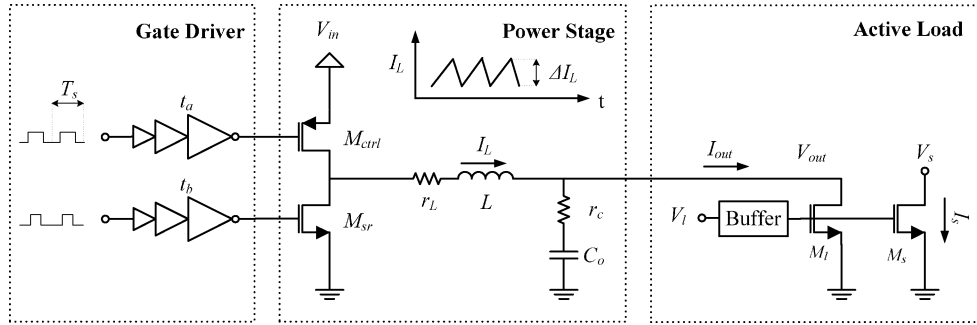


Fig. 2. Circuit diagram of a buck converter cell. The fabricated prototype uses two such cells operating in parallel.

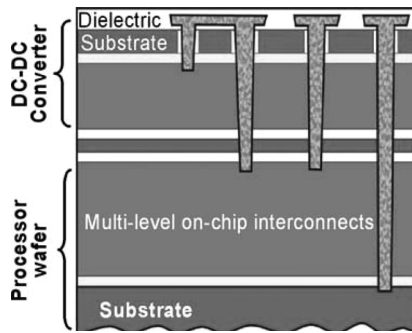


Fig. 1. Schematic representation of 3-D power delivery to microprocessor using wafer-to-wafer bonding.

in [5] and depicted in Fig. 1 has the advantage of having the least interconnect parasitics as well as low cost in high quantity production and high reliability due to monolithic IC-type interconnectivity.

To facilitate 3-D integration with the processor by wafer-to-wafer bonding, the footprint of the power supply must be comparable to that of the processor. Additionally, since only very limited amount of filtering capacitance can be incorporated in a 3-D package, the power supply must also be able to meet dynamic load regulation requirements without requiring large filter capacitance. Conventional dc-dc converter design using discrete active and passive components and operating up to a few megahertz switching frequency cannot meet these power density and control requirements.

One approach to achieving high power density and wide control bandwidth required by 3-D power delivery is to design the dc-dc converter in submicron CMOS processes where the MOSFET can be operated at much higher switching frequencies than what is possible with discrete power MOSFETs. To demonstrate the feasibility and performance of such monolithic dc-dc converters for 3-D power delivery, we report here a fully integrated, two-cell interleaved buck dc-dc converter with linear feedback control in a 0.18- μm SiGe BiCMOS process. The converter operates at a switching frequency near 200 MHz, and achieved a control bandwidth of about 10 MHz. All passives, including the inductors and output filter capacitors, are monolithically integrated with the power switches and control circuitry. A SiGe BiCMOS process was selected because of its enhanced passive components compared to Si CMOS processes available to us.

II. POWER STAGE DESIGN

A simplified circuit diagram of the buck converter power stage, including the gate drivers, control switch (M_{ctrl}), synchronous rectifier (M_{sr}), output filter inductor (L), and capacitor (C), and internal active load, is shown in Fig. 2. To simplify drive circuit design, the converter uses a pMOS as the high-side control switch and an nMOS as

the low-side synchronous rectifier. A tapered gate driver is used to drive the MOSFETs. The fabricated prototype includes two such converter cells operating in parallel. Each cell is designed to convert 1.8 V input to 0.9 V with a nominal output current of 500 mA. The nominal input voltage level was selected based on future power delivery system architecture as well as the device breakdown voltage in the CMOS process used to fabricate the prototype. The output current rating was chosen to make the design a common building block which can be duplicated in a cellular architecture to meet different load requirements.

The primary objective of the power stage design is to minimize power loss so as to maximize the conversion efficiency. The main sources of power loss in a monolithic buck converter are MOSFET conduction and switching losses, gate drive losses, and filter inductor losses. Optimal conversion efficiency requires careful design and selection of these components as well as the operation frequency, as discussed in the following. Power losses of monolithic capacitors can be neglected because of their very low equivalent series resistances (ESR).

To limit the size of on-chip inductors and capacitors, a switching frequency in the range of 200 MHz was targeted. With this switching frequency, sizing of the controlled switch and synchronous rectifier involves a tradeoff between static conduction losses and dynamic switching losses. The optimal MOSFET width, W_{opt} , and the corresponding power loss, P_{min} , for a target rms current (i_{rms}), and switching frequency (f_s) are defined by the following expressions [7], where R_0 is the equivalent on-state resistance of a 1- μm -wide MOSFET, and E is the energy consumed by such a unit-size MOSFET during a full switching cycle

$$W_{opt} = i_{rms} \sqrt{\frac{R_0}{f_s E}}, \quad P_{min} = 2i_{rms} \sqrt{R_0 f_s E}. \quad (1)$$

Based on device parameters of the 0.18- μm SiGe BiCMOS process used to fabricate the design, the pMOS control switch was designed to have an equivalent width of 16.6 μm , with an on-resistance of 152 m Ω , while the nMOS synchronous rectifier has an equivalent width of 11 μm and an on-resistance of 62 m Ω . The tapered gate drivers for both the control switch and synchronous rectifier have the same tapering factor of 9.

An air-core spiral inductor with two shunted metal layers was selected from the SiGe foundry library to implement the on-chip filter inductor L . Dimensions of the inductor were chosen to minimize the resistance of the inductor; namely the width of the spiral tracks was maximized (25 μm) while the track spacing was minimized (5 μm). The number of turns was chosen to be 3.5 to give an inductance of 2.14 nH, resulting in an outer diameter of 290 μm . The dc resistance of the winding was determined to be 201 m Ω . In addition, a patterned

TABLE I
PARAMETERS OF KEY POWER STAGE COMPONENTS

Components	Design Parameters	Equivalent Resistance
Control Switch	Width = 16.6 mm	$R_{DS(ON)} = 152 \text{ m}\Omega$
Syn. Rectifier	Width = 11 mm	$R_{DS(ON)} = 62 \text{ m}\Omega$
Inductor	$L = 2.14 \text{ nH}$	$R_{DC} = 201 \text{ m}\Omega$
Capacitor	$C = 8.22 \text{ nF}$	$R_{ESR} = 1 \text{ m}\Omega$

metal ground plane was used under the inductor to reduce capacitive substrate losses and boost Q_{max} by approximately 30% [7].

The output capacitor has 8.22 nF capacitance and 1 m Ω ESR, and is implemented by MOS capacitors since they have a larger capacitance per area than MIM or PIP capacitors. Table I summarizes the parameters of major power stage components.

Since the primary objective of the design was to provide a prototype for performance evaluation, an on-chip active load was included as part of the power stage design to allow generation of fast transient load currents to emulate loading of the converter by a microprocessor or high-performance application-specific integrated circuit (ASIC). The active load is a large MOSFET operating in the saturation region and acting as a current sink. A current buffer is used to drive the MOSFET such that fast load transients (10–100 A/ μ s) can be generated, as shown in Fig. 2. One drawback of an on-chip load is that all the power into the chip must also be dissipated on die; thus, the power level is limited by packaging thermal considerations.

III. COMPENSATOR AND CONTROL LOOP DESIGN

Control designs for on-chip dc-dc converters based on hysteretic [8] and peak-current control [9] have been reported in the literature. Both methods are nonlinear and avoid the need for a separate pulse-width modulator (PWM). However, hysteretic control cannot be synchronized and is not suitable for applications where the operation of multiple converter cells needs to be coordinated (e.g., interleaved as in our design.) Peak-current control can be interleaved and also ensures equal current sharing among parallel cells. However, dynamic response of peak-current control to load current changes is slower than that under voltage-mode control with the same control bandwidth [10]. Considering these, a voltage-mode control was selected. The lack of automatic current balancing capability of this control can be solved by adding a current sharing control loop which can be much slower than the voltage loop and, hence, is much easier to implement.

To maximize control bandwidth, a voltage feedback loop is typically closed at a frequency above the power stage resonant frequency. However, since our power stage design uses very small inductors and capacitors, placing the loop crossover frequency above the resonant frequency will make the loop difficult to stabilize. Therefore, we placed the loop crossover frequency at 10 MHz with a phase margin of 95°. This relatively conservative design for a 200 MHz converter still provides sufficient bandwidth for the control of the output voltage, as will be demonstrated in Section IV.

A compensator is traditionally implemented using an operational amplifier (op amp) in an inverting configuration, with two complex impedances realized using capacitors and resistors. This approach works well at low frequencies where the op amp can be treated as an ideal component, but is not suitable for high-speed compensators where the inherent poles and zeros of the op amp are close to the required external poles and zeros. An integral design approach is employed in our design to realize the required compensator transfer function.

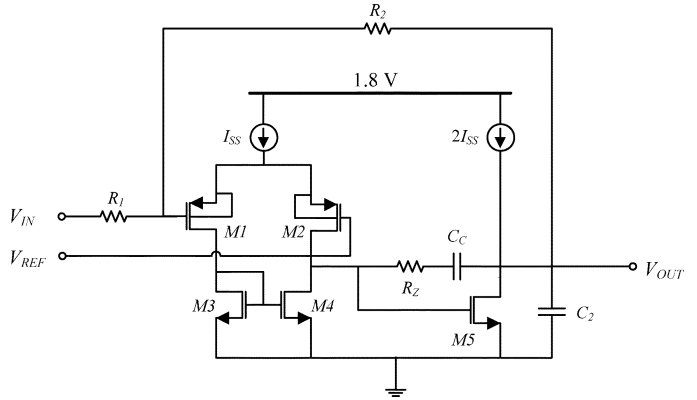


Fig. 3. Simplified diagram of the compensator design.

Fig. 3 shows a simplified diagram of the implemented voltage compensator. The locations of the poles and zeroes (in radians per second) of this circuit are defined by the following expressions where C_1 is the internal capacitance at the output of the first stage of the op amp (differential pair):

$$\omega_Z = \frac{1}{C_C(g_{M5}^{-1} - R_Z)} \quad (2)$$

$$\omega_{P1} \approx \frac{1}{(1 - g_{M5}R_Z)C_C R_1} \quad (3)$$

$$\omega_{P2} \approx \frac{-g_{M5}C_C}{C_1 C_2 + C_C(C_1 + C_2)}. \quad (4)$$

In order to realize the designed compensator transfer function, a compensation capacitor (C_C) of 66 pF, a feed-through resistor (R_Z) of 84 Ω , and a load capacitor (C_2) of 8 pF were chosen. A gain of 36 dB is set by resistors R_1 and R_2 , yielding a steady-state error of 12 mV. Since the output impedance of the op amp is 1.4 k Ω , R_2 must be larger to prevent loading; R_1 and R_2 were chosen to be 1 and 100 k Ω , respectively.

The control circuitry also includes a high-speed pulse-width modulator and an active dead-time controller. The modulator employs a high-gain (52 dB) comparator designed by cascading numerous high-speed low gain stages. The dead time between the control switch and the synchronous rectifier is controlled by a series of inverters and NOR gates. A more detailed description is provided elsewhere [11].

IV. FABRICATED PROTOTYPE AND PERFORMANCE

A two-cell interleaved buck converter based on the designs discussed in the previous sections has been implemented in a 0.18 μ m SiGe BiCMOS process. The power stage design was duplicated to give the two cells, while a common control loop (including pulse-width modulator and dead-time controller) is used for controlling both cells. The gate control signals for the two cells are shifted from each other by half a switching cycle to achieve maximal ripple cancellation at the combined output [13]. Fig. 4 shows a micrograph of the fabricated prototype.

The total area of the fabricated chip is about 10 mm², including input/output pads and test vias, as well as on-chip active loads for dynamic response testing. A breakdown of the total area by components and functions is given in Table II. As can be seen, most of the area is taken by the capacitors (57.9%), with the output capacitors occupying 27.1% and the input decoupling capacitors taking up 30.8% of the total area. Input decoupling capacitors are needed to filter out the discontinuous input current so as to limit the di/dt-related voltage generated

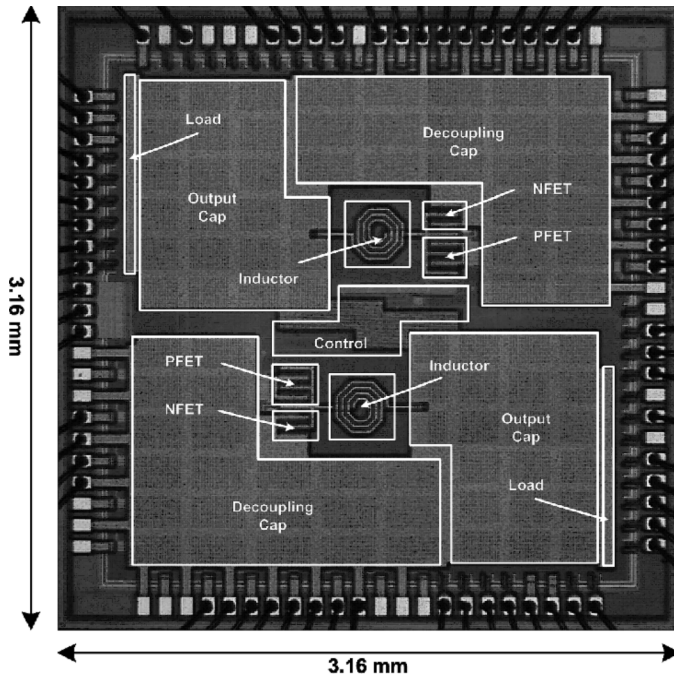


Fig. 4. Micrograph of the prototype buck converter test chip.

TABLE II
CHIP AREA BREAKDOWN OF THE FABRICATED PROTOTYPE

Components	Area (mm ²)
Input Decoupling Capacitors	3.08
Output Capacitors	2.71
All Other Components Combined	1.07
Bond Pads and ESR	3.14

through the parasitic inductance between the input voltage source and the prototype chip.

Operation of the fabricated converter chips was measured to evaluate their steady-state as well as dynamic performance. The second converter cell contains probe pads which significantly degraded converter performance; therefore, only one-cell performance has been fully characterized and reported in the following.

Fig. 5 shows the measured efficiency of the converter under different switching frequencies and load conditions. The efficiency is relatively independent of the switching frequency from 160 to 220 MHz, with a modest decrease with output current. A maximal efficiency of 64% is achieved at 200 MHz with an output current of 500 mA.

The output voltage transient response to a step-up in the load current is shown in Fig. 6, with a current step of 225 mA and slew rate of 10 A/ μ s. The voltage shows an overshoot of approximately 88 mV, and returns to the desired level in 86 ns. The output voltage drops approximately 6 mV at the higher current due to the relatively small dc gain of the compensator (34 dB). Response to a step-down of the load current is similar. Overall, the prototype converter was able to respond to a current transient with a slew rate of 10 A/ μ s while keeping the output voltage within a window of approximately 225 mV.

V. SUMMARY AND OUTLOOK

Fully monolithic dc-dc converters compatible with the 3-D integration platform are capable of meeting power delivery requirements

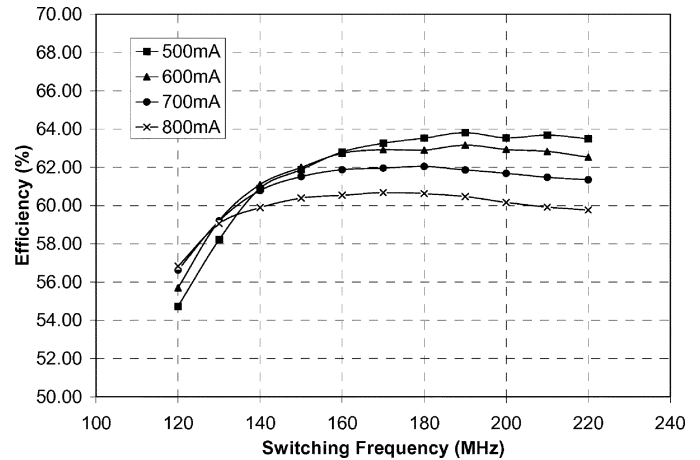


Fig. 5. Prototype chip efficiency measurement under variable load conditions and switching frequency.

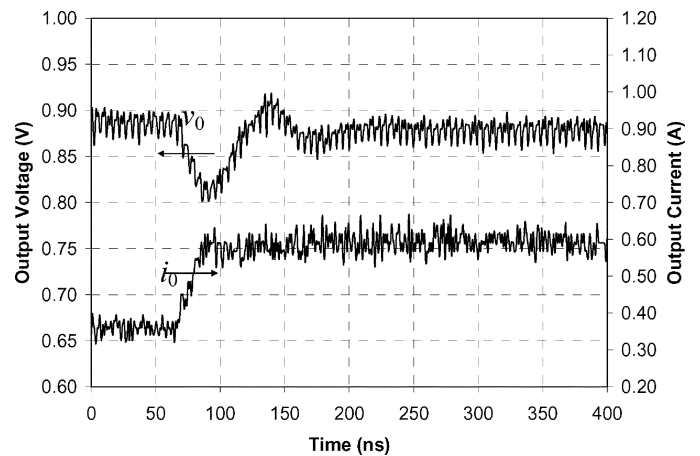


Fig. 6. Output voltage transient response to a load current step of 225 mA at a slew rate of 10 A/ μ s.

of future microprocessors and high-performance ASICs. The high switching frequency allows the use of small, on-chip filter inductors and capacitors while still meeting steady-state and dynamic voltage regulation requirements. The proposed cellular converter architecture enables full utilization of the benefits of interleaving to reduce both input and output filtering requirements, and is ideally suited for 3-D integration.

Several issues require further studies in order to bring the proposed technology into practical application. Efficiency of the monolithic converter needs to be improved, possibly through the use of a separate passive layer in the 3-D stack where more efficient inductors could be implemented by incorporating ferromagnetic materials. Scaling of the design to supply the full current required by a microprocessor will require a large number of parallel cells, which provides an opportunity to significantly reduce, by means of interleaving [13], the chip area occupied by input and output capacitors, but may also necessitate the addition of a current sharing control loop. The overall packaging scheme including thermal management for the 3-D stack also needs to be further developed.

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