Nucleation and Solidification of Silicon for Photovoltaics

by

Anjuli T. Appapillai

Submitted to the Department of Mechanical Engineering
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Mechanical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 2010
[June 2010]

Author .....
Department of Mechanical Engineering
May 19, 2010

Certified by .....
Emanuel M. Sachs
Professor, Mechanical Engineering
Thesis Supervisor

Accepted by .....
David E. Hardt
Chairman, Department Committee on Graduate Students

Nucleation and Solidification of Silicon for Photovoltaics

by

Anjuli T. Appapillai

Submitted to the Department of Mechanical Engineering
on May 19, 2010, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy in Mechanical Engineering

Abstract

The majority of solar cells produced today are made with crystalline silicon wafers, which are typically manufactured by growing a large piece of silicon and then sawing it into ~200 μm wafers, a process which converts one-half of the high-purity silicon into waste sawdust. To bypass the sawing process, a new method for making high-quality multicrystalline wafers without sawing is under development. This method begins with a poorly-structured silicon wafer made by a low-cost method which is then coated by a thin film capsule. The encapsulated wafer is zone-melted and recrystallized, thus improving the crystal structure for a higher-efficiency solar cell without material waste.

This work develops the wafer recrystallization process by gaining insight on three major areas, motivated by the need to increase recrystallized grain size and control thermal gradients. First, a novel method for measuring the temperature field in the wafer within the high-temperature zone-melt furnace is designed and demonstrated. Knowledge of the temperature gradients experienced by the wafer is important to improve the furnace design to minimize the thermal stress and resulting dislocation density in the recrystallizing silicon.

Secondly, a thermal model was created to determine the shape of the crystal-melt interface during recrystallization as a function of processing parameters such as wafer travel speed and thickness, because the orientation of the solidification interface dictates the direction of grain growth and the subsequent grain boundary orientation, which affects solar cell performance. A threshold wafer travel speed was found, above which the crystal-melt interface becomes non-planar and grain boundaries will form at the mid-wafer plane.

Lastly, to evaluate different wafer capsule materials, nucleation behavior of molten silicon on various materials was studied through differential scanning calorimetry. The level of undercooling reached by molten silicon in contact with variations of silicon nitride and oxide was evaluated and the optimal capsule configuration was determined; this configuration was demonstrated to improve recrystallized wafer structure. These insights gained from this work will inform future design decisions in tailoring the crystal structure for optimal solar cell performance.

Thesis committee members:
Samuel Allen, Professor, Materials Science Engineering, MIT
Tonio Buonassisi, Assistant Professor, Mechanical Engineering, MIT

Thesis Supervisor: Emanuel M. Sachs
Title: Professor, Mechanical Engineering

Acknowledgments

I would first like to thank my advisor, Professor Ely Sachs, for his guidance and wisdom throughout this thesis, and for encouraging me to think beyond the science while giving me space to try my own ideas. I'd also like to thank my committee members, Prof. Sam Allen and Prof. Tonio Buonassisi, for their support and expertise.

I am extremely grateful for the technical, intellectual, and moral support of my co-workers in the Sachs group past and present, especially collaborators on the wafer-making project: Eerik Hantsoo, Dr. Christoph Sachs, Chris Ruggiero, Jim Serdy, and Alison Greenlee. Thanks for being my sounding boards, my extra hands, my coffee break buddies. Special thanks also to Dr. Jim Bredt, Amine Berrada, and Laura Zaganjori for their support. I'd like to thank Damian Harris for depositing beautiful layers of silicon nitride on numerous samples, and Aaron Gawlik for lending his expertise in circuit design and signal processing. I'm also grateful to Tony Yu for many enlightening discussions of solidification modeling.

I would also like to acknowledge the Department of Energy for funding this project. This material is based upon work supported by the Department of Energy under Award Number DE-FG36-08GO18008. The generous support of Mr. Douglas Spreng is also gratefully acknowledged.

I could never have survived graduate school if not for the support of my friends and teammates. I thank my officemates in 35-135 for their moral support and comedic relief, as well as other friends in the LMP and the Mechanical Engineering community who really enriched my experience at MIT. Huge thanks to my teammates on the MIT Women's Ice Hockey team, the MIT Rowing Club, and LMP basketball for keeping me sane.

Finally, I am grateful to my parents for encouraging me to strive for excellence from day one, and to my college sweetheart, James Wright, for his support and for his willingness to weather six New England winters with me.

Contents

List of Figures

List of Tables

[THIS PAGE INTENTIONALLY LEFT BLANK]

Chapter 1

Introduction

1.1 The Potential of Solar Power

The need for renewable energy sources has increased dramatically over the last decade. According to 2008 reports, fossil fuels provide $\sim$ 84% of the world's energy [2], but the international community is increasingly looking for alternative energy sources that lack the harmful CO_2 production and reliance on a finite fuel supply. Solar photovoltaics are a promising alternative source of energy but currently supply less than one-tenth of one percent of the world's energy consumption [2]. Approximately 124,000 TW of the sun's radiation reaches the earth's surface [16], several orders of magnitude higher than the world's energy consumption, reported at 16.2 TW for the year 2007 [2]. If even a fraction of that radiation could be harvested through photovoltaics, it could provide a substantial amount of renewable energy for the world. The main barrier for increased usage of photovoltaics is its high cost compared to fossil fuel energy sources, but research and development efforts to improve cell efficiencies and lower costs have already contributed to an increase in photovoltaic production of an order of magnitude between 1998 and 2007, and further gains are expected in the future [1]. The current average price of photovoltaics is near $\$3/W_p$, and this price

must drop to less than $\$1/W_p$ in order to be competitive with fossil fuels [1, 10].

While thin-film solar technologies have been growing since the late 1990s, silicon-based solar cells, dubbed "first generation," still dominate the photovoltaics market with 67% of the market share in 2008 [1]. In order to keep up with the growing thin-film sector, silicon-based photovoltaics producers strive to improve effiencies, reduce the amount of silicon used, and decrease manufacturing costs [1]. Almost half of the silicon-based production is made up of multicrystalline silicon technologies, including cast and ribbon Si [1]. As shown in Figure 1-1, a significant fraction of the cost of manufacturing a multicrystalline silicon-based solar module comes from making the silicon wafer. This step in the manufacturing process represents a promising area for cost reduction of the module.

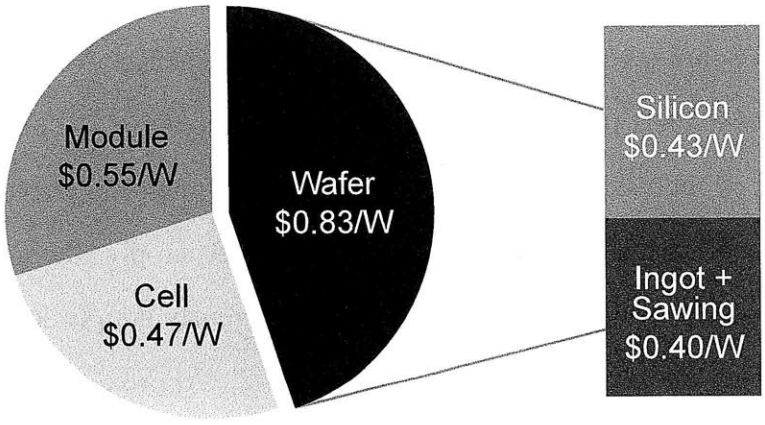
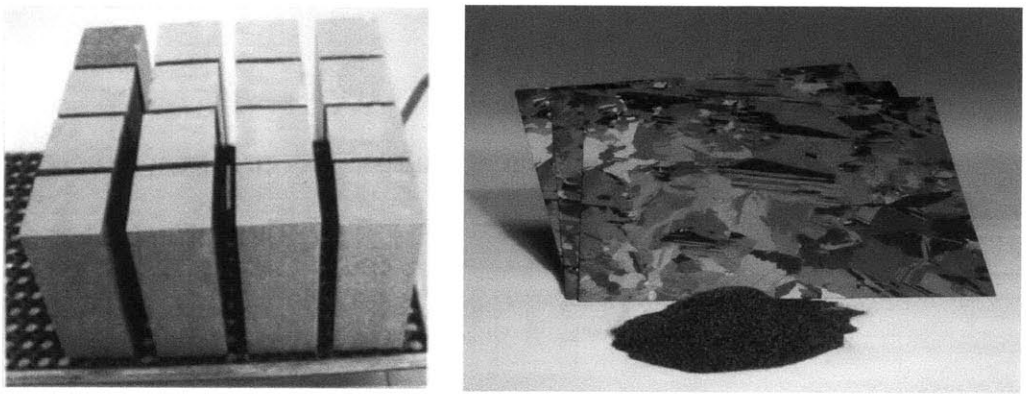


Figure 1-1: Cost breakdown of multicrystalline silicon photovoltaics manufacturing, average projected costs for 2010, with assumed average silicon prices of \$60/kg. [10]

1.2 Bulk Multicrystalline Silicon Wafers

Bulk multicrystalline silicon wafers are traditionally manufactured by casting and directional solidification, having gained popularity during the 1970s for their reduced cost and complexity in production compared to Czochralski and float-zone techniques for making monocrystalline silicon [4]. In the block-casting process, silicon is melted

and poured into a silicon-nitride-coated quartz crucible, where it undergoes directional solidification from the bottom as heater settings are adjusted to cool the block. Similarly, directional solidification in the Bridgman process is done in the same type of crucible, but the entire crucible is moved into and out of a hot zone to melt and resolidify the silicon from the bottom up [9]. The Si_3N_4 coating is needed as a release layer for the silicon to prevent sticking to the crucible, since the different coefficients of thermal expansion of silicon and quartz would cause breakage of the crucible upon cooling. Both methods result in columnar vertical grains in a silicon block of >300 kg.



(a) Cast multicrystalline silicon.

(b) Multicrystalline wafers with equivalent quantity of silicon dust waste.

Figure 1-2: Cast multicrystalline silicon wafer manufacturing.

Silicon blocks must be cut into ingots and then sawed into wafers, a process which typically wastes 50% of the high-purity silicon as dust [9]. Figure 1-2(b) shows a number of silicon wafers and the equivalent quantity of Si dust that was wasted in sawing them from a block. In the multi-saw process, shown schematically in Figure 1-3, ingots are cut by a stainless steel wire with a silicon carbide powder slurry which abrasively cuts through the thickness of the ingot. Besides kerf losses, the slurry and wires are not reusable and add to the total cost of sawing. Saw damage must be removed by etching wafer surfaces before solar cells can be made. These drawbacks to the cast multicrystalline wafer-making process have led many researchers to develop

methods which circumvent the sawing process altogether.

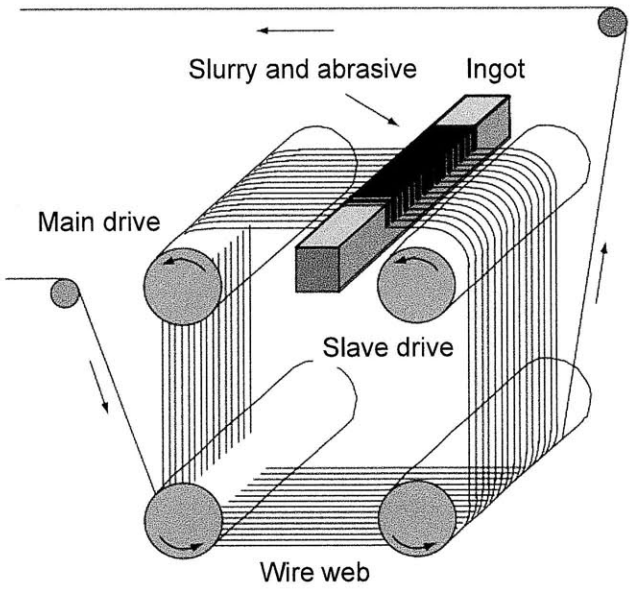
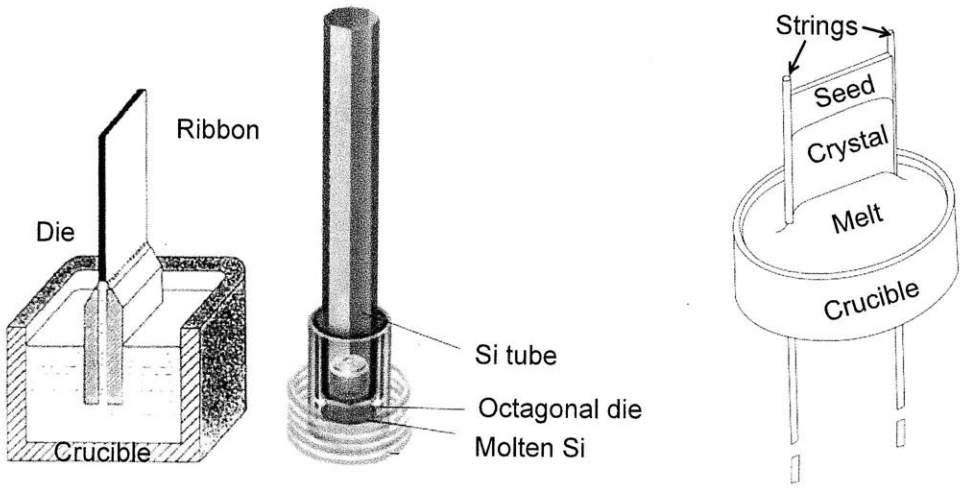


Figure 1-3: Schematic representation of multi-sawing process. [9]

1.3 Silicon Ribbon Technologies

Development of silicon ribbon manufacturing processes began in the 1970's and gained needed momentum in the 1990's [9]. Vertical growth techniques that have reached the production stage include Edge-defined Film-fed Growth (EFG) and String Ribbon. In these processes, the solidification interface moves parallel to the pull direction of the ribbon from the melt, and the latent heat of fusion is removed from the interface by conduction through the silicon, which radiates the heat to the environment. Crystal pull speeds are on the order of 20 mm/min, requiring high thermal gradients at the solidification interface which lead to thermal stresses and resultant dislocations [11]. Wafers grown by these methods often have a large number of twinning defects and high dislocation densities due to the large thermal gradient changes the silicon must go through to drop from the melting point to room temperature [3]. In addition, the wavy texture of the ribbon surface can often be challenging for processing steps in creation of the photovoltaic cell.

In the EFG process, an octagonal tube of silicon is pulled from the melt through a graphite die, shown schematically in Figures 1-4(a), creating eight panels of 10-12 cm width and $\sim$ 300 μm thickness. Graphite from the crucible and die typically dissolves into the molten silicon, causing erosion of the crucible over time. Similarly, the String Ribbon process also pulls a long ribbon of silicon from the melt, supported by two silicon carbide strings which pass through the melt. A meniscus forms between the two strings, and thermal control of the solidification interface is less stringent compared to the EFG process, allowing for more cost-effective furnace designs [6]. The String Ribbon process was commercialized by Evergreen Solar Inc., where multiple ribbons are now grown simultaneously to increase throughput [15]. However, concentrations of carbon from the string material, high internal stress and dislocation densities due to thermal gradients, and limited pull speeds are still major challenges for further improvement of this technique.



(a) Edge-defined Film-fed Growth. (b) String ribbon growth.

Figure 1-4: Schematic representation of ribbon growth processes [9].

Another category of ribbon growth method utilizes a crystal growth interface which moves perpendicular to the ribbon pull direction, referred to as horizontal growth methods. The primary example of this approach is the Ribbon-Growth on Substrate (RGS) method [8]. In this process, shown schematically in Figure 1-5, a shaping die filled with molten silicon sits on a moving "cold" substrate such that the silicon is cast onto the substrate and solidifies in a thin ribbon. Heat is extracted by conduction through the substrate, which allows for much faster wafer pull speeds than the vertical ribbon methods previously mentioned. RGS pull speeds are on the order of 6000 mm/min [6]. During cooling, the substrate is ideally released from the crystal and could be reused. In reality, achieving a clean release from the substrate is very challenging, as silicon is highly reactive when molten [13]. In addition, this method yields much smaller grain size than vertical methods, on the order of millimeters rather than centimeters, due to the nucleation of new grains on the substrate during solidification. Thermal stress should be much lower due to temperature gradients existing primarily through the thickness of the wafer, but in practice, dislocation densities are still higher than EFG and String Ribbon wafers, indicating that these gradients are challenging to control [6]. RGS wafers typically

have a very high concentration of oxygen and carbon as well, reducing their suitability for solar cells with competitive efficiency.

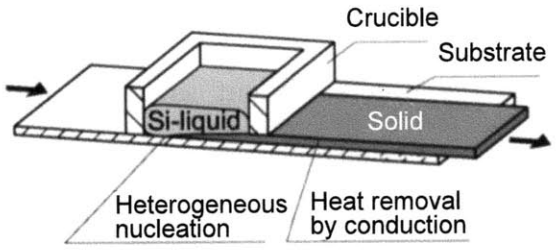


Figure 1-5: Schematic representation of Ribbon-Growth on Substrate (RGS) process.

Other approaches for making ribbon-like geometries have been researched. The Silicon on Dust Substrate (SDS) method is a two-step process developed by Serra et al. [14]. In the first step, silicon is deposited from high-purity silane gas by chemical vapor deposition onto a substrate of silicon dust, forming a nanocrystalline ribbon which is detached from the substrate. Next, the ribbon undergoes free-standing zone-melt recrystallization in a vertical elliptical-mirror furnace to form mm-wide vertical grains [14]. However, this configuration has similar heat transfer characteristics to the String Ribbon approach, where temperature gradients typically create problematic dislocation densities.

The advantage to these ribbon growth methods is that they do not require sawing of an ingot into wafers, therefore making better use of the expensive, high-purity silicon. However, they still face challenges in terms of minimizing impurities incorporated during high-surface-area growth processes, controlling thermal gradients to minimize dislocation densities, and balancing a high growth rate with crystal quality and uniformity. In the following section, a new approach to manufacturing high-quality wafers without sawing is described.

1.4 High-Quality Multicrystalline Wafers Without Sawing

Our novel approach for making multicrystalline wafers without sawing is shown schematically in Figure 1-6. The important feature in this process is the decoupling of the wafer geometry creation and the crystallization to produce good electronic properties. This process begins with a wafer of low crystal quality, created by a low-cost, high-throughput process such as rapid solidification. The wafer is then coated with a thin film capsule which can be deposited or thermally grown. Next, the encapsulated wafer is sandwiched between two silicon carbide backing plates and this wafer assembly is passed through a zone-melt furnace to recrystallize the wafer. The heat of crystallization is transferred away from the solidification interface both through the solid silicon and through the backing plates, which radiate to the surroundings. The thin film capsule, which has maintained the silicon in its wafer form during recrystallization, is now chemically etched away to reveal a multicrystalline wafer with increased grain size and lower dislocation density. The use of backing plates allows increased control over the heat transfer behavior around the recrystallizing wafer, and the thin film capsule prevents sticking to the plates and also reduces in-diffusion of impurities.

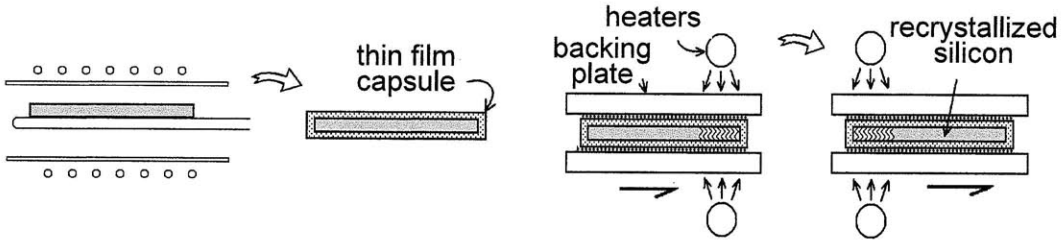


Figure 1-6: Schematic representation of zone-melt recrystallization of multicrystalline wafers without sawing.

Preliminary studies have shown the validity of this concept, producing recrystallized wafers with a completely changed grain structure from the original wafer [7].

Capsules made of 1-μm thermal SiO_2 layers are easily grown on the silicon surface in a 1000°C furnace and then etched away in a dilute hydrofluoric acid solution after recrystallization.The presence of the backing plates, which can be made of either solid silicon carbide or SiC-coated graphite, helps to maintain the flatness of the wafer surface, since molten silicon has a high surface tension and tends to bead up when unconstrained [5]. Because liquid silicon has a higher density than solid silicon, the recrystallization upon exiting the furnace hot zone is also accompanied by a volume increase, which often leads to small volumes of silicon bursting through the capsule layer at the trailing end of the wafer. The capsule otherwise remains continuous throughout the process. An example of a wafer before and after recrystallization is shown in Figure 1-7. Elongated grains in the pull direction are clearly visible, and some level of similarity is seen between the top and bottom grain structures.

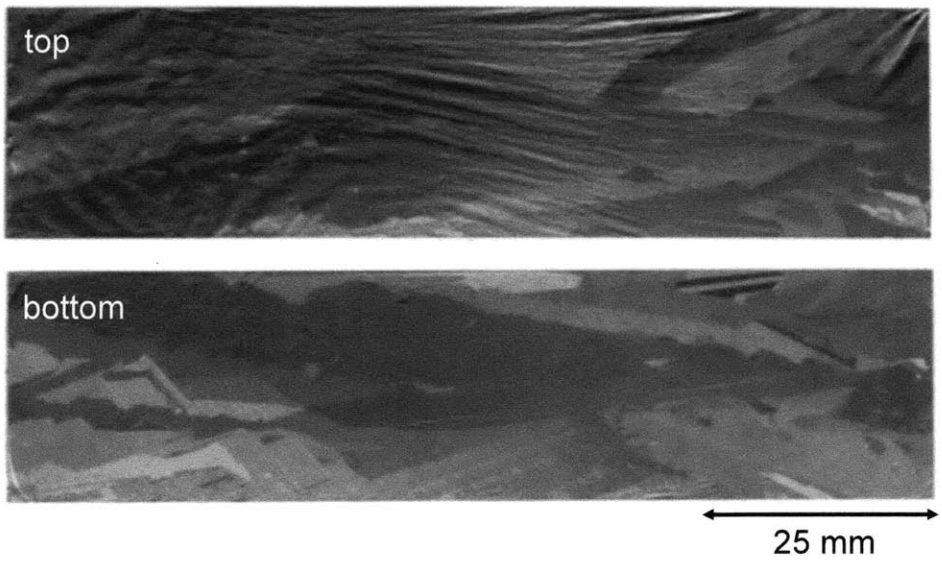


Figure 1-7: Multicrystalline wafer after encapsulation and zone-recrystallization, with capsule removed and texture-etched to reveal grain structure. Right side of wafer was the leading edge in the zone-melt furnace. (Image courtesy Christoph Sachs.)

The recrystallization furnace used in this process is a custom-designed in-house-built furnace of high purity materials. A photograph of the furnace with the top insulation blocks removed is shown in Figure 1-8. Six parallel heater elements are

arrange in two horizontal rows, between which the wafer is passed, to create the hot zone. These heater elements, which are spaced 25mm apart, are resistively heated in pairs (left, middle, and right) and their temperatures are controlled with the feedback of three two-color pyrometers which monitor the temperature of the top row of elements. Thus differently shaped hot zones can be created by adjusting the temperatures of the different heater pairs. Two parallel Hexoloy bars are shown passing through the center of the furnace, and the wafer assembly rests on these bars during zone-recrystallization. The slider bar movement is motor-driven and samples are typically pulled through the hot zone at a speed of ~10 mm/min. Furnace walls are made from SiC-based porous insulation blocks to minimize proximity of metal impurity sources. The recrystallization process is run in air, which has two major advantages. First, no costly gas supply and furnace seals are needed to create an artificial gaseous environment, and secondly, the oxygen content of air acts to oxidize the silicon should any discontinuities be created in the oxide capsule.

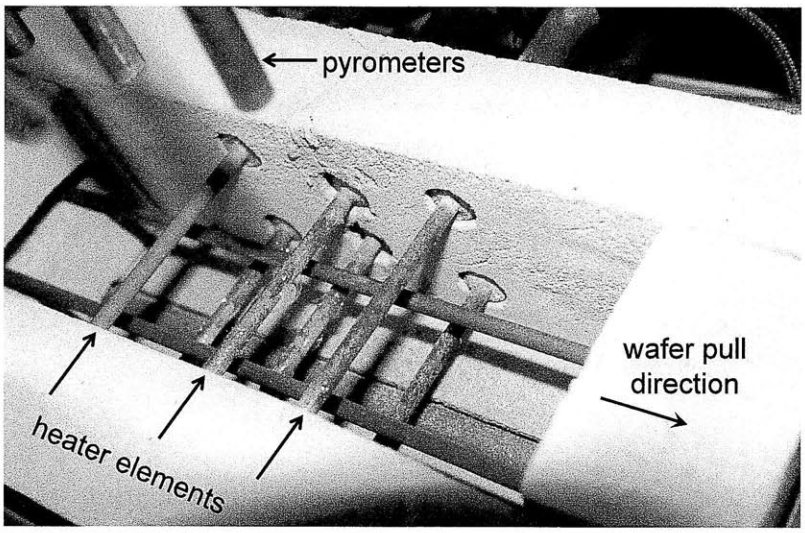


Figure 1-8: Photograph of high-purity zone-recrystallization furnace with top insulation removed.

After preliminary results and research [7], a few challenges remained in producing silicon wafers with competitive electronic properties and suitable geometric proper-

ties for solar cell manufacturing. One area for improvement was the nonuniformity in the wafer thickness and surface texture of the recrystallized wafer. Because silicon expands upon freezing and the oxide capsule is not rigid at silicon's melting temperature, wafers became thicker as the solidification front approached the trailing edge, and the capsule became wrinkled, as shown in Figure 1-7. Some work was done to find solutions to this geometry-control challenge by studying various backing plate configurations and capsule supports [12].

Preliminary wafers also showed relatively high dislocation densities [7], which is a result of the temperature field the recrystallized wafer experiences while exiting the hot zone. In order to improve and optimize the temperature gradients of the wafer, a more precise knowledge of the hot zone shape and size was needed. In this thesis, I describe a novel method for characterization of a two-dimensional temperature profile seen by a wafer, between two backing plates, in the furnace hot zone. This technique can be used to measure the temperature profile of any thin wafer or silicon film, without high-complexity auxiliary apparati or perturbation of the existing heat flows in a high-temperature environment. This method is described in Chapter 2.

The electronic properties of the wafer depend on both the dislocation density and the grain structure. Both of these characteristics are affected by the shape of the solidification interface across the thickness of the wafer. Because the typical wafer thickness is $\sim$200 μm and temperatures are near the silicon melting point of 1420°C, it is difficult to measure in-situ or characterize subsequently the shape of the recrystallization interface during the process. A crystal-melt interface which creates grain boundaries parallel to the plane of the wafer will degrade the performance of the final solar cell, and excessive temperature gradients will lead to thermal stresses and increased dislocations, which also contribute to carrier recombination. To improve understanding of the factors that affect the shape of this interface, I created a thermal model to find the equilibrium interface shape for different wafer travel conditions.

This model is described in Chapter 3.

Because this recrystallization technique relies on zone melting of the wafer, the manner in which the silicon resolidifies is critical to the final grain structure. Specifically, high nucleation rates at the wafer edges and where molten silicon contacts the capsule will lead to smaller grains and lower electronic quality. This nucleation behavior depends on the properties of the capsule material surrounding the molten silicon, and whether the interfacial energy between molten silicon and the capsule creates a driving force for nucleation that is larger than that of silicon solidifying on the already-solid region of the wafer after the molten zone. Growth of the existing grains that first nucleated at the leading edge of the wafer is desirable over nucleation of new grains along the length of the wafer, in order to produce elongated grains with fewer grain boundaries. In order to characterize the nucleation behavior caused by various possible capsule materials, I have studied the undercooling of molten silicon in contact with these materials to quantify their potential to resist unwanted nucleation. In addition to their maximum measured undercooling, indicative of the material properties of the capsule, efforts are made to improve the consistency of achieving such results by eliminating other causes of nucleation. These results are described in Chapter 4.

References

[1] Energy Information Administration. Renewable energy annual 2007. Technical report, Energy Information Administration, released 2009.

[2] U.S Energy Information Administration. International energy statistics, 2008.

[3] B. Chalmers. High-speed growth of sheet crystals. Journal of Crystal Growth, 70(1-2):3–10, 1984.

[4] T.F. Ciszek. Techniques for the crystal growth of silicon ingots and ribbons. Journal of Crystal Growth, 66:655–672, 1984.

[5] M.W. Geis, H.I. Smith, B.Y. Tsaur, J.C.C. Fan, D.J. Silversmith, and R.W. Mountain. Zone-Melting Recrystallization of Si films with a moveable-strip-heater Oven. Journal of the Electrochemical Society, 129(12):2812–2818, 1982.

[6] G. Hahn and A. Schönecker. New crystalline silicon ribbon materials for photovoltaics. Journal of Physics: Condensed Matter, 16(50):R1615, 2004.

[7] E.T. Hantsoo. Silicon cast wafer recrystallization for photovoltaic applications. Master's thesis, Massachusetts Institute of Technology, 2008.

[8] H Lange and I.A. Schwirtlich. Ribbon Growth on Substrate (RGS) - A New Approach To High-speed growth of silicon ribbons For Photovoltaics. Journal of Crystal Growth, 104(1):108–112, Jul 1990.

[9] A. Luque and S. Hegedus, editors. Handbook of Photovoltaic Science and Engineering, chapter 6. John Wiley and Sons Ltd, 2003.

[10] M. Meyers. Finding a balance: Photon consulting's monthly silicon update. Photon International, Jan 2010.

[11] H.J. Moeller, C. Funke, M. Rinio, and S. Scholz. Multicrystalline silicon for solar cells. Thin Solid Films, 487(1-2):179 – 187, 2005. International Conference on Polycrystalline Semiconductors- Materials, Technologies, Device Applications.

[12] C.W. Ruggiero. Geometry control of recrystallized silicon wafers for solar applications. Master's thesis, Massachusetts Institute of Technology, 2009.

[13] A. Schonecker, L. Laas, A. Gutjahr, P Wyers, A Reinink, and B Wiersma. Ribbon-growth-on-substrate: Progress in high-speed crystalline silicon wafer manufacturing. In Conference Record of the Twenty-ninth IEEE Photovoltaics Specialists Conference, pages 316–319. IEEE Electron Devices Soc, IEEE, 2002.

[14] J.M. Serra, C. R. Pinto, J.A. Silva, M.C. Brito, J. Maia Alves, and A.M. Vallêra. The silicon on dust substrate path to make solar cells directly from a gaseous feedstock. Semiconductor Science and Technology, 24(4):045002, 2009.

[15] R.L. Wallace, D. Harvey, A. Anselmo, and JI Hanoka. A high-yield, low-cost solar cell process utilizing string ribbon silicon dual ribbon growth. In Conference Record of the Thirty-First IEEE Photovoltaic Specialists Conference, pages 1139–1140, 2005.

[16] G Willson and A Mordvinov. Secular total solar irradiance trend during solar cycles 21–23. Geophysical Research Letters, 30(5):1199, 2003.

Chapter 2

Temperature Profile Measurement of Silicon Wafers at High Temperature

2.1 High-Temperature Measurements

Measurement of high-temperature environments often used in processing of silicon wafers can be difficult due to the reactivity of many materials at these high temperatures. Conventional invasive methods for measuring temperature above 1200°C include platinum-rhodium thermocouples, which must be in contact with the object to be measured [10]. Kreider et al. developed a platinum-palladium thim-film thermocouple array method for measuring two-dimensional temperature fields on silicon for rapid thermal processing applications, with an upper limit of 900°C [9]. Single-point temperature measurements of silicon near or at its melting point have also been conducted using optical fiber thermometry [3, 14], which uses an optical fiber cable threaded into the molten zone, connecting a carbon-coated fused quartz sensor to a photo diode outside the furnace. However this method measures only a single

physical location at any point in time, and a reaction between the molten silicon and quartz can alter the temperature data. Furthermore, the silicon volume must be large enough to surround a large sensor without significant perturbation of the temperature field, so such a technique would not be appropriate for wafer or thin film geometries.

Non-contact methods for temperature measurement include radiation pyrometry, which requires that either the emissivity of the object being measured is known, or that two radiation wavelengths are measured to reduce the effects of emissivity on the signal. Pyrometry can be even more challenging in a high-temperature furnace, where the presence of the heating elements can affect the signal measured. It can be difficult to have precise knowledge of the spectral emissivity of silicon samples undergoing various process steps which may cause emissivity variations. Ripple pyrometry, which measures both the sample radiation and the AC-modulated heater radiation, decouples the emissivity and reflectivity of the sample in-situ to get a more accurate measure of the sample temperature [12]. However this technique relies on a quick response time of the system, and requires multiple measurements and signal processing.

Thin films of silicon have been characterized near the melting point by Hatano et al., who used the reflection and transmission of an excimer laser signal through a partially-melted silicon film in conjunction with its conductance to determine its time-dependent temperature and phase change behavior, however the setup is quite complex and resolution is limited by the size of the laser spot [7]. Martan et al. have also used infrared radiometry and time-resolved reflectivity methods to measure the laser-induced melting of monocrystalline silicon [11], and these non-contact techniques require unobstructed optical pathways for signal measurement and would not be convenient in many furnace geometries.

In some cases, it is desirable to measure the two-dimensional temperature profile of a thin sample without perturbing the existing heat flow conditions and external

structure of the high-temperature environment. In this work, a new method has been developed to characterize a two-dimensional temperature profile experienced by a $\sim$200μm silicon wafer under steady-state conditions near the melting temperature of silicon.

2.2 Design of Novel Technique

The premise for this temperature profile measurement technique is to utilize the temperature dependence of the diffusivity of dopants in silicon. Solid state diffusivity of impurities in crystals increases with temperature, and the diffusivities of common dopants in silicon are generally well-known [5]. In addition, doping silicon with impurities such as boron or phosphorus in controlled concentrations results in a predictable change in electrical resistivity of the material [15, 16]. Therefore, introducing a given quantity of dopant atoms to the surface of a silicon wafer and allowing them to diffuse in at a steady-state temperature field for a given period of time will result in a repeatable change in sheet resistance of the wafer. Thus it should be possible to determine the temperature of the wafer during the diffusion process by measuring its final sheet resistance. A schematic representation of the concept of this method is depicted in Figure 2-1, showing that an imposed temperature profile will cause a boron surface dopant to diffuse into the wafer by a distance dependent on the local temperature at each point. For a single dopant, such as boron, diffusing into an undoped wafer, the slope of the dopant concentration as a function of depth from the surface becomes relatively small after an annealing step in the temperature range near silicon's melting point, such that samples annealed at different temperatures in that range have only small differences in their concentration profiles, since concentration gradients are small. Thus the ability to distinguish two different anneal temperatures in that range requires high resolution in the resistivity measurement, and allows less tolerance for

sample variability which might reduce precision of the T-ρ relationship.

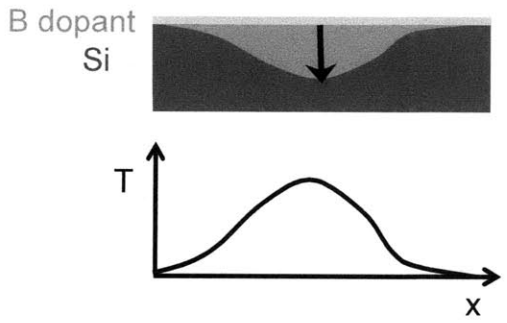
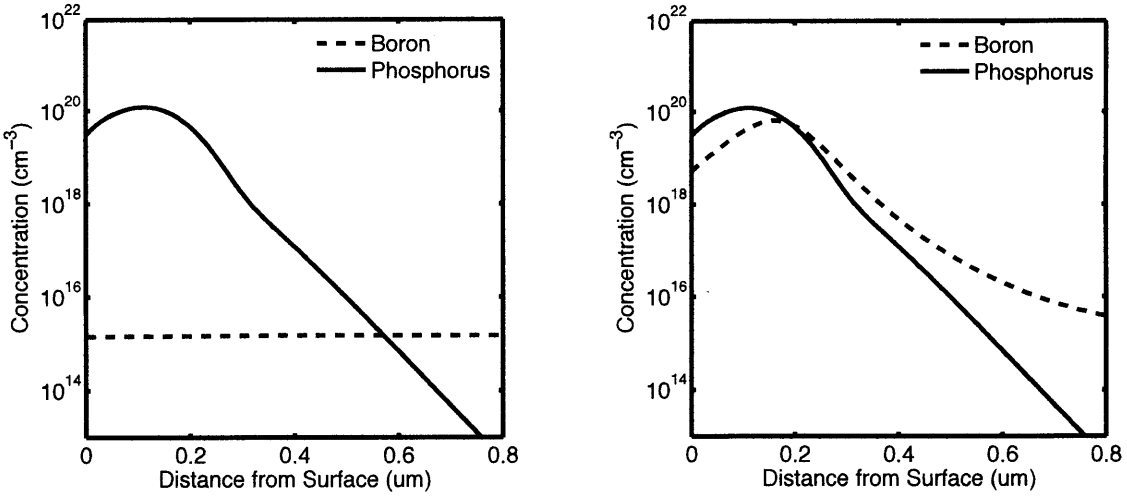


Figure 2-1: Schematic representation of the effect of temperature variation on the dopant penetration into a silicon wafer from an initial surface dopant source.

To increase the sensitivity of the resistivity measurement above 1200°C, the starting wafer can be uniformly doped with an initial concentration of one type of dopant, for example p-type dopant such as boron. Next, an n-type dopant can be deposited on the wafer surface, and as it diffuses into the wafer during the anneal, a p-n junction is formed where the two dopant concentrations are equal, as shown in Figure 2-2(a). By measuring the sheet resistance of the top region of the junction (where the n-type dopant source was deposited), a relationship can be distinguished between temperature and measured sheet resistance. For this case, the measured sheet resistance depends on the excess carrier concentration in the top region of the junction due to the implanted ion species. The creation of this junction improves the sensitivity of measured resistance to temperature because the resistivity is now based on the difference in carrier concentrations between the two oppositely-charged dopants.

For a surface ion source diffusing into a uniformly doped wafer, at temperatures near 1400°C the resistivity values begin to level out as a function of temperature, giving the poorest resolution at the upper end of the temperature scale. To further increase sensitivity of the relationship between temperature and resistance in this range, two dopants of opposite type can be diffused in at the same surface, as shown in Figure 2-2(b). A difference in diffusivity of the two dopants will cause one dopant



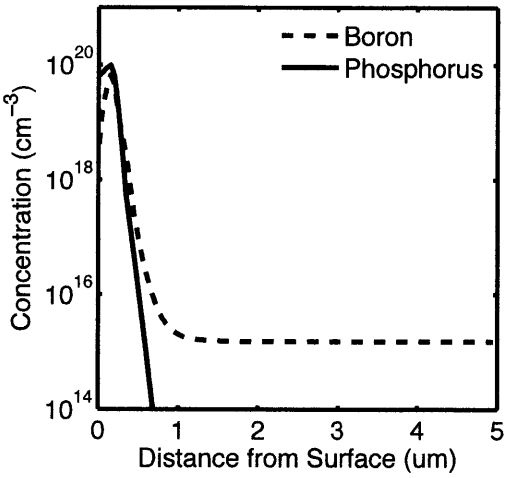
(a) Phosphorus implantation in p-type wafer.

(b) Boron and phosphorus implantation.

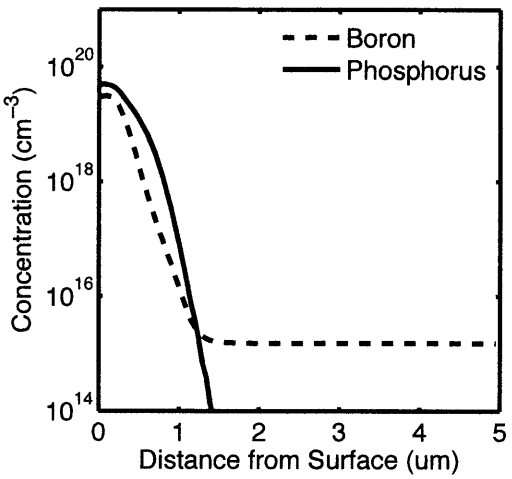
Figure 2-2: Dopant concentration profile after initial implantation of dopant source.

to penetrate farther in from the wafer surface during an anneal of fixed time. The progression of this dopant movement is illustrated in Figure 2-3. The sheet resistance of the top region of the resultant junction will depend on the difference in concentrations between the two dopants and the resultant excess of one type of charge carrier. The presence of the second dopant source increases the change in resistance with temperature in the high-temperature range.

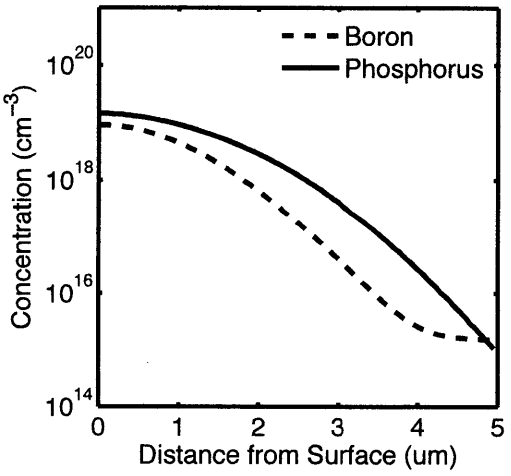
An added benefit of this method is that two-dimensional temperature maps can be generated by placing a large wafer into a high-temperature environment and measuring the sheet resistance of the top region of the junction as a function of position, using a four-point probe of small probe-tip spacing. This feature is useful for situations where temperature varies over small distances and precise knowledge of temperature gradients may be critical to the quality of a wafer being processed. Wafer thickness should not affect resistivity results, since dopant diffusion occurs within the top few micrometers from the surface, such that the most convenient wafer thickness can be chosen based on application. Because the resistivity depends on the high concentration of implanted ions very close to the surface, the starting wafer need not be high resistivity and accordingly high-cost.



(a) diffusion at 950C



(b) diffusion at 1100C



(c) diffusion at 1250C

Figure 2-3: Concentration profile after 30-minute diffusion at various temperatures.

2.3 Sample Preparation

Single-side polished Czochralski p-type silicon wafers with a starting resistivity of 20 Ω-cm were used. Wafers were thermally oxidized for 3 hours at 1000°C in dry oxygen to create a 100nm oxide layer to act as a protective layer during ion implantation. Ion implantation was used to implant a uniform distribution of both boron and phosphorus ions across the entire front polished surface of each wafer. The implantation doses were 1e15 cm^{-2} and 2e15 cm^{-2} at implantation energies of 80 keV and 170 keV, for boron and phosphorus respectively, in order to place the concentration peaks at the same depth from the surface. These doses were chosen such that the faster-diffusing phosphorus atoms would have a higher concentration in the top region of the wafer, and when the wafer is annealed at high temperatures, the concentration of both dopants decreases at every depth on the top side of the junction, but the top region of the wafer always remains n-type. This way the polarity of the junction never changes, reducing ambiguity in data interpretation, but the presence of boron in slightly lower concentration than phosphorus prevents a plateau of the profile change at high temperatures.

Spin-on dopants were considered as dopant sources due to their low cost compared to ion-implantation, and their relative ease of application. However, it is challenging to apply a very uniform and repeatable surface layer of spin-on dopant for a non-circular wafer. This lack of repeatability led to very scattered results which were unsuitable for a precision measurements of the sheet resistivity field in a large wafer.

After implantation, a 160nm-thick layer of silicon nitride was deposited on the front side of the wafer using plasma-enhanced chemical vapor deposition (PECVD), in order to prevent further oxidation of the surface during the diffusion process as well as outdiffusion of the dopants. Although the nitride layer will densify after a high-temperature anneal, it is deposited on top of the existing oxide layer such that submersion in a dilute hydrofluoric acid etch will reach the oxide layer through

pinholes and defects in the nitride, undercutting the nitride layer and completely removing it. Implantation and diffusion processes were modeled using the TSuprem-4 simulation program, to predict the changes in dopant concentration profiles under different process parameters.

Calibration of the method was carried out by placing small samples, prepared as described above, into a tube furnace of constant temperature for 30 minutes. Samples were then etched in a dilute hydrofluoric acid solution with periodic agitation to remove the nitride and oxide layers. Sheet resistance measurements were taken across the front surface of the bare wafer using a Jandel square-array four-point probe, with probe-tip spacing of 0.6mm.

2.4 Results and Discussion

2.4.1 Simulation of Diffusion and Resistance

After ion implantation, the boron and phosphorus profiles were mainly concentrated at 150nm from the wafer surface according to simulation of the implantation in TSuprem-4, as shown in Figure 2-2(b). The dopant profiles extend into the oxide layer due to its presence during implantation, acting as a protective layer against implantation damage and a screening layer to ion channeling. The dopants create a p-n junction approximately 190nm from the front surface, with the n-type side at the surface. As the wafer is annealed for 30 minutes at various temperatures, the dopants diffuse deeper into the wafer depending on the different diffusivities of boron and phosphorus at the given temperature. Phosphorus has a higher diffusivity than boron above ~900°C [5], but it is implanted in a higher dose so that the top side of the junction is always n-type. At higher annealing temperatures, the dopants diffuse farther into the wafer, decreasing the measured sheet resistance as the junction moves deeper into the wafer. The temperature dependence of this sheet resistance allows

the characterization of the temperature profile experienced by the wafer by measuring the final resistance of the material.

TSuprem-4 was used to model the behavior of the dopants during 30-minute anneals at a range of temperatures, and to calculate the expected sheet resistance of the top layer of the junction. The program was also utilized to determine the most appropriate ion-implantation parameters and annealing conditions. The results of this simulation with the chosen process parameters are displayed in Figure 2-4. The simulation predicts a constant sheet resistance for annealing temperatures below 700°C, for which there is no significant movement of the dopants during 30 minutes due to lower diffusivities in silicon. For example, the characteristic diffusion length of boron and phosphorus at 700°C is approximately 1.3nm and 0.42nm, respectively, which is small compared to the width of the implanted concentration profile, on the order of hundreds of nanometers. However, due to the presence of an oxide layer on the silicon surface during the anneal step, the concentration of phosphorus in the silicon has increased where it contacts the oxide layer due to a segregation coefficient greater than unity [2,6]. In contrast, the concentration of boron decreases at the silicon-oxide interface due to a segregation coefficient less than unity. The segregation coefficient represents a comparison of the equilibrium solubility of the dopant in silicon versus in silicon dioxide, which will dictate the concentrations on each side of the interface that will yield equal Gibbs free energy values of the dopant at the interface [8]. The result of both segregation behaviors are shown in Figure 2-5(a). This dopant redistribution causes very large concentration gradients at the interface, thus driving faster diffusion relative to other locations in the depth profile of concentration.

The consequence of this segregation is that the most significant diffusion of P and B at temperatures below 900°C is the movement of dopants to decrease this steep surface gradient, causing surface P concentration to decrease and surface B concentration to increase. Figure 2-5(b) shows the profile at 750°C, where the dopants in the bulk wafer

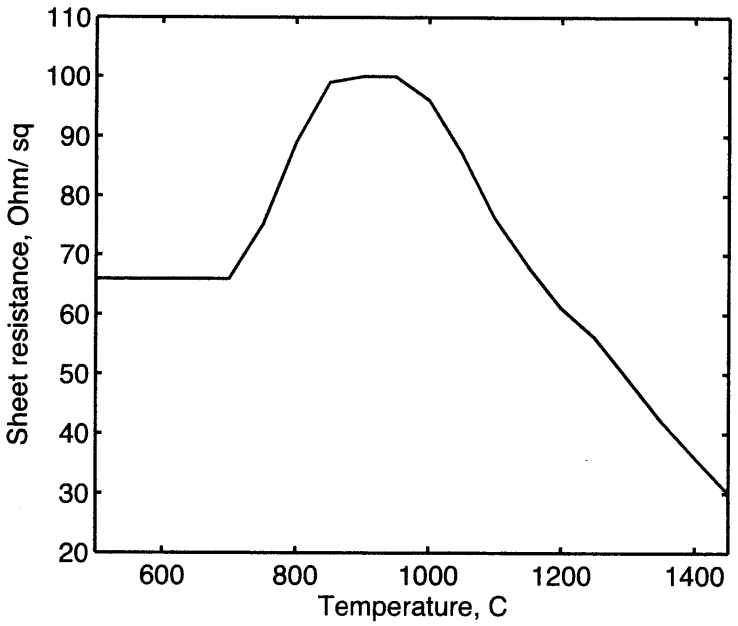


Figure 2-4: TSuprem-4 modeling results of sheet resistance variation in top layer of junction with annealing temperature.

have not moved noticeably but the surface concentrations of boron and phosphorus have increased and decreased respectively, compared to their profiles at 600°C. A decrease in the excess number of n-type carriers at the surface actually leads to an increase in resistivity, shown in Figure 2-4 by the increasing resistivity between 700°C and 900°C. For annealing temperatures around 900°C, shown in Figure 2-5(c), the segregation-related gradients have mostly flattened out, and the phosphorus has begun to increase again to smooth the gradient produced by the implantation process, i.e. the concentration peak at 190nm. For anneals above 1050°C, shown in Figure 2-5(d), bulk dopant concentrations are changing during the 30-minute timespan and the junction moves further into the silicon. At this point the final sheet resistance begins to diminish with temperature, above ~1000°C. In this higher temperature range, the faster-moving phosphorus is driving the location of the junction farther from the surface and resistance decreases.

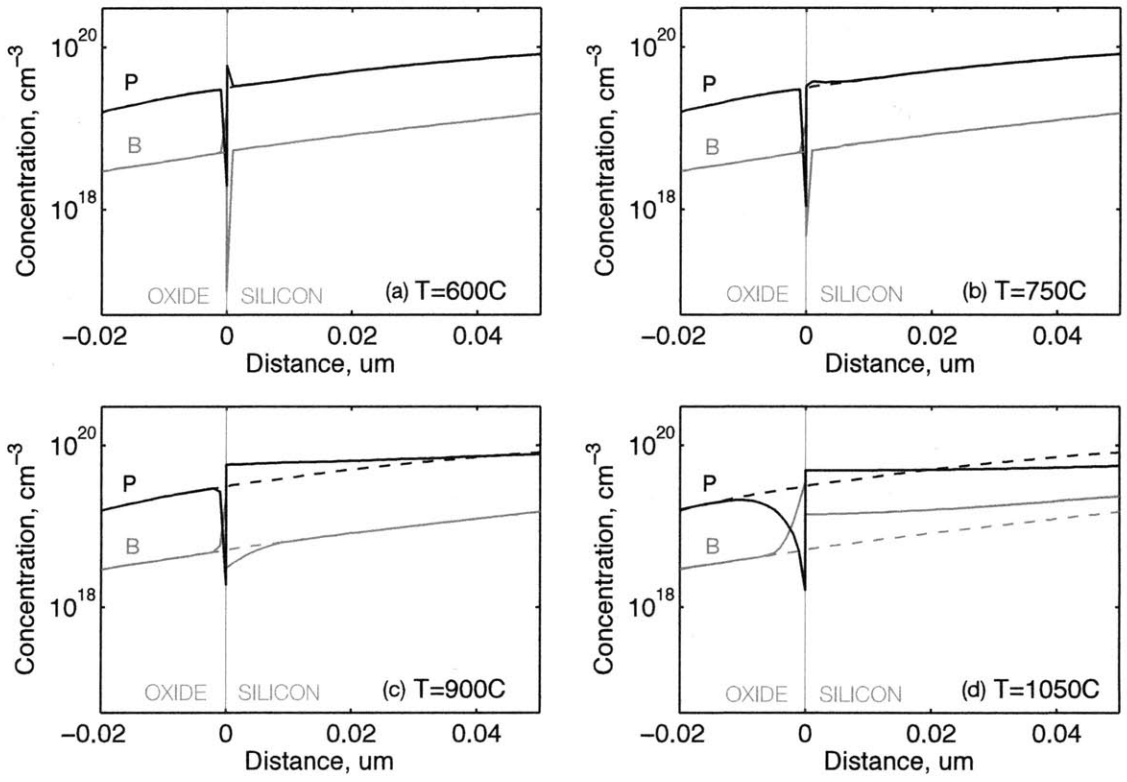


Figure 2-5: Simulation of dopant profiles near oxide-silicon interface after 30-minute anneal at various temperatures. Oxide is shown at x<0, and silicon at x>0. Phosphorus concentration is plotted in black, boron in red. Dashed lines represent profiles before annealing.

2.4.2 Calibration

To connect the simulated results with the actual prepared samples, calibration measurements were carried out at a range of temperatures between 800°C and 1400°C. These calibration measurements yielded the experimental relationship between temperature and sheet resistance of the top layer of the p-n junction. Several different samples were prepared and annealed at each temperature, and the results of this calibration are shown in Figure 2-6. A comparison with the values predicted by the TSuprem-4 model shows an overall shift to higher sheet resistance values for any temperature. However, the behavior of the resistance increase, maximum, and decrease with increasing temperature as predicted from the simulations was clearly shown by the calibration samples as well. One calibration sample was run with the tube furnace set at 1400°C, which caused the sample to melt. Given that the known melting temperature of silicon is approximately 1415°C, there may be a 15°C shift in the tabulated temperatures from the actual temperatures of the calibration samples. However, the overall relationship between resistivity and temperature still applies.

The higher measured resistance values compared to simulated values may be due to oxidation occurring through the nitride layer during high-temperature anneal steps, causing oxidation-enhanced diffusion (OED) [13]. Because both boron and phosphorus diffuse in silicon primarily by the interstitialcy mechanism [5], and the oxidation reaction injects interstitials into the underlying silicon, the diffusivities of both dopants in silicon are thus enhanced when oxidation occurs. Below 1000°C, small amounts of oxidation may cause OED effects to be most pronounced at the surface, causing a larger rise in resistivity than predicted by the TSuprem-4 model. Dopant diffusion enhancement by oxidation depends on the fraction of diffusion due to the intersticialcy mechanism, as opposed to the vacancy mechanism, for a particular dopant. Several researchers have measured this fractional contribution for boron and phosphorus, with varying results [13,17], but Antoniadis et al. suggest that phospho-

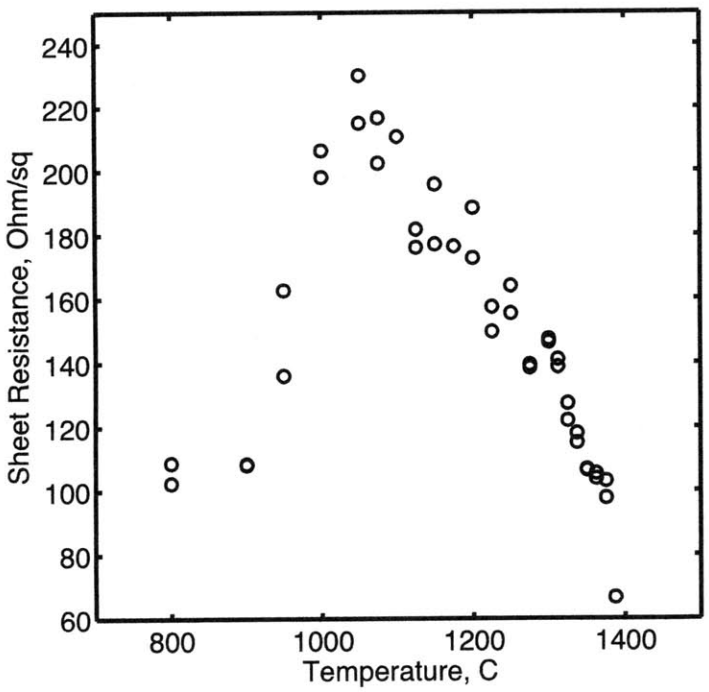


Figure 2-6: Calibration data measured from prepared samples annealed at various known temperatures.

rus may have a slightly higher fraction of intersticialcy diffusion [1]. In this case, the diffusivity of phosphorus would be more affected by the process of oxidation, and the phosphorus peak would diffuse more quickly than predicted, reducing the difference in concentration between dopants and increasing the resistivity.

Visual observation of samples after annealing above 1300°C revealed a noticeable change in color, indicating a change in the oxide layer thickness. This fact suggests that oxidation is able to occur despite the protective nitride layer capping the wafer. It is likely that lower-temperature annealing steps also incurred smaller amounts of oxidation.

To verify whether oxidation was causing this resistivity shift from predicted data, two samples were annealed for 30 minutes in a quartz tube furnace at 1000°C under flowing argon. The sheet resistance of these samples was measured to be 170 $\Omega/\square$, which is lower than that of samples annealed at the same temperature in air. This

supports the explanation that oxidation occurring in the air-annealed samples causes an increase in diffusion of the dopants. However, the argon-annealed sample still has higher resistivity than the simulations predict for that temperature.

To further determine the extent of oxidation, the depth profiles of air- and argon-annealed samples were measured using secondary ion mass spectroscopy (SIMS). As shown in Figure 2-7, both dopants have diffused farther from the wafer surface in the air-annealed sample, indicating that even at 1000°C, the oxidation-enhanced diffusion is enough to affect the underlyling dopant profile. The junction depth in the air-annealed sample is 36 nm farther from the surface than in the argon-annealed sample, and the phosphorus peak concentration is also lower for the sample annealed in air.

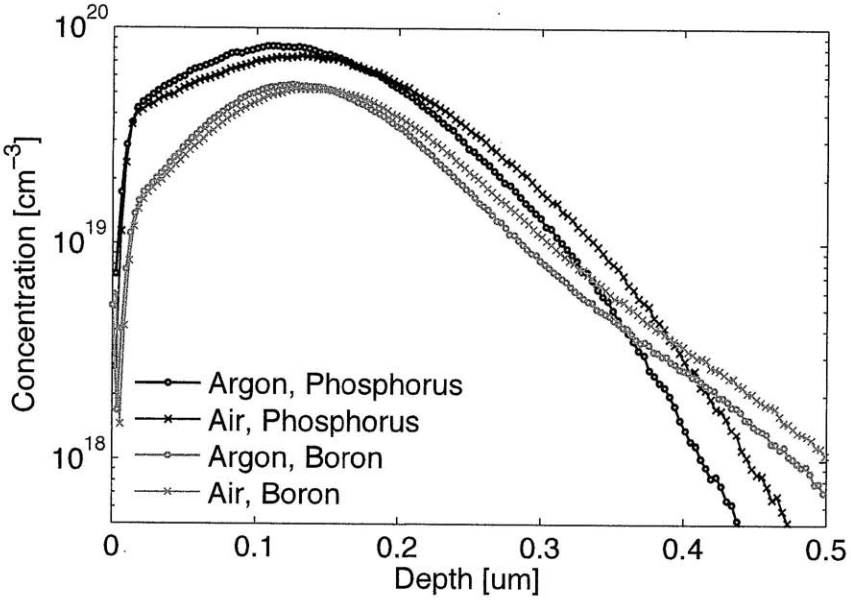


Figure 2-7: Depth profile of B and P concentration in samples annealed for 30 minutes in air (x) or argon (o) atmosphere at 1000°C.

Comparing the SIMS-measured depth profile of the argon-annealed sample to the simulated results in TSuprem-4, shown in Figure 2-8, it is clear that there is a significant difference in the profiles of both dopants between modeled and measured concentrations. Specifically, the difference in concentration between phosphorus and boron in the top 150nm for the modeled profile is much larger than the difference

in concentration for the measured sample. This profile difference should result in a higher resistivity for the calibration sample, and this is consistent with what is measured and shown in Figure 2-6.

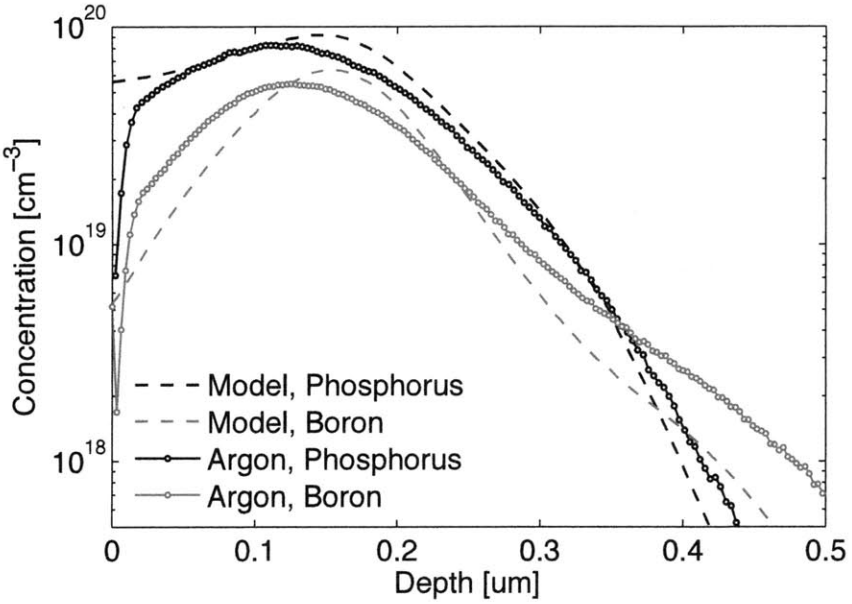


Figure 2-8: Measured depth profile of B and P concentration in sample annealed for 30 minutes in argon atmosphere at 1000°C (o) compared to simulation results (–).

Above 1000°C, the decrease in resistivity is due to a broadening of the n-type layer of the junction and overall decrease of both dopant concentrations at any position above the junction. The higher the temperature of the anneal step, the deeper the junction is and the lower the sheet resistance measured. This behavior corresponds well with the predictions of the TSuprem-4 model discussed previously.

It is clear that this technique in its current formulation is appropriate for measurement of environments with temperatures above 800°C, due to the negligible movement of the dopants in a 30-minute period at low temperatures. However a modification could be made by using longer annealing times such that dopant diffusion length is significant at the desired temperature range.

For a monotonic relationship between temperature and measured resistance, the current method is restricted to temperatures above 1050°C for the parameters de-

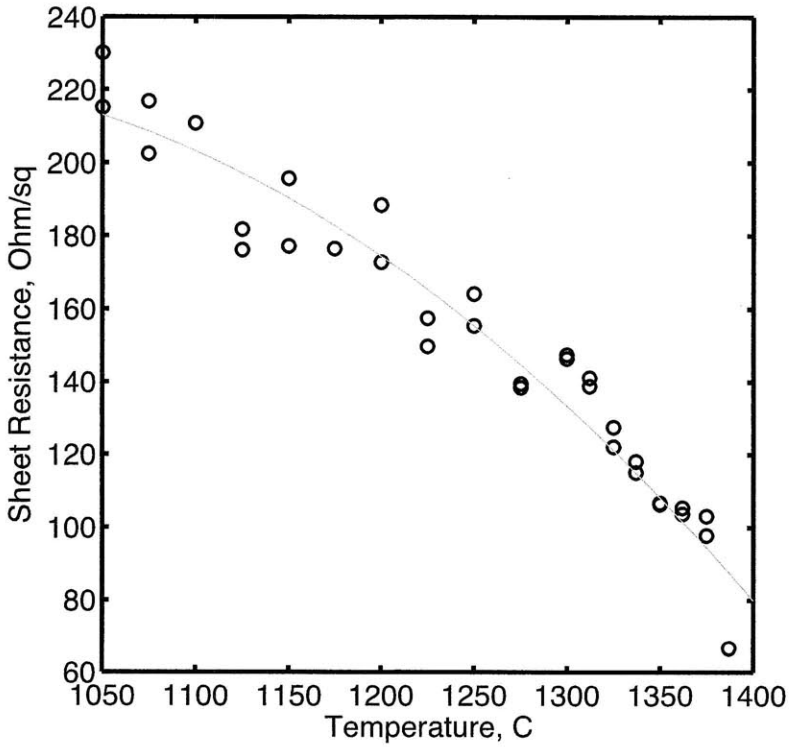


Figure 2-9: High-temperature subset of measured calibration data for temperature and sheet resistance shown in black circles, with curve fit shown in solid line.

scribed here. This range of data is depicted in Figure 2-9, which is a subset of the data shown in Figure 2-6. A quadratic fit was made to the calibration data in the range of temperatures above 1050°C, given by

$$R_{sh} = -.00061T^2 + 1.1T - 290$$

This relationship was then used to relate subsequently measured sheet resistances to corresponding temperatures between 1050°C and 1400°C.

2.4.3 Application of Technique

To apply this method in a high-temperature environment with a spatially-varying temperature field, a rectangular wafer of 1-inch width and 4-inch length was prepared using the procedures described in Section 2.3. This wafer was then placed centrally in the hot zone of the recrystallization furnace described in Section 1.4, defined by six resistive silicon carbide heater elements in two horizontal rows, with the wafer located between the two rows. The total width of the hot zone was approximately 2 inches. A schematic representation of the wafer's position in the furnace is shown in Figure 2-10. The temperature of the heater elements were set at 1585°C, controlled by a series of two-color pyrometers. The prepared sample was placed between two silicon carbide backing plates of 1mm thickness and was used to characterize the temperature field within the hot zone. Upon removal from the hot zone, it was observed that a small oval-shaped zone became molten during the 30-minute anneal. This region can be used as a reference point of known temperature.

The entire area of the sample can be measured using a four-point probe if a correction factor is used to adjust the sheet resistance measurement near the wafer edges. The correction factors, $C.F.$, for rectangular- and square-array probes are given by Catalano [4]. In general, $C.F.$ deviates from unity only when the distance of

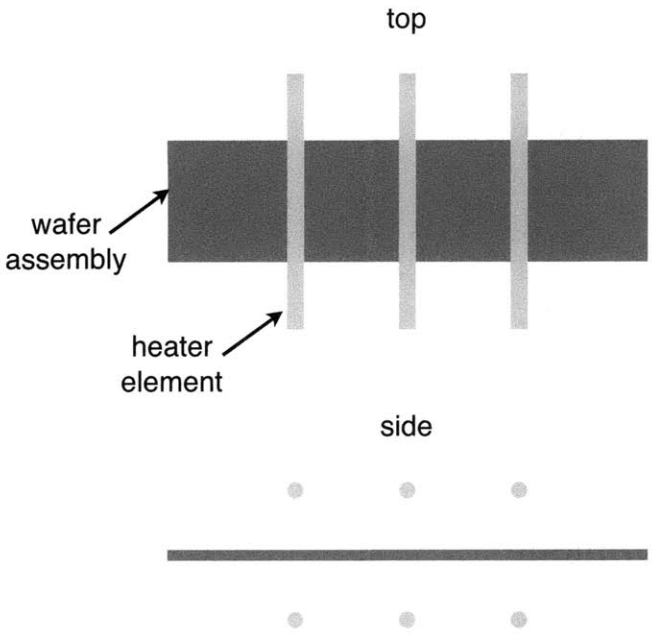


Figure 2-10: Schematic of wafer in resistively-heated zone furnace.

the probe from the wafer edge is less than $4s$, where s is the spacing between probe tips. The formula for sheet resistance for a square-array four-point probe for samples with thickness $t < 5s$, where s is the spacing between probe tips, is given by

$$R_{sh} = \frac{4.532}{2 - \sqrt{2}} \frac{V}{I} C.F.$$

Using resistivity correction factors near sample edges, a temperature map was generated from the sample resistance measurements. Shown in Figure 2-11, the temperature reveals a hot zone of ~50 mm in length, corresponding to the location of the three heater element rods above and below the sample. Temperatures are greater than 1400°C in this hot zone. The measurement has revealed that the hot zone has a central maximum near the center heating element. While the temperature-resistivity relationship cannot be applied to the region that was molten during the process, it can be used as a check to make sure the surrounding areas show temperatures approaching the melting temperature of silicon. Indeed, the measured points near this

region show a reasonable approach to 1420°C. It is also clear that the wafer center point is offset from the center of the hot zone, revealing more of the temperature profile on the right side of the furnace.

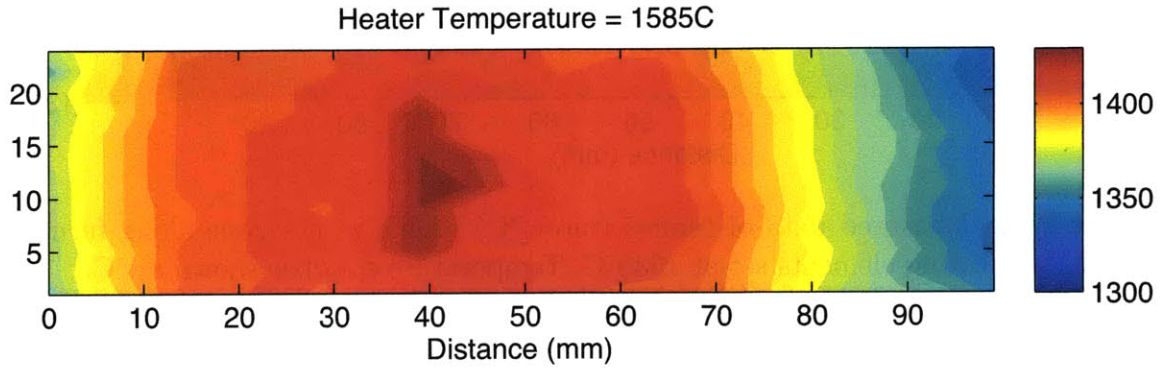


Figure 2-11: Measured data of temperature profile in hot zone along furnace length, for heating elements set at 1585°C. Temperature colorbar shown in °C.

A second wafer was tested at different heater element settings to test the sensitivity of the furnace profile to variations in heater element temperatures. In this case, the elements were set to a constant temperature of 1530°C, and the characterization sample was placed in the hot zone for 30 minutes as before. In this case, the entire sample remained solid during the process. The resulting temperature map is shown in Figure 2-12. This wafer reached a maximum temperature of 1389°C in the center, with a ~50mm hot zone with temperatures above 1375 °C. A comparison with the first sample shown in Figure 2-11 shows that the 55°C decrease in heater element setpoint results in a 25°C decrease in hot zone temperature.

One common feature between both measured temperature profiles is the slight curvature in the isotherms across the width of the wafer. The slightly lower temperatures at the wafer edges are most likely due to a temperature gradient in the cylindrical heater elements across their length, which is approximately 2 inches, and the decrease in temperature as they touch the electrical contacts at the furnace walls. Clearly, these measurements have revealed the temperature gradients surrounding the hot zone of the furnace and their dependence on heater setpoints, and such parameters

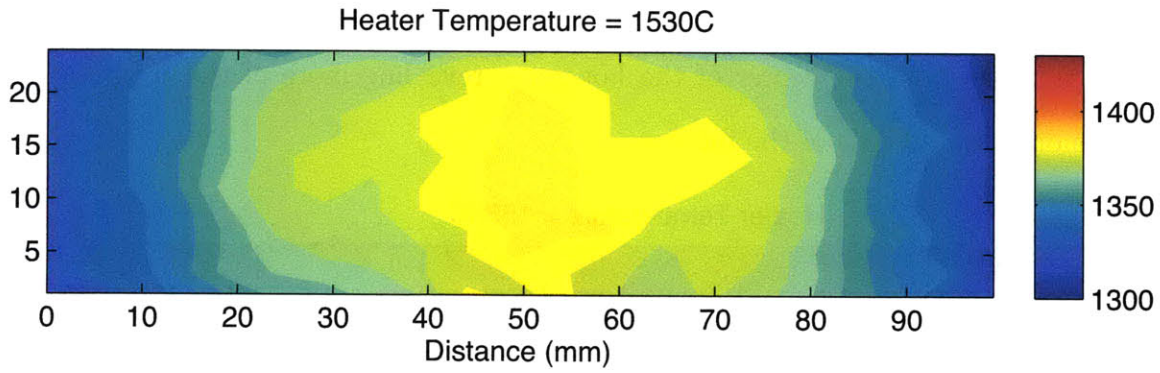


Figure 2-12: Measured data of temperature (°C) profile in hot zone along furnace length, for heating elements set at 1530°C. Temperature colorbar shown in °C.

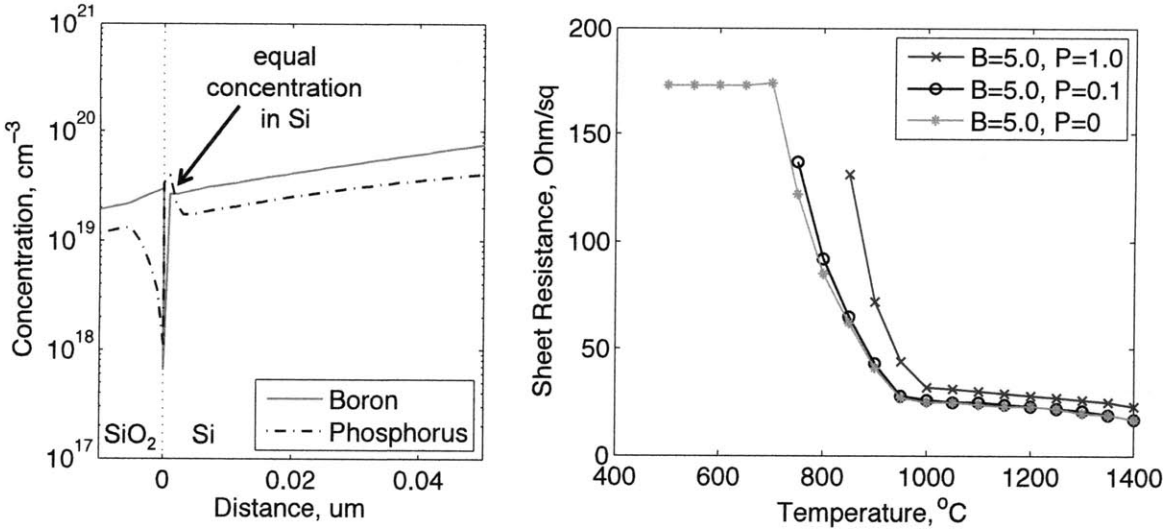
can be critical to the final quality of zone-processed wafers.

2.5 Concluding Thoughts

This new temperature profiling method has shown to be promising and useful for measurement of the high-temperature range field of thin silicon geometries. Using the specifications described in the previous sections, this method can be used for temperatures above 1050°C. As described in Section 2.4, these parameters yielded a non-monotonic behavior of sheet resistance with increasing temperature due to the movement of surface concentrations due to segregation effects at the silicon-oxide interface. Consideration was given to switching the dopant species such that the phosphorus implant dose was lower than the boron dose, such that segregation-related movement at the surface would not cause an increase in sheet resistance for temperatures between 700 and 1000°C. If this approach worked in achieving a monotonic relationship, it would increase the temperature range over which temperature profiling could be useful. However, the segregation effects still complicate the results – if the concentration of phosphorus is too close to the higher boron concentration, the segregation effects will cause the phosphorus to increase at the surface, *above* the surface level of boron, as shown in Figure 2-13(a). This behavior actually creates a

second junction near the surface, and changes the polarity of the surface region as the majority dopant has switched at the surface. Beyond the very surface, boron is the majority dopant up to a distance of ~190 nm, as implanted, and this junction at 190 nm is only one that should be present for this measurement. After an annealing step at a high temperature, these segregation effects diffuse away to leave a single junction as is desired, but the lower temperature anneals are not sufficient for this to occur. At a certain threshold temperature, the diffusivity of the dopants is high enough to diffuse away those surface effects in the 30-minute period. If the ratio of phosphorus to boron implant doses increases closer to unity, then the segregation effects cause a much larger surface excess of phosphorus, which increases that threshold temperature at which diffusion is fast enough to diffuse away the surface effects. This behavior is reflected in Figure 2-13(b), where the threshold temperature (the lowest-T plotted data point for X and O curves) is shown to increase as the ratio of P:B increases. Conversely, reducing the dose of phosphorus will decrease the effectiveness of its presence at all, approaching the result for implanting only boron in an n-type wafer, shown in grey diamonds in Figure 2-13(b). Above ~1000°C, the resistance-temperature curve has a very flat slope, as seen in Figure 2-13(b), making it poorly suited to measuring those temperatures. Therefore this technique produces better results when phosphorus is implanted in a higher dose than boron, and lower temperatures can be profiled by choosing a longer annealing time period such that dopants begin noticeably diffusing below 700°C.

In summary, a novel method has been developed and proven for characterizing the two-dimensional temperature profile experienced by a silicon wafer in a high-temperature environment. The simultaneous diffusion of two different dopants from the surface of the wafer was simulated using TSuprem-4 and successfully calibrated to show the same behavior of sheet resistance as a function of increasing temperature. The technique was successfully implemented to show the effects of variations



(a) Surface concentrations of dopants for boron implant dose of $5\times\ 10^{15}$ cm^{-2} and phosphorus of $1\times\ 10^{15}$ cm^{-2}. Equal concentration point represents unwanted junction.

(b) Sheet resistance behavior for implantation of higher doses of boron. Legend describes implanted doses of B and P in units of $1\ \times\ 10^{15}$ cm^{-2}. Circle and X curves are plotted for higher temperatures only, where a single junction was seen.

Figure 2-13: Dopant concentration profile after initial implantation of dopant source.

in furnace heater conditions on the temperature fields experienced by silicon samples without altering the furnace geometry or heat flow conditions. This unobtrusive, low-complexity method is promising for characterization of other thin-geometry high-temperature environments in silicon processing where other methods are not suitable.

References

[1] D. A. Antoniadis and I. Moskowitz. Diffusion of substitutional impurities in silicon at short oxidation times: An insight into point defect kinetics. Journal of Applied Physics, 53(10):6788–6796, 1982.

[2] M.M. Atalla and E. Tannenbaum. Impurity redistribution and junction formation in silicon by thermal oxidation. Bell System Technical Journal, 39:933, 1960.

[3] D. Bliss, B. Demczyk, A. Anselmo, and J. Bailey. Silicon-germanium bulk alloy growth by liquid encapsulated zone melting. Journal of Crystal Growth, 174(1-4):187 – 193, 1997. American Crystal Growth 1996 and Vapor Growth and Epitaxy 1996.

[4] S.B. Catalano. Correction factor curves for square-array and rectangular-array four-point probes near conducting or nonconducting boundaries. IEEE Transactions on Electron Devices, 10:185–188, May 1963.

[5] P. M. Fahey, P. B. Griffin, and J. D. Plummer. Point defects and dopant diffusion in silicon. Rev. Mod. Phys.; Reviews of Modern Physics", 61(2):289–384, Apr 1989.

[6] A. S. Grove, Jr. O. Leistiko, and C. T. Sah. Journal of applied physics; redistribution of acceptor and donor impurities during thermal oxidation of silicon. Journal of Applied Physics, 35(9):2695–2701, 1964.

[7] M. Hatano, S. Moon, M Lee, K Suzuki, and C.P. Grigoropoulos. Excimer laser-induced temperature field in melting and resolidification of silicon thin films. Journal of Applied Physics, 87(1):36–43, Jan 1 2000.

[8] Robert Hull, editor. Properties of Crystalline Silicon, chapter 9 - Impurities in silicon. IET, 2006.

[9] Kenneth G. Kreider and Frank DiMeo. Platinum/palladium thin-film thermocouples for temperature measurements on silicon wafers. Sensors and Actuators A: Physical, 69(1):46 – 52, 1998.

[10] E. Kuroda, M. Matsuda, and M. Maki. Growth of 10 cm wide silicon ribbon. Journal of Crystal Growth, 50(1):193 – 199, 1980.

[11] J. Martan, N. Semmar, and O. Cibulka. Precise nanosecond time resolved infrared radiometry measurements of laser induced silicon phase change and melting front propagation. Journal of Applied Physics, 103(8), APR 15 2008.

[12] B. Nguyenphu and A.T. Fiory. Wafer temperature measurement in a rapid thermal wafer temperature measurement in a rapid thermal processor with modulated lamp power. Journal of Electronic Materials, 28(12):1376–1384, 1999.

[13] David J. Roth and James D. Plummer. Oxidation-enhanced diffusion of boron and phosphorus in heavily doped layers in silicon. Journal of The Electrochemical Society, 141(4):1074–1081, 1994.

[14] M. Schweizer, A. Croll, P. Dold, T. Kaiser, M. Lichtensteiger, and K.W. Benz. Measurement of temperature fluctuations and microscopic growth rates in a silicon floating zone under microgravity. Journal of Crystal Growth, 203(4):500–510, Jun 1999.

[15] W.R. Thurber, R.L. Mattis, Y.M. Liu, and J.J. Filliben. Resistivity-Dopant Density relationship for boron-doped silicon. Journal of the Electrochemical Society, 127(10):2291–2294, 1980.

[16] W.R. Thurber, R.L. Mattis, Y.M. Liu, and J.J. Filliben. Resistivity-Dopant Density relationship for phosphorus-doped silicon. Journal of the Electrochemical Society, 127(8):1807–1812, 1980.

[17] A. Ural, P. B. Griffin, and J. D. Plummer. Fractional contributions of microscopic diffusion mechanisms for common dopants and self-diffusion in silicon. Journal of Applied Physics, 85(9):6440–6446, 1999.

[THIS PAGE INTENTIONALLY LEFT BLANK]

Chapter 3

Thermal Modeling of Solidification Interface

3.1 Motivation for Phase Transformation Model

The motivation for constructing a computer model of the silicon wafer solidification stems from a need to understand the factors that influence the shape of the solid-liquid interface within the wafer. Due to the sub-millimeter dimensions of the physical system, experimental measurement of the solidification interface is prohibitively difficult. Thus a thermal model of the heat transfer conditions imposed on a recrystallizing wafer as it exits the hot zone of the furnace can give critical insight into the behavior of the phase change interface in a 200μm-thick wafer.

Understanding the factors that affect final grain structure of the wafer includes knowing the direction of movement of the solid-liquid interface during solidification, to understand where grain boundaries might form relative to the plane of the wafer. A growth direction perpendicular to the wafer travel direction would result in grains growing from the top and bottom surfaces and meeting in the middle to form a grain boundary, as shown schematically in Figure 3-1. Such a grain boundary oriented

parallel to the wafer plane would cause minority carrier recombination before carriers could reach the current collectors at top and bottom surfaces of wafer.

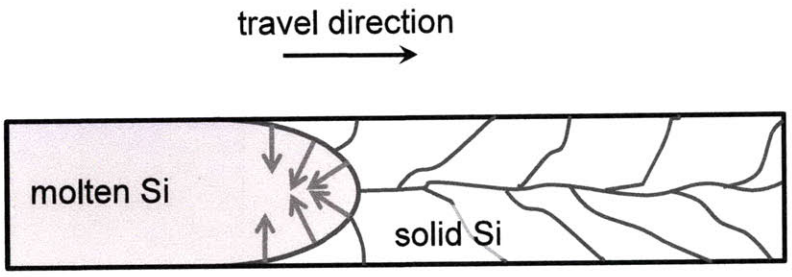


Figure 3-1: Schematic representation of wafer cross-section showing of effects of symmetrically curved interface on grain boundary orientations.

The thermophysical properties of silicon used in the following analyses are given in Table 3.1. For quick reference, the variables and constants used in this chapter are listed in Table 3.2.

Property	Units	Solid	Liquid	Reference
density, ρ	kg/m^3	2330	2500	[6]
heat capacity, c_p	J/kg K	1000	912	[4, 11]
thermal conductivity, k_{Si}	W/m K	22	60	[4, 6]
melting point, T_m	K	1687		[4]
heat of fusion, Δh_f	J/kg	1.8×10^6		[8]

Table 3.1: Thermophysical properties of solid and liquid silicon near T_m.

Variable	Definition	Value	Units
H	half-thickness of wafer	100×10^{-6}	m
W	width of wafer	25×10^{-3}	m
T_o	temperature of environment	1500	K
T_x	temperature at $y = 0$	$\sim T_m$	K
T_{avg}	mean temperature of radiation	1600	K
ϵ	emissivity of SiC	0.9	–
σ	Stefan-Boltzmann constant	5.67×10^{-8}	W/m^2K^4
α	thermal diffusivity of silicon	$k_{Si}/\rho c_p$	m^2/s
h_R	heat transfer coefficient	see Eq.(3.2.2)	W/m^2K
u	wafer pull speed	see text	m/s
L	length of interface	see text	m
L_c	characteristic length of fin	see Eq.(3.2.1)	m
A_c	cross-sectional area	see Eq.(3.2.1)	m^2
P	perimeter of fin cross-section	see Eq.(3.2.1)	m
δ	latent heat multiplier	see Eq.(3.4.1)	–

Table 3.2: List of variables and geometric parameters.

3.2 Fin Approximation

A silicon wafer exiting the hot zone of the recrystallization furnace has many similarities to a fin geometry, and may be analyzed within the fin framework. Figure 3-2 depicts a representation of the wafer exiting the furnace hot zone, with the left size at T_m where the silicon solidifies. Heat is primarily lost in the y direction through radiation as the wafer moves in the x direction. In the basic case of a fin, where no phase change occurs and therefore release of latent heat is not a factor, temperature gradients in the fin are much larger in the x direction than in y. This fin approximation is valid as long as heat transfer within the fin is much faster than heat removal from the surface of the fin. This condition is quanitified by the Biot number, Bi, which compares the heat transfer resistance inside and outside of an object. For a general fin, the Biot number is given by

$$Bi = \frac{hL_c}{k} \tag{3.2.1}$$

where L_c is the characteristic length, equal to $A_c/P = (2HW)/2(2H + W)$ for a rectangular fin. For the silicon wafer of thickness $2H = 200\mu$m and width $W = 25$mm, $L_c \approx 1 \times 10^{-4} m$. The temperature difference between the wafer and the surroundings, $\Delta T = T_m - T_o$, fits the criteria that $(\Delta T)^2 \ll T_{avg}^2$, where $T_{avg} = (T_m + T_o)/2$. The values of these figures can be found in Table 3.2. Satisfying this inequality condition allows us to approximate the heat transfer coefficient, h_R, for radiation from the fin surface as

$$h_R = 4\epsilon\sigma T_{avg}^3 \tag{3.2.2}$$

Using these values, the Biot number is calculated to be $Bi = 3.8 \times 10^{-3} \ll 1$ for a stationary wafer, indicating that temperature gradients in the y-direction can be neglected within the wafer.

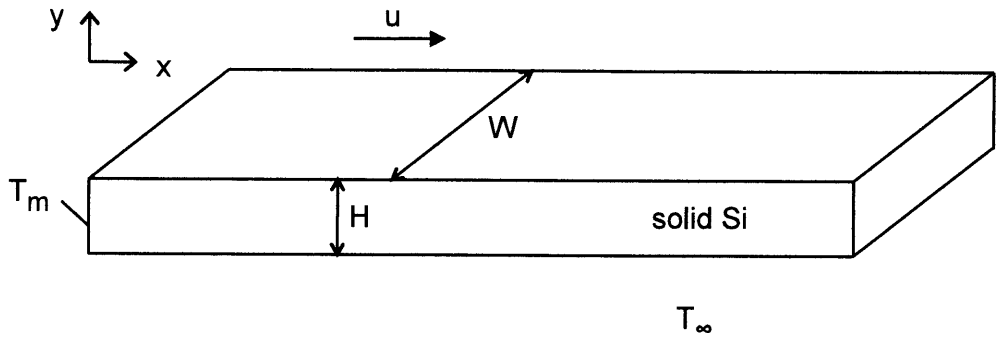


Figure 3-2: Schematic representation of silicon wafer as a fin.

For the case of a moving wafer, $u > 0$, the speed of the wafer motion may cause a non-zero y-gradient in temperature at a given x-location. The time constant of the heat loss from the stationary wafer, given that Bi $\ll 1$, can be calculated as

$$\tau = \frac{H^2}{\alpha Bi} \tag{3.2.3}$$

where $\alpha = k/\rho c_p$. This characteristic time actually has no dependence on k_{Si} because the internal resistance to heat transfer is negligible when Bi $\ll 1$. When the time

constant of the wafer motion is of the same order as the characteristic time of heat loss, the heat will accumulate in the wafer and cause a non-zero gradient of temperature in the y-direction. This condition of comparable characteristic times occurs when the wafer speed is greater than $\sim 3.6 \times 10^{-4}$m/s $= 21.6$ mm/min.

The temperature gradients will be further perturbed near the liquid-solid phase transition, where the addition of latent heat will provide a further quantity of heat to be removed from the wafer thickness. Therefore, this fin analysis has provided a useful insight into the relative magnitudes of different heat transfer mechanisms in the wafer and at which wafer pull speeds the y-direction temperature gradient will become non-negligible. This analysis will also provide a point of comparison for computational thermal models discussed in later chapters. We are interested in determining the relationship between the speed of the moving wafer/fin and the resulting shape of the interface for a given radiation condition.

3.3 Triangle Analytical Model

A most basic representation of the solidification interface would be to start with the assumed curved interface shape and approximate it with a straight line between the wafer edge and the wafer centerline, as indicated in Figure 3-3. Drawing a closed control volume with a triangle shape, as shown in Figure 3-4, an energy balance can be made to determine a relationship between the dimensions of the triangle and the wafer travel speed. In this analysis, the height H of the triangle is assumed to be 100μm, half the width of the 200μm wafer. The magnitude of the heat flowing into the control volume, per unit depth into the page, can be calculated from knowledge of the mass of silicon crossing the boundary in the x-direction and the latent heat of silicon per unit mass, as well as the specific heat capacity of silicon. Conduction from the liquid is considered to be negligible. The inflow of heat is represented as

$$Q_{in} = Q_{sensible} + Q_{latent} = \rho C_p T_m H u + \rho \Delta h_f H u = [W/m] \tag{3.3.1}$$

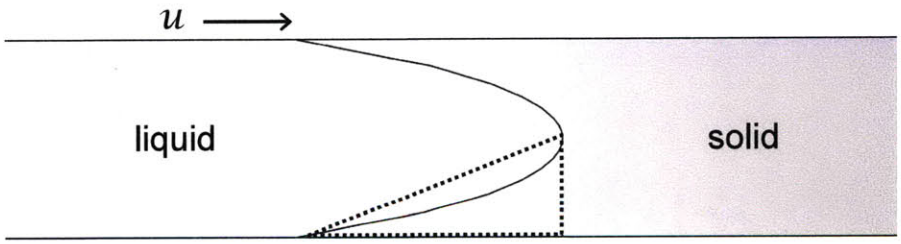


Figure 3-3: Approximation of half-interface curve as straight line to form triangular control volume.

The heat flux on the bottom boundary of the control volume is mainly controlled by the radiation losses to the surroundings. In the recrystallization process, the silicon wafer is surrounded by two silicon carbide backing plates as it travels through the hot zone. Physical contact between the wafers and the backing plates is assumed to be good, since both are flat and untextured. For this analysis, the heat transfer

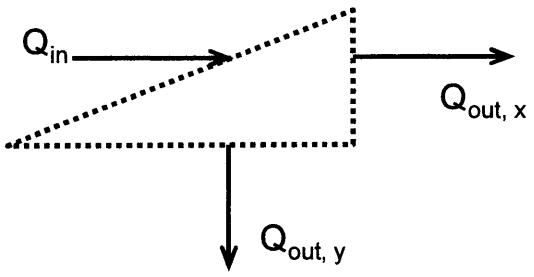


Figure 3-4: Triangular control volume with components of energy balance.

in the silicon carbide plates is assumed to be fast due to its relatively high thermal conductivity, such that the limiting factor for heat transfer in the y direction is the radiation of heat from SiC to the surroundings. For a 1-mm SiC plate with a thermal conductivity of ~40 W/mK near the melting point of silicon [7], the Biot number of the backing plate is calculated to be ~.02, confirming that the internal heat transfer resistance is much less than the external resistance, and the assumption of negligible temperature gradients in the SiC plate is valid. Thus the emissivity of SiC (ϵ=0.9) can be used to determine the radiative losses from the silicon wafer at this boundary. In this case, the outward heat transfer in the y-direction can be represented as

$$Q_{out,y} = Q_{radiation} = \epsilon\sigma L(T_x^4 - T_o^4) = [W/m] \tag{3.3.2}$$

where L is the length of the control volume in the x-direction and the parameter used to quantify the degree of curvature of the solidification interface. The temperature of the surroundings, T_o, is assumed to be 1500K, based on measurements of the inner furnace walls with a Type R thermocouple. The temperature of the wafer, T_x should be near to the melting temperature of silicon at this location, and an approximation of $T_x \approx T_m$ is made. The Stefan-Boltzmann constant, σ, is given as $5.67 \times 10^{-8} Wm^{-2}K^{-4}$.

The heat flux condition on the right-hand side of the control volume in Figure 3-4 includes a contribution from the flow of sensible heat across the boundary, as well

as conduction through the silicon. This outward heat flux in the x-direction can be represented as

$$Q_{out,x} = Q_{sensible} + Q_{conduction} = \rho c_p T_{out} H u - k_{Si} H \frac{\partial T}{\partial x} = [W/m] \tag{3.3.3}$$

In order to estimate the temperature gradient in the x-direction, the overall temperature gradient is assumed to be perpendicular to the hypotenuse of the triangular control volume, which is an isotherm at T_m. From the slope of this line, a relationship is determined between the x- and y-components of the temperature gradient, given by

$$L \frac{\partial T}{\partial x} = H \frac{\partial T}{\partial y} \tag{3.3.4}$$

H is a known quantity since the wafer thickness remains constant, and $\frac{\partial T}{\partial y}$ can be determined from an energy balance at the wafer lower boundary, setting the radiation heat loss equal to conduction in the y-direction through the silicon, as

$$\epsilon \sigma (T_x^4 - T_o^4) = k_{Si} \frac{\partial T}{\partial y} = [W/m^2] \tag{3.3.5}$$

With this estimation of $\frac{\partial T}{\partial y}$ and its assumed relationship to $\frac{\partial T}{\partial x}$, the conduction through the solid silicon is estimated. For the outward convection of sensible heat, the temperature T_{out} should vary as a function of y-position, and can be represented as the average temperature along that boundary, assuming the constant $\frac{\partial T}{\partial y}$ as mentioned.

$$T_{out} = T_m - \frac{\partial T}{\partial y} \frac{H}{2} \tag{3.3.6}$$

Given these representations of the fluxes into and out of the control volume, a steady-state energy balance can be done to determine the relationship between length

L and wafer travel speed u.

$$Q_{in} = Q_{out,y} + Q_{out,x} \tag{3.3.7}$$

$$\rho c_p T_m H u + \rho \Delta h_f H u = \epsilon \sigma L (T_x^4 - T_o^4) + \rho c_p T_{out} H u - k_{Si} H \frac{\partial T}{\partial x} \tag{3.3.8}$$

The relative magnitudes of the terms in equation (3.3.8) can be compared by subsituting approximate values for each variable. Looking at the first two terms, they have several factors in common, and both are equal to ~80 W/m, since the sensible heat of silicon at 1687K is approximately equal to the heat of fusion. On the right-hand side of the equation, the first term should be on the order of ~10 W/m, using the values noted in Table 3.2. The second term is similar to the first term on the left-hand side, on the order of ~80 W/m. If the temperature gradient in the x-direction is determined as described above, the third term on the right-hand side is on the order of ~30 W/m. However, this term will really depend on the magnitude of the temperature x-gradient needed to remove the heat of fusion. Making the substitutions mentioned in equations (3.3.4) and (3.3.5) and solving for u, we get

$$L = H^2 + \frac{\rho H u (c_p [T_m - T_{out}] + \Delta h_f)}{\epsilon \sigma (T_x^4 - T_o^4)} \tag{3.3.9}$$

Using this relationship, one could determine the required wafer travel speed, u, to achieve a certain curvature of the solidification interface with a length of L.

Given the wafer thickness of 200 μm, the above equation was evaluated for wafer pull speeds between 0 and 9 mm/min and the results plotted in Figure 3-5. This analysis indicates that as soon as the wafer speed becomes non-zero, the interface begins to curve from the initial planar shape. However, this relationship is based on the assumption that the solidification interface has a constant slope from the centerline to the wafer edge, and that the temperature gradients within the wafer remain parallel to that interface. However, when the wafer is moving

very slowly, the internal resistance to heat transfer by conduction should be low enough that the released latent heat can easily be conducted away from the interface. These approximations of a linear temperature gradient may be the cause for the disagreement with the fin analysis of Section 3.2, which indicates that there should be a range of low pull speeds for which no interface curvature is seen. For a more rigorous and detailed analysis of the interface shape, computational simulations were necessary.

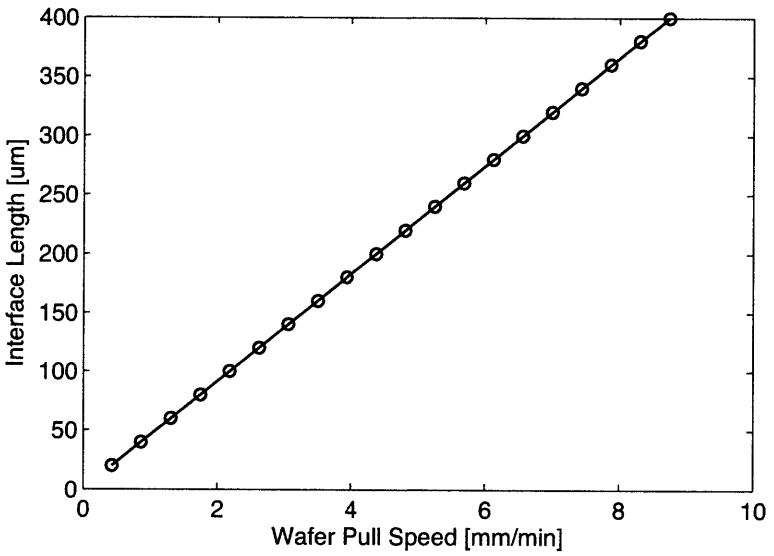


Figure 3-5: Relationship between wafer speed and curved interface length predicted by triangular control volume approximation.

3.4 COMSOL Model with Modified Heat Capacity

COMSOL Multiphysics was used to create a two-dimensional thermal model of the wafer solidification. Because the latent heat of fusion is released only at the moving interface between liquid and solid, and COMSOL, a finite element modeling program, is not capable of representing a heat source at a non-stationary boundary, the latent heat of fusion was first represented as a modified heat capacity, $C_p + \Delta h_f \delta$. This is a well-known method for modeling solidification, referred to as the enthalpy method, and is often used in simulations of casting or directional solidification [9, 10, 12].

In this approach, the latent heat of fusion was represented as a modification in the heat capacity of silicon. Specifically, a Gaussian function is centered at the melting temperature, as depicted in Figure 3-6. The equation for this "latent heat multiplier" curve is given by

$$\delta = \frac{\exp[-(T - T_m)^2/(dT)^2]}{dT\sqrt{\pi}} \tag{3.4.1}$$

such that dT represents the half-width of the curve. This representation works well for two-component solutions or alloys in which there is a "mushy zone" in the transition from liquid to solid, and the latent heat is released over a range of temperatures depending on the phase diagram of the particular system. This area under this Gaussian curve represents the additional amount of heat that must be removed or absorbed in order to solidify or melt a certain mass of material. In the case of a pure material, the width of this "mushy zone" of solidification should narrow down to a sharp spike of infinitely small width on the temperature scale. Computational power limited the narrowness of the spike that was possible find a solution for, since the mesh would have to be increasingly fine to resolve the interfacial features, so the model began with a finite-width Gaussian representation and decreased that width to find a convergence of the interface shape for smaller and smaller dT values.

However, as the value of dT was decreased, the length of the interface L in

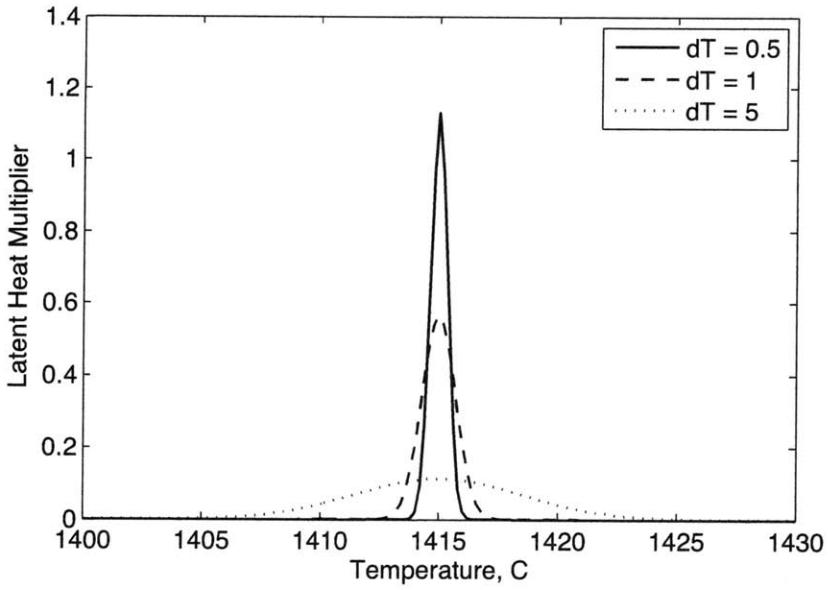


Figure 3-6: Representation of modification peak added to heat capacity of silicon at melting temperature.

the solution did not approach a steady value, but rather increased exponentially as shown in Figure 3-7. This result indicates that the modified heat capacity approach is not appropriate for modeling the interface shape in this thin-wafer geometry where the interface curvature has a characteristic length on the same order as the object thickness. For a larger object undergoing directional solidification, a small change in the width of the "mushy zone" may have a negligible effect on the overall shape of the interface due to the large amount of material available to remove the heat by conduction. Thus the enthalpy method should be restricted to large-scale solidification models of casting or directional solidification. Another approach was clearly needed to describe this problem of wafer solidification.

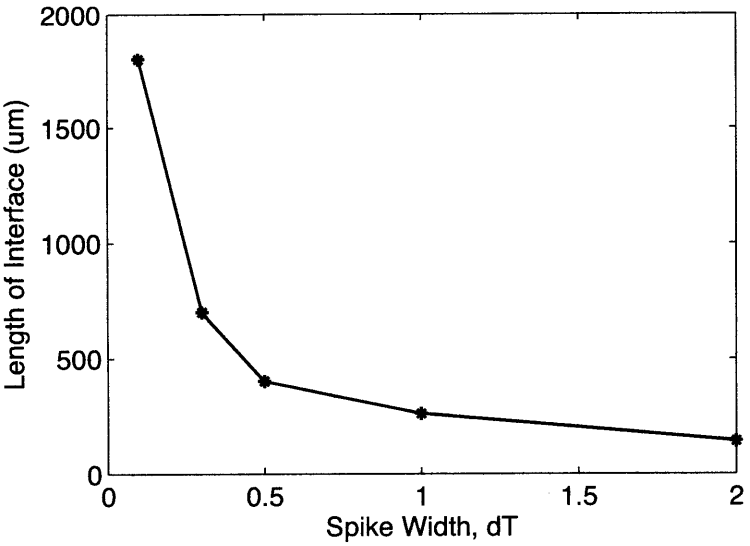


Figure 3-7: Non-convergence of interface length solution with decreasing width of latent heat gaussian.

3.5 Phase Field Modeling

One approach that was considered for solving this problem was the use of a phase-field model to analyze the phase change. In the phase-field method, a variable called ϕ is assigned to represent the phase of the material as a function of position, where ϕ=1 represents the solid phase and ϕ=0 represents the liquid phase. The model solves for the equilibrium and evolution of ϕ as well as T for a given set of boundary conditions. This decoupling of phase and temperature can allow for solutions to problems that include materials subcooled below the equilibrium melting temperature, or dendritic growth due to crystal anisotropy or interface curvature effects [3, 13]. For the case of alloys, a third variable representing concentration can be added. The advantage of this approach is that the location of the solid-liquid interface need not be known beforehand. The solution of the governing equations will include a region where ϕ transitions from 0 to 1, and the line representing $\phi = 0.5$ is generally taken to be the solid-liquid interface.

For a single-component system, where the composition is constant everywhere,

the free energy functional F is given by

$$F = \int_V \left[f(\phi, T) + \frac{\kappa}{2} |\Delta\phi|^2 \right] dV \tag{3.5.1}$$

where $f(\phi, T)$ represents the free energy density and κ can be considered as the phase diffusivity for ϕ, related to the surface energy and the interface thickness [1, 2]. The equilibrium condition requires a minimization of free energy in the system, so the variational derivative of F with respect to ϕ is set equal to zero [1]:

$$\frac{\delta F}{\delta \phi} = \frac{\partial f}{\partial \phi} - \kappa \nabla^2 \phi = 0 \tag{3.5.2}$$

The time-dependent governing equation for phase is therefore given by

$$\frac{1}{M_\phi} \frac{\partial \phi}{\partial t} = \frac{\partial f}{\partial \phi} - \kappa \nabla^2 \phi \tag{3.5.3}$$

where M_ϕ represents the phase mobility based on interface kinetics. The value of M_ϕ depends on the interface thickness as well as the kinetic coefficient and the latent heat of fusion. Note that phase is not a conserved quantity.

The free energy density, f, depends on two different functions, $g(\phi)$ and $p(\phi)$, and is given by [1]

$$f = W g(\phi) + (1 - p(\phi)) f_L(T) + p(\phi) f_S(T) \tag{3.5.4}$$

The double-well function $g(\phi)$ has minima at $\phi = 1$ and $\phi = 0$, and a maximum between them representing the energy barrier between phases. The magnitude of this potential energy hump is represented by W, which is related to the interfacial energy between phases [2]. $p(\phi)$ is an interpolating function that connects the free energies of the liquid and solid phases, $f_L(T)$ and $f_S(T)$ respectively. It basically serves to raise or lower the free energy of the solid phase depending on whether T is above or below T_m [1].

For the case of a pure element, the free energy of the liquid can be set to zero as a reference point and the difference in free energies can be simplified as

$$f_S(T) - f_L(T) = \frac{\Delta h_f (T - T_m)}{T_m} \tag{3.5.5}$$

where Δh_f is the latent heat of fusion [1]. This equation shows that when $T = T_m$, the free energies of liquid and solid phases are equal and both exist in equilibrium. When $T < T_m$, the liquid free energy is higher than the solid free energy, so the solid phase is more stable and there will be a driving force to solidify. Using this simplification, the free energy density is written as

$$f = Wg(\phi) + \Delta h_f \frac{(T - T_m)}{T_m} p(\phi) \tag{3.5.6}$$

In addition to the phase equation, the heat equation also has an additional term to represent the change of phase and the release of latent heat. This equation is given by

$$\frac{\partial T}{\partial t} = \alpha \nabla^2 T + \frac{\Delta h_f}{\rho c_p} \frac{\partial \phi}{\partial t} \tag{3.5.7}$$

The third term of equation (3.5.7) is non-zero only when there is a change in phase per unit time, and the latent heat of fusion, Δh_f, is released at the position where ϕ is changing. This dependence of the heat equation on ϕ and the dependence of the phase equation on T makes the problem very interesting and non-linear.

Efforts were made to create a two-dimensional phase-field model using FiPy, which is a partial differential equation solver written in Python by the Materials Science and Engineering Laboratory at the National Institute of Standards and Technology (NIST). This program is free for download, and is based on the finite volume approach. Using FiPy, the heat equation and phase equation can be constructed and then solved simultaneously, outputting a plot, for example, of the temperature field in

a small region of the solidifying wafer with a line plotted at $\phi = 0.5$ to demarcate the phase boundary. A realistic value for the interfacial thickness would be on the order of nanometers, which would require a very fine mesh to properly resolve, but the disparity between that scale and the 100μm wafer half-thickness made the problem computationally demanding. Non-dimensionalization of the governing equations with appropriate characteristic lengths and times can be carried out to bring the different terms in each equation closer to the same order, thereby facilitating arrival at a good solution.

This approach would be more suitable for a problem involving undercooling in the melt, such as molten silicon being solidified on a cold substrate, where the temperature and phase need to be specified as separate variables. The phase-field approach would also be appropriate for a two-component system, such as silicon with an initial concentration of an impurity, which could be modeled as a concentration variable, or for a model of polycrystalline solidification, where the anisotropy of different grain orientations could be included in the phase equation. The FiPy program is well-suited to certain types of problems, but becomes rather cumbersome when implementing convection boundary conditions and unusual geometries. In those cases, a better approach might be to write one's own code based on the finite volume method to solve the PDEs, which would allow greater control over how boundary conditions and solvers are implemented. For the problem of interest here, a thermal model without inclusion of the phase parameter was more appropriate, where phase is assumed to be solid or liquid based on temperature alone, and it is discussed in detail in the following section.

3.6 Fixed Interface COMSOL Model

An alternative approach to modeling the solidification interface shape is to utilize the boundary condition specified by the Stefan problem. The Stefan condition represents a heat flux discontinuity at a moving phase boundary between liquid and solid in order to satisfy conservation of energy. The rate of release of latent heat must be equal to the rate of heat removal at the interface, thus dictating the velocity of the interface. In order to apply such an energy balance, the location of this interface must be known. Given that the velocity of the wafer in the recrystallization process will be constant, the location of the solidification interface should be constant in time. However, its exact shape is still unknown. A reference frame can be defined at the steady-state location of the phase boundary and the Stefan problem can be applied to a pre-determined interface shape. Then the interface shape can be adjusted manually until the energy balance can be solved at each point on the interface.

COMSOL Multiphysics was used to create a two-dimensional thermal model for the solid region of the wafer, as shown in Figure 3-8, with the solid-liquid interface represented by the curved boundary on the left. The wafer movement is in the $+x$ direction at a speed of u, and the thickness of the wafer in the y-direction is 200μm. As the silicon crosses the curved boundary and enters the control volume, it solidifies and releases the latent heat of fusion. Given appropriate boundary conditions and material properties of silicon, COMSOL solves for the temperature field and heat fluxes for a given interface shape. At each point along this interface, a differential control volume can be drawn as in Figure 3-9, and the energy balance for this control volume is given by the following equation.

$$\rho_L \Delta h_f u dy + \rho_L c_{p,L} T_L u dy - k_L \cancel{\frac{\partial T}{\partial x}|_L dx} = \rho_S c_{p,S} T_S u dy - k_S \frac{\partial T}{\partial n}|_S ds \qquad (3.6.1)$$

The first term in Equation (3.6.1) represents the release of latent heat as a given

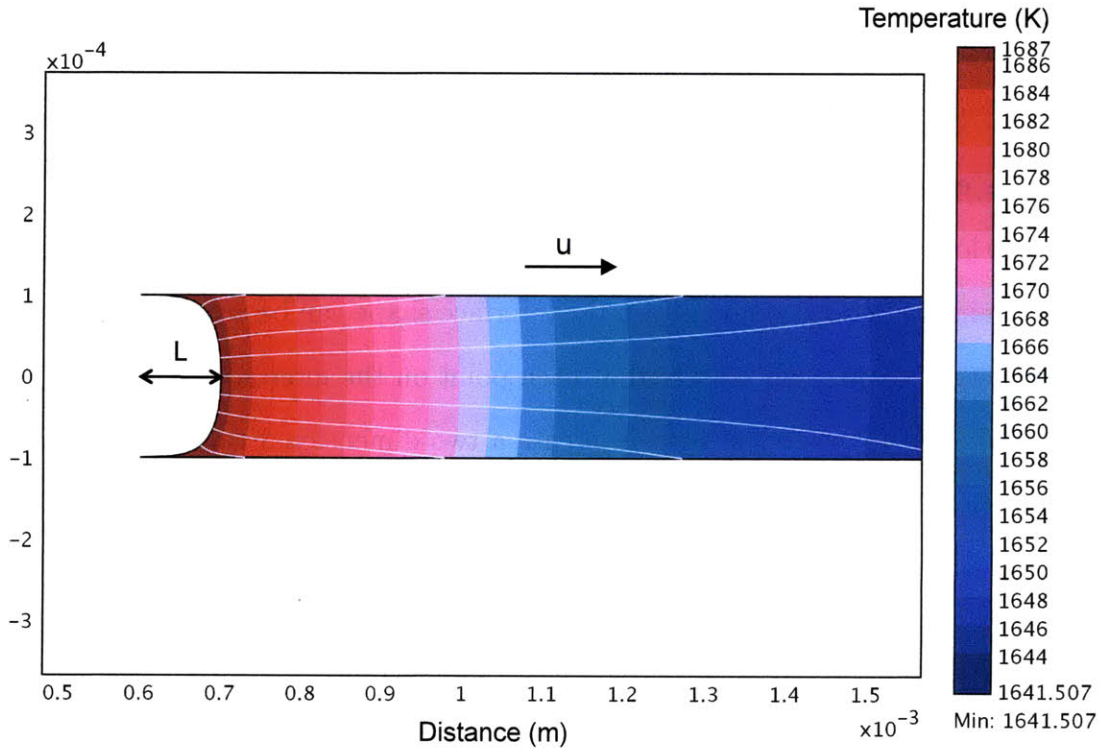


Figure 3-8: Two-dimensional COMSOL model of wafer with fixed solidification interface. White lines represent conductive heat flux streamlines.

amount of silicon moves past the interface and changes phase. The second term represents movement of sensible heat carried by liquid silicon to the interface. The third term, representing conduction through the liquid, is neglected because it is assumed that the material immediately to the left of the boundary is at constant temperature of T_m. This side of the equation can be calculated based on knowledge of the material properties of silicon and the wafer speed.

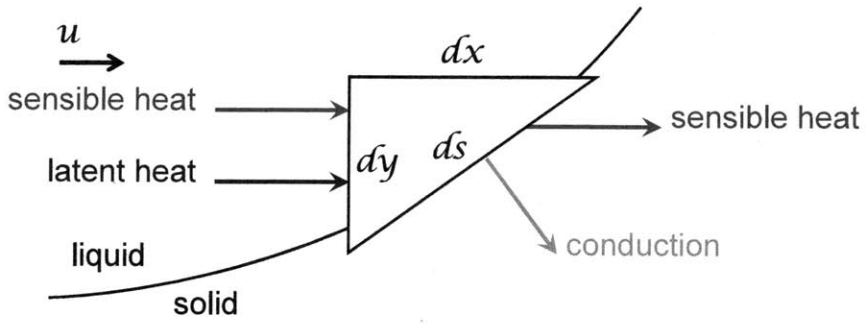
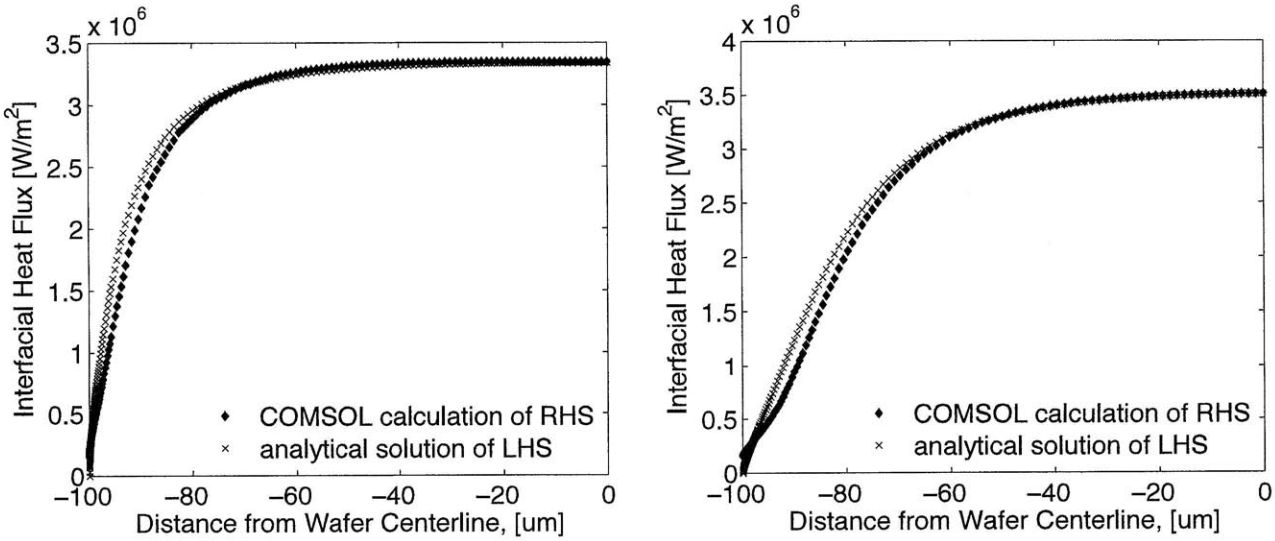


Figure 3-9: Schematic representation of energy balance at each point on the solid-liquid interface.

The right-hand side of the equation is extracted from the COMSOL solution. The hypotenuse of the triangular control volume is parallel to the solidification interface at each point, with a length of ds. The temperature gradient normal to this ds boundary is represented by $\partial T/\partial n$, and the silicon crossing this boundary is solid, represented by the S subscripts on the variables in equation (3.6.1). Comparing this outgoing heat flux to the calculated incoming heat flux, and adjusting the interface shape until they are equal, we can find the equilibrium interface shape for a given wafer speed and radiation boundary condition. In the following results, the vertical heat loss was assumed to be limited only by the radiation at the outer face of the silicon carbide backing plates, which have an emissivity of 0.9, to an environment temperature of 1500K inside the furnace.

Examples of the curve fitting results for two different wafer speeds are shown in Figure 3-10. Because a symmetric heating condition is being modeled, only one-

half of the wafer's heat flux needs to be solved, and thus the x-axis only shows 100 μm of the wafer. The curve of black diamonds represents the calculated heat flux normal to the solidification interface as determined by the COMSOL 2D model, as a function of position relative to the centerline of the 200-μm wafer. The black X curve shows the analytical solution for the heat flux as represented by the left-hand side of equation (3.6.1). For each curve length in the x-direction, L, the exact curvature of the solidification interface as well as the wafer speeds are adjusted until the best match is found between the two plotted curves. Curve fits are better towards the wafer centerline, partially due to the decreasing number of mesh points between the wafer edge and the solidification interface towards the wafer edge (distance from the wafer centerline approaching 100 μm), especially when the interface is steeply curved.



(a) u = 24 mm/min, L = 50 μm

(b) u = 25.2 mm/min, L = 150 μm

Figure 3-10: Sample curve fit for the two sides of equation (3.6.1) as a function of position across half-thickness of wafer.

The equilibrium interface shapes for increasing wafer speeds, u, are shown in Figure 3-11. The y-axis represents the full 200μm thickness of the wafer, and the distance in the x-direction between the most extreme points of of the interface curve will be referred to as the interface length, L. The wafer travel speeds which cause the interface to take these shapes are plotted against L in Figure 3-12.

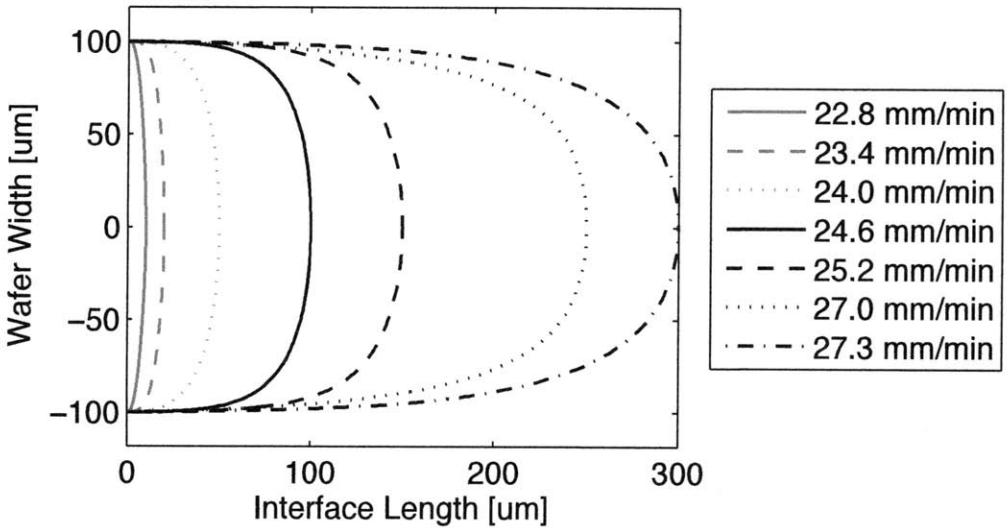


Figure 3-11: Equilibrium shapes of interface with increasing wafer pull speed.

These results indicate that the interface remains flat ($L = 0$) for $u <\sim 22$ m/s. This value agrees well with the limit estimated by the fin analysis in Section 3.2, which found a limiting value of 21.6 m/s for the assumption of negligible temperature variation in the y-direction. At these low speeds, the latent heat of fusion is released more slowly than heat is lost at the wafer surface due to radiation, so the isotherms are not perturbed from a planar shape. Once the latent heat release magnitude is of the same order as the radiation heat loss, the solidification interface must curve in order to maintain an equilibrium solid growth rate.

The equilibrium interface shapes do not correspond to a particular known equation, such as a parabolic or circular arc, but rather were custom-fit Bézier curves that most closely matched the heat flux condition at the boundary. Parabolic curves of different proportions were initially used in this approach, but the curve-matching

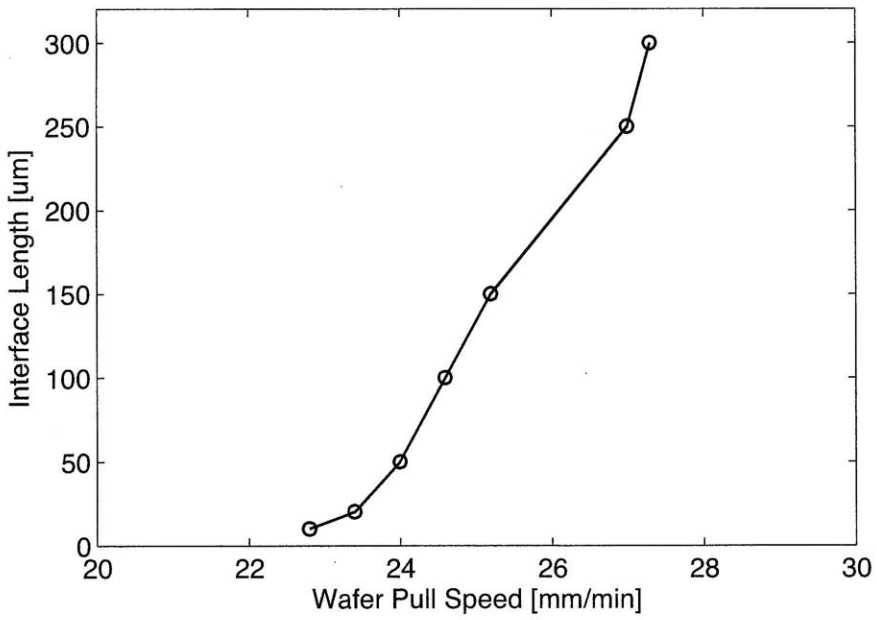


Figure 3-12: Equilibrium length L of interface variation with wafer pull speed.

near the wafer edges was increasingly poor as wafer speed, and therefore interface length, increased. Custom-adjusted curves were therefore required to obtain the best matching of heat fluxes. Curve shapes are generally flattest at the centerline of the wafer, with increasingly steep curves approaching the wafer surface as wafer speed increases.

These equilibrium shapes can be understood by considering the reason that the interface begins to curve. As the wafer speed increases, the rate of release of the latent heat of fusion also increases. When the wafer speed reaches a certain threshold, the latent heat released is so large that conduction from the interface is not large enough to transport the latent heat from the entire wafer thickness to the edge. Solidification occurs first at the wafer edge. As solidification proceeds inward from the edge, the interface must incline in the $+x$ direction in order to increase the area for heat removal by radiation at the edge. As a result of this slanted interface, the isotherms in the x-direction near the wafer centerline are compressed, since the interface must be at T_m and the edge of the solidified wafer continues to cool due to surface radiation to the surroundings. Therefore an increased temperature gradient in the x-direction

also increases the conduction at the centerline, which remains flat if that conduction becomes large enough to account for the large latent heat release for a particular wafer speed. Thus the curved interfaces are generally more vertical near the centerline rather than equally curved through the thickness, until the latent heat release rate is large enough that the interface must be inclined from the edge to the centerline, a condition which is being approached by the right-most curve for 27.3 mm/min in Figure 3-11.

3.7 Implications For Wafer Recrystallization

Highly curved solid-liquid interfaces can be detrimental to the quality of the recrystallized wafer. This model shows that the solidification interface should remain flat as long as the wafer speed is less than $\sim$ 23 m/s, for the given temperature of the environment, T_o. If the environment temperature is increased, radiation heat losses will decrease and the transition speed will be lower. Thus, if interface curvature is to be avoided, the wafer speed should be maintained below the limiting value as described here. A lower transition speed would also be caused by using a thicker wafer, which would release more latent heat per unit time for a given wafer speed.

One reason for the undesirability of high interface curvature is that the grain growth direction is dictated by the normal vector to the interface at each point. For a curved interface, the normal vectors point towards the centerline of the wafer, indicating that any grains growing along these directions will meet at the centerline, forming a grain boundary at this plane. However, the orientation of such a grain boundary is particularly detrimental to solar cell performance, given that minority carriers generated within the silicon bulk by photon absorption will need to travel in the y-direction to reach the current collectors. Since grain boundaries cause carrier recombination, carriers will likely recombine there before contributing to the output

power.

High curvature may also lead to increased dislocations in the solidified wafer. In the case of monocrystalline ingot growth by the Czochralski method, dislocation-free growth is achieved by forcing a slightly concave interface, curving towards the crystal [5]. However, a highly concave interface will lead to very high radial temperature gradients in the cooling crystal, leading to stress which creates dislocations. The shape of this Cz growth interface is controlled by heating inputs, melt size, and crystal pull rate. Similar considerations should be made for the wafer recrystallization interface.

Asymmetric heating conditions from top to bottom of wafer may be used to cause a slanting of the solidification interface, reducing the chances for grains growing on opposite faces to meet in the center and form a grain boundary. Very large temperature gradients again should be avoided, to prevent thermal stress leading to dislocation production. Consider the case of an adiabatic boundary condition on the top side of the wafer, which could be achieved by increasing the length of the hot zone on the top side of the furnace only, such that the top is maintained at a higher temperature while the bottom side begins to cool below T_m. This asymmetric condition bears an important similarity to the solution to the half-wafer with symmetric boundary conditions, as the centerline of the symmetric wafer was represented by an adiabatic boundary. Thus one can infer that the solidification interface shape for an adiabatic condition on the top of the wafer would have the same overall shape as those shown in Figure 3-11 below the centerline, for $-100\ \mu m < y < 0$. However, the scale of these curves would be twice as wide in the y-direction, for the full wafer width of 200 μm, as shown in Figure 3-13, and the corresponding wafer speed that would give such a curve should be lower than those solved in this symmetric case. Another way to understand this relationship is to consider the Biot number, which would be twice the Biot number found in Section 3.2, since the characteristic length would be the full wafer thickness of $2H = 200\ \mu m$ rather than just H. This new

value of Bi for the adiabatic top boundary condition would increase the time constant of heat loss by a factor of two, as it would take more time to cool the wafer to a lower temperature. The time constant of wafer motion scales as $1/u$, so it would match the time constant of heat loss at a lower wafer speed than discussed in Section 3.2. In general, the solutions found for the symmetric condition, shown in Figure 3-11, are indicative of the types of curve shapes one could expect for an asymmetric heat transfer condition. In this case, grains would generally be growing from the bottom of the wafer towards the top, eliminating the centerline grain boundary that would degrade the efficiency of the solar cell. Convection within the melt should not be an issue for such a thin geometry.

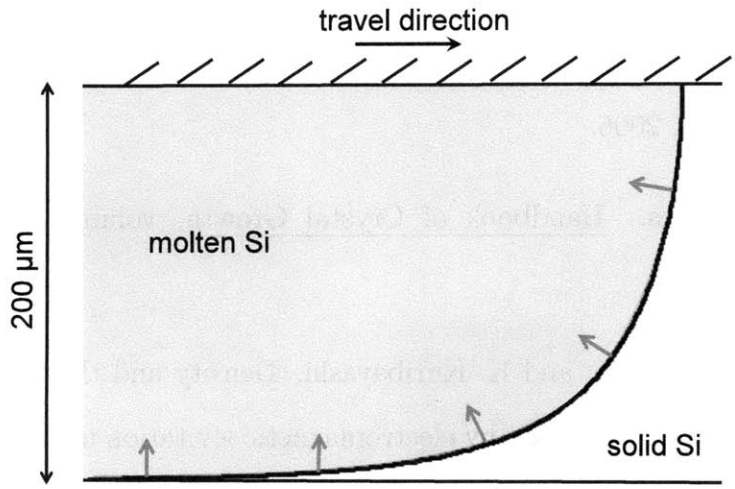


Figure 3-13: Schematic representation of solidification interface shape for asymmetric heat loss with adiabatic boundary condition at the top of the wafer.

This model has illuminated the relationship between the solidification interface shape and the wafer pull speed for a given set of conditions, including surrounding furnace temperature, wafer thickness, and backing plate properties. These parameters could be adjusted within the model to find the growth conditions required to produce a particular interface curvature at a certain speed which fits well with other processing steps. The model has also predicted a limiting wafer speed, beneath which there should be negligible interface curvature in the wafer.

References

[1] W.J. Boettinger, J.A. Warren, C. Beckermann, and A. Karma. Phase-field simulation of solidification. Annual Review of Materials Research, 32:163–194, 2002.

[2] P. Chen, Y. L. Tsai, and C. W. Lan. Phase field modeling of growth competition of silicon grains. Acta Materialia, 56(15):4114–4122, SEP 2008.

[3] L. Granasy, T. Pusztai, and J.A. Warren. Modelling polycrystalline solidification using phase field theory. Journal of Physics: Condensed Matter, 16(41):R1205–R1235, OCT 20 2004.

[4] Robert Hull, editor. Properties of Crystalline Silicon, chapter 4 - Thermal Properties. IET, Books 24x7., 2006.

[5] D.T.J. Hurle and R.W. Series. Handbook of Crystal Growth, volume 2A, chapter 3. North-Holland, 1994.

[6] Y. Inatomi, F. Onishi, K. Nagashio, and K. Kuribayashi. Density and thermal conductivity measurements for silicon melt by electromagnetic levitation under a static magnetic field. International Journal of Thermophysics, 28(1):44–59, Feb 2007.

[7] St G. Mueller, R. Eckstein, D. Hofmann, J. Fricke, R Horn, H Mehling, O Nilsson, and R Hofmann. Experimental and theoretical analysis of the high temperature thermal conductivity of monocrystalline sic. Materials Science Forum, 264-268(1):623–626, 1998.

[8] W.C. O'Mara, R.B. Herring, and L.P. Hunt, editors. Handbook of Semiconductor Silicon Technology. Noyes Publications, 1990.

[9] N. Shamsunder and E.M. Sparrow. Analysis of multidimensional conduction phase-change via enthalpy model. Journal of heat transfer, 97(3):333–340, 1975.

[10] D.M. Stefanescu, G. Upadhya, and D. Bandyopadhyay. Heat transfer-solidification kinetics modeling of solidification of castings. Metallurgical and Materials Transactions A, 21(3):997–1005, March 1990.

[11] YS Sung, H Takeya, K Hirata, and K Togano. Specific heat capacity and hemispherical total emissivity of liquid Si measured in electrostatic levitation. Applied Physics Letters, 83(6):1122–1124, Aug 11 2003.

[12] C.R. Swaminathan and V.R. Voller. A general enthalpy method for modeling solidification processes. Metallurgical and Materials Transactions B, 23(5):651–664, 1992.

[13] J.A. Warren, T. Pusztai, L. Kornyei, and L. Granasy. Phase field approach to heterogeneous crystal nucleation in alloys. Physical Review B, 79(1), Jan 2009.

[THIS PAGE INTENTIONALLY LEFT BLANK]

Chapter 4

Nucleation of Undercooled Silicon at Various Substrates

4.1 Motivation for Nucleation Study

In any zone-recrystallization process, the preferred mechanism of solid silicon crystallization is continuous growth from the already-solidified region of the crystal, rather than nucleation of a new grain on the substrate material upstream of the solid-melt interface. The character of this crystallization depends on the temperature profile imposed upon the wafer, but also on the interfacial energy between substrate and melt, which will lower the energy barrier for nucleation of the solid. We can differentiate between different substrates by measuring the amount of undercooling below the melting temperature that molten silicon will undergo before heterogeneously nucleating on the substrate. A substrate that allows a large level of subcooling before molten silicon nucleates will be less likely to provide nucleation sites for a directionally solidifying wafer.

Several studies have attempted to measure the homogeneous nucleation behavior of silicon by reducing contact with foreign materials that could cause nucleation.

Studies have measured up to 350°C of undercooling for levitated silicon droplets [13] and silicon surrounded by a liquid flux of SiO_2-BaO-CaO [20]. Dutartre [5] found a maximum undercooling of 240°C for silicon in contact with SiO_2 layers created by both thermal growth and chemical vapor deposition, however the use of optical detection of solidification and separate thermocouple measurement led to large margins of error in undercooling determination, and the performance of other substrate materials is still unknown. The goal of this research is to determine how much the nucleation barrier, and thereby the level of undercooling, is reduced as a function of the substrate material, as well as determine causes for and thereby reduce variability in this undercooling.

4.2 Theory of Surface Energy and Nucleation Behavior

Solidification is a discontinuous phase transformation which requires the formation of a nucleus of the solid phase in order to begin. Nucleation is necessary due to the positive free energy associated with the interface between solid and liquid phases. As the system cools below the melting temperature of a pure material, the free energy of the solid phase becomes lower than that of the liquid phase, and there exists a driving force to convert to solid in order to reach the lowest-energy state. However, there is an energy barrier to this transition stemming from the requirement to form an interface between phases. In the classical case of a spherical solid nucleus of radius r forming in a liquid system [18], the overall change in free energy is given by

$$\Delta G = \frac{4}{3}\pi r^3 \Delta G_v + 4\pi r^2 \sigma \tag{4.2.1}$$

where σ is the solid-liquid interfacial energy per unit area and G_v is the volumetric free energy difference between the solid and liquid phases. This change in free energy must be negative in order for the nucleus to be stable and continue to grow. This equilibrium between solid and liquid for a nucleus of a critical radius r^* is shown in Figure 4-1.

The free energies of solid and liquid bulk phases are temperature dependent, generally defined as $G = H - TS$. In equilibrium, $G^L = G^S$ at T_m and it can be assumed that the difference between specific heats of the solid and liquid phases is negligible for small $\Delta T = T - T_m$. The volumetric free energy difference between solid and liquid therefore depends on the level of undercooling below the melting temperature as

$$G^S - G^L = \Delta G_v = \frac{L_v \Delta T}{T_m} \tag{4.2.2}$$

where L_v is the latent heat of fusion per unit volume [18]. The equation shows that the transformation from liquid to solid becomes more favorable as temperature decreases below the melting point, T_m.

The barrier for nucleation can be decreased significantly by the presence of a foreign particle or boundary, which can act as a favorable site for heterogeneous nucleation. In the classical description of heterogeneous nucleation, the nucleation barrier is reduced by the fact that a hemispherical nucleus can form at the wall, such that the overall change in free energy becomes

$$\Delta G_{het} = V_s \Delta G_v + A_{SL}\sigma_{SL} + A_{SW}\sigma_{SW} - A_{WL}\sigma_{WL} \tag{4.2.3}$$

Thus the presence of a wall or impurity particle can facilitate the nucleation of the solid (S) phase, as the last term in the above equation reduces the interfacial energy contribution from the elimination of some interface area between wall (W) and liquid (L). The amount by which the nucleation barrier is decreased should depend on the

properties of the particle or wall material. The interfacial energy between wall and liquid, σ_{WL} is often assumed to be equal to that between wall and solid, σ_{SW}, but if it is in fact significantly greater than σ_{SW}, then there is an additional benefit to forming a solid nucleus that reduces the interface between liquid and wall. Another way to look at this would be that a very small value of σ_{SW} would make nucleation very favorable. For two different wall materials in contact with a liquid phase, any difference in the energy of the liquid-wall or solid-wall interfacial properties would make one wall material more favorable for nucleation. Different properties could stem from different crystal structures or grain orientations of the wall material.

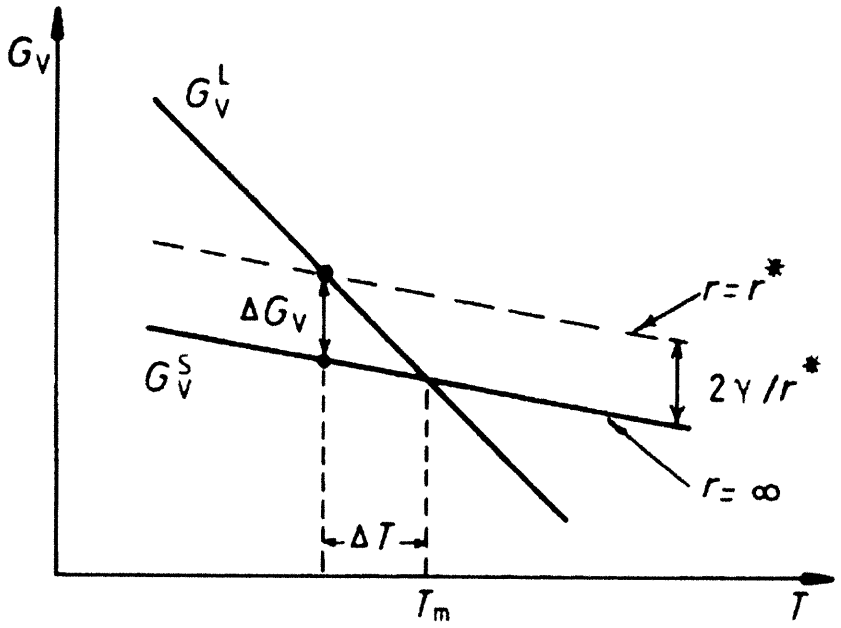


Figure 4-1: Volumetric free energy as a function of temperature for solid and liquid phases. Dotted line includes increased energy of solid nucleus due to interfacial energy σ_{SL} [18]

One way to characterize the free energy change for heterogeneous nucleation at a particular wall material is by contact angle θ between the solid nucleus and the wall.

This relationship can be represented by

$$\Delta G_{het} = \{\frac{4}{3}\pi r^3 \Delta G_v + 4\pi r^2 \sigma\} S(\theta) \tag{4.2.4}$$

where

$$S(\theta) = (2 + cos\theta)(1 - cos\theta)^2/4 \tag{4.2.5}$$

It can be shown that the smaller the contact angle, the greater the reduction in energy barrier to heterogeneous nucleation. However, it is difficult to experimentally measure the contact angle of a solid silicon nucleus forming at such high temperatures given the high reactivity of molten silicon.

Another approach to measurement of interfacial energies is to study the liquid-substrate behavior in a gaseous medium, such as air or vacuum. By measuring the wetting angle of a liquid silicon droplet on various substrate materials, one could determine the relative interfacial energies for different wall materials with regard to molten silicon. Several researchers have measured the wetting behavior of molten silicon using the sessile drop method [3,10,22], either in vacuum or inert atmosphere. Whalen et al. reported a contact angle for molten silicon of 40° ± 5° on SiC and 43° on hot pressed Si_3N_4 at 2600°F (≈1427°C), the latter decreasing to 10° as temperature was increased to 2700°F. However, Croll et al. measured the contact angle of molten silicon on substrates coated with various powder coatings, as often used in cast silicon manufacturing, and obtained measurements of 10°, 80°, and 150° for powders of Si_3N_4, SiO_2, and BN powders respectively [3]. It's true that a powder substrate would yield higher θ values than a solid substrate, but the relative behaviors of the different materials tested should be the same. This behavior would indicate that Si_3N_4 had the lowest interfacial energy of the three powders tested, and BN the highest of the three. However, because this study of liquid-silicon/substrate relationship was conducted with the third phase being vacuum atmosphere, it is difficult to translate

the findings into a prediction of the behavior of a liquid-silicon/solid-silicon/substrate system, because changing that third component can have varying effects on the relative interfacial energies which cause the wetting angles. However, this reported data implies that silicon has a low interfacial energy with silicon nitride, which would make it the most favorable material upon which to nucleate. In contrast, the data indicates that Si-SiO_2 has a high interfacial energy, such that nucleation of solid silicon would be less favorable.

In order to specifically determine the nucleation behavior of liquid silicon on various substrate materials, this study measures the amount of undercooling below the melting temperature that molten silicon is able to reach before it nucleates in contact with the substrate. The larger the undercooling below T_m, the less likely the substrate material is to cause new nucleation sites in a recrystallizing sample and thereby initiate new grains of solid silicon.

4.3 Observation of Recalescence

One approach to measuring the undercooling level of molten silicon before nucleation is to utilize the emissivity difference between solid and liquid silicon to optically indicate the onset of freezing. The emissivity of solid and liquid silicon at infrared wavelengths near T_m are reported to be 0.65 and 0.20 respectively [21]. This property as allowed many researchers to visually observe the solidification phenomenon through microscopes or cameras [4,5,9,16]. If the silicon subcools below T_m before solidifying, there will be a recalescence event, where the latent heat of fusion is released and the silicon heats up to the melting temperature to change phase completely to solid [7]. Thus the solidification event can be observed both optically, in the emissivity change, and thermometrically, in the temperature increase upon recalescence.

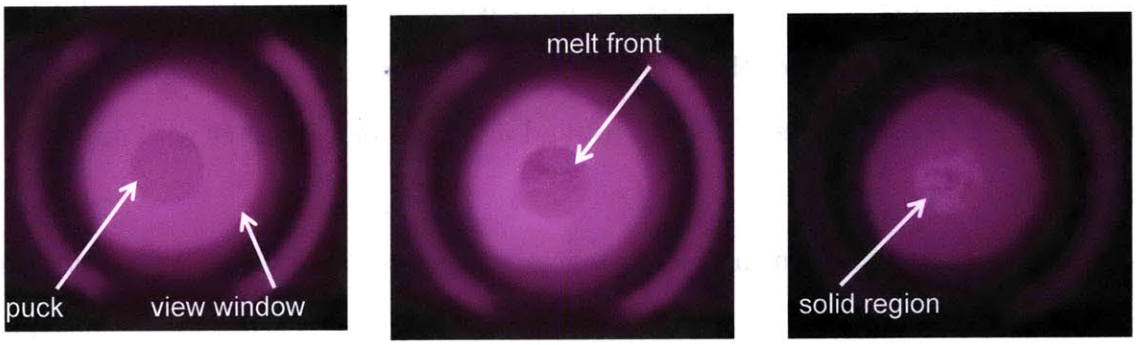
Efforts to observe the emissivity change and recalescence event using

thermocouples and a video camera are described here. Puck-shaped samples of high purity silicon (99.999%) were cut from a silicon rod of 8.28 mm diameter and etched in an $HF/HNO_3/HCOOH$ solution to remove saw damage and subsequently annealed in O_2 to form a dry oxide coating. The puck is then placed on a SiC plate in a small box furnace with a viewing window at the top. Silicon carbide was used for its high-temperature stability and low likelihood of contaminating the silicon. Resistive silicon carbide "Starbar Type RR" heating elements from I-Squared-R Element Company were used in conjunction with an phase-angle-fired SCR power controller from Watlow, which allowed better control of furnace temperature than the simpler on-off heater control option, in order to have careful control of the sample temperature and heating rates near T_m. An Omega controller was used to implement PID control of the temperature according to a pre-determined program. A CCD camera records an image of the sample through a filter stack, including an IR lens, a cold mirror, a cobalt blue welding lens, and a neutral density filter with an optical density of 1.

One challenge in measuring undercooling by recalescence and thermocouples lies in finding appropriate thermal insulation of high purity for furnace construction, that could withstand temperatures above 1400°C for extended periods of time. Ceramic insulation options considered for use in the furnace were composed of Al_2O_3 and SiO_2 and had rigid, non-flaky structures, preferably machinable. Among the insulations considered was Fiberfrax Duraboard 2600, rated to 1427°C, which was conveniently cuttable with a utility knife and underwent minimal degradation during extensive testing, after an initial burnoff of binders. In an effort to avoid aluminum-containing materials for purity purposes, a pure silica insulation was obtained from the Kennedy Space Center gift shop – LI-900 is a highly porous matrix of silica fibers used as part of the thermal protection on NASA space shuttles. However, the silica could not withstand extended exposure to temperatures above 1400°C, softening and

losing rigidity, and was deemed unsuitable for this furnace application. Another possible candidate for furnace walls was Vesuvius Zyafoam 75, a rigid silica-based insulation of slightly higher density than other insulations considered – this material maintained rigid corners and precise cuts, unlike the Duraboard 2600, which tended to erode with extensive handling. However, both materials were used together to construct a working furnace. Other useful materials include Zircar Al-R/H, a colloidal alumina rigidizer used with softer insulation blocks, and Aremco Ceramabond, a high-temperature ceramic adhesive useful for assembling sample-holder platforms.

Images of the Si puck during melting and resolidifying are shown in Figure 4-2. The large purple circle represents the circular viewing window through which the darker circular puck is seen in the center, in Figure 4-2(a).



(a) Sample before melting. (b) During melting. (c) During freezing.

Figure 4-2: Screenshots of oxide-coated Si puck melting and resolidifying.

When the sample is heated to the melting temperature, a wrinkle appears on the puck surface indicating the melting front shown in Figure 4-2(b), as silicon shrinks upon melting. This wrinkle is probably the deformation of the oxide coating as the silicon volume decreases. The molten sample is then cooled until solidification is observed by the appearance of a brighter region which grows across the sample, shown partially frozen in Figure 4-2(c). Clearly, solidification can be observed with this method, but the sample temperature must also be monitored simultaneously to determine the undercooling level.

To measure the sample temperature, a Type R thermocouple was used to measure the temperature of the underside of the SiC plate holding the sample, and the furnace was heated at 11.5°C/min, held constant for 3 minutes, and cooled down at 10.0°C/min. The temperature was recorded using a Measurement Computing USB-TC box for data acquisition. Deviations in the sample temperature from the constant slope during heating and cooling indicated a change in phase, as shown in Figure 4-3. From this data, it is evident that there is a significant lag in measured temperature from the true temperature of the sample, and a more precise apparatus is needed to measure the absorption and release of latent heat. In this case, differential scanning calorimetry (DSC) would give an appropriate measurement of the desired events.

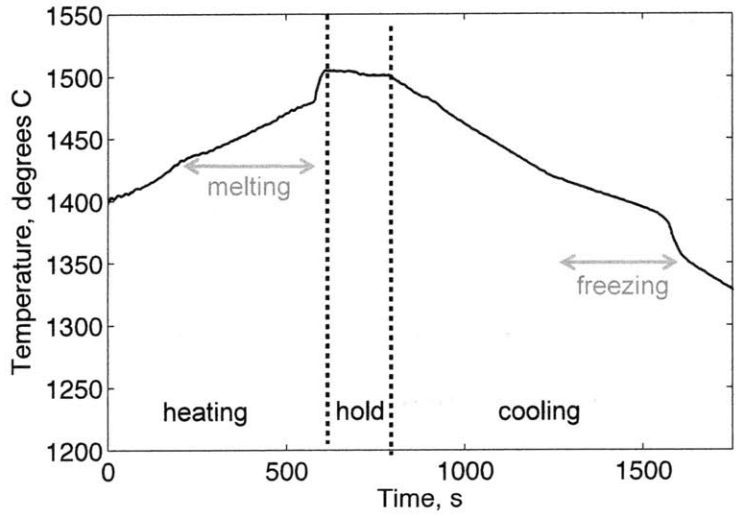


Figure 4-3: Thermocouple measurement of melting and freezing of Si puck.

4.4 DSC Experiments

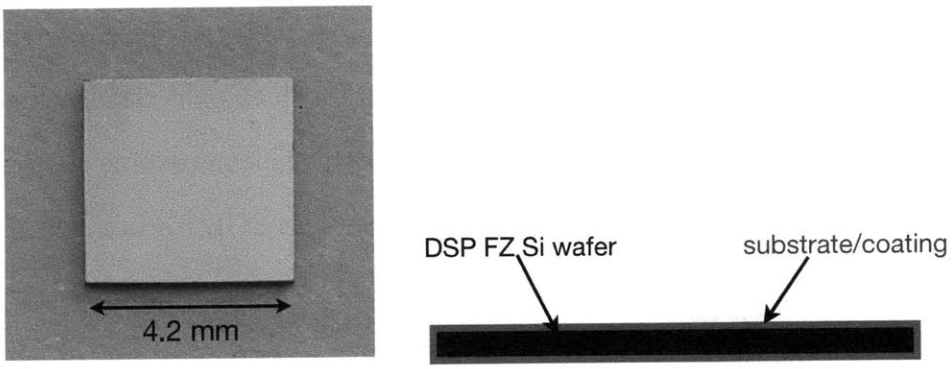
Differential scanning calorimetry (DSC) was used to measure the level of undercooling below the melting temperature for various substrates of interest. Samples were tested on a Netzsch STA 449 Jupiter with DSC and thermogravimetric analysis (TGA)

capabilities. The STA is equipped with a silicon carbide furnace tube which can reach temperatures up to 1500°C. The sample is placed in a small round crucible with a flat bottom, covered by a removable lid with a small hole in it for any reaction gases to escape. This test crucible, along with an empty reference crucible, is placed on a sample carrier assembly which consists of a platinum platform under each crucible. Thin thermocouple wires are soldered to the bottom of each platform to measure the sample temperature as well as the heat flow between the two crucibles. Using the differential heat flow between crucibles and the sample mass, the STA software calculates the amount of heat released or absorbed by the sample during a reaction, along with the temperature at which the reaction occurs.

Samples consisted of double-side-polished float zone wafers cut into 4.2-mm squares, and the substrate under investigation was applied as a coating on the sample. Single-side polished wafers were considered, but surface roughness added a source of variability in the potential results. Circular disks were also tried, but similar results were achieved for squares, which were easier to prepare from large wafers. Another sample option was silicon pellets from MEMC, with an almost-spherical shape that would reduce the amount of shape-change the sample would undergo upon melting, but the impurity levels and crystal structure of these pellets were unknown and therefore difficult to make conclusions from. Thus laser-cut squares of double-side polished wafers were primarily used for DSC experiments. Before application of the coating to the wafer squares, they were cleaned using the standard RCA I process and etched in an $HF/HNO_3/HCOOH$ solution. Figure 4-4 shows a photograph and representative schematic of a prepared sample before entering the DSC.

4.4.1 Crucible Properties

Initial attempts to measure undercooling utilized alumina crucibles to hold samples in the DSC. However, the oxide and nitride coatings routinely stuck to the alumina



(a) Photograph. (b) Schematic.

Figure 4-4: Square cut of polished float-zone wafer prepared with applied coating before testing by DSC.

when the silicon became molten, which often caused cracking of the crucible upon cooling due to different coefficients of thermal expansion between the alumina and the silicon. This sticking inhibited the reusability of the crucibles, and also damaged the structural integrity of the crucible bottoms due to small cracks. Furthermore, interaction between the alumina-coating reaction and the nucleation behavior of silicon could not be ruled out.

To avoid this reactivity between alumina crucibles and silicon, custom crucibles were fabricated in the lab from graphite grade R6510, provided by SGL Carbon. This particular grade of graphite is used at SGL Carbon due to its thermal properties such that it can be coated with a layer of silicon carbide and undergo large temperature changes without thermal mismatch. Machined circular graphite crucibles were sent back to SGL Carbon for purification and coating in two layers of 50 μm each, for a total of 100 μm, as is the SGL standard procedure for continuous coatings of SiC of graphite. It should be noted that any graphite dust particles left inside the crucible due to a lack of thorough cleaning can act as seed sites for the coating layer, and result in undesirable surface roughness on the crucible where the sample would contact it. Softened SiO_2 on the sample surface tends to stick to these large roughness features, preventing release from the crucible after testing.

In order to reliably prevent the sample from sticking to the test crucible, the silicon carbide layer must be sufficiently oxidized to create a thick oxide layer which will not stick to the SiO_2 coating on the sample. The pristine silicon carbine coating texture is shown in Figure 4-5, just after the coating process at SGL Carbon.

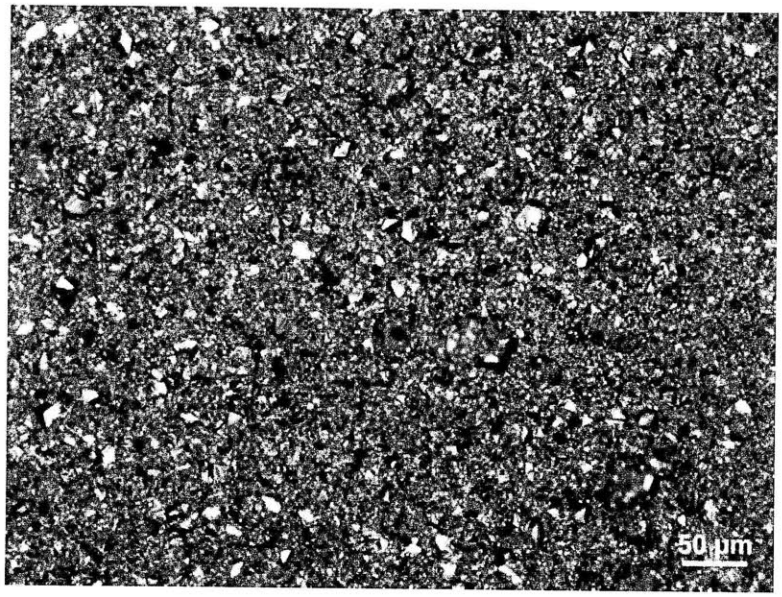


Figure 4-5: Surface texture of silicon carbide coated graphite crucible before oxidation.

To achieve this thick oxide layer, crucibles were oxidized for >12 hours at 1450°C in air until a scaly-textured oxide layer formed in the bottom of the crucible interior. The formation of this oxide layer with scaly texture was unique in that it did not form uniformly over the entire SiC surface, but rather began in small circles radiating from a center point, shown in Figure 4-6, and then gradually grew to cover the whole surface with further dwell time at high temperatures. The non-scaly oxide layer can be seen outside of the scaly colored circle in the image.

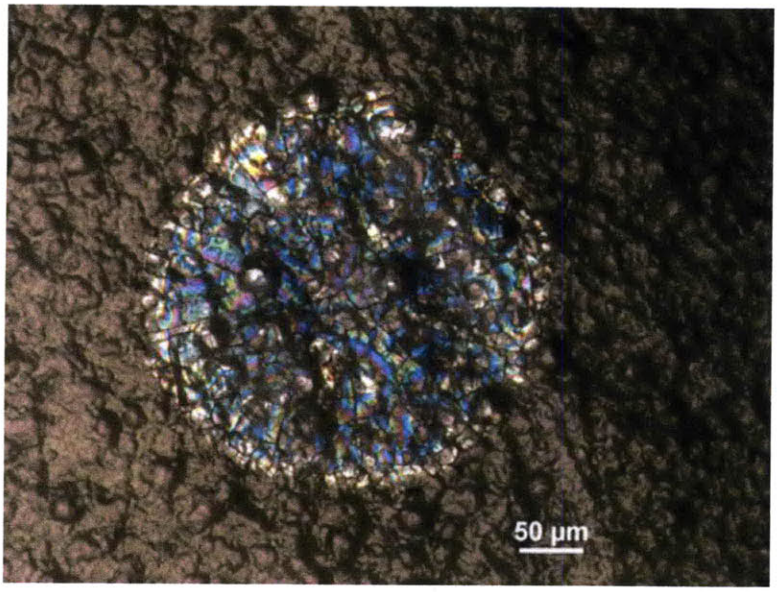


Figure 4-6: Surface texture of silicon carbide coated graphite crucible with start of scaly oxide growth.

4.4.2 Coating Preparation

Various coatings on the silicon samples were tested for their influence on nucleation. The first coating was dry thermal oxide, grown at 1100°C under flowing dry oxygen in a quartz tube furnace. Dry thermal oxidation produces an amorphous SiO_2 layer and occurs via the following reaction [8].

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \tag{4.4.1}$$

The second coating was wet thermal oxide, grown at 1000°C in a saturated steam environment in a quartz tube furnace. Wet oxidation is often favored over dry oxidation due to its fast growth kinetics, since H_2O has a higher solubility in SiO_2 than O_2 by about three orders of magnitude [23].

$$Si(s) + 2H_2O(g) \rightarrow SiO_2(s) + 2H_2(g) \tag{4.4.2}$$

The third coating was silicon nitride deposited by plasma-enhanced chemical vapor

deposition (PECVD). The deposited amorphous nitride layer had a refractive index of 2.1, and was deposited using a gas flow ratio, R_G, of 0.46, defined as

$$R_G = \frac{\Phi_{SiH_4}}{\Phi_{SiH_4} + \Phi_{NH_3}} \tag{4.4.3}$$

and therefore the film contains some concentration of H, on the order of 10-20% [11].

Each sample was placed in a crucible with an alumina cover in the DSC to be heated and cooled in air at a rate of 10°C/minute. The crucible lid increased the temperature uniformity of the sample for better accuracy of the heat flow data. The difference in temperature between the onset of melting during heating and the onset of freezing during cooling represents the undercooling for each sample.

4.5 Results of DSC Experiments

Figure 4-7 shows an example of data collected showing undercooling of the sample, in this case, with a 1μm dry oxide coating. The sample heats up along the lower grey curve, and the sample melting is signified by a downward peak representing the absorption of latent heat. Once the sample reaches 1450°C, it begins cooling at 10°C/min until the solidification peak is observed. In this particular data set, the large undercooling of 125°C achieved by the sample led to a very rapid solidification and therefore very fast release of latent heat. The exothermic nature of this sudden reaction led to a slight increase in the measured temperature of the sample, shown by the retrograde character of the solidification peak, before the sample continued to cool according to the prescribed program.

The overall comparison of undercooling results for sample types with the highest undercooling is shown in Figure 4-8. Most data sets, as seen further in the following sections, contained a bimodal distribution of undercooling levels for a particular sample type. The maximum undercooling measured can be considered as the true

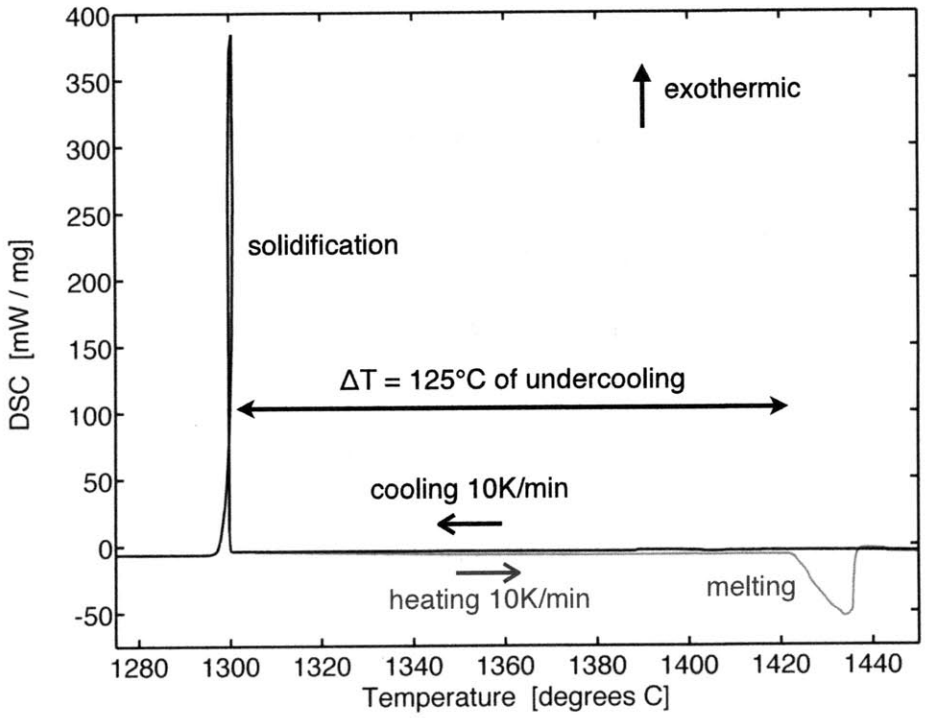


Figure 4-7: Example DSC results for 1μm dry oxide coating with measured ΔT = 125°C. Grey curve represents heating, black curve represents cooling.

measure of nucleation behavior for a particular material, and the lower-ΔT group of data points were likely the result of other defects or impurity particles. The dry oxide coating sustained the highest maximum undercooling levels, up to 141°C below the melting point, indicating a high interfacial stability with the molten silicon which should reduce the probability of unwanted heterogeneous nucleation. The wet oxide overall showed slightly lower levels of undercooling with a maximum of 130°C, and the silicon nitride coating consistently showed low undercooling levels below 17°C. This finding indicates that a nitride substrate would be more likely to cause nucleation of new grains at low levels of undercooling in a recrystallization process. However, deposition of a nitride layer over an inner dry oxide layer reduced the undercooling from the >100°C typical of dry oxide to a maximum of <60°C, the causes of which will be discussed in the following sections. Variations in the processing and coating thicknesses were investigated, as described below.

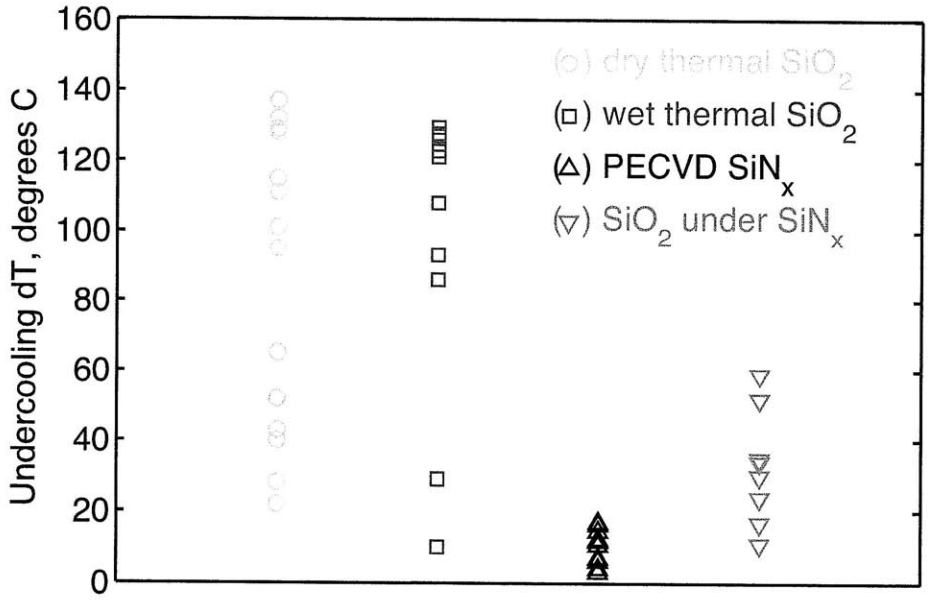


Figure 4-8: Summary of undercooling levels measured on various coating materials and thicknesses. Dry and wet oxide layers were grown in a two-part oxidation for a total of 40 and 20 hours, respectively. The nitride consists of a 160nm layer. The composite oxide-nitride coating includes a two-part dry oxidation and 40nm of silicon nitride.

4.5.1 Dry Oxide Coating Results

Undercooling results of silicon samples coated with various thicknesses of dry thermal oxide are shown in Figure 4-9. The first data set shows samples coated with a 1-μm layer of dry oxide. The data shows a gap between samples with very high levels (>100°C) of undercooling and samples with much lower (<60°C) undercooling. The high ΔT samples prove that the dry oxide material is not the cause of nucleation at lower ΔT, and that it is capable of sustaining large undercooling before solid nuclei are stable enough to grow continuously. However, some samples may have another factor, such as a foreign particle or a microcrack, that might cause nucleation before a larger undercooling is reached. If no such factors are present, the sample is able to cool more than 100°C below T_m before nucleation.

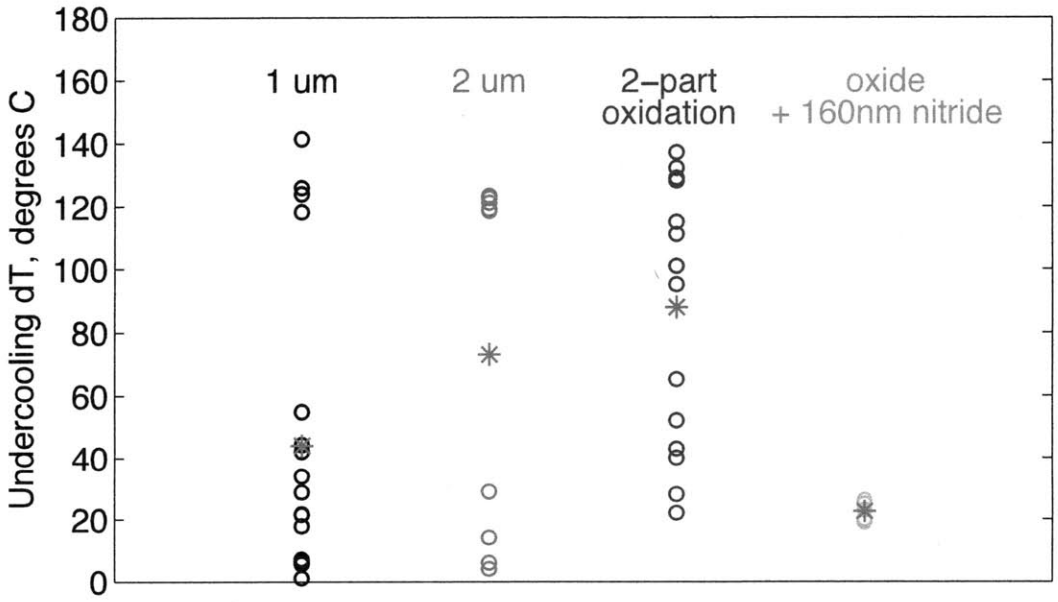


Figure 4-9: Undercooling results for dry thermal SiO_2 coatings. Grey asterisks represent mean values of each data set.

One hypothesis for causes of nucleation at low undercooling levels was the deformation that some samples underwent while molten. Several of the large-ΔT samples retained their rectangular shape throughout melting, as shown in Figure 4-10. The surface texture became more wavy but the corners remained sharp. The

sphere of shiny silicon in the middle was the last part to solidify, bursting through the oxide. To probe this theory of deformation-caused nucleation, samples were prepared with a thicker dry oxide layer of 2 μm, grown continuously in an oxygen atmosphere at 1100°C for ~130 hours, to see if the increased coating thickness could consistently constrain the sample shape. The results for this set of samples is shown in the second column of Figure 4-9. It is clear that the proportion of samples with small undercooling levels is lower than that of the 1μm samples, and the mean value of undercooling, shown as grey asterisks, has also increased. However, the thicker oxide did not have a significant effect on reducing sample deformation, but the frequency of high undercooling increased nonetheless.

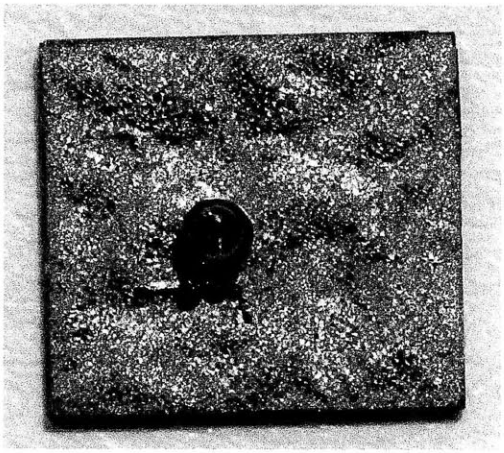


Figure 4-10: Dry oxide-coated sample with large undercooling and minimal deformation from original rectangular shape.

Another possible reason for the variation in undercooling data might be any nonuniformity in the oxide coating, given that the thermal growth is conducted with samples resting on a quartz sample holder. Regions of the sample in contact with the holder may have more limited access to the oxygen environment and thus oxide growth may be slower. To avoid this scenario, a batch of samples was prepared with a two-part oxidation, with each sample rotated 180° after 20 hours at 1100°C, for a total of 40 hours of growth. In this case, every point on the sample surface should have at least 1 μm of oxide. The data from this sample set is shown in the

third column of Figure 4-9. While the variation in undercooling is larger, there were no samples with $\Delta T<20°C$, and the mean value of the set was higher than that of the 2μm samples, as shown by the grey asterisks. These results indicate that a full 2 μm oxide is not necessary to improve the consistency of high undercooling, which is important because the long time required to grow such an oxide is not practical in many industrial situations. Overall, dry oxide looks very promising because it will not be a cause for nucleation unless the sample is recrystallizing wafer is cooled 120°C below T_m, which is unlikely to occur in the zone-melt furnace.

4.5.2 Wet Oxide Coating Results

The undercooling behavior of wet thermal oxide coatings is shown in Figure 4-11. The first wet oxide coating to be investigated was a 1-μm wet oxide grown under saturated steam conditions at 1000°C for 4 hours. Saturated steam conditions are achieved by heating high-purity water to 89°C and bubbling high-purity O_2 gas through it and into the quartz tube furnace. While the mean value of undercooling was 27°C, the maximum value observed was 77°C. This high maximum indicated that wet oxide had the potential to suppress nucleation, but that some other factors might be causing some samples to nucleate at lower undercooling levels. The lower maximum ΔT value could be related to the fact that fast oxidation under steam conditions can lead to dangling bonds at the oxide-silicon interface, a high-energy situation which might also favor nucleation [6, 8].

Another possible explanation was that the oxide coating was too thin to physically constrain the deformation of the samples when molten, causing unwanted geometrical irregularities that would trigger nucleation. An example of such deformation is shown in Figure 4-12. Wet oxidation is known to yield a lower-density oxide than the dry process, which could explain the difference in performance for similar coating thicknesses. Thus a 2-μm oxide layer was grown, using similar conditions to

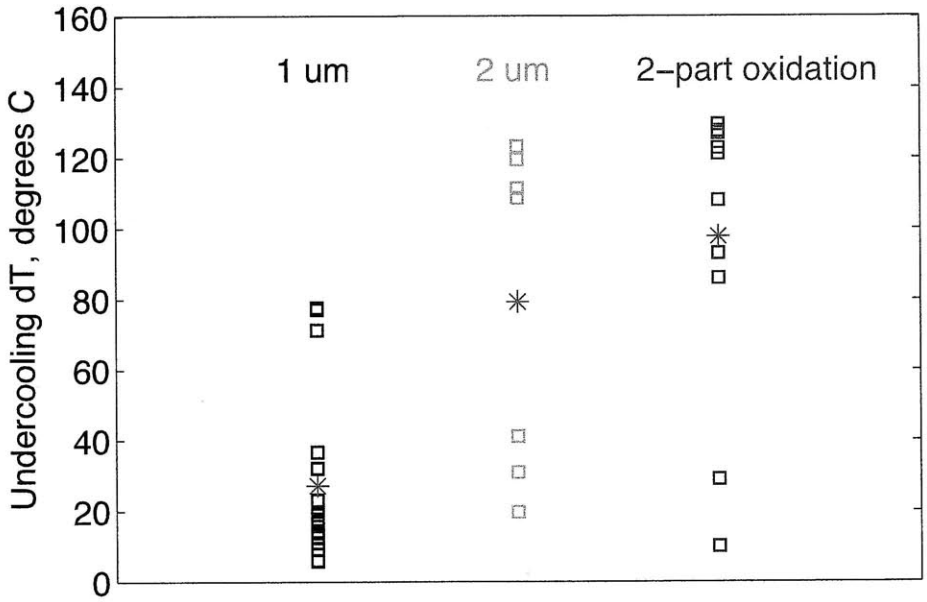


Figure 4-11: Undercooling results for wet thermal oxide coatings. Grey asterisks represent mean values of each data set.

the aforementioned samples, but for 20 hours total. In this case, the maximum undercooling level observed was significantly increased over the 1-μm wet oxide, showing ΔT = 123°C. This undercooling level comes much closer to what was seen for the dry oxide levels, and the frequency of higher undercooling behavior increased as well. The average ΔT for this set of samples was 79°C, indicating that the thicker oxide coating improved the suppression of nucleation. These results indicate that any interfacial dangling bonds due to the fast wet oxidation were not significant causes of nucleation.

Similar to efforts undertaken with the dry oxide samples, a batch of samples were oxidized in two parts under steam atmosphere, rotating their orientation relative to the sample holder after 10 hours, for a total of 20 hours in the oxidizing steam environment. The data collected from these samples are depicted in the third column of Figure 4-11. Again, the two-part oxidation process improves consistency of high undercooling levels in the wet oxide samples. This sample set shows a maximum of ΔT = 131°C with the highest average undercooling of any other sample set. This

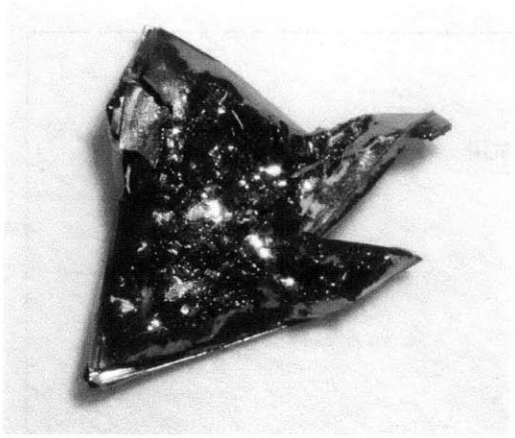


Figure 4-12: Wet oxide-coated sample with "folding" deformation from original shape.

result reinforces the idea that a uniform oxide coating of the silicon is required for the best performance in non-nucleation. This data also indicates that wet SiO_2 is practically equivalent to dry SiO_2 in terms of nucleation properties, which is beneficial since wet SiO_2 can be thermally grown at higher rates and is therefore more conducive to a high-throughput manufacturing process.

4.5.3 Silicon Nitride Coating Results

Undercooling results for silicon nitride coatings are shown in Figure 4-13. The 160nm silicon nitride layer was the first to be studied, yielding consistently low undercooling results – less than 17°C. The 160-nm nitride-coated samples very consistently deformed into more rounded shapes with rough, colorful surfaces and poorly defined corners, as shown in Figure 4-14(a).

It was initially hypothesized that the thinner coating layer of the nitride was allowing more morphological changes during melting that might influence the measured undercooling for silicon nitride. To attempt to reduce this deformation, a thicker nitride layer of 600nm was applied to a set of silicon samples. In this case, the nitride was thick enough to maintain the rectangular shape of the sample throughout the experiment, as shown in Figure 4-14(b). However, the 600-nm nitrided

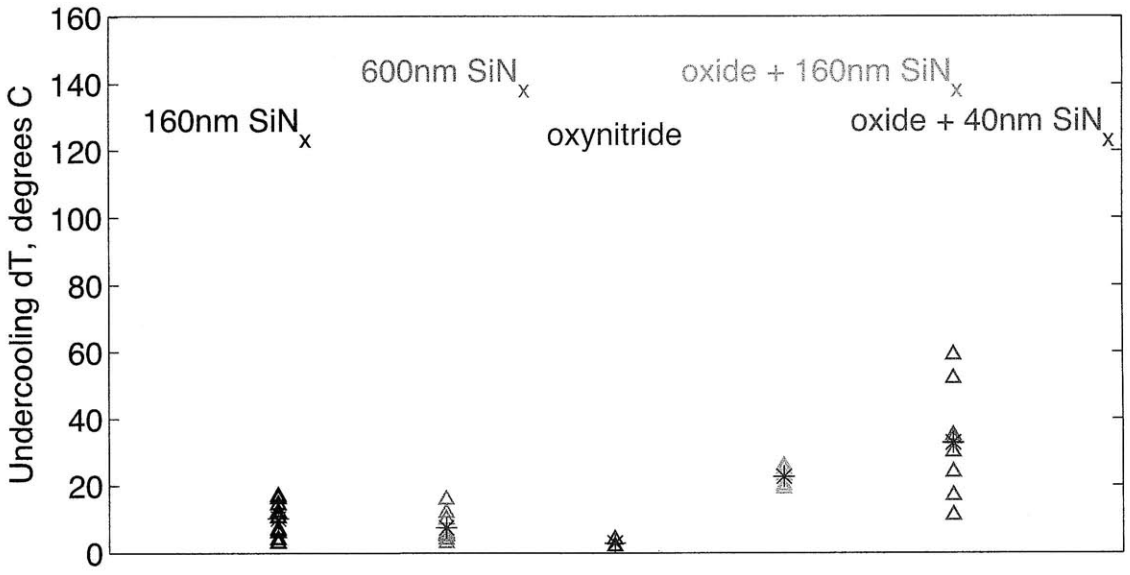
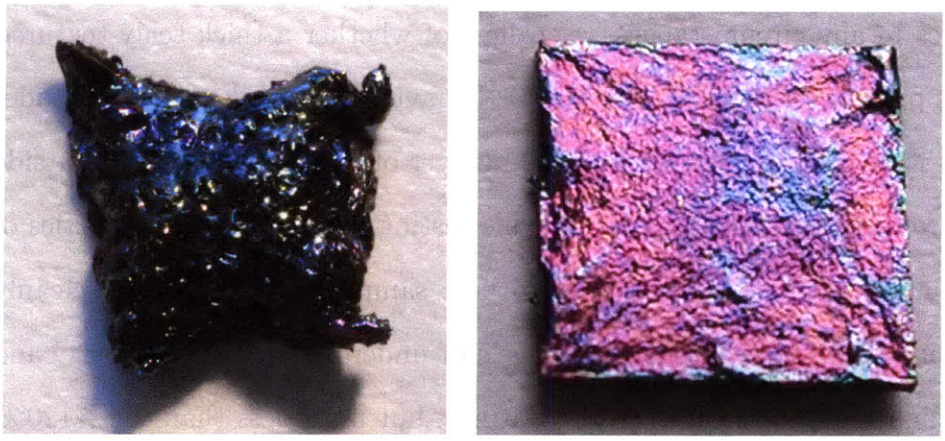


Figure 4-13: Undercooling results for silicon nitride coatings. Grey asterisks represent mean values of each data set.

samples did not reach undercooling levels greater than 17°C below T_m, shown in the second column of Figure 4-13, which indicates that the sample deformation was not responsible for the low undercooling of the thinner nitride coating. In fact, these results indicate that the nitride material itself is unable to sustain contact with metastable supercooled silicon and causes nucleation of the solid phase before $\Delta T = 17°C$. These results imply that the SiN_x substrate material will cause the most nucleation during crystallization.

As described earlier, the nitride coatings caused much lower undercooling levels than the thermal oxides, but the nitride material has a beneficial quality of releasing from SiC crucibles without sticking. As such, a batch of samples was prepared with an SiO_xN_y coating composition deposited by PECVD to see if moving the coating composition closer to that of silicon dioxide improved the undercooling behavior. The SiO_xN_y coating was deposited with a 2:1 ratio of N:O gases in the PECVD chamber, resulting in a layer with a refractive index of 2.0. The thickness of this coating layer was 500nm. As seen in the data shown in the third column of Figure 4-13, this oxynitride layer yielded the smallest undercoolings of any materials tested,



(a) 160nm Si_3N_4 coating (b) 600nm Si_3N_4 coating

Figure 4-14: Morphology of silicon nitride-coated samples for coating thicknesses of 160nm and 600nm after melting and resolidifying.

consistently less than 5°C below the melting point. This oxynitride coating also had an interesting texture post-melting, with parallel wrinkles oriented at 45 degrees from the sample edges, shown in Figure 4-15(b). This texture was much smoother and more uniform in color than that of a post-melting nitride-coated sample, shown in Figure 4-15(a).

(a) 600nm SiN_x coating texture (b) 500nm oxynitride coating texture

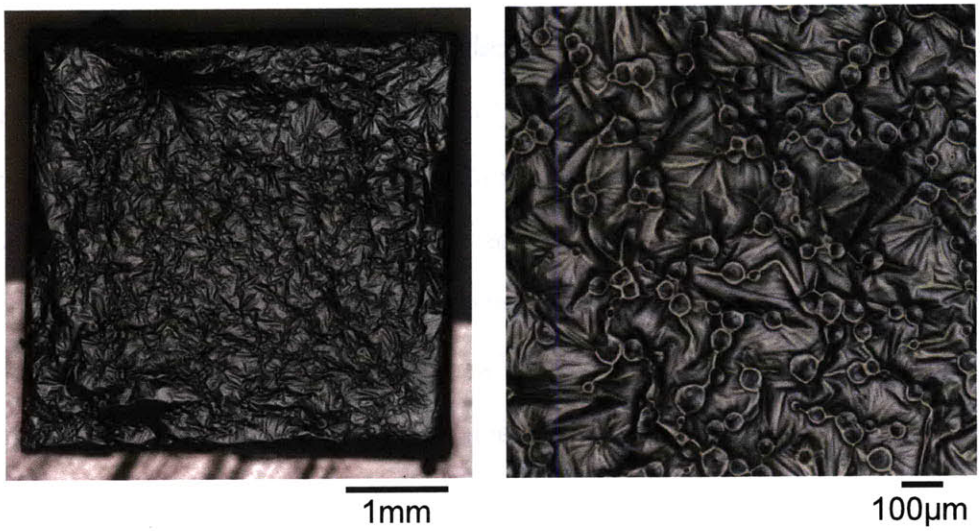
Figure 4-15: Optical micrographs of morphology of silicon nitride and oxynitride-coated samples after melting and resolidifying.

It has been noted that the nitride-coated samples did not stick to the silicon

carbide crucibles in any circumstances, regardless of whether a thick scaly-textured oxide layer was present on the SiC. Due to this behavior, several dry thermal oxide-coated samples were coated again with a 160nm layer of SiN_x to protect the outside of the sample from sticking to the crucible while testing the nucleation properties of the oxide in contact with the silicon. While these samples indeed released cleanly from the crucible, they showed very small levels of undercooling between 19°C and 26°C, slightly higher than data for nitride coatings, but much less than the >120°C undercooling levels seen for dry oxide prepared in the same batch. The data is shown both in Figure 4-9 and Figure 4-13. It was suggested that the nitride layer might react with or diffuse through the oxide coating at high temperatures and form an oxynitride coating layer for the silicon, which would increase its tendency to cause nucleation. Several samples were tested using a faster heating rate of 30 K/min to minimize the total time spent above 1000°C, but no improvement in the undercooling level was measured. However, both layers are still able to be etched away in a dilute HF solution after recrystallizing, via undercutting of the nitride layer and etching away the oxide layer, as evidenced by clean removal of both layers with flakes of SiN_x floating in the solution. This behavior indicates that the two capsule layers are still separate and distinct. Therefore the original SiO_2 was probably in sole contact with the silicon.

Another possible mechanism for the undercooling reduction caused by depositing SiN_x over the oxide capsule is high-temperature stress between the layers which could cause wrinkling or warping of their surfaces. Such wrinkles could create small features that would be favorable nucleation sites for undercooled silicon if their dimensions are on the order of the critical nucleus size for a particular temperature below T_m. An image of the surface texture of a sample with SiN_x over SiO_2 after recrystallization in the DSC is shown in Figure 4-16(a). This side of the sample was facing the SiC-coated crucible, and a wrinkled texture can be seen. These wrinkles, shown

larger in Figure 4-16(b), consist of circular and straight features, which may have resulted from the differing high-temperature behaviors of the two capsule materials. It is known that silicon nitride deposited by PECVD undergoes a densification process at high temperatures, during which the hydrogen incorporated in the film may be released [2, 19]. SiO_2 also undergoes softening above 1000°C which might render it more susceptible to strain due to thermally-induced stress from thermal expansion/contraction of SiN_x.



(a) Entire recrystallized sample surface. (b) Magnified view of texture.

Figure 4-16: Optical micrograph of bottom surface of DSC-recrystallized silicon sample coated with composite capsule of 160nm SiN_x over SiO_2.

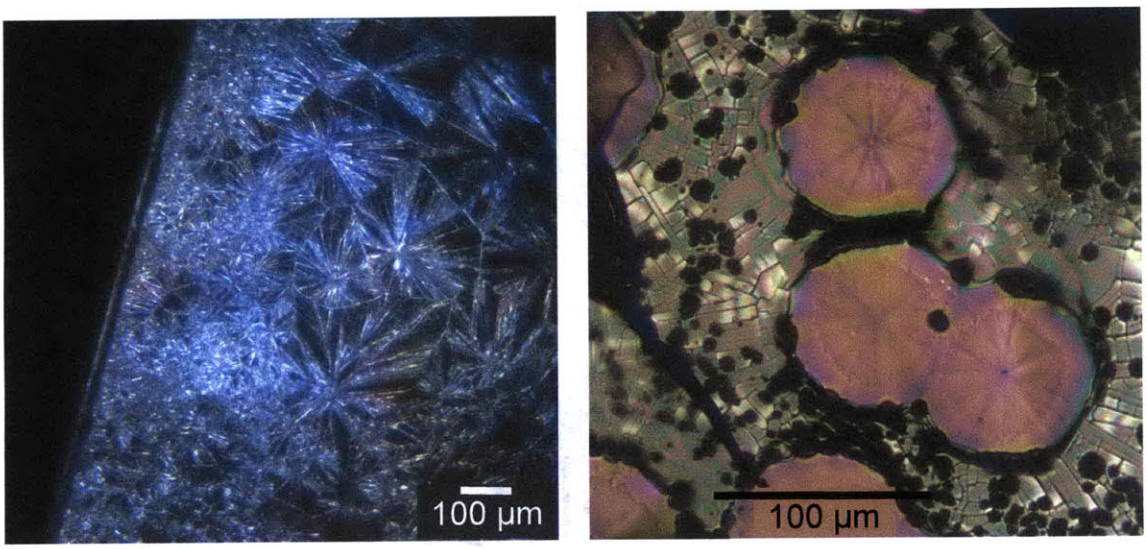
To minimize the possible influence of this structural change on the underlying SiO_2 capsule, the thickness of the nitride layer was reduced to 40nm. This alteration resulted in an increase of the maximum undercooling level to 56°C, as shown in the right-most column of Figure 4-13. This result supports the idea that a densification and CTE mismatch of the composite coating layers was causing the reduced undercooling, and that reducing the nitride layer thickness decreases its ability to apply stress to the oxide layer. Since the nitride layer is only needed as a release layer, its thickness can be reduced farther, to impart the least stress on the oxide layer, as long as a continuous layer is present to prevent sticking to

the crucible or backing plates. This capsule configuration looks the most promising for achieving large recrystallized grains without adhesion to backing plates in the zone-melt recrystallization furnace.

4.5.4 Surface Morphology

Optical microscopy revealed unique surface morphologies for the different coatings after re-solidification. In the case of the dry oxide coating with large undercooling, shown in Figure 4-17(a), there is an overall scale pattern, with each region having a central point from which striations radiate outwards; these central points may represent nucleation centers. These nucleation sites are very finely spaced near the sample edge, indicating that nucleation was initiated in this region, and as the released latent heat caused the sample temperature to increase, nucleation occurred with lower frequency in the inner areas of the sample, resulting in larger distances between nucleation sites there. Growth from each nucleus proceeded quickly enough for nucleus boundaries to impinge on each other, forming polygonal regions on the surface.

In contrast, samples coated with silicon nitride revealed many small colorful circle morphologies, as shown in Figure 4-17(b), which suggest that these small portions around each nucleation site froze more quickly before the sample temperature was raised and the surrounding areas froze more slowly as heat was removed. However, due to the small overall undercooling, nucleation sites did not grow fast enough to touch the next nucleation site as in the dry oxide case, which is consistent with studies of crystal growth velocity with undercooling level by Panofen and Herlach [16]. The size of these nucleus circles should be proportional to the amount of sensible heat removed from the molten silicon to subcool it to the temperature at which nucleation occurred. These observations show further insight into the different behaviors caused by different coating materials.



(a) resolidified 1-μm dry SiO_2 coating

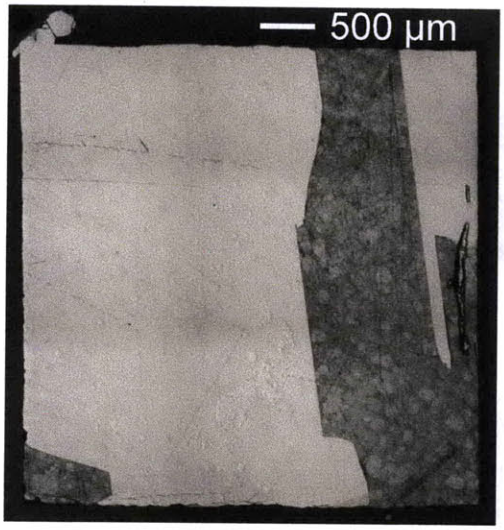
(b) resolidified 160-nm SiN_x coating

Figure 4-17: Optical micrographs of surface morphologies of undercooled and resolidified samples.

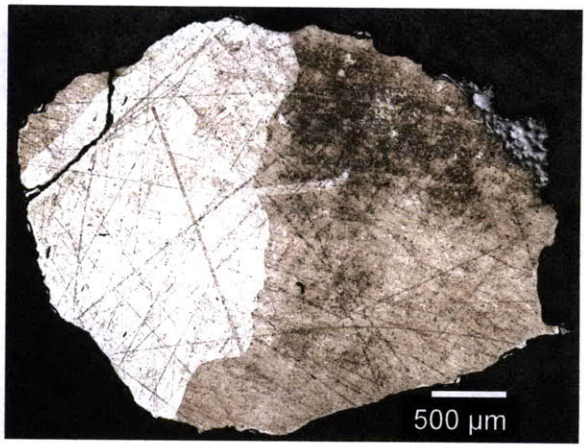
4.5.5 Grain Structure

To get a closer look at the recrystallized grains in the DSC samples, they were cross-sectioned and texture-etched. Samples were first embedded in clear epoxy and polished to a smooth finish in preparation for etching in a 70°C NaOH solution to reveal the grain structure. High undercooling should result in small grains in the final structure [7, 12], since the driving force for solidification is very high at such temperatures and nucleation rates increase with undercooling level [13, 16]. Faceted grains have been observed by various researchers for undercooling levels below 85°C, and as undercooling increases, more dendritic growth is seen [17].

The grain structure of a Si sample coated with 600nm SiN_x that reached only 15°C below T_m before nucleation occurred is shown in Figure 4-18(a). Large, faceted grains can been seen, consistent with findings for low-undercooling silicon in the literature [1, 17]. Samples with this level of undercooling typically took $\sim$ 60 seconds to completely solidify. Kuribayashi et al. have reported that silicon solidifying with undercooling levels of up to 100°C typically solidify with stable {111} interfaces [12].



(a) Coated with 600nm SiN_x, ΔT=15°C



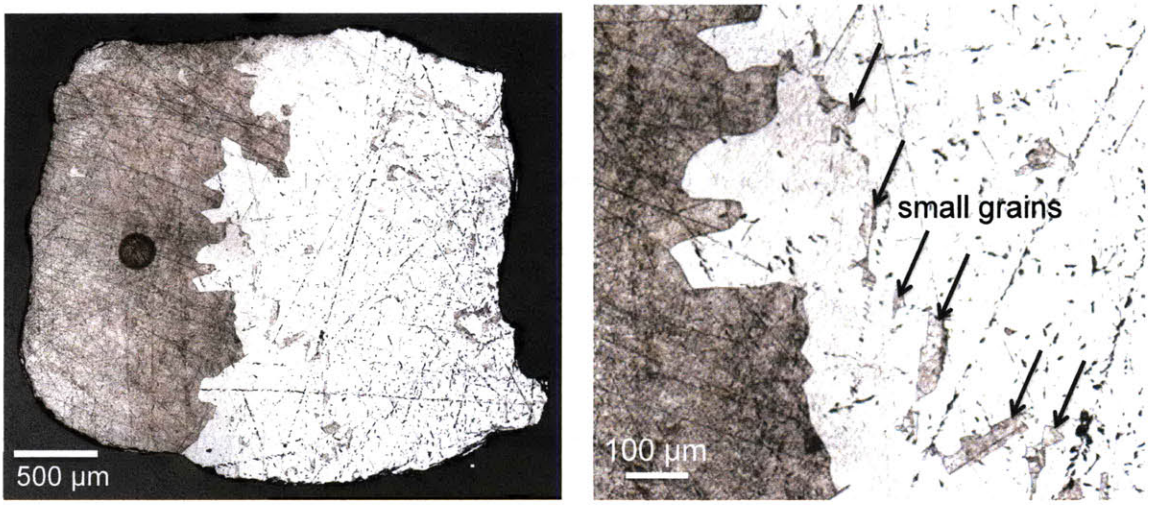
(b) Coated with dry oxide and 40nm SiN_x, ΔT=55°C

Figure 4-18: Grain structure in resolidified Si samples which showed low levels of undercooling.

Similar grain structures were seen for samples coated with a combination of dry oxide and SiN_x, an example of which is shown in Figure 4-18(b). Two or three main grains are seen in this sample, and grain boundaries are slightly less faceted than those with the lowest undercooling. This sample completed solidification in approximately 20 seconds, slightly faster than those with high levels of faceting, but is mostly likely dendrite-free because it is in the undercooling range of ΔT <100°C [15].

The grain structure of a dry oxide-coated Si sample with ~120°C undercooling before solidification is shown in Figure 4-19. In this case, the grains are much less faceted and the grain boundaries are rougher, and these samples typically solidify within 10 seconds. At first glance there appears to be two main grains within the cross-section. However, a closer view of the structure, as seen in Figure 4-19(b), reveals many small, irregular grains scattered throughout the sample. This increase in grain density corresponds with the literature for mid-range levels of undercooling, between ~100°C and 250°C [15]. Nagashio et al. have reported that the dendritic growth of silicon undercooled by more than 100°C typically results in grain refinement,

due to fragmentation of the higher-order arms of the dendrites into small spheres [14]. This fragmentation may occur when the silicon recalesces to the melting temperature after nucleation, at which point the silicon tries to minimize the interfacial area between solid and liquid by breaking off high-order dendrite arms into spheres. Thus the small grains seen along the edge of another elongated grain in Figure 4-19(b) may be the result of this fragmentation and refinement. Silicon undercooled by more than 250°C often undergo fragmentation of even lower-order dendrite arms, resulting in even finer grain structure [14, 15]. This grain refinement behavior is one reason to avoid high undercooling in the silicon melt during the wafer recrystallization process, where large grains are desired and the molten silicon should not actually reach high levels of undercooling as it grows from the already-solid region at the leading edge.



(a) Grain structure of Si DSC sample.

(b) Zoomed in view of fine grain structure.

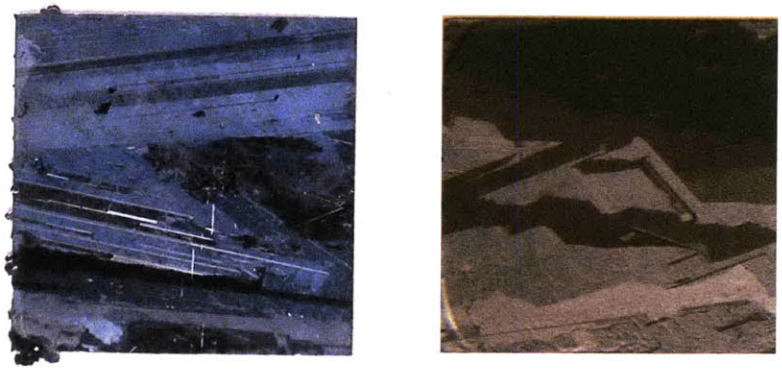
Figure 4-19: Texture etched grain structure of high-undercooling 2-part dry oxide sample, ΔT=120 °C. Black dotted lines are residual scratches from the polishing process.

4.6 Implications for Recrystallization of Wafers

The results of this nucleation study indicate that dry or wet thermal oxide films have the highest potential for being good non-nucleating capsule materials. As long as the silicon has begun to solidify in the part of the wafer which has exited the furnace hot zone first, further nucleation of new grains should not nucleate on the rest of the wafer due to the oxide capsule. In this situation it is reasonable to assume that the molten silicon will not have a chance to subcool far below the melting temperature since the leading edge has already provided a growing solid phase. Thus the SiO_2 capsule should not be a source for new nuclei. However, a capsule of SiN_x would be a more favorable site for nucleation, which should manifest in an increased number of grains in a zone-recrystallized wafer.

To test these findings in an actual zone-melt recrystallization process, silicon wafers (1-inch width, 4-inch length) were prepared with a 160nm SiN_x coating and run through a recrystallization furnace between two supporting SiC backing plates by Christoph Sachs. A 1-inch square piece was cut, polished, and etched in a saturated NaOH solution to reveal the grain structure of the wafer. The resulting grain structure is shown in Figure 4-20(a). Grains are elongated and tend to increase in number towards the trailing edge, which is on the left. This arrangement indicates that new grains are nucleating as the solidification front moves towards the left. Multiple points of the capsule are breached at the left side as silicon bursts through upon final solidification. Grain widths range from $\sim$0.2 – 2.2mm.

For comparison, another sample was recrystallized in the zone-melt furnace under the same conditions, but with a coating of SiO_2 grown in a two-step oxidation and an outer coating of SiN_x. The capsule layers were etched off in a dilute HF solution, and the wafer was subsequently etched in an NaOH solution to reveal the grain structure, which is shown in Figure 4-20(b). In this case, the grains are elongated but much wider due to decreased nucleation at the capsule. Grain widths range from $\sim$1.8mm



(a) SiN_x capsule (b) SiN_x over SiO_2 capsule

Figure 4-20: Grain structure in 1-inch section at trailing edge of Si sample coated with SiN_x or composite capsule, recrystallized in zone-melt furnace. (b) courtesy of Christoph Sachs

– 6.0mm and are generally increasing in width toward the trailing edge at the left side of the image. This clear difference in grain structure shows the manifestation of the different nucleation properties of the two types of capsule. The undercooling data indicates that the molten silicon would have to be undercooled at least 30°C in order for the oxide-nitride composite coating to cause new grain nucleation, and this small shift in nucleation condition was enough to increase the resulting grain size by a factor of ~3. Since the undercooling data indicates that a thinner SiN_x film would increase the required undercooling to cause nucleation, it's probable that using a film of <40 nm would further increase the grain size. However, this effect depends on the level of undercooling reached by the recrystallizing silicon. If it is able to solidify by the growth of existing grains without experiencing any undercooling of more than 30°C, then the 160nm SiN_x outer coating may be sufficiently thin to avoid influencing nucleation of the molten silicon. For best results, the SiN_x outer layer should be reduced below 40nm to reduce inter-layer stresses and nucleation sources.

References

[1] T. Aoyama, Y. Takamura, and K. Kuribayashi. Dendrite growth processes of silicon and germanium from highly undercooled melts. Metallurgical and Materials Transactions A, 30(5):1333–1339, May 1999.

[2] L Cai, A Rohatgi, D Yang, and M.A. ElSayed. Effects of rapid thermal anneal on refractive index and hydrogen content of plasma-enhanced chemical vapor deposited silicon nitride films. Journal of Applied Physics, 80(9):5384–5388, Nov 1 1996.

[3] A. Croll, R. Lantzsch, S. Kitanov, N. Salk, F.R. Szofran, and A Tegetmeier. Melt-crucible wetting behavior in semiconductor melt growth systems. Crystal research and technology, 38(7-8):669–675, 2003.

[4] G. Devaud and D. Turnbull. Undercooling of molten silicon. Applied Physics Letters, 46(9):844–845, 1985.

[5] D. Dutartre. Journal of applied physics; maximum supercooling of silicon encapsulated in sio2. J. Appl. Phys., 59(6):1977–1981, 1986.

[6] A. Esteve, M. Djafari Rouhani, Ph Faurous, and D. Esteve. Modeling of the silicon (100) thermal oxidation: from quantum to macroscopic formulation. Materials Science in Semiconductor Processing, 3(1-2):47 – 57, 2000.

[7] M.C. Flemings and Y Shiohara. Solidification of undercooled melts. Materials science and engineering, 65(1):157–170, 1984.

[8] S. Franssila. Introduction to microfabrication. John Wiley and Sons Ltd, 2004.

[9] K. Fujiwara, Y. Obinata, T. Ujihara, N. Usami, G. Sazaki, and K. Nakajima. Grain growth behaviors of polycrystalline silicon during melt growth processes. Journal of Crystal Growth, 266(4):441–448, Jun 1 2004.

[10] S.C. Hardy. The Surface-Tension of Liquid Silicon. Journal of Crystal Growth, 69(2-3):456–460, 1984.

[11] Damian Harris. Private communication.

[12] K. Kuribayashi, K. Nagashio, and M. Tajima. Spherical crystallization of si during free fall in drop-tubes. Journal of Crystal Growth, 311(3):722 – 726, 2009. The Proceedings of the 4th International Asian Conference on Crystal Growth and Crystal Technology.

[13] R.P. Liu, T. Volkmann, and D.M. Herlach. Undercooling and solidification of si by electromagnetic levitation. Acta Materialia, 49(3):439 – 444, 2001.

[14] K. Nagashio, M. Adachi, K. Higuchi, A. Mizuno, M. Watanabe, K. Kuribayashi, and Y. Katayama. Real-time x-ray observation of solidification from undercooled Si melt. Journal of Applied Physics, 100(3), Aug 1 2006.

[15] K. Nagashio, H. Okamoto, H. Ando, K. Kuribayashi, and I. Jimbo. Spherical silicon crystal formed by semisolid process in drop tube. Japanese Journal of Applied Physics, 45(24-28):L623–L626, Jul 2006.

[16] C. Panofen and D. M. Herlach. Rapid solidification of highly undercooled si and si–co melts. Applied Physics Letters, 88(17):171913, 2006.

[17] C. Panofen, R.P. Liu, D. Holland-Moritz, Volkmann T., and Herlach D.M. Solidification and crystallization, chapter 17. Wiley-VCH, 2004.

[18] D.A. Porter and K.E. Easterling. Phase transformations in metals and alloys. CRC Press, 2nd edition, 1992.

[19] F.L. Riley. Silicon nitride and related materials. Journal of the American Ceramic Society, 83(2):245–265, Feb 2000.

[20] Y. Shao and F. Spaepen. Undercooling of bulk liquid silicon in an oxide flux. Journal of Applied Physics, 79(6):2981–2985, 1996.

[21] E. Takasuka, E. Tokizaki, K. Terashima, and S. Kimura. Emissivity of liquid silicon in visible and infrared regions. Journal of Applied Physics, 81(9):6384–6389, May 1 1997.

[22] T.J. Whalen and A.T. Anderson. Wetting of SiC, Si3N4, and carbon by Si and binary Si alloys. Journal of the American Ceramic Society, 58(9-10):396–399, 1975.

[23] Xiaoge Gregory Zhang. Electrochemistry of silicon and its oxide. Kluwer Academic / Plenum Publishers, 2001.

Chapter 5

Conclusion

5.1 Summary of Work

The development of the new no-sawing silicon wafer manufacturing process has the potential to dramatically decrease the cost of photovoltaics. In this thesis, three main challenges in the development of this approach were addressed.

First, a novel method for measuring the two-dimensional temperature profile of a silicon wafer in a high-temperature environment was designed, proven, and applied to the zone-melt recrystallization furnace used in the no-sawing wafer-making process. This temperature profiling method introduced a low-impact, low-complexity way to measure a silicon wafer's temperature near its melting point, without introducing contaminating metals or altering the structure of the furnace itself. This process exploited the temperature dependence of dopant diffusivity in crystalline silicon and the well-known relationship between dopant concentration and silicon resistivity in order to infer wafer temperature from a measured sheet resistance. Both a donor and an acceptor dopant species were implanted at the wafer surface to utilize their differing magnitudes of diffusivity with temperature and increase the sensitivity of sheet resistance to a change in temperature. These

behaviors were modeled using the TSuprem-4 program to understand and optimize the dopant implantation parameters. Calibration data was successfully related to the predicted relationship between temperature and resistance after 30 minutes in the high-temperature environment, and implanted wafers were used to implement this method to quantify the temperature gradients in our zone furnace. This method has further potential to measure temperature profiles in other thin-geometry high-temperature situations, and the parameters can be easily adapted to measure a particular temperature range other than the one optimized here.

Secondly, a thermal model was developed to determine the shape of the crystal-melt interface in a thin silicon wafer undergoing directional solidification, addressing the inadequacy of traditional directional casting models for this thin geometry. The wafer was first compared to a heat-transfer fin, with the hot end at the freezing temperature of silicon as it exits the furnace hot zone. A threshold wafer travel speed was estimated, above which the temperature gradients through the thickness of the wafer can no longer be neglected. Next, a thermal model was created in COMSOL Multiphysics, in which a curved boundary of prescribed shape represents the crystal-melt interface, and a stationary reference frame is taken within the furnace, at the location of silicon solidification. The heat flux moving away from this curved boundary is matched to the analytical calculation of the quantity of heat flowing into the boundary, plus the latent heat of fusion released by the phase change of silicon occurring at the boundary. This new approach to modeling this irregular interface shape was able to solve for the equilibrium wafer speed that successfully removed the latent heat of fusion for a given interface length. Subsequently, the evolution of the solidification interface shape was determined as wafer speed increased, and the threshold speed above which the interface begins to curve matches well with the fin analysis. These interface shapes provide critical insight into the grain growth direction and subsequent grain boundary formation in the plane of the wafer.

Thirdly, the nucleation behavior of subcooled molten silicon was studied based on the effect of different coating materials in contact with the silicon. The tendency for different coating materials to initiate heterogeneous nucleation was measured using differential scanning calorimetry to measure the level of undercooling below silicon's melting point at which samples solidified. For the first time, the nucleation behavior of silicon on silicon nitride and silicon dioxide was measured. It was found that silicon nitride has the highest tendency to cause nucleation of molten silicon, with the lowest undercooling levels of ΔT <17°C below T_m. Deformations of samples while molten was ruled out as the primary cause for this low undercooling level for this material. Despite its undesirable nucleation properties, silicon nitride has the beneficial quality of easily releasing from SiC substrates after high-temperature processing. In contrast, both wet and dry thermal oxides showed low tendencies to cause nucleation, reaching up to ~130°C of undercooling before nucleation occurred. Sample cleanliness and uniformity of the oxide layer were found to be important factors in improving the consistency of achieving high levels of undercooling. These thermal oxides could be released from SiC crucibles only with prior heavy oxidation of the crucible, so 160nm of silicon nitride was coated over the oxide coating to improve release. However, it was found that this composite coating layer reduced the undercooling levels to ~20°C from that of the solitary oxide layer, due to the thermal stresses and resulting strain between the two layers. This composite coating was still able to improve grain size over the silicon nitride coating. To further reduce grain nucleation in the directional solidification of the wafer, a very thin outer silicon nitride layer is recommended, which allowed the undercooling level to increase to $\Delta T = 56°C$ for a 40nm SiN_x outer layer.

In summary, this work not only furthered the development of the new wafer manufacturing method without sawing, but also increased our basic understanding of interactions between molten silicon and its surroundings, which will impact a

multitude of different silicon manufacturing techniques. Any crystalline silicon growth process involving contact with a wall or substrate can utilize the knowledge gained here to improve the quality of the resulting silicon crystal. A new approach for modeling the crystal-melt interface for a thin-geometry directional solidification process was introduced, when traditional methods used in casting models are inadequate and more complex approaches are unnecessary. In addition, the novel temperature field measurement technique is a new, non-disruptive, low-complexity method which can be applied to a variety of non-traditional silicon manufacturing scenarios, including wafer recrystallization and silicon thin film crystallization.

5.2 Future Work

Further extension of the work described in Chapters 2 and 3 would aim to improve the no-sawing wafer recrystallization process. In particular, the effect of changing the temperature gradients in both the travel direction and the direction perpendicular to the wafer plane would be interesting to study. Gradients parallel to the travel direction could be changed by altering the setpoints of the heater elements to create a more gradual decrease in temperature that would minimize the formation of dislocations in the cooling wafer, and the temperature profiling method developed here could facilitate the diagnosis of different gradients. Furthermore, this method would be a convenient way to measure the consistency of the temperature profile in the furnace after making design changes or replacing heater elements or contacts.

In terms of temperature gradients perpendicular to the wafer plane, through the thickness of the wafer, the thermal model described in Chapter 3 could be applied to the case of an asymmetric heat transfer condition. This asymmetry could be achieved by setting the top and bottom heater elements at different temperatures to cause heat to be lost more quickly from one side of the wafer sandwich upon exiting

the hot zone. This change would affect the radiation boundary conditions used in the model. Asymmetry could also be imposed by using different backing plates on the top and bottom of the wafer. Backing plate properties could be changed by using different plate thicknesses, altering plate emissivities with coatings, or using different backing plate materials. In some cases, it would be necessary to add the backing plate into the COMSOL model in order to include its effect and temperature gradients within the plate in the model.

Further development of the nucleation behavior study could expand to other materials of interest in the silicon processing realm. For example, it would be interesting to characterize silicon carbide in terms of silicon nucleation properties, since silicon grown in contact with graphite often includes the formation or precipitation of silicon carbide, which can cause the formation of smaller grains. It would also be useful to investigate the properties of different types of silicon oxide, such as an oxide layer deposited by PECVD using tetraethyl orthosilicate (TEOS) or by application of spin-on glass. The effects of using a doped oxide layer would also be of interest to measure, as well as the level of impurities in silicon at which nucleation behavior is affected. Such extensions of the current work would increase our understanding and ability to improve crystalline silicon growth processes.