

MIT Open Access Articles

Guest Editorial for Special Issue on High-Performance Multichip Interconnections

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

Citation: Stojanovic, V. M., C.-K. K. Yang, and R. Ho. "Guest Editorial for Special Issue on High-Performance Multichip Interconnections." *Circuits and Systems II: Express Briefs, IEEE Transactions on* 57.5 (2010): 317-318. © Copyright 2010 IEEE

As Published: <http://dx.doi.org/10.1109/tcsii.2010.2048057>

Publisher: Institute of Electrical and Electronics Engineers

Persistent URL: <http://hdl.handle.net/1721.1/62014>

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

Terms of Use: Article is made available in accordance with the publisher's policy and may be subject to US copyright law. Please refer to the publisher's site for terms of use.



Guest Editorial for Special Issue on High-Performance Multichip Interconnections

THIS special issue on high-performance multichip interconnections illustrates a broad spectrum of challenges facing designers of high-speed communication circuits. Seeking to improve both the energy efficiency and throughput density of high-performance interconnects, designers have turned to the optimization of microcommunication systems across multiple design layers. The papers here represent this cross-layer approach and span novel transmitter and receiver equalization and data-recovery architectures, channel architecture organizations, comparisons with optical transmission techniques, advanced signal processing and coding concepts, and network optimization.

Kao and Liu present a 20-Gb/s adaptive transmitter pre-emphasis filter adjusted by detecting the propagation time through the channel, a technique that helps decouple the adaptation from transmitter/receiver collaboration on smooth channels with relatively high loss and low reflections. An adaptive receiver equalizer by Cheng *et al.* operates at 5 Gb/s and uses low-voltage zero generators to achieve high-frequency gain boosting without inductors, leveraging a spectrum-balancing technique and current-steering power detector circuits to adjust the equalization settings.

Amortizing the overhead of clock and data recovery in multiple parallel links, Nassar *et al.* introduce a new methodology for multichannel clock and data recovery, showing that the architecture can be reduced to an ensemble of weakly interacting delay-locked loops, asymptotically eliminating the jitter-peaking problem and allowing control of voltage-controlled oscillator jitter transfer to the recovered clock without affecting the data jitter transfer.

In order to improve overall link performance, channel redesign, where possible, also represents a powerful design knob. The papers by Lee *et al.* and Aryanfar and Amirkhany present advances in channel engineering for memory interfaces. The paper by Lee *et al.* optimizes reflection coefficients at branch junctions in a multislot memory system for post-DDR3 applications, creating an improved channel transfer function similar to that for point-to-point connections at rates up to 3.2 Gb/s. Ayanfar and Amirkhany introduce low-cost passive resonance mitigation techniques for multidrop memory channels, coupling transmission lines to prevent destructive signal resonance caused by reflections from capacitive loads and channel mismatches at rates up to 4 Gb/s.

Analyzing an alternative signaling medium, Palaniappan and Palermo compare various optical interconnect architec-

tures for chip-to-chip applications. The brief considers the power efficiency of near-term vertical-cavity surface-emitting laser drivers and discrete photodetectors, as well as longer term single-mode integrated photonic solutions, promising to achieve data rates past 30 Gb/s/wavelength at energy efficiencies of 500 fJ/b in the 45-nm node. Han *et al.* present a 20-Gb/s transformer-based current-mode optical receiver with a common-gate transimpedance amplifier and a six-stage postamplifier. Employing source degeneration and interleaving active feedback techniques, they achieve 12.6-GHz bandwidth and flat-frequency response with a cumulative gain of 60 dB Ω .

In addition to these circuit- and channel-level design techniques, more advanced signal processing and coding methodologies can also help in eliminating channel artifacts and relaxing power/noise specifications for analog links. Namgoong presents receiver techniques that reconstruct the signal from a bank of low-frequency analog-to-digital converters operating on a frequency-channelized input signal. Using single-carrier cyclic-prefixed communication reduces the computational complexity in channels with moderate to large intersymbol interference. Narasimha and Shanbhag explore the utility of forward error correction (FEC) in shifting the power allocation from analog link blocks to a more scalable digital back end, trading off transmit swing, jitter, and receiver sensitivity for coding gain. The paper presents these tradeoffs using a scalable custom BCH decoder architecture, showing that FECs are on the brink of providing a net positive gain in high-speed link applications.

At the system level, the paper by Seiculescu *et al.* presents a comparative analysis of networks on chip (NOCs) for 2-D and 3-D integration, with multiple voltage and frequency islands. These emerging design techniques can provide relatively large energy-efficiency improvements but require careful design-space exploration at the NOC level.

VLADIMIR M. STOJANOVIC
Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139-4307 USA

CHIH-KONG KEN YANG
Department of Electrical Engineering
University of California—Los Angeles
Los Angeles, CA 90095 USA

RON HO
VLSI Research Group, Oracle
Menlo Park, CA 94025 USA

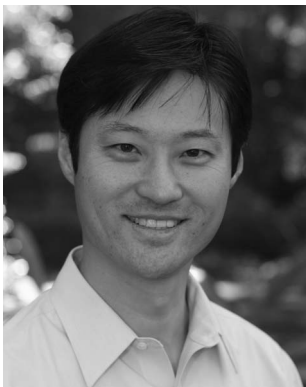
REFERENCES

- [1] S.-Y. Kao and S.-I. Liu, *A 20 Gbps Transmitter With Adaptive Pre-Emphasis in 65 nm CMOS Technology*.
- [2] K.-H. Cheng, Y.-C. Tsai, Y.-H. Wu, and Y.-F. Lin, *A 5 Gb/s Inductorless CMOS Adaptive Equalizer for PCI Express Generation II Applications*.
- [3] A. Nassar, A. Emira, A. N. Mohieldin, and A. Hussien, "Multichannel clock and data recovery: A synchronous approach," Ph.D. dissertation, Cairo Univ., Giza, Egypt, 2006–2009.
- [4] J. Lee, S. Lee, and S. Nam, *Multi-Slot Main Memory System for Post DDR3*.
- [5] F. Aryanfar and A. Amirkhany, *A Low Cost Resonance Mitigation Technique for Multi-Drop Memory Interfaces*.
- [6] A. Palaniappan and S. Palermo, *Power Efficiency Comparisons of Inter-Chip Optical Interconnect Architectures*.
- [7] U. Han, B. Choi, M. Seo, J. Yun, D. Lee, T. Kim, Y. Eo, and S. Min Park, *A 20-Gb/s Transformer-Based Current-Mode Optical Receiver in 0.13- μm CMOS*.
- [8] W. Namgoong, *Digital Processing of Cyclic Prefixed Frequency Channelized Receiver for Serial Links*.
- [9] R. Narasimha and N. Shanbhag, *Design of Energy-Efficient High-Speed Links via Forward Error-Correction (FEC)*.
- [10] C. Seiculescu, S. Murali, L. Benini, and G. De Micheli, *Comparative Analysis of NoCs for 2D vs 3D SoCs Supporting Multiple Voltage and Frequency Islands*.



Vladimir M. Stojanovic (S'96–M'05) received the Dipl.Ing. degree from the University of Belgrade, Belgrade, Serbia, in 1998, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2000 and 2005, respectively.

He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge. His current research interests include the design, modeling, and optimization of integrated systems from standard mixed-signal and VLSI blocks to CMOS-based electrical and optical interfaces and networks.



Chih-Kong Ken Yang (S'94–M'98–SM'07) was born in Taipei, Taiwan. He received the B.S. and M.S. degrees in 1992, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1998.

He joined University of California, Los Angeles, as an Assistant Professor in 1999, where he has been a Professor with the Department of Electrical Engineering since 2009. His current research area is high-performance mixed-mode circuit design for VLSI systems such as clock generation, high-performance signaling, low-power digital functional blocks, and analog-to-digital conversion.



Ron Ho received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA.

He is currently a Consulting Hardware Engineer with the VLSI Research Group, Oracle, Menlo Park, CA. He was with the Intel Corporation, working on processor projects ranging from the 486 to the Itanium generations. In 2003, he joined Sun Labs, which is now part of Oracle, where he has been working on chip-to-chip and on-chip communication technologies. He has more than 45 publications at peer-reviewed conference proceedings and journals. He is the holder of 25 patents.

Dr. Ho received the Chairman's Award for Innovation from Sun Labs in 2004 for his work on proximity communication. He has been on the technical program committees for the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE Asian Solid-State Circuits Conference (A-SSCC), the IEEE Hot Interconnects Symposium, the IEEE International Symposium on Asynchronous Circuits and Systems, and the International Symposium on VLSI

Design, Automation and Test (VLSI-DAT). He has served as Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE JOURNAL OF QUANTUM ELECTRONICS.