High Fidelity Pattern Transfer in InP Photonic Device Fabrication

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Evelyn Wallis Kapusta
Bachelor of Arts in Physics, Mount Holyoke College (2005)

Submitted to the

Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Degree of Master of Science in Electrical Engineering and Computer Science

At the

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Abstract

The photonic industry is driven by the information ages demand for higher bandwidth. To meet the future demands of 10 Tbit networks, photonic integrated circuits (PIC) are required. Device performance is affected by everything from component coupling to electrical connectivity of the active components. However the most fundamental and often challenging aspect of photonic device fabrication is dimensional control. At 1550 nm, line width tolerance range between 1 μm to 0.05 μm.[**1**] Although these tolerances are easily achieved using lithography technology such as electron beam lithography (EBL) or 193 nm projection, neither are viable optical options for InP production.[**2**] The purpose of this thesis is to develop a fabrication process for InP faraday rotators using standard, high throughput lithographic and etching techniques. The Faraday rotator is a 1.4 μm InP-InGaAsP-InP waveguide with a line width tolerance of ± 0.07 μm.

Thesis Supervisor: Rajeev J. Ram
Title: Professor

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I came to graduate school to learn how to think, and that is exactly what I got. It has been an ugly process but one the most worthwhile thing I have ever done. To my mentors, colleagues, friends, and family – I wish to thank you for your continued belief in me throughout every stage of this adventure.

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1 Background

From 2000 to 2009, the United States saw the average per capita bandwidth grow from 28 kbit/sec to 3.8Mbit/sec according to the Akamai quarterly state of internet report. [**3**] This unprecedented growth in communication requirements has pushed the telecom industry from electrons to photons. By switching to optical networks Verzion was able to increase its maximum residential bandwidth from 7.1 Mbit/sec to 250 Mbit/sec.[**4**] Photonic integration has grown to provide a cost-competitive infrastructure for optical communications.

Infinera and the University of California in Santa Barbara (UCSB) have produced photonic integrated circuits (PICs) supporting 40Gbit per channel data rates.[**5**][**6**] In 2004 Infinera successfully deployed monolithic dense wavelength division multiplexed (DWDM) transmit and receive PICs in optical networks across the northern hemisphere. The initial transmit device consisted of a 10 channel array each operating at 10 Gbit/sec. Each channel consists of a distributed feedback (DFB) laser, high-speed electroabsorption modulator (EAM) and variable optical attenuator (VOA). The 10 channels were then combined with an array waveguide grating (AWG) to generate a single DWDM output. [**7**] Further scaling has supported photonic integrated circuits with 40 channels each channel to 40 Gbit/sec. [**5**] In parallel UCSB was generating an 8 channel monolithic tunable optical router operating at 40 Gbit/sec/channel. The USCB optical router utilizes a tunable DFB to generate the wavelength conversion within the device. A combination of semiconductor optical amplifiers (SOAs), Mach-Zehnder interferometers (MZI), variable optical attenuators (VOAs), and multimode interferometers (MMI) are used to manipulate the phase of each channel before being redistributed by a 8x8 AWG.[**6**]

Each of the chips described above are comprised of photonic elements utilizing a variety of physical principals to achieve optimal device performance chief among them is the principle of wave interference. AWG multiplexer operation is based on the devices ability to couple light from a series of input waveguides to the proper output waveguides according to the wavelength of the input light, and the dimensions and effective indices of the waveguides. Mach-Zehnder interferometers within optical modulators split optical signals among two arms and constructively or destructively combine them at the output depending on the optical path length and effective index of each MZI arm. MMI power splitters also utilize the signal interference in a multi-mode waveguide to generate uneven splitting at the output of the device. The amount of light coupled into the output waveguides of a MMI is controlled by the multimode cavity dimensions. By adjusting the length and width of the AWG waveguides, MZI arms, and MMI cavity, one adjusts the optical path length, phase, and effective index

of refraction of each of the devices.[**8**] Thus it is the device dimensions that defined the critical performance parameters for the elements within integrated photonic circuits.

In Section 1.1 we will explore the relationship of photonic device performance to physical parameters. Starting with optical waveguides we will derive the relationship of propagation constant to the waveguide dimensions. We will extend our understanding to MZI, MMI, and Faraday rotators to define dimensional tolerances for a variety of common photonic devices. Once a dimensional baseline has been established we will explore the fabrication of photonic devices and its ability to meet the requirements established in Section 1.1. This is followed by an overview of the fabrication process for InP Faraday rotators developed by Guo from the Physical Optics and Electronics group at MIT in 2006. The chapter concluded with an introduction to the fabrication process developed in this thesis for InP Faraday rotators which utilizes contact optical lithography and inductively coupled reactive ion etching to achieve high throughput, high fidelity pattern transfer.

1.1 Dimensional Tolerances of Interference Dependent Photonic Devices

Photonic integrated circuits are comprised of a multitude of components ranging from waveguides to active modulators. In this work we will focus on passive components whose performance relies on interference effects. By examining how five common photonic devices operate we can examine how changes in physical dimensions effect their performance. Our discussion begins with the optical waveguides, whose mode is dependent on the core width. Next is a review of signal splitting in MZI and MMI through the utilization of different optical path lengths and multimode interference. Microring resonators act as add/drop filters by destructively interfering light within the ring and the bus waveguide. Finally polarization rotation, viewed as interference between the TE and TM branches of the input light, is considered.

Optical waveguides provide the backbone of all photonic integrated circuits, moving signals from one region of the chip to another. They are built of a high index core surrounded by low index material that is used to trap the input light within the core by total internal reflection as shown in Figure 1-1.

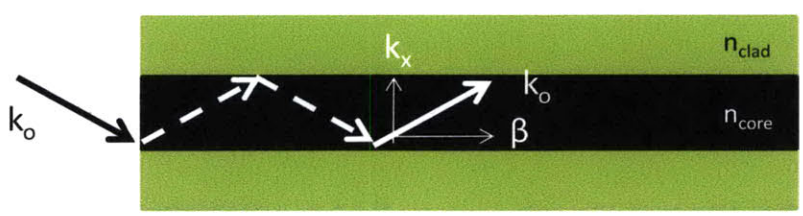


Figure 1-1: Waveguide

The uniform phase front generated by the interference of the wave vector within the core is described by the propagation vector (β). This parameter is defined mathematically in terms of the input wave vector, k_o, the effective index of the waveguide, and the wave vector in the x direction.

$$\beta = k_o n_{eff} = \sqrt{(k_o n_{core})^2 - k_x^2} \quad 1.1$$

The effective index of a device is determined by the mode overlap with the surrounding material. Consider a III-V waveguide with an InGaAsP (n_{core} = 3.22) core of width, d, surrounded by InP (n_{clad} = 3.14). By increasing the width of the waveguide, the effective index will increase approaching the index of the core. A graph of waveguide width vs effective index (n_{eff}) is shown in Figure 1-2. The derivation of this figure is based on the normalized waveguide function described in Appendix A.

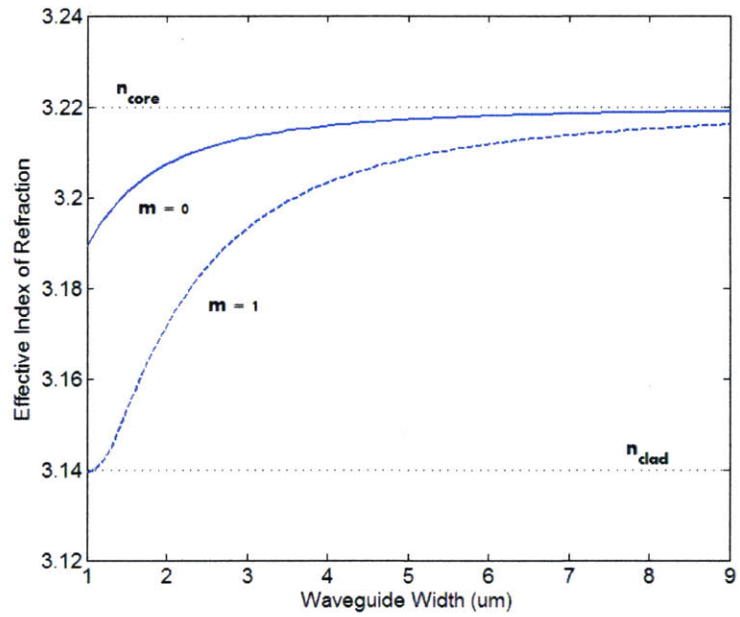


Figure 1-2: Waveguide Width vs Effective Index. m is the mode of the waveguide

Variations in the effective index affect the EM field within the waveguide as the phase term in equation 1.2,

$$E(z) = E_o e^{-j\beta z} = E_o e^{-j(k_o n_{eff})z} \quad 1.2$$

The dependence of the effective index and phase on the device dimension will continue to be an important consideration as photonic devices become more complicated.

Mach-Zehnder interferometers are comprised of two waveguides (or arms) combined by power splitters at either end as shown in Figure 1-3.

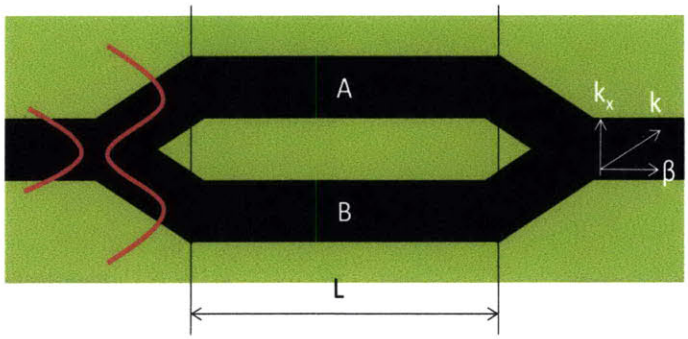


Figure 1-3: Mach-Zehnder Interferometer

As the light passes through the Mach-Zehnder each arm generates a slightly different phase shift depending length (L) and width of the waveguide arms (effecting n_{eff} and the material index of refraction), according to equation 1.2. The resulting output, I_{out}, is due to the constructive or destructive interference of the electric field in each arm of the MZI,

$$I_{out} \sim (E_A + E_B)(E_A^* + E_B^*) \qquad 1.3$$

where E_A and E_B are the electric field in MZI arm A and B respectively. The importance of the phase term (and in turn the dimension control) on the output intensity is investigated by varying the length and width of arm B. MZI output intensity verses change in length and width is shown in Figure 1-4 and Figure 1-5 .[**9**]

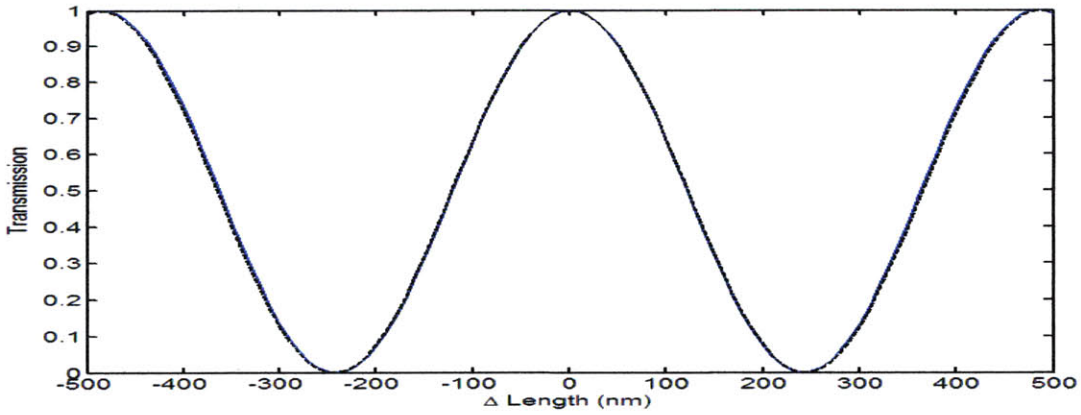


Figure 1-4: Mach-Zehnder: ΔLength vs Transmission

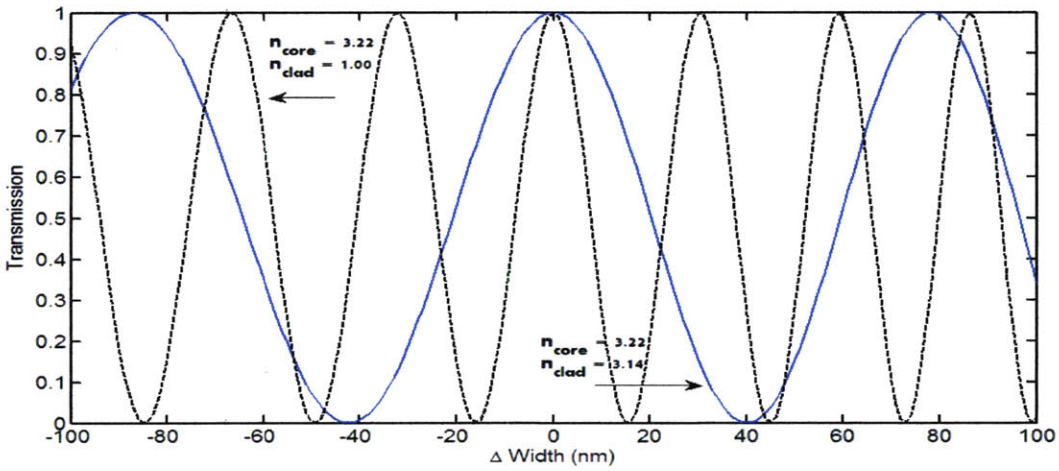


Figure 1-5: Mach-Zehnder: ΔWidth vs Transmission

From Figure 1-4 we find that a 71 nm difference in MZI arm length generates a 1 dB drop in output intensity. While only a 12.6 nm error in waveguide width will generate the same 1dB drop in intensity. The MZI reliance on phase makes is susceptible to small errors in device dimensions.

Another phase dependent device is the multimode interferometer power splitter. A MMI utilizes interference of the modes to manipulate the location of the peak intensity within the waveguide. Figure 1-6 shows a 2x2 MMI power splitter. Light input enters the MMI through a single mode waveguide at port 1 exciting multiple modes within the cavity.

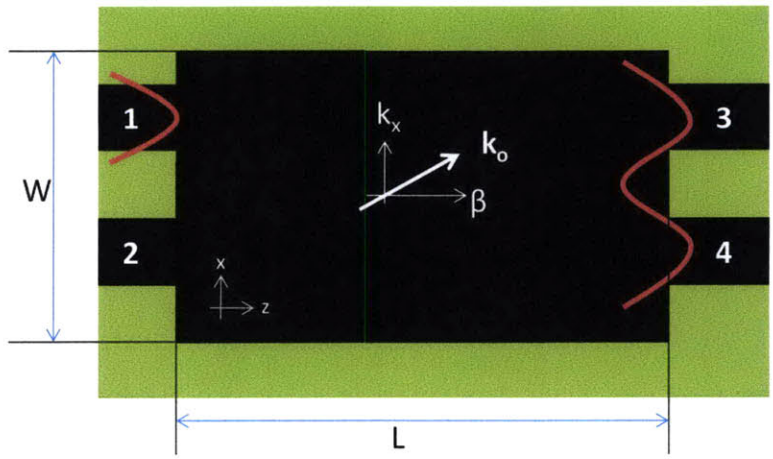


Figure 1-6: 2x2 Multimode Interferometer

As the electric field propagates within the cavity, the peak intensity will appear to oscillate back and forth within the chamber due to the interference of the multiple modes as shown in Figure 1-7. The movement of the intensity peak can be described as a phase shift in the intensity according to

$$E_1 = A_0 \cos\left(k_{y0} y\right) e^{-i\beta_o z} \tag{1.4}$$

$$E_2 = A_1 \cos\left(k_{y1} y\right) e^{-i\beta_1 z} \tag{1.5}$$

$$\cdots$$

where E_1 is the electric field of the first order mode, and E_2 is the second order mode.

$$I \sim (E_1 + E_2)(E_1^* + E_2^*) \tag{1.6}$$

The side to side oscillations of the peak intensity are used to steer and redistribute the power. By varying the length and width of the MMI one can control where the peaks are located at a particular length z. Consider Figure 1-7 assuming a MMI with a constant cavity width with single mode outputs. At point B, the MMI acts as a switch moving the power from port 1 to port 4 in Figure 1-6, while output waveguides placed at location A or C makes the MMI a 50/50 splitter.

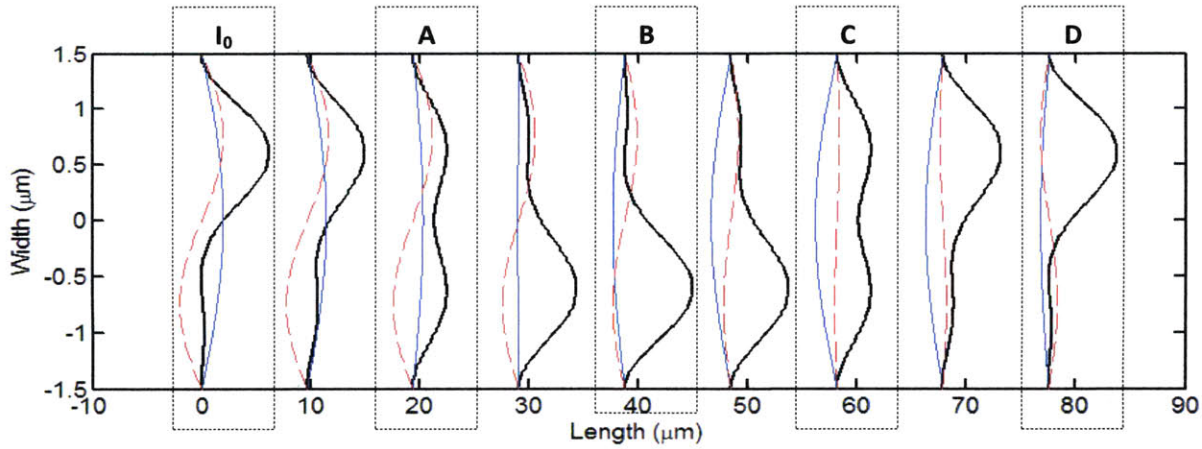


Figure 1-7: Electric Field Intensity within an MMI. This figure shows the variations in peak intensity due to changes in the length with a constant device width of 3μm. The heavy line is the field intensity. The thin solid is the 0th order mode of the electric. The dash thin line is the 1 order mode of the electric field.

The distance required to produce a π phase shift in the intensity is referred to as the beat length of the device and is defined by the difference of the propagation constants for the first and second order modes.

$$L_\pi = \frac{\pi}{\beta_{00} - \beta_{01}} \qquad 1.7$$

Difference in β_{00} and β_{01} are due to the difference in the effective index according to Figure 1-2 and our discussion of optical waveguide. An InP-InGaAsP MMI with a cavity width of 3μm, would have beat length of 38.8 μm. Splitting of the electric field power can also be achieved by adjusting the width of the device and keeping the length constant as shown depicted in Figure 1-8A.

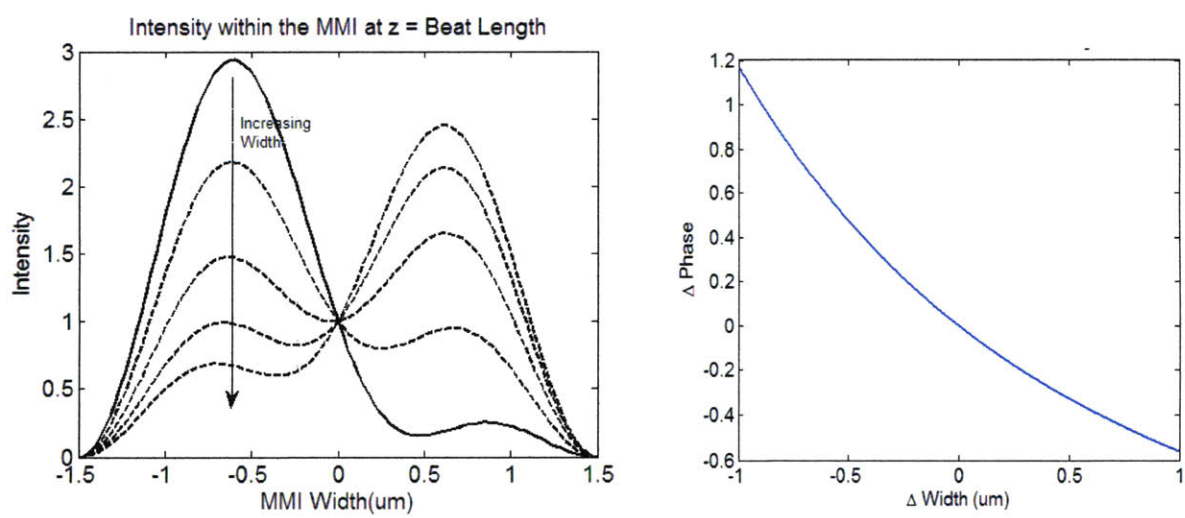


Figure 1-8: MMI: Phase vs Width

Our discussions of MMI waveguides have shown that variations in the length and width generate changes in the effective mode index and ultimately the phase. An error of 9.8 μm in the MMI cavity

length and 0.5 μm in cavity width results in a π/4 phase shift of the intensity profile. By fabricating the proper width and length of the multimode cavity, a MMI can be used to achieve a variety of different splitting situations. [**9**]

Optical filters in photonics integrated circuits utilize interference within ring structures to isolate specific frequencies. Consider the microring resonators shown in Figure 1-9. Light traveling along the bus waveguide corresponding to the ring's resonant frequency will be coupled into the ring, be amplified by constructive interference, and eventually couple into the drop port along the bottom of the device. All other frequencies will pass the ring and exit the resonator at the through port.

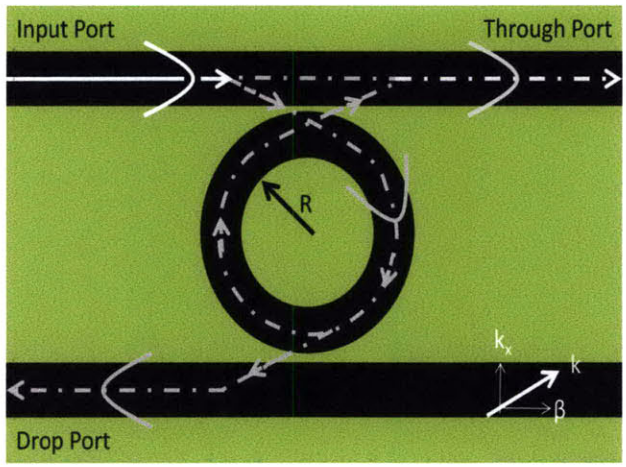


Figure 1-9: Microring Resonator

The resonant frequency of a microring resonator is defined by the radius and effective index of the ring according to

$$f_{resonant} = \frac{m\,c}{2\pi R * n_{eff}} \qquad 1.8$$

where m is the number trips around the ring and c is the speed of light in a vacuum. Filter tuning is achieved by manipulating the optical path length and effective index. This can be done during fabrication by adjusting the width and radius of the waveguides. The effect of varying the ring radius and waveguide width while at the resonant frequency is shown in Figure 1-10 and Figure 1-11 respectively.

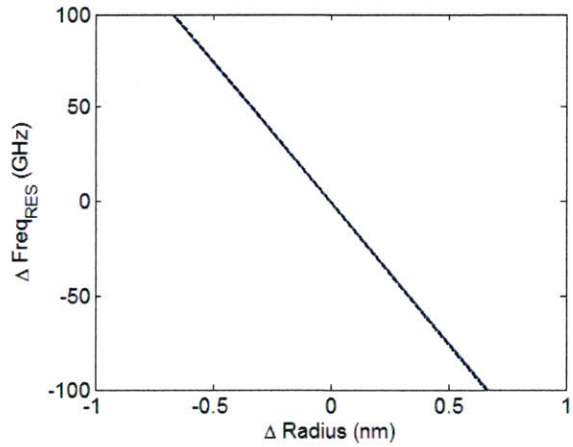


Figure 1-10: Microring Resonator: Radius vs Resonant Frequency

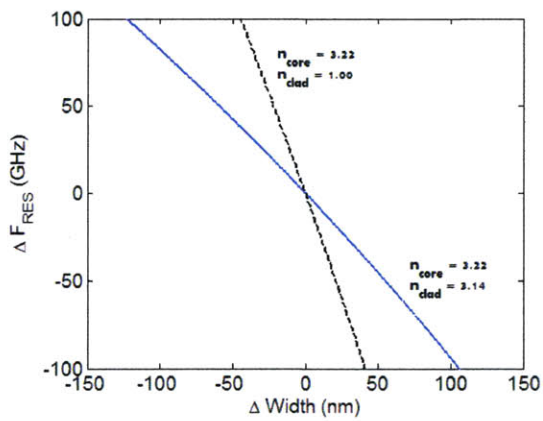


Figure 1-11: Microring Resonator: Waveguide Width vs Resonant Frequency

A PIC being used for WDM has a typical channel spacing of 100 Ghz. Thus a microring resonators being used to pull the proper frequency for each channel of the AWG has a maximum error of ±50 Ghz. This corresponds to a fabrication error of 1.2 nm in the radius width and 101 nm in the waveguide width, assuming an ideal InP-InGaAsP microring resonator with a width of 1.4µm and ring radius of 3µm.[**10**]

The last interference dependent photonic device we will examine is the Faraday rotator. A Faraday rotator is an optical waveguide with a unique material property that generates non reciprocal polarization rotation when exposed to a magnetic field. Electric field polarization is determined by the amount of light in the TE and TM electromagnetic modes, described by

$$\theta = tan^{-1}\left(\frac{E_{TE}}{E_{TM}}\right) \qquad 1.9$$

As light propagates within the Faraday rotator it couples from TE to TM mode producing polarization rotation. The amount coupling between the modes is defined by the Verdet coefficient which describes the strength of Faraday effect within the material. The electric fields at a point along the length of the device can be found by solving the coupled mode equations for Faraday rotators [**11**]:

$$\frac{dA_{TE}}{dz} = -j\beta_{TE}A_{TE} + VA_{TM}$$
$$\frac{dA_{TM}}{dz} = -j\beta_{TM}A_{TM} - VA_{TE} \qquad 1.10$$

where A_X is the amplitude of the electric field for that mode and V is the Verdet coefficient. By solving the differential equations we find the eigenfunction and eignevalues which describe the TE and TM electric fields.[**11**]

Maximum polarization rotation occurs when the electric fields propagate within the Faraday rotator at the same speeds. If the two modes travel at different rate the light will be unable to perfectly couple from one to the other. Differences in propagation constants (Δβ) are due to difference in the indices of refraction defined as birefringence:

$$\Delta n = n_{TE} - n_{TM} \qquad 1.11$$

There are two major types of birefringence, intrinsic and geometrical. Intrinsic birefringence is defined by the lattice structure of the material. Geometrical birefringence describes the difference in effective indices of refraction generated by the device's physical dimensions and material composition. Using a eigenmode solver the effective indices for each mode (n_{TE} and n_{TM}) in a InP-InGaAsP-InP waveguide can be calculated from coupled mode theory. The theoretical InP-InGaAsP-InP waveguide in Figure 1-12A, has a geometrical birefringence corresponding to Figure 1-12B at an operating wavelength of 1550nm. The zero birefringence for this device is 1.39μm.

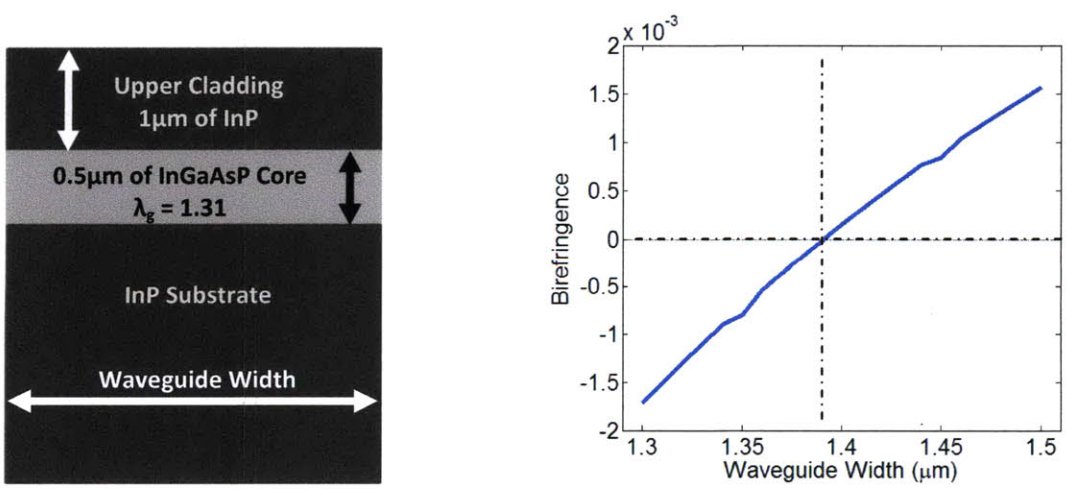


Figure 1-12: Faraday Rotator : Birefringence vs Waveguide Width

The effect of geometrical birefringence on Faraday rotator performance is apparent when solving for the ratio of electric fields, $R_{TE/TM}$ [**12**]:

$$R_{TE/TM} = \frac{(VB)^2}{\left(\frac{\Delta\beta}{2}\right)^2 + (VB)^2} sin^2\left(L\sqrt{\left(\frac{\Delta\beta}{2}\right)^2 + (VB)^2}\right) \quad 1.12$$

where $\Delta\beta = k_o * \Delta n$. With zero birefringence the coupling equation collapses to $\sin^2(LVB)$, producing a 100% coupling ratio between the TE and TM modes for the proper choice of LVB. Plugging the range of birefringences shown in Figure 1-12 into Equation 1.12, we can generate a relationship between polarization rotation and waveguide width. All figures are based on a nominal 1.39µm waveguide with a Verdet coefficient of 100 deg/cm/T in a 0.2T magnetic field.

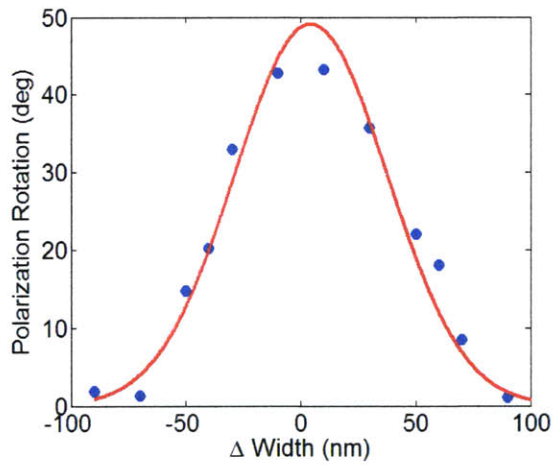


Figure 1-13: Faraday Rotator : Polarization Rotation vs Waveguide Width (L = 50mm)

The significant drop off in polarization rotation beyond the zero birefringence width mandates Faraday rotator operation at the zero birefringence wavelength for optimal performance. Thus the dimensional tolerances of a Faraday rotator are defined by the testing equipments ability to operate at the zero birefringence wavelength. Plotting the zero birefringence point verses waveguide width enables us to define the acceptable range of device widths.

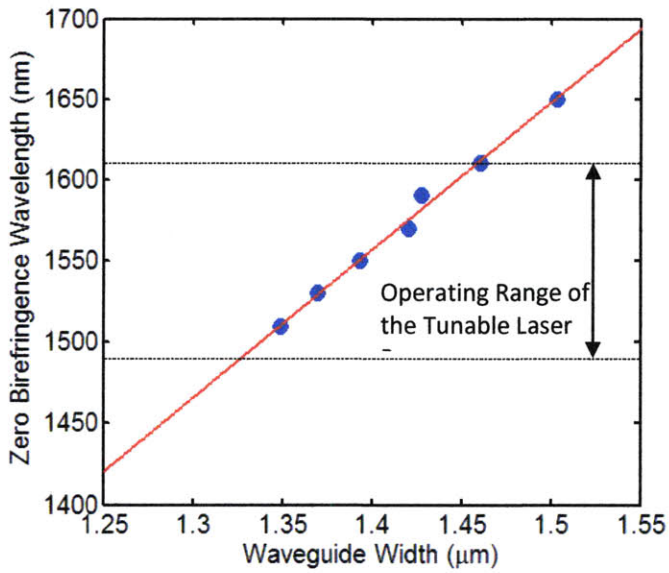


Figure 1-14: Zero Birefringence Point for a Theoretical Waveguide

In our case the operating range of the Agilent 81640A tunable is 1490nm – 1610nm, which sets the dimensional tolerances to ±65nm.

We have shown a clear dependence of device performance on critical dimension for a variety of passive photonic devices ranging from waveguides to filters and polarization rotators. Table 1-1 summarizes maximum dimensional error for each of the devices discussed above.

Table 1-1: Critical Dimension Error of Various Photonic Devices

	Performance Limit	Dimensional Tolerance				
Mach-Zehnder Interferometer	1 dB drop in Intensity	ΔWidth	=	±	12.6	nm
		ΔLength	=	±	71	nm
Multimode Interferometer	π/4 Phase shift in Intensity	ΔWidth	=	±	250	nm
		ΔLength	=	±	4900	nm
Microring Resonator	±50 GHz Resonant Frequency	ΔWidth	=	±	50	nm
		ΔRadius	=	±	0.3	nm
Faraday Rotator	Zero Birefringence at 1550 nm	ΔWidth	=	±	65	nm

The tight requirements on waveguide width prompts the question, are these achievable tolerances in device fabrication? In Section 1.2, we will explore this question starting with an overview of photonic device fabrication. After that we will examine the linewidth error generated at each step of the fabrication process as well as what can be done to control it. Finally we will match fabrication techniques to the device requirements in Table 1-1 .

1.2 Fabrication Tolerances

As we showed in Section 1.1, small variations in critical dimensions can generate drastic changes in device performance. However control of critical dimensions down to 50 nm requires fabrication technology that can meet these demands.

The success of microchip fabrication is determined by a process' ability to transfer the desired pattern to a specific location on the substrate. The process involves transferring a pattern into an energy sensitive material called resist and then etching it into the substrate. The pattern can be transferred into the resist by photon exposure, electron beam exposure, or physical pressure. Once the temporary pattern is established deposition and etching can used to transfer the pattern into the wafer. Consider the fabrication of a simple structure shown in Figure 0-15, the process begins by spinning on a uniform layer of resist over the surface of the substrate (Figure 1-16A). For this example we will assume the pattern is transferred using contact photolithography, in which a shadow mask containing the pattern is pressed against the resist (Figure 1-16B). The resist is exposed with UV light from above the sample causing the resist to breakdown or become crosslinked depending on whether it is positive or negative resist. When rinsed in a developer solution regions of the exposed resist will be removed, successfully transferring the pattern from the mask into the resist as shown in Figure 1-16C.

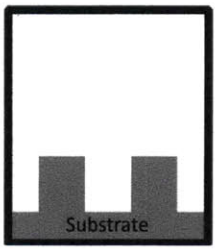


Figure 1-15:

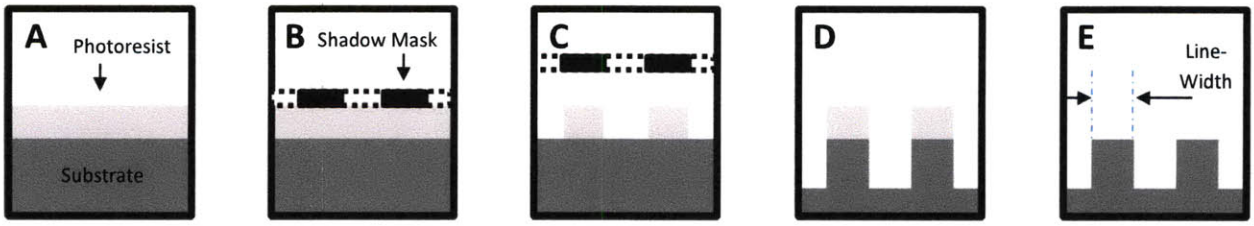


Figure 1-16: Basic Fabrication

The exposed regions of the substrate can be removed through etching. A wet etchant will evenly etch the exposed substrate in the horizontal and lateral direction. Anisotropic profiles are achieved by dry etching producing a device like the one shown in Figure 1-16D.

If the resist is not strong enough to withstand the etching process additional steps may be added to create a hard mask to replace the soft resist mask. The mask material can be deposited before photolithography and then etched in a separate process before etching the substrate as shown the process flow in Figure 1-17. The hard mask material can also be deposited after the photolithography. This will deposit material directly on the substrate and on top of the resist. By removing the resist, we effectively lift off the additional hard mask transferring the inverse pattern onto the substrate. This process flow referred to as lift-off is shown in Figure 1-18.

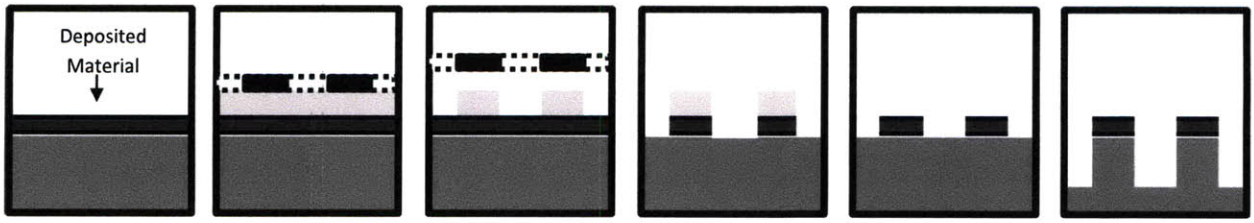


Figure 1-17: Process Alternative 1: Hard Mask

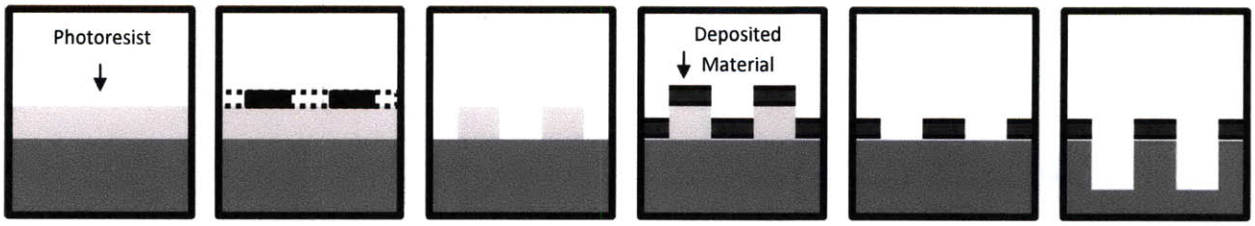


Figure 1-18: Process Alternative 2: Lift-off

After removing the photoresist or hard mask the fabrication of the waveguides shown above are complete. Through the combination of different types of resist, etching, and deposition techniques any number of devices can be created. The linewidth of the final device (Figure 1-16E) is due to the fidelity of pattern transfer from one step to another. With a basic understanding of the microchip process flow, we can explore each step of the fabrication process and its ability to meet the critical dimensions limits established in Section 1.1.

1.2.1 Lithography

Lithography is the cornerstone of dimensional control in fabrication, since errors generated in this step are propagated later in the process. Lithography techniques available allow for features down to 7 nm with dimensional errors as low as 1 nm, however this level of precision comes at a cost. In this section we will examine the pros and cons of various lithography techniques including optical, electron beam, and imprint.

1.2.1.1 Optical Lithography

Optical lithography utilizes light propagating through a shadow mask to excite one of two photo-sensitive resists, positive or negative. Positive photoresist reacts to exposure by breaking the bonds within the polymer allowing the exposed material to easily be removed during development (Figure 1-19A). Polymers chains within negative photoresist become crosslinked during an exposure and bake cycle. After the exposing the entire sample for a second time, the regions of the resist that were crosslinked in the first step will remain in place during development as is shown in Figure 1-19B.

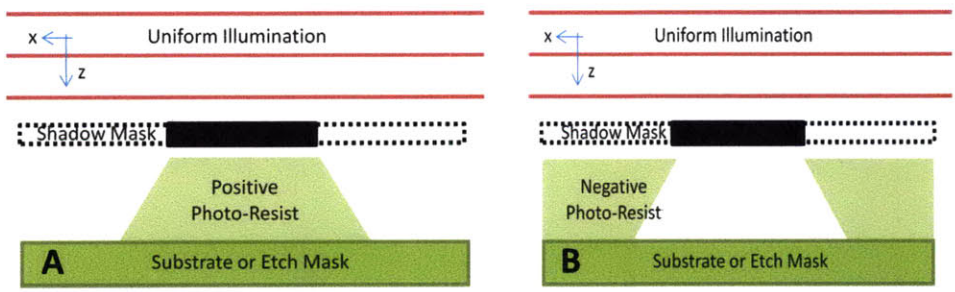


Figure 1-19: Types of Resist

If the energy irradiating a high contrast resist is greater than the resist threshold, all the material in that region will be exposed. The position of the sidewall at a depth z, is defined by the width of the exposure envelop, x_o, at threshold energy as shown in Figure 1-20. The envelope will expand as it passes through the resist according to diffraction theory and shrink in intensity due to absorption. Thus vertical sidewalls are generated by selecting an exposure dose, which has a constant x_o independent of the profile growth.

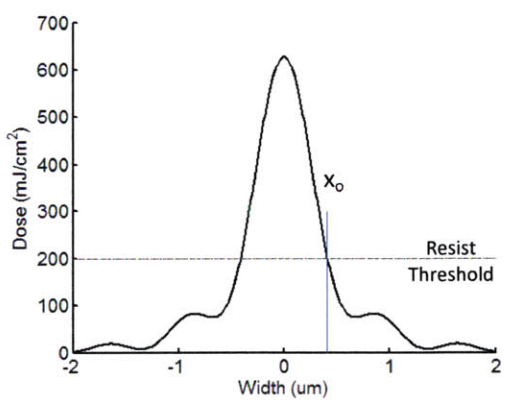


Figure 1-20: Dose Threshold

The dose is delivered by the intensity profile from the optical system and exposure time. In projection lithography the shadow mask is located well above the substrate, allowing for a demagnification of the image to expose the resist. The intensity profile at the wafer is determined by the far field diffraction pattern generated through the mask, setting the minimum feature size to the diffraction limit:

$$d_{min} = \frac{\lambda}{2NA} \text{ for coherent illumination} \quad 1.13$$

$$d_{min} = \frac{\lambda}{NA} \text{ for incoherent illumination} \quad 1.14$$

Typical projection lithography systems operate at 365 nm with an NA of 0.95, setting the minimum half-pitch to 48 nm. Cutting-edge immersion lithography tools add water between the projection lens and the resist increasing the index of refraction and thus the NA to 1.25. By using a coherent 193 nm source, immersion lithography sets the industry resolution limit for projection lithography at 32 nm (half-pitch). In contact lithography the mask is in direct contact with the substrate, creating an intensity profile via near field optical diffraction pattern. With a thin resist and perfect contact the resolution limit for contact lithography approaches the feature sizes on the mask, more precisely defined as [**13**]:

$$d_{min} = \frac{3}{2}\sqrt{\lambda\left(Z_{gap} + \frac{T_{resist}}{2}\right)} \quad 1.15$$

where z_{gap} is the distance between the mask and resist, and T_{resist} is the thickness of the resist. With zero gap and ultra thin resist of 5nm, contact lithography operating at the i-line wavelength of 365nm generates a minimum half pitch of 22 nm. However patterns of 22nm with optical lithography require a shadow mask with comparable feature sizes. Photolithography masks are generally fabricated by electron beam lithography whose resolution is defined by the width of the exposure beam rather than optical diffraction bringing the resolution down to a few nanometers. The pluses and minuses of electron beam lithography will be discussed in more detail later in the section. [**14**]

Although feature resolution is a critical parameter in lithography, linewidth is determined by the width at the base of the resist established by the dose envelope and threshold. Any variations in these parameters will generate dimensional errors. The common sources of error originate in variations in dose, space between the mask and substrate, and resist sensitivity. Errors in the dose profile and thickness affect the width of the envelope shifting the location of x_o, while variations in the resist sensitivity alter the threshold point and in turn slope of the sidewalls. Figure 1-21 shows the effect of varying each of the above variables on the linewidth.

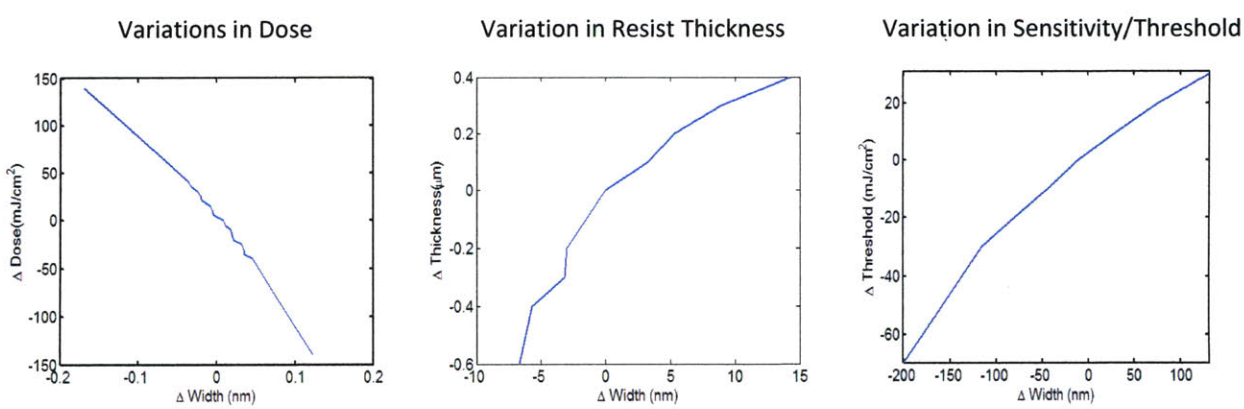


Figure 1-21: Source of Linewidth Variation

From the data shown in Figure 1-21, we find that variations in thickness have the greatest impact on the line width, generating 10nm of line width error with a mere 200nm gap between the mask and substrate. These parameters were generated for contact lithography with 1.4μm of resist, by decreasing the resist thickness one amplifies the errors caused by variations in height generated by nonuniformities in the resist coating and gaps between the mask and the resist. [**15**][**16**]

From the above discussion we have found that optical lithography can meet the demands established in Table 1-1 for device fabrication, however the physical limitation of these systems have not been considered. In contact lithography, gaps between the mask and the photoresist quickly expand the minimum period and linewidth error. The requirement of intimate contact between the mask and the resist introduces contamination transfer between the mask and the sample. As an additional expense repeated use the mask will damage the surface requiring it to be replaced. The pressure applied to the mask to guarantee flush contact can also fracture the samples. Because of the cost of mask replacement, contact errors, and damage to the samples, contact lithography not used in production systems. Projection lithography removes these concerns at the cost of less resolution and lens aberrations due to the optical column. The complexity of an aberration free, high speed, high resolution lithography system makes these tools a luxury found only in high end production labs. However the greatest limitation in optical lithography is the diffraction limit, to achieve resolutions less than 32nm requires a drastic redesign of the optical system such as the new extreme ultra violet system or pattern transfer with electrons, ions, and physical pressure.

1.2.1.2 Electronbeam Lithography

Electron beam lithography uses a focused electron beam and magnetic lens to trace a pattern directly into the resist. Unlike photolithography that is limited by the diffraction limit of light, electronbeam lithography features are limited by the electron spot size and scattering in the resist.

Ebeam resists, like photoresists, chemically change when radiated with energies greater than the threshold value. For high resolution features the threshold maybe on the order 50,000 electron volts, requiring only a few electrons to expose the resist. As the electrons enter the resist they break the bonds of the material causing a generation of secondary electrons that expand away from the initial beam. Each of the generated secondary electrons carries energy that may expose the surrounding resist. As the primary and secondary electrons move through the resist they are scattered away from the initial line forming a cone of exposure within the resist. In polymer resists the secondary electrons may scatter as far as 4-12 nm from the initial line before running out of energy. After passing through the resist, the electrons will pass into the substrate where they continue to generate secondary electrons. Some of the scattered electrons from the substrate will travel back to the substrate surface, further exposing the base of the resist. Low energy electron beam systems generate a broad exposure pattern and shallow profile because the slow speed of the primary electrons allows for easy dissipation of energy to the secondary electrons. In contrast, high energy electron beams will generate tight exposure columns that penetrate deep into the substrate, as shown in Figure 1-22B.

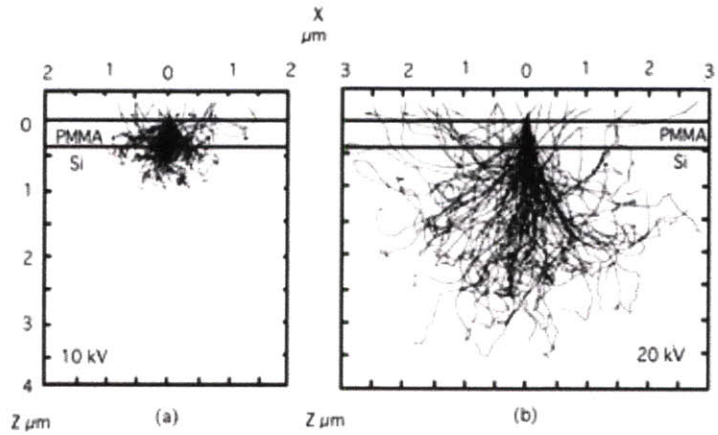


Figure 1-22: Electron scattering in Ebeam Resists[13]

Electron scattering and generation affects the fidelity of the photolithography mask. Electron beam lithography has a negligible spot size with a spread of 1-10 nm depending on the energy of the electron beam. Photolithography's minimal feature size is 32 nm, thus a scattering error of ±2 nm has a minimal effect on the final shape of the features. The effect of scattering is also minimized in optical lithography by the width of the features. A large percentage of the scattering will occur within regions that already have energies above the threshold, thus not effecting the pattern further. [**14**]

With a minimum resolution of 7nm and negligible error electron beam lithography could easily fabricate the devices in Table 1-1.[**17**] However with a spot size of 5 nm a 20 nm by 20nm feature would require 80 separate exposures at 2 seconds a piece. Writing an entire pattern in this manner is time consuming and expensive, making it a poor choice for production. High throughput techniques such as contact optical and nanoimprint lithography can produce an entire chip in a few seconds. As we have discussed above contact lithography is limited by optical diffraction, thus for as a high throughput low resolution lithography alternative we will consider nanoimprint lithography.

1.2.1.3 Nanoimprint Lithography

Nanoimprint lithography uses a 3D mask that is then pressed into the photoresist and held there while the resist is exposed (either from above or below the mask depending on the transparency of the substrate or mask to the UV exposure). A typical nanoimprint process flow is shown in Figure 1-23. By growing thin stacks of material and then selectively etching only one of the two material nanoimprint masks can be made with grating periods of angstroms.

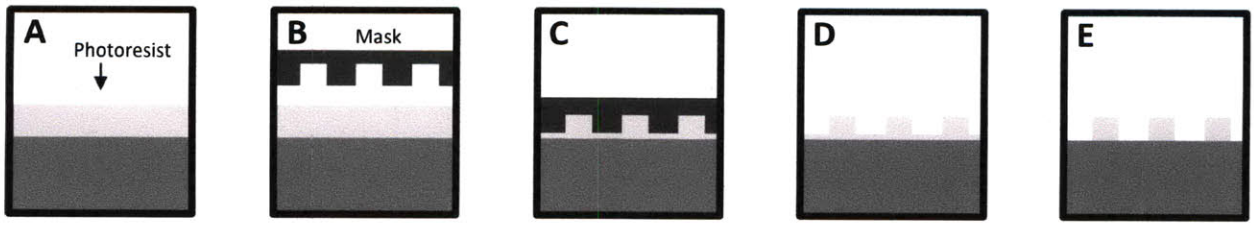


Figure 1-23: Nanoimprint Lithography

The challenges of nanoimprint lithography are similar to that of contact lithography, including contamination transfer, mask deterioration, and the effects of pressure on the substrate. The nanoscale features of the mask may also prevent the material from going up into the crevasses of the mask due to capillary action. However, the biggest problem in nanoimprint lithography is the adhesion of the mask to the resist. Without a good release system removing the mask will rip the small features from the resist and substrate base. This is analogous to removing a cake from an ungreased pan. A secondary step such as ashing is usually required to remove any excess resist left that may have gotten caught under the edges of the mask (Figure 1-23D). Unfortunately this process also damages the fine features transferred into the polymer. Although nanoimprint lithography is found to be a high resolution high throughput solution the combination of mask cost and the damage caused to the resist after exposure out weights the benefits.

After reviewing three forms of lithography we find that all of them can meet the dimensional tolerances defined in section 1.1. However for the production of low tolerance PIC devices the most cost effective and efficient system is contact lithography. From this point on we will assume contact lithography for all lithographic processing.

1.2.2 Etching

Pattern fidelity in etching is achieved through vertical transfer of the mask pattern into the substrate with minimal shrinkage due the isotropic etching, physical damage, or sloped masking materials. After a brief introduction to general etching we shall explore various forms of anisotropic chemistries to determine the most effective method to meet the dimensional demands of monolithic photonic integrated circuits.

Etching is the process of physically and/or chemically removing material. Isotropic or uniform etching occurs when there is an equal amount of etching in the horizontal and vertical directions. The most common isotropic etch is wet etching in which liquid chemicals wash across the device eating away at the surrounding material. By selecting a masking material with a lower etch rate than the substrate, the wet etch will remove the material surrounding the mask transferring the pattern into the substrate. However as the etch progresses the wet etch will aggressively undercut the mask while slowly removing the surrounding mask material as shown in Figure 1-24B.

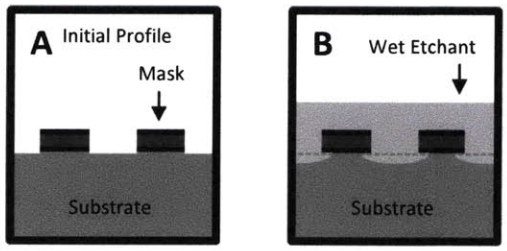


Figure 1-24: Wet Etching

Although vertical profiles can be achieved through crystallographic wet etching, the most reliable technique is anisotropic dry etching.

Dry etching occurs due the substrate's physical and chemical reaction to reactive plasma ions. A common dry etching technique is reactive ion etching (RIE), where a wafer is placed in a vacuum chamber consisting of two parallel plates surrounding a flowing gas mixture as shown below.

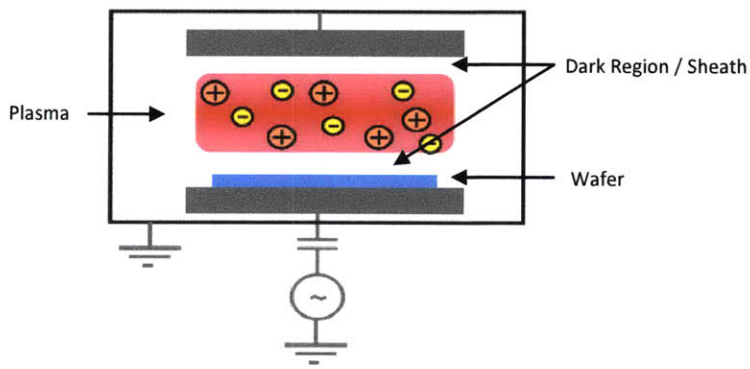


Figure 1-25: RIE Chamber[18]

An AC voltage is applied across the plates sparking a plasma and separating electrons and ions from the gas molecules. The small mass of the electrons allow them to follow fluctuations in the AC field causing them to accumulate on the surface of the plates. At equilibrium a dark region or sheath is formed between the negatively charged plates and plasma, creating a voltage drop across the dark region. The positive ions from the plasma are accelerated through the sheath striking the substrate positioned on the bottom plate. The inert ions will strike the surface of the device, physically etching the substrate through erosion similar to sandblasting. The collision of ions with the substrate may generate volatile reactants, non volatile reactants, or simply break the chemical bonds within on the surface of the device allowing chemical etching. Argon is commonly added to gas mixtures to encourage physical etching due to its lack of reactivity. If the gas is selected so that the ions chemically react with the substrate, the radicals will diffuse into material producing a variety of products. Ideally the etch will produce volatile products that desorb from the surface back into the plasma where they are pushed from the chamber by the gas flow. Nonvolatile products will collect on the surface of the device to be removed by physical etching.[**19**]

The etch rate of the material is established by the gas composition, chamber conditions, and substrate material. The amount of ions in the chamber is set by the RF power used to spark and sustain the plasma in the chamber. The bias voltage generated by the RF power determines the force that the ions strike the surface. While ion directionality set by the chamber pressure, which sets by average ion path length within the chamber. A RIE with a large RF power and low pressure, generates a high density of high energy ions that vertically approach the substrate due to minimal collisions. The high etch rate and directionality of this etch generates vertical sidewalls and heavy surface damage to the substrate. Damage is reduced while retaining etch rate and directionality through inductively coupled plasma reactive ion etching (ICP RIE). In an ICP RIE chamber a secondary coil is introduced to strip the ions and electrons from the gas molecules in the chamber, while the parallel plate power sets the DC bias voltage. By decoupling the ions density and energy, high etch rates can be achieved with minimal surface damage. The rate of material removal given a constant ion energy and density is based on the chemical reaction occurring between the substrate and plasma elements. The most common RIE gas chemistries are based on oxygen, fluorine, methane, or chlorine. Oxygen plasmas are effective for removing organic materials such as photoresist with an etch rate of 1000 A/sec. [**20**] Fluorine plasmas aggressively react with silicon, while chlorine and hydrogen are commonly used for indium etching. Monolithic PICs are built on indium phosphide substrates with SiO_2, photoresist, titanium, or aluminum masks. A given substrate and gas mixture can have a broad range of etch rates, due to the number of process variables in RIE and ICP etching. However it important to have a feel for the range of etch rates for the common substrate, mask, and gas etchants.

Table 1-2: Typical Etch Rates

	Oxygen Etching [A/min]	Fluorine Etching [A/min]		Methane Etching [A/min]	Methane Chlorine Etching [A/min]
	O_2	**CF_3:O_2**	**CF_4**	**CH_4:H_2**	**Cl_2:CH_4:H_2**
Temperature	~25° C	~25° C	~25° C	~25° C	~25° C
Photoresist	1000 [20]	127 – 150 [20]	300 – 720 [21]	-	-
SiO_2	Negligible	255 – 300 [20]	110 – 520 [20]	19 [22]	242 [22]
InP	Negligible	Negligible	Negligible	270-1140[22][23]	8480 [22]*

*Etch rate is inflated due to Bias Power of 1200W

	Chlorine Etching [A/min]						
	Cl_2	**Cl_2: Ar**	**BCl_3 : N_2**	**BCl_3 : $SiCl_4$**	**$SiCl_4$: Ar**	**$SiCl_4$**	**$SiCl_4$: Ar**
Temperature	~200° C	~25° C	~25° C		~25° C	~200° C	~200° C
Photoresist	Large	Large	Large	400,0000 [24]	Large	Large	Large
SiO_2	50[25]	-	-	-	-	50 – 450 [26]	-
InP	1000 [25]	100 – 2000 [27][28]	2750 [28]	-	200-1500 [27]	500-2000 [26]	1300-4000 [29][26]

Table 1-2 shows a variety of material combinations that can be used to effectively etch an InP device. Next we explore the pros and cons of the most common InP dry etching chemistries and relate them to the process ability to minimize linewidth error. Methane hydrogen (CH_4) was the first gas used to etch InP because of its volatility at room temperature and low toxicity. CH_4 reacts with InP to produce PH_3 and $In(CH_3)_X$. The $In(CH_3)_3$ is a volatile substance at room temperature that desorbs from the surface back into the plasma. The organic polymer binds to the inert material such as the mask and previously etched regions of the substrate preventing etching in those regions due to the polymers low etch rate. Although polymer generation has been used to protect sidewalls from isotropic etching, build up of the polymer on the mask will enlarge it causing an expansion of the pattern features in the substrate. To minimize this effect, the polymer is removed through periodic oxygen etches during between CH_4 etches. Poorly timed alternations between CH_4 and O_2 etching will generate a scalloped sidewall.

Chlorine etching was introduced as an alternative to CH_4 because of its fast etch rate of InP and lack of polymer generation. Chlorine etching of InP produces volatile PCl_x and nonvolatile $InCl_x$. The presence of the $InCl_x$ on the surface of the device decreases etch rates while increasing surface roughness. However unlike PH_3, which requires an oxygen plasma step to remove, $InCl_x$ can be removed by increasing the chamber temperature to 140°C or greater. The etch rate increases with temperature until 300° C, at which point the formation of etch products competes with ion assisted desorption for resources lowering the etch rate and promoting lateral etching.[**30**] Thus maximum etch rate occurs when the removal of PCl_x is equal to that of $InCl_x$.[**31**] $InCl_x$ desorption is also increased through the presence of heavier ions in physical etching. Ion mass is increased in chlorine chemistry by introducing bigger molecules such as BCl_3 and $SiCl_4$, as is shown in Table 1-2. Any indium chlorine remaining on the surface at the completion of the etch appears will appear as 'grass' or micro-needles at the base of etch profile, as we will see in Chapter 2.

The effectiveness of the etch is described by the ratio between the etch rate of the substrate over the mask referred to as selectivity. A system with a selectivity of 10:1 will etch the substrate at 10 times faster than mask. High selectivity in wet etching generates a large uncut below mask like the one shown in Figure 1-24B, while high selectivity in dry etching generates highly anisotropic profiles. As discussed previously pattern fidelity is dependent on the verticality of the etch. The angle of the substrate wall is defined by the slope of the mask profile and selectivity according to[**32**]:

$$\theta_{substrate} = \tan^{-1}\left(Selectivity * \tan\left(\theta_{mask}\right)\right) \qquad 1.16$$

This equation is derived from the etching force generated by the ions striking the surface of the wafer. Ideally the ions strike the wafer normal to the surface generating a 100% vertical etching. A slope in the mask will divide the force into the vertical and horizontal components causing lateral recession of the etch mask. This effect defines the linewidth error in etching and points to the importance of lithographic precision.

1.3 First Generation InP Faraday Rotators

First generation InP-InGaAsP-InP faraday rotators were fabricated in 2006 in the MIT Microsystems Technology Laboratories (MTL) by Xiaoyun Guo of the Physical Optics and Electronics Group. The linewidth constraint of 1.4μm ± 50 nm required for maximum Farady rotation necessitated the use of high tolerance low throughput fabrication techniques to ensure success. Electron beam lithography was used to trace the optimal pattern directly into 200nm of Poly-methyl-methacrylate (PMMA), a positive profile electron beam resist. The VS 26 in the nanostructurelab (NSL) was used to expose a 0.3 mm^2 area of resist consisting of 32 1.35μm waveguides each 7 mm long. The pattern of ±5 nm error was exposed over 6 hours using an exposure dose of ~400 $\mu C/cm^2$ and beam size of 6.1 nm. In Section 1.2.2 we found that optimal InP etching is achieved through ICP RIE using chlorine gas. However due to equipment limitations Guo fabricated the device using a methane hydrogen chemistry in an RIE chamber. To improve etch selectivity and reduce the amount resist to be exposed during ebeam lithography, a hard etch mask was pattern using lift off. A comparison of the common etch masks for CH_4 etching found titanium to be superior over SiO_2 because of its improved selectivity and limited micromasking when patterned using lift-off.[**33**] After electronbeam patterning of the resist, 300 nm of titanium was deposited onto the substrate before being etched in a $CH_4/H_2/O_2$ chemistry at MIT LL. This fabrication process is outlined below in Figure 1-26.

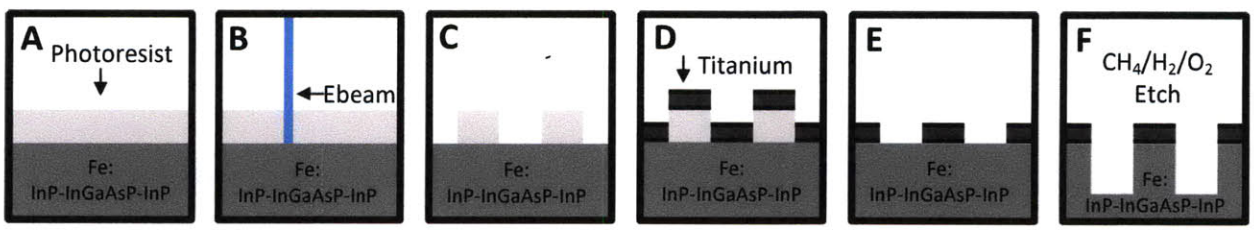


Figure 1-26: Fabrication Process for First Generation Fe:InP Faraday Rotators

The Faraday rotators produced in 2006 utilized iron doped InP to achieve increased polarization rotation. In doing so they removed the need for YIG core, and generated a faraday rotator that can be used for monolithic integration in photonic integrated circuits. However the effect of Fe on the CH_4 etching process had to be considered. Fe^{+3} was found to act as a catalyst for polymer formation during etching. To avoid lengthy oxygen depolymerization etches O_2 was added to the plasma, allowing for continual polymer removal and a smoother more uniform etching profile. An etch rate of 50 nm/min was achieved for the $CH_4/H_2/O_2$ plasma, etching 2.5μm of Fe doped InP in 50 mins. The resulting device is shown in Figure 1-27. Testing of the Fe:InP faraday rotators found a device loss of 4.34 dB/cm and Verdet coefficient of 100 deg/cm/T. [**1**]

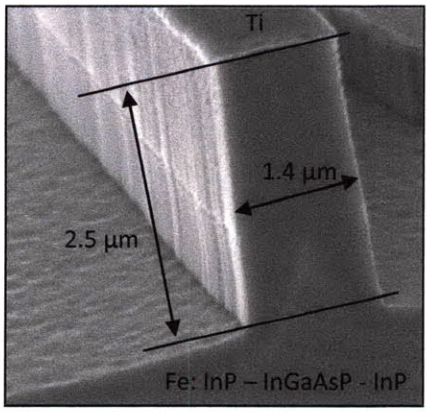


Figure 1-27: First Generation Fe:InP Faraday Rotator [34]

1.4 Fabrication Overview

Proof that iron doped InP can be used for Faraday rotation was the first step to monolithic integration in photonic integrated circuits. A high throughput fabrication process is the next. My process utilizes contact optical lithography and chlorine based ICP RIE to fabricate multiple iron doped InP faraday rotators with a dimensional tolerance of ±250nm.

The InP faraday rotators in this thesis are built on four iron doped epitaxial wafers with an InGaAsP core sandwiched between an InP substrate and upper cladding. The first batch of devices were constructed of the same IQE epitaxial wafer used to fabricate Guo's first generation devices. After a lithographic redevelopment 3 additional sets of InP faraday rotators were fabricated out of MIT Lincoln Lab's iron doped epitaxial wafers. Each wafers used for Faraday rotator fabrication had a different Fe concentration and core width as is outlined in Table 1-3.

Table 1-3: Expitaxial Wafer used for Faraday Rotation Fabrication

Batch Number		Fe Concentration ($1/cm^3$)	InGaAsP Core Thickness(µm)	InP Upper Cladding Thickness (µm)	InGaAsP Q (λpeak)
MITT01-1-2 406-858B	IQE	5.00E+17	0.49	1.04	1.30 +/- 30nm
CCS-0562-A	LL	1.00E+17	0.60	1.00	1.45
CCS-0563-A	LL	undoped	0.60	1.00	1.45
CCS-0568-A	LL	undoped	0.50	1.00	1.34

All devices were patterned with an array of waveguides ranging in width from 1µm - 2µm increasing by 0.05µm every 10 waveguides within the 1 cm^2 pattern. By varying the widths across the sample a Faraday rotator of the proper dimensions is ensured after the accumulation of unexpected fabrication errors. Although a range of devices is available, all linewidth errors were calculated by subtracting the physical width from the intended one on the shadow mask. Contact optical lithography was used to transfer this pattern into positive tone AZ-5214E photoresist with a dose of 1365 mJ/cm^2.

The photoresist's inability to with stand a chlorine etch mandated the need for an SiO_2 hard mask, which was uniformly deposited by plasma enhanced chemical vapor deposition (PECVD) before lithography. The 250 nm of SiO_2 was then patterned in a combination CHF_3 / CF_4 reactive ion etch over the course of 26 minutes. After removing the photoresist, the iron doped InP-InGaAsP-InP wafer was etched for 2 minutes in a Cl_2 / $SiCl_4$ /Ar ICP RIE etch chemistry to obtain a uniform 2μm etch depth across the sample. This fabrication process for InP Faraday rotators involving SiO_2 deposition, contact lithography, RIE fluorine etching, and ICP RIE chlorine etching of the epitaxial wafer is outlined in Figure 1-28. The specific parameters and handling conditions for each step in the process are described in detail within the following chapters.

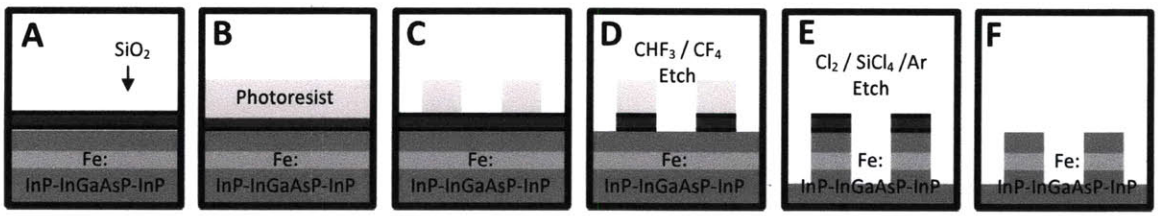


Figure 1-28: InP Faraday Rotator Process Flow

1.5 Thesis Overview

The purpose of this thesis is to develop a high throughput low cost method for fabrication the InP photonic devices, which produces repeatable linewidth control of ±65 nm. As a proof of concept we fabricated iron doped Faraday rotators and half-wave plates. The fabrication process utilizes contact optical lithography and chlorine ICP RIE to ensure linewidth control while maintaining the high throughput requirement. Chapter 2 considers ICP RIE etching of InP-InGasAsP-InP devices, exploring the effects of carrier wafer material, vacuum grease, chamber preconditioning, as well as the gamit of etching parameters defined in Section 1.2.2. With an established ICP RIE recipe we consider the single and bi-layer dielectric etch masks and the RIE fabrication process required to pattern them in Chapter 3. This is followed by a detailed lithographic review exploring the effects of exposure wavelength and resist thickness, as well as the most effective method for ensuring flush contact between the mask and the resist. The dimensional fidelity will be verified with the loss and zero birefringence wavelength of the Faraday rotation performance data. The effect of variations in core thickness and iron doping will also be tested and theoretically verified. Chapter 6 will consider future and ongoing work including fabrication status of monolithic integration of InP half waveplates and optical isolators.

2 Fabrication Process Overview for ICP RIE Etching of InP Photonic Device

Optimal performance of a Faraday rotator at 1550 nm occurs within a 1.4μm waveguide with an etch depth of 2μm. These dimensional parameters are defined by the geometrical zero birefringence width and depth required for optical confinement within the core. The performance parameters for an InP Faraday rotator are measured after etching the epitaxial wafer. Thus it is important to develop an ICP RIE recipe that will produce features with linewidth tolerances of ± 65nm, smooth vertical sidewalls, and minimal micromasking on the surface of the wafer. By meeting these specifications we can fabricate low loss faraday rotators which will operate within the wavelength range of a tunable laser.

In this chapter we will examine the ICP RIE recipe developed for etching of InP in silicon-tetrachloride ($SiCl_4$). Smooth anisotropic etches were achieved by balancing gas composition, ICP and bias power, and chamber pressure. While repeatability was obtained by establishing a series of fabrication steps that ensured reproducible chamber conditions in the ICP RIE etcher. In Section 2.1.1 and 2.1.2 we examine the effect of external factors such as carrier wafer material and the use of vacuum effect on repeatability and etch profile. Once these chamber conditions have been established, a detailed discussion of recipe optimization using a design of experiment called the Taguchi Method is held in Section 2.1.3. The chapter concludes with a detailed overview of the ICP RIE process used to fabricate InP Faraday rotators.

2.1 Process Development

The fabrication process developed for InP Faraday rotators was the result of experimental optimization of previously established ICP RIE recipes. Development began with a literature review of ICP RIE recipes used for etching InP in a $SiCl_4$ etch chemistry. A summary of our findings as well as the recipes used by colleagues on campus and at MIT Lincoln Laboratory is shown in Table 2-1.

Table 2-1: Published ICP RIE Etch Recipes for InP

	Gas Chemistry	ICP Power	Bias Power	Pressure	Temp	Carrier Wafer	Vacuum Grease
Recipe 1[35]	$SiCl_4$/Ar : 7 /20 sccm	1000 W	200 W	2 mTorr	25°C	Silicon	No
Recipe 2 [36]	$SiCl_4$: 20sccm	300 – 1200W	5 – 150 W	2-30 mTorr	-175°C to 80°C	-	-

Recipe 3[26]	$SiCl_4$/Ar : 3 / 30sccm	300 W	100 W	5 mTorr	180°C or 300°C	-	Both
Recipe 4[26]	$SiCl_4$/Ar /N_2O: 15 / 50 / 1.5 sccm	500 W	120 W	10 mTorr	-	-	-
Recipe 6[37]	$SiCl_4$ or Cl_2 or Ar: 1 sccm	300 W	100 W	3.75 mTorr	180°C	-	-
Recipe 7[29]	$SiCl_4$/Ar : 0.5 / 8 sccm	500 W	100 W	1.5 mTorr	200°C	Silicon	Yes
Shih Recipe[38]	$SiCl_4$/Ar /Cl_2: 2 / 10 / 0.5 sccm	250 W	160 W	4.5 mTorr	220°C	Ceramic	No
LL Recipe 1[39]	$SiCl_4$/Ar /Cl_2: 0.5 / 10 / 0.75 sccm	250 W	250 W	3.75 mTorr	220°C	Silicon	Yes
LL Recipe 2[39]	$SiCl_4$/Ar /Cl_2: 0.29 / 8.3 / 0.56 sccm	250 W	250 W	3.75 mTorr	220°C	Silicon	Yes

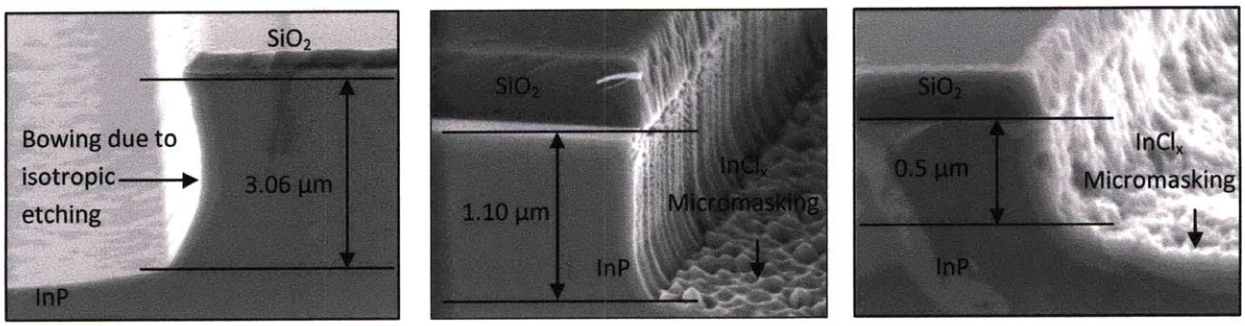
The recipe variations in Table 2-1 stems from the dependent interaction of etching parameters such as plasma composition, ICP power, bias power, and pressure with the chamber conditions such as temperature, carrier wafer material, and the use of vacuum grease. Consider Shih's recipe, he developed a III-V etching recipe in the SAMCO ICP RIE without vacuum grease between the sample and a ceramic carrier wafer. As opposed to Lincoln Labs' etch recipes that uses a silicon carrier wafers with vacuum grease. Most recipes in Table 2-1 etch the InP with a high temperature vacuum chuck to help promote $InCl_x$ desorption during etching, however recipe 1 and 2 showed anisotropic etching at low temperatures. Because of the influence of the physical parameters on the etch profile and micromasking, it was important to define the carrier wafer, temperature, and vacuum grease protocols before optimization of the etching parameters.

In Section 2.1.1 we use Shih's recipe as a baseline to explore the effects of vacuum grease and chuck temperature on the etch. The effects of different carrier wafers on etch rate, profile, and micromasking will be examined in Section 2.1.2. After establishing the significances these three physical parameters, we optimize the etch results by adjusting the gas flow, power, and pressure. From Table 2-1 we see broad variation in these etching values. Recipe optimization was performed by defining a high, median, and low set point for each parameter. Testing every permutation of etching parameters and set points would require 64 individual etches, however by utilizing a design of experiment technique referred to as the Taguchi method we were able to obtain the same optimization information in 9 etches. The theoretical justification behind the Taguchi method and the results of the design of experiment optimization is examined in Section 2.1.3.

2.1.1 Temperature

As mentioned in Chapter 1 sample temperature plays an important role in the physical and chemical dynamics of etching InP. During the etch process, chlorine ions are striped from the $SiCl_4$ and Cl_2 gas within the plasma. The ions diffuse to the surface and generate PCl_3 and $InCl_x$. The PCl_3 is highly volatile compound that desorbs back into the plasma and is removed. The $InCl_x$ remains on the surface until it becomes volatile at temperatures above 140°C or is remove by physical etching. This trend remains constant until the substrate temperature reaches 300°C, at which point the etch rate falls off and lateral etching is observed. With this physical intuition we can efficiently approach temperature based etching optimization.

In Chapter 1 we discussed the importance of the sample temperature remaining between 140 °C - 300°C for effective $InCl_x$ and PCl_x desorption.[**31**] With temperatures ranging from 6000°C – 9000°C, the hot plasma will increase the temperature of InP sample during etching. [**40**] Consider the etch profiles shown Figure 2-1. Each of the samples were etched using Shih's recipe from Table 2-1 for 2 minutes.



(A) InP Sample on 220°C ceramic wafer without vacuum grease

(B) InP Sample on 170°C ceramic wafer without vacuum grease

(C) InP Sample on 220°C ceramic wafer with vacuum grease

Figure 2-1: Temperature Dependent Etch Profiles

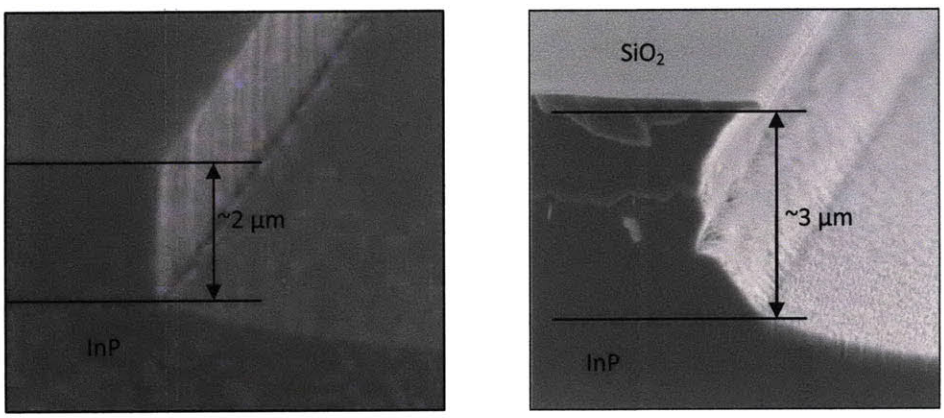
Figure 2-1A is the result of an InP sample etched on a 220°C ceramic wafer without vacuum grease. As the surface temperature of the InP sample rises so will etch rates until the surface reaches 300°C. At which point isotropic chemical etching of the InP sidewalls begins along with a significant slowing of the etch rate. This is clearly seen in the etch profile in Figure 2-1A. By decreasing the carrier wafer temperature, we can decrease the sample temperature during etching. In Figure 2-1B the ceramic wafer is set to 176°C. This reduces the sample temperature enough to prevent isotropic etching but also reduces the desorption of $InCl_x$ radicals on the surface of the wafer. By thermally adhering the sample to the helium cooled carrier wafer with vacuum grease, sample heating due to the high temperature plasma was minimized. Figure 2-1C is the etch result of an InP sample on a 220°C ceramic carrier wafer with vacuum grease, now we see a drastic an increase in $InCl_x$ micromasking and a significant decrease in the etch rate - both are a direct result of reduced sample temperature.

The results of this section establishes a clear need for vacuum grease to improve temperature control during etching. The introduction of a thermally control environment will ultimately reduce

variability in the etch profile. However the etch results in Figure 2-1C is unacceptable for production and mandates a need for recipe retuning to increase etch rates and remove the $InCl_x$ build up on the surface of the structure.

2.1.2 Carrier Wafer

Consider the etch recipes in Table 2-1, the common feature in most of etch recipes is the presence of a silicon carrier wafer. Matsutani explored the effect of silicon carrier wafer verse ceramic and found that the reduction of Si ions in the chamber added to the build up of $InCl_x$ and deterioration of the photoresist etch mask.[**37**] His results point to the dramatic effect of etching radicals originating from the carrier wafer. We tested this hypothesis by etching a bulk InP sample on a ceramic carrier wafer with a recipe developed at MIT Lincoln Lab for InP etching on a silicon wafer. The resulting profiles are shown below in Figure 2-2.



(A) MIT Lincoln Lab Recipe[**39**] (B) Ceramic Wafer Trail

Figure 2-2: Carrier Wafer Test

$SiCl_4$/Ar /Cl_2:	$SiCl_4$/Ar /Cl_2:
0.5 / 10 / 0.75 sccm	0.5 / 10 / 0.8 sccm
ICP Power: 250 W	ICP Power: 250 W
Bias Power 250 W	Bias Power 250 W
Pressure: 3.75 mTorr	Pressure: 3.00 mTorr
Silicon Carrier Wafer	**Ceramic Carrier Wafer**
220°C	220°C
Vacuum Grease Used	**Vacuum Grease NOT used**

The etch profile on ceramic wafer shows an increase in $InCl_x$ but its presence on the surface is minimized by the high InP substrate temperature as a result of poor thermal contact. Although the industry standard for InP etching in ICP RIE uses a silicon carrier wafer, recent concerns over material build up on the chamber walls due to the additional etching material has lead to interest in non reactant carrier wafers such as Al_2O_3 ceramic wafers. Use of a ceramic wafer will also minimize variability by removing a radical source. For these reasons we focus on the development of InP etching recipes on a ceramic carrier wafer.

2.1.3 Recipe Optimization

At this point we have established that ICP RIE etching of InP samples on ceramic carrier wafer with vacuum grease cooled to 220°C produces consistent temperature profiles across the wafer that will lead to better repeatability. With the chamber conditions defined we can optimize the etch profile by adjusting the gas composition, ICP and bias power, and chamber pressure. Because of the infinite permutation of ICP RIE etching parameters we decided to optimize the etch recipe using a design of experiment technique called the Taguchi method.

The Taguchi method uses probability theory to generate the minimum number of experiments required to understand the effect of each design parameter and its variability on the system. The scientist defines a set of design parameters for the product and their corresponding range of set points or factors. Our products has four design (or etch) parameters with 3 factors - low, middle, and high. A test case or performance parameter(PP) is a single permutation of the design parameters and factors. In our example the PP is an etch recipe, with 64 total PP permutations in the experiment. Taguchi proposed a method to minimize the number of required fabrication tests by finding the test cases or PP with most significant variation from the target product. [**41**] The subset of permutations was selected by assuming that the higher order process variable combinations are insignificant. This assumption can be verified by finding the response function of each permutation.[**42**] The set optimization tests are defined by series of orthogonal arrays which are based on the number of design parameters and factors for a given product. The L-9 orthogonal array shown in Table 2-2 defines the 9 test cases for 4 design parameters and 3 factors.[**43**]

Table 2-2: Taguchi L-9 Orthogonal Array

Test #	Design Parameter 1	Design Parameter 2	Design Parameter 3	Design Parameter 4
1	Factor 1	Factor 1	Factor 1	Factor 1
2	Factor 1	Factor 2	Factor 2	Factor 2
3	Factor 1	Factor 3	Factor 3	Factor 3
4	Factor 2	Factor 1	Factor 2	Factor 3
5	Factor 2	Factor 2	Factor 3	Factor 1
6	Factor 2	Factor 3	Factor 1	Factor 2
7	Factor 3	Factor 1	Factor 3	Factor 2
8	Factor 3	Factor 2	Factor 1	Factor 3
9	Factor 3	Factor 3	Factor 2	Factor 1

At the completion of testing the scientist can empirically determine the test case producing the target product.[**44**][**45**]

For our design of experiment we had to define the high, middle, and low factors for each of the 4 design parameters. The recipes from collaborators run on ceramic carrier with vacuum grease generated poor etch profiles with heavy micromasking as seen in Figure 2-1. A baseline recipe was

defined by taking the median values from all of the etches in Table 2-1, which became the center factors for the Taguchi optimization.

Gas: $SiCl_4$	2.5 sccm
Gas: Ar	17.5 sccm
Gas: Cl_2	0.6 sccm
ICP Power	300 W
Bias Power	150 W
Pressure	4 mTorr
Temperature	220°C
Carrier Wafer	Ceramic
Vacuum Grease	Yes

Next the high and low values for gas composition, ICP and bias power, and chamber pressure had to be determined. Because of the amount of variables in the gas composition we defined two constants. First, the total amount of gas within the chamber is equal to 20 sccm. Second the ratio of $SiCl_4$:Cl_2 remains constant at 4:1. Thus the adjustment factor for gas composition was the ratio of $SiCl_4$:Ar – which we defined as 1:5, 1:7, and 1:10. These values were selected because of the consistent trend in Table 2-1 to have more argon in the chamber than $SiCl_4$. The following three design parameters had factors defined by observing the range values in Table 2-1 and defining a good step size. This resulted in the factors defined below in Table 2-3.

Table 2-3: Taguchi Parameters: Trial #1

Design Parameter	Factor 1	Factor 2	Factor 3
Ratio of $SiCl_4$: Ar $SiCl_4$: Ar : Cl_2 (sccm)	1:5 3.33 : 16.7 : 0.8	1:7 2.5 : 17.5 : 0.6	1:10 1.8 : 18.2 : 0.4
Pressure	2 mTorr	4 mTorr	6 mTorr
ICP Power	200 W	300 W	400 W
Bias Power	100 W	150 W	200 W

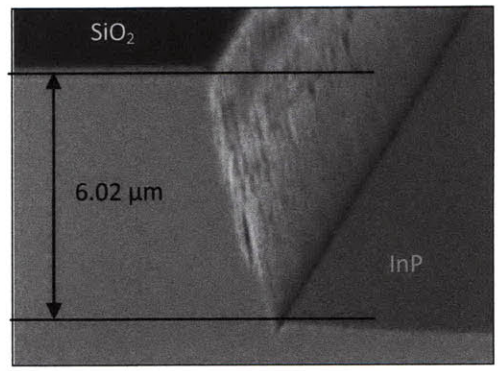
Matching the factors to the design parameters in the L-9 orthogonal array we defined the 9 individual etch recipes used for optimization.

Every optimization etch consisted of 2 min period of gas flow to prime the lines and chamber before sparking the plasma. This was followed by 10 seconds of high power, high pressure etching to ensure plasma sparking and then a 5 min etch using the etch recipes established by the Taguchi method. If we define the target product as a vertical etch profile with smooth side walls and minimal micromasking, the best etch profile resulted from trial 8. The recipe and etch profile are shown below.

Table 2-4: Results of Taguchi Etch Trial #1

Design Parameters	Optimal Variations
$SiCl_4$ Ar Cl_2	1.8 sccm 18.2 sccm 0.4 sccm
ICP Power	200 W
Bias Power	200 W
Pressure	4 mTorr

Resulting Etch Profile



The pronounced sidewall angle in the resulting etch is a consequence of poor ion directionality resulting from shorten mean free path from excess bias power and pressure. To improve the profile further a second Taguchi optimization was performed. The sidewall roughness is due to defect in the SiO_2 etch mask developed during RIE etching, this problem and its solution will be discussed in Chapter 3.

The second Taguchi optimization was centered around the recipe defined by in the first optimization process (Table 2-4) and used smaller variation around the median to define the high and low points. In contrast to the first design of experiment, the gas concentration was defined by the ratio of $SiCl_4$:Cl_2 while the ratio of $SiCl_4$:Ar remained constant at 1:10. The chamber pressure was further reduced to help improve the mean free path length, and the step size defined in pascals rather than mTorr, which explains the awkward spacing of the pressure factors in Table 2-5. The design parameters and factors for the second Taguchi optimization are defined in Table 2-5.

Table 2-5: Taguchi Parameters: Trial #2

Design Parameter	Variation 1	Variation 2	Variation 3
Ratio of $SiCl_4$: Cl_2 $SiCl_4$: Ar : Cl_2 (sccm)	2 : 1 1.7 : 17.2 : 0.8	4 : 1 1.8 : 17.2 : 0.6	6 : 1 1.8 : 18.0 : 0.4
ICP Power	150 W	200 W	250 W
Bias Power	150 W	200 W	250 W
Pressure	2.25 mTorr	3 mTorr	3.75 mTorr

In the second optimization trial 1 produced the best etch exhibiting a vertical profile with a deep trench at the base of the ridge (Figure 2-3). Since the device operation occurs within the epitaxial core located 0.75 µm below the surface, trenching at the base will have no effect on operation and can be ignored.

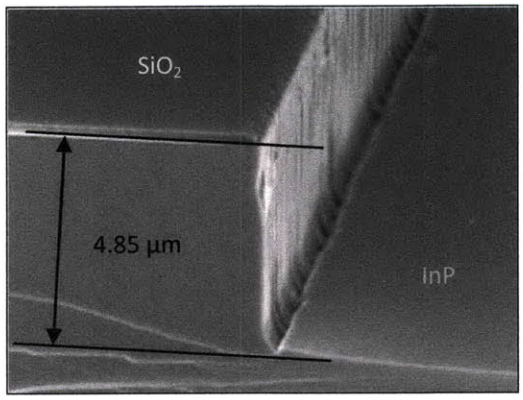


Figure 2-3: Best Etch Profile from Second Taguchi Optimization

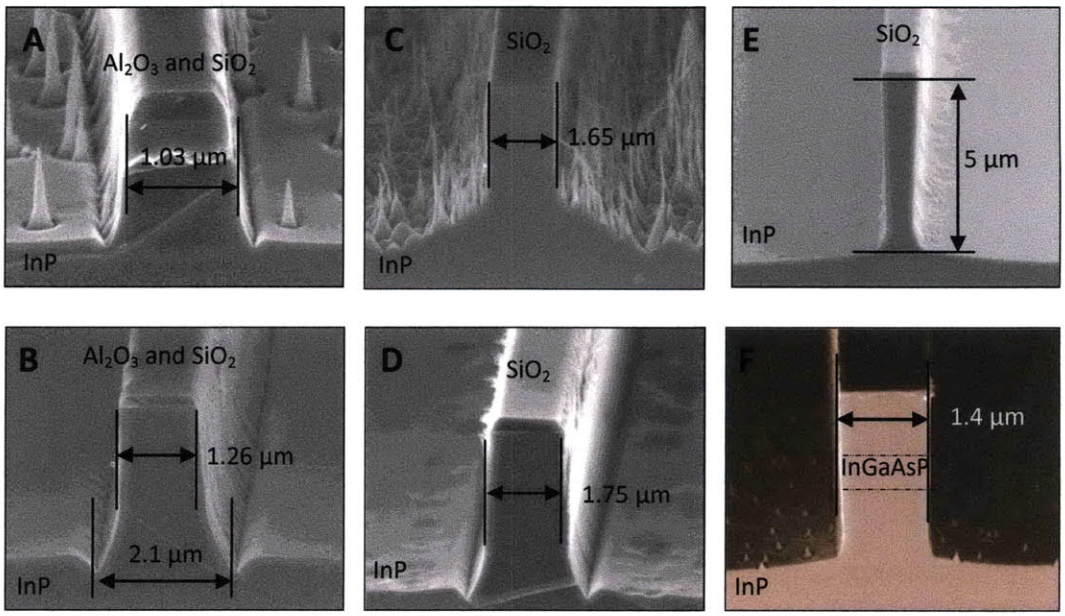
The final recipe defined by Taguchi optimization is outlined in Table 2-6.

Table 2-6: ICP RIE Recipe developed through Taguchi Optimization

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time	2 mins	10 sec	2-3 mins
Gas: Cl_2	0.8 sccm	0.8 sccm	0.8 sccm
Gas: $SiCl_4$	1.7 sccm	1.7 sccm	1.7 sccm
Gas: Ar	17.2 sccm	17.2 sccm	17.2 sccm
ICP Power	0 W	200 W	150 W
Bias Power	0 W	200 W	150 W
Pressure	~15 mTorr (set gate to 27%)	~15 mTorr (set gate to 27%)	2.25 mTorr

The optimized ICP RIE etch recipe was defined early on in process development, leading to repeatability testing of the ICP RIE recipe in Table 2-6. In doing so it highlighted two major limitation in the etch recipe. The first is the linewidth broadening and the deep trench at the base of the structure as seen in Figure 2-4A, Figure 2-4B, and Figure 2-4D. These features are caused when non-reactive ions ricochet off the sidewalls and are redirected towards the substrate physically etching away a groove at the base of the device. The redirection of the physical components of the etch caused a broadening of the profile at the base, ultimately generating linewidth error. By decreasing the physical etching component of the recipe, namely argon, we were able to remove these effects.

Figure 2-4: Evolution of the ICP Etch Profile



Recipe 1: Al_2O_3 and SiO_2 Hardmask

Recipe 1: SiO_2 Hardmask

Optimized Recipe 1: SiO_2 Hardmask

The second concern lies in the appearance of heavy micromasking of $InCl_x$ in ~30% of the etches, an unacceptable side effect for photonic device fabrication (Figure 2-4C). $InCl_x$ is generated during the chemical reaction between $SiCl_4$ and InP. The heavy molecule does not readily desorbs and remains on the surface as microneedles until it is removed thermally or by physical etching. From the trenching in the etch profile, we know there is already an excess of physical etching in recipe. Thus the solution to the micromasking issue must lie in the reduction of chemical etching components such as $SiCl_4$ and Cl_2. Implementing both of these changes to the etch recipe developed with the Taguchi method showed improve etch verticality and limited micromasking during ICP RIE etching of InP (Figure 2-4E and Figure 2-4F). Table 2-7 contains the finalized etch recipe used for etching InP photonic devices in this thesis.

Table 2-7: ICP RIE Etch Recipe for InP Devices

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time	2 mins	10 sec	2-5 mins
Gas: Cl_2	0.4 sccm	0.4 sccm	0.4 sccm
Gas: $SiCl_4$	2.5 sccm	2.5 sccm	2.5 sccm
Gas: Ar	12 sccm	12 sccm	12 sccm
ICP Power	0 W	200 W	150 W
Bias Power	0 W	200 W	150 W
Pressure	~15 mTorr (set gate to 27%)	~15 mTorr (set gate to 27%)	2.25 mTorr

Fabrication success was determined by measuring the linewidth of each waveguide and comparing against the intended width defined on the shadow mask. Figure 2-4 shows a collection of ICP RIE etch profiles generated during the process development. Figure 2-5 plots the linewidth error at the top and bottom of the waveguide verses run number. If more than one measurement was taken from a given sample the data points are stacked vertically over the run number as is done for run #79 below.

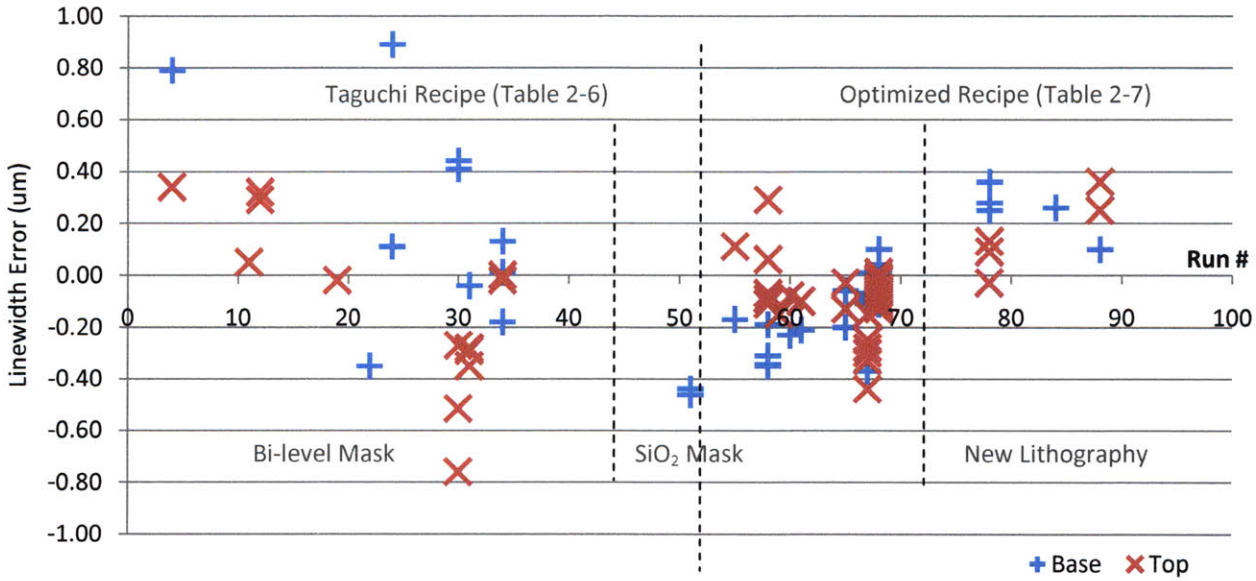


Figure 2-5: ICP RIE Linewidth Error

The Taguchi recipe defined in Table 2-6 corresponds to the first 51 etches in Figure 2-5. By replacing the dual layer SiO_2 and Al_2O_3 mask with a pure SiO_2, we found in drastic improvement in the RIE mask control and in turn an improvement in ICP RIE linewidth error. The next significant improvement came after the optimized Taguchi recipe (Table 2-7) was implemented. This trend continued for some time until an increase in lithographic variability added to the linewidth error during ICP RIE. Any additional improvements in linewidth error in are a result of improved profile control during photolithography and etching. By selecting the etches that correspond to good photolithographic pattern transfer, a method refined during process development and discussed in Chapter 4, we find a linewidth of ±250 nm as shown in Figure 2-6. Measurements of linewidth error at this stage will be confirmed in Chapter 5 through the experimental derivation of the zero birefringence point.

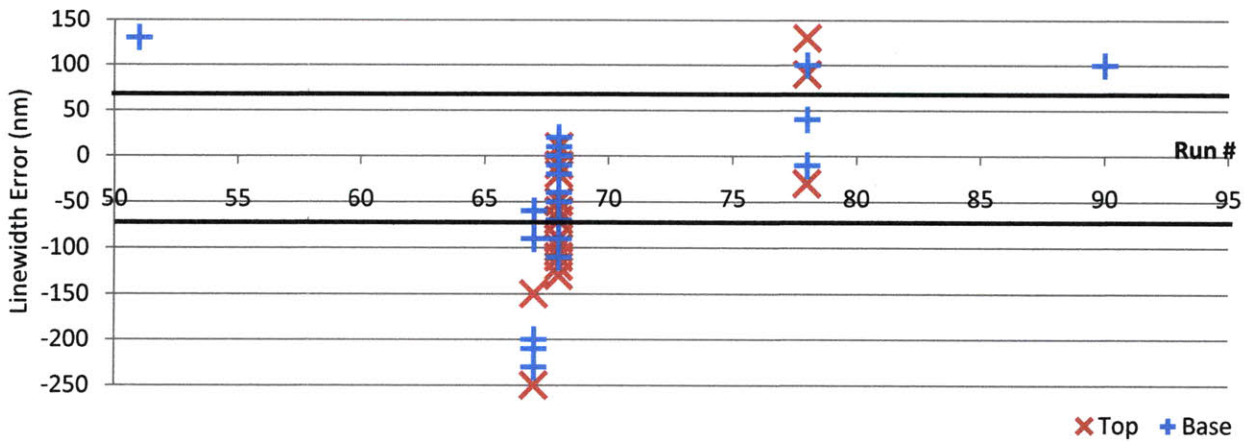


Figure 2-6: ICP RIE Linewidth Error for samples with Optimal Lithographic Contact

2.2 Fabrication Process Overview for ICP RIE Etching of InP Photonic Device

2.2.1 ICP RIE Etching

With a detailed understanding of the ICP RIE parameter one can now appreciate the nuances of the fabrication process to obtain repeatable high tolerance results. In this section we will closely examine the ICP RIE fabrication process used to etch InP photonic devices in this thesis.

The first step in any etching process is chamber preconditioning. The procedure begins with a deep clean of the etching chamber using argon and oxygen plasma combination. This will remove any residual etch products within the etch chambering providing a blank slate for future etches. After cleaning is complete the etch recipe is run for 16 minutes to prime the lines and to coat the sidewalls proper etch reactants. The most critical step in chamber preconditioning is the introduction of InP to a clean etch chamber by etching a bulk InP device. The first InP etch within the chamber always has a significant $InCl_x$ build on surface appearing black to the eye. After this initial etch, micormasking is no longer an issue with the recipe described in this section. Whether this first etch adds vacuum grease, PCl_x, $InCl_x$, or simply removes or absorbs the remaining argon or oxygen radicals from the etch chamber is unknown. At the completion of this step the etch chamber is properly conditioned and ready for future etches.

During the course of process development two different vacuum greases were used to thermally adhere the sample to the carrier with identical etching results. Apiezon H is a thick high temperature grease, is applied best by dabbing it onto the back of the sample with a wooden rod, typically the end of cleanroom swab. Several approaches were suggested for the repeatable application of vacuum grease to the sample, all following two rules of thumb. One, vacuum grease should completely cover the back of the sample ensuring good contact when pressed flat against the carrier wafer. Two excess vacuum grease on the wafer or edges of the sample surface will not affect the etch. Grease that ends up on the face of the sample should be left alone until after etch, it will not affect the etch profile but will leave particles within the trench of the wafer. Attempting to clean the sample before etching will smear the

grease across the surface further. MIT Lincoln Laboratory applies vacuum directly onto the carrier wafer then spreads it uniformly with small rakes fabricated in house. Lack of access to micro-rakes makes this a nonviable option for my research. On campus I squeeze vacuum grease onto a glass slide allowing for easier access to the material. For high viscosity grease I suggest smearing the grease across the slide, placing sample into the grease, and moving it around with tweezers to sufficiently coat the back of the sample. Thick vacuum grease such as Apiezon was collected on the end of wooden stick that is then used to dab and smooth the material across the back of the sample while being held with tweezers. Once coated use a clean pair of tweezers to gently place the sample grease side down on the ceramic carrier wafer and press it flush against the surface. During this stage be aware of excess grease escaping from beneath the InP sample. Any grease collected on the edges of your tweezers is easily transferred the sample surface while applying pressure to the four corners to ensure contact.

Once the sample is thermally attached to the ceramic carrier wafer, both are placed into the load lock chamber of the SAMCO ICP RIE. When placing the wafer into the mechanical arm ensure the ceramic carrier wafer is pressed against the back edge (edge closest to the user) of the load arm to prevent He pressure errors during loading. The optimized etch recipe developed above has an etch rate of ~1μm/min, using this information calculate the desired etch time and execute the following recipe.

Table 2-8: ICP RIE Etch Recipe for InP Devices

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time	2 mins	10 sec	2-5 mins
Gas: Cl_2	0.4 sccm	0.4 sccm	0.4 sccm
Gas: $SiCl_4$	2.5 sccm	2.5 sccm	2.5 sccm
Gas: Ar	12 sccm	12 sccm	12 sccm
ICP Power	0 W	200 W	150 W
Bias Power	0 W	200 W	150 W
Pressure	~15 mTorr (set gate to 27%)	~15 mTorr (set gate to 27%)	2.25 mTorr

At the completion of the etch carefully remove the InP sample and place it in a bath of trichloroethylene.

The carrier wafer and sample can be cleaned by gently scrubbing the surface with trichloroethylene to remove burnt on vacuum grease. Excess vacuum grease on the ceramic carrier wafer will appear black after etching. These regions will clean themselves during subsequent etches or during the 10 min preconditioning etch. The sample and wafer are then rinsed with acetone, methanol, and isopropanol and blown dry with N_2. If this is the last etch with this material, place the cleaning ceramic carrier wafer into the load lock of the ICP RIE and start the 6 hour 'Post Clean.'

2.2.2 Remove SiO_2

After etching the SiO_2 mask must be removed to reduce loss in the waveguide. This is easily accomplished by soaking the InP sample in a bath of 7:1 buffered hydrofluoric acid. Before working with buffered HF ensure that you have been properly trained to use the chemical and wear the correct

personal protective equipment (PPE). Carefully pour a minimal amount of buffered HF into a plastic or ceramic bowl, place the InP sample into the container and gently agitate the solution. With an etch rate of 90 nm/min the hydrofluoric acid will completely remove the 250 nm of SiO_2 in 4 minutes. At the completion of the etch remove the InP sample and rinse in flowing DI water for 1-2 minutes and put away. During cleanup be sure to thoroughly the tweezers, container, and gloves.

No matter how tight the etch control of the ICP RIE parameters maybe, device linewidths are ultimately limited by the linewidth control of the previous fabrication steps as is apparent in Figure 2-5. The presence of an Al_2O_3 /SiO_2 bi-layer hard mask increased the linewidth by an order of magnitude because of sputtering of the low etch rate material around the mask. We also observed in Figure 2-3 an increase in sidewall roughness for the devices that were fabricated with a damaged or 'feathered' SiO_2 mask. Although the devices measured in Figure 2-6 do not meet the ±65 nm fabrication requirement for Faraday Rotators. This width is not a by product of the ICP RIE process but rather the collimation of all the fabrication steps to this point. Chapter 3 explores the RIE process that lead to a ±250nm linewidth error in the SiO_2 hardmasks. During this discussion the effects of different etch chemistries, ion energies, and masks will be closely examined in order to determine the optimal combination of factors to produce the SiO_2 hardmask used in this chapter.

3 Fluorine Etching of Dielectric Hard Masks

SiO_2 was selected as the ICP RIE etch mask because of its 1:25 selectivity over InP. As mentioned in the last chapter, device properties such as linewidth, sidewall roughness, and verticality are a direct result of the etch mask. In this fabrication process the SiO_2 etch mask is patterned using a photoresist mask and a CHF_3 / CF_4 combination etch to achieve linewidth variation on the order of ±250nm. In Section 3.1, the pros and cons of CHF_3 and CF_4 are considered as well as the decision to use a two step etching process that utilizes both chemistries. During the discussion of CF_4 we will also examine two RIE etch masks, ultimately deciding on photoresist over aluminum oxide because of Al_2O_3 sputtering errors that lead to unacceptable variability in the RIE and ICP RIE linewidth error. The chapter closes with a detailed overview of the RIE procedure highlighting critical processing details as was done at the conclusion of Chapter 2 for ICP RIE etching.

3.1 Process Development

Reactive ion etching (RIE) of SiO_2 in a fluorine plasma is a well established technique that is been used in the literature and MIT since Irving's work in 1969.[**46**] Rather than starting from scratch, RIE process development began with the established recipes of MIT's Nanostructure Laboratory (NSL) summarized in Table 3-1. The RIE recipes were developed for the Plasmatherm 790 series in the MIT's Nanosctructures Laboratory. The tool supplies RF power to the gas within the etching chamber sparking the plasma and pulling electrons and ions from the molecules. Just as in ICP RIE the free electrons build up on the parallel conducting plates that surround the plasma. This produces a DC bias voltage in the chamber that accelerates the ions towards the sample resting on the grounded bottom plate. The etch rate is determined by the number ions in the chamber and the energy at which they strike the wafer. In an RIE chamber both of these values are determined by the RF power. An increase in RF power ionizes more molecules within the plasma, generating more electrons which accumulate and increase the bias voltage. To generate greater DC voltages without the need for excessive RF power, the electron path to ground the through a small hole on the outside of the bottom plate can be blocked with a glass slide. This technique is commonly used in the MIT's NSL to achieve high RIE etch rates within the Plasmatherm. Because of the coupling between the chamber power and DC bias voltage, RIE etching recipes target one of the two parameters. Table 3-1 provides a summary of established RIE etch recipes collected from various graduate students at MIT.

Table 3-1: Established SiO_2 Etch Recipes[47]

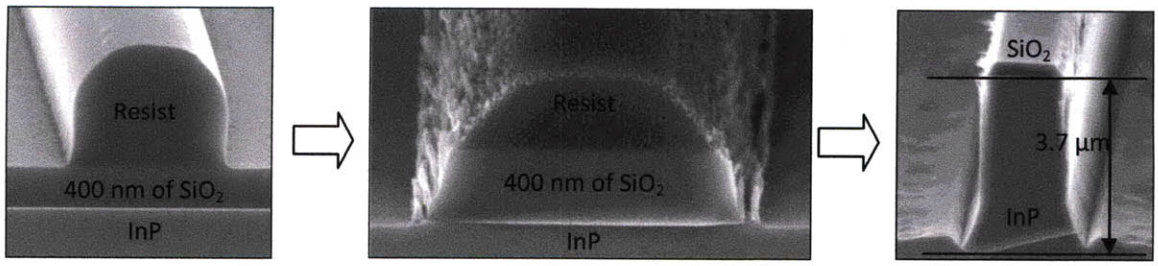
	Recipe 1	Recipe 2	Recipe 3	Recipe 4	Recipe 5	Recipe 6	
Gas (15 sccm)	**CF_4**	**CF_4**	**CF_4**	**CHF_3**	**CHF_3**	**CHF_3**	**CF_4**
Control Parameter	DC Bias	RF Power	DC Bias	RF Power	DC Bias	DC Bias	DC Bias
Set Point	50 V	200 W	200 V	450 W	200 V	200 V	200 V
Pressure	10 mTorr	10 mTorr	10 mTorr	10 mTorr	10 mTorr	10 mTorr	10 mTorr
Glass Slide	Yes	No	No	Yes	No	No	
Measured Param.	250 W	400 V	65-100W	300 V	80-100W	80-100W	65-100W

The SiO_2 was initially patterned using recipe #1 and a photoresist etch mask. However poor etching results mandated the need for RIE process development. Several process alternatives were explored including replacing the soft polymer mask with a dielectric hardmask, reducing chamber power, and changing the plasma chemistry. All of these approaches are discussed in the following sections.

3.1.1 CF_4 Etching with a Photoresist Mask

Initial CF_4 etches utilizing recipe 1 in Table 3-1 showed significant damage to the photoresist and subsequent SiO_2 mask. Within the plasma the fluorine ions are stripped from the fluorocarbon molecule. These ions diffuse to the silicon dioxide surface, where they form a protective layer that slows product desorption. This fluorine layer is removed as volatile SiF_4 after energy is added to the system through ion bombardment. The carbon on the surface of the wafer bonds with the oxygen in the dielectric to the form CO, CO_2, and COF_2 which readily desorbs back into the plasma and is removed with the gas flow. Oxygen in the substrate provides a radical element for the carbon to bind to preventing the consumption of fluorine ions as CF_3 and CF_4.**[46]**

Recipe 1 from Table 3-1 uses CF_4 plasma with a 50V bias to etch SiO_2. The low bias produces low energy ions. In an attempt to increase SiO_2 etch rates the ion concentration for a given DC voltage was increased to by preventing the bottom plate from discharging through a grounding hole in the bottom plate of the etching chamber. The presence of the glass slide required powers of 250W to maintain a DC voltage of 50V within the chamber, causing a significant increase in the number of ions for physical etching. Every ion that struck the wafer damaged the photoresist and dielectric mask, however because of the low ion energy they did little damage. Only because of the excessive number of low energy ions was this recipe able to the etch the SiO_2 at a rate of 19nm/min. The constant bombardment of the low energy ions slowly damaged the resist generating a 'feathered' edge as seen in Figure 3-1B. When this mask was used for ICP RIE etching, the feathering along the SiO_2 hardmask was transferred to into the InP as was seen in Figure 2-3 and Figure 3-1C. The photoresist's inability to withstand etching generated a need to explore other etching masks and chemistries.



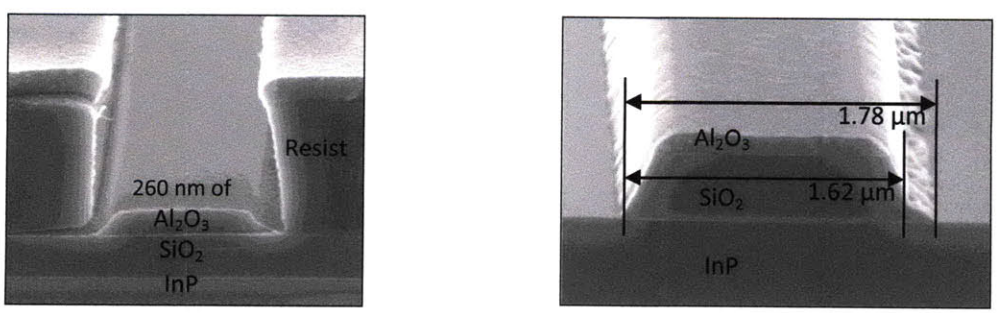
(A) Photolithography : AZ-5214E (B) RIE Etch using Recipe 1 (C) ICP RIE Profile after etching with the Taguchi Recipe

Figure 3-1: Evolution of the Feathered RIE Mask

One attempt to remove SiO_2 feathering was to create an etching environment where the SiO_2 is removed with fewer ions each with a higher ion energy. This reduces the number of ions required to remove the resist and decreases damage. This was accomplished by reducing the RF power to 200W and allowing the DC bias to float to 200V without the glass slide (Recipe 2). This recipe produced smooth side walls with an etch rate of 31 nm/min (Figure 3-4B). Although this process produced acceptable results, additional sidewall verticality was obtained by combining the resist strengthening properties of CHF_3 etching and the etch rates of CF_4.

3.1.2 CF_4 Etching with an Al_2O_3 Mask

Another approach to reduce mask damage was to replace the soft photoresist mask with 80 nm of aluminum oxide deposited by electron beam sputtering. The improved selectivity of $5_{SiO2} : 1_{Al2O3}$ verses $1_{SiO2} : 2_{Resist}$ prevented mask deterioration during etching, however any imperfections in the etch mask generated during lift-off were transferred to the mask. The selectivities were derived experimentally from calibrated scanning electron microscope images collected throughout process development.



(A) NR7-1500PY and Al_2O_3 after deposition (B) RIE Etch using Recipe 1

Figure 3-2: RIE Etch of SiO_2 using an Al_2O_3 Hardmask

During Al_2O_3 deposition, the dielectric material collected under the edge of the photoresist lift-off mask producing a thin layer of Al_2O_3 around the pattern (Figure 3-2A). Even with nearly vertical photoresist sidewalls, a thin layer of Al_2O_3 was able to accumulate along the edges generating ICP RIE linewidth variations of ±0.8µm, an unacceptable margin of error.

3.1.3 CHF_3 Etching with an Photoresist Mask

Soft photoresist can be used for fast high resolution pattern transfer when the resist is strengthen by the etch chemistry. RIE with CHF_3 generates a fluorine deficient plasma, due to the reduced number of available F ions and the easy generation of HF molecules. This chemistry also generates a passivation layer over the photoresist which prevents the chemical etching of the resist.[**48**] These factors cause a reduction in the photoresist etch rate from 50 nm/min to negligible generating a selectivity of $25_{SiO2} : 1_{Resist}$ in CHF_3 verses $1_{SiO2} : 2_{Resist}$ in a CF_4 plasma.

When etching SiO_2 in CHF_3 with in a high ion density/high ion energy environment, the ions will attempt to chemical remove the resist but will be thwarted by passivation layer. The constant physical bombardment will eventually remove a small section of the protective layer allowing chemical etching to take place in that region until the passivation layer is regrown. These moments of insolated chemical etching along the resist produce deep holes throughout the rest giving it a mangles look after etching as shown above in

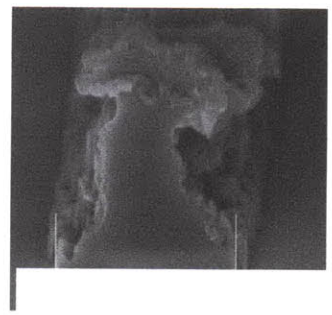


Figure 3-3: RIE device profile after a high power CHF_3 Etch (Recipe 4)

Figure 0-3. This misshaping of the resist will be transferred into the SiO_2 substrate producing large linewidth errors in the final device. When the RF power was reduced from 450W to 200W the photoresist remained intact. However the SiO_2 removal is significantly slowed by the lack of available fluorine ions for chemical etching. In response to this a combination CHF_3 / CF_4 etch recipe was developed which takes advantage of the protective aspects of CHF_3 etching and the high etch rate of CF_4.

3.1.4 CHF_3 / CF_4 Etch Results

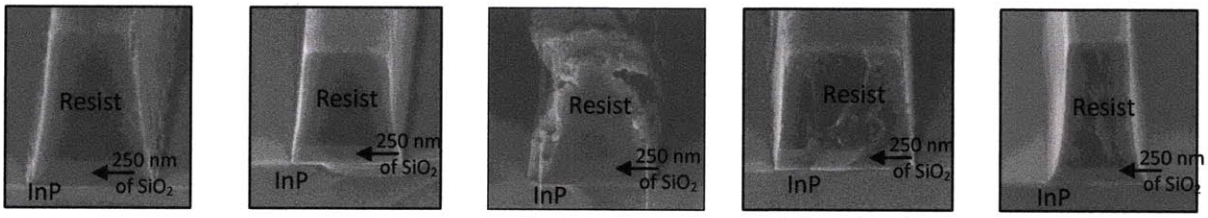
Optimal linewidth transfer occurred during CHF_3 / CF_4 etches. The first half of the recipe allows CHF_3 to deposit a protective polymer on photoresist but not the SiO_2. [**49**] The second stage of etching adds fluorine to the chamber from the CF_4 plasma, which increases chemical etching within the chamber. Recipe 6 in has a $1_{Resist} : 2_{SiO2}$ etch selectivity with an SiO_2 etch rate of 22 nm/min. The process produces a more vertical sidewall when using the glass slide as shown in Figure 3-4D because of the increased etching rate, with minimal damage to resist.

3.2 Fabrication Results

RIE process development investigated the SiO_2 etch profiles generated by CF_4, CHF_3, and CHF_3/CF_4 plasmas. A summary of all the etch rates derived experimentally from the SEM images during process development recipe is summarized in Table 3-2 and the resulting profiles shown in Table 3-2.

Table 3-2: RIE Etching Rates

	Recipe 1 GS	Recipe 2	Recipe 3	Recipe 4 GS	Recipe 6 GS	Recipe 6
Resist	46 nm/min	57 nm/min	19 nm/min	0 nm/min	13 nm/min	14 nm/min
SiO_2	19 nm/min	31 nm/min	10 nm/min	24 nm/min	22 nm/min	10 nm/min
Al_2O_3	4 nm/min	-	-	-	-	-
Al_2O_3 & SiO_2	31 nm/min	-	-	-	-	19 nm/min
Ti & SiO_2	-	-	-	-	-	13 nm/min



(A) Recipe 1: With Glass Slide (B) Recipe 2 (C) Recipe 4: With Glass Slide (D) Recipe 6 : With Glass Slide (E) Recipe 6

Figure 3-4: Resist Profiles after RIE Etching

Even during the times of greatest damage to the SiO_2 the linewidth error when compared to the shadow mask was only ±600nm, dropping to ±250nm with the final process as seen in Figure 3-5.

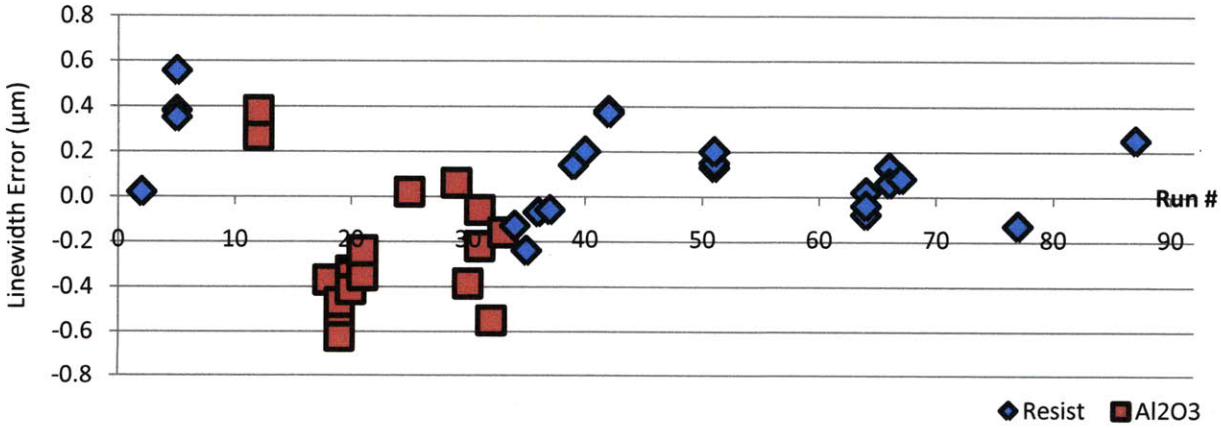


Figure 3-5: RIE Linewidth Error compared to the Shadow Mask

The total linewidth errors observed at this stage fabrication was comparable to the error observed after ICP RIE etching and only ±50nm larger than the errors generated during photolithography. This points to the strength of the fabrication process developed for ICP RIE and RIE systems.

The SiO_2 hardmasks discussed above were fabricated in a CHF_3/CF_4 RIE etching chamber in the Nanostructure Laboratory (NSL) at MIT. The process was selected because of its ability to obtain etch rates of 22 nm/min while retaining the dimensions of the photoresist mask to ±50nm. A detailed overview of this fabrication process is provided in the following section.

3.3 Fabrication Process Overview for RIE Etching of SiO_2

Once the pattern is successfully established in resist it must be transferred to SiO_2 to generate a hardmask for ICP etching of the epitaxial wafer. The etch depth of 250nm does not necessitate an inductively coupled system allowing the SiO_2 to be etched in a readily available RIE tool. The samples were etched in the Plasmatherm 790 series located in the Nano Structure Laboratory (NSL) at MIT. It is small parallel plate reactor ion etcher used of oxygen and fluorine etches. Both CF_4 and CHF_3 etch chemistries were tested, resulting in an etch profiles discussed in Section 3.2.

Before etching the RIE chamber is cleaned in high power, high pressure oxygen etch to remove contaminants left over from previous etches. The samples are then placed in the center of the RIE plate and the system is pumped down to vacuum. The samples are then left to vacuum cure within the chamber for 10-20 minutes to pull remaining solvents from the polymer and harden the resist. Etching begins by flowing gases into the chamber for 2 mins at the correct chamber pressure but no power to prevent sparking the plasma. Gas flow before etching ensures the gas lines are primed and the chamber contains the optimal gas chemistry. The plasma is sparked with a high DC bias voltage of 200 V for 5 seconds, before the chamber settles to the etch parameters outline in Table 3-3.

Table 3-3: Oxide Recipe

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch	Step 4: Flow Gases	Step 5: Spark Plasma	Step 6: Etch
Time:	30 secs	5 secs	6 min	1 min	5 sec	7 min
Gas (sccm):	CHF_3 : 15	CHF_3 : 15	CHF_3 : 15	CF_4 : 15	CF_4 : 15	CF_4 : 15
DC Voltage:	0 V	200 V	200 V	0	200 V	200 V
Pressure:	15 mTorr	15 mTorr	10 mTorr	15 mTorr	15 mTorr	10 mTorr

The final recipe is a two stage plasma which protects the photoresist with a passivation polymer during the CHF_3, followed by an aggressive etching stage due to the addition of radical fluorine ions from the CF_4 plasma. This recipe etches the SiO_2 at a rate of 10 nm/min, with selectivity of 1:1 without the glass slide and 2:1 (SiO_2: Resist) with it. The process is repeated and then the chamber is evacuated. Optical inspection of the SiO_2 color can be used to determine the remaining mask thickness. If all of the SiO_2 is removed the wafer will appear grey, any color between the resist features indicates that the highly reflective dielectric material is still present on the wafer. Any remaining SiO_2 can be removed with a short CF_4 etch. Although over etching does not damage the InP substrate it will increase the profile slope of the SiO_2 as the photoresist continues to be consumed by additional etching. The sidewall angle and linewidth are measured with a scanning electron microscope (SEM).

After etching, the photoresist is removed from the sample in an acetone bath and oxygen plasma. The samples are submerged in an acetone for 10 minutes, then agitated in an ultra-sonic tub of water for 30 seconds. This process will shake free any stuck on resist not dissolved by the acetone. To ensure a clean surface the wafers are then placed in an oxygen plasma asher for 15 minutes to remove any

organic remnants. Over ashing the wafers will not damage the device, and complete resist removal is critical to the repeatable ICP RIE results.

In this chapter we showed that development of RIE etch recipe which retains the photoresist dimensions is critical to maintaining the pattern fidelity throughout processing. By following the procedure outlined in Section 3.3, we were able to successful transfer the photoresist pattern into the SiO_2 hardmasks with a dimensional error of ±50nm. In the next chapter we will explore the fabrication process developed for obtaining photoresist profiles with nearly vertical sidewalls and linewidth errors of ±200nm.

4 Contact Photolithography

This chapter provides an overview of the photolithography process used to generate photonic integrated devices with linewidth errors of ±200 nm. The process used in this chapter was optimized for AZ-5214E photoresist on 0.5 cm^2 chip of InP coated with 250 nm of SiO_2 exposed in a Karl Süss MA-6 contact lithography tool. Although this recipe originated in the work of Ryan Williams in the Integrated Photonics Devices and Materials Group at MIT, every process parameter was examined and optimized to generate a fabrication recipe producing resist patterns within our range of acceptable error. Section 4.1 examines the recipe optimization process emphasizing the effect of resist thickness, exposure time, and mask contact on the resist profile. Section 4.2 provides detailed overview of the lithographic process highlighting the processing steps used to ensure flush contact between the mask and the resist is provide provided in.

Additionally, a bi-layer hardmask of Al_2O_3 and SiO_2 was explored as ICP RIE mask alternative. Unlike single layer masks, the aluminum oxide was defined through a lift-off process requiring a negative resist profile and material deposition. Two lithography processes were developed producing trenches with a repeatable linewidth error of ±350nm. An overview of the lithography process for liftoff and the Al_2O_3 deposition is provided in Appendix C.

4.1 Process Development

Successful pattern transfer is dependent on the interplay of all stages of the lithographic process. In this section we examine the effects of the 4 major processing steps – spin coating, prebake, exposure, and development – on the photolithographic linewidth error. Section 4.1 is an examination of positive photoresist, with a focus on the techniques used to reduce variations in thickness between the mask and the substrate. This is followed by an examination of exposure dose and develop time on sidewall verticality and linewidth error. By tracking the pattern fidelity under the influence of the lithographic parameter variation, we were able to derive the recipe parameters used for the fabrication InP photonic devices.

4.1.1 Resist

Although several positive tone photoresists exist on the market our research focused around the resists provided by MIT in the MTL facility namely Clariant AZ-5214E and OCG 825-20. AZ-5214E is a chemically amplified image reversal resist, which means it will be removed from the exposed regions of the wafer with less power to produce an undercut profile due to the increased resist sensitivity. The resist is

comprised of a novolak resin and a diazonnaphthoquinone (DNQ) photoactive compound. [**14**] The DNQ changes the polarity for the resist causing it to be hyrodphobic and resisting development.[**50**] The exposure of resist with wavelengths between 320-420nm causes the DNQ to breaks down allowing the novolak resin to be removed in a liquid developer. [**51**] The Karl Süss MA-6 has been adjusted to output a narrow exposure band around 365 nm (i-line), making AZ-5214E a good fit for lithographic processing on that tool. The drawback of the resist being an image reversal can be negated by removing a series of bakes and flood exposures from the suggested processing recipe. OCG 825-20 is a thin positive tone resist designed for exposure at 436 nm. Although OCG was able to produce thinner resist layers, AZ-5214E was selected because of its repeatable results, sensitivity at 365 nm, and easy removal after fluorine etching.

Photoresist is uniformly spread across a wafer by spin coating, which utilizes the equilibrium of frictional and centrifugal forces to produce repeatable resist thicknesses. Using calibration data like the set shown in Figure 4-1 one can select the proper thickness for a given fabrication by simply adjusting the spin speed. The equilibrium point is achieved in the first few seconds of spin coating. The additional 30 seconds of spin coating is used to evaporate solvents from the resist causing it to solidify on the wafer.

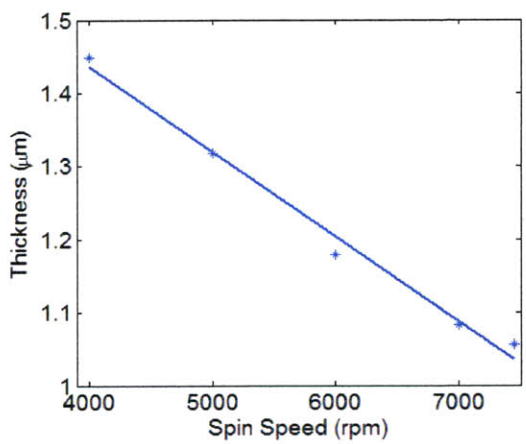
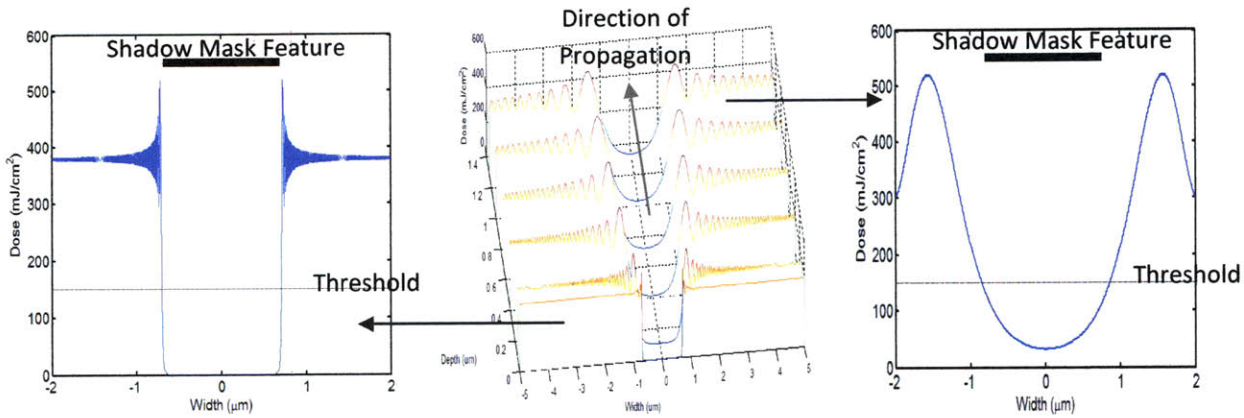


Figure 4-1: AZ-5214E Spin Rate

1.2 - 1.4 µm of AZ-5214E are used in literature in order to generate thick resist for improve lift-off. [**21**][**52**] [**53**] This thickness allows for a significant expansion of the exposure envelope as it passes through the resist. Consider Figure 4-2B, as the light propagates from the shadow masking into the resist is expands according to near field diffraction theory exposing the resist with a different dose profile at the top and bottom of the resist.



(A) Dose Profile at the top of the Resist: z = 1 nm

(B) Dose Profile evolution through the 1.4 µm of resist

(C) Dose Profile at the bottom of the Resist z = 1.4 µm

Figure 4-2: Dose Profile through the Resist

Recall from Chapter 1 that feature widths are defined by the intersection of dose envelope and threshold, thus an expansion of the exposure envelope within the resist can easily generate sloped sidewalls. Optimal pattern transfer during etching occurs with vertical resist profiles. Thin resists prevent dose profile expansion and are ideal for tight dimensional control. Unfortunately the spinner available in MIT's TRL cleanroom has intermittent motor functions at spin rates above 4000 rpms, preventing the us from thinning the resist to improve the profile.

The expansion of the dose profile is the source of the thickness induced linewidth error. An additional 20nm between the mask and the substrate allows the profile to expand an additional 10nm assuming an initial thickness of 1.4 µm. In the next section we will examine the two major sources of thickness variation, spin coater repeatability and poor contact of the photoresist and mask during exposure.

4.1.1.1 Resist Thickness

Over the course of process development the spin coater was used over 90 times generating a good baseline for spin coater repeatability. Figure 4-3 plots thickness error verses run number for spin speeds of 4000 rpms and 5000 rpms. Even at reasonable spin speeds the coater produced a ±0.2 µm variation in thickness.

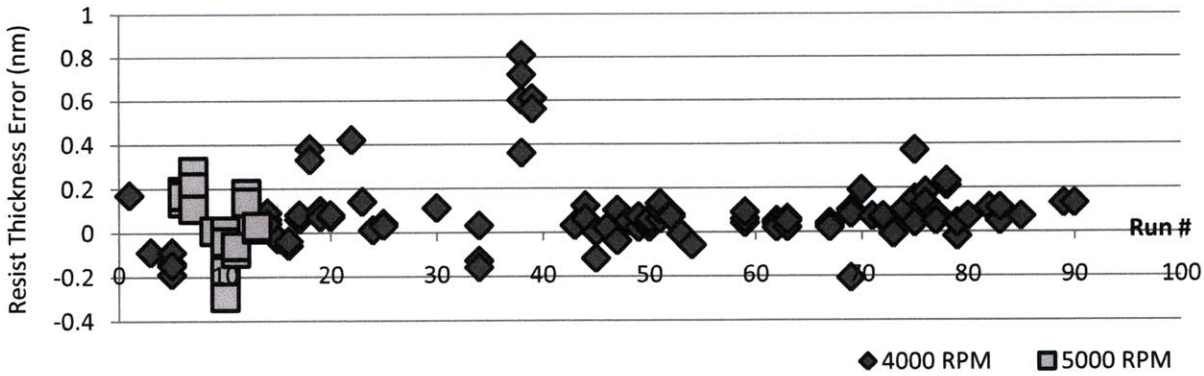


Figure 4-3: Resist Thickness Repeatability (Resist: AZ-5214E)

4.1.1.2 Contact

Any gaps between the photoresist and mask will generate linewidth errors according to near field diffraction theory. Assume a dust particle is caught between the mask and the resist. The resulting gap will change the dose profile at the top of the resist, ultimately effecting pattern transfer. Figure 4-4 is a model of the dose profile at the top of the resist with various amounts of gap between the mask and the the resist.

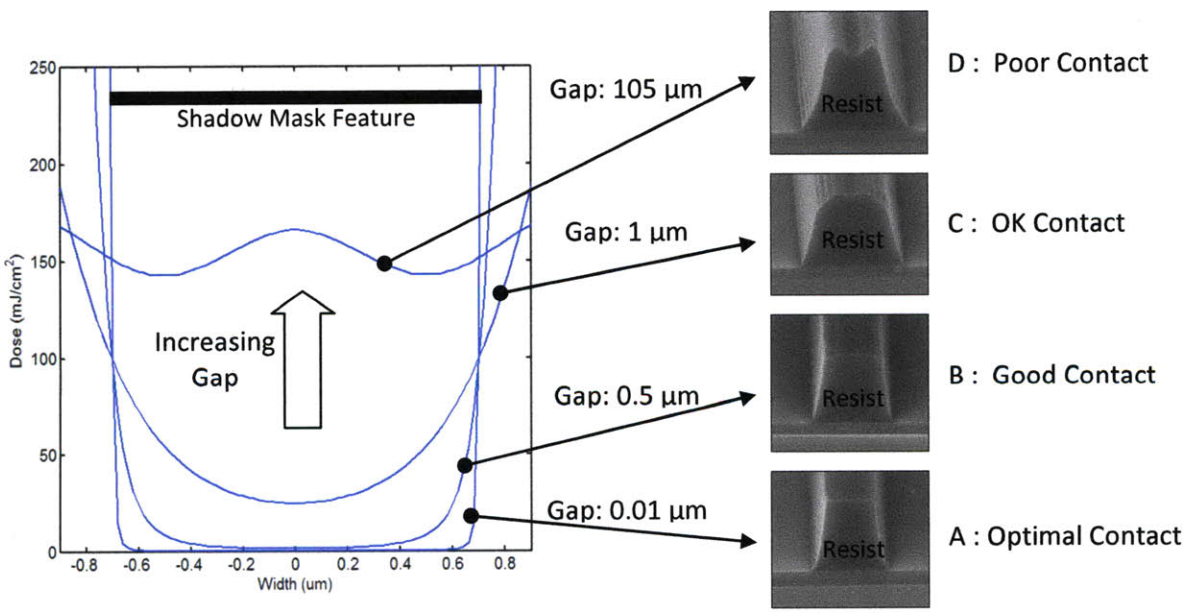
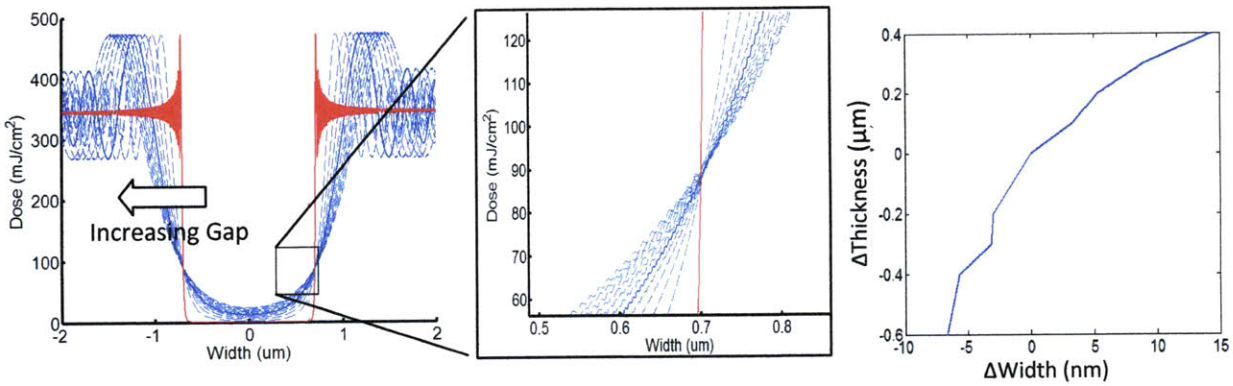


Figure 4-4: Effect of Gaps between the Mask and Resist on the Top of the Resist

The figures to the right of the theoretical model are AZ-5214E resist profiles on SiO_2 and InP. Profile A in Figure 4-4 occurs when there is intimate contact between the mask and the resist. The lack of exposure dose below the shadowed region prevents the breakdown of DNQ in that region generating the profiles

shown above. As the gap between the mask and the resist increases, the light begins to expose the resist under the feature generating the other profiles to the right of Figure 4-4.

Gaps between the mask and resist also effect the base of the profile. After propagating 1.4 µm to the substrate the exposure profile has already significantly expanded, thus an additional ±0.2 µm exposure depth simply broadens the profile rather than reshaping profile like was seen at the top of the resist. Figure 4-5C shows the theoretical variation in linewidth verses gap.



(A) Dose Profile with Expanding Gap Thickness

(B) Zoomed Region of Figure5A

(C) ΔThickness vs ΔLinewdith

Figure 4-5: Effects of Gaps at the Base of the Resist

The effects of poor contact during exposure is summarized in Figure 4-6 which shows the measured linewidth error at the base of the resist profile with various contact. All linewidth were measured with a calibrated scanning electron microscope.

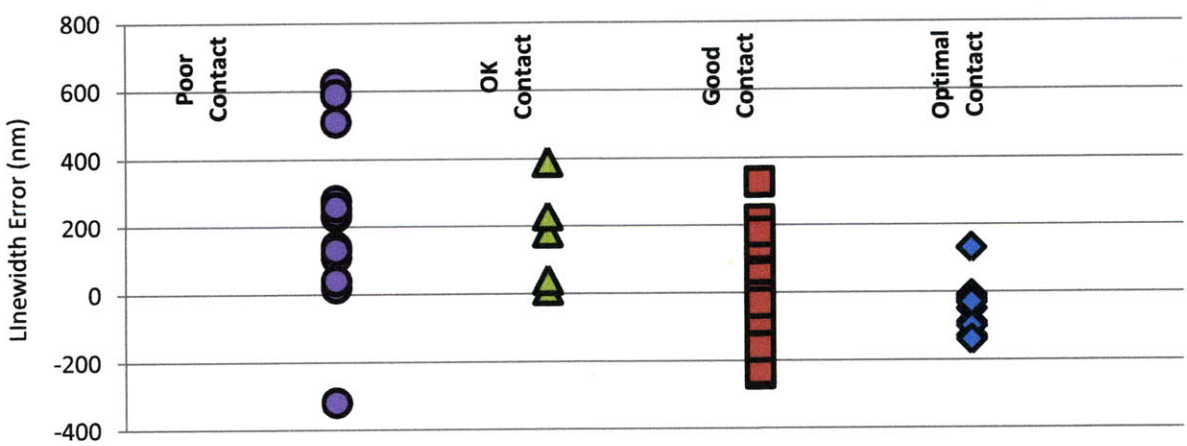


Figure 4-6: Photoresist Linewidth verse Contact

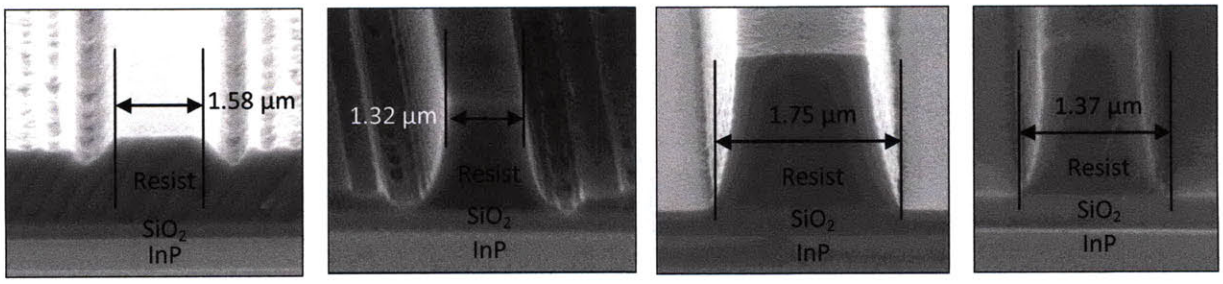
The maximum error of ±140nm verse ±600nm, highlights the importance of a minimal gap between the mask and resist for clean pattern transfer in contact optical lithography. The fabrication recipe detailed in Section 4.2 highlights critical handling techniques such as edge bead removal, particle prevention

before spin coating, and excess resist removal before exposure that generated repeatable flush contact during exposure.

4.1.2 Exposure

Every step of the lithographic process affects the resulting pattern. In this section we shall examine the most critical parameter of contact optical lithography, dose. Dose is defined as the optical intensity multiplied by the exposure time. Since intensity is determined by the mechanical assembly and light bulb within the tool, dose is controlled through exposure time.

Dose optimization was performed by processing several InP samples at once and exposing each wafer for a different length of time. Exposure times of less than 20 seconds did not provide sufficient dose to remove the resist as seen in Figure 4-7A and Figure 4-7B.



(A) 11 sec Exposure of a 1.4 µm feature

(B) 15 sec Exposure of a 1.4 µm feature

(C) 20 sec Exposure of a 1.4 µm feature

(D) 37 sec Exposure of a 1.4 µm feature

Figure 4-7: Resist Linewidth at Various Exposure Times

This indicates that the threshold of AZ-5214E as a positive resist lies between 15-20 seconds of exposure with a lamp intensity of 39 mW/cm^2. The exposure time was continually adjusted until the shadow mask pattern was transfer into the resist with a ±200nm linewidth error occurring at 35 seconds or a dose of 1365 mJ/cm^2. The results of the exposure optimization are shown in Figure 4-8.

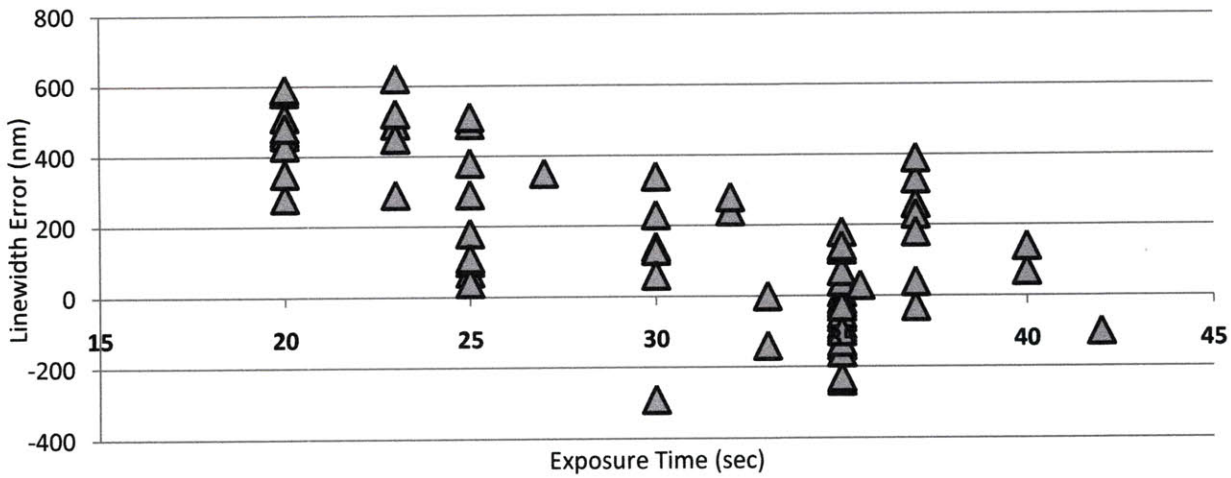


Figure 4-8: Linewidth Error verse Exposure Time

The photolithographic linewidth error is reduced to ±140nm when intimate contact was paired with a 35 second exposure as is shown in Figure 4-9.

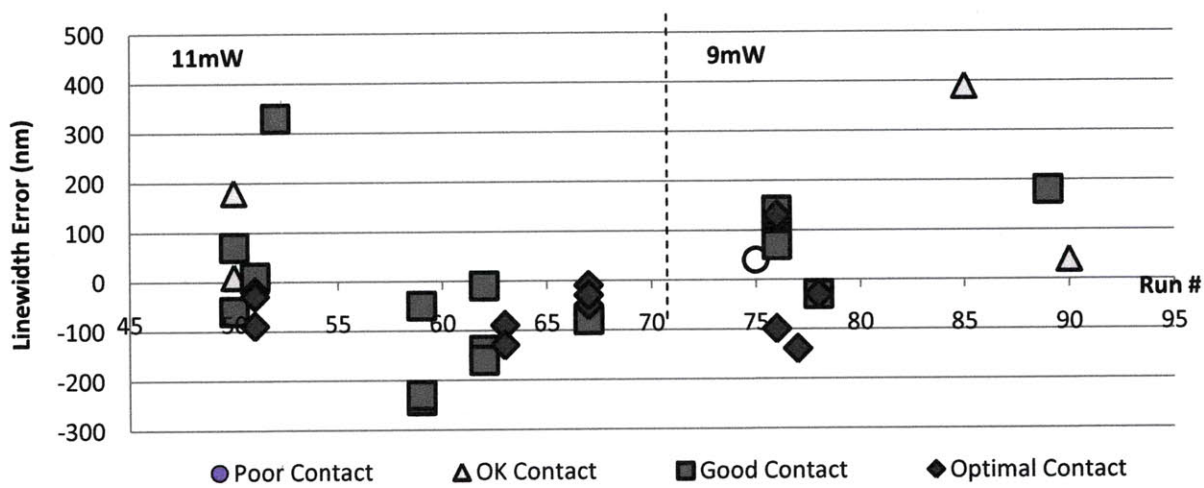


Figure 4-9: Linewidth Error of Samples with a 35 & 37 second Exposure Time

After initial development and processing of the IQE epitaxial wafer, the Karl Süss MA6 bulb intensity was adjusted from 11mW to 9mW, dropping the exposure energy to 32 mW/cm^2. To keep the dose constant from the previous process would require a 42 second exposure, however this produced poor results. Exposure times from 11 – 40 seconds were selected for retesting. After exposure and bake redevelopment, the new lithographic process had similar exposure times (37 seconds) for the 1.4µm of AZ-5214E on SiO_2. This verified the process developed for the IQE epitaxial wafer (run #68). Table 4-1 outlines the process parameters used for etching the IQE epitaxial wafer and the newly developed recipe used on the Lincoln Laboratory epitaxial wafers.

Table 4-1 : Lithographic Recipe for Epitaxial Wafers

Lithographic Parameters	IQE Epitaxial Wafer Runs #68	LL Epitaxial Wafer Runs #88-90
HMDS	Yes	Yes
Resist	AZ-5214E	AZ-5214E
Spin Rate	4000 rpm for 30 sec	4000 rpm for 30 sec
Bake Time	25 mins (oven)	20 mins (oven)
Exposure Dose	1365 mJ/cm^2	1184 mJ/cm^2
Exposure Time	35 secs	37 sec
Develop Time	90 sec	60 sec

Every device fabricated has a narrowing at the top of the resist as is seen in the SEMs in Figure 4-4 and Figure 4-7. Positive resist has a natural angle of about 85°, however my process produced an average sidewall angle of 79°, which implies an additional factor in the narrowing. An exploration of the prebake time was to done during process redevelopment in an attempt to straighten the sidewalls, but no correlation was found. Ridges along the edge of the resist are generated by the standing wave between the mask and the substrate. This back reflected light will continue to expose the resist and may have added to the narrowing. Another source of narrowing may be due to a greater evaporation of solvents from the top resist during spin coating in an open spin bowl. Fewer solvents will reduce the resist threshold in that region allowing for more material removal with the same dose.

4.1.3 Development

During exposure the polymer bonds within the resist are broken, leading to the easy removal of the exposed resist in AZ-422 developer solution. During early process development the resist was exposed with 98 mJ/cm^2 in the Electronic Visions EV620 exposure tool. This tool is a broadband source which exposes the resist with a wavelength range of 365-405nm.[**54**] This wavelength range corresponds to the AZ-5214E sensitivity as shown in Figure 4-10.

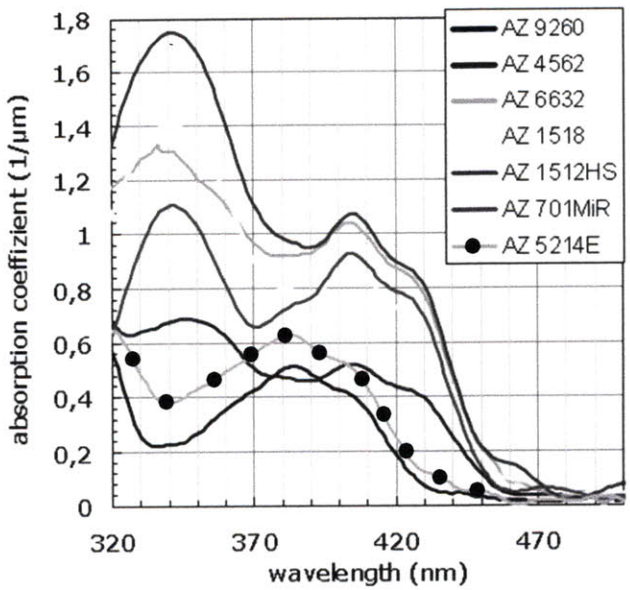
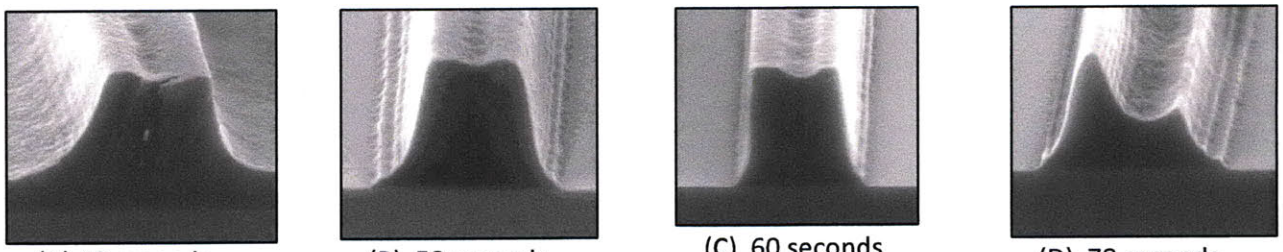


Figure 4-10: Photoresist Absorption[51]

Pattern fidelity of AZ-5214E exposed with this wavelength was highly dependent on development time, changing from the ideal profile to washed out one in 10 seconds as shown below in Figure 4-11. After increasing the dose to 1200 mJ/cm^2, the resist was able to retain its shape during development. The processes ability to maintain pattern fidelity independent of develop time makes the process developed above a strong candidate for photonic device fabrication.



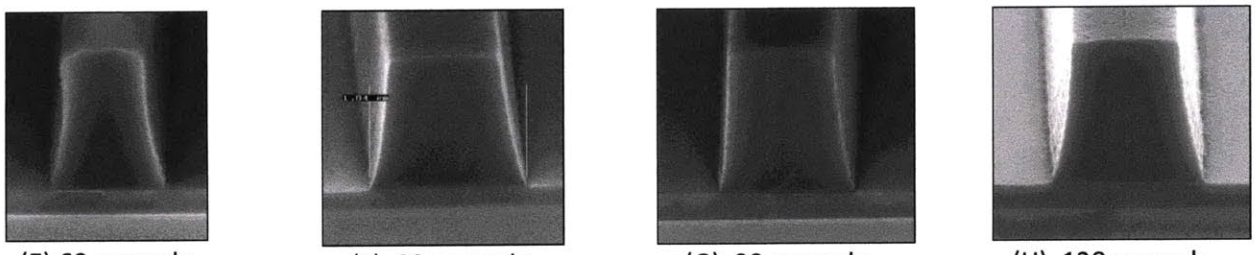
(A) 40 seconds
Top Width 1.4 µm

(B) 50 seconds
Base Width 2.03 µm

(C) 60 seconds
Base Width 1.6 µm

(D) 70 seconds
Base Width 1.9 µm

Figure 4-11: The effect of Develop Time on Resist Profile with an Exposure Dose of 98 mJ/cm^2



(E) 60 seconds
Base Width 1.19 µm

(F) 80 seconds
Base Width 1.84 µm

(G) 90 seconds
Base Width 1.47 µm

(H) 120 seconds
Base Width 1.75 µm

Figure 4-12: The effect of Develop Time on Resist Profile with an Exposure Dose of 1200 J/cm^2

During the process develop of the a photolithography recipe we found that good dimensional control is established by adjusting of the exposure dose and ensuring flush contact between the mask and the resist to minimize gaps. The difficulty of obtaining repeatable flush contact is so large that production houses spend billions of dollars on developing optical projection lithography tools with minimal diffraction error. In the next section we shall examine the techniques used during photolithographic processing to ensure optimal contact.

4.2 Fabrication Process of Contact Photolithography of InP Photonic Device

Photolithography is the foundation for all other processing. By developing a series of repeatable steps that produce features with dimensional errors of ±200nm we have set the ground work for fabricating InP Faraday rotator fabrication, and in this case miss the operational tolerances. This section provides a detailed overview of the processing steps and techniques used to produce the resist profiles shown above.

Photolithography begins by cleaning of all the wafers. When processing at MIT Lincoln Laboratories cleaning begins with a spray wash of soapy water to remove grease that may have collected on the surface of the wafer. This is followed by rinsing the sample with acetone, methanol, and isopropanol before blow drying in N_2 compressed air. Then samples are then baked for 2 minutes in a 120°C oven to remove any additional moisture on the surface. The clean samples are now ready processing.

Before application of photoresist the wafer are treated with hexamethyldisilazane (HMDS) to promote adhesion between the resist and SiO_2. Silicon dioxide is a hydrophilic material consisting of a series of exposed OH bonds that naturally repel the photoresist. A coating of HMDS removes the OH molecule and replaces them with an organic compound to increase adhesion. Vapor deposition of HMDS within an oven of 100°C-300°C allows for a greater percentage of OH replacement and is the optimal method for HMDS application.[**16**] In the MIT's TRL facilities samples are places into the HMDS oven and coated using recipe 5.

The photoresist is then uniformly applied to the treated wafers by spin coating. The wafer is placed on a vacuum turntable paying special attention to centering the wafer, this ensures uniform

revolutions. Once attached spray the wafer with compressed air to remove any particulates that may have accumulated on the surface since HMDS. Fresh AZ-5214E is dispensed for 3 seconds onto the wafer spinning at 500rpms. The spin speed is increased to 750rpms for 6 seconds, and then 4000rpms for 30 seconds. This allows for a gradual increase in acceleration and solvent evaporation. As the spin rate increases resist flies off the edge of the wafer until the frictional force between the resist and wafer matches the centrifugal force generated by the vacuum chuck rotation. The equilibrium point is reached within the first few seconds of spin coating. Thus the subsequent 30 seconds are used to accelerate the solvent evaporation from the resist causing it to become a solid. By adjusting the spin speed one can adjust the final thickness of the resist. For AZ-5214E 4000rpms results in 1.4 μm of resist. Although the resist could be thinned to 1μm at 7000rpms, the spinner does not produce consistent speeds above 4000rpms.

Surface tension at the edge of the wafer causes a build up of resist around the edge. This edge bead will generate a gap between the mask and resist, and must be removed to ensure good pattern transfer. The edge bead is carefully removed with an acetone soaked swab. Pointed swabs with small amounts of acetone should be used to minimize the amount of resist removed. To prevent damaging the 0.5 cm^2 sample while wiping the edge, I suggest leaving the sample attached to the chuck. When removing the sample gently wipe the back with the acetone swab. Don't worry about removing all the resist at this time, the back is cleaned again after the prebake.

Variations in the amount of residual solvent in the resist will effect the development rate of the resist at the end of the process. To ensure uniformity the resist is baked in a 90°C oven for 20 minutes. This allows all of the solvent within the resist to evaporate. The result is thinner less tacky polymer that is ready to be cleaned and exposed. After baking, one last check should be made for resist build up on the back and edges of the wafer. Placing the wafer face down in a watch glass allows for easy removal of the stuck on resist on the backside. One should still be careful of acetone seeping around the edges and removing the resist on the front face.

In lithography the contrast and threshold are determined by the properties of the resist, thus the profile is controlled by variations of the dose during exposure. The Karl Süss MA6 exposure tool was used with an i-line filter to produce an incoherent 9 mW intensity at 365nm. The dose is defined as intensity*time, was set at 1184 $J/cm^2$with an exposure time of 37 sec. A critical parameter in resist profile repeatability is flush contact with the mask. In the MA6 is this achieved with a clean mask and proper settings on the MA6. The shadow masked used during fabrication is a 15.2cm^2 (6 in^2) quartz mask from Compugraphics with chrome patterned waveguides and MMIs, as shown in Figure 4-13.

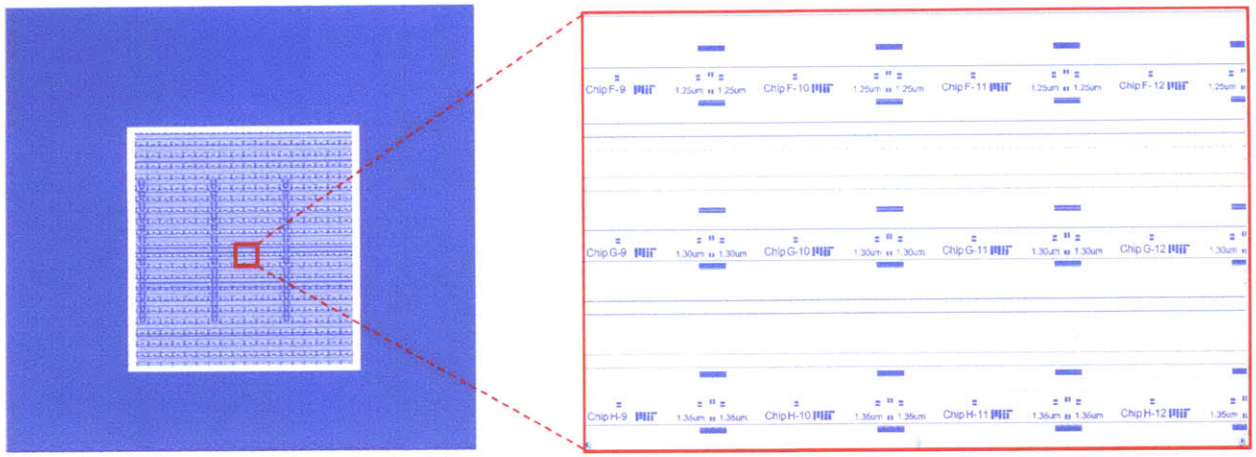


Figure 4-13: Shadow Mask

The mask is prepared for lithography by washing it. The mask is set vertically in a wafer holder allowing materials rinsed from the surface to fall into a collection jar below the mask. While flowing acetone over the surface, a wide swab is used to scrub the 2 cm^2 pattern region on both sides of the mask. Both sides are thoroughly rinsed with acetone, methanol, and isopropanol and then blown dry with N_2 with drying starting at the center of the mask to prevent streaking. The mask should be scrubbed and rinsed in AMI after every etch to remove particles and dried resist that adhered to the surface of the mask during the last exposure. Every 50 exposures the mask should be deep cleaned by soaking the pre-cleaned mask for 30 minutes in an organic solvent such as Microstrip.

The clean mask is placed in MA6 chrome side down and feed into the machine. The wafer is then loaded in the center of the vacuum chuck of the MA6 and 'Load Wafer' selected on the control panel. After automatic alignment, the tool allows for visual alignment of the mask and wafer. For our process the alignment stage, allows for rotation adjustment of the sample ensuring the waveguides are perpendicular the edges of the wafer. By commanding the tool to expose, the sample is automatically brought into intimate contact with the mask and then vacuum sealed to together by the mount according to the vacuum pressure defined by the user. To ensure flush contact the wafer stage is built on a pivot which allows it rotate until optimal contact is achieve detected by the wedge error compensation (WEC) sensor. The Karl Süss MA6 parameters used for exposure are shown Table 4-2 .

Table 4-2: Contact Exposure Parameters

Mode:	Vacuum Contact
Exposure Time:	37 sec
Alignment Gap:	10 µm
WEC Pressure:	1.0
Vacuum Chamber:	0.8
Pressure Vacuum:	10 sec
Full Vacuum:	10 sec
Vacuum Purge:	10 sec

After exposure the vacuum seal is released and the wafer stage lowered. At this point the sample may be removed.

The final stage in lithography is resist development. During this phase the exposed AZ-5214E is removed by gentle agitation while soaking in AZ 422 development solution. Agitation of the beaker during development increases the development rate. Over development of the sample produces features with reduced linewidth, rounded edges, and even removal of small features, while under development leaves exposed resist on the surface of the wafer. Most lithography processes have very small window of optimal development time ranging on the order of seconds, as was seen in Section 4.1.3. Fortunately the process outlined above is relatively invariant to develop time, a by product of the large exposure dose selected. All samples were developed in AZ 422 for 90 secs.

After development the features are inspected with a 40x microscope objective to ensure clearing of the resist and good shape to the features. Good lithography produces results like the ones shown in Figure 4-14 and Figure 4-15.

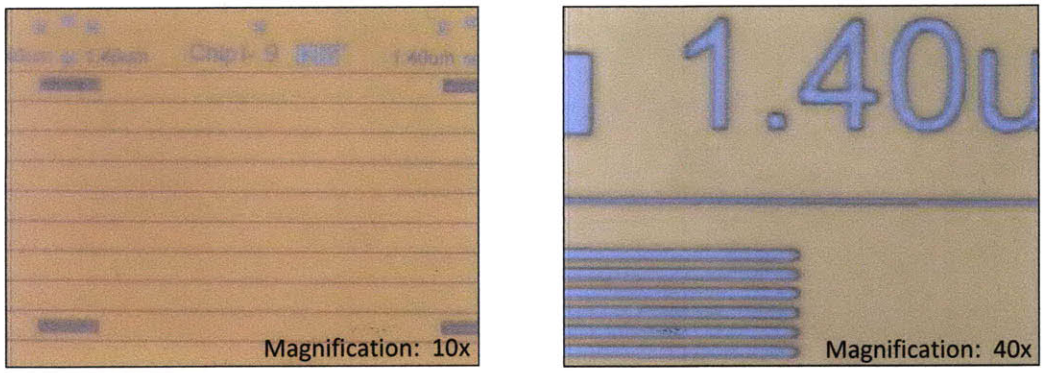


Figure 4-14: Microscope Inspection

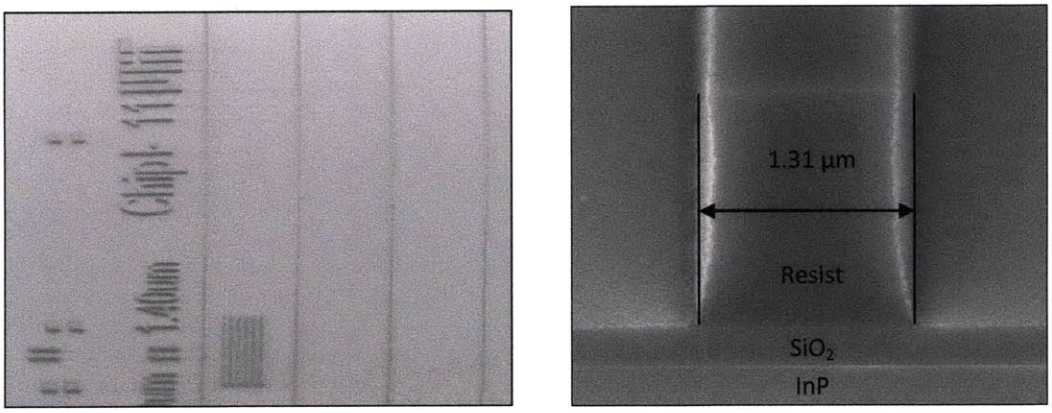


Figure 4-15: Scanning Electron Microscope (SEM) Inspection

Although approximate linewidths can be measured on a microscope, precision measurements are made with a scanning electron microscope (SEM). This tool uses a single stream of electrons to image the surface by collecting the reflected electrons and secondary electrons generated as the electrons strike

the surface of the wafer. The size and spread of the electrons and allow for a high resolution 3D image that is a valued addition to the inspection tool set. A SEM image of resist profile shown under the microscope in Figure 4-14 is shown in Figure 4-15 for comparison. Unfortunately due to working distant require to measure the full width of the device, SEM measurement precision of less than 10 nm was impossible.

At the conclusion of this chapter we have found that contact optical lithography in MIT's MTL was not able to produce 1.4μm ±65nm of linewidth error. Even in sample #67 (Figure 4-9), which showed the tightest range of linewidth error of -100nm we unable to meet the specification. The error established in this step of the fabrication was carrier forward in each successive step resulting in a device width error of ±250nm.

5 Testing of Faraday Rotators

In this chapter we examine the performance of InP Faraday rotators to validate the fabrication process developed in Chapter 2-4. In Chapter 1 we examined the effects of dimensional errors on device performance and found that geometrical birefringence within a waveguide will limit polarization rotation. Differences in the TE and TM propagation constants generated by the birefringence, will prevent 100% coupling between the modes as the polarization is rotated by the Faraday effect. Through simulations of the Faraday rotator performance under the influence of birefringence, we discovered a 20% reduction in polarization rotation with a birefringence of 1e-3. Thus only devices operating at the zero birefringence wavelength will produce maximum Faraday rotation.

In the following section we introduce a theoretical toolset to determine device birefringence and the Verdet coefficient from the TE and TM optical power of a Faraday rotator. Because the polarization rotation we are attempting to detect is on the order of 0.07° for a 1mm device in 0.2T magnetic field, it is important to construct an experimental setup which will remain stable over the course of testing. Section 5.2.1 describes the test setup used for InP device testing while highlighting the setup components which allow for accurate repeatable data collection. This discussion is followed by the test procedures and results for the Faraday rotators built of four the epitaxial wafers described below.

The Faraday rotators tested in Section 5.3 are constructed of four different epitaxial wafers described in Table 5-1 and depicted in Figure 5-1.

Table 5-1: Expitaxial Wafer used for Faraday Rotation Fabrication

Batch Number		Fe Concentration ($1/cm^3$)	InGaAsP Core Thickness(μm)	Upper InP Cladding Thickness (μm)	InGaAsP Core Q (λpeak)
MITT01-1-2 406-858B	IQE	5.00E+17	0.49	1.04	1.30 +/- 30nm
CCS-0562-A	LL	1.00E+17	0.60	1.00	1.45
CCS-0563-A	LL	undoped	0.60	1.00	1.45
CCS-0568-A	LL	undoped	0.50	1.00	1.34

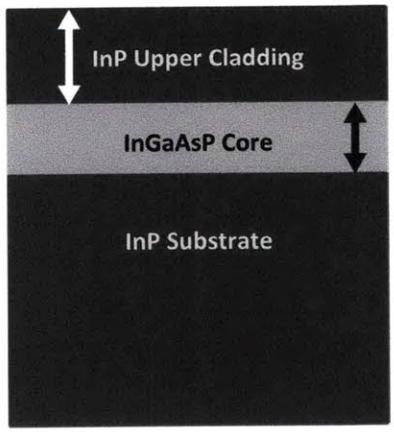


Figure 5-1: Epitaxial Stack

The iron doping in IQE and LL-0562 wafers was added to increase the Faraday rotation by improving the devices response to a magnetic field. The final two wafers have reduced the material bandgap in order to increase the strength of the optical interaction with the InGasAsP and thereby increase the Verdet coefficient.

Although the Verdet coefficient is a critical parameter for monolithic integration, optimization of Faraday rotation is not the focus of this thesis. Instead we shall examine the zero birefringence and loss measurement of each device. These characterization parameters highlight the effect of the fabrication process rather than the material selection. The zero birefringence wavelength can be used to back calculate the waveguide widths using an eigenmode solver such as BeamProp. This information is used to validate the linewidth error calculated with the scanning electron microscope (SEM) in Chapter 2-4. Loss measurements describe the effects of the core material as well as the sidewall roughness of the device. The results from this chapter provide a solid foundation to examine the success of the fabrication process developed in this thesis.

5.1 Theory

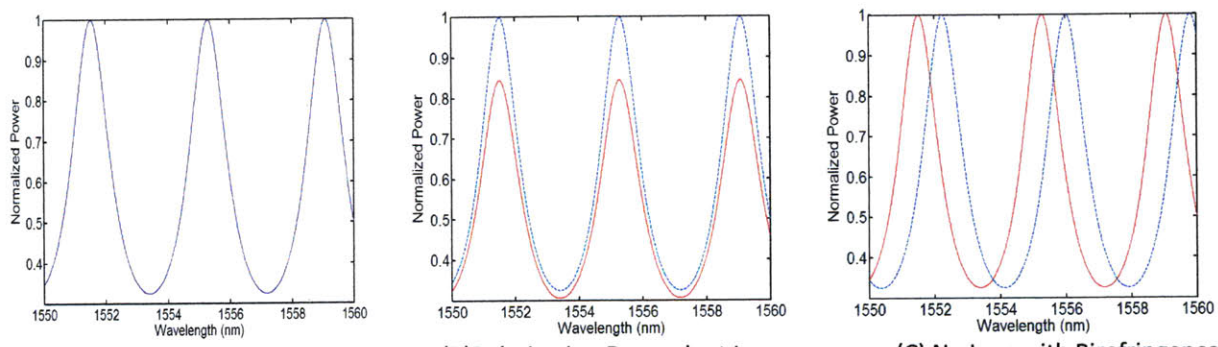
InP Faraday rotation is a result of the right hand circular and left hand circular polarizations propagating at different rates within the epitaxial material. By monitoring the total power in the TE and TM branches of the electric field we can derive the polarization rotation and zero birefringence. The reflective facets of the device establish a resonant cavity, which results in Fabry Perot fringes in the output power. This section will show how to determine the Figure of Merit for a Faraday rotator from Fabry Perot fringes in the output power of the TE and TM modes. The peak to trough height can be used to define loss, while the spacing between the peaks indicate birefringence and the group index.

Fabry Perot fringes in the power data that can be used to derive the device birefringence. The transmission maximums occurring at the resonant wavelength defined as[**11**]:

$$\lambda_{TE} = \frac{2\, n_{eff,TE}\, L}{m}$$

$$\lambda_{TM} = \frac{2\,(n_{eff,TE} + \Delta n)\, L}{m} \qquad 5.1$$

where m is the resonance order, Δn is the birefringence, and L is the length of the device. Consider Figure 5-2 which shows three theoretical resonant cavity outputs. These models assume the power is split evenly between the TE and TM fields and a device length of 1mm.



(A) No Loss and No Birefringence

(B)Polarization Dependent Loss and No Birefringence

(C) No Loss with Birefringence

Figure 5-2: Theoretical Fabry Perot Fringes

Figure 5-2A is shows a system with zero birefringence and no loss, resulting in the alignment of the resonant peaks in the TE and TM modes. The Fabry Perot profile is defined by the transmission and reflectivity at the facets, and the propagation loss in the cavity. Combining all these factors the output from the resonant cavity is defined as:

$$T = \left| \frac{t_{out} t_{in} e^{-ik_o L} e^{-\alpha/2L}}{1 - r_{out} r_{in} e^{-i2k_o L} e^{-\alpha L}} \right|^2 = 1 - R_{cavity} \qquad 5.2$$

where L is the length of the device, α is the loss, k_o is the wave vector in a vacuum. The term t_x is the electromagnetic surface transmission and r_x is the electromagnetic surface reflection at input and output facets, defined as

$$r = \frac{n_{eff} - n_{air}}{n_{eff} - n_{air}} \qquad t = \sqrt{1 - r^2} \qquad 5.3$$

where n_{eff} is the effective index of the device and n_{air} is the index of refraction for air(n_{air} =1). By taking the absolute value and squaring it we find the power reflectivity at the facet of the device:

$$R = \left| \frac{n_{eff} - n_{air}}{n_{eff} + n_{air}} \right|^2 \qquad 5.4$$

Loss is added to the TE mode in Figure 5-2B, reducing the peak to trough ratio from 2.8 to 2.4. This effect can be used to derive the waveguide loss (α) from the F number which is defined as[**11**],

$$F = \sqrt{\frac{P_{Peak}}{P_{Trough}}} = \frac{1 + Re^{-\alpha L}}{1 - Re^{-\alpha L}} \qquad 5.5$$

where R is the facet reflantance defined above. Rearranging the terms we can easily solve for the loss of in the waveguide directly from the Fabry Perot data.

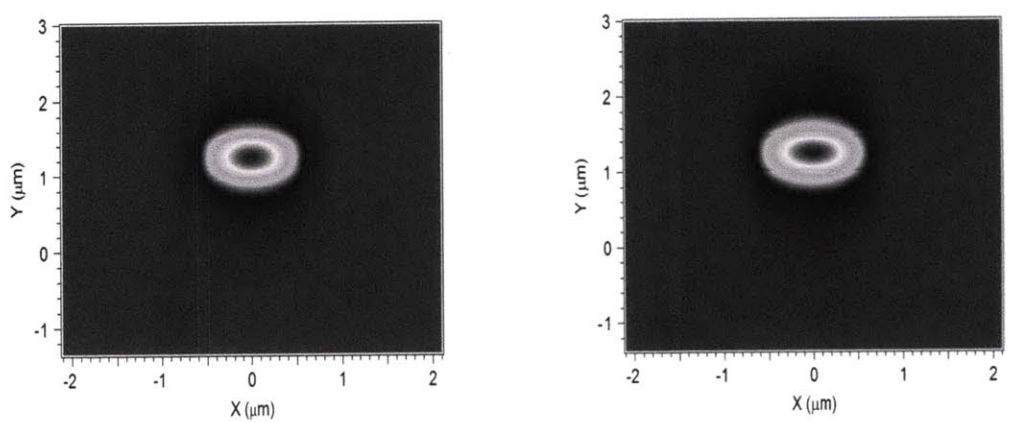
Figure 5-2C adds birefringence. This causes the TE and TM peaks to separate because of the larger effective index for one of the mode modes. Therefore we can solve for the device birefringence by solving for Δn in Equation 5.1,

$$\Delta n = n_{eff,TE}\left(\frac{\lambda_{TM}}{\lambda_{TE}} - 1\right) \qquad 5.6$$

The effective index in Equations 5.1, 5.4, and 5.6 is the refractive index acting on the light as it propagates within the material. It is determined by waveguide dimensions and the refraction indices of the core and cladding. In Chapter 1 we theoretically derived the effective index from the normalized waveguide equation (Appendix A). Here we shall determine it experimentally from the resonant order spacing for each mode. The wavelength dependence of the refractive index is described by the group index,

$$n_{group} = \frac{1}{2L}\frac{\lambda_m \lambda_{m+1}}{\lambda_{m+1} - \lambda_m} = n_{eff} - \lambda\frac{dn_{eff}}{d\lambda} \qquad 5.7$$

where m is the resonant order, λ is the operation wavelength, and L is the device length. Our devices consist of a InGaAsP (n_{core} = 3.22) core surrounded by InP (n_{clad} = 3.14). By simulating the waveguide mode within a 1.4μm device using 1D BeamProp, we generated a mode profiles like the one shown below in Figure CYXY from which we extracted the corresponding effective indices.



(A) TE Mode **(B) TM Mode**

Device Width: 1.32 μm, Wavelength: 1490 nm, Core Height: 0.5 μm, Cladding Height: 1 μm, InGaAsP Q: 1.31

Figure 5-3: Theoretical Modes

By solving for the TE and TM modes at a variety of wavelengths, we are able to derive the theoretical birefringence as a function of wavelength and device width for each epitaxial wafer.

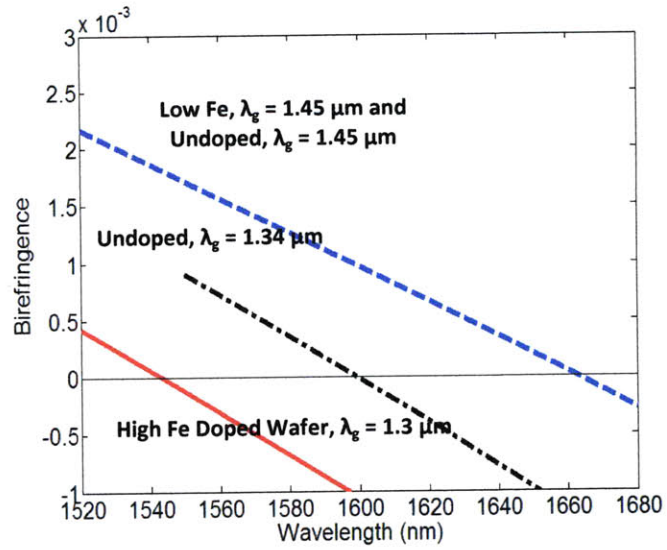
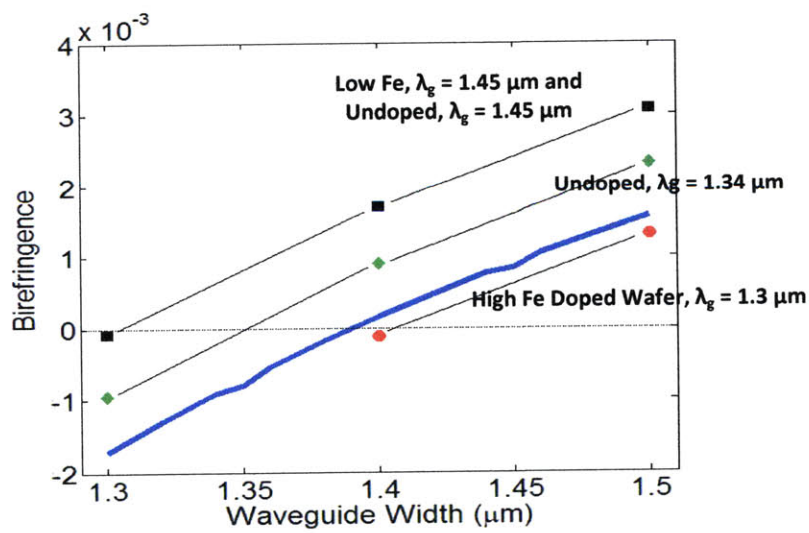


Figure 5-4: Theoretical Birefringence vs Wavelength within a 1.4µm Device

From this theoretical model we can extract the theoretical zero birefringence point for each epitaxal wafer.

The wavelength dependence of the birefringence appears in the raw data of the Faraday rotator as the distance between the TE and TM peaks expands or contracts across the wavelength range. Thus by sweeping across a range of wavelengths and examining the wavelength separation of the TE and TM modes, one can easily obtain the zero birefringence point. Knowing the zero birefringence wavelength, one can determine the device width from the theoretical model of the zero birefringence wavelength verses device width developed in BeamProp.



Design Parameters for Solid Line: Wavelength: 1550 nm, Core Height: 0.5 µm, Cladding Height: 1 µm, InGaAsP Q: 1.31

Figure 5-5: Variations in Device Width verse Birefringence at 1550 nm

A summary of the zero birefringence points for each epitaxial wafer is provided n Table 5-2.

Table 5-2: Theoretical Zero Birefringence Parameter for the Epitaxial Wafers

	Zero Birefringence Device Width at 1550 nm (Figure 5-5)	Zero Birefringence Wavelength for a 1.4μm Device(Figure 5-4)
High Fe doped Wafer, λ_g = 1.3 μm	1.41 μm	1542.8 nm
Undoped Wafer, λ_g = 1.34 μm	1.35 μm	1598.7 nm
Low Fe doped Wafer, λ_g = 1.45 μm and Undoped Wafer, λ_g = 1.45 μm	1.30 μm	1662.5 nm

5.1.1 Verdet Coefficient

The evolution of the electric field within the Faraday rotator is described by the mode coupling equation shown below[**11**]:

$$\frac{dA_{TE}}{dz} = -j\beta_{TE}A_{TE} + VA_{TM}$$
$$\frac{dA_{TM}}{dz} = -j\beta_{TM}A_{TM} - VA_{TE} \qquad 5.8$$

where A_X is the amplitude of the TE and TM electric fields. By solving the differential equations we can derive the rotation matrix for a Faraday rotator and in turn output electric field:

$$E_{out} = \begin{bmatrix} cos(\psi L) + j\frac{\Delta}{\psi}\sin(\psi L) & -\frac{V}{\psi}\sin(\psi L) \\ \frac{V}{\psi}\sin(\psi L) & cos(\psi L) - j\frac{\Delta}{\psi}\sin(\psi L) \end{bmatrix} E_{in} \qquad 5.9$$

where V is the Verdet coefficient, Δ is the differences in TE and TM propagation constants, and Ψ is a defined as:

$$\Delta = \frac{\beta_{TE} - \beta_{TM}}{2} = \frac{\Delta n\, k_o}{2} \qquad 5.10$$

$$\psi = \sqrt{\Delta^2 + V^2} \qquad 5.11$$

k_o is wavevector in a vacuum, and Δn is the birefringence. By knowing the input and output electric fields, one can solve for the Verdet coefficient of that device. To avoid having to solve the rotation

matrix, we use the differences in TE and TM output power to produces a simple expression containing the Verdet coefficient and the birefringence.

$$P_{TE} - P_{TM} = \frac{V}{\psi}\sin(2\psi L) \qquad 5.12$$

We solved for the Verdet coefficient (V) from the difference in the TE and TM output powers. The waveguide loss(α) was determined by the height of the Fabry Perot fringes in Equation 5.5. By dividing these two parameters we can solve for the Figure of Merit of the Faraday Rotator according to:

$$\frac{V}{\alpha} \qquad 5.13$$

5.2 Sample Preparation & Optical Testbed

Validation of dimensional control can be achieved during device testing through the experimental determination of the zero birefringence wavelength and loss. Before testing the wafers must be cleaved into 1mm waveguides with flat facets that allows light to be coupled into the device. Poor facet quality will render a device unusable, so it is important to develop a lapping a cleaving and process that will ensure good facets. After cleaving the devices are approximately 1mm long, 250μm - 80μm thick, and with 10 mm of other devices. The delicate samples are adhered to the edge of a glass slide to allow for easy handling and mounting in the optical testbed. In this section we shall examine the post processing step require to prepare the InP epitaxial wafers for testing, followed by an overview of the experimental testbed.

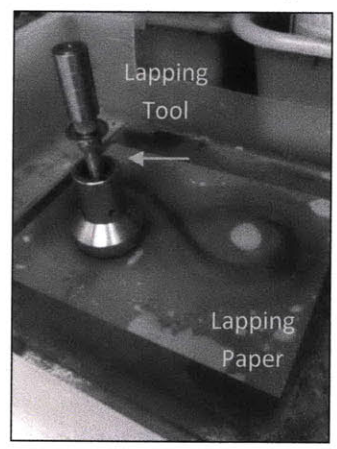


Figure 5-6: Lapping Setup

Light can only be coupled into flat clean facets obtained by cleaving the wafer along an atomic plane. To obtain good cleaves on both sides of the sample, the device should have half the thickness the desired device length. Thus a 1 mm waveguide requires a substrate thickness of 0.5 mm to ensure good facets. With an initial thickness of 0.44 mm, the wafers did not require thinning but were lapped to ensure good facets and allow 0.5mm device lengths.

Lapping is the process of mechanically sanding a wafer using a attachment and fine grit sandpaper. My samples were hand lapped using 12μm grit aluminum oxide lapping paper on a flat glass surface. The sample was attached to the epi side down to the lapping tool using crystal bond. After adhering the sample to the tool, we measured the thickness with a digital micrometer to establish a baseline thickness of ~0.45μm. Next the lapping paper is wetted with DI water and the lapping tool moved slowly across the paper in a figure 8. This should leave a dark traces of InP on the lapping paper as shown in Figure 0-6. After approximately 50 laps recheck the thickness and continue until the optimal thickness is achieved.

The sample can be removed by placing the sample holder onto 160°C hotplate to allow the crystal bond to melt. After removing from the tool with tweezers thoroughly rinse with acetone, methanol, and isopropanol, then blow dry with N_2.

Although the sample can be successful cleaved by hand, my sample were taken to MIT LL where they were cleaved with the Loomis LSD-100 automated tool generating devices of the proper length with good facets.

After cleaving the devices they are mounted to the edge of a glass slide with crystal bond. This is done holding the glass slide vertically on a 210° hotplate with two small metal blocks. After heating place a few small flakes of crystal bond on the edge of the sample and allow it to melt. With the tweezers thin the crystal bond to prevent it from piling on along the edges of the device. Now very carefully, with a clean pair of tweezers, grab the device length wise (don't touch the facet edges) and place it on the sample. Gently push the sample down into the glue and remove the glass slide and attached wafer from the hotplate. After drying remove excess crystal bond by rinsing the device with acetone, methanol, and isopropanol, then drying with compressed N_2.

5.2.1 Optical Testbed

Photonic device testing is performed by coupling light into the device and collecting the output power for analysis. The testing of integrated Faraday rotators requires power data from the TE and TM electromagnetic modes. From this data alone we can determine the loss, birefringence, and Verdet coefficient of the device.

The basic setup must consist of a tunable light source, a way of coupling light into the device, polarization splitter, and method for collecting the output of the two modes simultaneously. The laser source was an Agilent 81640A tunable laser with wavelength range of 1490-1610 nm. One meter of polarization maintaining (PM) optical fiber was connected to laser output and coupled to a meter of Nanonic polarization maintaining lens optical fiber. With a spot size of 2μm, the light was able to coupled into the device mode of ~1.4μm with minimal loss. PM fiber was used through the setup to minimize environmental polarization rotation.

Some setups use lens to fiber at both facets to reduce intensity loss during input and output coupling. To reduce the number of polarization sensitive elements, our testbed collected and collimated the diverging output light with a Mitutoyo 100x near IR microscope objective. From there the light passes to the polarization beam splitter, which separates the light into its TE and TM components. The optical power from each mode is collected at the HP 81521B free space optical power detectors. A schematic of the photonic testbed is provided in Figure 5-7.

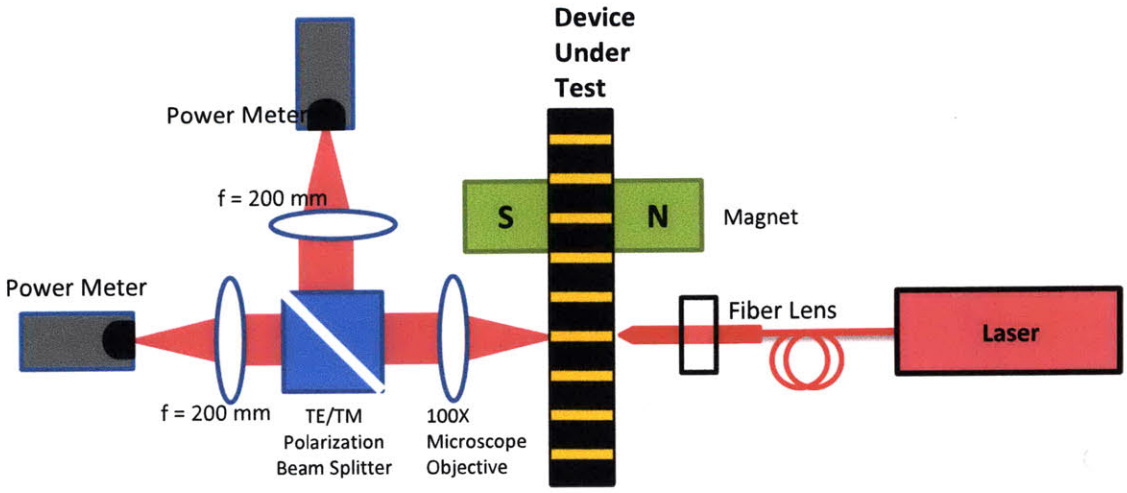


Figure 5-7: Test Setup

In an ideal optical testbed (without the device under test), the power and polarization within the setup should remain constant across the range of operating wavelength. The output polarization is defined by:

$$\theta = tan^{-1}\left(\frac{E_{TE}}{E_{TM}}\right) \qquad 5.14$$

where E_{TE} and E_{TM} are obtained from the optical power meters. The input polarization is set by the orientation of the optical fiber in the fiber mount. By rotating the fiber we were able to adjust the splitting from all TE, to all TM, to 50/50 splitting (or 45°).

Consider this example which sets the polarization to all TE. The polarization beam splitter is removed and a polarizer (set to 0°) is then placed in the beam path as shown in Figure 5-8.

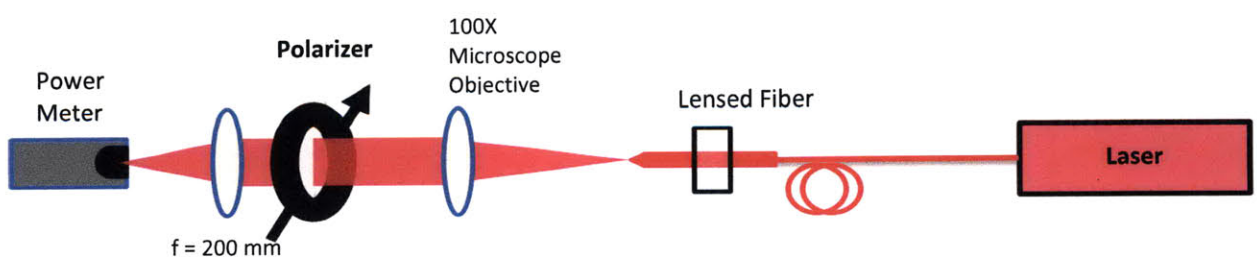


Figure 5-8: Polarization Alignment Testbed

By rotating the polarizer the output power, collected at the detector, will cycle from high to low as the polarizer blocks a portion of the light. To align the polarization to TE, maximize the power at the detector with the polarizer and note the new polarizer setting. Next rotate the optical fiber by the amount on the polarizer and set the polarizer back to 0°, this should result in the same maximized output power. To ensure proper alignment, adjust the polarizer for a second time. If maximum power is found at a polarization angle other than 0°, adjust the fiber accordingly. Once this is completed,

remove the polarizer and return the polarization beam splitter to its proper location in the test setup. One should observe minimal power at the TM power detector.

Although we were able to align the polarization and have it remain constant at a 1550nm, the wavelength sweep showed significant wavelength dependent polarization rotation and an increase in output power, as seen in the raw data of Figure 5-9 And the process data in Figure 5-10.

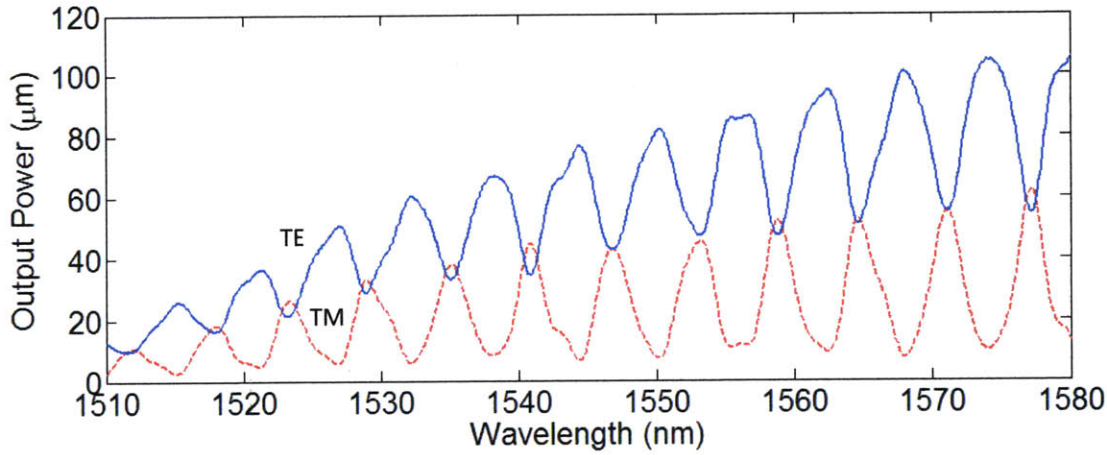


Figure 5-9: Lensed Fiber Output Power vs Wavelength

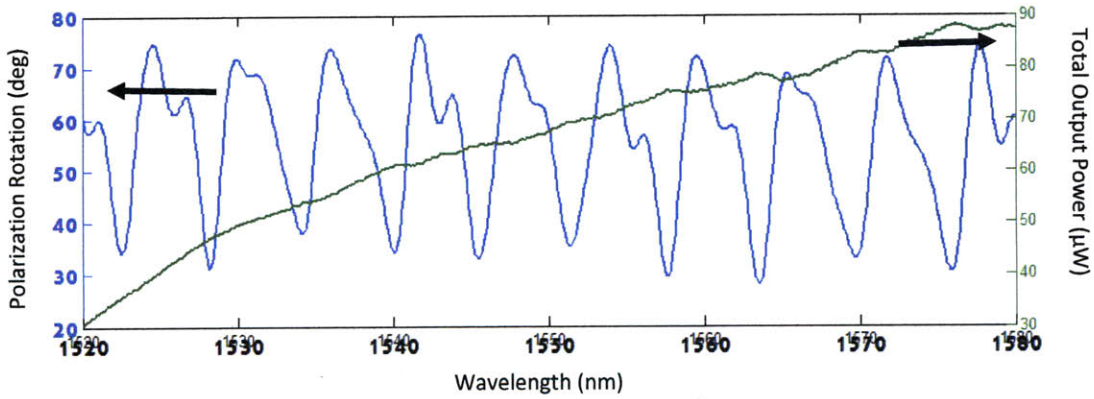


Figure 5-10: Fiber Output with polarization set to 45°

The increasing output power (solid line Figure 5-10) is a performance characteristic of the Agilent laser source and can be removed from the data as background effect. The more pressing concern in this the beating of the TE and TM modes over the wavelength range which indicates a wavelength dependent polarization rotation in the test setup.

Initial investigations into the source of the test setup polarization looked at the optical fiber. By replacing the lens fiber with another Nanonic PM lens optical fiber. By sweeping across the wavelength with this fiber we saw a reduction in the TE and TM beating but an increase in small signal noise that was on the order of the Fabry Perot spacing (Figure 5-11).

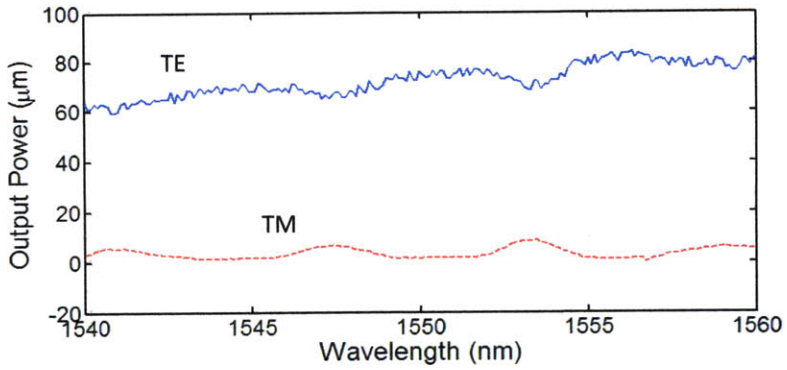


Figure 5-11: Output Power of the second Lensed PM Fiber

The high frequency noise prevented us from running data with the second fiber, but proved that optical fiber was the source of wavelength dependent rotation.

The polarization rotation seen in the baseline data may be a result of poor alignment between the polarization components. Suppression of the polarization rotation in polarization maintaining (PM) fiber is achieved by creating a large geometrical or stress induced birefringence in the fiber, which prevents coupling between the TE and TM modes. If the input light is perfectly aligned with the slow axis of the PM fiber then the input polarization will remain intact at the output. Poor performance in the PM fiber occurs when the light is scattered at the connectors and randomly coupled into the fast and slow axis of the of the fiber. Reasonable polarization extinction ratios of 20dB require a polarization axis alignment of ±6°.[**55**] I believe poor coupling alignment is the source of beating in our setup. However this is not a random alignment error that can be removed by twisting the fiber at the connector. Disconnection and reconnection of the optical fibers had no effect of the beating of the output data and still present (although drastically decreased) with a different fiber. These results imply a bigger polarization problem in the setup that could not be solved without extensive time. Areas that are still not investigated at the time of printing include ensuring the wavelength of operation for the polarization beam splitter matches the wavelength range of operation, obtaining PM lensed fiber from another vendor with better keying, and fusion splicing the connectors.

5.3 Waveguide Birefringence Measurement

Processing of raw output power begins by defining the peaks of the Fabry Perot fringes in the TE and TM data set. A Matlab algorithm (provided in Appendix E) is used to find the peaks and trough of the Fabry Perot fringes. To remove the error associated with the absolute peak not being located within raw data, a Gaussian is fit to the data ±5 points around the local maximum. The span was selected to generate the minimum error between the peak and the fit peak. Figure 5-12 shows a few fringes from TE output power, the circle marks the local maximum, while the diamond indicates the calculated maximum after the fitting to the curve.

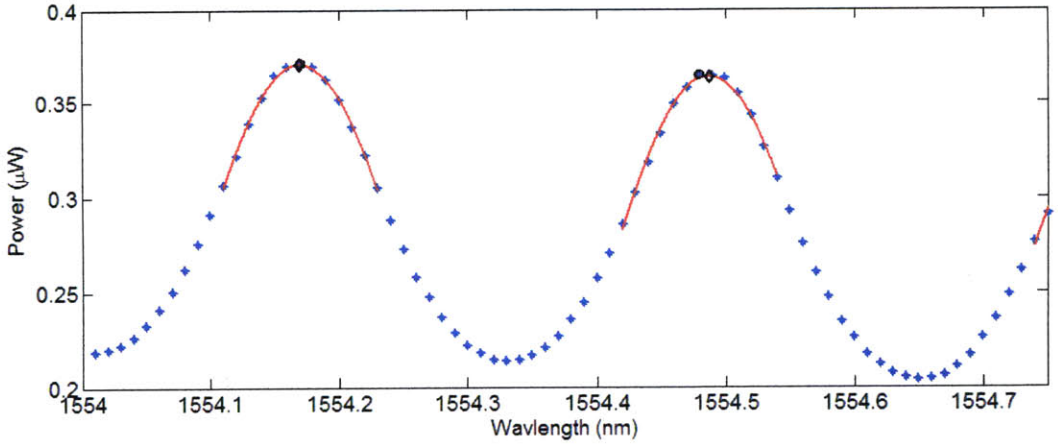


Figure 5-12: TE Output Power

The average wavelength difference between the in the calculated and measured peak is 24pm and the difference in power is 89nW.

The spacing of the Fabry Perot peaks is then used to calculate the group index for that device according to Equation 5.7. All the devices tested in this thesis were 1mm long. This measurement can be trusted because it was generated by an automated cleaving tool at MIT Lincoln Laboratories and verified by the dimensional markers on the mask. The average group index estimated from the peak to peak difference for a 1.3μm waveguide on an undoped wafer (λ_g=1.34μm) was 3.86 and 3.84 over the wavelength range of 1535-1540 nm for TE and TM respectively, these values match the theoretical curves shown Figure 5-13. Although the raw data in Figure 5-13 has a broad range around the theoretical, the average falls along the theoretical curve. The consist fit of average group index to the theoretical curve allowed us to assume the effective index as 3.2 for the TE and TM during testing.

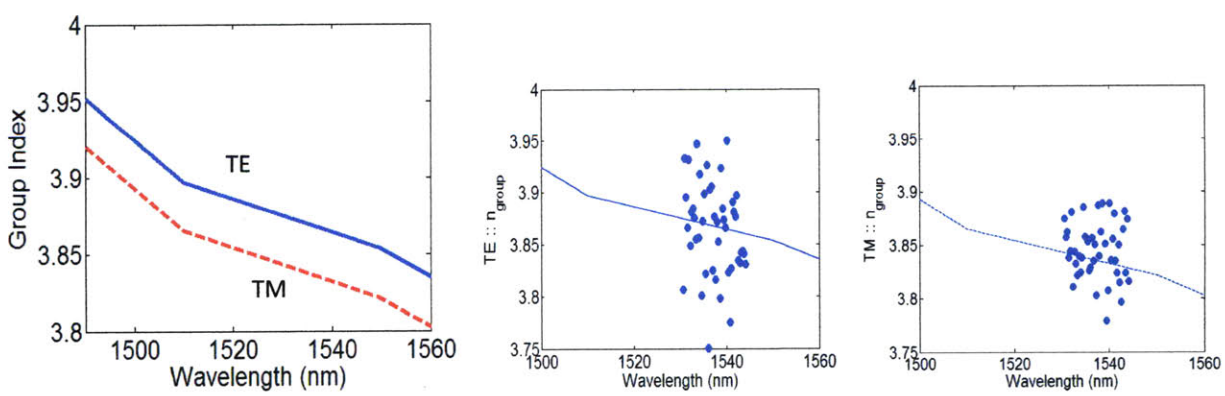


Figure 5-13: Group Index for a 1.3μm Waveguide on an undoped Epitaxial Wafer, λ_g=1.34μm

The low frequency oscillations of the output data, which track the intrinsic wavelength dependent rotation of the lens fiber, generate both an additive and multiplicative error. The peaks along the rise and fall of the fiber oscillations will be stretched to follow the power trend as seen in

Figure 5-14. This will corrupt the peak to trough ratio of the signals, generating unreliable loss measurements.

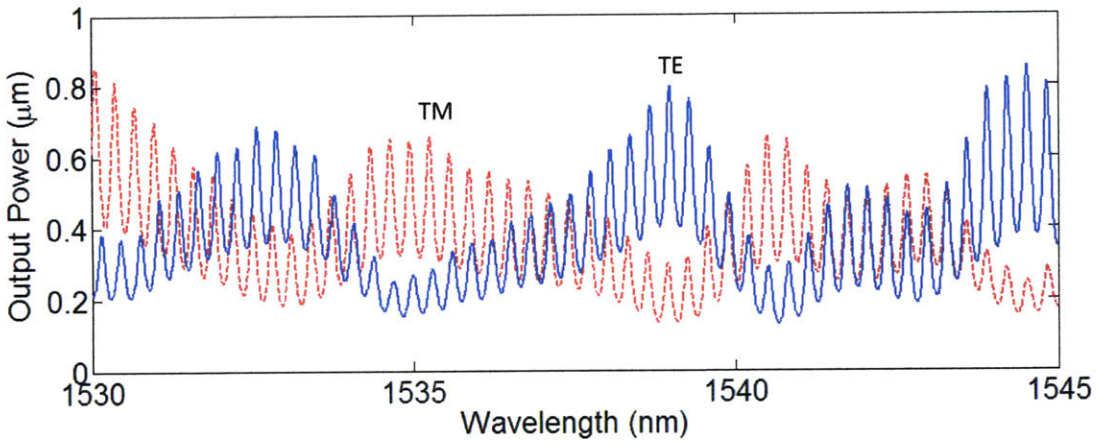


Figure 5-14: Raw Output Power for an undoped Epitaxial Wafer with λ_g=1.34μm

By considering the log of the output power, we observe the data with a uniform multiplicative error that simplifies the measurement of the peak to trough ratio for the device. Once again a Matlab algorithm was used to locate the local maximum and minimums of the raw data. Code was written to ensure the only peaks from successive resonant modes were used for the calculation. Analysis of the TE and TM Fabry Perot fringes in Figure 5-15 showed losses of 2.2 dB/cm and -1.2 dB/cm for the TE and TM modes respectively. The negative is a major testing concern that is discussed in more detail at the end of the chapter. The output power in dBm for the other epitaxial wafers is shown in Figure 5-16, Figure 5-17, and Figure 5-18. The presence of negative loss indicates and error in the calculation most likely due to the background oscillations in the data.

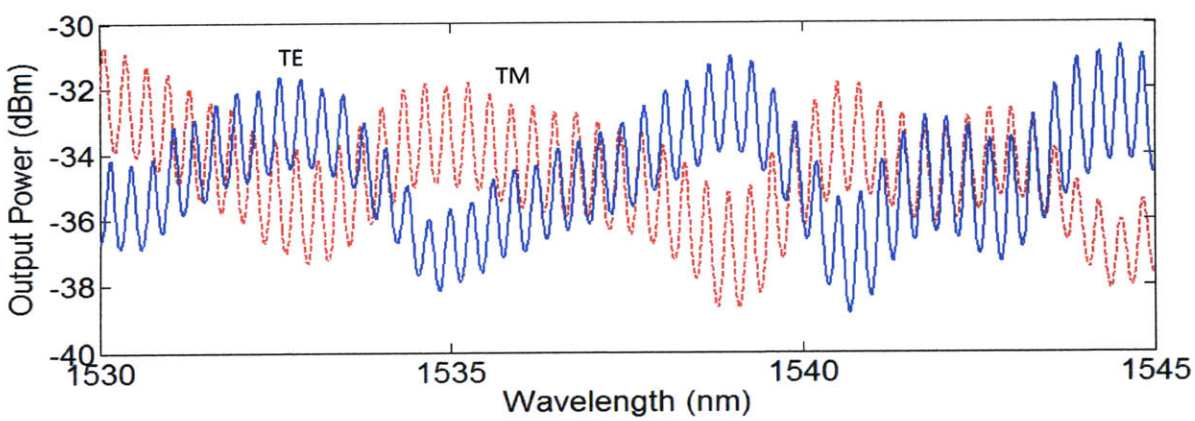


Figure 5-15: Output Power for an undoped Epitaxial Wafer with λ_g=1.34μm in dBm

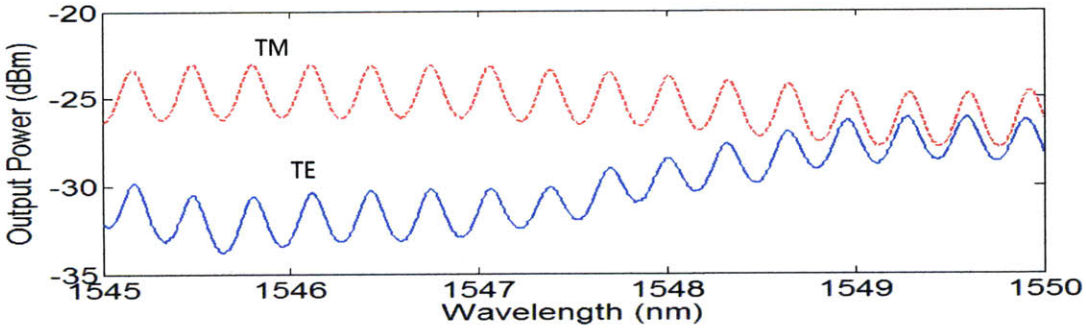


Figure 5-16: Output Power for a High Fe doped Epitaxial Wafer, λ_g=1.3μm in dBm

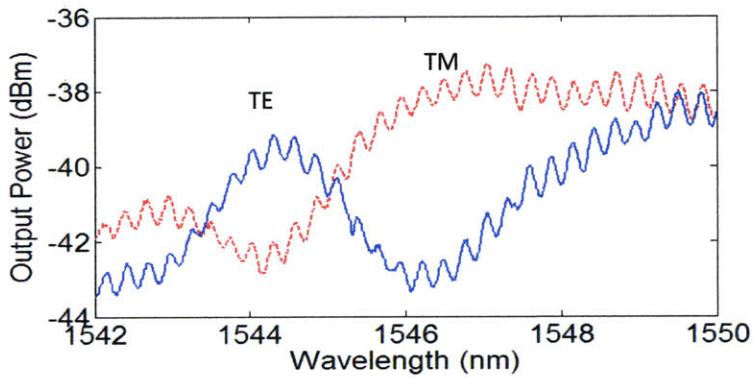


Figure 5-17: Output Power for a Low Fe doped Epitaxial Wafer, λ_g=1.45μm in dBm

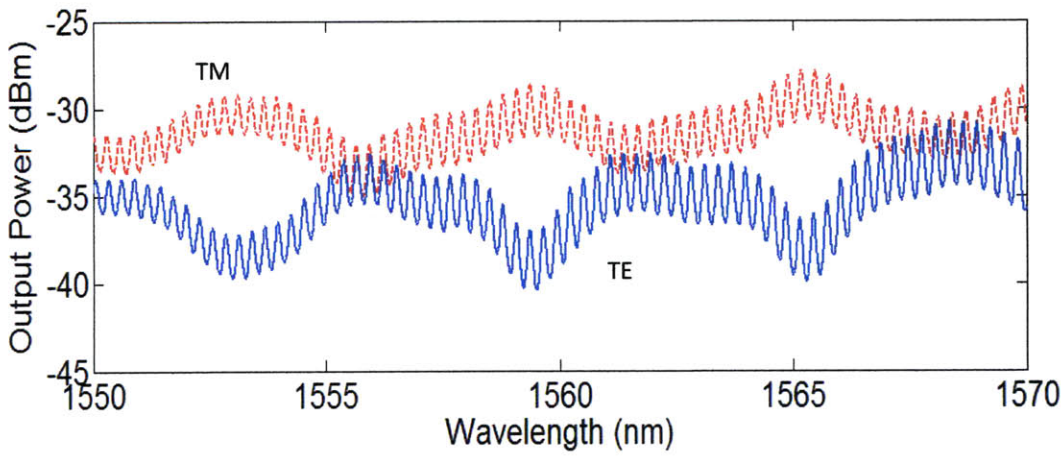


Figure 5-18: Output Power for an undoped Epitaxial Wafer, λ_g=1.45μm in dBm

The final device parameter that speaks to the success of fabrication is the zero birefringence wavelength. Geometrical birefringence can be defined as the wavelength difference between the peaks of the TE and TM electric fields. By finding the peaks and ensuring they belonged to the same resonant

mode we were able to calculate the birefringence as a function of wavelength. From the linear fit we extracted the zero birefringence wavelength for each device. The measured birefringence for the undoped wafer (λ_g = 1.45μm) is shown in Figure 5-19. It has a zero birefringence wavelength of 1544 nm, which when plotted with the theoretical zero birefringence curve for this device (Figure 5-23) corresponds to a device width of 1.34 μm. The mask width of this sample is 1.3μm, when measured with the scanning electron microscope we found a linewidth expansion of +70nm for this device. Thus linewidth calculated from the experimental data is reasonable given the physical width measurements taken after fabrication. The birefringence figures for the other three epitaxial wafers are shown in Figures Figure 5-20, Figure 5-21, and Figure 5-22.

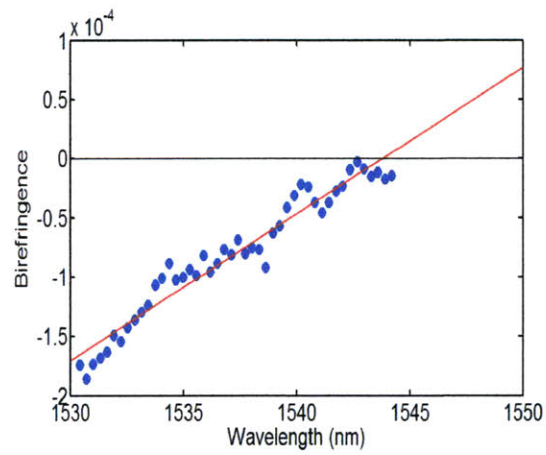


Figure 5-19: Measured Birefringence of an undoped Epitaxial Wafer with λ_g=1.34μm

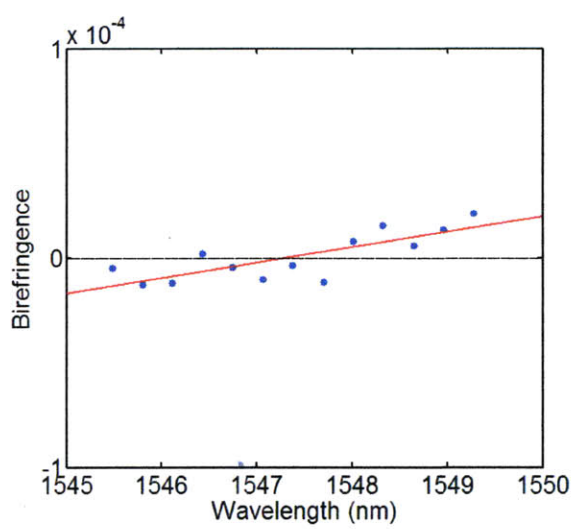


Figure 5-20: Measured Birefringence of the highly Fe doped Epitaxial Wafer, λ_g=1.3μm

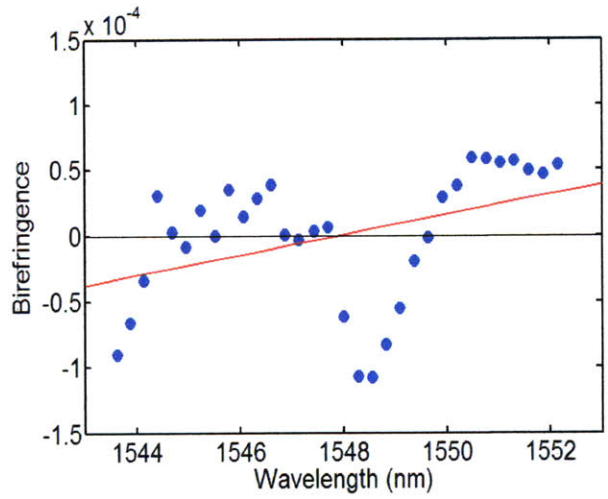


Figure 5-21: Measured Birefringence of a Low Fe doped Epitaxial Wafer, λ_g=1.45μm

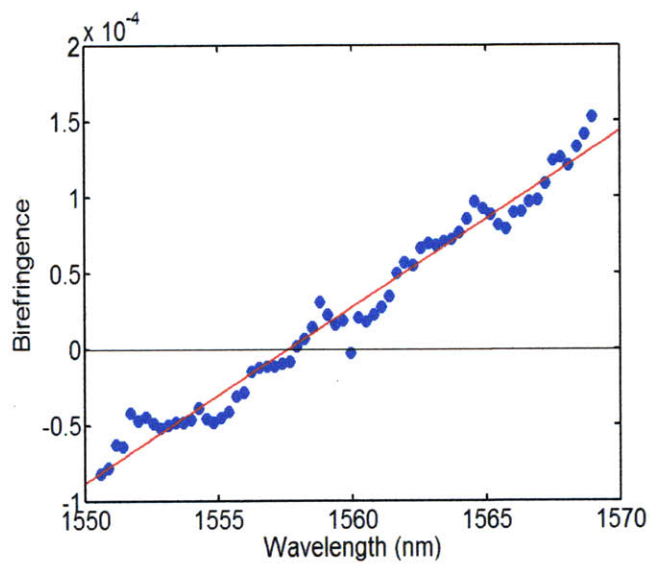


Figure 5-22: Measured Birefringence of an undoped Epitaxial Wafer, λ_g=1.45μm

The zero birefringence point for each of the epitaxial wafers was recorded and used to calculate the device width from Figure 5-23 below. Figure 5-21 show poor fitting around the zero birefringence as compared to the other three fits. The movement around the zero birefringence point is by product of a 10x reduction in the TE and TM output power from the laser during device testing. The calculated zero birefringence and group index for each epitaxial wafer are summarized in the tables below.

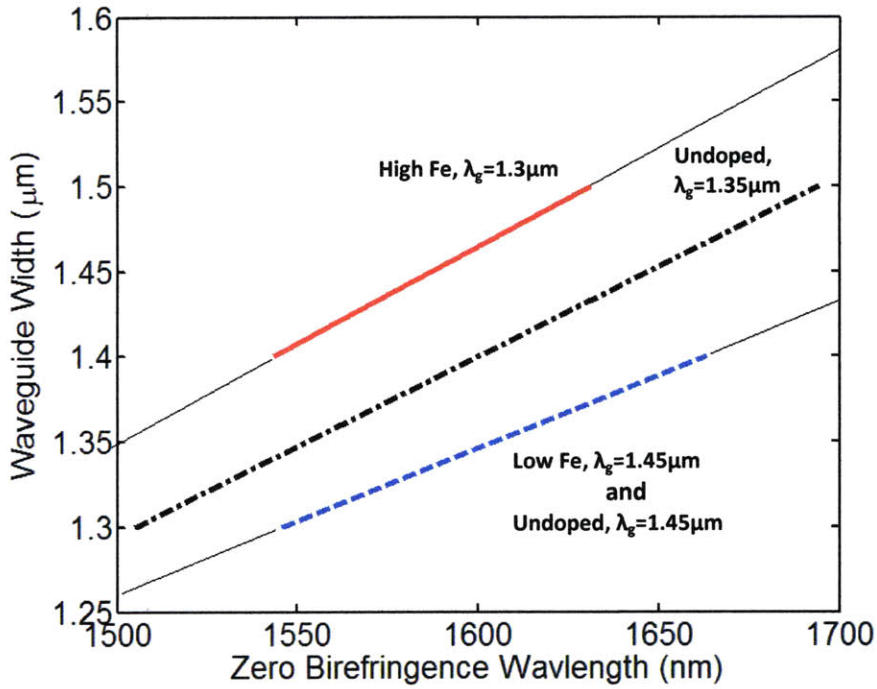


Figure 5-23: Theoretical Model of Zero Birefringence Wavelength vs Waveguide Width

Table 5-3: Epitaxial Testing Summary: Group Index

	Device Length	n_{group}	n_{group}
		TE	TM
Undoped, λ_g = 1.34 μm	1 mm	3.86	3.84
High Fe doped, λ_g=1.3μm	1 mm	3.78	3.76
Low Fe doped, λ_g = 1.45 μm	1 mm	4.40	4.37
Undoped, λ_g = 1.45 μm	1 mm	4.28	4.22

Table 5-4: Epitaxial Testing Summary: SEM Linewidth Measurements

	Mask Width	Average Linewidth Error		
		Photolithography	Mask Contact	ICP
Undoped, λ_g = 1.34 μm	1.30 μm	+40 nm	Good	+70 nm
High Fe doped, λ_g=1.3μm	1.55 μm	-70 nm	Optimal	-110 nm
Low Fe doped, λ_g = 1.45 μm	1.35 μm	+180 nm	OK	+305 nm
Undoped, λ_g = 1.45 μm	1.35 μm	+180 nm	OK	+270 nm

Table 5-5: Epitaxial Testing Summary: Birefringence & Calculated Linewidth Error

	Mask Width	Theoretical Zero Bire. Wavelength	Measured Zero Bire. Wavelength	Calc. Width	Calc. Linewidth Error from Test
Undoped, λ_g = 1.34 μm	1.30 μm	1505 nm	1544 nm	1.34 μm	+40 nm
High Fe doped, λ_g=1.3μm	1.55 μm	1674 nm	1547 nm	1.40 μm	-150 nm
Low Fe doped, λ_g = 1.45 μm	1.35 μm	1606 nm	1545 nm	1.30 μm	-50 nm
Undoped, λ_g = 1.45 μm	1.35 μm	1606 nm	1557 nm	1.30 μm	-50 nm

Testing of the epitaxial wafers shows a tighter linewidth error than that calculated using the SEM. This may be the result of a number of factors. First there is always some measurement error with the SEM because there no set dimension within the tool. To account for this error, calibration features were added to the mask that have 6μm pitch. By measuring the pitch rather than the linewidth we were able to calibrate the measurements in the SEM. Another consideration in SEM error lies in the limits of resolution. Measurements in an SEM are taken by the user manually selecting the edges of the device. This will generate ambiguity in line placement and an error of at least ±10nm in placement.

Consider the raw data shown in Figure 5-15 through Figure 5-18. The amplitude and general course of the waveforms are determined by the background power and oscillations of the optical fiber as shown in Figure 5-24. To the test the influence of these oscillations on our analysis, the background was subtracted from the undoped wafer (λ_g=1.34μm) data and performance parameters calculated.

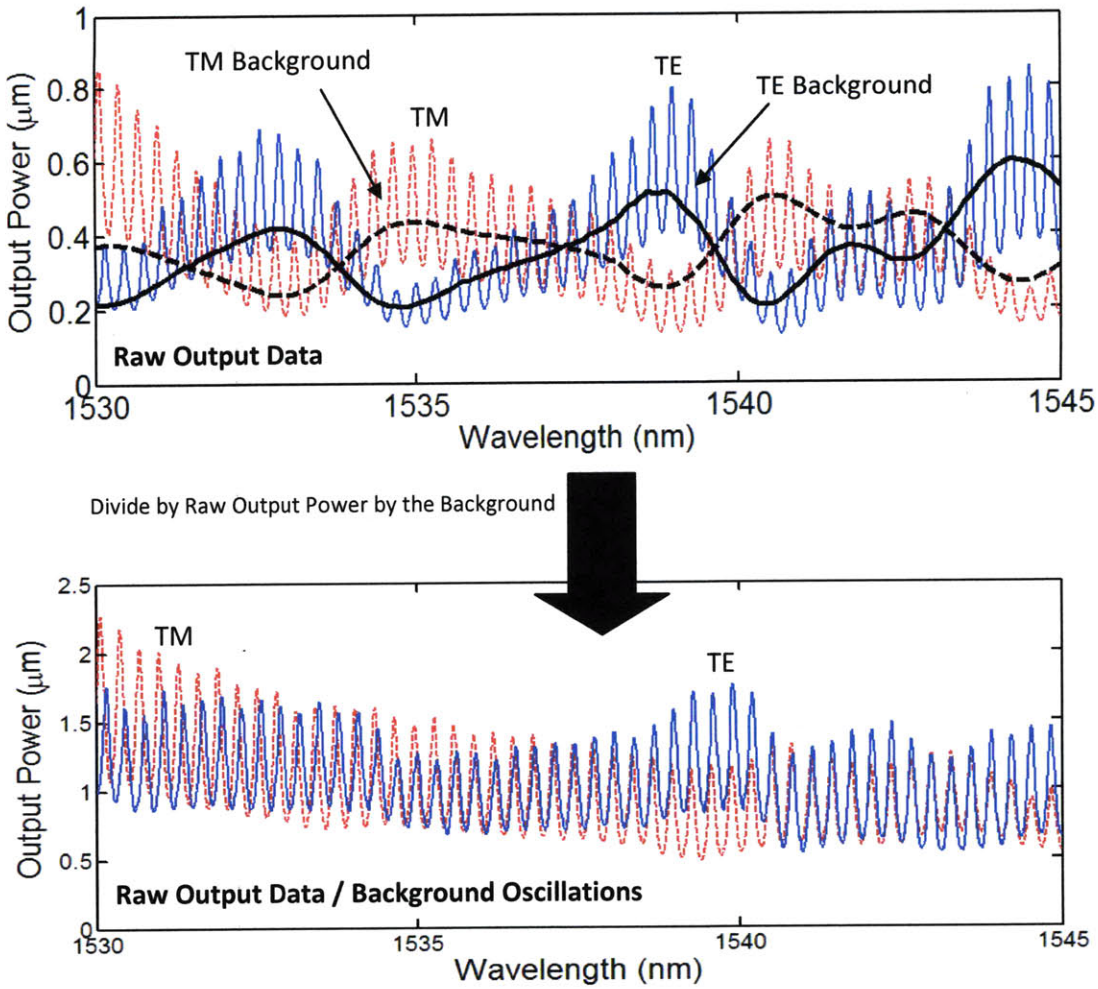


Figure 5-24: Background Oscillations for an undoped Epitaxial Wafer with λ_g=1.34μm

By comparing the loss, zero birefringence point, and group index with and without background (Table 5-6) we found comparable values. The birefringence values have less error around the fit but produce the same zero birefringence point. The loss is reduced, although still negative. This process validates the analysis for the other epitaxial wafers in which the background data was not removed.

Table 5-6: Undoped Epitaxial Wafer with λ_g=1.34μm Device Performance with and without Background Correction

Undoped, λ_g = 1.34 μm		Calculated Values without Subtracting the Background	Calculated Values with Subtracting the Background
n_{group}	TE	3.86	3.86
n_{group}	TM	3.84	3.84
Loss	TE	2.2 dB/cm	1.9 dB/cm
Loss	TM	-1.2 dB/cm	-0.9 dB/cm
Zero Bire. Wavelength		1544 nm	1543.7 nm

After analysis two issues remain unresolved. The first is the negative loss, a blatantly incorrect value. Recall the equations used for loss calculation:

$$\alpha = \frac{\ln(R) - \ln\left(\frac{F-1}{F+1}\right)}{L} \qquad 5.15$$

where R is the cavity reflectivity (R_{facet} = 0.27 for an n_{eff} = 3.2), L is the device length, and F is defined by $F = \sqrt{\frac{P_{peak}}{P_{trough}}}$. When calculating the loss from the raw data rather than the log of the data, we find TE and TM mode losses of 21.1 dB/cm and 18.06 dB/cm respectively. The extreme variation in this calculation imply that Equation 5.15 is an over simplification of the loss for this setup. Equation 5.15 assumes the source of the peak to trough oscillations is purely the Fabry Perot fringes. The raw data alone show that this is not the case. The problem requires a deeper understanding of the test setup and remains an open concern.

The second lies in the calculation of the Verdet coefficient. Although initial Faraday rotation measurements were taken on the device, that showed peaking at the zero birefringence point, the 0.07° of rotation expected for this device were masked by the intrinsic polarization rotation of the lens fiber. Several suggestions can be made for improving Faraday rotation measurements. The first is to decrease polarization sensitivity in the testbed. This can be achieved by replacing the optical fibers, fusion splicing the connectors, and ensuring the wavelength of the polarization beam splitter matches the test range. The second is to isolate the source of rotation in the data by collecting data from positive and negative orientation of the magnet. With the magnet positioned NS the polarization will increase by 0.07°, while positioned SN the polarization will rotate by the same amount in the opposite direction. The work done by Zaman in 2006 obtained polarization measurement with a setup utilizing a rotating magnet and lock-in amplifier. However initial tests run with a similar setup showed significant coupling with the metal devices used to mount the epitaxial wafer.

The zero birefringence measurements in this section provide us with insight into the dimensional control during fabrication and the devices' response to the variations in the epitaxial composition. By matching the zero birefringence wavelengths to the theoretical device width we found a linewidth error of ±150nm which is significantly less than the ±250nm of linewidth error measured at the SEM. Although the devices were fabricated outside the dimensional limits, the zero birefringence point was easily found on all of the devices tested. A clear shift in the zero birefringence wavelength was also seen according to the bandgap energy, and core and cladding thickness as described by Figure 5-23. Issues with polarization stability complicated Figure of Merit calculations, which ultimately were left unresolved due to time restrictions.

6 Future and Ongoing Work

6.1 Thesis Review

The goal of this thesis was to develop a fabrication process that could reliably control the feature dimensions to ±65nm. The importance of dimensional control was introduced in Chapter 1 when we investigated the fabrication requirements of common photonic devices such as the Mach Zehnder interferometers that require length control of ±71nm. Because of the importance and limited success in the fabrication of monolithic optical isolators, much work has been put into developing techniques to fabricate InP Faraday Rotators and halfwave plates. First generation InP Faraday rotators were fabricated in 2006 using slow, expensive, low throughput techniques such as ebeam lithography and methane hydrogen reactive ion etching. Although successful this technique it did not provide a good fabrication process for production. These needs defined the objective of this thesis: define a low cost, high speed, high throughput fabrication process that can accurately transfer a pattern into InP with ±65nm precision.

Chapter 2 introduced inductively coupled plasma reactive ion etching as a high speed alternative for etching of III-V materials. During process develop we examined the complex interplay of the etching parameters such as ICP power, bias power, pressure, and gas chemistry with the chamber conditions temperature and carrier wafer composition. Within the ICP RIE chamber, the ICP power determines the ion density in the chamber as it strips the radical chlorine ions from the $SiCl_4$ and Cl_2 molecules in the plasma. After being accelerated by the bias power the ions react with InP substrate to generate PCl_3 and $InCl_x$. The etch rates and profile were highly dependent on sample temperature which was adjusted to balance $InCl_x$ desorption and with isotropic chemical etching occurring above 300°C. This was achieved by thermally adhering the InP sample to the temperature controlled ceramic carrier wafer. Dependent relationship of the etching parameters presented an overwhelming array of options during recipe optimization. Rather than trial and error, the process was established using a design of experiment called the Taguchi method to reduce the number of etch tests required to produce adequate profiles. At the conclusion of the chapter we detailed the fabrication process used to generate InP faraday rotators with a maximum linewidth error of ±250nm from the intended dimensions, and negligible errors when compared to the dimensions of the SiO_2 hardmask.

The exploration of the fabrication process continued in Chapter 3 as we examined reactive ion etching of SiO_2. For the fabrication of InP devices SiO_2 is used as an etch mask for the $SiCl_4$ ICP RIE of InP. The dielectric mask is patterned in a CHF_3/CF_4 plasma with a photoresist mask and selectivity of $1_{SiO2}:25_{InP}$. During process development high radical densities were shown to increase the etch rate but

damage the photoresist to the point that it was unable to retain its shape during etching. To improve the resist strength in a high energy CF_4 plasma, a preliminary 6 minute etch in CHF_3 was used to coat the outside of the resist with organic polymer. This significantly decreased the etch rate of the photoresist and improved linewidth verticality. A proven recipe, this processing step was not focused on during development, so ended up increasing the linewidth error from the photoresist pattern by ±50nm, leading to a ±250nm error from the desired width on the mask. When using this process in the future I suggest using a glass slide to prevent the path to ground and increase the physical etching as well as reducing the amount of SiO_2 deposited (for more details on that suggestion refer to 0). This will further improve etch rate as well as the profile and pattern transfer during RIE.

Chapter 4 focused on the foundation of all dimensional errors in device fabrication, lithography. In order to reduce costs, improve repeatability, and throughput a fabrication process was developed using contact optical lithography rather than electron beam lithography. By using a narrow exposure band around 365nm, the optimal exposure wavelength for AZ-5214E, we were able to significantly decrease feature size resolution and increase repeatability. Errors in the process were a result of poor contact between the mask and photoresist due to the build up of edgebead or particles on the surface of the resist. The gap generated by the particles broadens the diffraction pattern and in turn the resulting resist profile. The process was optimized to the point that development time no longer affected the resist profile. With good contact between the mask and the resist we saw a linewidth error of ±200nm. This value is outside the range of acceptable fabrication errors for the Faraday rotator fabrication. With optimal contact we saw the error reduced to ±140nm with values as low as +40nm when fabricating the undoped epitaxial wafer (λ_g = 1.34 μm). Linewidth narrowing was a trend seen with optimal contact, one that implies a slight over exposure that can be adjusted by fine tuning of the exposure time.

By processing 4 different epitaxial wafers using the recipe outline in the first 4 chapters, we were able to produce a large array of InP Faraday rotators. In Chapter 5 we examined the experimental setup used to the test the devices. Although several parameters could be tested for, this thesis focused on the tests that provided feedback on the fabrication process rather than the epitaxial material composition. Linewidth error calculated using a scanning electron microscope (SEM) in Chapters 2-4 were validated by determining the zero birefringence wavelength for each device. In doing so we found linewidth errors of ±150nm, a significant improvement over the linewidth error calculated with the SEM. The ±100nm difference in linewidth errors between the two measure methods, may be attributed to calibration errors in the SEM and/or poor output data due to fiber birefringence in the test setup. Other tests results such as scattering loss and the Verdet coefficient showed inconsistent results due to the polarization errors in the testbed and limited magnetic data.

Although the fabrication process outlined in Appendix B did not meet the ±65nm fabrication requirement for InP Faraday rotators, the success of device testing at the zero birefringence point encouraged us to expand the process to the fabrication of InP half waveplates. Since 1991 several attempts have been made to make integrated polarization controllers of various materials and configurations. A periodic array of materials with different indices of refraction, gave way to waveguides with angled facets. These ideas were simplified in Zaman's optical isolator design, when a

notched upper cladding in the waveguide generated a geometrical birefringence that was used to rotate the polarization. His design specified an 850nm notch on 1.4µm waveguide along 0.16 mm to produce 22.5° of rotation.[**1**] In this work the dimensional control was not focused on, but rather a proof of concept that contact optical lithography and ICP RIE could be used to fabricate a notched waveguide. An overview of the process development for InP half waveplate fabrication is provided in Section 6.2.

6.2 InP Half Waveplates

At the conclusion of my time at MIT I began work on an InP half-wave plate (HWP) as part of the optical isolator design put forth by Zaman in 2006.[**1**] This section begins with an introduction to the physics behind polarization rotation. Followed by a look at the 4 different fabrication approaches explored as viable options to produce an InP notched waveguide. First generation HWPs were successfully fabricated using the process developed for Faraday rotators. It begins by producing a 1.4µm waveguide and then aligning and patterning a notch guide on top of the first offset by the gap width. Unfortunately testing was never completed on these devices, but preliminary results are shown in Section 6.2.3. Special attention should be paid Section 6.2.2.4, which examines a self-aligned process that with some additional development can be powerful tool for optical isolator fabrication.

6.2.1 Theory

The polarization of an electromagnetic field is a description of the amount of light in the TE and TM mode of the electric field as defined by:

$$\theta = tan^{-1}\left(\frac{E_{TE}}{E_{TM}}\right) \qquad 6.1$$

Traditional polarization rotators utilize a material's intrinsic birefringence to retard one of the modes causing the power from one mode to couple to the other along the length of propagation. Early integrated polarization controllers used periodic structures with different indices of refraction. The different indices rotated the slow and fast axis off the vertical as shown in Figure 6-1. [**56**]

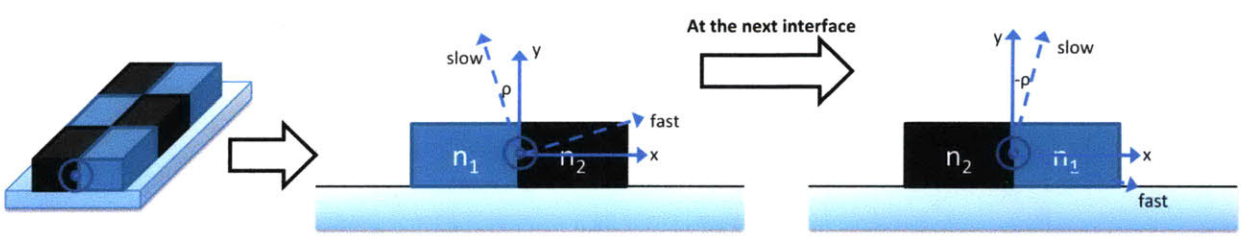


Figure 6-1: Periodic Polarization Controller

At the junction between the materials the light is scattered and codirectionally coupled into the other modes. Because of the alternating pattern the device acts as a folded Solc filter doubling the polarization rotation (Γ) at every interface.[**56**] Unfortunately this design required several millimeters to

generate a 90° of rotation with loss at every junction. The design evolved in 1995 with the introduction of angle facets in the periodic structure. These features generated pronounced rotation of the electric field axis that increased the rotation per junction and reduced the device length by 20x.[**57**]

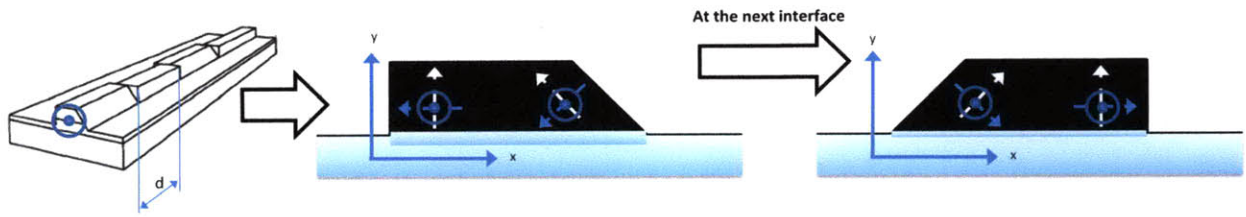


Figure 6-2: Angled Facet Periodic Polarization Controller [58]

Tzolov proved that the periodic structure could be removed entirely by simply engineering the shape of the waveguide to create a geometrical birefringence which would rotate the polarization during propagation.[**59**] Zaman took this idea and step further and simplified the design from an angled facet to a notched waveguide showing that a gap width of 0.55µm in a 0.16mm device could be used to produce 22.5° of rotation, as shown in Figure 6-3. XX

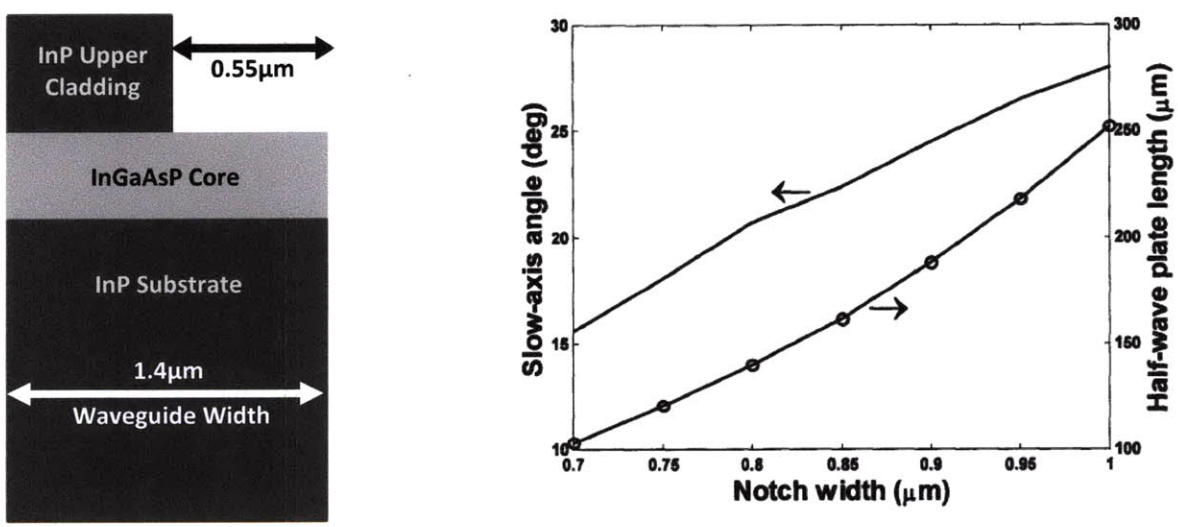


Figure 6-3: Zaman HWP Specifications[11]

Before any of these theoretical designs can be verified the device must be fabricated. The rest of this section is dedicated to the fabrication process development for the first generation notched waveguides.

6.2.2 Fabrication Process

The desired polarization rotation of 22.5° occurs with a notch of 0.85µm on a 1.4µm wide device. Four different fabrication approaches were explored to produce a notch at the top of a waveguide:

- Notch Fabrication using Al_2O_3 Liftoff

- Wet Etching of InP Notched Waveguides using a Photoresist Mask
- Dry Etching of InP Notched Waveguides using a SiO_2 Hardmask
- Titanium Self-aligned Process

The first process involved etching the notch first and then patterning the waveguide on top of the recess in the substrate. The poor initial results motivated a design shift that produces the InP waveguide first and then patterned the notch through wet or dry etching. The wet etching test used photoresist to mask the top of the device, where the width was visually aligned with the microscope on the Karl Süss MA-6. The InP was then removed with a 1:1 mixture of hydrochloric and phosphoric acid. The second process, also visual aligned, defined the notch with photoresist and an SiO_2 hard mask using the fabrication processes defined for the Faraday rotator. The final development test was the most promising in terms of notch width control because of its ability to control the etch mask removal down a few nanometers.[**60**] The devices produced in this work were developed as a proof of concept rather than focusing on the dimensional control of the notch. Thus a photo mask was never designed to help facilitate the alignment of the notch with the top of the waveguide. Traditionally alignment is controlled by matching a series of alignment marks on the mask and substrate, a process not available at this time but one which would significantly improve dimension control and placement of the waveguide notch.

6.2.2.1 Notch Fabrication using Al_2O_3 Liftoff

The initial fabrication plans for the polarization rotator were designed to etch the notch first and then the waveguide. The first attempt was a lift-off process with Al_2O_3 to generate a series of wide stripes across the face of the wafer. The 50μm period was selected so that if one 1μm waveguide was not centered along the ridge of the pre-etched trench, another waveguide on the wafer would be. Figure 6-4 shows an outline of the fabrication process used for the Al_2O_3 patterning of a half waveplate.

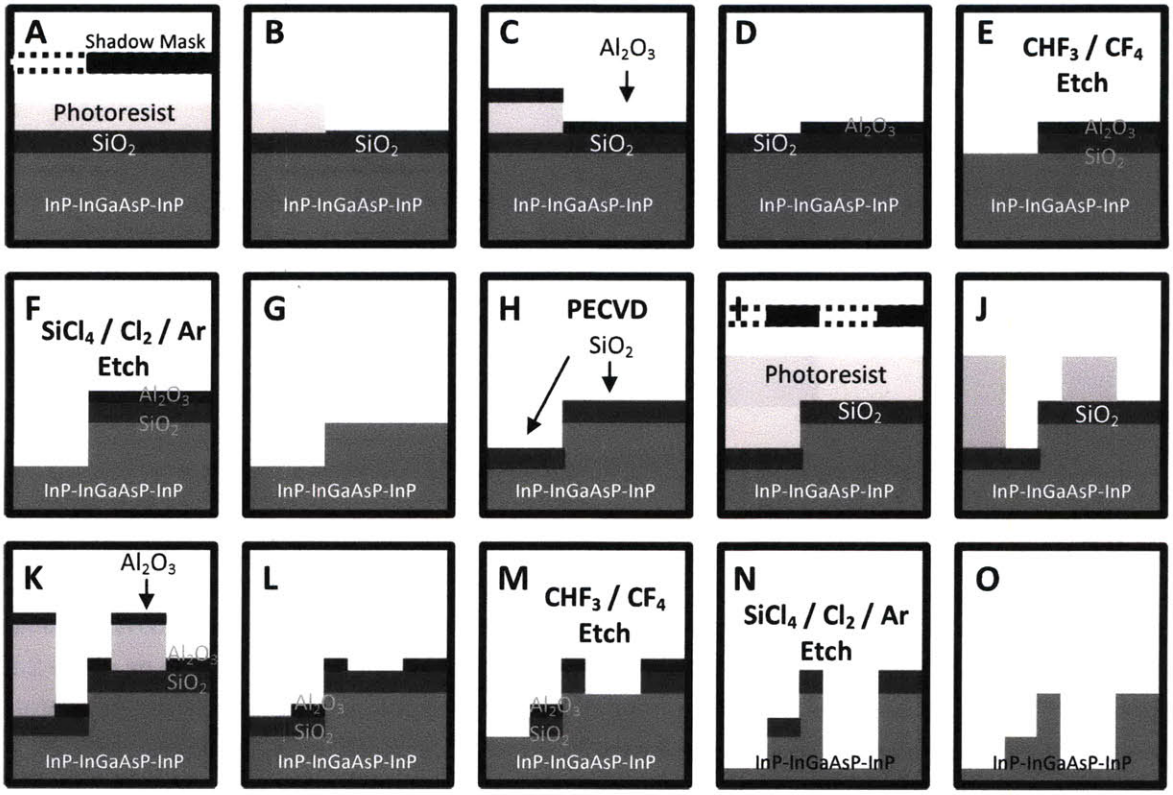


Figure 6-4: Half Waveplate Fabrication: Attempt #1

After the deposition of 250nm of SiO_2 on the InP substrate, contact optical lithography was used to transfer the wide feature pattern from the first mask into the NR7-1500PY resist (Figure 6-4B). The fabrication details for the lift-off of 80nm of Al_2O_3 used here and in Chapter 2, Section 2.1.3 is found in Appendix C. This dielectric layer was used as a hardmask in the CF_4 (recipe 1) RIE plasma to pattern the SiO_2 (Figure 6-4E). The large features were then transferred into the InP with the original Taguchi optimization recipe given in Chapter 2, Section 2.1.3 Table 2-6. After the notch was in place the remaining SiO_2 was removed in a buffered HF dip, and then redeposited using the PECVD described in 0. This provided a uniform SiO_2 layer to use as the ICP RIE etch mask for the waveguide fabrication step. In the second round of processing the NR7-1500PY is patterned with the small feature mask (Figure 4-13) designed for the Faraday rotators (Figure 6-4I). Special care was taken during the alignment stage to position the waveguide over the trench edge on the substrate. The liftoff and etching process was repeated in steps I-O in Figure 6-4 to produce the final waveguide.

Unfortunately for this process, the fabrication recipe had not be refined enough to produce repeatable or reliable results. Figure 6-5 shows a SEM image corresponding to step J in Figure 6-4. Although this process showed poor initial results, it proved that we could align a 1.4µm waveguide around a predefined trench using the microscope alignment tools provided on the Karl Süss MA-6. This process was abandoned, once the Al_2O_3 ICP RIE process was abandoned due to large linewidth errors during fabrication. However it showed that microscope alignment could be used to offset a waveguide on a ridge, and produce a notched pattern. This proof provided us with a stepping stone for future half waveplate fabrication.

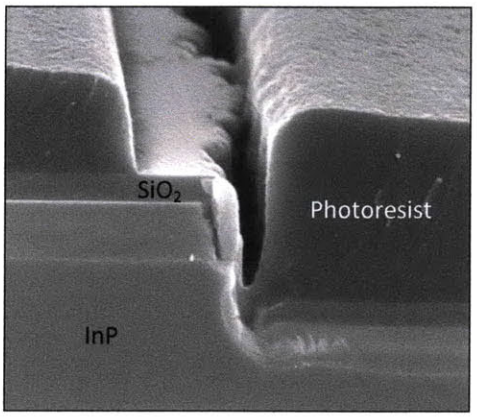


Figure 6-5: Proof of Photoresist Alignment around a Notch (Step J)

6.2.2.2 Wet Etching of InP Notched Waveguide using a Photoresist Mask

The additional complexity generated by the large number of steps in the process described in Section 6.2.2.2 led to an exploration of other techniques which defined the InP waveguide first and then etched the notch. In this section we examine the fabrication process which attempted to wet etch the notch using HCl and phosphoric acid. The process works by attacking the In or P bonds that form the planes in the InP. By aligning the waveguides along a crystal plane wet etching should result in a smooth square edge. Two samples were processed during this test. The first was design so the waveguide ran parallel to the crystal axis and the other with the waveguides perpendicular to the crystal axis.

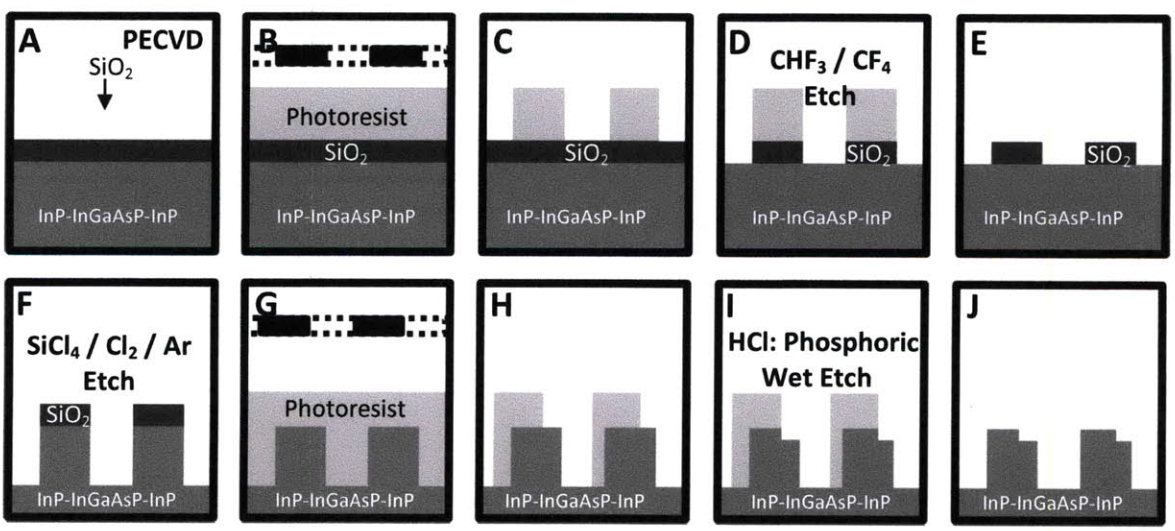
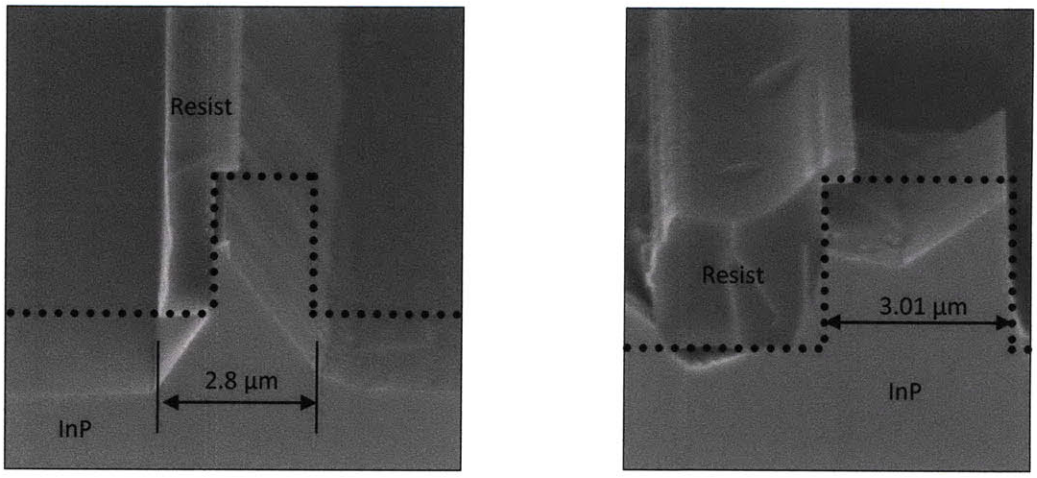


Figure 6-6: Fabrication Process: Attempt #2

The fabrication process begins by etching InP waveguides using the process developed for the Faraday rotators shown in steps A-F of Figure 6-6. Clariant AZ5214E was spun on at a thickness of 1.4μm planarzing the surface before exposure. The shadow mask is aligned, offset from the original

waveguides, to generate an exposed region of the waveguide which will become the waveguide gap after etching. (Figure 6-6G and Figure 6-6H). Both wafers were placed in a bath of 1:1 HCl and phosphoric acid. After approximately 1.5 minutes of agitation the wafers were removed, rinsed in DI water, and examined in the scanning electron microscope. The resulting profiles are shown in Figure 6-7. We expected to find a strongly defined etch profile in the device with the waveguides along the crystal axis. Instead we saw angular etching on both samples, a result that should be explored in future.



(A) Sample 1 (B) Sample 2

Figure 6-7: Wet Etch Results

6.2.2.3 Dry Etching of InP Notched Waveguide using a SiO_2 Hardmask

The inability of the wet etch to remove the material in the desired location, lead to a fabrication process that utilized the process developed for the Faraday rotators. Consider the process outline below in Figure 6-8. The waveguide is patterned first using the 3 step process of contact lithography, RIE etching of the SiO_2, and ICP RIE etching of the InP. The notch is then defined along the top of the waveguide by offsetting the small feature shadow mask designed for faraday rotator from the prefabricated waveguide as seen in Figure 6-8E and Figure 6-8F. The critical alignment of the notch occurs before exposure by visually aligning the top of the mask waveguides with the previously etched device that is visible through the 1.4µm of photoresist. In order to reduce the number of processing step the SiO_2 from the first waveguide definition is also used for the notch mask. The 1_{SiO2}:25_{InP} selectivity of SiO_2 over InP allows the material to withstand the first $SiCl_4/Ar/Cl_2$ plasma etch, allowing it to be left on the sample and used for masking the notch.

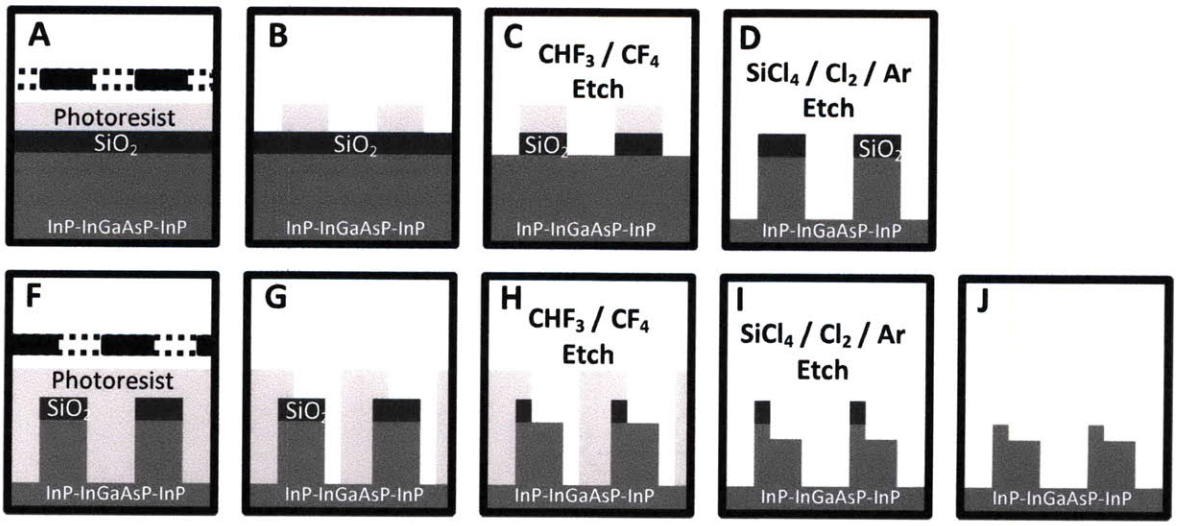
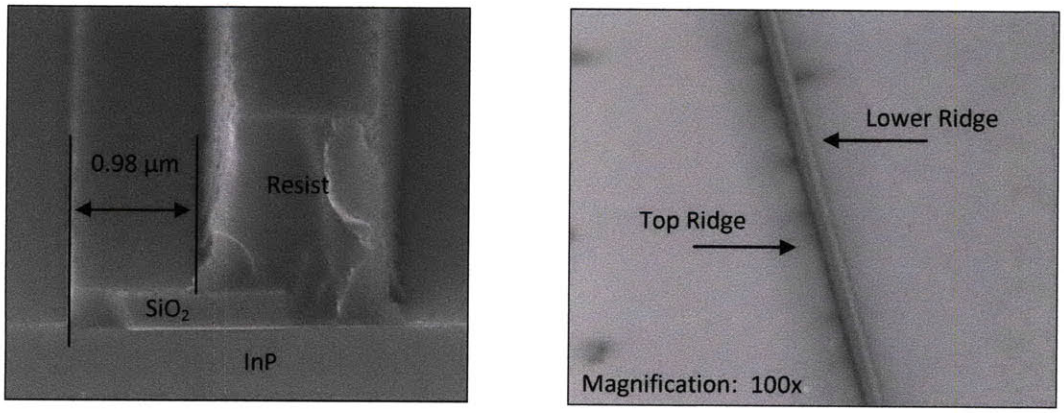


Figure 6-8: Halfwave Plate: Attempt #3

The success of the notch alignment using visual inspection on the MA6 can be seen in the early SEM image of the resist profiles over SiO_2 (Figure 6-9A) and microscope images throughout processing (Figure 6-9B). The image shown in Figure 6-9A does not correlate to any of the steps in Figure 6-8 but was a test sample run before the InP was etched as a proof of positive photoresist alignment. By placing the samples shown in Figure 6-9 into the CHF_3/CF_4 plasma the exposed SiO_2 will be removed generating a profile like the one shown in Figure 6-8G.

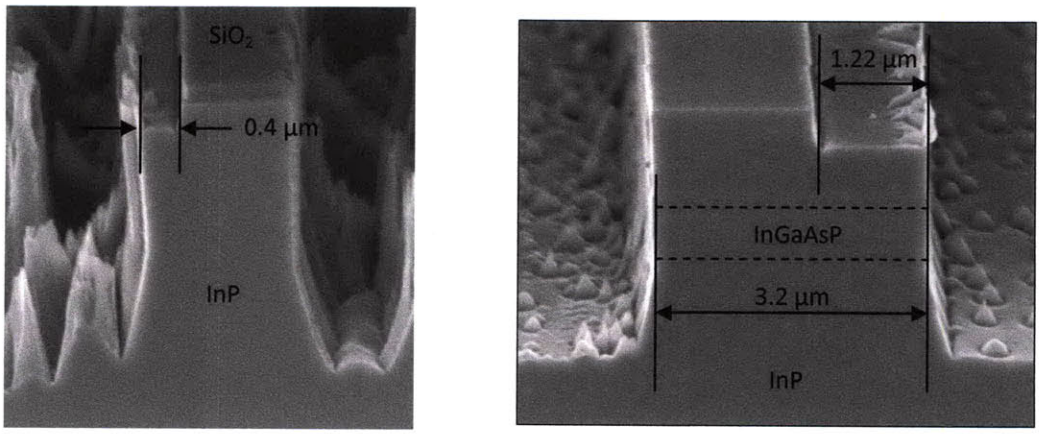


(A) Alignment Proof: Photoresist aligned over SiO_2 (B) Step G observed with a 100x microscope

Figure 6-9: Photoresist Offset Alignment

In Chapter 2 we produced an ICP RIE etch recipe that produced smooth vertical sidewalls, limited trenching, and minimal $InCl_x$ on the surface. These benefits allowed us to use the Samco ICP RIE tool to etch a clean recess in the top of the InP waveguide as shown in Figure 6-10. The device fabricated

using this process, were functional prototypes that were tested using the setup and procedures outlined in Chapter 5. Initial test results are discussed in Section 6.2.3.



(A) Early proof of concept (B) Functional Proof of Concept

Figure 6-10: Functional Integrated InP HWP

Figure 6-10A is an early device that shows significant build up along the shelf edge, this maybe be due to the roughness of the SiO_2 that can be seen in along the top of the device. However it may also be $InCl_x$. Both device show $InCl_x$ across the surface, which is by product of the additional processing steps and should be examined further. The function proof of concept HWP were fabricated out of the low Fe doped wafer (λ_g = 1.45µm). Two functional devices were found both located in the 1.50µm portion of the mask. The initial test results for these samples is provided in Section 6.2.3.

6.2.2.4 Titanium Self-aligned Process

Although a notched waveguides were generated using the process outlined above, that method will ultimately be limited by the alignment resolution of the MA6 exposure tool. The notch positioning will be improved by adding alignment marks to shadow masks but achieving alignment control down to ±10nm is a difficult task. Thus a process was developed to define with the notch width using a thin Titanium layer and a slow reaction Ti wet etchant to defined the notch width.

The idea originated from a paper by Fujimaru in which 50nm of TiO_2, generated by anodic oxidization, was selectivity removed from the surround Ti mask.[**60**] Due to time constraints we were unable to construct an anodic oxidation setup to test the process the outlined in Faujimaru's paper. Instead we used a thin layer of Ti sandwiched between the SiO_2 and photoresist, which was removed with a premixed Ti etchant solution produced by the Transene company. Figure 6-11 outlines the fabrication process.

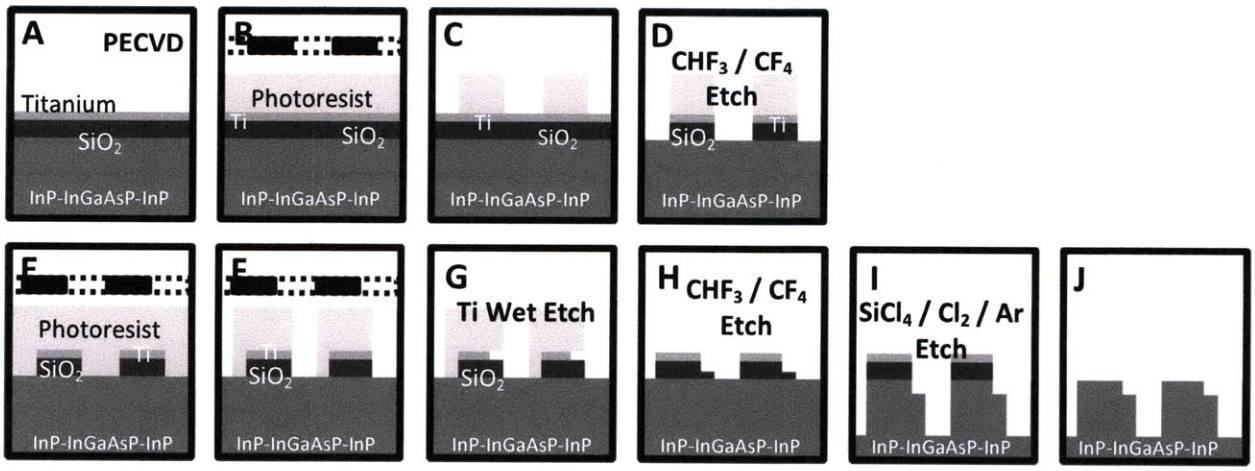


Figure 6-11: Self-Aligned Notch Process: HWP Attempt #4

The fabrication process starts by depositing 250nm of SiO_2 and 80nm of Titanium onto the surface of a clean InP wafer. The SiO_2 was deposited using the STS CVD tool in MIT TRL cleanroom using the procedure outlined in Appendix B. The Ti was deposited by Jim Daley in the Nanostructures Laboratory (NSL). The bi-layer hardmask was then patterned using contact optical lithography and RIE etching in a CF_4 plasma (Figure 6-11E). To protect the Ti from being etched from both sides during etch etching, half the feature is protected by a second layer of photoresist deposited by contact optical lithography and offsetting the alignment of the waveguides (Figure 6-11G). The Ti was then removed in a 10:1 bath of DI water to Transene Titanium etchant. After soaking the sample in the bath for 10 seconds ~450nm of Ti were removed as shown in Figure 6-12. By plotting the amount of Ti removed verses time we found a linear relation between Ti removal and etch time, this can be used to calculate the optimal dilution and etching time to obtain a 0.55μm gap in the waveguide.

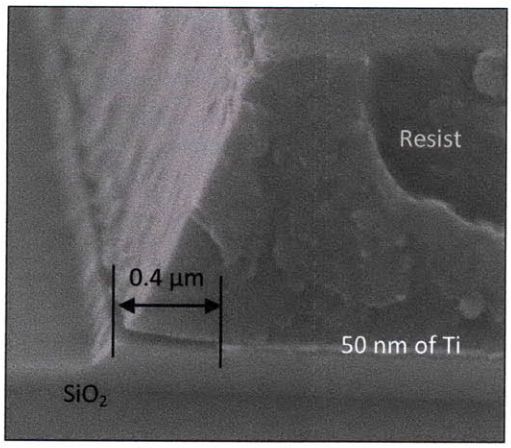


Figure 6-12: Ti Etched

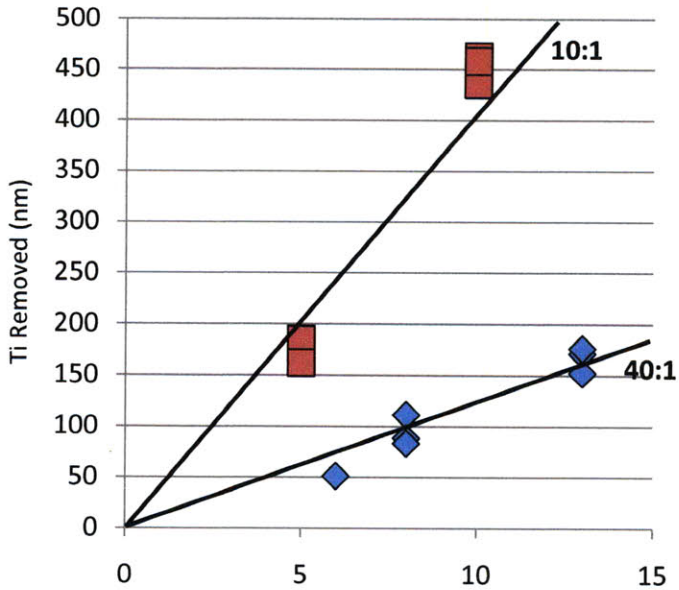


Figure 6-13: Ti Etch Rate in Diluted Ti Etchant

The drawback of this process was the uneven edge created by agitation of the liquid etchant as shown in Figure 6-14. Note, the sample shown in Figure 6-14 was not protected on one side by photoresist, thus both sides were removed evenly by the liquid etchant. Solutions to this problem would be to soak the sample in the wet etchant without agitation. Another could be to use the anodic oxidation process described in the Fujimaru paper. The roughness seen after wet etching precluded us from continuing to the ICP RIE step. However preliminary tests with Ti masks in the ICP RIE tool during a $SiCl_4/Ar/Cl_2$ etch have been run. After 2 minutes of etching the 50nm of Ti was still intact on the surface of the wafer.

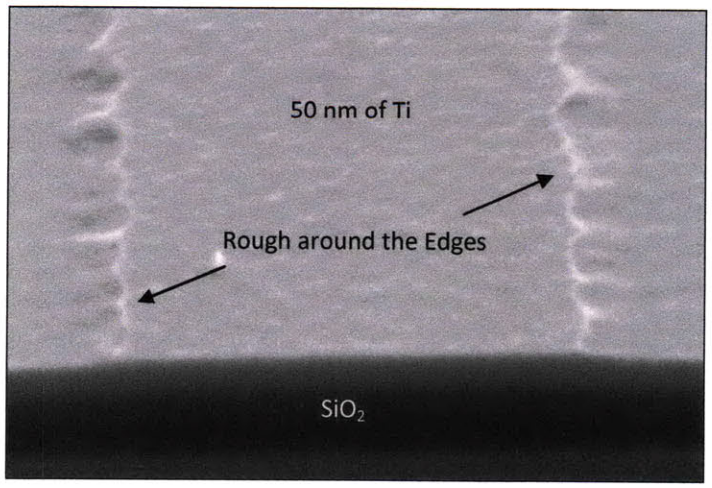
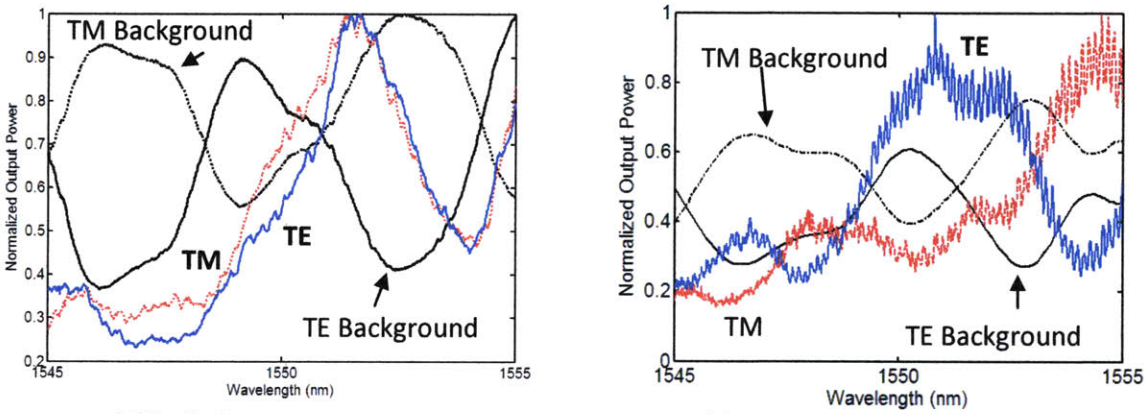


Figure 6-14: Ti mask after Wet Etching

6.2.3 Test Results

The epitaxial prototypes were lapped, cleaved, and mounted on a glass slide according to the procedure outlined in Section 5.2. Light was successfully coupled into the device and collected at the TE and TM free space detectors. These results are shown below in Figure 6-15.



(A) Preliminary HWP Data (B) Poorly Coupled Faraday Rotator Data

Figure 6-15: Preliminary HWP Data

Figure 6-15A is the normalized output power for the TE and TM modes of the HWP. The general shape and lack of clearly defined Farby Perot fringes mimics the behavior of a poorly coupled Faraday rotator, whose is data is shown in Figure 6-15B for comparison. The interesting and consistent effect seen in the HWP data is the lack of beating in the TE and TM modes, which indicates a constant polarization. The normalized power for a different HWP over a range of wavelengths is shown in Figure 6-16. This data is provided to allow for easy comparison of the TE and TM powers and to highlight lack of mode beating in the output power. The physical meaning of this data is not understood is left for future work.

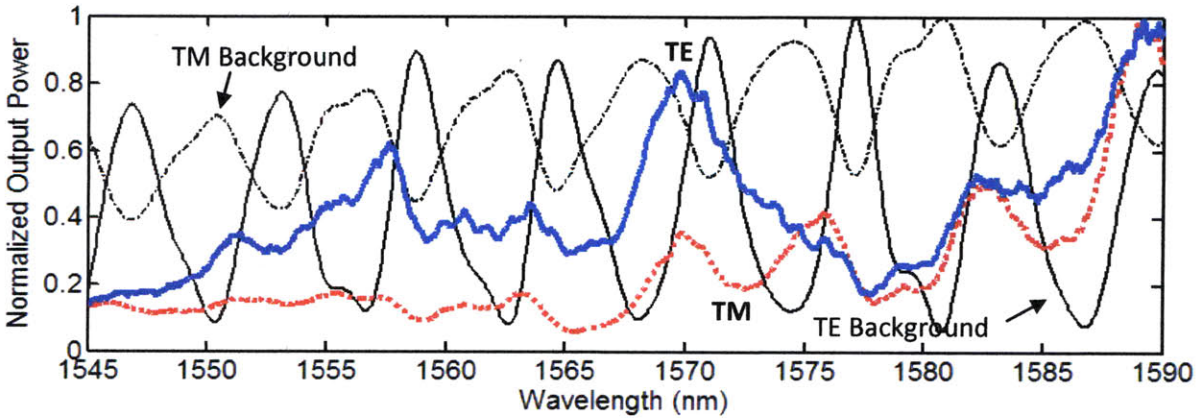


Figure 6-16: HWP#2 Normalized Output Power

6.3 Suggested Improvements

The fabrication process and devices produced by this thesis provide a strong foundation for the future fabrication projects. Although pattern transfer from the mask to InP substrate did not meet the ±65nm dimensional requirements for Faraday rotator fabrication, I was able to produce Faraday rotators and half waveplate structures in a single epitaxial run. My process reliably generates features in InP with a maximum linewidth error of ±250nm, error as little as ±70nm when a optimal contact is achieved during photolithography. All SEM measurements were verified with the experimentally with the zero birefringence point for each wafer, which indicated even tighter dimensional control with errors as low as ±40nm. Although this process can achieve the dimensional control required for photonic fabrication it is important to continue process development to reduce the maximum linewidth error.

Several fabrication process improvements can be made which will increase the pattern transfer fidelity. Photolithography error stem from poor contact between the mask and resist during exposure. Thus by continuing to improve photoresist removal from the back and edges of the sample as well as the shadow mask, we greatly increase the likelyhood of optimal contact and good feature reproduction. The RIE was the biggest factor in easily controllable dimensional errors. Unlike photolithography which is highly dependent on several processing step, RIE transfer is dependent on chamber conditions and etching parameters which should be tuned to produce negligible errors during pattern transfer as was seen with the ICP RIE precipe. Suggested RIE improvements include adding a glass slide to the CHF_3/CF_4 plasma etch, thinning of the SiO_2, and a Taguchi optimization test. The ICP RIE did not add to the dimensional error, but linewidth narrowing at the base of deep etches and the continued presence of $InCl_x$ on the etching surface should be examined and reduced.

Another major challenge in this work occurred during device testing. Poor polarization stability caused use to question the raw data and masked the polarization rotation induced by the Faraday effect. Time should be taken to understand what is going on at each stage of the test setup to verify the source of the error. Once a stable platform for testing has been established, the testing itself should be examined. The critical mistake in the testing of the Verdet coefficient lied in a poor understanding of what to expect theoretically and the masking effects of the environment. By simply taking data in a forward and backward magnetic field, rather than just forward, I would have been able to isolate the rotation from the background. Lack of basic device mechanics also hampered the loss calculations in this thesis.

The weakness in theoretical understanding and gaps in the big picture define this work as a master thesis rather than PhD. Fabrication would be complimented by a deep understanding of how each of photonic device performs. This goes beyond electromagnetic field interactions discussed in this work. A complete understanding of a photonic device involves having a physical picture of systems and understanding how epitaxial material, thicknesses, band gap energies, device dimensions, and external influences such as magnetic fields effect the operation of the device. This will allow me to design better devices in the cleanroom and predict the experimental results. By improving the testbed design and analysis, I will generate more reliable results. It is clear from this discussion that future work in this field will be highly reliant on the strong theoretical understanding of the device, something that was not appreciated early enough during my Master's thesis.

Assuming that this foundation is in place a strong PhD thesis would include the fabrication of several photonic devices all related to photonic integration and optical isolation. Initial challenges would include the fabrication of the InP half waveplate, multimode interferometers, and integrated optical isolator. The high mesa integrated isolator could be used as a stepping stone to explore buried structures as well as other integrated photonic devices. What these device would be, would materialize from an in depth understanding of the needs of the photonic industry. What is going on in the market and who needs it are critical questions to the success of any project and the source of relevant research projects.

Appendix A Normalized Waveguide Function

The behavior of an electromagnetic wave is dependent on system constants such wavelength and refractive index of the surrounding materials. Consider light in a waveguide of width d with refractive indices of the core and cladding defined as n_{core} and n_{clad} respectively. The amount of influence each of these materials has on the EM wave is expressed as the effective index (n_{eff}) for the system, which is dependent on the width of the device.

The effective index, as well as the number of mode within a waveguide, can be determined from the relationship of the normalized refractive index and normalized width of the device. The normalized width is defined as:

$$V = \frac{m\pi + tan^{-1}\left(\sqrt{\frac{b}{1-b}}\right) + tan^{-1}\left(\sqrt{\frac{a+b}{1-b}}\right)}{\sqrt{1-b}} \qquad \text{A.1}$$

where m is the waveguide mode, b is the normalized refractive index (defined in Equation XYXY) and a is defined as:

$$a = \frac{n^2_{lower\ cladding} - n^2_{upper\ cladding}}{n^2_{upper\ cladding} - n^2_{lower\ cladding}} \qquad \text{A.2}$$

a is included in the calculation of the normalized width to allow for complicated epitaxial stacks comprised of multiple cladding materials . In our work we are dealing with a homogenous InP cladding, thus a=0. b is the normalized refractive index ranging from 0 to 1. In Figure A-1, we assume all possible values of b and plot the normalized waveguide width at different modes.

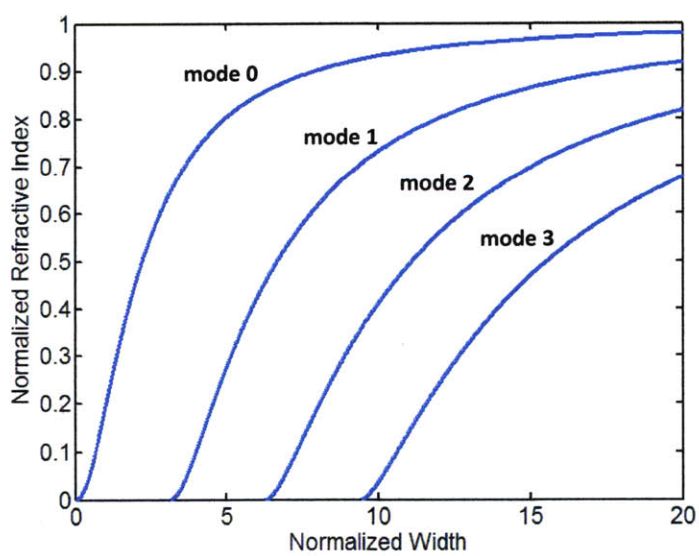


Figure A-1: Normalized Width vs Normalized Refractive Index

The width of the device is related to the normalized width according to:

$$V = kd\sqrt{n_{core}^2 - n_{clad}^2} \qquad \text{A.3}$$

Given a width d and the indices of refraction for the core and cladding of the waveguide of interest, we can solve for a device specific normalized width (V). From Figure A-1 we can determine the normalized refractive index and number of modes within that waveguide. For a 1.4μm InP-InGaAsP-InP waveguide the refractive indices of n_{core} = 3.22 (InGaAsP) and n_{clad} = 3.14 (InP) and an operational wavelength of 1550nm, the normalized width is 4.05. Plotting this on the normalized curve (Figure A-2), we find b_o = 0.73 and b_1 = 0.11. Since the V crosses both the first and second mode lines in Figure A-2, we know this device is a multimode waveguide.

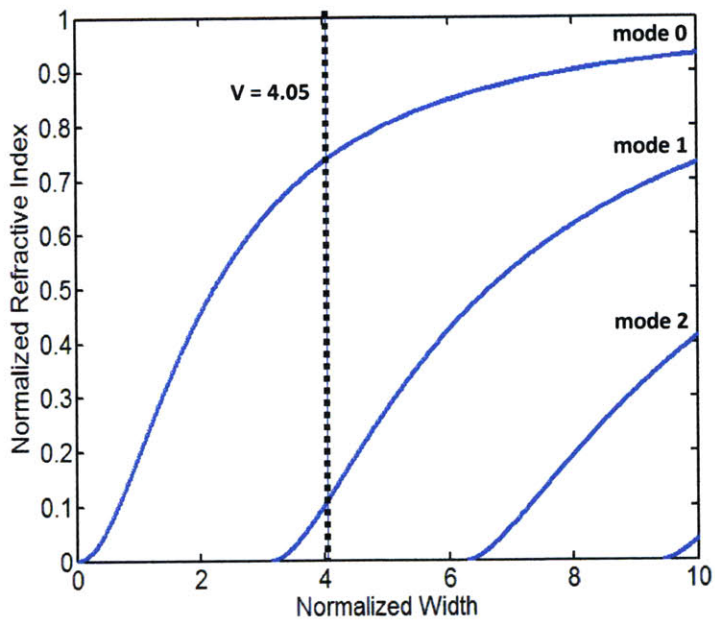


Figure A-2: Normalized width of an InP-InGaAsP-InP Wavguide

From the normalized effective index we can solve for the effective from:

$$n_{eff} = \sqrt{b(n_{core}^2 - n_{clad}^2) + n_{clad}^2} \qquad \text{A.4}$$

For our device the first order effective index is n_{eff} = 3.2. This process was used in the derivation of Figure 1-2 in Chapter 1.

Appendix B Recipe

The recipe outlined below was used to transfer shadow mask features of 1-2 µm into into InP-InGaAsP-InP with ±250nm precision. Fabrication steps in bold indicate critical processing steps for device fabrication. While underlined steps are a series of commands that are used repeatedly and referenced throughout the chapter.

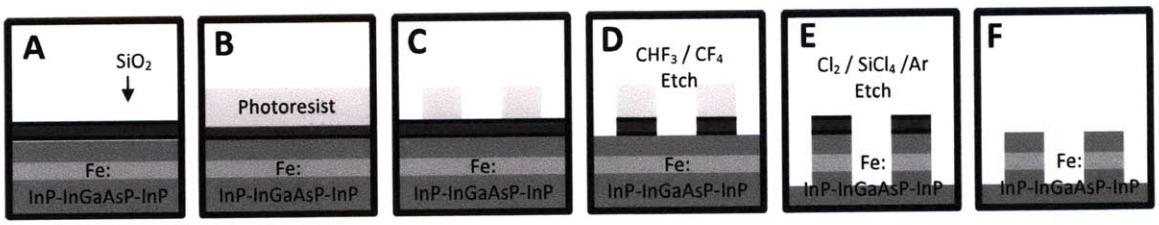


Figure B-1: InP Faraday Rotator Process Flow

B.1 Plasma Enhanced Chemical Vapor Deposition (PECVD)

1. Clean Wafers
    a. Hold wafer with tweezers over a small collection beaker/bowl
    b. Rinse wafer with acetone, methanol, and isopropanol and dry with compressed N_2
    c. Place wafers into a 120°C oven for 2 minutes to remove additional moisture on the surface

2. **Run a Deposition Rate Calibration** on the the STS systems PECVD tool in MTL MIT
   A silicon sample is run in the PECVD to calibrate the deposition rate of the tool on a given day
    a. Load Silicon wafer into load lock chamber
        i. Vent the Chamber by selecting 'Vent' from the Transfer window on the main panel (Figure B-2) and open the latch on the load lock chamber
        ii. Clean both sides of the carrier plate with an clean room wipe sprayed with isopropanol
        iii. Place dummy silicon wafer chip on the center of the carrier wafer
        iv. Close and Latch the load lock chamber
        v. Pump down the load lock chamber by selecting 'Pump + Map' from the Transfer window on the main panel (Figure B-2)

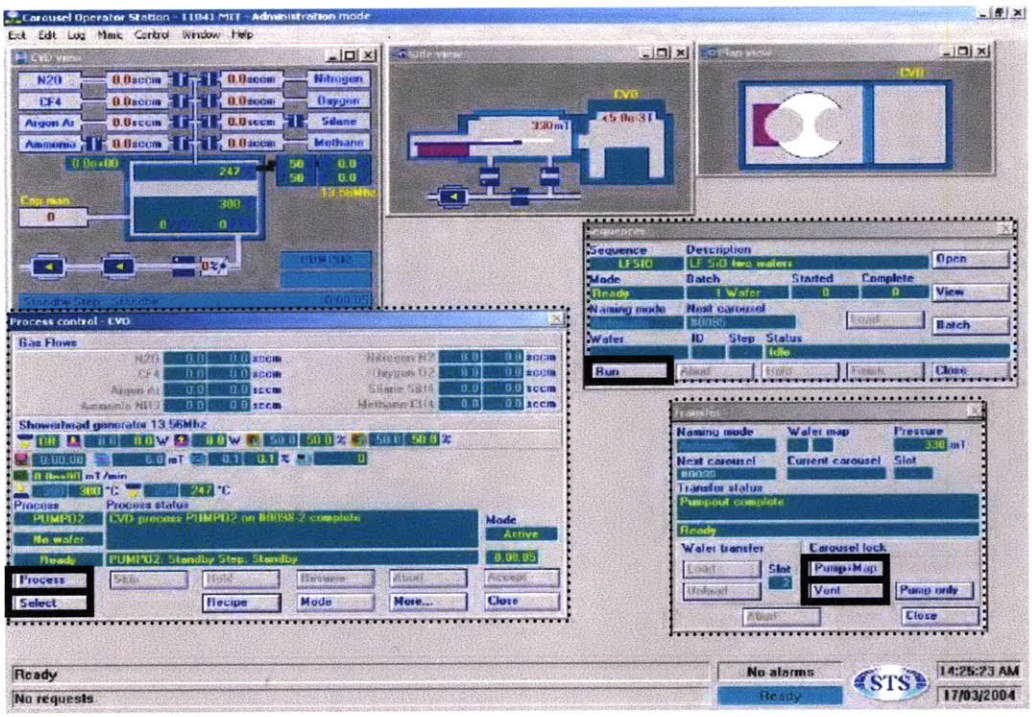


Figure B-2: PECVD Control Panel

b. Load LFSiO2 Recipe

   i. Load recipe by selecting 'Select' from the Process Control window on the main page(Figure B-2)

   ii. Select recipe 'LFSIO2' and Press OK

Table B-1: LFSIO2 Recipe in the STS-CVD Tool

General	Pressure	Temperature	Gases	R.F.
Pump Down Time: 20 sec	Trip: 1899 mTorr	Platen: 300C ± 10C	N_2O: 1420 ssccm Tolerance: 10%	RF: 380 kHz (showerhead only)
Gas Stabilization: 1 min	Process: 550 mTorr	Showerhead: 25C ± 10C	N_2: 392 ssccm Tolerance: 25%	Power: 60W
Process Time: Variable	Tolerance: 25%		SiH_4: 12 ssccm Tolerance: 25%	Tolerance: 25%
Pump Out Time: 10 sec				

c. **<u>Change Deposition Time in the Recipe</u>**

   i. Edit recipe by selecting 'Process' in the Process Control window of the main page (Figure B-2)

   ii. Select 'LFSIO2' from left hand side of the recipe edit window

   iii. Select the 'General' tab of the recipe edit window

   iv. In the 'Process Time' box, set time according to the etch rate

1. For the calibration etch set the time to 5 minutes [00:05:00]

v. Select the 'Recipe' drop down menu, Save and Close

d. **Start SiO_2 Deposition** on by selecting 'Run' in the Sequencer Window on the main page (Figure B-2)

e. Vent Camber and Remove Sample

3. **Measure SiO_2 Thickness** on the Silicon Wafer using the Nanospec 3000
   This device measures the thickness of the SiO_2 on Si substrate by monitoring the reflected power of the sample at various wavelengths
   a. Place the wafer on the tool stage and adjust the focus
   b. Press 'Measure'
4. From the thickness calculate the deposition rate of the STS-CVD tool

5. **Run a second Silicon wafer Calibration Run** on the STS-CVD to double check the etch rate using the process described in step 2 above
   Note: Step 2.b can be skipped the recipe has already been loaded into the tool
6. Measure SiO_2 on the second silicon calibration wafer using the process, as described in step 3
   a. Calculate the deposition time required for 250nm of SiO_2

7. **Deposit 250 nm of SiO_2 onto a Epitaxial Wafer**
   a. Load the epitaxial samples and a calibration Si wafer into the tool as described in step 2.a
   b. Adjust the deposition time in the LFSIO2 recipe (step 2.c) according to the value calculated in step 6.a
   c. Start SiO_2 Deposition on by selecting 'Run' in the Sequencer Window on the main page (Figure B-2)
   d. Vent Camber and Remove Sample
8. Measure SiO_2 deposited on the epitaxial wafers by on measuring the film thickness on the Si sample using the process described in step 3

B.2 Photolithography

Fabrication steps marked that are italicized indicate processing steps that are critical to obtaining flush contact between the mask and photoresist

9. Clean all Samples
   a. Hold samples with tweezers over a small collection beaker/bowl
   b. Rinse samples with acetone, methanol, and isopropanol and dry with compressed N_2
   c. Place samples into a 120°C oven for 2 minutes to remove additional moisture on the surface

10. Coat Epitaxial samples with HMDS

a. Place samples into aluminum foil trays and place inside the HMDS oven in MTL TRL facility
b. Select 'Recipe 5'with the thumb dial on the front of the oven
c. Start the recipe by pressing the red 'Run' button
   After ~25 minutes the tool will beep loudly indicating the recipe is over
   d. Press 'Reset' to stop the buzzing and Remove Samples

11. Spin Coat wafers with Clariant AZ-5214E

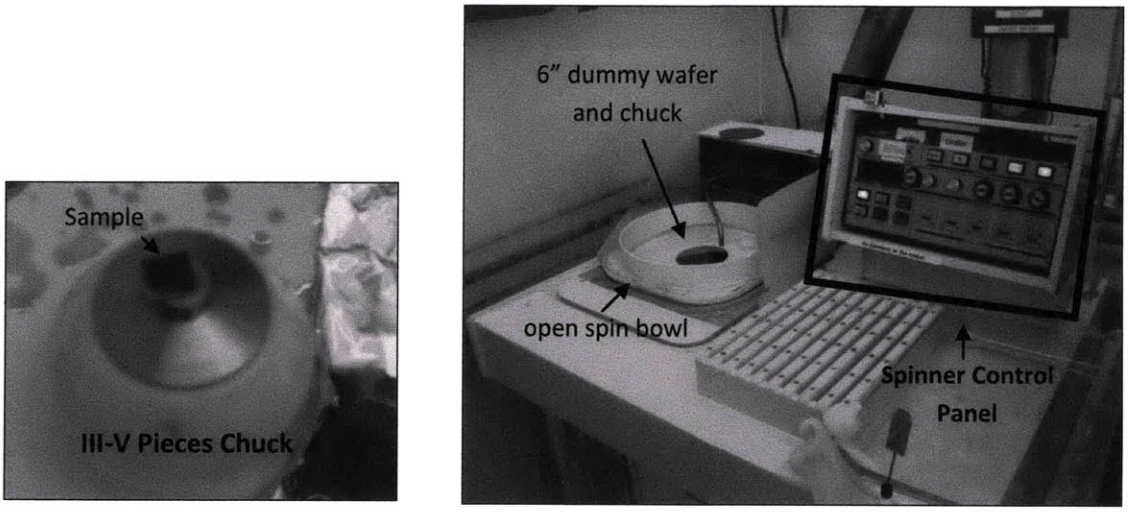


Figure B-3: Photoresist Spinner

a. Remove dummy wafer from the spinner (Figure B-3)
   i. Press 'Vacuum' on the spinner control panel to release the vacuum
   ii. Gently lift the 6" silicon wafer with your hand or tweezers
   iii. Remove 6" vacuum check by pulling up on the vacuum mount with both hands
   iv. Return 6" chuck to the rack
b. Attach III-V pieces chuck to the spinner (Figure B-3)
   i. Select the smallest spinner chuck from the chuck rack
   ii. Center the chuck on the vacuum spindle and press down
c. Using tweezers place an InP sample in the center of the spinner vacuum chuck
d. Press 'Vacuum' on the spinner control panel to engage the vacuum
e. **Setup Spin Coater**
   i. Ensure that Dispense, Spread, and Spin mode are ON by checking the lights above each dial
      Note: Only 2 modes are ON in Figure B-3
   ii. Set the times below to the dials to 30 secs, to allow time to adjust the spin speeds
   iii. Press 'Start'

iv. Adjust the knobs on the right of the control panel to set the spin rate in each mode to the following values: (note: this process may have to be repeated a get the correct times)
   - **Dispense: 500 rpm**
   - **Spread: 750 rpm**
   - **Spin: 4000 prm**

v. Set the time below each setting to the following values:
   - **Dispense: 3 seconds**
   - **Spread: 6 seconds**
   - **Spin: 30 seconds**

vi. **Set the resist type to AZ-5214E** using the knob in the top left hand corner of the spin coater and set the dispense mode to 'Auto'

vii. *Press 'Start' and allow the AZ-5214E to run out into the bowl, this will remove any particles that may have accumulated in or around the photoresist dispense nozzle*

f. *Spray the sample attached to the vacuum chuck with compressed N_2 to remove particulates from the surface*

g. Press 'Start' to coat the wafers with AZ-5214E

i. *Allow the resist to drop into the bowl for 0.5 second before centering the nozzle over the wafer. Push the nozzle away from the wafer before the last drops. This prevents particles generated by the start and stop of resist flow from landing on the resist.*

12. ***Remove Edge Bead*** from the sample while it is still on the spinner vacuum chuck
    a. *Take a small swab and soak it with acetone*
    b. *Shake swab to remove loss liquid*
    c. *Slowly wipe around the outside edge of the sample to remove the edge bead, be careful not let the acetone wrap around the front of the sample*
    d. *Press 'Vacuum' to disengage the vacuum chuck and slowly pull the sample off the chuck with a piece of tweezers*
    e. *Gently wipe the resist from the back of the sample (it is not necessary to remove all the resist on the back at this stage)*
13. Place the coated sample into a aluminum tray
14. Repeat steps 11.c - 12.e (skipping step 11.e) until all of the samples have been coated
15. Clean the Spin coater:
    a. Removal all resist from inside the bowl with acetone
    b. Remove the III-V pieces chuck and replace large vacuum chuck and 6" silicon wafer
    c. Press 'Vacuum' to engage the system

16. Pre-Bake samples for 25 minutes in a 95°C Oven

a. Place each tray into then oven

b. *Place a sheet of aluminum foil over trays within the oven, to prevent particles from falling onto the resist*

17. Remove Samples from the oven
18. ***Inspect each sample for photoresist around the edges and back of the sample***
    a. *Remove any resist found on the sample with an acetone soaked swab, being careful to let the acetone remove the resist on the front of the wafer*
19. **<u>Clean the Shadow Mask</u>**
    a. Place the 6" Mask into a 6" wafer holder and place it over a collection beaker/bowl
    b. Rinse the chrome side of the sample with acetone with scrubbing it with a wide swab
    c. Rinse with the chrome side with methanol, and isopropanol
    d. Air dry with compressed N_2 starting at the center of the mask to prevent streaking
    e. Clean the non-chrome side by repeating steps 19.a – 19.d

20. **Expose Wafers in the Karl Süss MA6**
    a. Load the mask chrome side down into the MA6
    b. **Setup the Exposure Tool:**
        i. **Set the Mode to: *vacuum contact* with**
        ii. **Set the Exposure Time to 37 seconds**
        iii. Set the other exposure parameters listed in

Table B-2: Contact Exposure Parameters

Alignment Gap:	10 µm
WEC Pressure:	1.0
Vacuum Chamber:	0.8
Pressure Vacuum:	10 sec
Full Vacuum:	10 sec
Vacuum Purge:	10 sec

    c. **Press 'Load'**, the system will walk you through the process of opening load tray and when to place the wafer
    d. Center the wafer on the 4 vacuum holes in the center of the wafer chuck
    e. Close the wafer tray, this is will put the tool into alignment mode
    f. **Using the micrometers at the edge of the wafer stage rotate and align the sample with the mask** (note: alignment is used to the waveguides orthogonal to the edges of the sample, and set the offset for HWP)
    g. **Press 'Expose'**, after exposure is complete the wafer will be lowered from the mask and it can be removed
    h. Remove the sample with tweezers and place it into a fluoroware container
    i. Repeat the process until all of the samples have been exposed
        i. Clean the masks every 2 exposures to remove stuck on resist using the process described in step 19

21. Remove the shadow mask from the Karl Süss MA6

22. Clean Mask as described in step 19 and put it away

23. Develop samples in Clariant AZ-422 resist developer

a. Pour AZ-422 into a small beaker
b. Fill a large beaker with DI water
c. Using tweezers place a sample into the AZ-422
d. Agitate the beak until the sample clears, approximately 90 seconds
e. Quickly remove the sample with tweezers and rinse in the DI water
f. Air dry with compressed N_2

24. Visually inspect the wafers under a microscope to ensure all the resist has been removed

B.3 Reactive Ion Etching (RIE)

25. Load and Run 'New Clean' recipe on the Plasmatherm 790 series to **Precondition the Chamber**

a. Select 'Process' from the toolbar at the top of the control window (Figure B-4)

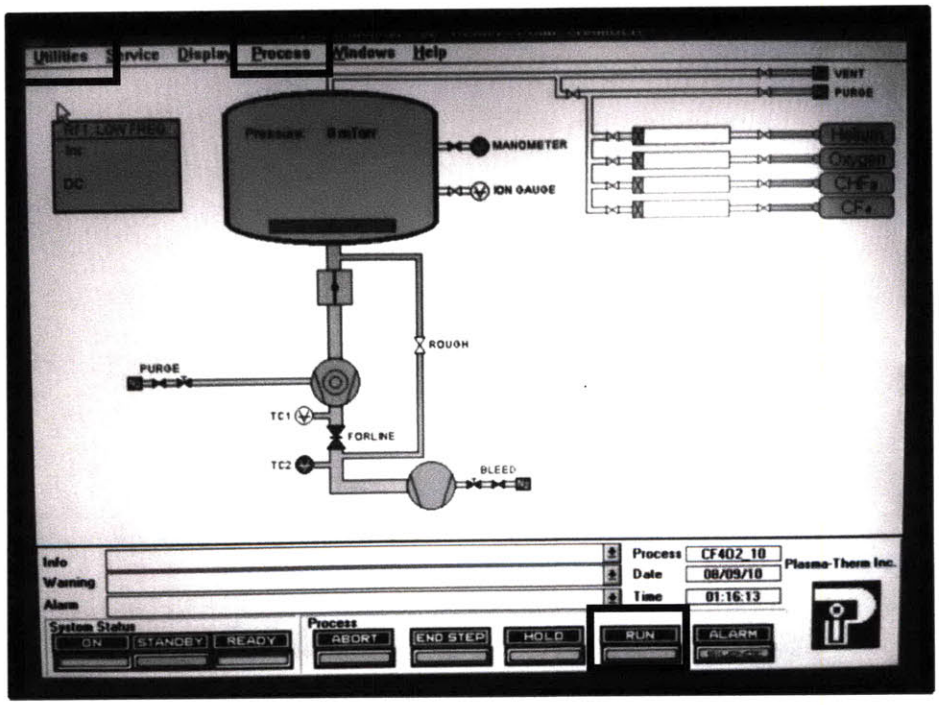


Figure B-4: RIE Control Screen

b. Open 'New Clean' recipe from the pop-up menu

Table B-3: New Clean Recipe

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time:	30 sec	5 sec	5 min
Gas (sccm):	O_2 : 20 CF_4: 4	O_2 : 20 CF_4: 4	O_2 : 20 CF_4: 4
DC Voltage:	0 V	300 V	300 V
Pressure:	20 mTorr	20 mTorr	20 mTorr

c. Press 'Run' on the front screen to run the recipe

26. Vacuum Cure the Resist

a. Vent the Chamber by selecting 'Vent' from the 'Utilities' drop down menu
b. Place samples in the center of the platen
c. Pump down the Chamber by selecting 'Turbo Pump' from the 'Utilities' drop down menu
d. Hold the top down until the tubro pump starts
e. Wait for 12-20 minutes to cure the resist

27. Etch SiO_2 in a combination CHF_3 / CF_4 chemistry

a. Select 'Process' from the toolbar at the top of the control window (Figure B-4)
b. Open and Run 'Oxide' from the pop-up menu

Table B-4: Oxide Recipe

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch	Step 4: Flow Gases	Step 5: Spark Plasma	Step 6: Etch
Time:	45 sec	5 sec	6 min	1 min	5 sec	7 min
Gas (sccm):	CHF_3 : 15	CHF_3 : 15	CHF_3 : 15	CF_4 : 15	CF_4 : 15	CF_4 : 15
DC Voltage:	0 V	200 V	200 V	0 V	200 V	200 V
Pressure:	15 mTorr	15 mTorr	10 mTorr	10mTorr	15mTorr	10 mTorr

c. Repeat Etch
   i. With an etch rate of 10 nm/min and 250 nm of SiO_2 to remove, 26 minutes of etch time should be sufficient
   ii. Check sample color to ensure the SiO_2 is etched through
d. Vent Chamber and Remove Sample
e. Check Sample color to ensure the SiO_2 is etched through

   SiO_2 reflects a different color according to the thickness of the resist, shifting from purple to blue after the addition of 25 nm of SiO_2.

28. Remove Photoresist

a. Soak samples in Acetone bath for 10 minutes
   i. Agate beaker on occasion to improve resist removal
b. Hold acetone bath containing the samples within an ultra-sonic bath for 30 seconds (Figure B-5) to loosen stuck on resist
c. Rinse samples with Methanol and Isopropanol before drying with compressed N_2
d. Ash in Oxygen plasma for 15 minutes to remove remaining organics from the surface
e. Inspect the surface under a microscope to ensure all of the photoresist has been removed

Figure B-5: Ultra-Sonic

B.4 Inductive Coupled Plasma Reactive Ion Etching (ICP RIE)

The recipe outlined below was used to fabricate InP-InGaAsP-InP faraday rotators tested in Chapter 5. Fabrication steps in bold indicate critical processing steps for device fabrication. While underlined steps are a series of commands that are used repeatedly and referenced later in recipe.

29. Load and Run profile 1 on the Julabo circulator.
30. This will bring the SAMCO ICP RIE-200iP etcher chuck temperature up to 220°C over 30 mins. The system will remain at 220°C for 8 hours before returning to room temperature.
31. Open the Chlorine and $SiCl_4$ gas canisters located in the gas the cabinet behind the ICP etcher. Then open the main gas lines by pushing the button above the gas cabinet.
32. Access the run history on the ICP RIE laptop and ensure the 'Post Clean' (Recipe 0) was run. If not, run it was not run now.
33. <u>Run</u> PreClean <u>(Recipe 1) on ICP RIE etcher</u>
    a. At the touchscreen control panel, press 'Set' in the top left corner of the screen. This will open the Control page.

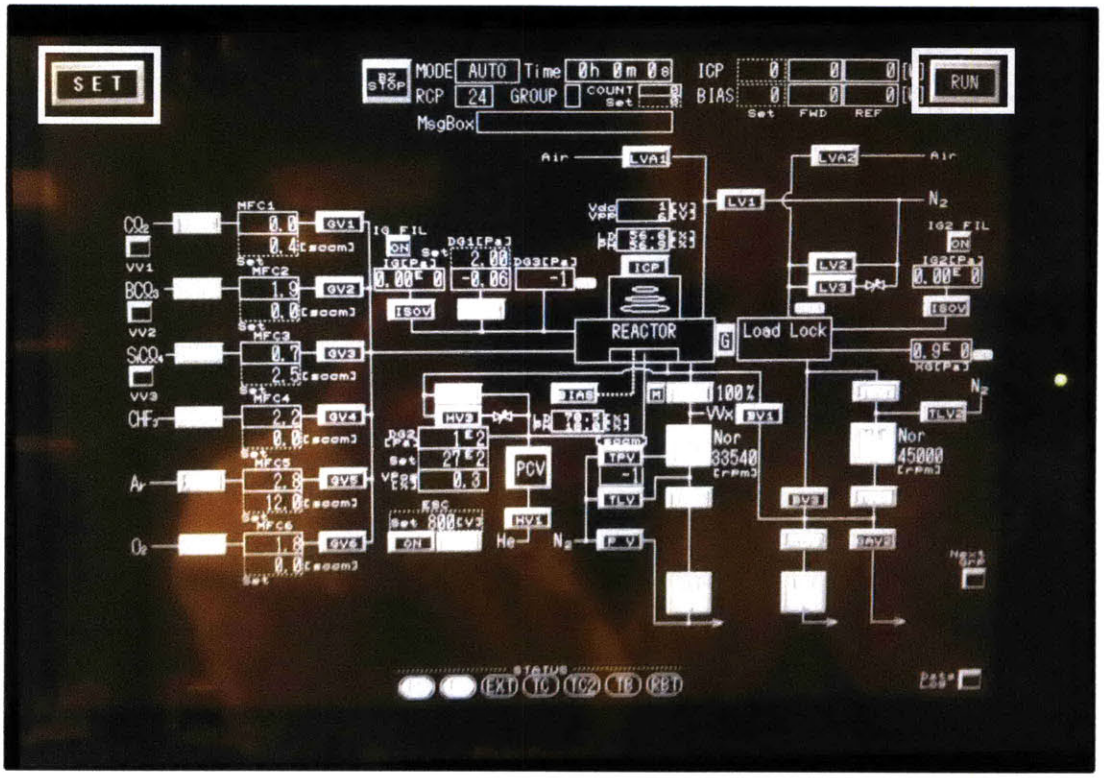


Figure B-6: ICP RIE Main Window

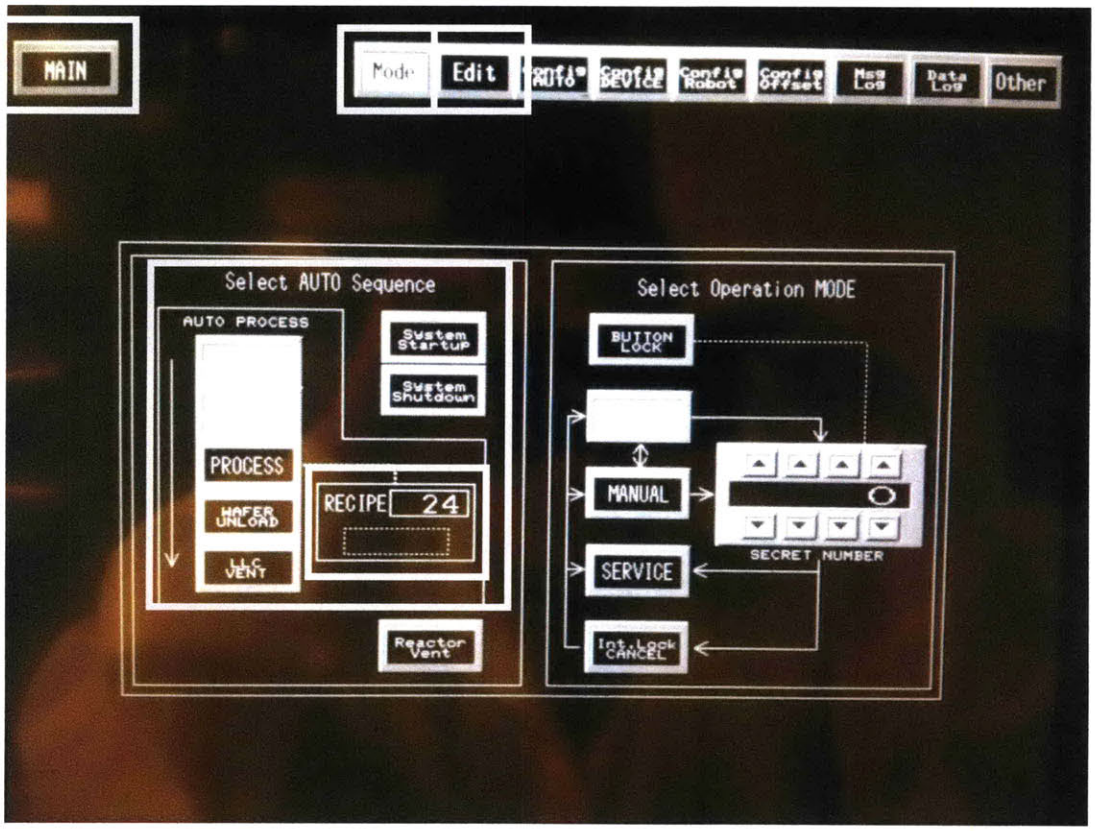


Figure B-7: ICP RIE Control Screen

b. Touch the number under recipe and spin the large dial to set the value to 1, for the pre-clean recipe. Press the physical 'Set' button to lock in the value.
c. Assuming the ceramic carrier wafer for cleaning was previously loaded into the etching chamber. Highlight 'Process', 'Wafer Unload', and 'LLC Vent', then press 'Main' to return to the main screen (Figure B-7)
d. Press and HOLD 'Run' for 5 seconds until it beeps twice to start the process.
e. At the completion of the recipe the tool will beep.

34. Remove ceramic carrier wafer designated for chamber cleaning
35. This wafer is to used for cleaning purposes only, and will be placed back into the tool after all III-V etching is complete

36. Condition the Chamber – Part I: Flow Gases

37. By allowing the gases to flow into the chamber and spark without the presence of a wafer, preconditioning will prime the gas lines, and place an initial coating of $SiCl_4$ and Cl_2 radicals on the interior walls of the etching chamber
    a. Load the SAMCO ceramic carrier wafer designated for InP recipes into the etching chamber of the ICP RIE
    b. A separate carrier wafer is used for every material set to prevent contamination.
        i. Open the load lock chamber and place the wafer into the mechanical arm.
        ii. Close the lid to the load lock chamber
        iii. Access the Control screen by pressing 'Set' in the top right corner of the main touchscreen.
        iv. Highlight 'LLC Pump Down', 'Wafer Load', then press 'Menu' to return to the main screen.
        v. Press and HOLD 'Run' for 5 seconds until it beeps twice.
        vi. At the completion of the process the tool will beep.
    c. Load the following recipe in the ICP RIE 'Recipe' page (Figure B-8)

Table B-5: Precondition Recipe

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time	2 mins	10 sec	**10 mins**
Gas: Cl_2	0.4 sccm	0.4 sccm	0.4 sccm
Gas: $SiCl_4$	2.5 sccm	2.5 sccm	2.5 sccm
Gas: Ar	12 sccm	12 sccm	12 sccm
ICP Power	0 W	200 W	150 W
Bias Power	0 W	200 W	150 W
Pressure	~15 mTorr (set gate to 27%)	~15 mTorr (set gate to 27%)	2.25 Torr

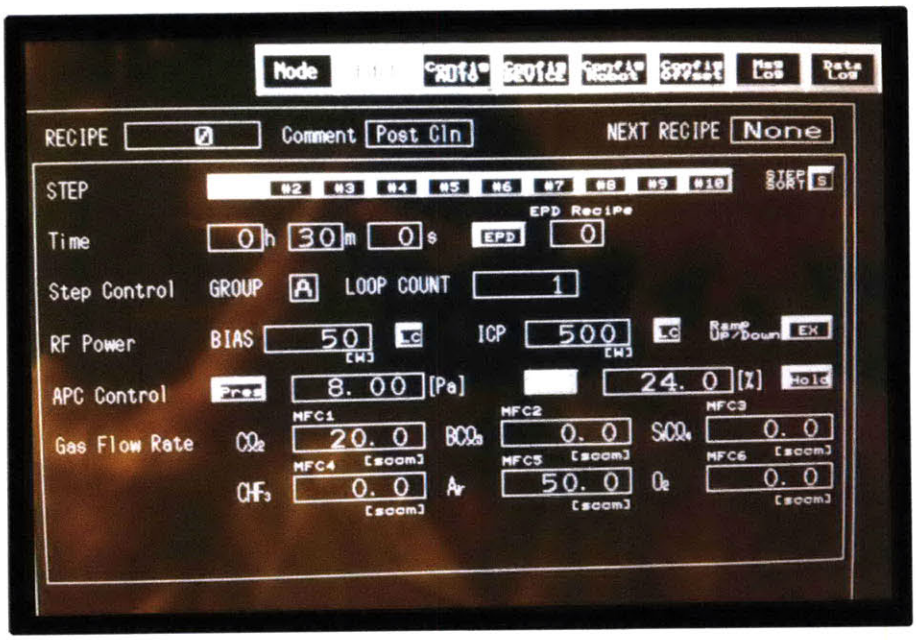


Figure B-8: ICP RIE Recipe Screen

i. Access the Recipe Screen by pressing 'Edit' from the Control touch screen
ii. Press 1, to access step one and press the physical 'Set' button
iii. Press the region to the left of Cl_2, and set the value using the spin dial, and lock by pressing 'Set'
iv. Continue this process for each of the parameters in the table and then repeat for each successive step until the recipe complete.
v. Define a Recipe # in the top box and set by pressing 'Set'

d. Run Recipe # by setting on the XYX screen as described in step 33
e. After etching, remove the ceramic carrier wafer from the load lock

38. Condition the Chamber – Part II: Etch InP dummy wafer

39. Etching of a InP sample before the epitaxial wafer will add InP radicals to the plasma and chamber walls which helps reduce $InCl_x$ micromasking in later etches.

a. Adhere InP dummy wafer to ceramic carrier using Apiezon H vacuum grease
   i. Squeeze grease onto a glass slide
   ii. Collect vacuum grease on the end on swab stick by rolling around the end of the rob
   iii. Dab and smear the vacuum grease across onto the back of the sample while holding it carefully in a set of tweezers

      Warning: The vacuum grease behaves like taffy creating long strings when pulled away, be careful not to let the strings fall onto the face of the InP sample wafer

   iv. Transfer the sample onto ceramic carrier wafer with a clean set of tweezers

v. Carefully push the InP sample down on all four corners until it is flush against the ceramic carrier wafer
vi. Gently grab the edge of the sample and move it around to ensure a uniform coating on the backside of the InP sample wafer
vii. Remove excess vacuum grease from around the sample by collecting it on the end of a swab stick. DO NOT wipe the surface of the InP sample with any form of solvents such as trichloroethylene, acetone, methanol, or isopropanol in an attempt to remove vacuum grease. This will simply smug the grease across the face of the InP wafer. If too much vacuum grease has accumulated on the face of the InP sample, remove the sample from the ceramic carrier wafer, clean both wafer as described in step e and begin vacuum grease application again.

b. Load the ceramic carrier wafer and InP sample into the etching chamber, as described in step 37.a
c. Load and Run the following recipe, refer to steps 37.c and 33 respectively for step by step instructions.

Table B-6: ICP RIE Etch Recipe

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time	2 mins	10 sec	3 mins
Gas: Cl_2	0.4 sccm	0.4 sccm	0.4 sccm
Gas: $SiCl_4$	2.5 sccm	2.5 sccm	2.5 sccm
Gas: Ar	12 sccm	12 sccm	12 sccm
ICP Power	0 W	200 W	150 W
Bias Power	0 W	200 W	150 W
Pressure	~15 mTorr (set gate to 27%)	~15 mTorr (set gate to 27%)	2.25 mTorr

d. Remove the ceramic carrier wafer from the ICP RIE load lock
    i. Note: Excess vacuum grease on the carrier wafer will appear black after etching.
e. <u>Clean the InP sample and ceramic carrier wafer</u>
    ii. Remove the InP sample with tweezers and place it in trichloroethylene bath
    iii. Scrub the ceramic carrier wafer with a swab trichloroethylene then rinse with acetone, methanol, and isopropanol and dry with compressed N_2
    iv. Gently wipe the back and top of the InP sample with a swab soaked in trichloroethylene
        1. Warning: Be careful not to crush the newly etched waveguides on the surface of the InP wafer
    v. Rinse sample with acetone, methanol, and isopropanol and dry with compressed N_2

40. Etch Epitaxial Wafer in the ICP RIE etcher

a. Adhere the epitaxial wafer to ceramic carrier wafer with Apiezon H vacuum grease as described in step 39.a

b. Load the ceramic carrier wafer and epitaxial sample into SAMCO ICP RIE etching chamber, as described in step 37.a
c. Load and Run the following recipe, refer to steps 37.c and 33 respectively for step by step instructions.

Table B-7: ICP RIE Etch Recipe

	Step 1: Flow Gases	Step 2: Spark Plasma	Step 3: Etch
Time	2 mins	10 sec	3 mins
Gas: Cl_2	0.4 sccm	0.4 sccm	0.4 sccm
Gas: $SiCl_4$	2.5 sccm	2.5 sccm	2.5 sccm
Gas: Ar	12 sccm	12 sccm	12 sccm
ICP Power	0 W	200 W	150 W
Bias Power	0 W	200 W	150 W
Pressure	~15 mTorr (set gate to 27%)	~15 mTorr (set gate to 27%)	2.25 mTorr

41.

d. Remove the ceramic carrier wafer and epitaxial wafer from the ICP RIE load lock
e. Clean the epitaxial sample and ceramic carrier wafer as described in step e
    i. Run any additional etches using the process outlined in step 40
    ii. Load the SAMCO ceramic carrier wafer designated for cleaning into the etching chamber of the ICP RIE
    iii. Run the 'Post Clean' (Recipe 0) on the ICP RIE
    iv. This is a 6 hours etch recipe consisting of high power oxygen, chlorine, and argon plasma to remove particulates within the chamber.

42. Remove SiO_2 hardmask from the Epitaxial sample

a. After donning personal protective equipment pour a small amount of buffered hydrofluoric acid (7:1 concentration) into a plastic or ceramic bowl
b. Carefully place the epitaxial wafer into the liquid bath
c. Soak and agitate the sample for 4 minutes
d. Remove the sample and thoroughly rinse the in DI water at least 1 minute
e. Clean all tools and containers, then put away personal protective equipment

Appendix C Photolithography: Negative Profile Recipes

During process development dual layer Al_2O_3 and SiO_2 were explored for RIE and ICP RIE etching. The aluminum oxide was patterned using lift off with from a negative resist profile. In this appendix we provide the process recipes used to produce negative resist profiles with ±350 nm linewidth errors. During develop vertical recipes for Clariant AZ-5214E in image reversal mode and Futurex NR7-1500PY, both recipes are provided below.

C.1 Clariant AZ-5214E : Image Reversal Recipe

1. All wafers were rinsed with acetone, methanol, and isopropanol then baked in 120C oven for 2 minutes before being places in the HMDS
2. HMDS Oven: Recipe #5
3. Spin Coater:
   - Dispense: 500 rpms for 3 seconds
   - Spread: 750 rpms for 6 seconds
   - Spin: 4000 rpms for 30 seconds
   - Ensure to blow off the samples before coating
4. Remove Edge Bead: wipe the edge of the samples with an acetone soaked swab
5. Pre-Bake: in a 95°C for 25 min
6. Remove Edge Bead (recheck): Clean the back of the wafer really well with an acetone swab to help improve contact
7. Exposure in the MA6
   a. Settings: Vac Contact, Time settings all 10 sec
   b. Exposure Time: 25 seconds :: Dose: 275 mJ/cm^2
8. Image Reversal Bake: Hotplate (on a glass slide) at 110C for 50 secs
9. Flood Exposure: Exposure Time: 90 sec
10. Develop for ~90 sec in AZ-422 until cleared (develop time is not a critical parameter)

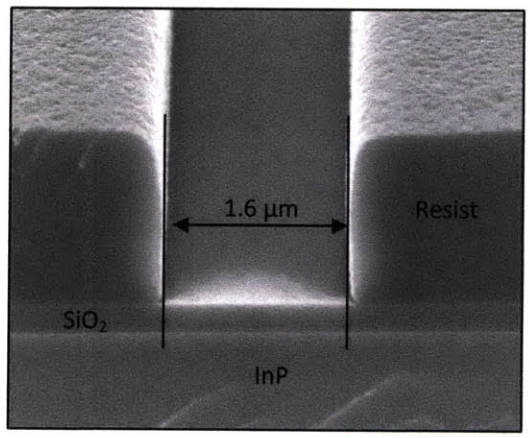


Figure C-1: AZ-5214E (IR) profile

C.2 Futurex NR7-1500PY: Negative Resist

11. All wafers were rinsed with acetone, methanol, and isopropanol then baked in 120C oven for 2 minutes before being places in the HMDS
12. HMDS Oven: Recipe #5
13. Spin Coater:
    - Dispense resist manually with a syringe on a stationary sample
    - Spread: 750 rpms for 6 seconds
    - Spin: 5000 rpms for 40 seconds
    - Ensure to blow off the samples before coating
14. Remove Edge Bead: wipe the edge of the samples with an acetone soaked swab
15. Pre-Bake: Hotplate (no foil) at 150C for 60 secs
16. Exposure on the ElectroVision LC1
    a. Settings: Manual Top Side; Transparent ; Cosntant dose; Vacuum Contact
    b. **Dose: 250 mJ/cm^2** : Total Exposure Time: ~60 sec (measured)
17. Bake: Hotplate (no foil) at 100C for 120 sec
18. Develop for ~10 sec in RD6 until cleared

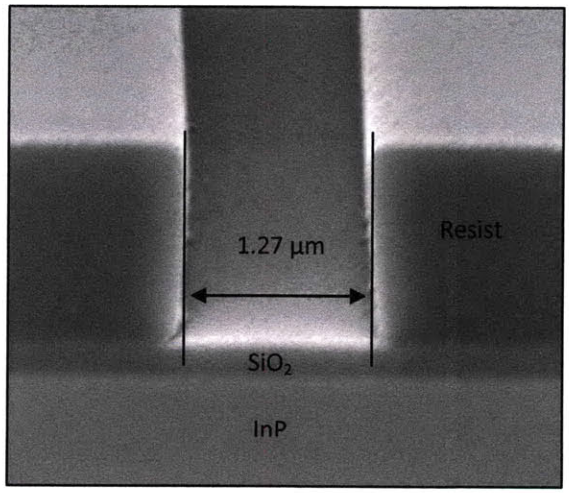


Figure C-2: Futurex NR7-1500PY Resist Profile

Appendix D Plasma Enhance Chemical Vapor Deposition

Device fabrication begins with a uniform deposition of SiO_2 across the wafer via plasma enhanced chemical vapor deposition (PECVD). PECVD, like RIE, uses radial ions generated within a RF plasma to produce chemical reactions on the surface of the wafer. The growth of SiO_2 occurs when silane(SiH_4) and nitrous oxide(N_2O) react to form SiO_2 and N_2 and H_2. The highly volatile mixture of SiH_4 and O_2 will produce a SiO_2 film independent of the plasma, quickly coating the chamber and device with SiO_2 when combined. By replacing O_2 with N_2O, the point of reaction can be controlled by the RF electric field. [**61**]

Before deposition particulates were removed from the wafer by rinsing it with acetone, methanol, and isopropanol, being blown dry with N_2, and baking it for 2 minutes at 120°C. The sample was then placed on a carrier wafer and loaded into the deposition chamber of the STS-CVD. Just as in RIE etching, PECVD is dependent on plate power, chamber pressure, gas compositions, and plasma frequency. The chamber settings listed in Table D-1 generate a disposition rate of ~70nm/min. The photonic devices in this thesis required a 2μm etch of InP in a $SiCl_4/Ar/Cl_2$ plasma. The selectivity of 1_{SiO2} : 25_{InP} in this chemistry establishes a minimum SiO_2 thickness of 80nm. Although the selectivity was improved to allow for a thinner SiO_2 hardmask, the thickness of 250nm was grandfathered into the process. A deposition time of 3.5 minutes was used deposit ~250 nm of SiO_2 onto the wafer.

Table D-1: PECVD SiO_2 Deposition Parameters

Gas Flow Rate: SiH_4	12 sccm
Gas Flow Rate: N_2O	1420 sccm
Gas Flow Rate: N_2	392 sccm
Power	60 W
Pressure	550 mTorr
Frequency	380 kHz

Verification of the SiO_2 thickness was performed through visual inspection and reflectivity. Variation in the SiO_2 thickness as little as 25 nm can be observed by changes in the surface color. A 250 nm film appears gold, while 275 nm is bright purple. By matching the surface color to a SiO_2 thickness vs color tabel, one can easily determine the approximate film thickness on the wafer. Another nondestructive measurement of the dielectric film thickness is reflectometry. This technique monitors the changes in reflected power verses wavelength in order to determine the thickness of the film. This measurement is dependent on the refractive index of the substrate and film, so is dependent on the materials being measured. The Nanospec 3000 measures the SiO_2 thickness on a silicon wafers. Thus a silicon dummy wafer is included in every deposition to test the dielectric thickness after processing. Comparison of reflectometry measurements, visual observation, and destructive measurements taken later with a scanning electron microscope confirm the resist thickness – produce consistent results.

It is important to note that variability in gas flow and pressure within the chamber can generate drastically different disposition rates from week to week. To ensure proper thickness test runs should be done before the sample to establish today's disposition rate. The process used for PECVD deposition in this thesis, is outlined in Appendix B.

Appendix E Matlab Source Code

This appendix includes all of the Matlab code used within this thesis.

E.1 Chapter 1 Theory Figures

ThesisMe

```
%Setting for Air cladding

flag = 1;

%% 1D Waveguides

%Constants
ko = (2*pi)./1550e-9; %wave vector in a vaccum given lambda = 1550 nm
nclad = 3.14; %index of refraction for the cladding:  n of InP = 3.14
ncore = 3.22; %index of refraction for the core: n of InGaAP = 3.22


%% Part I:  Generate loss*d vs kx*d
%The interesections tell you what values of kx*d and loss*d are true for
%each mode, this function is dependent on d!

d = 1.4e-6;  %waveguide width

if(flag == 2)

kxd = [0:0.01*pi:6*pi];  %random selection of kx*d values as a starting point

V = ko.*d.*sqrt(ncore^2-nclad^2);  %normalized width determined by system
constants
loss1 = sqrt(V.^2 - kxd.^2);  %loss# is really loss*d

%TE Modes
loss2 = kxd.*tan(kxd); %even modes
loss3 = -kxd.*cot(kxd); %odd modes

% TM Modes
%TMfact = (nclad/ncore)^2;
%loss2 = TMfact.*kxd.*tan(kxd); %even
%loss3 = -TMfact.*kxd.*cot(kxd); %odd

% Plot Functions
figure(1);

plot(kxd,loss1); hold on;
plot(kxd,loss2, '-- r');
plot(kxd,loss3, '-. k');

title('TE Modes (1D) [ncore = 3.22 nclad = 3.14  d = 1.4 um  lambda = 1550
nm]');
xlabel('k_x*d (radians)');
ylabel('loss*d (radians)');
```

```
xlim([0 5]); ylim([0 5]);

end

%% Part II:  Generate V vs b (normalized parameters)
%Generates a master graph of all possible values of normalized width (V)
%vs b

if(flag == 2)

b = [0:1e-3:0.99]; %NOTE: V(b=1) = Inf, so the range goes to 0.99
    % b = (neff^2 - nclad^2)./(ncore^2 - nclad^2)

m = 0; %mode
a = 0;
    %a =(ncl.^2-ncu^2)./(ncu^2-ncl^2)
    %where ncl = nclad_lower   and ncu = nclad_upper
    %a=0 for sysmetric waveguides

V = (m*pi + atan(sqrt(b./(1-b)))+ atan(sqrt((a+b)./(1-b))))./sqrt(1-b);
    %V = normalized width this allows for easier calculation d and beta

%Plot function
figure(2);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(V, b,'LineWidth',2); %nomalized width vs normalized b
hold on;
title('V vs b'); xlabel('V'); ylabel('b');
xlim([0 25]);  %NOTE: good zoom point at xlim([0 15]), but can't see Vair

%Plot other parameters (ie V at m = [0:1:10], a=[0:1:10] and all combination)
PlotVvsb(b);

%Plot Critical Points(ie: what happens at d = 1.4e-6? .. aka how many modes
etc)
ncore = 3.22; %index of refraction for the core: n of InGaAP = 3.22
%d = 1.4e-6;
d = 1e-6;

%Air Clad Waveguide
nclad = 1.00;
Vair = ko.*d.*sqrt(ncore^2-nclad^2);

%InP Clad Waveguide
nclad = 3.14; %index of refraction for the cladding:  n of InP = 3.14
Vinp = ko.*d.*sqrt(ncore^2-nclad^2);

%plot(Vair,b,' -- k');
plot(Vinp,b,'-. k');

end
```

```
%% Part III: Plot beta vs d
%Given a d (waveguide width), solve for beta (propgation constant)


d = [1e-6:1e-9:2e-6]; %Select a range of waveguide widths

if(flag == 2)
%d = [0.5e-6:1e-9:3e-6]; %Select a range of waveguide widths


% EPI CLADDING

%Set waveguide material parameters
nclad = 3.14; %index of refraction for the cladding:  n of InP = 3.14
ncore = 3.22; %index of refraction for the core: n of InGaAP = 3.22

%NOTE: only 2 modes for a waveguide with the above parameters

%Solve for V
V = ko.*d.*sqrt(ncore^2-nclad^2);

%Find b from the the normalized V equations (see Part II)
b0 = Find_b(V,0); %b for mode = 0
b1 = Find_b(V,1); %b for mode = 1
%b2 = Find_b(V,2); %b for mode = 2

%Solve for neff from the defnition of b = (neff.^2-nclad^2)./(ncore^2-
nclad^2);
neff0 = sqrt(b0.*(ncore^2-nclad^2)+ nclad^2);
neff1 = sqrt(b1.*(ncore^2-nclad^2)+ nclad^2);
%neff2 = sqrt(b2.*(ncore^2-nclad^2)+ nclad^2);


%Solve for beta from the definition of beta = ko*neff
beta0 = ko*neff0;
beta1 = ko*neff1;



if(flag == 1)
% AIR CLADDING

%Set waveguide material parameters
nclad = 1.00; %index of refraction for the cladding:  n of InP = 3.14
ncore = 3.22; %index of refraction for the core: n of InGaAP = 3.22

%NOTE: only 2 modes for a waveguide with the above parameters

%Solve for V
V = ko.*d.*sqrt(ncore^2-nclad^2);
```

```
%Find b from the the normalized V equations (see Part II)
b0a = Find_b(V,0); %b for mode = 0
b1a = Find_b(V,1); %b for mode = 1

%Solve for neff from the defnition of b = (neff.^2-nclad^2)./(ncore^2-
nclad^2);
neff0a = sqrt(b0a.*(ncore^2-nclad^2)+ nclad^2);
neff1a = sqrt(b1a.*(ncore^2-nclad^2)+ nclad^2);

%Solve for beta from the definition of beta = ko*neff
beta0a = ko*neff0a;
beta1a = ko*neff1a;

end

figure(3);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(d*1e6 ,neff0, 'r','LineWidth',2); hold on;
plot(d*1e6 ,neff1, 'b','LineWidth',2);
%plot(d*1e6 ,neff2, '-- b','LineWidth',2);

plot(d*1e6, 3.22, 'k');
plot(d*1e6, 3.14, 'k');

%title('1D Waveguide: Waveguide Width vs Propagation Constant');
xlabel('Waveguide Width (um)');
ylabel('Effective Index of Refraction');

%Idea: You should be able to draw a limit line across this plot - not all
%modes can exist in the waveguide ... it is dependent on the indices and
%dimensions, see critical point lines in Part II.  For example of nclad =
%3.14 if you plot modes 3 and 4 you get garbage because they don't exist
%until d = ??.  The limit line should make this apparent.

end

%% Mach Zender Interformeter
% This section examines the effect of different arm lengths (deltaL) and
%widths (deltaD) on the progation constant(beta)

if (flag == 2)

% MODE = 0 EPI

%Waveguide Parameters
beta = beta0;

A = 1; %amplitude in arm A (assumed)
La = 1e-3; %length of arm A (assumed)
betaA = beta(401);
```

```
    %for d = [1e-6:1e-9:2e-6], d(401) = 1.4 um
    % for d = [1.3e-6:1e-12:1.5e-6]; , d(996) = 1.4 um
deltaD = d(401) - d;

%We will vary the parameters of arm B
B = 1; %amplitude in arm B (assumed)

%Keep beta constant and vary L
betaB = betaA;
Lb = [(La - 1e-6):0.01e-6:(La + 1e-6)]; %length of arm B
deltaL = Lb-La;

Ea = A.*exp(-i.*betaA.*La); %Electric Field in Arm A
Eb = B.*exp(-i.*betaB.*Lb); %Electric Field in Arm B

IL = (Ea + Eb).*(conj(Ea) + conj(Eb)); %Output Intensity
IL_max = max(IL);

%Keep L constant and vary d (ie vary beta)
Lb = La; %equalize the arm lengths
betaB = beta;  %%NEED A BIGGER DATA SET FOR THIS

Ea = A.*exp(-i.*betaA.*La);
Eb = B.*exp(-i.*betaB.*Lb);

ID = (Ea + Eb).*(conj(Ea) + conj(Eb));
ID_max = max(ID);

%Plot Intensity vs Dimensional Variance
figure(5);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(deltaL*1e9, IL./IL_max,'b','LineWidth',2); hold on;
%title('Mach Zender:  Intensity vs Delta L of each Arm');
xlabel('\Delta L (nm)');
ylabel('Transmission');



figure(6);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(deltaD*1e9, ID./ID_max, 'b','LineWidth',2); hold on;
%title('Mach Zender:  Intensity vs Delta d of each Arm');
xlabel('\Delta d (nm)');
ylabel('Transmission');
```

```
% MODE = 0 AIR

%Waveguide Parameters
beta = beta0a;

A = 1; %amplitude in arm A (assumed)
La = 1e-3; %length of arm A (assumed)
betaA = beta(401);
    %for d = [1e-6:1e-9:2e-6], d(401) = 1.4 um
deltaD = d(401) - d;

%We will vary the parameters of arm B
B = 1; %amplitude in arm B (assumed)

%Keep beta constant and vary L
betaB = betaA;
Lb = [(La - 1e-6):0.01e-6:(La + 1e-6)]; %length of arm B
deltaL = Lb-La;

Ea = A.*exp(-i.*betaA.*La); %Electric Field in Arm A
Eb = B.*exp(-i.*betaB.*Lb); %Electric Field in Arm B

IL = (Ea + Eb).*(conj(Ea) + conj(Eb)); %Output Intensity
IL_max = max(IL);

%Keep L constant and vary d (ie vary beta)
Lb = La; %equalize the arm lengths
betaB = beta;  %%NEED A BIGGER DATA SET FOR THIS

Ea = A.*exp(-i.*betaA.*La);
Eb = B.*exp(-i.*betaB.*Lb);

ID = (Ea + Eb).*(conj(Ea) + conj(Eb));
ID_max = max(ID);

%Plot Intensity vs Dimensional Variance
figure(5);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(deltaL*1e9, IL./IL_max, '-- k','LineWidth',2); hold on;
%title('Mach Zender:  Intensity vs Delta L of each Arm');
xlabel('\Delta L (nm)');
ylabel('Transmission');

figure(6);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(deltaD*1e9, ID./ID_max, '-- k','LineWidth',2); hold on;
%title('Mach Zender:  Intensity vs Delta d of each Arm');
xlabel('\Delta d (nm)');
```

```
ylabel('Transmission');


end

%% Micro-Ring Resonator
%This sectio examines how the resonant frequency varies with waveguide
%width and ring radius

c = 3e8; %speed of light in a vacuum
m = 10; %number of resonants in the ring

if(flag == 1)

%Define the center point
R0 = 1e-6;
d0 = 1.4e-6;


%Keep d constant and vary R
R = [0.5e-6:1e-9:6e-6]; %Ring Radius based on the

    %Solve for neff for that d0
        V_width0 = ko.*d0.*sqrt(ncore^2-nclad^2);
        V_width0_air = ko.*d0.*sqrt(ncore^2-(1)^2);

        %Find b from the the normalized V equations (see Part II)
        b0_width0 = Find_b(V_width0,0); %b for mode = 0
        b0_width0_air = Find_b(V_width0_air,0); %b for mode = 1

        %Solve for neff from the defnition of b = (neff.^2-
nclad^2)./(ncore^2-nclad^2);
        neff0_width0 = sqrt(b0_width0.*(ncore^2-nclad^2)+ nclad^2);
        neff0_width0_air = sqrt(b0_width0_air.*(ncore^2-(1)^2)+ (1)^2);

Fres_dR = (m.*c)./(2.*pi.*R.*neff0_width0); %Resonance frequency of a Micro-
ring resonator
Fres_air_dR = (m.*c)./(2.*pi.*R.*neff0_width0_air); %Resonance frequency of a
Micro-ring resonator

%Define the Initail Conditions
Fres0 = (m.*c)./(2.*pi.*R0.*neff0_width0); %Resonance frequency of a Micro-
ring resonator
Fres0_air = (m.*c)./(2.*pi.*R0.*neff0_width0_air);


%Plot Parameters
figure(7);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

%plot(R*1e6, Fres0,'- b'); hold on;
```

```
plot((R0-R)*1e9, (Fres0 - Fres_dR)*1e-9,'b','LineWidth',2); hold on;
plot((R0-R)*1e9, (Fres0_air - Fres_air_dR)*1e-9,'-- k','LineWidth',2);
%title('Resonance Frequency vs Radius');
xlabel('\Delta Radius (nm)');
ylabel('\Delta Freq_R_E_S (GHz)');


%Vary d and keep R constant (use the range of neff calculated before
for%speed reasons)
R = R0;
d = [1e-6:1e-9:2e-6]; %Select a range of waveguide widths

    %Solve for neff for that d
        V = ko.*d.*sqrt(ncore^2-nclad^2);
        V_air = ko.*d.*sqrt(ncore^2-(1)^2);

        %Find b from the the normalized V equations (see Part II)
        b0 = Find_b(V,0); %b for mode = 0
        b0_air = Find_b(V_air,0); %b for mode = 0 in air

        %Solve for neff from the defnition of b = (neff.^2-
nclad^2)./(ncore^2-nclad^2);
        neff0 = sqrt(b0.*(ncore^2-nclad^2)+ nclad^2);
        neff0_air = sqrt(b0_air.*(ncore^2-(1)^2)+ (1)^2);

%Calculate the Resonant Frequency

Fres_dW = (m.*c)./(2.*pi.*R0.*neff0); %Resonance frequency of a Micro-ring
resonator
Fres_air_dW = (m.*c)./(2.*pi.*R0.*neff0_air); %Resonance frequency of a
Micro-ring resonator (Air Cladding)


figure(8);

set(gca,'FontSize',14);
set(gca,'LineWidth',2);

%plot(d*1e6, Fres0, '- b'); %d generated neff --> neff goes into the equation
for Fres
plot((d0 - d)*1e9, (Fres0 - Fres_dW)*1e-9, 'b','LineWidth',2); hold on;
plot((d0 - d)*1e9, (Fres0_air - Fres_air_dW)*1e-9, '-- k','LineWidth',2);
%title('Resonance Frequency vs Waveguide Width');
xlabel('\Delta Width (n m)');
ylabel('\Delta Freq_R_E_S (GHz)');



end
```

E.2 Faraday Rotator Theory

```
[R, Rotation] = TheoryFaraday(Bire, dWidth, L)
%Theortical plots for the background chapter of the thesis.  This finally
%works!


%% Constants
V = 100.*100; %[deg/m/T]   *100 to convert from 1/cm to 1/m
%L = 1e-3; %[m]
%L  = 44e-3; %[m]
B = 200e-3; %[T]
%B = 1;
%Bire = 1e-3;

ko = (2.*pi)./(1550e-9);

dProp = Bire.*ko;

%% Calculate Polarization Rotation

R = ((V.*B).^2)./( (dProp./2).^2 + (V.*B).^2 ).* sind(L.* sqrt( (dProp./2).^2
+ (V.*B).^2 ) ).^2;

Rotation = atand(R);


%% Plot Figure

close all;

set(gca,'FontSize',20);
set(gca,'LineWidth',2);

figure(1);
plot(Bire, R, 'LineWidth',2);
xlabel('Birefriengence');
ylabel('Ratio of TE/TM :: Coupling');


figure(3);
plot(Bire, Rotation, 'LineWidth',2);
xlabel('Birefriengence');
ylabel('Rotation');


figure(2);

set(gca,'FontSize',20);
set(gca,'LineWidth',2);

%plot(dWidth, Rotation, 'LineWidth',3);
```

```
plot(dWidth.*1000, Rotation, 'o b', 'MarkerSize', 10, 'MarkerFaceColor',
'b'); hold on;


[waveFitMAX, FitMAX, X, Fit] = FindTrueMax(dWidth, Rotation);

plot(X.*1000,Fit,'- r', 'Linewidth', 3);

%Calculate the Fit Line for the Birefringence Data
%coeff = polyfit(dWidth, Rotation,3);
%BireFit = polyval(coeff, dWidth);
%hold on;
%plot(dWidth,BireFit,'- r', 'Linewidth', 2);


xlabel('\Delta Width (nm)', 'FontSize', 20);
ylabel('Polarization Rotation (deg)', 'FontSize', 20);
```

E.3 Analysis of Raw TE and TM Output Power

```
CrunchFaradayRotatorData(Wavelength, TE_data, TM_data, neff_TE, neff_TM, L)

%L = Device Length(m)
%neff_TE = effective index of the TE mode, assumed to be 3.2


%% Find the Peaks of the Data

[TEpeak_wavelength, TEpeak_power] = FindPeaks2(Wavelength,TE_data);
[TMpeak_wavelength, TMpeak_power] = FindPeaks2(Wavelength, TM_data);


%% Calculate n
%this is ngroup ... for EPI around 3.8, neff is a the value between ncore
%and nclad that decribes which of the two is more effective (~3.2)

[ngroupTE, ngroup_TE_wavelength] = Find_n(Wavelength, TE_data,
TEpeak_wavelength, TEpeak_power, L);
[ngroupTM, ngroup_TM_wavelength] = Find_n(Wavelength, TM_data,
TMpeak_wavelength, TMpeak_power, L);


%% Calculate Loss

% Convert all Data to dBm
TE = 10.*log10(TE_data./1000);
TM = 10.*log10(TM_data./1000);

[lossTE] = CalcLoss(Wavelength, TE_data, neff_TE, L);
[lossTM] = CalcLoss(Wavelength, TM_data, neff_TM, L);
```

```
%% Calculate Birefringence
[WaveTE, WaveTM, PowerTE, PowerTM] = MatchPeaks(Wavelength, TE_data, TM_data,
TEpeak_wavelength, TEpeak_power, TMpeak_wavelength, TMpeak_power);
[Birefringence, BireFit] = CalcBirefringence (WaveTE, WaveTM, neff_TE,
Wavelength);

%% Output Parameters
TEavg_ngroup = ngroupTE
TMavg_ngroup = ngroupTM

TE_loss = mean(lossTE)  %dB/cm
TM_loss = mean(lossTM)  %dB/cm
```

E.3.1 Find Peaks

```
[GuassPeak_wavelength, GuassPeak_power, DataPeak_wavelength, DataPeak_power,
GuassCurve_X, GuassCurve_Y] = FindPeaks2(Wavelength, Data)
%This function take a large array of data and isolates each peak and
%generated a Guassian fit.

%% Find Raw Data Max

[MAX, indexMax] = lmax(Data,3);


Index = 1;
while(Index <= length(indexMax))

        %Build Wavelength and Power Vectors on the Raw Data
        DataPeak_wavelength(1, Index)= Wavelength(indexMax(Index));
        DataPeak_power(1,Index) = MAX(Index);

        Index = Index+1;
end

reply = input('Check the Peaks? Y/N [N]', 's');
if isempty(reply) || reply == 'n'
    flag = 0;
else
    flag = 1;
    figure(12); plot(Wavelength,Data); hold on;
end


%% Find Gaussian Max

NumPeaks = length(indexMax);
Span = 6; %Number of Points around the the central peak
J = 2; %index
```

```
index = 1;
while(J <= NumPeaks-2)
    CurrentIndex = indexMax(J);

    %Isolate the Range of Data to Fit the Guassian to
    PeakPower = Data((CurrentIndex-Span):(CurrentIndex+Span));
    PeakWave = Wavelength((CurrentIndex-Span):(CurrentIndex+Span));

    %Fit Peak
    [waveFitMAX, FitMAX, X, Fit] = FindTrueMax(PeakWave, PeakPower);


    if 1 == isempty(waveFitMAX)
    else
        if 1 == isempty(FitMAX)

        else

            if(flag == 1) %check peaks

                plot(waveFitMAX, FitMAX, 'd');

            reply = input('Keep Peak? Y/N [Y]', 's');
                if isempty(reply)

                    %Store Fit
                    GuassPeak_wavelength(:,index) = waveFitMAX;
                    GuassPeak_power(:,index) = FitMAX;

                    GuassCurve_X(:,index) = X;
                    GuassCurve_Y(:,index) = Fit;

                    index = index + 1;
                else
                    %don't move the index forward
                end

            else
                %Store Fit
                GuassPeak_wavelength(:,index) = waveFitMAX;
                GuassPeak_power(:,index) = FitMAX;

                GuassCurve_X(:,index) = X;
                GuassCurve_Y(:,index) = Fit;

                index = index + 1;

            end
        end
    end

    %Increase Index
```

```
    J = J+1;
end


%% Plot
figure(4);
set(gca,'FontSize',14);
set(gca,'LineWidth',2);

plot(Wavelength, Data, '-* b'); %Raw Data
hold on;
plot(GuassCurve_X,GuassCurve_Y,'-r', 'Linewidth', 2); %Fit Curve
plot(GuassPeak_wavelength, GuassPeak_power, 'd k', 'Linewidth', 2);
%Calculated Max
plot(DataPeak_wavelength, DataPeak_power,'o k', 'Linewidth', 2);


title('Raw Data with fit Maximum');
xlabel('Wavlength (nm)');
ylabel('Power (\muW)');

close(figure(12));
```

E.3.2 Calculate Group Index

```
[ngroup, Wave] = Find_n(Wavelength, Data, Peak_wavelength, Peak_power, L)
%%
%This function will take a given Fabry Perot Range and find n_group! over the
%wavelength, it does this by find the max peaks for the range of
%wavelengths - then compare each successive peak wavelegnth.

%Inputs:
%L == device length (m)

%group index should be about 3.78

L = L.*1e9; %convert from m to nm
Index = 2;
INDEX = 1;

while(Index <= length(Peak_wavelength))

    %% Check Peaks
    close(figure(14)); figure(14); plot(Wavelength, Data); hold on;
    plot(Peak_wavelength(Index-1), Peak_power(Index-1),'d');
    plot(Peak_wavelength(Index), Peak_power(Index),'d');

    reply = input('Are these sucessive resonant modes? Y/N [Y]', 's');
    if isempty(reply) || reply == 'y'
```

```
        if(Index > 1) %skips the first data point to save because neff is
calculated by comparing 2 successive points

        %% SOLVE FOR N_group
        ngroup(INDEX) = (1/(2*L))*((Peak_wavelength(Index-1)*
Peak_wavelength(Index)) / (Peak_wavelength(Index)-Peak_wavelength(Index-1)));

        Wave(INDEX)= (Peak_wavelength(Index)+ Peak_wavelength(Index-1))./2;

        INDEX = INDEX + 1;
        end
    end

    Index = Index+1;
end



%% Plot Data
figure(2);set(gca,'LineWidth',2); set(gca,'FontSize',20);
plot(Wave,ngroup,'o b', 'MarkerSize', 10, 'MarkerFaceColor', 'b');
%title('n_g_r_o_u_p vs Wavelength');
xlabel('Wavelength (nm)');
ylabel('n_g_r_o_u_p TE');

%Calculate the Fit Line for the n data
%coeff = polyfit(Wave,ngroup,1);
%xfit = linspace(min(Wave),max(Wave),Index);
%nfit = polyval(coeff,xfit);
%hold on;
%plot(xfit,nfit,'- k');

close(figure(14));
```

E.3.3 Calculate Loss

```
[loss_dB] = CalcLoss(Wavelength, Data, neff, L)
% This function calculates the loss of the data.
% neff = effective index calculated from Find n

%L = Length of the device (m)
% This function assumes the data is coming in at the log!!



%% Find Max and Min

[WaveMax, Max, WaveMin, Min] = GenMaxMin(Wavelength, Data);
```

```
if length(WaveMin) >= length(WaveMax)
    NumPeaks = length(WaveMax);
else
    NumPeaks = length(WaveMin);
end


index = 1;
check = 1;
MAX = 1;
MIN = 1;
flag = 0;

figure(16); plot(Wavelength, Data, 'b'); hold on;

while(check <= NumPeaks)


    plot(WaveMax(MAX), Max(MAX), 'r d');
    plot(WaveMin(MIN), Min(MIN), 'r d');


    reply = input('Skip Peak? Y/N [N]', 's');
    if isempty(reply) || reply == 'n'


        %Check that the Peaks Match
        while(flag == 0) %move loop


            reply = input('Do the Peaks Match? Y/N [Y]', 's');
            if isempty(reply) || reply == 'y'

                WaveMAX(index) = WaveMax(MAX);
                PowerMAX(index) = Max(MAX);

                WaveMIN(index) = WaveMin(MIN);
                PowerMIN(index) = Min(MIN);

                flag = 1;

            else


                reply = input('Move MIN Peak(blue)? Y/N [Y]', 's');
                if isempty(reply) || reply == 'y'

                    reply = input('Move Forward? Y/N [Y]', 's');
                    if isempty(reply) || reply == 'y'
                        plot(WaveMin(MIN+1), Min(MIN+1), 'b d');
                        MIN = MIN+1;
                    else
                        if (index-1 > 0)
```

```
                    plot(WaveMin(MIN-1), Min(MIN-1), 'b d');
                    MIN = MIN-1;
                else
                    display('Cant Move Back');
                end

            end


        end



        reply = input('Move MAX Peak (red)? Y/N [Y]', 's');
        if isempty(reply) || reply == 'y'

            reply = input('Move Forward? Y/N [Y]', 's');
            if isempty(reply) || reply == 'y'
               plot(WaveMax(MAX+1), Max(MAX+1), 'd');
               MAX = MAX+1;
            else
               if (index-1 > 0)
                   plot(WaveMax(MAX+1), Max(MAX+1), 'd');
                   MAX = MAX-1;
               else
                   display('Cant Move Back');
               end
            end

        end

    end

  end

  end

  MAX = MAX + 1;
  MIN = MIN + 1;


  if MAX >= MIN
      check = MAX;
  else
      check = MIN;
  end


  flag = 0;
  index = index + 1;

end
```

```
Wave = (WaveMAX + WaveMIN)./2; %Wave the wavelengths and find the center

Ratio = PowerMAX(:)-PowerMIN(:);  %subtracted rather than divided because we
are working with the log of the data
AvgRatio = mean(Ratio);


%% Calc Loss

F = sqrt(AvgRatio); %Loss

R = abs((neff-1)./(neff+1)).^2; %Reflectivity  (using avg_neff is probably
cheating since neff changes with wavelength but it works in a pinch
loss = (log(R) - log( (F-1)./(F+1) ) )  ./L;  %loss/m   --> ORIGINAL
%loss = -(log( (F-1)./(F+1) ) - log(R.*2) )  ./L;  %loss/m

%loss = log(- (F-1)./ ((F+1).*R) ) ./ L;

loss_cm = loss.*0.01;  %convert from 1/m to 1/cm
loss_dB = loss_cm.* (10.*log10(exp(1))); %concert to 1/cm to dB/cm


%% Plot Loss

%figure(4);
%plot(Wave, loss_dB, '+ k');
%title('Loss vs Wavelength');
%xlabel('Wavelength (nm)');
%ylabel('Loss (dB/cm)');



%Fit Loss Line

%coeff = polyfit(Wave, loss_dB,1);
%LossFit_x = linspace(min(Wave),max(Wave), length(Wave));
%LossFit_y = polyval(coeff, LossFit_x);
%hold on;
%plot(LossFit_x,LossFit_y,'-- b');


close(figure(16));
```

E.3.4 Calculate Birefringence

```
[WaveTE, WaveTM, PowerTE, PowerTM] = MatchPeaks(Wavelength, TE_data, TM_data,
TE_wavelength, TEpeak_power, TM_wavelength, TMpeak_power)
%% Given two sets of peaks - match the points


if length(TEpeak_power) >= length(TMpeak_power)
    NumPeaks = length(TMpeak_power);
else
    NumPeaks = length(TEpeak_power);
end


index = 1;
check = 1;
TE = 1;
TM = 1;
flag = 0;


while(check < NumPeaks)

    close(figure(11));
    figure(11); plot(Wavelength, TE_data, 'r'); hold on; plot(Wavelength,
TM_data, 'b');
    plot(TE_wavelength(TE), TEpeak_power(TE), 'r d');
    plot(TM_wavelength(TM), TMpeak_power(TM), 'b d');


    while(flag == 0) %move loop

        plot(TE_wavelength(TE), TEpeak_power(TE), 'k d');
        plot(TM_wavelength(TM), TMpeak_power(TM), 'k d');

        reply = input('Do the Peaks Match? Y/N [Y]', 's');
        if isempty(reply) || reply == 'y'

            WaveTE(index) = TE_wavelength(TE);
            PowerTE(index) = TEpeak_power(TE);

            WaveTM(index) = TM_wavelength(TM);
            PowerTM(index) = TMpeak_power(TM);

            flag = 1;

        else


            reply = input('Move TM Peak(blue)? Y/N [Y]', 's');
            if isempty(reply) || reply == 'y'

                reply = input('Move Forward? Y/N [Y]', 's');
```

```
            if isempty(reply) || reply == 'y'
                plot(TM_wavelength(TM+1), TMpeak_power(TM+1), 'b d');
                TM = TM+1;
            else
                if (index-1 > 0)
                    plot(TM_wavelength(TM-1), TMpeak_power(TM-1), 'b d');
                    TM = TM-1;
                else
                    display('Cant Move Back');
                end

            end


        end



        reply = input('Move TE Peak (red)? Y/N [Y]', 's');
        if isempty(reply) || reply == 'y'

            reply = input('Move Forward? Y/N [Y]', 's');
            if isempty(reply) || reply == 'y'
               plot(TE_wavelength(TE+1), TEpeak_power(TE+1), 'd');
               TE = TE+1;
            else
               if (index-1 > 0)
                   plot(TE_wavelength(TE+1), TEpeak_power(TE+1), 'd');
                   TE = TE-1;
               else
                   display('Cant Move Back');
               end
            end

        end

    end

end

if TE >= TM
    check = TE;
else
    check = TM;
end


TE = TE + 1;
TM = TM + 1;

flag = 0;
index = index + 1;

end
```

```
figure(15);
plot(Wavelength, TE_data, 'r'); hold on;
plot(Wavelength, TM_data, 'b');
plot(WaveTE, PowerTE, 'r d');
plot(WaveTM, PowerTM, 'r d');

display('Find Peaks DONE');

close(figure(11));



[Bire, BireFit,TM_wavelength, TE_wavelength] =
CalcBirefringence(TE_wavelength, TM_wavelength, neff_TE, Wavelength)
% Thie function compared the two wavelength peaks distance and draws a
% general fit line.


%% Calc Birefringence

Bire = neff_TE.*((TM_wavelength./TE_wavelength)-1);


%% Plot Data and Fit a Line to it

AvgWave = (TE_wavelength + TM_wavelength)./2;

%NewWave = [1530:0.01:1550];

figure(43); plot(AvgWave, Bire, 'o b', 'MarkerSize', 10, 'MarkerFaceColor',
'b');
set(gca,'LineWidth',2); set(gca,'FontSize',20);

%Calculate the Fit Line for the Birefringence Data
coeff = polyfit(AvgWave, Bire,1);
BireFit = polyval(coeff, Wavelength);
hold on;
plot(Wavelength, BireFit,'- r', 'Linewidth', 2);
%title('Birefringence vs Wavelength: PeakData1 - PeakData2');
xlabel('Wavelength (nm)');
ylabel('Birefringence');

%Plot Zero Line
hold on;
plot(Wavelength, 0, '-- k');
```

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