Evaluation of Phase Change Materials for Reconfigurable Interconnects

by

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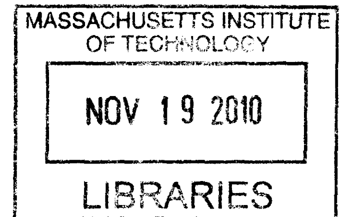

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ABSTRACT

The possible use of programmable integrated circuit interconnect vias using an indirectly heated phase change material is evaluated. Process development and materials investigations are examined. Devices capable of multiple cycles between on/off states for reconfigurable applications have been successfully demonstrated in a standard CMOS-compatible technology. Building computer chips with these vias would create a new kind of field programmable gate array (FPGA), whereby the design can be reconfigured depending on its application. The phase change reprogrammable-via is nonvolatile, unlike SRAM-based technology. It also has a relatively low on-state resistance and occupies less real estate on the chip. As the "switches" are placed at the metallization level, it provides flexibility for the designer to place them. Programmable-via can operate at a relatively low voltage compared to FLASH-based technology. Similar to the case of antifuses, programmable-via interconnect structures are projected to be radiation hard. However, the most challenging part of implementation is the circuit design. Issues such as integration of materials and design with current tools need to be overcome. A lack of expert personnel in this area also makes the implementation of programmable-via FPGAs complicated. The market for FPGA is promising due to the attraction of the programmable logic market. An intellectual Property (IP) analysis indicates there exist a significant new space for exploration in this area. The best-suited business model is as a new start-up that demonstrates feasibility and develops intellectual property. The potential commercialization of such technology is also discussed. Although this concept is promising result, more research is needed to show the reliability and feasibility of such a technology in complex circuits. It will take some time before this approach can be considered for production.

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1 Introduction

1.1 Background

Phase change materials are used in phase change random access memory (PRAM) and Micro-Electro-Mechanical Systems (MEMS). This material possesses unique features whereby it changes phases between crystalline and amorphous phases when subjected to laser-induced or current-induced heating and quenching, and exhibits large differences in optical reflectivity and electrical resistivity in these two states. reversible switching between these two distinct state is useful in many applications. It can be used in optical digital data storage and also used as the storage medium in a electronic memory cells. It can also be used in mechanical switches or actuators in MEMS application.

Phase change material with such characteristics has also been considered for usage in other applications. With its properties of fast switching between the two phases, it is a proposed candidate for future Field Programmable Gate Array (FPGA) designs. The phase change material is used to fill up the vias connecting in the metal wiring layers and acts as a switch that is reprogrammable. Through the use of an integrated electrical heater with controlled a current pulse and duration, it can be switched from the crystalline or amorphous state and back as desired.

1.2 Objectives

In this report, the feasibility of using phase change materials as reconfigurable interconnect will be examined. The objectives are:

- Evaluate the properties of phase change materials to examine their suitability as materials used in vias
- Determine the advantages and challenges of this technology compared to current technologies
- Analyze the IP space of this area
- Determine the commercialization potential of such technology in the future

1.3 Scope and Overview

No experimental work was carried out for the purpose of this thesis. Analyses were carried out with the data obtained from work done by others in this area of research. Reviews of experts from this area were also employed. The report starts with a review of the technological background of phase change materials and FPGA design. This is followed by evaluation of phase change material for reconfigurable interconnects with also discussion of current technologies. Subsequently, analysis of the FPGA market is carried out. An Intellectual Properties (IP) analysis follows, which shows a promising IP space in this area. The commercialization potential will be discussed with a proposed business model for new start-up companies for this technology.

2 Technological Background

The idea of phase change recording dates back to the mid 1960s when S.R. Ovshinsky first suggested the use of differences in electrical and optical properties between amorphous and crystalline phases of Te-based chalcogenides for data storage [1].

2.1 Phase Change Materials

Phase change materials (PCM) show a reversible phase transformation between amorphous state and crystalline state. The attractiveness of PCM are their very large changes in optical reflectivity and electrical resistivity when switching between these two phases. Although many materials possessed the ability to phase change but the speed at which phase changing can occur often determines its practical usage in applications. A chalcogenide material is capable of switching between crystalline and amorphous states within nanoseconds making it suitable for various applications.

The switching of amorphous and crystalline state is shown in Figure 1. When a PCM in the high resistance amorphous state is heated above the glass transition temperature by applying electrical pulse, the material rearranges into the stable crystalline state. In order to switch it back to the amorphous state, the material is heated by a larger current pulse above the melting temperature. Rapid cooling quenches it in the amorphous state.

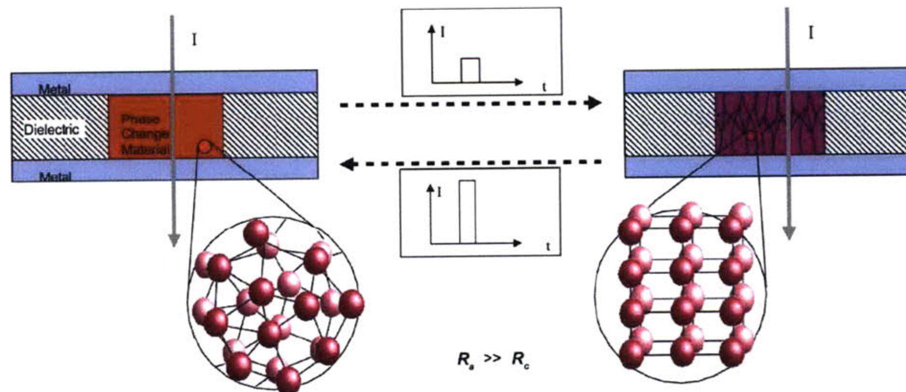


Figure 1. Electrical switching of PC materials for non-volatile electronic storage. A current pulse of high intensity and short duration (*bottom*) is used for amorphization, while a pulse of lower intensity but longer duration (*top*) re-crystallizes the material. Read-out is performed at lower currents, that do not change the state of a bit [2].

The two key properties that characterize PCM are their contrast between the amorphous and crystalline phases and their remarkable crystallization kinetics. A schematic plot of the crystallization speed between glass-transition temperature (T_g) and melting temperature (T_m) is shown in Figure 2. As seen from the plot, crystallization of a liquid phase is thermodynamically allowed once the material is cooled below the T_m. The free energy between the liquid and crystal favors the crystalline state, which is the driving force of transformation. It vanishes at T_m, where the liquid and the crystalline coexist, but increases on cooling below T_m. Therefore, the driving force to form crystalline nuclei increases with decreasing temperature. However, the atomic mobility rapidly decreases. Crystallization is therefore slow close to the T_m, as the high atomic mobility is over-compensated by the marginal driving force for nucleation. At temperatures slightly above T_g or lower, the driving force for nucleation is high but the atomic mobility is low, again resulting in slow crystallization. The highest crystallization speeds are encountered at intermediate temperatures between T_g and T_m, where a good compromise between atomic mobility and driving force enables a fast transition.

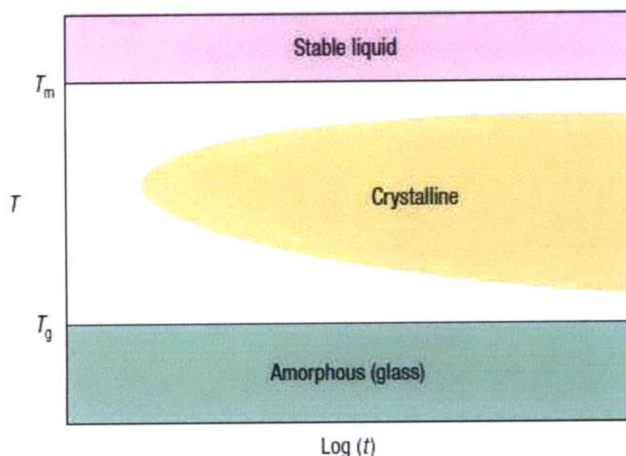


Figure 2. Time-temperature-transformation diagram of an undercooled liquid [3].

Various materials have been studied for potential use in commercial products such as phase change memories and the best to-date in terms of speed and stability are ternary Ge-Sb-Te and quaternary Ag-In-Sb-Te alloys. Detailed discussion on these two material systems will be carried out in a later part of this report.

2.2 Crystalline and Amorphous State

A crystal or crystalline solid is a solid material, whose constituent atoms, molecules, or ions are arranged in an orderly repeating pattern extending in all three spatial dimensions. When a material is in the crystalline state, it has long-range ordering. The crystalline state is the thermal-dynamically-stable phase below T_m, whereby a particular crystalline material has the lowest Gibbs free energy of all possible atomic configurations. In contrast, solids in the amorphous state do not exhibit any long-range order. In principle, given a sufficiently high cooling rate, any liquid can be made into an amorphous solid. Cooling reduces molecular mobility. If the cooling rate is faster than the rate at which molecules can organize into a more thermodynamically favorable crystalline state, then an amorphous solid will be formed.

2.3 Field Programmable Gate Array (FPGA)

Reconfigurable circuits have a wide range of microelectronic applications, which includes the use in field-programmable gate arrays (FPGAs) and repair of defective memory elements. With FPGA, reconfigurable logic systems can be made on a single chip. In the FPGA concept, a set of simple reconfigurable logic blocks is arranged in an array with interspersed switches. These switches function to rearrange the interconnections between the logic blocks. The FPGA architecture is shown in Figure 3.

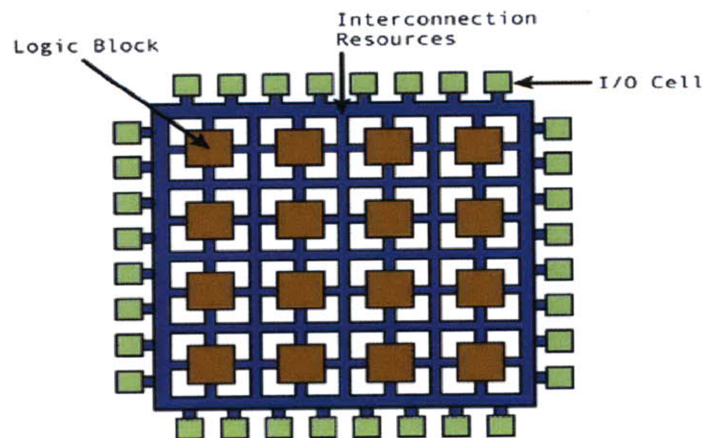


Figure 3. Field-programmable gate arrays (FPGA) architecture [4].

FPGAs are fully standardized chips, which can be configured after manufacturing. Modern FPGA chips often contain embedded application specific integrated circuit (ASIC) blocks for memory and signal processing. When the first FPGAs were introduced by Xilinx in 1980s, the number of transistors on a chip was limited and only relatively simple functions could be implemented using FPGAs. The rapid scaling of chip features makes it possible to download several microprocessors and complete digital systems on today's FPGAs.

Technical advances and steep learning curves have enabled new functionality to be implemented at constantly declining costs in the IC industry. In 1992, Tsugio Makimoto from Sony proposed a model of ten-year cycles in the semiconductor industry between standardization to customizability [5]. Figure 4 shows the Makimoto pendulum. According to his theory, the semiconductor industry swings like a pendulum between customization and standardization.

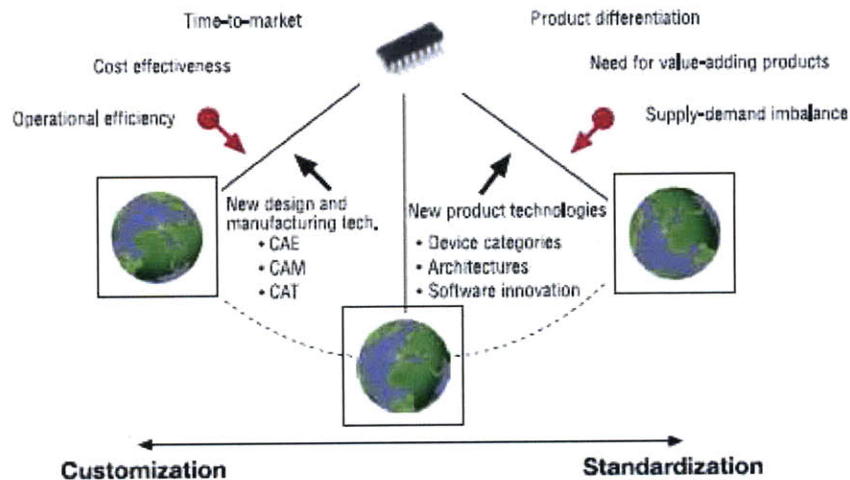


Figure 4. The Makimoto pendulum [5].

The swings of the Makimoto pendulum creates cycles as shown in Figure 5, where two cycles have been added to the original model.

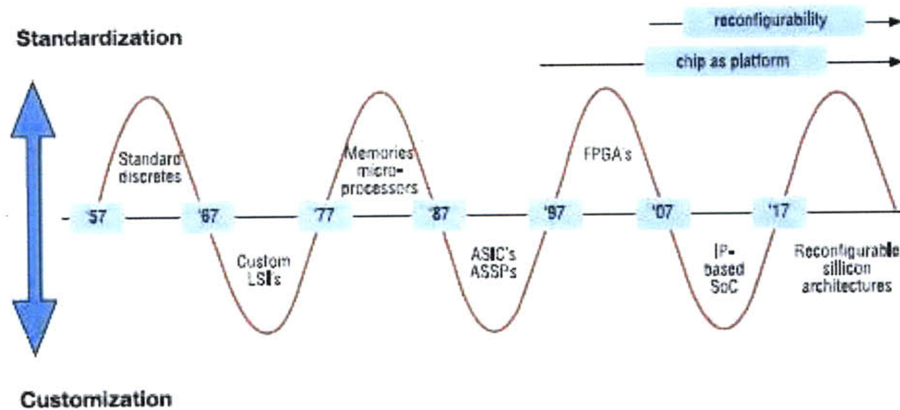


Figure 5. Extrapolated Makimoto waves, 1957-2020 [5].

The original Makimoto pendulum was driven by the continuous improvement in technology and normal competitive forces. This includes time-to-market, cost effectiveness, operational efficiency, product differentiation and many more. Chips that have processing capabilities do not necessary completely define product functionality. In fact, their processing function is gradually defined during the life-time of the product. The development towards looser coupling between the chip design and product design is shown in Figure 5 by adding two new trends in the diagram, which are chips as system platforms and reconfigurability.

FPGAs, alternative to custom ICs, can be used to implement an entire System On one Chip (SOC). FPGAs are easy to implement within a short time with the help of Computer Aided Designing (CAD) tools as there is no physical layout process, no mask making and no IC manufacturing involved.

The main difference of FPGAs compare to ASICs is that the front end cost of ASICs can be very large, measured in tens of millions of USD, whereas commercial FPGA chips and development platforms can cost only tens of dollars [5]. Errors in ASIC design can become extremely expensive, as a new mask set must be created and the manufacturing process often has to be started anew. Also, design errors that are discovered after the chip is manufactured can lead to a new manufacturing cycle that may take several months. In consumer electronics where time to market is a critical factor in profitability, such a delay can cost a lot. However, the marginal cost of producing new copies of a chip is low after the non-recurring costs are paid in ASICs.

With much lower non-recurring costs compared to that of ASICs, FPGAs have emerged as the main entry platform for ASIC design. Chips and the related software are now developed using FPGA development boards. It is also common nowadays for products to be launched using FPGAs that can be easily reprogrammed if bugs are found or if new features are introduced. Only when the product volume is high is the chip converted from an FPGA to an ASIC chip. Figure 6 show the typical cost curves for different IC technologies with respect to the manufacturing volume.

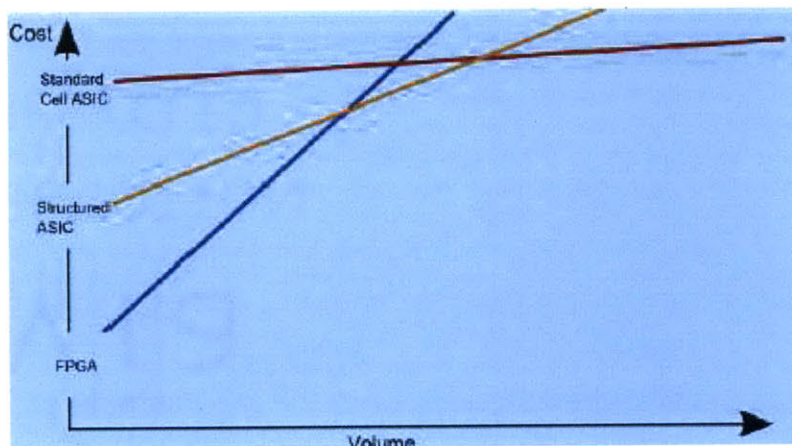


Figure 6. Cost curves for different IC technologies [5].

Currently, the commonly employed technologies used in FPGAs are SRAM-based, FLASH-based and antifuse-based, which will be discussed in a later chapter. A novel concept will be introduced that uses phase change materials in vias that are reprogrammable. Its properties will be discussed to show its suitability in the proposed architecture. The advantages and limitations of the programmable-via concept will be discussed.

3 Evaluation of phase change materials for reconfigurable interconnects

3.1 Current Technologies

3.1.1 SRAM-based technology

The Static Random Access Memory (SRAM) programming technology employs SRAM cells to control pass transistors or multiplexers as shown in Figure 7. For the pass-transistor element in Figure 7, the state of the SRAM cell controls the ON and the OFF of the transistor, which acts like a switch. When ON, the pass transistor exhibits a relatively low resistance between the two adjacent routing wires, and thus the switch is closed. When OFF, the switch is open and the transistor incurs a very high resistance between the two routing wires. For the multiplexer approach in Figure 7, the state of the SRAM cells serve as select signals and control the choice of the multiplexer's input.

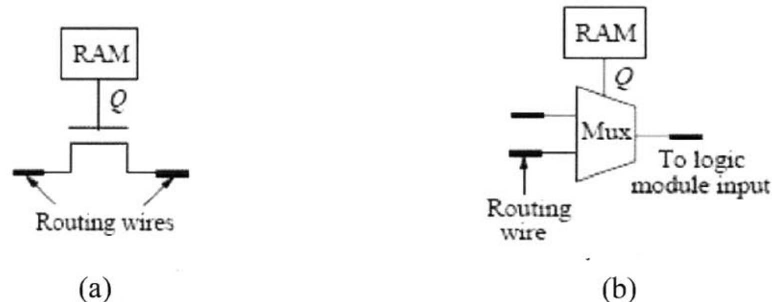


Figure 7. SRAM programming technology with (a) a pass-transistor switch and (b) a multiplexer switch [6].

Figure 8 shows a typical SRAM cell. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. Figure 9 shows a schematic view of the SRAM-controlled programmable switch.

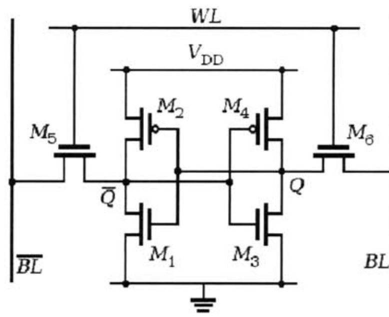


Figure 8. Schematic diagram of a typical SRAM cell [7]

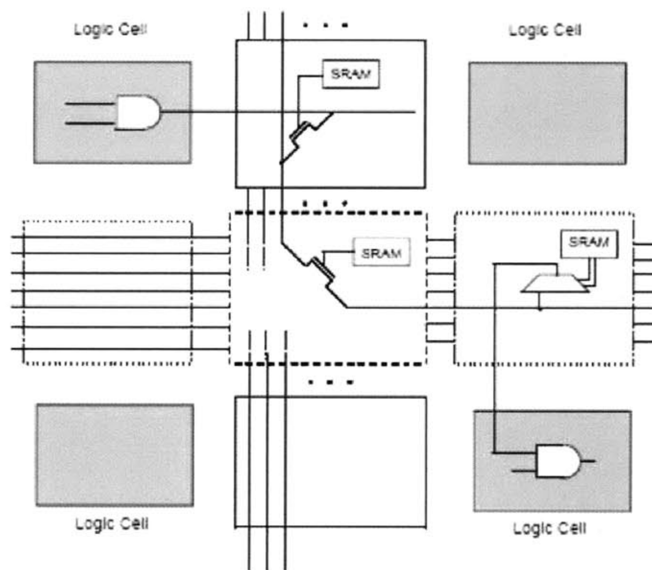


Figure 9. SRAM-controlled programmable switch [6].

The entire cell comprises a multitransistor SRAM storage element whose output drives an additional control transistor. Depending on the contents of the storage element (logic 0 or logic 1), the control transistor will be either OFF (disabled) or ON (enabled). Once a value has been loaded into an SRAM cell, it will remain unchanged unless it is specifically altered or until power is removed from the system.

There are several advantages that make SRAM-based technology the popular choice used in FPGAs. It can be configured over and over again, with easy and fast reprogramming. Also, new design ideas can be quickly implemented and tested, while evolving standards and protocols can be accommodated relatively easily. Most importantly, SRAM cells are created using exactly the same CMOS technologies as the rest of the devices, therefore no special processing steps are

required in order to create these components. Besides, this technology is at the forefront, being the state of the art. Major players in the FPGA market and memory device companies expend tremendous resources on research and development in this area.

However, this approach is faced with several limitations and disadvantages. In SRAM-based technology, each cell consumes a significant amount of silicon real estate because the cells are formed from six transistors as a latch. Also, the device's configurable data (programmed state) will be lost when power is removed from the system and has to be reprogrammed or reconfigured when the system is power turned back on. Therefore, it requires the use of a special external memory device, which increases the cost and consumes real estate on the board.

In terms of security issues, it is difficult to protect intellectual property (IP) as the configuration file used to program the device is stored in some form of external memory. Some SRAM-based FPGAs support the concept of bitstream encryption, whereby the final configuration data is encrypted before being stored in the external memory device. The encryption key itself is loaded into a special SRAM-based register in the FPGA via its JTAG port. This key allows the incoming encrypted configuration bitstream to be decrypted as it is loaded into the device. The command/process of loading an encrypted bitstream automatically disables the FPGA's read-back capability. Therefore, unencrypted configuration data is typically used during development and then encrypted data is used when moved into production. The downside to the encrypted bitstream scheme is that a battery backup is required on the circuit board to maintain the content of the encryption key register in the FPGA when power is removed from the system. This battery (lifetime of year or decade) need only maintain a single register in the device, but it adds to the size, weight, complexity and cost of the board.

3.1.2 Antifuse technology

An antifuse is a two terminal, one-time programmable circuit element with high resistance (>100 MΩ) between its terminals in the unprogrammed state and low resistance (~500 Ω) in the programmed state. Programming is performed by applying a higher than operating voltage (eg. 18 V) across the anti-fuse's terminals, causing dielectric breakdown and drastically reducing the

device resistance. Programming this particular element effectively "grows" a link, known as a via, by converting the insulating oxide into conducting state as shown in Figure 10.

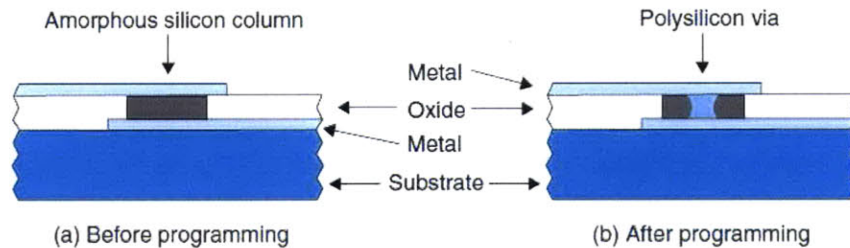


Figure 10. Growing an antifuse [8].

The major advantages of antifuse technology used in FPGAs are the small device size and relatively low ON resistance and OFF capacitance. The size of an amorphous antifuse is approximately 1 μm^2 in a 65 nm process. These allow a much denser switch population and thus can alleviate the routing constraints imposed by the limited connectivity of routing resources. Antifuse-based devices are programmed offline using a special device programmer. These devices are nonvolatile (their configuration data remains when the system is powered down) and are immediately available as soon as power is applied to the system. Therefore, this approach does not require an external memory chip to store their configuration data, which saves the cost of an additional component and saves real estate on the board. Most importantly, the interconnect structure is naturally rad hard, whereby they are relatively immune to the effects of radiation. This is therefore extremely useful for military and aerospace applications because the state of a configuration cell in an SRAM-based component can be "flipped" if that cell is hit by radiation. Figure 11 shows the cross section of a programmer antifuse.

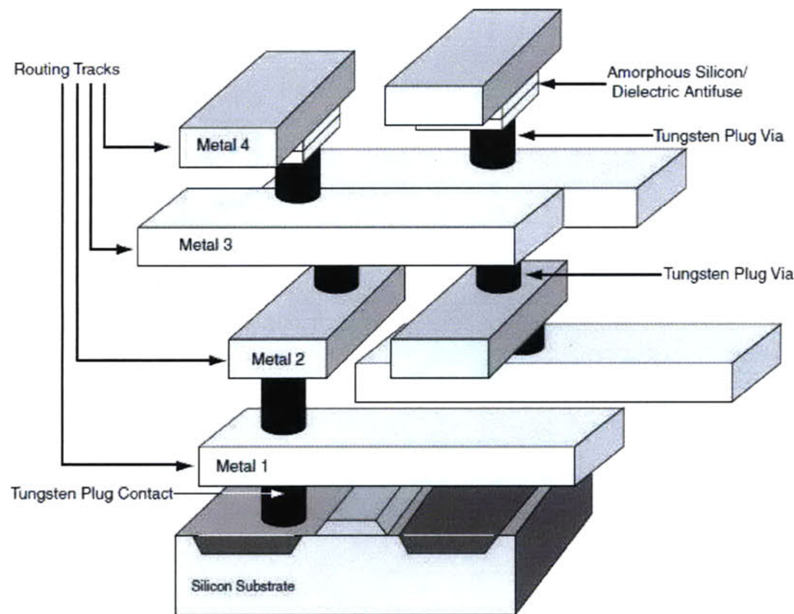


Figure 11. Cross section of a programmer antifuse [6].

Their configuration data is buried deep inside them, making it almost impossible to reverse-engineer the design. As each antifuse is being processed, the device programmer keeps on testing it to determine when that element has been fully programmed. They then move on to the next antifuse. Once the device has been programmed, it is possible to set (grow) a special security antifuse that subsequently prevents any programming data from being read out of the device. Even if the device is decapped (top removed), programmed and unprogrammed antifuses appear to be identical, and the fact that all of the antifuses are buried in the internal metallization layers makes reverse engineering close to impossible.

However, antifuse based technology is one time programmable (OTP). Once an antifuse has been triggered, it cannot be reversed. Vendors claim that it consumes only approximately 20 percent of the standby power of an equivalent SRAM-based component, their operational power consumption is also significantly lower, with their interconnect-related delays are smaller. It also occupies less real estate on the chip than an equivalent SRAM cell. However, antifuse devices also require extra programming circuitry, including a large,-programming transistor for each antifuse. It also requires the use of around three additional processing steps compared to SRAM-based systems, after the main manufacturing process has been qualified. Antifuse technology is

usually several generations (technology nodes) behind SRAM-based components. Therefore, it effectively wipes out any speed or power consumption advantages that might otherwise be of interest.

3.1.3 FLASH-based technology

A relatively new technology known as FLASH is being used in some FPGAs today. This technology grew out of an earlier technology known as erasable programmable read-only memory (EPROM) that allows devices to be programmed, erased and reprogrammed with new data. An EPROM transistor has the same basic structure as a standard MOS transistor but with the addition of a second polysilicon floating gate isolated by layers of oxide as shown in Figure 12.

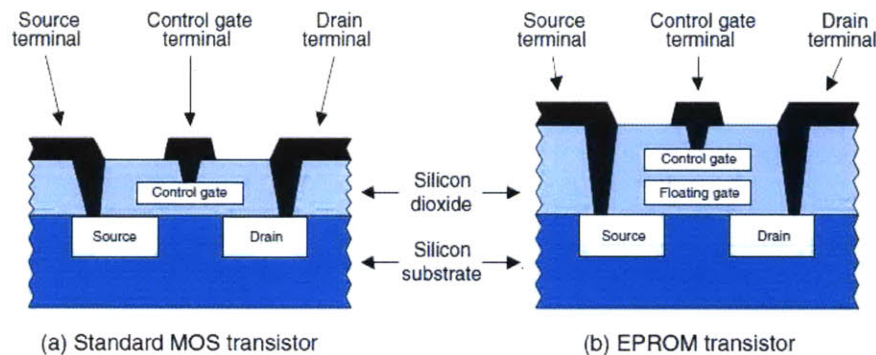


Figure 12. Standard MOS vs EPROM transistors [8].

In its unprogrammed state, the floating gate is uncharged and does not affect the normal operation of the control gate. In order to program the transistor, a relatively high voltage (on the order of 12 V) is applied between the control gate and the drain terminals. This causes the transistor to be turned hard on, and energetic electrons force their way through the oxide into the floating gate in a process known as hot (high energy) electron injection. When the programming signal is removed, a negative charge remains on the floating gate. This charge is very stable and will not dissipate for more than a decade under normal operation of the control gate, and thus distinguishes these cells that have been programmed from those that have not. The main problems with EPROMs are their expensive packages, that use quartz windows through which

ultraviolet radiation is used to erase the device and the time it takes to erase them, on the order of 20 minutes. The next rung up the technology ladder was electrically erasable programmable read-only memories (EEPROMs or E^2PROMs). It is approximately 2.5 times larger than an equivalent EPROM cells as it comprises two transistors, one access and one programmed transistors, and the space between them as show in Figure 13.

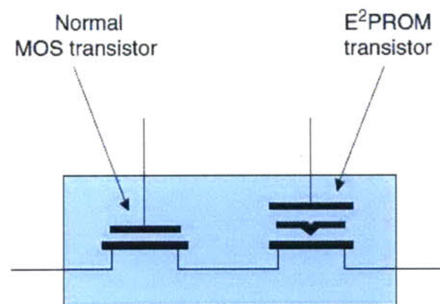


Figure 13. EEPROM cell [8].

It is similar to that of EPROM transistor in that it contains a floating gate but the insulating oxide layers surrounding this gate is very much thinner. The second transistor can be used to erase the cell electrically. The major advantages of EPROM and EEPROM technologies are their reprogrammability and full testability before shipment. Also, unlike SRAM-based FPGAs, they require no external permanent memory to program the chip at power on. However, they suffer from some drawbacks such as relatively high ON-resistance, high static power consumption and complicated manufacturing processes.

FLASH can trace its ancestry to both EPROM and EEPROM technologies. The term FLASH was originally coined to reflect its rapid erasure times compared to EPROM. Components based on FLASH can employ a variety of architectures. Some have a single floating gate transistor cell with the same area as an EPROM cell but with the thinner oxide layers characteristic of an EEPROM component. These devices can be electrically erased but only by clearing the whole device or large portions thereof. Other architectures feature a two transistor cell, similar to that of an EEPROM cell, thereby allowing them to be erased and reprogrammed on a word-by-word basis. Similar to SRAM counterparts, their configuration cells are connected together in a long shift-register-style chain. These devices can be configured off-line using a device programmer.

Some are in-system programmable but programming time is about three times that of an SRAM-based component.

With regard to protection, some use the concept of a multibit key (ranging from around 50 bits to hundred bits in size). Once the device is programmed, the user-defined key (bit-pattern) can be loaded to secure its configuration data. After the key has been loaded, the only way to read data out of the device, or to write new data into it, is to load a copy of the key via a JTAG port. It runs around 20 MHz, which take billions of years to crack the key by exhaustively trying every possible value. Besides, FLASH-based devices are nonvolatile, it will be "instant on" when power is first applied to the system. It is also much smaller than SRAM-based devices, whereby the logic can be much closer together, thereby reducing interconnect delays. However, it requires around five additional steps on top of the standard CMOS technology. It is lagging behind SRAM-based devices by one or more generations. It also requires a relatively high static power consumption as it contain vast numbers of internal pull-up transistors.

3.2 Programmable-via concept

Current non-phase-change technologies have several limitations and disadvantages such as occupying a large chip area, high on-state resistance, volatility which loses data during power interruption, one time programmability and a high programming voltage. It is therefore desirable to have a switch device that is reconfigurable which possesses the lowest possible on-state resistance, occupies a small cell area, is nonvolatile, is capable of operating at a low voltage, has sufficient reliability for repeated write operations, and is capable of retaining stored data for a long time. In 2008, a programmable-via design was first proposed using an indirectly heated phase change switch by Chen *et al.* [9].

Figure 14 shows a schematic temperature versus time relationship for programming in phase change material. During the RESET switching operation, an abrupt high current pulse is used to melt and quench/amorphize the phase change via adjacent to the heater. The SET switching is accomplished by a relatively low but long current pulse applying through the heater. The heat generating from the current on the heater is capable of annealing the amorphous phase change materials to the crystalline state.

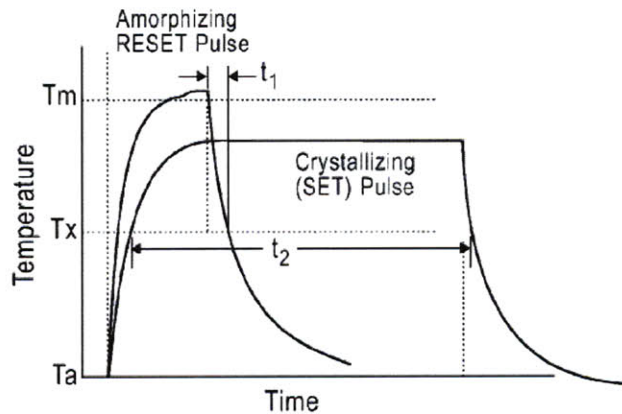


Figure 14. Schematic temperature-time relationship during programming in a phase change material [10].

The detailed characteristics and properties of phase change materials used in the programmable-via and the various proposed designs of programmable-via will be discussed in a later chapter.

A programmable-via holds the promise to enable high performance reconfigurable logic applications without significantly sacrificing logic gate density or power. Phase change materials, are an attractive option for this application and have drawn most attention for memory applications as a possible replacement for FLASH memory. Although the proposed programmable-via concept is similar to that used in phase change memory (PCM), its device design issues are different. Figure 15 shows PCRAM cell structures.

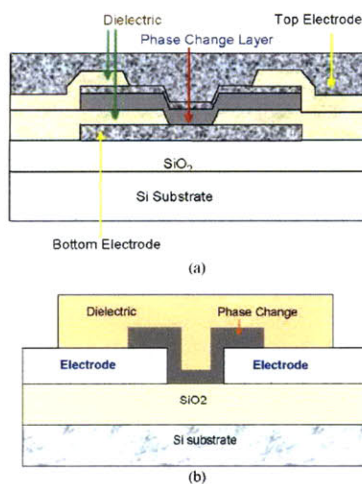


Figure 15. Phase-change memory devices. (a) Vertical structure and (b) horizontal structure or line type structure [11].

In PCMs, the phase change volume must be minimized, whereas for a programmable-via, the via size must be kept large enough to ensure low contact resistance. This constraint makes programming through a direct current flow impractical. Therefore, the operation of a programmable-via that utilizes a novel indirect-heating mechanism was proposed [9, 12]. Logic circuits associated with the programmable-via are decoupled from the configuration circuits by using an independently contacted heater electrode. To achieve the best efficiency of electrical-thermal transformation from heater to via, the heater should be a thin layer of a refractory metal with relatively high resistivity and low thermal conductivity [9]. Figure 16 shows a schematic diagram of the programmable concept using phase change material and indirect heating mechanism. This device structure can be fabricated with CMOS-compatible processes. The via is filled with phase change material ($Ge_2Sb_2Te_5$), which can be switched between resistive (OFF-amorphous-RESET) and conductive (ON-crystalline-SET) states. An external heater using doped TaN material is integrated with the programmable-via as it has low thermal conductivity and high sheet resistance. The switching process is based on the programming current pulse passed through the heater.

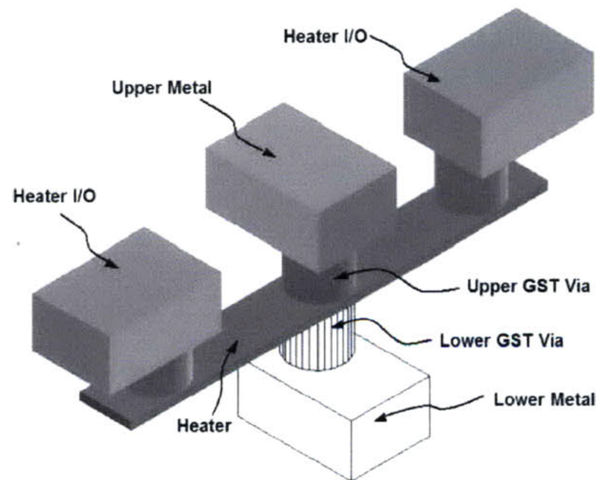


Figure 16. Programmable-via concept. Solid filled structures represent the implemented prototype device [9].

The resistance of the programmable-via in the OFF state was normally higher than 2 MΩ, whereas that in the ON state was generally lower than 60 kΩ. It is shown that the proposed device possesses a desirable ON/OFF ratio. It was shown that the ON/OFF resistance ratio remains stable at approximately 400 throughout the entire testing cycle range, which proved its

stability under the normal circuit operating conditions. The heating required to program the device is well localized to the heater/via surface. The OFF-switching thresholds depends on the via dimension and the pulse duration time. Simulation of the dependences of the OFF-current, I_{OFF} on via size and on t_{OFF} are shown in Figure 17. It follows a simple scaling prediction, which provides useful guidelines for future device performance when the feature size is reduced.

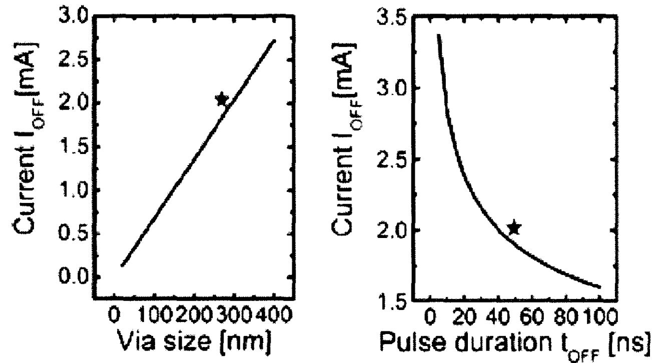


Figure 17. Simulation results of OFF-current versus the via size and OFF-current vs pulse duration [9].

This proves the feasibility of the structure to be used for reconfigurable logic applications. Addition of capping layers on top the phase change via was also proposed to act as a diffusion barrier between the phase change material and the overlying metallic features [13].

Figure 18 shows a schematic diagram illustrating a one switch unit structure design, which includes a four terminal programmable-via structure and two field effect transistors (FET) that are connected to the heater. Circuit block A and B include any conventional circuit that is capable of any logic and memory function such as a signal computing unit or a data storage unit. The gates of the FET are connected to a write line (WL). The source region or the drain region of FET L which is not connected to the heating element, is connected to a bit-line (BL). On the other hand, the source or drain region of FET R which is not connected to the heating element is always grounded. Assuming the initial state of the phase change via is ON (crystalline state), both FET L and FET R need to be turned on by applying enough current on the gates through WL. At the same time, an abrupt high current pulse is sent through BL into FET L and passes through the heating element to melt and quench/amorphize the phase change via adjacent to it. The resistance states of the PCM vias will increase and achieve the OFF state. In order to turn

PCM vias back ON, enough current has to be passed to the gates through WL to turn on both FET L and FET R. A relatively low current, but longer pulse is then applied from BL to FET L and passes through the heating element to anneal the amorphous phase change via to the crystalline state. With such, the two circuit blocks are able to communicate with each other.

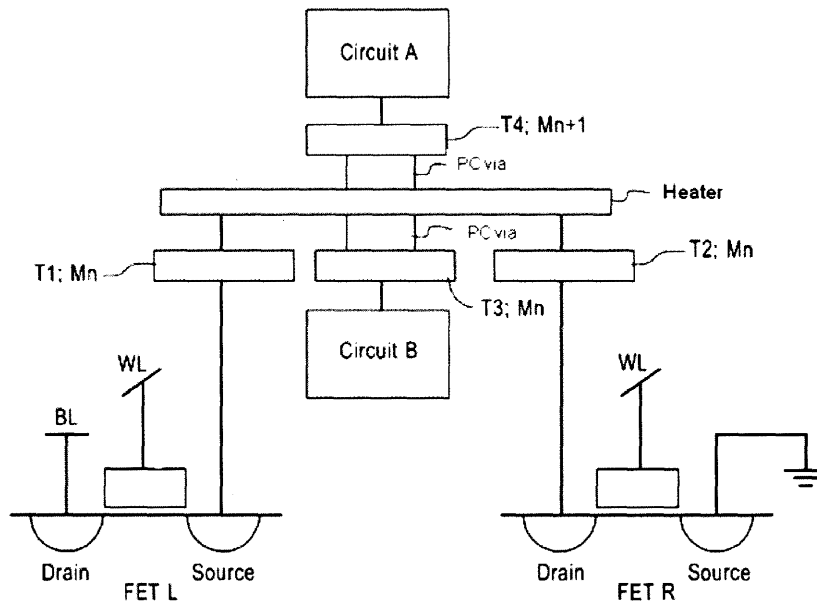


Figure 18. Schematic diagram illustrating a one switch unit structure, which includes a four terminal programmable-via structure and two field effect transistors (FET L and FET R) [14].

Chen *et al.* also proposed other designs such as programmable-via devices with air gap isolation [15]. A heat insulator is used around the heater to minimize heat loss during operation. Heat loss can undesirably increase the operating power of the device. Air has a lower thermal conductivity and thus is a better heat insulator than silicon oxides. Although no experimental data was published using the proposed structure, it was predicted that it would be able to enhance performance of a programmable-via device. However, it must be noted that these proposed ideas will complicate the processing steps. To-date, Chen *et al.* has about 25 patents covering different programmable-via designs. Details of these patents will be covered in a later chapter.

Besides the above mentioned design structure, there are other proposed architectures for multi-terminal phase change devices (PCD). Kordus *et al.* proposed two different device arrangement as shown in Figure 19 [16].

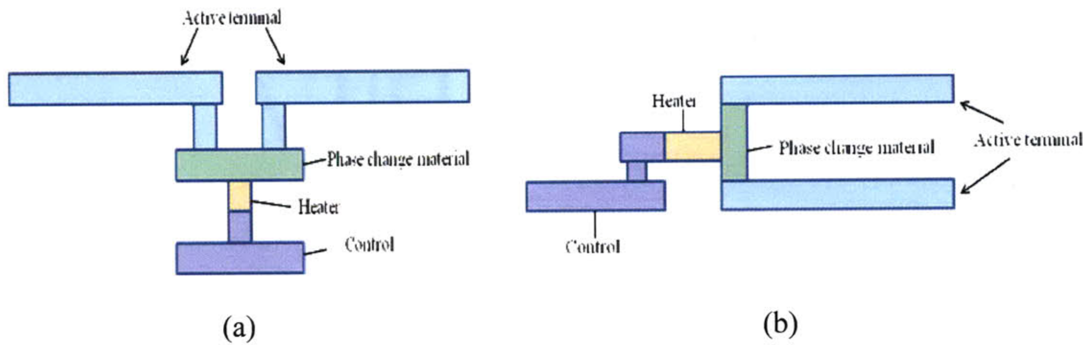


Figure 19. Schematic showing two different arrangement of three-terminal PCD, (a) stacked three-terminal PCD and (b) lateral three-terminal PCD [15].

The control terminal activates the heater, causing the change in state of the phase change material. The multi-terminal device can be used as a means of creating cross-bar or switching fabric in a programming device.

3.2.1 Programmable-via Device Fabrication

The device fabrication includes three sections using a standard CMOS technology, which includes the heater, programmable-via and electrical connection. The heater fabrication is started by depositing the doped TaN film above the silicon dioxide film on the Si wafer. After the pattern of the heater is defined on the doped TaN film by reactive ion etching (RIE), another silicon dioxide film is deposited to cover the heater. This is followed by the programmable-via fabrication. The via is defined by a lithography process and is then etched using RIE. This process requires a good etching selectivity between oxide and doped TaN. Figure 20 shows the via hole that is clearly defined and its bottom lands well on top of the doped TaN heater.

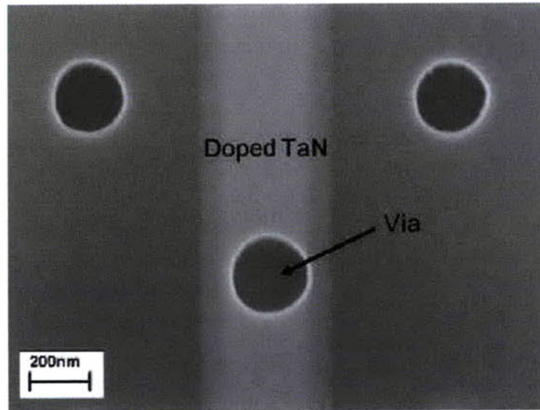


Figure 20. SEM images showing the via hole clearly defined on the doped TaN heater region [12].

After depositing TiN (acts as a diffusion barrier), Ti (acts as a adhesion layer) and $Ge_2Sb_2Te_5$ onto the via, a chemical mechanical polishing (CMP) process was performed to remove any materials outside the via. In order to prevent any contamination of the $Ge_2Sb_2Te_5$ via, a TiN cap layer which was designed to be larger than the via size was fabricated to fully cover the via. Figure 21 shows an SEM image of the device structure after the cap layer was fabricated.

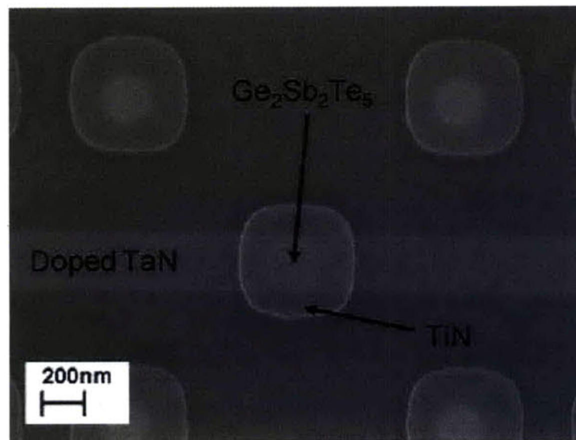


Figure 21. Top-down SEM image of the device structure after the cap layer was fabricated [12].

During the CMP process, the polishing rate of $Ge_2Sb_2Te_5$ via is higher than that of the oxide, making the region lower than the adjacent region as shown in Figure 22.

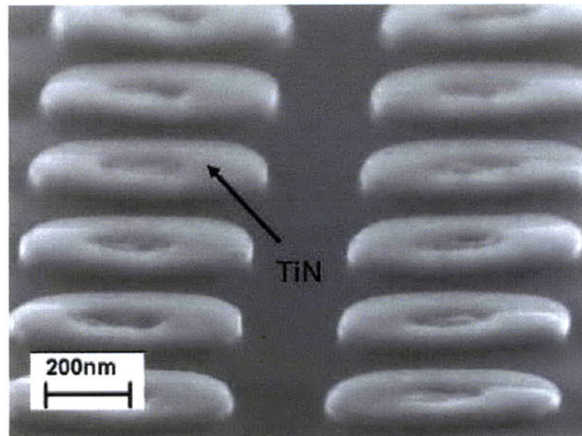


Figure 22. SEM image after the cap layer was fabricated showing that the central region of the cap layer, which corresponds to the via area is lower than the adjacent region [12].

The final section of device fabrication is the electrical connection. Two tungsten (W) vias were fabricated to connect the heater for electrical current delivery in the heater. The device structure is completed after the testing W pads were fabricated. Figure 23 shows an SEM image of the programmable-via region of the final device. Vias with diameters of 200-280 nm were fabricated atop 20 nm thick TaN heaters that had the same width as the via diameter and a length-to-width ratio of 6. The resistance of the doped TaN heater is about 1700 Ω and its resistivity is 6 x 10^{-4} Ωcm.

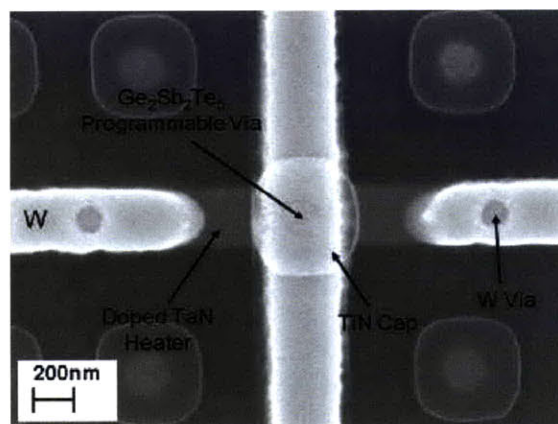


Figure 23. SEM image of the programmable-via region of the final device [12].

3.3 Important Consideration/Properties of Material Used in a Programmable-Via

3.3.1 Ge-Sb-Te (GST)

As the material used for the programmable-via possesses similar properties as that used for optical data storage, similar materials are explored. The most popular materials used for optical data storage are ternary chalcogenides such as Ge-Sb-Te. These materials are used for DVD-random access memory phase-change optical disks. The composition range of frequently used materials is along the pseudobinary line between GeTe and Sb_2Te_3. This is shown in Figure 24. Alloys on this line form a metastable rocksalt-like structure, where Ge and Sb atoms occupy one lattice site, while Te atoms occupy the second lattice site.

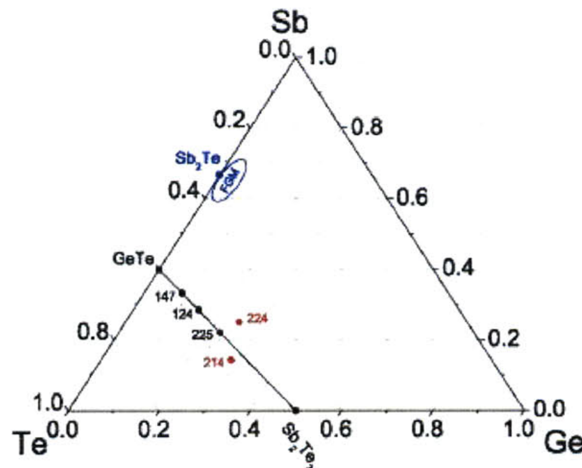


Figure 24. Typical compositions of phase-change materials [17].

The solid line shows the GeTe-Sb_2Te_3 tie line, in which many phase change alloys are located and have been explored for data storage applications. Within the class of Ge-Sb-Te materials, the compound materials, $Ge_2Sb_2Te_5$, $GeSb_2Te_4$, $GeSb_4Te_7$ and the pseudo-binary compositions at the Ge-Te-Sb_2Te_3 line in particular have short crystallization times [18]. The most currently used material for optical disk application is the Ge-Sb-Te series, especially $Ge_2Sb_2Te_5$ [19].

A phase change diagram of the Ge-Sb-Te system is shown in Figure 25. The rapid and reversible transformation between an amorphous and crystalline state without phase separation is important.

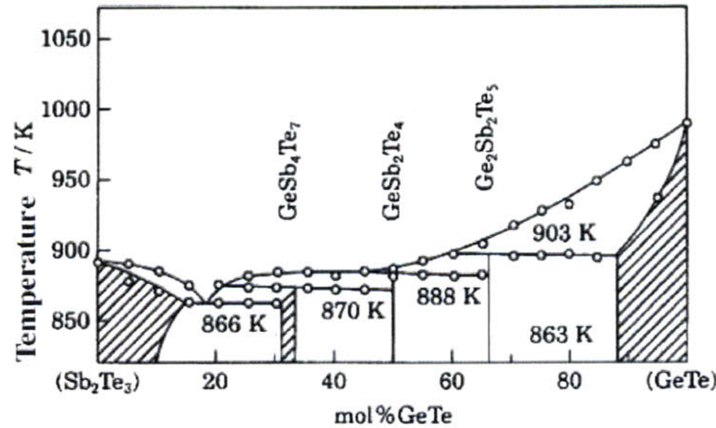


Figure 25. Phase diagram of Ge-Sb-Te [20].

3.3.1.1 Activation Energy

It was found that the $Ge_1Sb_2Te_7$, $Ge_1Sb_2Te_4$ and $Ge_2Sb_2Te_5$ compositions undergo two phase transformations, from amorphous to face center cubic structure (fcc cubic) and then from fcc cubic to hexagonal structure [21].

In optimizing the physical requirements for programmable-via, thermo-physical constants and parameters in the materials are extremely important. Activation energy, E_a, is one of the most important parameters related to the chemical reaction or transition speed. Observations of the phase transition from the amorphous to crystalline phase are usually made by two methods: optical change observation and differential scanning calorimetry (DSC). Kissinger's plot is by far the most common method used to evaluate E_a [22]. The crystallization temperatures obtained at different heating rates are used to estimate the activation energy for crystallization.

For $Ge_2Sb_2Te_5$, it is clear that the change of optical and electrical properties is theoretically reproduced by the exchange of Ge and Te layers between two states, which is $[-(Te-Sb-Te-Sb-Te)-(Te-Ge-Ge-Te)-]_n$ in the amorphous and $[-(Te-Sb-Te-Sb-Te)-(Ge-Te-Te-Ge)-]_n$ in the crystalline state [23-24]. The volume of the amorphous structure is slightly larger than the crystal. This is due to the generation of a small space or an imaginary layer for the charge balance

between the two Ge layers. For the transition between the two states, the Ge and Te layers have to diffuse into their respective layers mutually. The transition between the two states is shown in Figure 26.

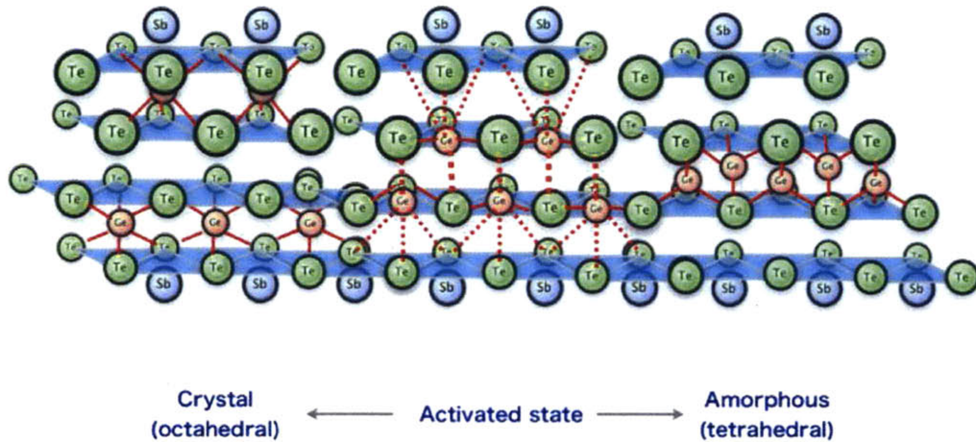


Figure 26. Three phases of $Ge_2Sb_2Te_5$ super-lattice structures. Left: crystal state composed of Ge octahedral coordination (six bonds), Center: activated state, and Right: amorphous state composed of Ge tetrahedral coordination (four bonds) [25].

Three different super-lattice models are shown in Figure 27.

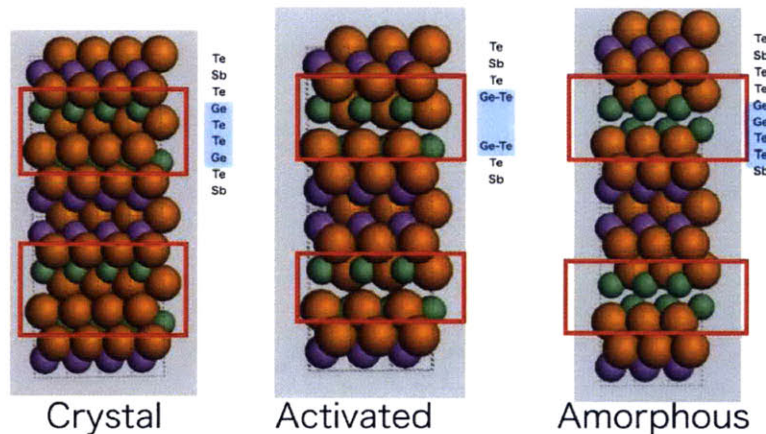


Figure 27. Three computer models for crystal (left), activated (center), and amorphous (right) states. Big, medium and small balls are Te, Sb, and Ge, respectively [25].

E_a of the alloys reflects the thermal stability and also the transition speed. A higher E_a corresponds to a higher thermal stability. However, the transition speed from crystalline to amorphous or vice versa will be slower. Therefore, a compromise between these two parameters has to be made. E_a of different Ge-Sb-Te compositions have been reported for the last 20 years. Some of the results are summarized in Table 1.

Table 1. Activation energies for crystallization of Ge-Sb-Te alloys reported in literature.

	Sample Preparation	**Method**	**E_a (eV)**	**Reference**
$Ge_2Sb_2Te_5$	Scratched single film powder	DSC	2.23 - 2.3	[19, 26-28]
	Sandwiched film on glass	Optical transition	2.5	[29]
	Single film on glass	Optical transition	2.29 ± 0.09	[30]
	-	Simulation	2.34	[25]
$Ge_1Sb_4Te_7$	Single film on glass	Optical transition	2.09 ± 0.07	[30]
	Scratched single film powder	DSC	1.52	[28]
$Ge_1Sb_2Te_4$	Single film on glass	Optical transition	2.22 ± 0.08	[30]
	Scratched single film powder	DSC	1.82	[28]

It was found that the E_a of $Ge_2Sb_2Te_5$ is the highest, followed by $Ge_1Sb_2Te_4$ and $Ge_1Sb_4Te_7$. This shows that the $Ge_2Sb_2Te_5$ exhibits a higher thermal stability. There is always a compromise between thermal stability and crystallization speed. However, the $Ge_2Sb_2Te_5$ is able to show amorphization in 20-50 ns (RESET) and crystallization in 60-80 ns [31-33] which is good enough for use as the material for the programmable-via.

3.3.1.2 Crystallization Temperature (T_x) and Melting Temperature (T_m)

The crystallization temperature (T_x) and the melting temperature (T_m) of the alloys determine the crystallization speed and amorphization speed respectively. With a higher T_x, more heat must be supplied before crystallization takes place. With such, this is accompanied by an increase in the crystallization time. Similarly, a higher T_m has been correlated with an increase in amorphization time [28]. The ease of glass formation is often found to correlate with small thermodynamic driving forces for crystallization, kinetic constraints on crystal nucleation and/or growth and also high viscosity in the undercooled liquid regime

T_x is a strong function of the material and can vary over a large temperature range depending on the materials composition. Figure 28 shows an example T_x for a series of GeSb alloys with varying Ge:Sb ratios.

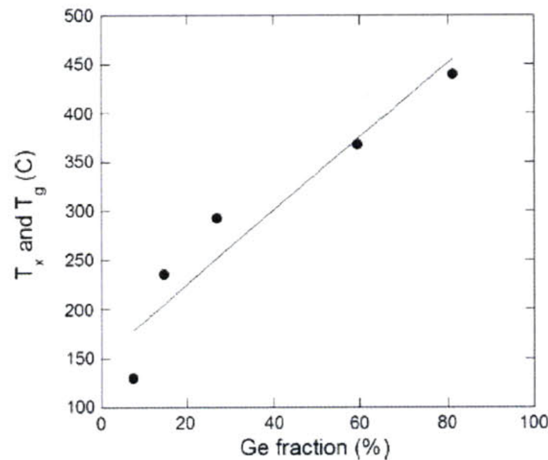


Figure 28. T_x for a series of GeSb alloys with varying Ge:Sb ratios. Dots are the experimental values, the line is the simulation for the glass transition temperature [34].

Besides composition, T_x is also affected by the materials surrounding the phase change material [35]. Figure 29 shows the structures of samples for single-layer GST film and trilayer films with GST film in between two dielectric protective films. By changing the dielectric films, different T_x were observed as shown in Table 2.

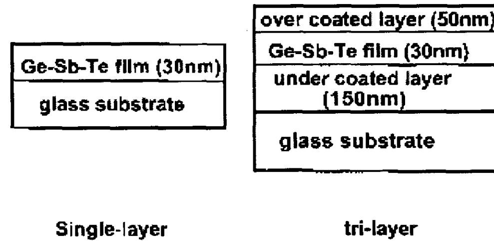


Figure 29. Structures of samples for (a) single-layer film and (b) trilayer films [35].

Table 2. Crystallization temperatures for Ge–Sb–Te films under different heating rates [35].

Heating rate (K/min)	Single layer (K)	SiO_2 (K)	Si_3N_4 (K)	Ta_2O_5 (K)	ZnS (K)	ZnS−SiO_2 (K)
5	417	422	432	416	426	421
10	421	424	437	421	430	426
20	425	432	442	424	432	429
50	432	432	444	431	438	435
90	436	437	452	434	442	439

In the paper, it was reported that chemical factors such as the reactivity and chemical affinity are responsible for the difference in the crystallization process that brings about the difference in T_x. From a microscopic point of view, these differences may originate from chemical binding states at their interface between Ge-Sb-Te film and the dielectric film used. Wettability measurements indicate that the ZnS form the binding state with the Ge-Sb-Te film whereas SiO_2 and Si_3N_4 hardly bind with it.

For thin films with thickness below 10 nm, it also depends strongly on the film thickness [36-37]. Moreover, T_x is also a strong function of the way the amorphous phase was created.

T_x and T_m of the different alloys can be obtained using differential scanning calorimetry (DSC). There are slight variations in the values obtained in different literature due to different factors described above. Table 3 shows the T_x and T_m of three stoichiometric compositions obtained from DSC measurements. It can be seen from the table that the melting points coincide well with the value for the bulk materials shown in the phase diagram of Figure 25.

Table 3. Crystallization temperature and melting temperature of three stoichiometric compositions.

	T_x (K)		T_m (K)
Composition	Ref [30]	Ref [28]	Ref [28]
$Ge_2Sb_2Te_5$	411	415	889
$Ge_1Sb_4Te_7$	383	396	887
$Ge_1Sb_2Te_4$	404	404	880

After examining the thermal properties of three stoichiometric compositions, it was found that the activation energy, crystallization temperature and melting temperature of $Ge_2Sb_2Te_5$ is the highest, followed by $Ge_1Sb_2Te_4$ and $Ge_1Sb_4Te_7$. As mentioned earlier, there is a compromise between thermal stability and switching speed. $Ge_2Sb_2Te_5$ exhibits the highest thermal stability, which might be drawback when switching speed is concern. However, reports have shown that it still exhibits good switching speed, where it amorphizes in 20-50 ns and crystallizes in 80-100 ns [31-32]. As the thermal stability and switching speed are the two most important criteria in examining material used for programmable-via, $Ge_2Sb_2Te_5$ will be used to examine its other properties to evaluate its suitability in this application.

3.3.1.3 Electronic Properties

In order to have two distinct states, the resistivity values between the amorphous and crystalline state must be a few order of magnitude different. This is important so that the via can act as a switch, ON when it is in crystalline state and OFF when it is in the amorphous state. In the crystalline state, the resistivity of the via will be low whereas the resistivity will be high when it is in the amorphous state [19]. In order to understand the different electronic properties of the two phases, the microscopic electronic structure needs to be studied.

First-principles calculations of various alloys were performed to explore the electronic properties in the metastable crystalline and amorphous states [38]. By using simple structural models for amorphous $Ge_1Sb_2Te_4$, it was shown that the observed change in coordination of the Ge atoms from octahedral to tetrahedral on amorphization results in a substantial change in the electronic valence states [38].

Figure 30 shows the temperature dependence of the resistivity in various Ge-Sb-Te alloys. All show a few orders of magnitude difference in the resistivity value between the amorphous and crystalline state.

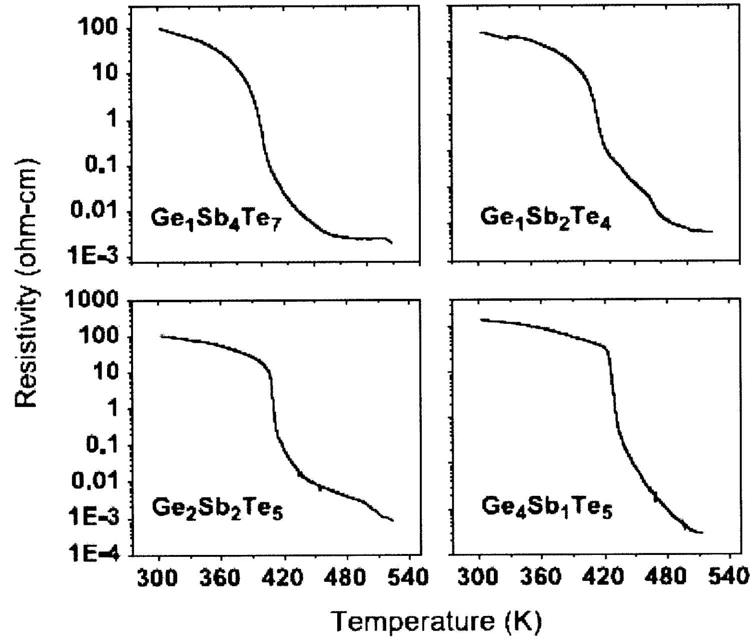


Figure 30. Temperature dependence of the resistivity in $Ge_1Sb_4Te_7$, $Ge_1Sb_2Te_4$, $Ge_2Sb_2Te_5$ and $Ge_4Sb_1Te_5$ alloys [30].

While the resistivity in the crystalline state exhibits an ohmic behavior, its characteristics in the amorphous state are far more complex. Figure 31 shows the response of a phase change memory cell in its amorphous state to an applied voltage. For a small voltage applied initially, only a marginal current flows through the cell. This is due to the high resistivity of the amorphous state and leads to rather low heat dissipation in the cell. This would in turn make the recrystallization at low voltages practically impossible. However, at a moderate voltage, the amorphous material undergoes a fast electronic transition, which leads to a much lower resistance in the amorphous state. This is also called threshold switching. When a much larger current now flows through the amorphous region, it produces enough heating to crystallize the material.

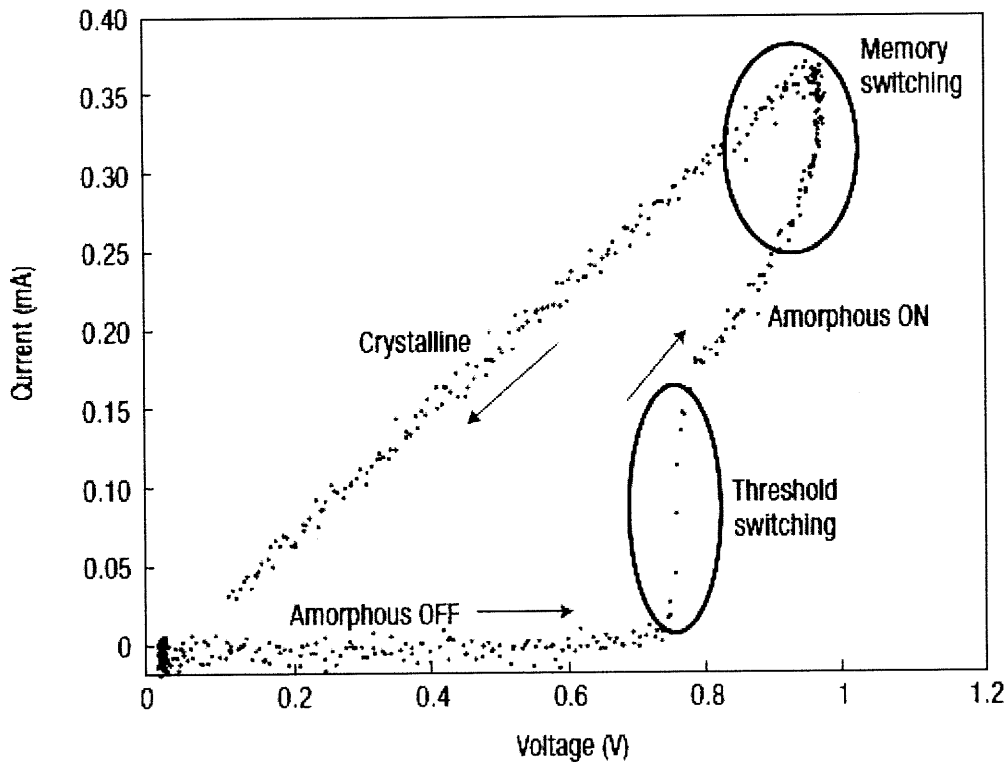


Figure 31. Typical current-voltage curve of a phase-change alloy that was initially in the amorphous state [3].

All solids show a change of electrical resistance between the amorphous and the crystalline states. For applications as programmable-via, though, the useful materials are those that crystallization can be accomplished with lower power. Hence, materials like Ge-Sb-Te alloys that exhibits threshold switching are essential.

Figure 32 and 33 show the R-I switching characteristics of a programmable-via without a switching history. In Figure 32, starting from the OFF state, 1 μs pulses with gradually increased power were applied to the heater. When the pulse current reached around 0.9 mA, the via resistance started to decrease and finally implemented switching of the device to the ON state.

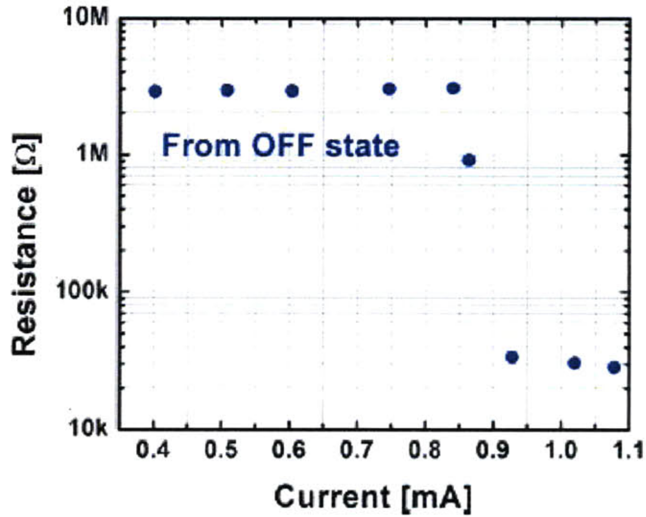


Figure 32. R-I characteristics for switching to the ON state. Via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm. ON pulse = 200 ns ramp up + 1000 ns plateau + 200 ns ramp down [39].

In Figure 33, 50 ns pulses with gradually increased power were applied to the heater from the ON state. After each pulse, the via was switched back to the ON state. When the pulse current reached around 2 mA, the via resistance started to increase and finally reached the OFF state.

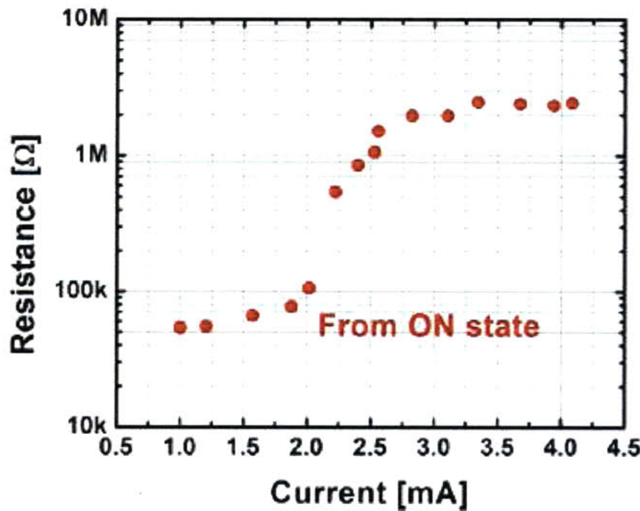


Figure 33. R-I characteristics for switching to the OFF state. OFF pulses are 19 ns rise time and 2 ns fall time [39].

In order to further understand the behavior and predict the performance of an energy-efficient programmable-via structure, several simulations were carried out and compared with the

experimental results of the prototype device. Figure 34 shows simulated required OFF currents versus programmable-via dimension. The experimental data of this device structure is marked in the figure, showing good prediction. Figure 35 shows the simulated OFF current and pulse time at plateau. The experimental data is also marked in the figure, showing good prediction within the reasonable range from the simulation. These simulation results provide references for future device performance predictions.

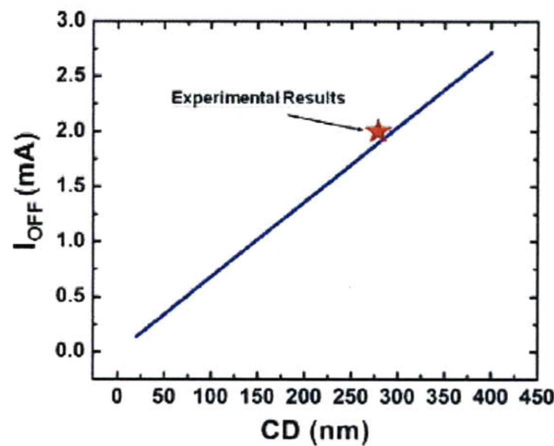


Figure 34. Simulated required OFF current and programmable-via dimension. Via size = heater width = 1/6 x heater length; heater thickness = 20 nm; 50 ns OFF pulse width with 19 ns rise time and 2 ns fall time [39].

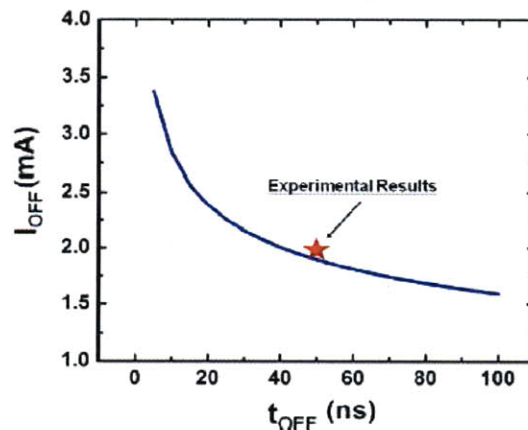


Figure 35. Simulated OFF current and pulse time at plateau. Via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm; OFF pulses with 19 ns rise time and 2 ns fall time [39].

3.3.1.4 Thermal Conductivity

From the low thermal conductivity of amorphous phase, the conductivity increases irreversibly with increasing temperature and undergoes large changes with phase transformation. Thermal transport in the amorphous and early cubic phases can be described by a random walk of vibration energy whereas in the hexagonal phases, the electronic contribution to the thermal conductivity is large than the lattice contribution [40]. There have been data that were published on a variety of materials with stoichiometries between $Ge_2Sb_2Te_5$ and GeTe [41], and $Ge_2Sb_2Te_5$ [40]. The thermal conductivity for the amorphous phase is typically between 0.15 and 0.35 W/m K and between 0.5 and 2.0 W/m K for the crystalline phases.

Even though the thermal conductivity of the phase change material has a strong influence on the thermal properties of the programmable-via, there is not much room in terms of optimization as most phase change materials have similar thermal conductivity. There does not seem to be much variability in the thermal conductivity that could lead to a substantial modification of the programmable-via thermal behavior by changing the phase change alloy. Figure 36 shows the measured thermal conductivity of amorphous and crystalline GeSbTe films using indirect [42-44] and direct [40-41, 45-46] measurement techniques. The data was usually obtained from indirect measurements of a hexagonal phase for the crystalline state. Indirect measurements were performed on $Ge_2Sb_{2.3}Te_5$ films whose crystallization temperatures were about 170°C [42], whereas direct measurements were performed on $Ge_2Sb_2Te_5$ films whose crystallization temperatures were about 130°C [40-41].

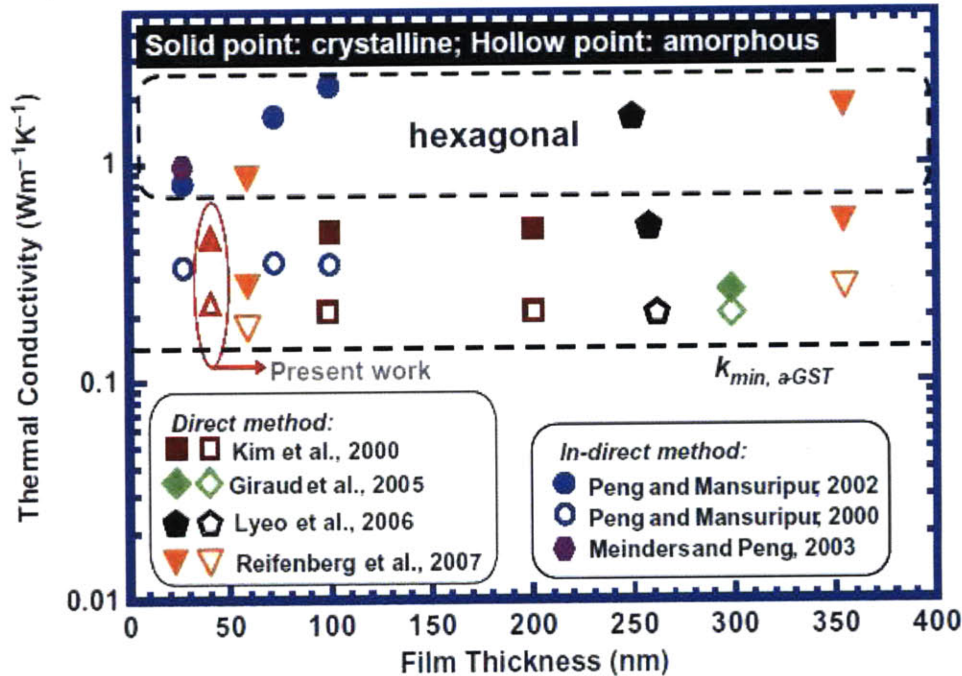


Figure 36. Measured thermal conductivity of amorphous and crystalline GeSbTe films using indirect and direct measurement techniques [47].

3.3.1.5 Mechanical Reliability

There are basically four contributing factors to the stress in GST film and PRAM devices, and which will also be present in the programmable-via interconnect. First of all, the stress present due to the mismatch of the lattice parameters of the phase change material and the surrounding materials. Secondly, the thermal stress which originates from the mismatch in the coefficient of thermal expansion of the phase change material with the surrounding material. The phase-change stress induced by the change in density [48] due to phase transformation from the amorphous to the crystalline phase is also present. Lastly, there will be residual stress due to sputter deposition. The major contributions of the stresses will be from the thermal stress as well as the phase change stress. These stresses have been calculated using finite element analysis (FEA) [49]. The hydrostatic stress can be obtained as the arithmetic average of the three normal stress components when the shear stress is zero. As the hydrostatic stress will result in volume changes, it contributes to a great threat to the reliability of interconnects. A large hydrostatic stress is known to be a driving force for the stress voiding nucleation whereas the gradient of hydrostatic

stress is a driving force for stress void growth. Compressive stresses can also lead to cracking of the surrounding material.

Figure 37 shows the stress evolution as a function of annealing temperatures for three different phase change materials, $Ag_{5.5}In_{6.5}Sb_{59}Te_{29}$, $Ge_2Sb_2Te_5$ and Ge4Sb1Te5, which are obtained from conventional wafer curvature measurement technique.

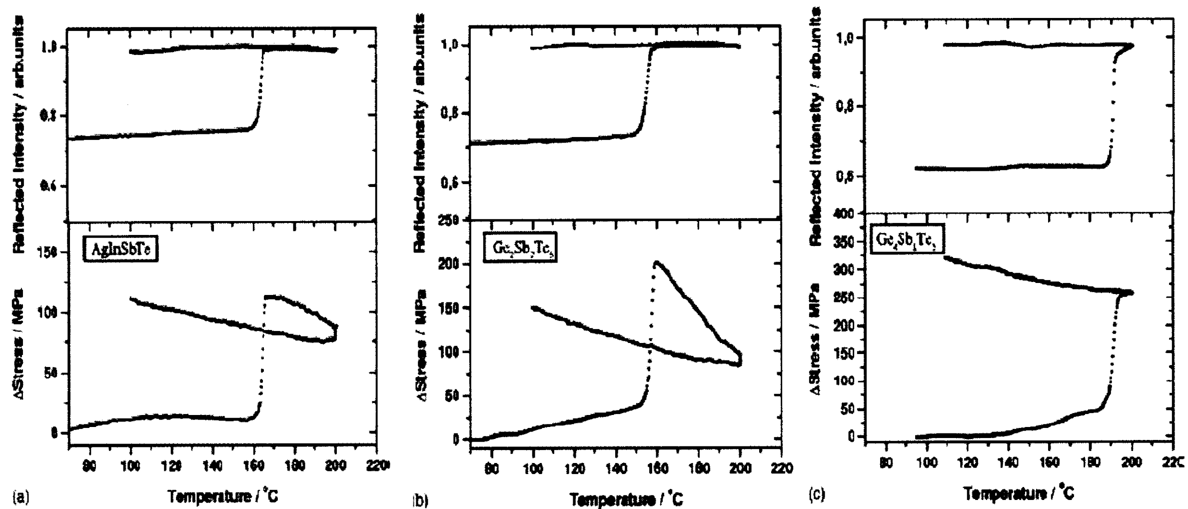


Figure 37. Stress and reflected intensity from (a) 85 nm thick $Ag_{5.5}In_{6.5}Sb_{59}Te_{29}$ deposited on a 150 μm thick glass substrate (b) 85 nm thick $Ge_2Sb_2Te_5$ deposited on a 200 μm thick Si substrate and (c) 61 nm thick $Ge_4Sb_1Te_5$ deposited on a 200 μm thick Si substrate. The upper figures of (a), (b) and (c) show the reflectivity changes of the films whereas the lower figures show the corresponding changes in thin film stresses as a function of temperature [48].

As shown in Figure 37, there is a substantial increase in the film reflectivity at their respective crystallization temperatures, indicating the crystallization of the film. It is also shown that there is a change in the biaxial film stress in the tensile direction as a result of the densification of the films upon crystallization, approximately 0.105 GPa for $Ag_{5.5}In_{6.5}Sb_{59}Te_{29}$, 0.165 GPa for $Ge_2Sb_2Te_5$, and 0.215 GPa for $Ge_4Sb_1Te_5$. With these stress data, the tensile biaxial strains associated with crystallization can be calculated to be 0.20% for $Ag_{5.5}In_{6.5}Sb_{59}Te_{29}$, 0.33% for $Ge_2Sb_2Te_5$, and 0.46% for $Ge_4Sb_1Te_5$. However, the value is substantially lower than the 2% in-plane strain estimated from the density changes values. The crystallization-induced stresses from a 2% mismatch strain will be about 1 GPa, which is higher than the reported 0.1-0.2 GPa stresses

obtained from the wafer curvature measurements. These differences indicate that most of the density changes are not elastically accommodated. Also, the majority of the stress associated with crystallization relaxes during the crystallization process.

Mechanical failure accompanied by volumetric changes, such as void and hillock formation, can be attributed to the phase-change stress as well as the thermal stress. Therefore, both stresses need to be taken into consideration for understanding the mechanism of mechanical failure and optimizing the mechanical reliability of the programmable-via device.

3.3.1.6 Endurance

The crystalline-amorphous transformation in GST is fast and gives stable performance. Figure 38 shows an example of the set and reset states of a PCM cell as a function of the programmable cycle. Each program cycles included a 40 ns reset pulse and a 100 ns set pulse. A resistance window of a factor 10^2 is retained over 10^{11} cycles. This shows the excellent stability of the programming characteristic.

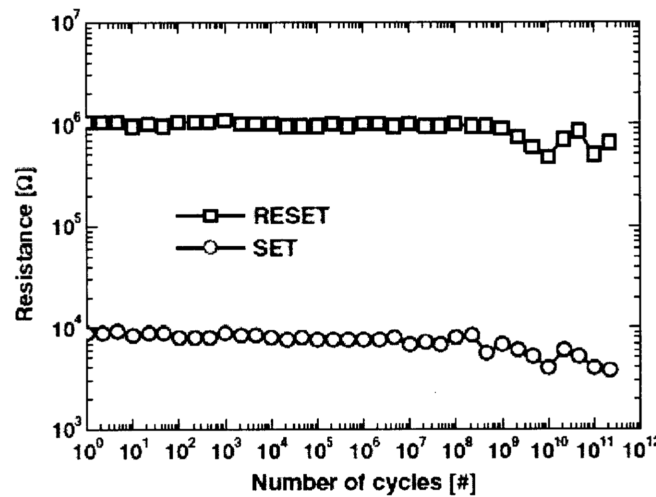


Figure 38. The resistance in set and reset states as a function of the number of cycles [50].

The remarkable endurance is related to the microscopic structure of the GST alloy. GST in the crystalline state has a rock-salt structure as shown in Figure 39.

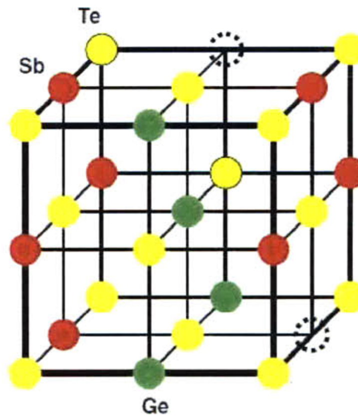


Figure 39. Schematic view of the GST crystal. Te atoms form an FCC sub-lattice, while Sb, Ge and vacancies form the other sub-lattice [31].

Based on extended X-ray absorption fine structure (EXAFS) measurements [23], it was found that the chemical short-range order of the ternary GST system is almost the same in the crystalline and amorphous state. Neither strong covalent bonds are broken nor do atoms drastically change their position in the lattice during transition.

After 10^{11}-10^{12} cycles, the PCM cell fails featuring either a stuck-set (inability to reset the cell) or a stuck-reset (inability to set the cell). The main factor responsible for this failure mode is the quality of the heater/GST interface which might lead to a physical separation of the chalcogenide alloy from the heater. Besides, the mechanism that is responsible for failure is the interdiffusion of chemical species from adjacent materials. This is called short-mode failure, where the device is permanently stuck in the highly conductive condition. Since cell programming requires high current densities, another mechanism that would impact the device endurance is electromigration . However, this is not expected to be a concern below 10^{12} programming cycles [50]. The current density and high operating temperature experience by the device act as the accelerating factors for the failure to take place. Figure 40 shows that endurance at constant programming current scales inversely with the reset pulse width. The longer the pulse, the faster the interface degradation, and the lower is the endurance.

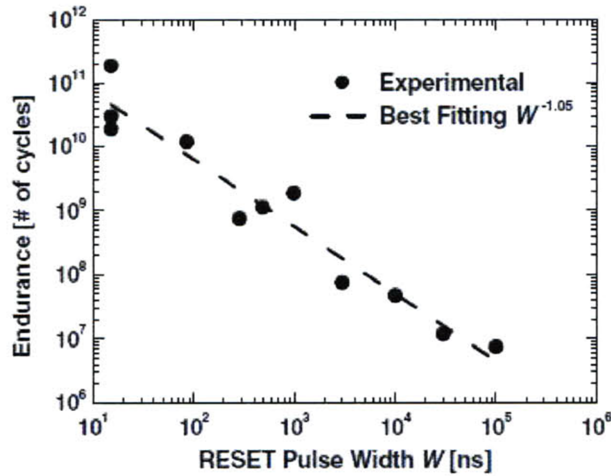


Figure 40. Endurance vs. reset pulse width [31].

An experiment was carried out using a programmable-via and Figure 41 shows the endurance test results. It shows a stable OFF/ON ratio of about 400 without obvious degradation. An estimate OFF/ON ratio of an ideal four-terminal device can reach 1000 when the resistance contribution from the heater to the ON resistance becomes small.

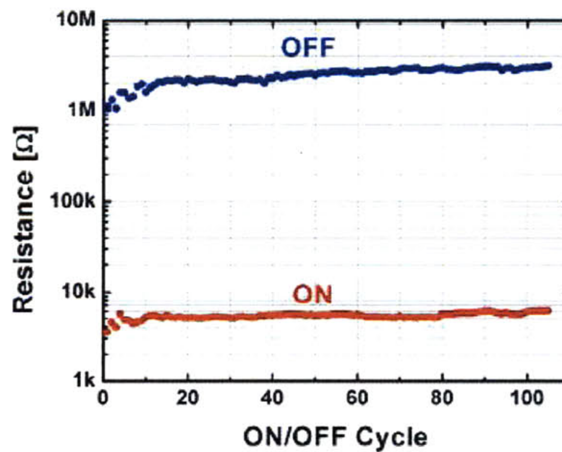


Figure 41. Cycling data from endurance tests at room temperature [39].

3.3.1.7 Electromigration

When a high electric field or current is applied to materials, electric-field-enhanced atomic transport, or electromigration will occur. The main driving force of electromigration may be

classified into two parts, the direct force of the electrostatic field on the diffusing ions (electrostatic force) and the momentum exchange between the moving charge carriers and the diffusing atoms (wind-force). In the case of metals, where there are large conducting carriers and shielding of core ions by free electrons, the wind-force effect is much greater. However, in the case of multicomponent chalcogenide materials, the electromigration behavior is different. The electromigration behavior of $Ge_2Sb_2Te_5$ in the molten and crystalline state was investigated using a pulsed dc stress [51].

Figure 42 shows a schematic view of the atomic migration due to the wind-force and electrostatic force in the crystalline and active region. It was shown that the electrostatic force-induced migration was dominant in the liquid phase. Cationic Ge and Sb ions move toward the anode, and anionic Te ions move toward the cathode. In crystalline $Ge_2Sb_2Te_5$, the mass transport of constituent elements to the cathode due to the wind-force was observed. As the bottom electrode is a cathode in typical PRAM operation, Ge and Sb atoms drift to the bottom electrode and Te drifts to the top electrode in the active region during reset operations. The study on electromigration for the mechanism of compositional variation may provide useful information to improve the endurance characteristics of phase change materials.

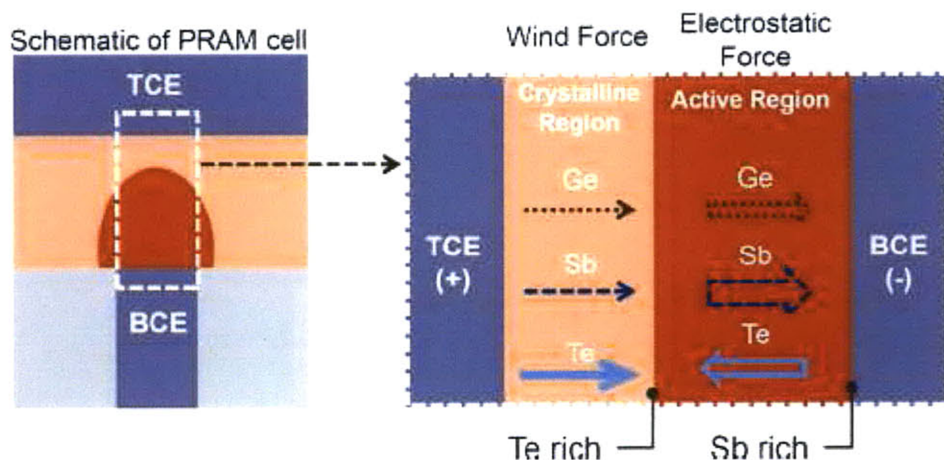


Figure 42. Schematic view of electromigration in a conventional PRAM cell. Te is accumulated between the crystalline and the active region, and Sb is accumulated above the bottom contact electrode [51].

3.3.2 Doped Ge-Sb-Te

Many studies have shown that doping the GST system can improve the properties and performance of phase change material based devices. Antimony (Sb), Molybdenum (Mo), Silicon (Si), Silver (Ag), tin (Sn) and Nitrogen (N) have been reported to improve the properties of the Ge-Sb-Te system [27, 33, 52-59]. Among these, Sn and N are the two most commonly used.

Incorporation of Sn into the Ge-Sb-Te (GST) system has shown advantages such as lowering of the crystallization and melting temperatures [33]. With such, a lower SET and RESET current is needed. A higher crystallization speed is also observed [56-57]. This might be due to the fact that the weaker bonding of Sn-Te (359.8 kJ mol^{-1}) can accelerate the crystallization rather than the GST containing stronger bonding of Ge-Te (397 kJ mol^{-1}). However, it faces problems such as a lowering in Δ R and decrease in stability of amorphous state at high temperature [57]. Other properties such as endurance and electromigration have not been explored.

On the other hand, incorporation of N into the GST system shows a better stability with higher activation energy [27, 59]. However, it shows a higher crystallization temperature so that a higher RESET current is needed [27, 58-59]. Higher resistivity in both phases are observed due to the reduction of the grain size in the crystalline state [58]. Similar to the case of Sn-doped GST, endurance and electromigration issues have yet to be studied.
Although doping GST has shown some advantages over conventional GST, more studies need to be carried out to explore its potential to be used as the material for the programmable-via device.

3.3.3 Ag-In-Sb-Te (AIST)

The Ag-In-Sb-Te system is also among the promising candidates used in high speed and high density optical recording media. It gives direct overwrite capability within a short period of time and is reported to give a well-defined shape with edges and increases the linear density [60]. A composition close to $Ag_5In_5Sb_{60}Te_{30}$ is frequently used in rewritable optical storage media [3]. In AIST system, Ag contributes to the thermal stability [61] with an activation energy of 2.9 – 3.03 eV [62-63] compared to about 2.3 eV for the GST system. This, on the other hand, contributes to a high speed phase change due to the weaker binding energy of In and In-Sb [61].

It also shows a significant difference in resistivity when it is in amorphous and crystalline state [62]. An overwrite cyclability of more than 10^5 times was also reported [64]. Compared to the GST system, less research work has been carried out to study this material system.

3.3.4 Comparison of Ge-Sb-Te (GST) and Ag-In-Sb-Te (AIST)

Both GST and AIST show similarities and differences in crystal structure and dynamic function. Both have high-symmetry crystal structures enabling them to crystallize at fast rates. The amount of amorphous material remaining after crystallization is about the same in both systems, and very small, indicating that most of the alloy in both systems can be completely crystallized [65]. Both showed good erase times with GST materials having a better erase performance than AIST. Table 4 shows a comparison of properties between the GST and AIST materials systems.

Table 4. Comparison between GST and AIST material systems.

Properties	**GeSbTe**	**AgInSbTe**
Application	Land-groove	Groove-only
Activation Energy (eV)	~ 2.3	~3.0
Tc	150°C	200°C [66]
Crystallization Speed	Comparable, GeSbTe exhibits slightly faster speed	
Δ R	GeSbTe exhibits more prominent contrast	
Cyclability	GeSbTe generally one-two orders of magnitude better [67]	
Electromigration	AgInSbTe might have more problem due to the additional element	
Others	Marks written on AgInSbTe have a well defined shape and sharp edges – lower jitter values [67]	

Generally, GST shows better combined properties compared to AIST for use in a programmable-via. Also, more research has been carried out on this material system. This will be extremely useful in understanding the properties of GST and in assessing its suitability as the material for the programmable-via.

3.4 Technological Advantages

Phase change programmable-via can be reversibly switched between an amorphous state and a crystalline state quickly, and is highly capable of continuous changing its phase, which shows reprogrammability. Most importantly, it is nonvolatile, unlike SRAM-based technology. Besides, it is also compatible with conventional processes of manufacturing of silicon-based devices. There is no need to invent an entire new manufacturing chain. It also has a relatively low on-state resistance. The unit F is commonly used to indicate the area of a device. The cell area of a switch device, including PRAM, is 8F2 or less, which is much smaller than that of an SRAM and a pass-gate, 120F2. The cell area can therefore be reduced to 1/15 that of the conventional switch device. However, it must be noted that in programmable-via designs, two additional FETs for each via must be taken into consideration to control the heater element. Therefore, the space saving will not be as great as in the case of PRAM. Having said that, it still occupy less real estate on the chip as the "switches" are placed at the metallization layer instead in the substrate. It therefore provides flexibility for the designer to place the switches. Programmable-via can operate at a relatively low voltage compared to that in FLASH-based technology. Similar to the case of antifuse, programmable-via interconnect structures are projected to be radiation hard. Table 5 shows the comparison of the phase change via concept with current technologies.

Table 5. Comparison of phase change via with current technologies.

Feature	SRAM	Antifuse	FLASH	PC Via
Technology node	State-of-the-art	One or more generation behind	One or more generation behind	Novel concept
Reprogrammable	Yes (in system)	No	Yes (in system or offline)	Yes
Volatile	Yes	No	No	No
Requires external configuration file	Yes	No	No	No
Instant-on	No	Yes	Yes	Yes

IP Security	Acceptable	Very good	Very good	Very good
Size of configuration cell	Large (6T)	Very small	Small (2T)	Small (2T)
Power consumption	High	Low	Medium	Low

3.5 Technological Challenges and Limitations

Although the programmable-via concept looks promising to create a new kind of FPGA, there are several challenges and limitations for such technology implementations. As a heater element must be incorporated into the design, additional processing steps are required compared to that of SRAM-based systems. Reliability issues such as electromigration are still not fully understood. The effect of volume changed due to the phase transformation has yet to be established.

The most challenging part of implementation is the circuit design. Current proposed designs and work are still in an early research stage. A proof of concept on a single via is very different from building a whole reconfigurable chip. Issues such as integration of materials in the process need to be overcome. Besides, there are also issues pertaining to integration with current tools. A lack of expert personnel in this area also makes the implementation of programmable-via FPGAs complicated.

There is also risk involved in the FPGA design as reliance on third-party Intellectual Property (IP) and re-use of common IP cores from other programs are unavoidable.

4 Market Analysis

4.1 FPGA Market Analysis

The value of worldwide FPGA shipments is expected to increase from $1.9 billion in 2005 to $2.75 billion by 2010, with much of the revenue coming from low-volume shipments, according to high-tech market research firm In-Stat. [66]. FPGA revenue is projected to grow to nearly $3.5 billion in 2013 from $2.55 billion in 2009, a faster growth rate than is anticipated for the broader IC market, according to a study released by market research firm The Linley Group [67]. Figure 43 shows the FPGA/Programmable Logic Devices (PLD) combined revenue by year.

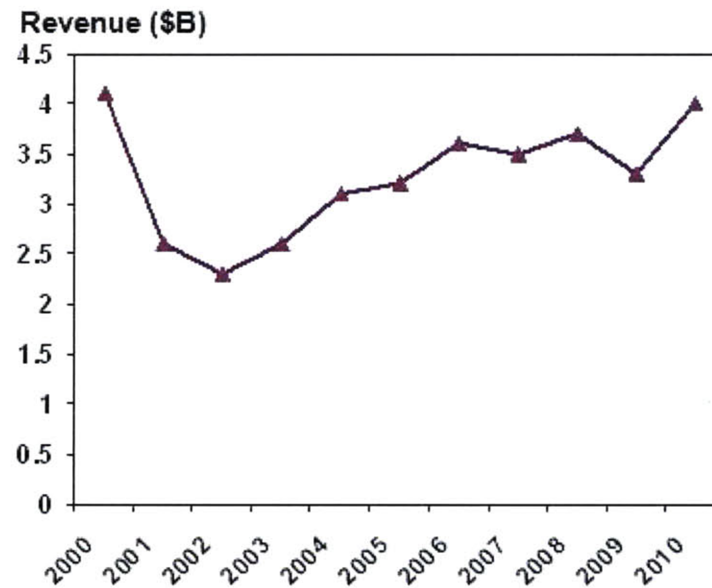


Figure 43. Total FPGA/PLD revenue by year [68].

The report, titled "A Guide to FPGAs for Communications," concludes that FPGAs are likely to continue displacing ASICs and application-specific standard products (ASSPs) for many applications. However, FPGAs cannot compete with the cost advantages of ASICs for many high-volume applications, such as those found in video-game consoles, set-top boxes and other consumer applications.

An analysis of the end-user markets provides a picture of the overall PLD market shipments. Vendors report sales in approximately similar categories. Figure 44 gives an overview of the PLD market by end applications.

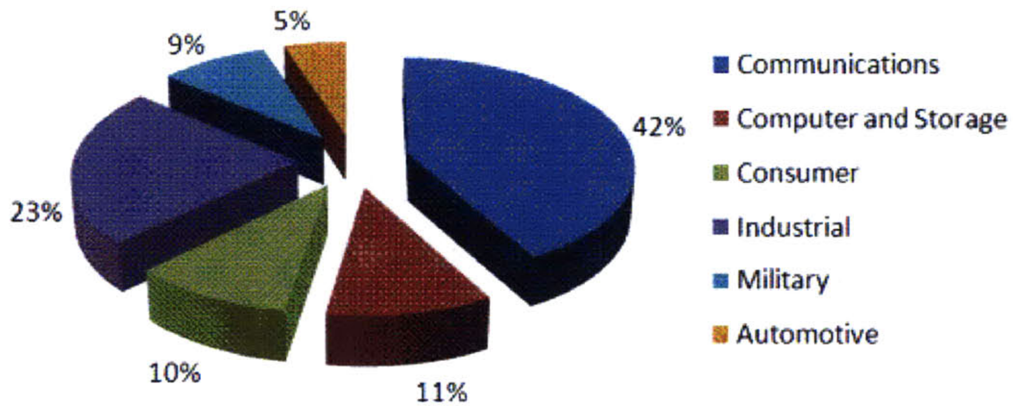


Figure 44. PLD market by end applications Q3CY09 [69].

Figure 45 shows the PLD market segment share from year 2005 to 2009 and Figure 46 shows the worldwide FPGA/PLD vendor revenues in year 2007-2008.

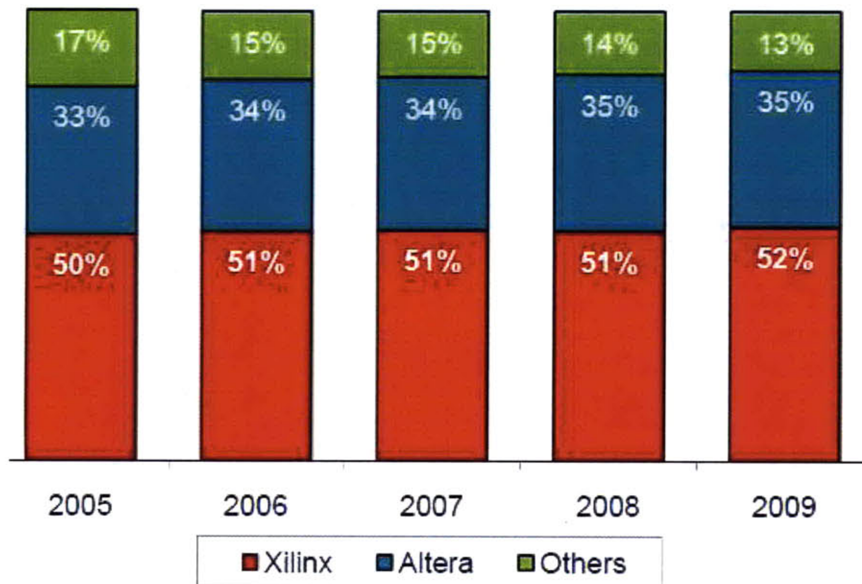


Figure 45. PLD market segment share from year 2005 to 2009 [70].

Worldwide FPGA/PLD vendor revenues and rankings, 2007-2008

Rank 2007	Rank 2008	Company	Revenue ($M) 2007	Revenue ($M) 2008	Revenue Change 2007-2008	Market Share 2008
1	1	Xilinx	1,809	1.906	5.4%	51.2%
2	2	Altera	1,216	1,323	8.8%	35.5%
3	3	Lattice Semiconductor	229	222	-3.1%	6.0
4	4	Actel	196	218	11.2%	5.9%
6	5	QuickLogic	28	23	-17.9%	0.6%
5	6	Cypress Semiconductor	32	21	-34.4%	0.6%
7	7	Atmel	14	9	-35.7%	0.2%
8	8	Chengdu Sino Microelectronics System	4	3	-25.0%	0.1%
		Others	0	0	NM	0.0%
		Total Market	**3,528**	**3,725**	**5.6%**	**100.0%**

Source: Gartner

Figure 46. Worldwide FPGA/PLD vendor revenues and ranking, 2007-2008 [71].

The FPGA market has been in a duopoly situation, dominated by the two main companies, Xilinx Inc. and Altera Corp. for a number of years. In 2008, according to Gartner Inc,, both companies hold together 87% of the market of programmable logic. The two companies compete across a wide spectrum of the available market, but completely dominate the lucrative high-performance sector. They are joined at the cost-sensitive end by smaller players such as Lattice Semiconductor and Actel Corp, at 6% each. New market entrants Achronix, SiliconBlue and XMOS have started shipping products and their strategies and market positioning are analyzed in "The FPGA Market Report" prepared and published by High Tech Marketing. All these players are fabless semiconductor companies.

4.2 Business Opportunity for Enterprises on Phase Change Reconfigurable Interconnects

There have been numerous attempts to challenge the comfortable equilibrium between these two FPGA giants. The number of FPGA start-ups increased after the 2000 downturn. Figure 47 shows the history of PLD start-ups. Over the past 7-10 years, venture capitalist founded FPGA start-ups one after another. Besides the attraction of the programmable logic market that has been

growing a healthy 8-11%, compared to a stalled ASIC market, the availability of engineers and executives have been a factor in driving more venture capitalist money into FPGA start-ups [71].

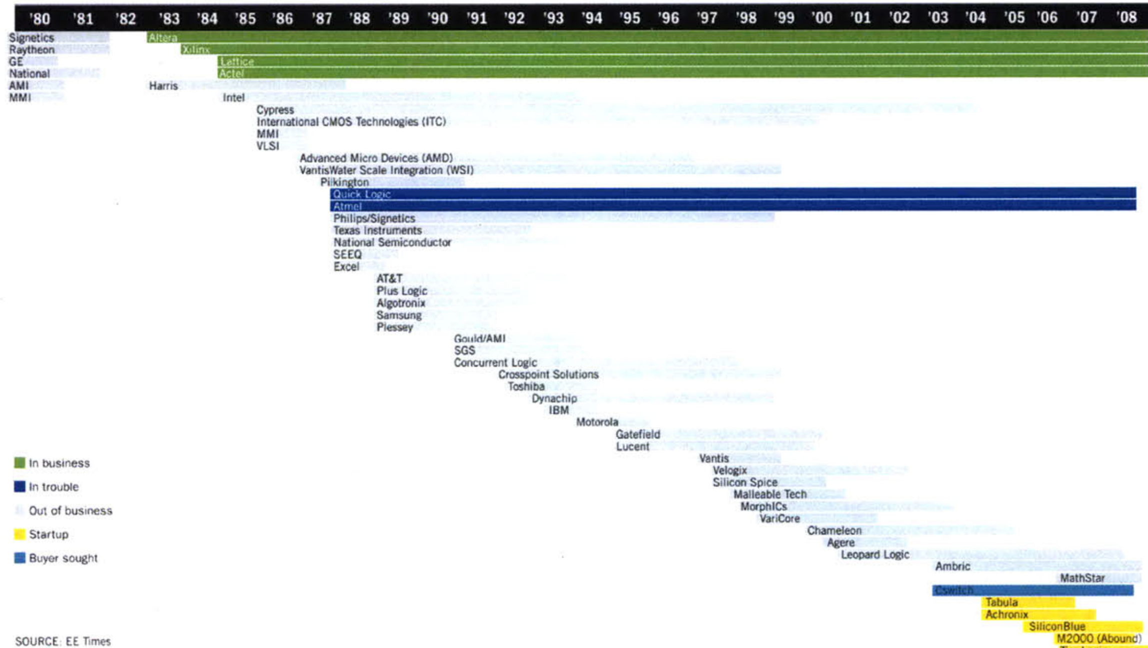


Figure 47. History of PLD start-ups [71].

As shown in Figure 47, most of these start-ups die after a few years. These includes Chameleon Systems, which died in 2002, the promising Velogix (formerly known as Flexlogics) that was created in 2002 which eventually ran out of funds, Ambric Inc whose assets were acquired by Nethra in 2008, Mathstar Inc which stopped operation in 2008 and CSwitch which stop business in 2009.

However, there are still a number of active FPGA start-ups. Among which includes Tabula, Achronix, SiliconBlue, Tier Logic, Abound Logic (formerly known as M2000). Tabula went through a full reset and raised a considerable amount of money. SiliconBlue on the other hand aims at low power applications.

So far, attempts to jeopardize the duopoly have failed. From the failed examples, it is learnt that any new venture needs to come with a significant differentiation if it wants to challenge the existing companies. Many FPGA start-ups came out with claims of higher densities and better clock cycles. Start-ups that claim 2x of higher density eventually have to face the harsh reality that the two big companies just need to move to the next technology node to match or substantially reduce the performance claims. Moving to the next technology node is certainly more accessible to these companies than to a start-up for which a new mask can consume half of a second- or third-round financing. Thus, in order to compete with them, start-ups must come up with a more than 2x density improvement. It is important to introduce software that can exploit that extra density to deliver better results. And also for most applications, density is less important compared to power consumption. Power reduction is therefore an important driver.

Phase change reconfigurable interconnect has shown its advantages over current technologies as discussed in previous chapter. Not only increasing the density, it offers much more flexibility for the designer to place the programmable-via that acts like a switch. It is not restricted to the real estate area but instead makes use of the metallization layers. Having said that, this novel idea is still at the very early stage of research and a proof of concept on a single via is very different from building a whole reconfigurable chip. In order to penetrate into the FPGA market in the future, much more research and studies need to be carried out. Besides identifying the combination of materials used in the architecture, alternative designs need to be explored. After which, the most challenging part would be to integrate these into a real FPGA design with the aid of computer software. As what Chen, the first to produce a prototype device said, it could take up to three to five years before a phase-change FPGA makes it to market [72].

5 IP Analysis

5.1 US Patent Overview

According to my personal statistics, there are close to 30 US patents directly related to the phase change via concept used for reconfigurable interconnect in FPGAs. The majority of these patents have been filed within the last 3 years. As this is a novel concept and researchers have just started to explore the feasibility of such technology, there are not many patents filed yet. Having said this, it is predicted that more patents related to this area will be filed soon. Chen *et al.* from International Business Machines Corporation (IBM) hold the majority of the filed patents. They have come out with different proposed layouts of the phase change via design.

5.2 Analysis of the Patents

Table 6 shows patents filed that are related to the phase change via concept. The majority of the patents proposed using phase change material as the via for the reconfigurable interconnect. By utilizing the properties of phase change materials, it can act as a switch and is reprogrammable. The advantages of this design were discussed in earlier chapter.

Table 6. List of the patents that are related to phase change via concept.

Patent No.	Patent Title	Patent Publication Date	Inventor
0108977 A1 [73]	Nonvolatile Programmable Switch Device Using Phase-change memory Device and Method of Manufacturing the Same	May 6, 2010	Yoon et al., Electronics and Telecommunicati ons Research Institute
0091560 A1 [16]	Multi-terminal Phase Change Devices	Apr 15, 2010	Louis et al., JW Law Group
7,365,355 B2 [74]	Programmable Matrix Array with	Apr 29, 2008	Ward Parkinson,

	Phase-change Material		Ovonyx Inc.
0097343 A1 [75]	Programmable Matrix Array with Phase-change Material	May 11, 2006	Ward Parkinson, Ovonyx Inc.
0038621 A1 [10]	Four-Terminal Reconfigurable Devices	Feb 18, 2010	Chen et al., IBM
0014885 A1 [76]	Four-Terminal Reconfigurable Devices	Jan 15, 2009	Chen et al., IBM
7,659,534 B2 [15]	Programmable Via Devices with Air Gap Isolation	Feb 9, 2010	Chen et al., IBM
0305460 A1 [77]	Programmable Via Devices with Air Gap Isolation	Dec 10, 2009	Chen et al., IBM
0033360 A1 [78]	Programmable Via Devices with Air Gap Isolation	Feb 5, 2009	Chen et al., IBM
7,652,278 B2 [79]	Programmable Via Structure and Method of Fabricating Dame	Jan 26, 2010	Chen et al., IBM
0311858 A1 [80]	Programmable Via Structure and Method of Fabricating Dame	Dec 17, 2009	Chen et al., IBM
0142775 A1 [81]	Programmable Via Structure and Method of Fabricating Dame	Jun 19, 2008	Chen et al., IBM
7,579,616 B2 [82]	Four-terminal Programmable Via-containing Structure and Method of Fabricating Same	Aug 25, 2009	Chen et al., IBM
0251778 A1 [83]	Four-terminal Programmable Via-containing Structure and Method of Fabricating Same	Oct 16, 2008	Chen et al., IBM
0303786 A1 [14]	Switch Array Circuit and System Using Programmable Via Structures with Phase Change Materials	Dec 10, 2009	Chen et al., IBM

7,608,851 B2 [84]	Switch Array Circuit and System Using Programmable Via Structures with Phase Change Materials	Oct 27, 2009	Chen et al., IBM
0277644 A1 [85]	Switch Array Circuit and System Using Programmable Via Structures with Phase Change Materials	Nov 13, 2008	Chen et al., IBM
0111263 A1 [86]	Method of Forming Programmable Via Devices	Apr 30, 2009	Chen et al., IBM
0101882 A1 [13]	Programmable Via Devices	Apr 23, 2009	Chen et al., IBM
0033358 A1 [87]	Programmable Via Devices in Back End of Line Level	Feb 5, 2009	Chen et al., IBM
0003045 A1 [88]	CMOS Process-compatible Programmable Via Devices	Jan 1, 2009	Chen et al., IBM
0072213 A1 [89]	Programmable Via Structure for Three Dimensional Integration Technology	Mar 19, 2009	Elmegreen et al., IBM
7,511,532 B2 [90]	Reconfigurable Logic Structures	Mar 31, 2009	Narbeh et al., Cswitch Corp.
0224260 [91]	Programmable Vias for Structured ASICs	Sept 18, 2008	Schmit et al., Easic Corp.
0091630 [92]	Programmable Interconnect Structures	Apr 28, 2005	Raminda Udaya Madurawe

From Table 6, it is obvious that IBM holds most of the phase change via related patents, which is about 70% of the list. Most of the earlier patents suggested using phase change materials as a switch without going into detail about the layout of the device. However, Chen *et al.* from IBM came up with more detailed structures of the reprogrammable device. The way to fabricate it was also proposed. Four-terminal devices consist of the two terminals that control the heater and two terminals to connect the phase change via. Simple one programmable-via structure is shown.

However, these patents are all limited to just one programmable-via, which is not realistic for large scale production. Nevertheless, it provides good background for future work to build a more complex FPGA system using this phase change via concept. Yoon *et al.* from the Electronics and Telecommunications Research Institute proposed a nonvolatile programmable switch device using a phase change memory device [73]. Louis Charles Kordus *et al.* also proposed a multi-terminal phase change device which is similar in concept with those from Chen *et al.* [16]. The resistance of the heater element can be increased independently from the resistance of the path between the two active terminals. This allows the use of smaller heater elements and thus requiring less current to create the same amount of Joule heating per unit area. The resistance of the heating element does not impact the total resistance of the phase change device. The detailed working mechanism was discussed in an earlier chapter.

To date, the patents filed only propose phase change material to be used as a reprogrammable switch. The latest patents are mostly focusing on the simple concept of using phase change material as the via that acts as a switch.

5.3 IP Opportunities for New Business in FPGA Market

There is a huge IP space to be explored in this area which utilizes the phase change via concept. There are many opportunities in the materials aspects as there is no patent that covers the detailed analysis of the material used for the phase change via. They only mentioned that phase change material in general can be considered. Besides, more complex design layouts have yet to be proposed. Therefore, there is minimal risk of any patent infringement and more patents can be filed for devices that use the phase change via concept. This enables acquirement of some portion of the IP landscape in this area that could be utilized in the future for economic gain by licensing and collection of royalties if other companies are interested in the proposed idea. Given the low risk of any patent infringement, there exist a good opportunity to license the patents to interested companies. It is therefore important to produce good patents so as to pursue companies to adopt this novel concept due to its attractiveness and benefits of this technology. This is possible as analysis of single programmable-via shows promising results. However, before this can be achieved, more thorough studies and research must be carried out to substantiate this

concept. Most importantly, there is a need to show that this concept is workable in more complex design layouts.

6 Commercialization Potential

6.1 Business Model

There are basically three different business models. First of all is the traditional integrated device manufacturer (IDM) model. Until the 1980s, the semiconductor industry was dominated by independent IDMs. They have their own wafer fabrication facilities and internally developed design tools to make and package integrated circuits [5]. These companies include firms such as IBM, Motorola, Texas Instruments, Siemens and Intel.

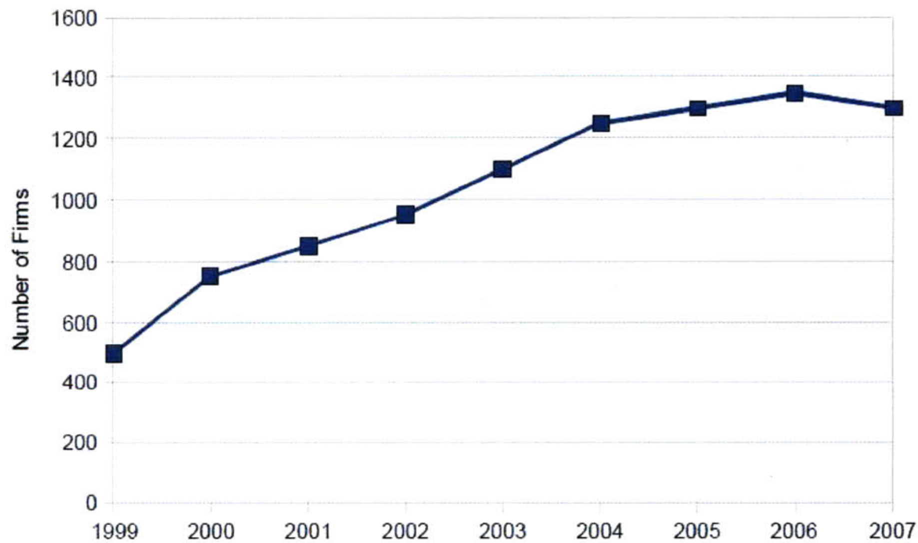
The second business model emerges as a variation of the IDM model, which is the fabless model. It is based on close collaboration among specialist semiconductor fabrication firms or foundries and device producers that operate without having their own fabrication plants. Today, it is getting to be more common for IDMs provide their chip manufacturing to companies that do not have their own fabrication facilities. IDMs that extensively use wafer fabrication outsourcing are often described as following a "fab-lite" business model. Currently, more and more IDMs are transforming themselves toward the fabless model. For example, in 2007, Texas Instruments announced that it will stop its internal development at the 45 nm process and will rely on its foundry partners to create chips in the more advanced process nodes [93]. In October 2008, AMD announced that it will become a fabless firm [94]. The foundry firms are those that enable the fabless business model in the semiconductor industry. All new semiconductor manufacturers launched after 1990 have been fabless firms that rely on their foundry partners to fabricate their products. Table 7 shows the top ten foundries worldwide by revenue in year 2007.

Table 7. Top 10 foundries worldwide by revenue in 2007 (millions of dollars).

Rank 2006	Rank 2007	Company	Revenue 2006	Revenue 2007	Growth (%) 2006-2007	Market Share (%) 2007
1	1	TSMC	9,716	9,828	1.2	44.3
2	2	UMC	3,191	3,263	2.3	14.7
4	3	SMIC	1,465	1,550	5.8	7.0
3	4	Chartered Semiconductor	1,527	1,445	-5.4	6.5
5	5	IBM Microelectronics	688	605	-12.1	2.7
8	6	Vanguard	398	488	22.6	2.2
10	7	X-Fab	293	411	40.3	1.9
6	8	Dongbu HiTek	462	405	-12.4	1.8
7	9	MagnaChip	404	370	-8.4	1.7
9	10	Hua Hong NEC	300	321	7.0	1.4
		Top 10 Total for 2007	**18,444**	**18,686**	**1.3**	**84.2**
		Others	3,201	3,506	9.5	15.8
		Total Market	**21,645**	**22,191**	**2.5**	**100.0**

Source: Gartner (April 2008).

The total number of fabless firms as reported by the GSA is shown in Figure 48.



Source: GSA, 2008.

Figure 48. Number of fabless semiconductor firms from year 1999 to year 2007 [5].

IDMs and fabless companies cannot be compared simply by using the generated revenues. The attractiveness of the fabless model is that foundries can amortize their plant and R&D costs

among many customers. IDMs have to generate much more revenues than the fabless firms as they have to cover additional fixed asset costs.

The third model is the chipless model that focuses on creating and selling designs. The key characteristic of the semiconductor IP business is that it does not transfer ownership. Instead, they sell rights to use and copy the designs. These designs include "virtual components", "IP blocks" and "IP cores". The revenue typically generated from license fees, royalty payments and complementary services, such as training, technical support, customization and development tools. Table 8 shows the semiconductor IP licensing models.

Table 8. Typical semiconductor IP licensing models [5].

	Per Use	Time Based	Royalty Based	Access Based
Purpose	Fee for each IP on defined user scope	Multiple uses over a period of time	Share risk and reward	Fee for an IP portfolio over a period of time
Payments	Event Based	Time Based	Value Based	Subscription Based
Structure	One time fee	Fee for all designs within a given time	Some or all fees spread across units	Up Front Fee plus discounted use fee
Scope	Per Design Per Device	Multiple Uses Per Device	% of Device Value	Multiple IPs per Organization

Semiconductor IP blocks are licensed by different types of firms. Foundries will provide large libraries of pre-designed and pre-tested IP that is optimized for its fabrication process. Such IP consists of basic logic components and "standard cells" and also complex IP cores developed by third-party IP vendors. A special case among fabless firms is the FPGA vendors. FPGA chips provide a platform onto which different designs can be downloaded. Designers now typically use IP blocks provided by the FPGA vendor as components in their designs due to the increasing complexity of implemented designs. The semiconductor IP industry consist of a large variety of rapidly evolving business models. Chipless-model or pure-play IP vendors do not have their own products but they focus on creating and licensing designs to chip designers. These IP blocks are typically used by independent design service firms and fabless semiconductor firms and also licensed by traditional IDMs.

6.1.1 Review of the Business Model Adopted by Current Players

Currently, the FPGA market is dominated by two companies, Xilinx and Altera. Xilinx was founded in 1984 by two semiconductor engineers, Ross Freeman and Bernard Vonderschmitt, who were both working for integrated circuit and solid-state device manufacturer Zilog Corp. Bernie Vonderschmitt, an engineer and an MBA graduate came up with a powerful business model as he was convinced that semiconductor factories were expensive and burdensome [95]. He came up with the fabless idea and was convinced that finding partners who can do the manufacturing was not a difficult task. And this was exactly what Xilinx did in year 1984. They have pioneered the fabless manufacturing model, inventing the FPGA and ranking among the world's leading patent holders. As FPGAs are becoming more like a system, it is almost impossible for a single company to build all the components of a system. Xilinx therefore depends on external foundries to manufacture their chips. Currently, they are working closely with United Microelectronics Corp. (UMC) and Toshiba. Xilinx being the leading provider of programmable platforms had $1.8B in revenues in fiscal year 2010 and more than 50 percent market share in the programmable logic device (PLD) according to the market analysis firm iSuppli Corp. Their technology responds to the new realities of business by allowing their customers to move quickly. Getting innovative new products to market is just a matter of weeks.

Altera also employs the fabless model. It depends on Taiwan Semiconductor Manufacturing Co (TSMC) to manufacture its chips. Altera enhances its own place-and-route design software with tools from best-in-class electronic design automation vendors. Other FPGA vendors also adopt the fabless model. Such a model is good for start-up companies in the sense that it does not cost a lot of money. As long as the company owns good intellectual properties, it would easily draw attention from the manufacturers of the industrial supply chain.

6.1.2 Business Model Proposed for New Companies in the Market

The evolution of business models in the semiconductor industry has been greatly influenced by the fact that IC fabrication costs have been rising fast and very large investments are now needed when new leading edge manufacturing plants are set up. The IDM model is definitely unsuitable for new companies that want to penetrate into the market. This is due to the high initial

investment for setting up the fab. Figure 49 shows the increase in the fab start-up cost with increased complexity.

Figure 49. Fab start-up cost with increased complexity [96].

At the 32 nm technology node, a single fab can cost $4B and in just two years it will need to be upgraded (to the tune of around a billion dollars) to support 22 nm production. It is therefore impractical for a start-up company to adopt this model.

The fabless model can be considered for a start-up company in the FPGA market as this is the model that most companies adopt. However, due to the past history of PLD start-ups discussed in the previous section, it is not easy to jeopardize the duopoly in the FPGA market.

The third model, the chipless or IP model, seems best suited for an FPGA start-up company. A new company should therefore emphasize on establishing good IP. As discussed in an earlier section, there is a big IP space for new discoveries in the phase change via concept, both in the materials and the design aspect. By doing so, it is more probable for the company to attract investment from major semiconductor manufacturers on developing the prototype structures and devices, so that less initial investment is needed and the risk involved is much lower. When the technology becomes more matured and the concept becomes more established, the company can then consider whether to expand and switch to the fabless model.

6.2 Supply Chain – Manufacturing and Partnership

Figure 50 shows a schematic diagram of the supply chain for FPGA production. IP generation will be the first step, followed by circuit or product design. Once this is established, it will be supplied to the semiconductor foundry for production. Finally, the product will be put out in the market.

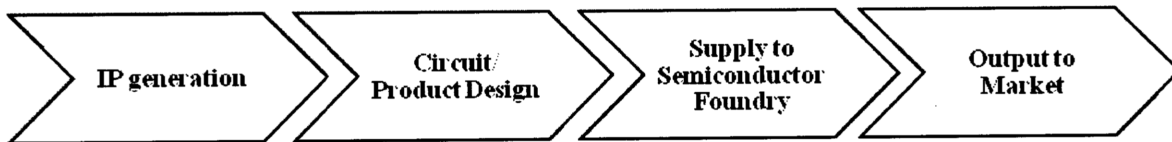


Figure 50. Schematic diagram of the supply chain of the FPGA production.

For a start-up company that intends to penetrate the FPGA market, emphasis will be on the first two steps in the supply chain. As mentioned before, most effort should be placed in generating good and solid IP for the phase change via concept. It was reported that IDM companies have started to show interest in buying an FPGA vendor. According to a JP Morgan Securities Wall Street analyst in a report titled "Top 10 Semiconductor Predictions for 2010", Intel may be soon in the market to acquire an FPGA supplier [97]. Although these giant companies are more interested in acquiring established FPGA companies, new ideas that are able to revolutionize the FPGA sector will be of interest to them too. When successful in attracting interest from giant IDM companies, royalty fees for licensing can be a few percent of the total revenue of the licensee. By doing so, the total royalty income is sufficient to keep the company going, after which, the company can start to explore circuit or product design. These designs can then be supplied to semiconductor foundries like what is done by all other FPGA companies. It is therefore important to build alliances and relationships, partner with other companies and leverage on their expertise.

6.3 Financing Start-up

Venture capitalists and other early professional investors are willing to risk their entire investment only if there is a realistic possibility exists that their investment will be multiplied

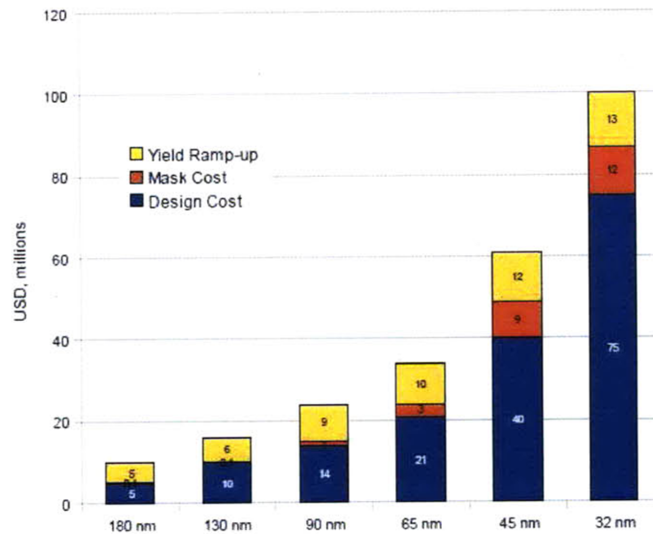
many times. Thus, businesses that can initiate or dominate markets that can grow only $5 or $10 million are not of interest to venture or seed funds in most cases. Bank financing is not usually available to start-ups. Major venture capitalists should be targets for financing. It is common to be offered only $50-100k at the seed stage, and $250-750k in the first full investment round. Before this is achieved, initially funds can be obtain from individual investors but these are generally inadequate and professional financing relationships need to be developed as early as possible. In our case, the government or commercial R&D funding is an important source of early stage financing.

Before seeking any sort of financial support, it is important to name a management team with financial, marketing and if possible technical leadership. Although this team may not yet all be on-board, it is important to have letters and accompanying vitae indicating that they will join the start-up, and on what basis and conditions. Also, it is necessary to review all of the legal aspects of the business. It is extremely important to make sure the intellectual property underlying the business concepts does not infringe the rights of others. Patents and trademark applications should be filed before seeking financing. This is to prevent proprietary ideas being exposed. Good confidentiality agreements for potential investors need to be developed for them to sign and how much proprietary information that will be exposed to investors and at what stage of the negotiations must be decided.

Having said that, the phase change via is a novel concept at a very early stage of development. Much more research effort is needed before commercialization takes place. Fundamental research on the materials and design of the circuits is the main concern in successful implementation. In Singapore, initial funding of research activities for this area started in 2009, which is funded by the Singapore-MIT Alliance (SMA). A research proposal has been submitted to other government agencies, such as A*STAR in Singapore, to support this research area. With continued funding, further improvement on the materials aspects and design layouts can be achieved. Only when coming closer to the commercialization phase, should other funding agencies which include venture capitalist funding be considered.

6.4 Cost Analysis

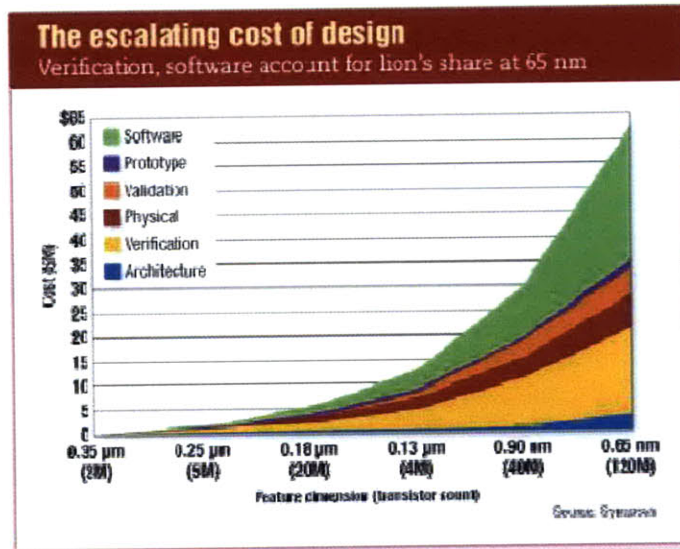
Figure 51 shows the IC design cost at different processing nodes. It is obvious that the design cost is escalating as the designs become more complex. A chip with millions of transistors cannot be designed without the help of automated tools.



Source: Data from Chartered, Synopsys, GSA

Figure 51. IC design costs at different process nodes [5].

As the complexity of designs increases they also become increasingly difficult to test it. In addition to software costs, verification costs have been increasing rapidly as new technology generations are introduced as show in Figure 52.



Source: Synopsys.

Figure 52. Design cost breakdown [5].

In order to have an idea of the cost involved in FPGA design, a design sample was co-developed by Altera with engineers at Galorath, creators of SEER-SW, SEER-H and SEER-IC software. These tools allow users the flexibility to enter parametric descriptions of the equipment designs and to develop cost and schedule estimates for both proposal development and resource planning [98]. The estimates were based on knowledge databases developed by Galorath and various users of the SEER-series software tools.

As the phase change FPGA is proposed to compete with antifuse and other approaches, a military FPGA design example was used to provide an estimation of the cost involved. The FPGA design example allows the user to estimate the program cost and schedule, measure progress and control costs as shown in Figure 53. Also, it allows the user to look at the total impact of software productivity as an independent variable.

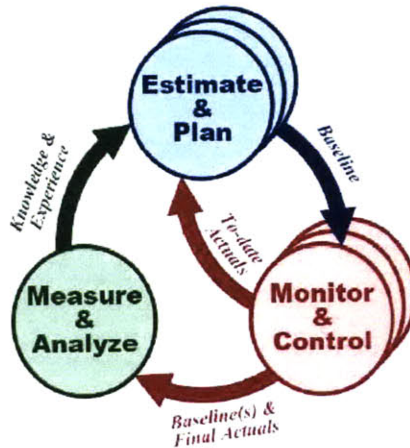


Figure 53. Galorath's Design Estimation Tools Can Be an Integral Part of System-Level Cost Control [98].

By using some assumptions, Table 9 shows the total cost of the military reference design in both hours and dollars, using a placeholder labor hour cost. This serves as a good basis cost for estimating both the impact of software on program cost, as well as potential savings from other programs.

Table 9. Reference military FPGA cost [98].

Development	Hours	Cost
Architectural design	1886.9	$378,660
Detail design	4745.1	$952,210
Simulation, verification, and implementation	5376.3	$1,078,870
Place and route	1809.2	$363,050
Total	**13,817.7**	**$2,772,800**

Galorath's SEER-IC tool divides the cost into architectural design, detail design, simulation, verification and implementation and place and route. The total labor effort for this application comes out to about 13,800 hours at a nominal cost of $2.7 million.

In terms of manufacturing, a phase change via in FPGA will incur extra cost compared to that of the SRAM based FPGAs as additional processing steps are needed. However, it provides more benefits as discussed in earlier chapters. Also, its production will be compatible with conventional processes of manufacturing silicon-based devices.

6.5 Productivity Risks

Several different productivity risk factors are present which includes personnel shortage, uncertain development schedules, lack of product support, IP re-use and integration, and also system verification. The most important is the shortage of trained design personnel. As this is an entirely novel concept, there are not many experienced personnel that are available. Also, the length of development schedules is difficult to estimate. As this is an entirely new concept, there will definitely be a lack of product support even if it makes it to the market.

When designing the entire FPGA, besides using one's own IP, there is a need to rely on third-party IP specialists and the re-use of common IP cores from other programs so as to achieve a sensible cost reduction. This is a well established risk.

System verification is the other portion of system design that becomes a significant cost risk with design growth. The number of verification steps increases with the number of interconnects and potential block IP states [98]. Test cases might grow exponentially if not controlled and defined intelligently. It is therefore advisable to take an incremental approach to redesign and recompile of the design when problems are discovered or requirements redefined in verification. If not, burdensome compile times will pose a significant risk to the program schedule and resources.

7 Summary

Phase change materials are examined for use as via materials in reconfigurable interconnect structures. The ability of this technology to be commercialized has been investigated from different perspectives including technological aspects, market, IP space and the business model to be adopted. Based on the analysis, this technology is found to be suitable from technological point of view. The material possesses desired properties for such an application. The phase change reprogrammable-via is nonvolatile, has a relatively low on-state resistance and occupies less real estate on the chip. It provides flexibility for the designer as they are placed in between the metallization layers. Programmable-via can operate at a relatively low voltage and similar to the case of antifuse, it is projected to be rad hard. However, the most challenging part of implementation is the circuit design. Issues such as integration of materials and design with current tools need to be overcome. Also, a lack of expert personnel in this area makes the implementation of programmable-via FPGAs complicated. There is an attractive FPGA market. A chipless model is preferred for start-up companies as there is a great IP space in this area, especially in the material aspect and also the design of the device. This model is desirable as it has lower risk and a possible of high return. However, this concept is still at a very beginning stage of investigation and not much work has been published in this area. More research work needs to be carried out to further show the reliability of such a technology as pioneering work has only illustrated proofs of concept with single vias. Although it is still far from commercialization, this initial investigation shows that this technology has a good prospect for commercialization in the future.

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