Current Limiters based on Silicon Pillar un-gated FET for Field Emission Application

by Ying Niu

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Author _____
Department of Electrical Engineering and Computer Science
July 16, 2009

Certified by _____
Akintunde Ibitayo Akinwande
Professor of Electrical Engineering
Thesis Supervisor

Accepted by _____
Arthur C. Smith
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Theses

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Abstract

This research investigates the use of vertical silicon ungated field effect transistors (FETs) as current limiters to individuallycontrol emission current in a field emitter and provide a simple solution to three problems that have plagued field emission arrays—emission current uniformity, emission current stability and reliability. The ungated FET is an high aspect ratio silicon pillar individually connected in series with silicon or carbon nanofiber (CNF) emission tip. The transistors were designed as high aspect ratio silicon pillars in order to achieve velocity saturation of carriers and obtain current source-like characteristics. Device and process simulations were initially conducted to solidify the derived analytical model and optimize design parameters. Devices were fabricated and characterized in the Microsystems Technology Laboratory. The main outcome of this study is that individual control of field emitter current is feasible using un-gated FETs based vertical Si pillars.

Thesis supervisor: Akintunde Ibitayo Akinwande
Title: Professor of Electrical Engineering and Computer Science

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Chapter 1 – Introduction

1.1 Background

Current-limiting devices are essential components to the operation of most electronic circuits. For functional current limiters, the circuit designer often resorts to the simple but inferior resistor or uses a three-terminal transistor. The third terminal is frequently a disadvantage because it requires an additional voltage bias supply and space. The best available two-terminal current limiter has been a field-effect transistor with the gate tied to the source and it occupies a finite area.

A more viable solution is to build a two-terminal un-gated field effect transistor (FET) that utilizes velocity saturation in Si or Ge when they are biased at high fields to provide current-limiting function. Figure 1 shows the electron drift velocity versus electrostatic field relationship in silicon [1].

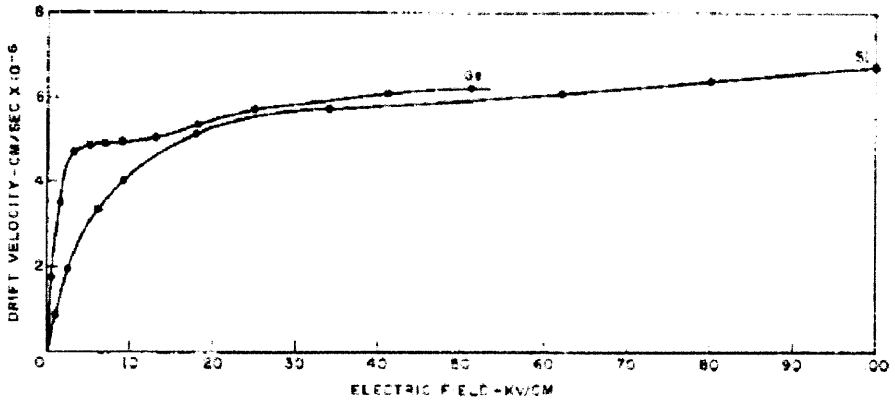

Figure 1. Electron drift velocity in germanium and silicon
The electron drift velocity versus electric field relationship in silicon shows velocity saturation occurring at high electrostatic fields [1].

In previous research, current limiters based on high-field saturation of electron-drift velocity in germanium have been fabricated [2]. These current limiters were fabricated by making two closely spaced ohmic contacts to a lateral surface n-layer diffused into the Germanium substrate. Similar attempts for current limiters based on high-field saturation of electron-drift velocity in silicon met with only limited success. There are other examples of GaAs un-gated FETs acting as current-limiters were seen in the work of Baek, et al [3].

Vertical un-gated FETs were formed by exploiting the physics of velocity saturation at high fields in the high aspect ratio silicon pillars. Voltage is applied across very high aspect ratio structure and generates a very high electric field in regions of the structure. The application of a high electrostatic field results in the saturation of the velocity of electrons in the channel of the transistor. At low drain-to-source voltages i.e. when electrostatic fields in the channel are below saturation field , the transistor has a triode or resistor-like behavior. At high drain-to-source voltages, i.e. when the electrostatic field in the channel is above the saturation field, the transistor behaves as a current limiter.

Un-gated FETs can be formed by adding electrical contacts at both ends of the pillars. High aspect ratio silicon pillars with dimensions of 100μm height and cross-sectional area of $1\mu m^2$ (100μm x 1μm x 1μm) were fabricated using a MEMS-based deep trench forming technology.

The high-aspect ratio silicon pillars act as current limiters and consequently were used in this research to control emission current in field emitters, depicted in Figure 2.

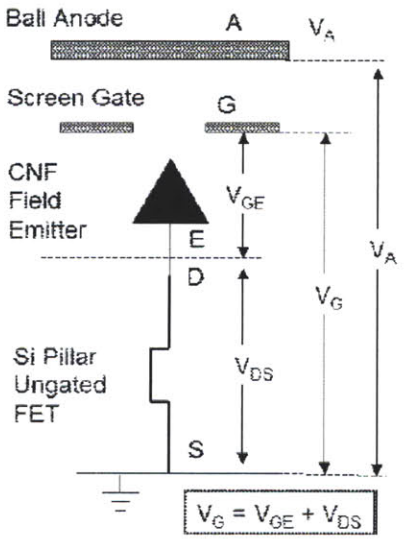

Figure 2. Schematics of field emitters ballasted with un-gated FET
The equivalent circuit diagram is depicted for un-gated field effect transistor ballasted with carbon nano-fiber field emitters [4].

Field emission is the quantum-mechanical phenomenon of electrons tunneling from a pointed source into vacuum. Electrons are field emitted from the surface of metals or semiconductors when the surface potential barrier is deformed upon the application of a high electrostatic field. Field emitters use high aspect ratio structures with nanometer-scale tips to generate very high fields at low applied voltages [5]. The high electrostatic field narrows the potential barrier, allowing electrons to tunnel into vacuum.

The field emission process, depicted in Figure 3, could be thought as a two step process consisting of a flux of electrons to the surface and a transmission of electrons through the surface barrier described by a transmission probability.

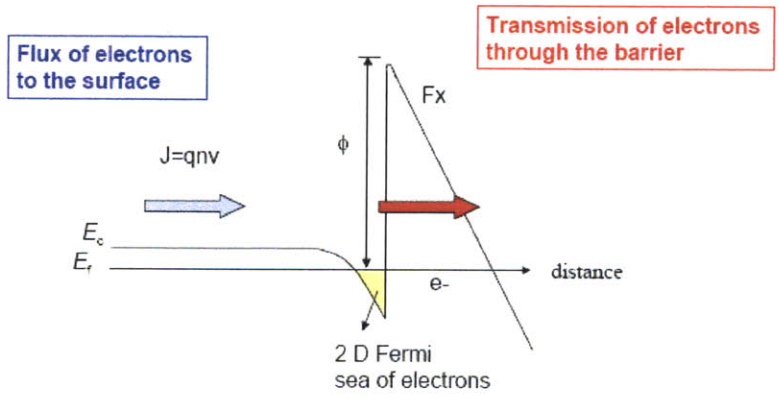

Figure 3. Electron emission energy band diagram model
Electron emission at the surface of n-type silicon is depicted [6].

Field emission device consists of sharp emitter tips as cold cathodes that emit electrons to a collecting electrode (anode). The sharp tips are arranged in two dimensional matrix-addressable arrays, also known as field emission arrays (FEAs). Figure 4 illustrates a typical field emission device structure. Voltage is applied to the gate while the tip is grounded. The tip surface experiences high electrostatic fields due to the voltage applied at the gate. As a result of the high electrostatic field, electrons tunnel from the tip through vacuum to the anode metal structure.

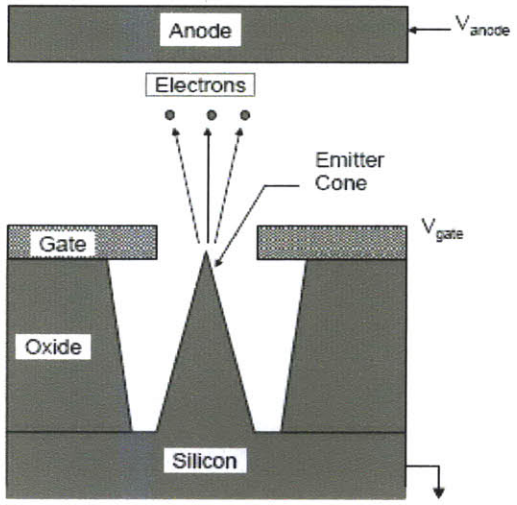

Figure 4. Basic Field Emitter Structure
Emitter structure with tip grounded and voltage applied to the gate to produce a high electrostatic field at the tip. Upon the applied field, electrons travel in vacuum towards the anode screen [7].

One of the most remarkable aspects of field emission theory is the prediction of very high emission current densities. High emission current densities are possible due to two factors [8]: minimal energy is required for the emission process when the electrons tunnel from the solid through vacuum; a large reservoir of electrons near the Fermi level of metal can sustain a very high current flow of electron from the semiconductor surface through vacuum interface.

Another important aspect of field emitters is that the scale down of devices leads to a significant reduction in the operating voltage. Early Spindt field emitters with gate apertures of 1μm operated in the range of 100-300V [9]. In recent years, along with the advancement of lithography and thin film deposition technology, field emitters fabricated by Pflug at MIT reported 70-nm gate aperture silicon FEAs with gate voltage of 10-15V [10]. The reduction in the operating voltage of the FEAs to 10-15 V enables the control of the electron source by high speed current limiters.

High current density, energy efficiency and low operating voltage aspects of field emission devices afford a variety of electronic device applications. Among the research and commercial uses, field emitter devices applies to areas of flat panel displays [6], power amplifiers, as well as microwave power devices, image sensors and electron sources. Furthermore, the development of high aspect ratio electron sources with uniform and high current density would enable new power amplifiers that operate in the upper millimeter wave frequency range and source amplifiers that operate in the terahertz range [11].

1.2 Motivation

While FEAs have been proposed as promising devices for applications as displays and microwave devices, they encounter serious problems with stability, uniformity, and reliability. For example, emitter-tip meltdown often immediately destroys the tested displays.

Another major difficulty for large field emitter arrays is that the emission current is highly sensitive to slight variations of the surface potential barrier. The shape of the potential barrier is determined by several factors including the tip geometry and applied voltage. Due to the small device geometries, small fluctuations in the barrier height can cause significant changes in emitted current resulting in non-stable operation.

Non-uniformity of field emitter tip geometry due to variability in the fabrication process can also result in large spatial variations of the emission current and output current

density. Studies of the distribution of Si field emitter tip found a log-normal distribution of the tip radii [12].

This result implies that without a feedback mechanism, the tips would emit different currents at a particular gate voltage. As the gate voltage is increased, more tips turn-on; however, the tips that turned on at lower voltage may suffer destructive burnout due to Joule heating at very high current densities. The net effect is that even though more tips are turned-on as the gate voltage is increased, the early burn out of the sharper tips limits the overall current.

This phenomenon illustrating the field emission current versus gate voltage with tip radius as a parameter is shown in Figure 5. At any particular voltage, only a small percentage of the emitter tips contribute to the observed emission current [6].

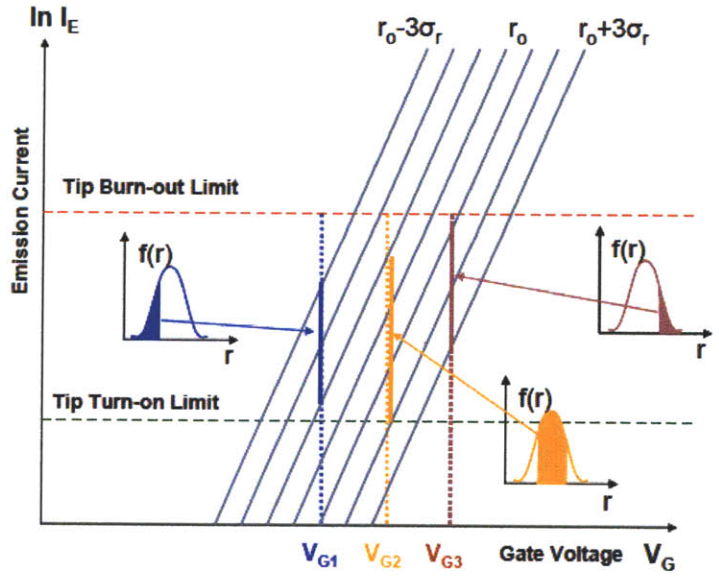

Figure 5. Tip radii, emission current and voltage relationship
Emission current versus gate voltage is plotted for varying tip radii. For tip radii with log distribution and constant gate bias, only a small percentage of the tips contribute to the total emission current [6].

Making all emitter tips uniform is impractical. The slightest tip radii variation leads to huge variations in the current because of the exponential dependence on the tip radius. Instead of aiming to obtain uniform tip radii, negative feedback is employed to overcome the non-uniformity in emission current due to tip radii distribution.

To limit the range or variations in emission current, two types of resistors were proposed to ballast FEA emitter. One is a lateral resistor located on an insulated substrate. The other is a vertical resistor imbedded below the emitter tips. The vertical resistor could maintain high emitter array density and high resistance; the drawback is low resistance because the spreading current reduces effective resistor length [13]. In contrast, the lateral resistor has resistance but at the cost of low emitter array density [14]. Figure 6 (a) shows the current ranges that result from ballasting the FEAs using resistors.

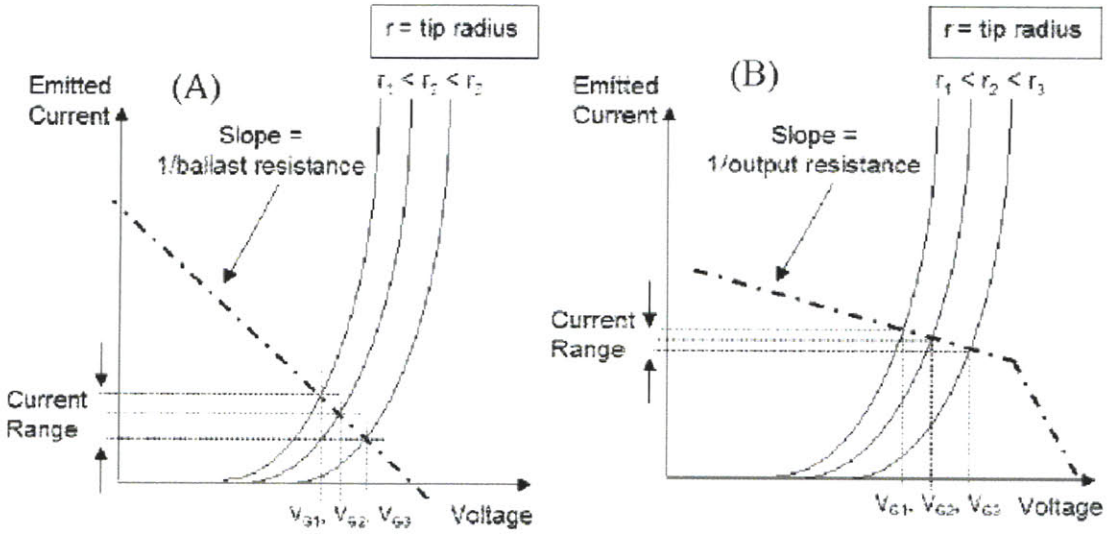

Figure 6. Un-gated FET/FEA concept
(a) Ballasting of the FEAs using resistors is shown on the left (**b**) Ballasting of the FEAs using current limiters is shown on the right. Note the reduction in the emission current variation due spatial variation of tip radii. Note also that the current limiter is more effective in reducing the current variation [4].

From this figure, it is observed that current uniformity (ΔI) improves as ballast resistance increases, but at the same time the current level drops.

To obtain uniform currents while maintaining high emission current, this research effort proposes to individually ballast each field emitter with un-gated FET acting as a current limiter. Figure 6 (b) shows that a smaller current range results from ballasting the FEAs with current limiters. Applying the un-gated FET device as a current limiter to each field emitter has enabled high current density, uniform, stable and reliable electron sources.

1.3 Objectives and Approach

The objective of this work is to create high-aspect ratio silicon pillar arrays to be integrated as un-gated FETs with a field emitter array. A vertical structure is desired so that each field emitter can be controlled individually while maintaining a compact device structure. To evaluate the un-gated FET, test structures with selected sizes of arrays of Si pillars were created. The test structures were characterized and compared with simulated results.

1.4 Thesis Outline

The second chapter in this thesis presents analytical models derived for the un-gated FET. In Chapter 3 the fabrication process used to create the vertical transistor test structure is outlined. Device simulation and experimental results are shown in Chapter 4. Conclusions are presented in Chapter 5.

Chapter 2 – Analytical Modeling of the un-gated FET

2.1 Device Modeling and Analysis

Silicon pillars acting as current limiters or un-gated FETs exploit saturation of carrier velocity in silicon at high electrostatic fields. The drift velocity of electrons is proportional to the electric field, with the electron mobility as the proportionality constant. At high electrostatic fields, the electron mobility is no longer a constant value and has dependence on the applied field [15]. Therefore, at high fields, a nonlinear dependence of the drift velocity on electric field is observed and the drift velocity of the carriers tends to saturate or approach a field-independent constant value. The velocity field relation incorporating velocity saturation in silicon at high electrostatic fields is given by: [16]

$$v_n(E) = \mu_{no} E \left[\frac{1}{1 + \left(\frac{\mu_{no} E}{v_{satn}} \right)^2} \right]^{1/2} \qquad (1)$$

where μ_{no} is the low field electron mobility, v_{satn} is the electron saturation velocity, and E is the applied electrostatic field. The saturation velocity of carriers in silicon is approximately 10^7 cm/s when biased with high electrostatic fields ($> 10^4$ V/cm).

The velocity field relation in Equation 1 was used to derive the current-voltage model for the un-gated FETs. The drain current along the channel is proportional to electron velocity:

$$I_D = Aqnv_n(E) \qquad (2)$$

where A is the cross-sectional area, q is the electronic charge, n is the number of electrons, and $v_n(E)$ is the velocity field relation given in Equation 1. To relate the drain current to the drain-to-source voltage, V_{DS}, the electrostatic field given by the following equation was used:

$$E = \frac{dV}{dy} \tag{3}$$

where y is a point along the channel of the device. Putting Equations 1, 2 and 3 together, The differential equation was solved to relate the drain current to the drain-to-source voltage V_{DS}. The resulting analytical model for the current-voltage relation is given by:

$$I_D = \frac{Aqn\mu_{no}}{L} V_{DS}\left[1+\frac{V_{DS}}{V_A}\right] / \sqrt{1+\left(\frac{V_{DS}}{V_{DSS}}\right)^2} \tag{4}$$

where parameters include I_D the drain current, L the channel length, V_{DS} the drain-to-source voltage, V_{DSS} the saturation voltage, and V_A the Early voltage. A, q, n, μ_{no} and L were parameters introduced in Equation 1 and Equation 2. The cross-sectional area A is assumed as constant, but in strict terms it should not be. As voltage is applied across the channel, the depletion layer changes the area that the current flows.

For this analytical model, the $\left[1+\frac{V_{DS}}{V_A}\right]$ term in the numerator describes the effect of channel length modulation, in order to accurately model the drain current in the saturation regime. Channel length modulation in a transistor device is caused by the increase of the depletion layer width at the drain as the drain voltage increases. The change in the depletion width at the drain leads to a shorter channel length. Figure 7 describes channel

length modulation by illustrating the changes in the depletion regions within the channel of the device as drain voltage is applied.

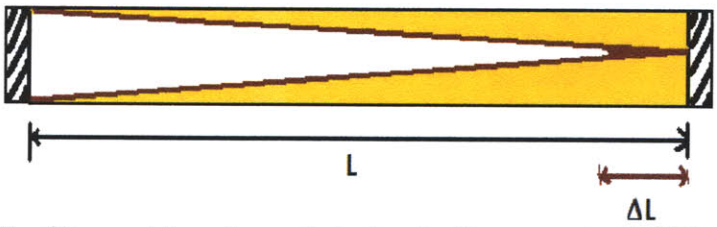

Figure 7. Channel length modulation in the un-gated FET
As drain voltage increases in the saturation regime, the depletion width at the drain is widened. This effect modifies and shortens the channel length.

Instead of a constant drain current for the saturation regime, a gradual increase in drain current is observed due to a decrease in channel length as the drain to source voltage is increased.

2.2 Simulated Device Performance vs. Analytical Model

Device simulation using SILVACO software tool were employed in order to predict current – voltage characteristics for the un-gated FET and extract device parameters. Device simulation tools from SILVACO solve semiconductor device equations, Poisson's equation and continuity equations self-consistently using appropriate boundary conditions for surface, interfaces, Schottky barriers and ohmic contacts. Figure 8 shows simulations of the current voltage characteristics for the un-gated FETs for channel lengths of 30 - 70 μm.

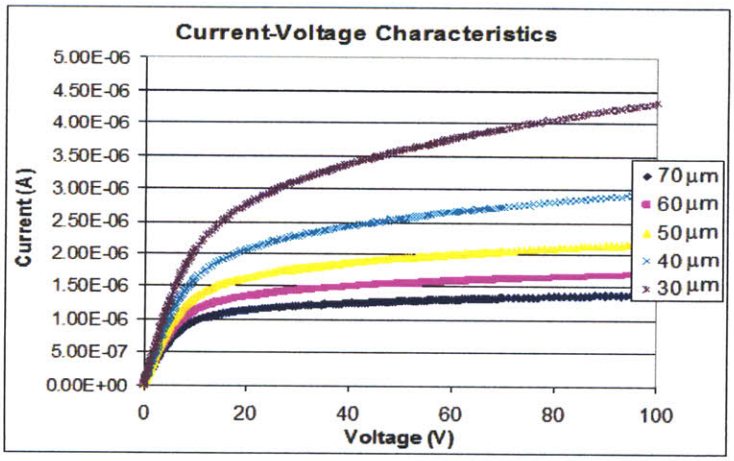

Figure 8. Simulated I-V characteristics of the un-gated FET
Current-voltage characteristics of simulated devices are shown. In the SILVACO program, different channel lengths were specified and current-voltage characteristics were predicted.

A comparison was made between the analytical model derived by Equation 4 with the I-V characteristics of the simulated device. The results found that channel length modulation did not adequately model the saturation current

2.3 Modeling the Saturation Regime of the un-gated FET

For further understanding of the un-gated FET, improvements to the analytical model need to be added to describe the drain current behavior in saturation regime. The current-voltage behavior in the saturation region is governed by channel length modulation and drain induced barrier lowering. For the earlier analytical model described in Equation 4 channel length modulation was already taken into account. Therefore, to improve the analytical model of the current in saturation regime, the drain induced barrier lowering effect needs to be incorporated into the existing analytical model.

2.3.1 Drain Induced Barrier Lowering

A small potential barrier exists between the heavily doped drain and source region and the lighter doped channel region of the un-gated FETs. When a high drain-to-source voltage is applied, the barrier height decreases, as indicated in Figure 9, leading to an increase in injection of carriers into the channel and hence the drain current. This effect is similar to the Schottky barrier lowering that is often observed in metal-semiconductor diodes.

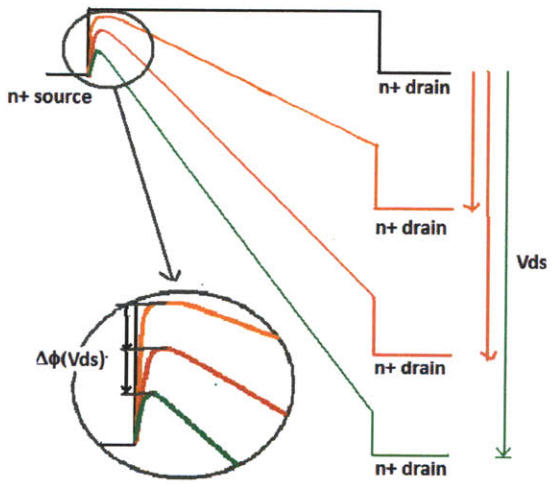

Figure 9. DIBL effect on the un-gated FET
Drain induced barrier lowering is shown. A decrease in potential barrier is observed for an applied drain-to-source voltage.

2.3.2 Potential Barrier and Drain-to-Source Voltage Relation

To effectively characterize the drain induced barrier lowering (DIBL) effects, simulated results were used to determine the empirical relationship between potential difference $\Delta\phi$ in the depletion regime and the drain-to-source voltage V_{DS}.

Several steps were taken to extract the potential barrier lowering from the device simulation. First, the potential profile was plotted along the center of the channel. The potential barrier lowering $\Delta\phi$ was extracted by finding the change in potential barrier at

the source end of the channel when a voltage was applied to the drain relative to when no voltage was applied. The procedure was repeated for different drain-to-source voltages and the corresponding $\Delta\phi$ values were extracted.

Extracted $\Delta\phi$ values were plotted versus the applied drain-to-source voltage. Finally, to obtain the relationship between the potential barrier and the drain-to-source voltage, the un-gated FET was simulated at five different channel lengths (70μm, 60μm, 50μm, 40μm, 30μm) to extract $\Delta\phi$ values for applied drain-to-source voltages. Figure 10 depicts the potential barrier change versus the drain-to-source voltage relationship for varying channel lengths of the un-gated FET.

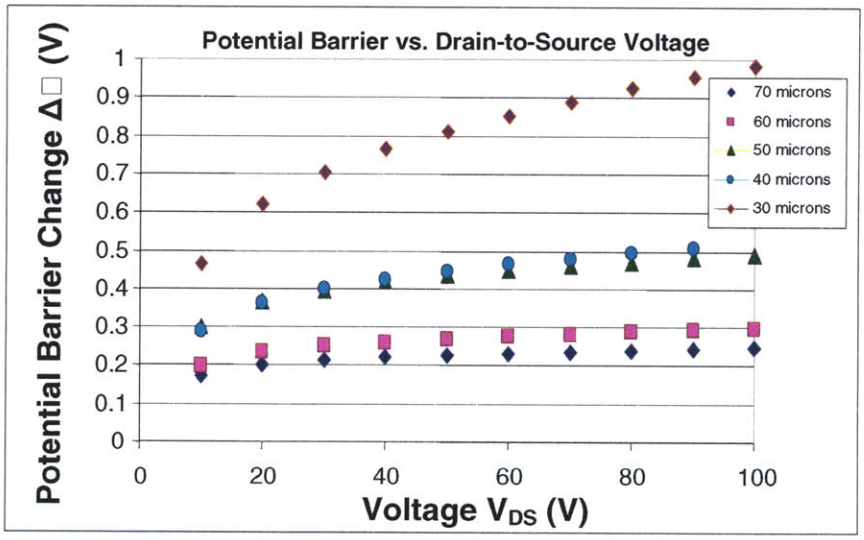

Figure 10. DIBL potential barrier vs. drain-to-source voltage relationship
The potential barrier change vs. drain-to-source voltage relationship is shown for un-gated FETs simulated for five different channel lengths.

An empirical relationship was found between the extracted potential barrier lowering $\Delta\phi$ and the drain-to-source voltage:

$$\Delta\phi = \alpha \ln(V_{ds}) + \beta \qquad (5)$$

where α and β values are summarized in Table 1.

Table 1. Summarized α and β parameters for the different channel lengths

Channel Length (μm)	α	β
30	0.2228	-0.0519
40	0.0969	0.0681
50	0.0806	0.1189
60	0.0415	0.1052
70	0.0304	0.1075

2.3.3 Current Saturation Model with DIBL

Once the relationship between the drain-to-source voltage and potential lowering in the depletion regime was determined, the drain induced barrier lowering effects could be used to model the current in the saturation regime. The earlier model for the current-voltage relationship of the un-gated FET was extended by incorporating drain induced barrier lowering (DIBL) effects.

In drain induced barrier lowering, there exists a potential barrier difference $\Delta\phi(V_{DS})$ between the n^+ source and the n^- channel. Electrons are injected into the channel. This results in an increase in the flux of electrons into the channel and hence an increase in the channel current is observed. The change in channel current is modeled using the Boltzmann relation [14], which describes the change in effective carrier density:

$$n = n_o e^{\Delta\phi / V_{th}} \qquad (6)$$

where n_o is the electron concentration before the barrier lowering, n is the electron concentration after the barrier lowering, $\Delta\phi(V_{DS})$ is the potential barrier lowering due to an applied drain-to-source voltage, and V_{th} is the thermal voltage.

At high drain-to-source voltages, the electron velocity and the drain current saturate. For an applied drain-to-source voltage greater than V_{DSS}, the saturation current occurs at

$$I_{DSS} = \frac{Aqn_o\mu_{no}}{L} V_{DS}\left[1+\frac{V_{DS}}{V_A}\right] / \sqrt{1+\left(\frac{V_{DS}}{V_{DSS}}\right)^2} \qquad (7)$$

The drain current in saturation regime is then formulated thus:

$$I_D = I_{dss} e^{\Delta\phi / V_{th}} \qquad (8)$$

Using Taylor's Series Expansion, a simplified relationship for the current is obtained:

$$I_D = I_{dss}\left(1+\frac{\Delta\phi(V_{DS})}{V_{th}}\right) \qquad (9)$$

The derived Equation 9 describes that drain current in the saturation regime depends on potential barrier lowering $\Delta\phi$. The potential barrier lowering $\Delta\phi$ is a function of the applied drain-to-source voltage V_{DS}, which was determined an empirical relationship in Equation 5.

Finally, to determine the accuracy of the drain induced barrier lowering effect for modeling current behavior in the saturation regime, the analytical model in Equation 9 was plotted along with the simulated current-voltage characteristics. The comparison of the DIBL modeling of the current in the saturation regime is shown in Figure 11.

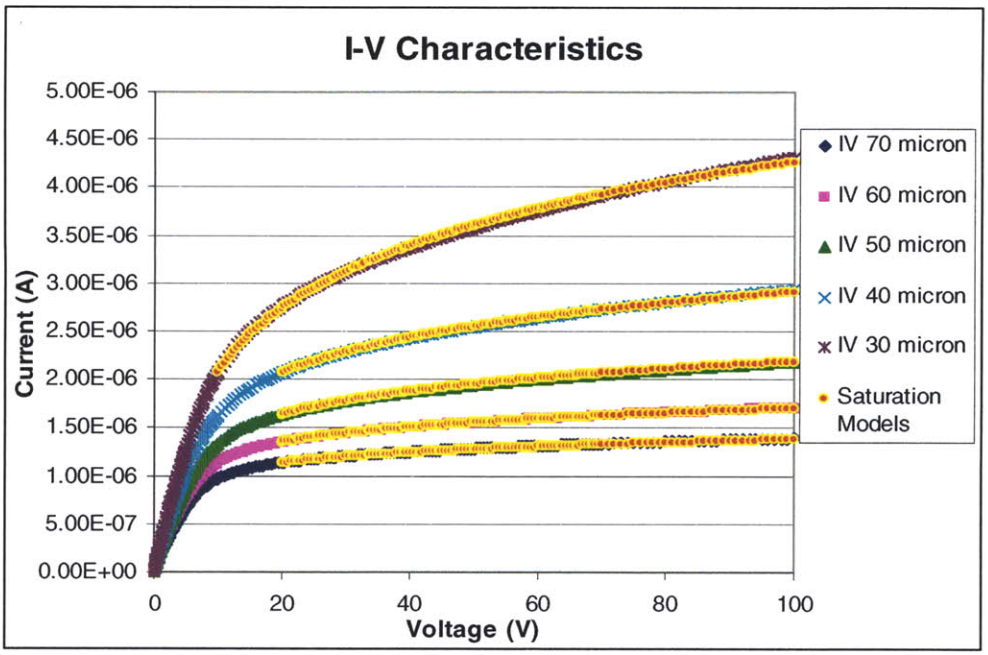

Figure 11. Comparison of the DIBL modeling with simulation

The I-V characteristics of the drain induced barrier lowering effects for the saturation regime were plotted and compared with the simulations.

Chapter 3 – Device Fabrication

3.1 Device Design

Device fabrication was carried out with the objective of creating vertical high-aspect ratio pillars that exhibit electrical characteristics similar to current limiters. Initial stages of this research [20] demonstrated the feasibility of fabricating a dense array (10^6 pillars/cm^2) of vertical silicon pillars with dimensions of 100μm height and cross-sectional area of 1 x 1 μm^2. Later stages of this research focused on designing and fabricating of high aspect ratio silicon pillars with ohmic contacts as test structures for the un-gated FET. The testing structures were constructed based on three main reasoning: to provide accurate and precise characterization of the un-gated FET device, demonstrate high saturation current (1 mA) capability, and investigate the effects on key device parameters when connecting different-sized array of pillars in parallel.

The approach taken to fabricate the test structures for the vertical un-gated FET consisted of four major steps. The first step was to pattern the wafer and etch vertical columns into the silicon substrate. The second major step was to fill the high aspect ratio gaps between adjacent pillars with oxide dielectric. The third step consists of selectively etching the silicon dioxide and exposing selected pillar tips. The final step involved depositing and patterning TiN/Al metal pads to create low resistance contact points at the silicon pillar tips. A cross-sectional view of the test structure is illustrated in Figure 12.

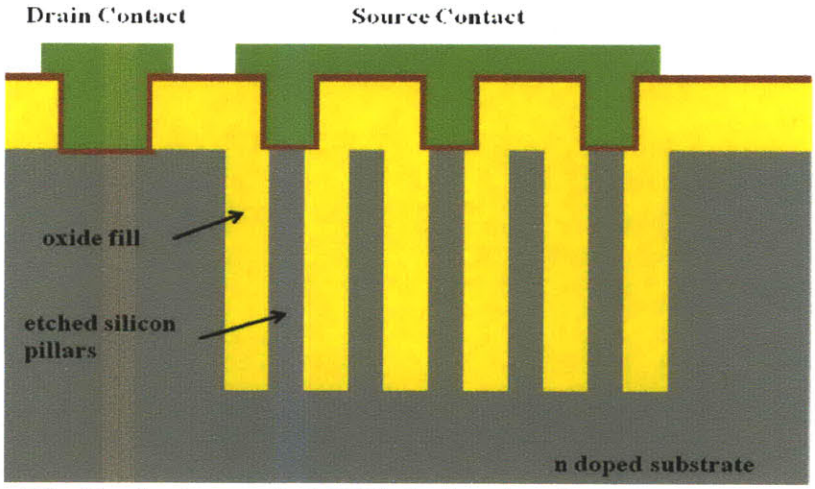

Figure 12. Vertical un-gated FET device structure
Un-gated FET structure fabricated by etching silicon pillars followed by an oxide fill of the voids between adjacent pillars, etch back, vertical ion implantation and metal patterning.

3.2 Device Design/Mask Layout

The test structure of the un-gated FET device was designed with the objective of making ohmic contacts to selected sized arrays of silicon pillars. To begin with, the basic design of this test structure consisted of a dense array (~10^6 cm^{-2}) of silicon pillars. The silicon pillar dimensions were designed as 4μ m x 4μm cross-sectional area squares with 7.5 μm pitch between adjacent pillars. These pillars were patterned and etched using a hard mask, and silicon dioxide was used to fill the void between adjacent pillars.

Then a second layer design of this test structure consists of patterning and exposing selected arrays of insulated pillars through etch back. The array sizes were designed as 1 x 1, 3 x 3, 9 x 9, 15 x 15, 31 x 31, 50 x 50 and 100 x100 exposed pillars. The array sizes were also scaled by orders of magnitude to precisely characterize and determine the relationship of the key parameters of the un-gated FET device. Finally the third layer design of this testing structure consists of patterning metal contact pads for the

different sized arrays of exposed silicon pillars etched in the second layer. Figure 13 illustrates the complete design of the test structure of the silicon pillars.

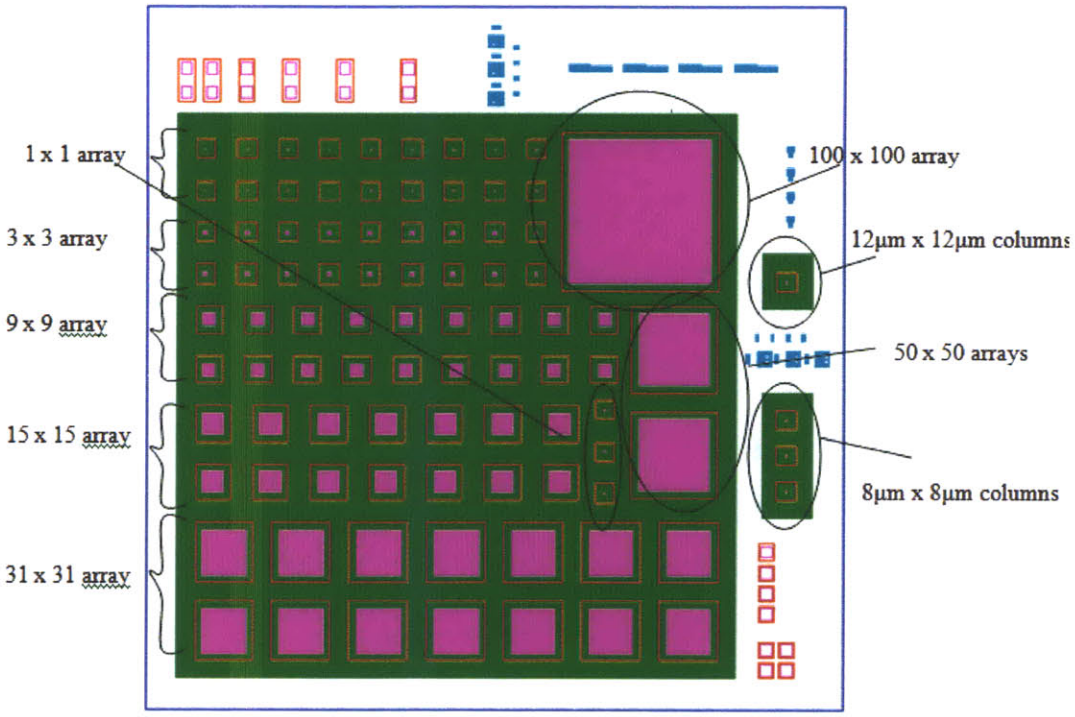

Figure 13. Top view of the device testing structure
Green square pads indicate arrays of etched silicon pillars. Pink squares indicate the arrays of exposed pillars. Red square frames indicate the metal contact points.

Sheet resistivity test structures (Van der Pauw, TLM, and 4 point probe) were added along the sides of the die in order to obtain the sheet resistivity, contact resistance, and majority carrier mobility of the wafer. Figure 14 shows test structures.

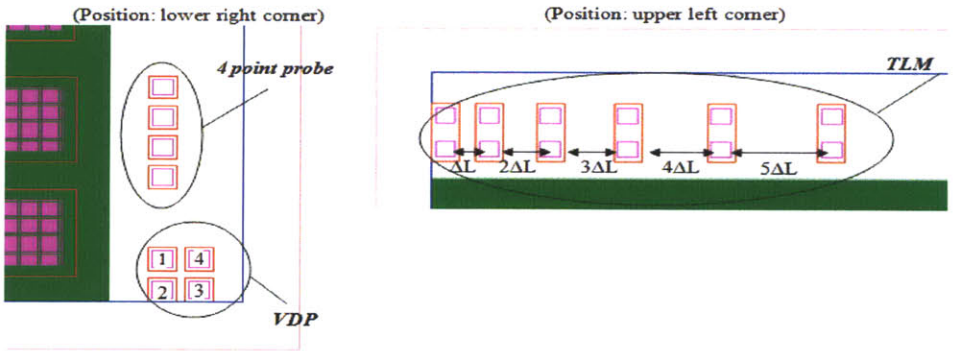

Figure 14. Sheet Resistivity Testing Structures
The 4 point probe, TLM, and Van der Pauw test structures are located on the sides of the die. These test structures are used to determine the contact resistivity, sheet resistivity, and mobility of the test wafer.

The Van der Pauw technique [21] used in this design consists of four small contact points arranged in a symmetric rectangle. The specific resistivity can be determined by passing a known current through two adjacent terminals and measuring the voltage across the other two terminals. The sheet resistivity calculation using the Van der Pauw equation can be summarized by the following equation,

$$\rho = \left(\frac{\pi t}{\ln 2}\right)\left(\frac{R_{12,43} + R_{14,23}}{2}\right) \tag{10}$$

where t is the layer thickness and $R_{12,43}$ is the potential difference across contacts 4 and 3 resulting from unit current flow between contacts 1 and 2. Once the sheet resistivity is calculated, the impurity dopant concentration of the substrate can be determined with the resistivity versus dopant concentration relationship.

The transmission line measurement (TLM) technique is commonly used to measure metal-semiconductor contact resistance and sheet resistance. Voltage is applied across pairs of contact and the resulting current is measured. The measured resistance is a linear combination of the contact resistance of the first contact, the contact resistance of the second contact, and the sheet resistance of the semiconductor between the contact points. The resistance relationship is summarized using the following equation [22],

$$R_T = 2R_{CS} + R_S = \frac{V}{I} \tag{11}$$

where R_T is the total resistance, R_{CS} is the contact resistance, R_S is the sheet resistance. This resistance measurement is repeated between pairs of contacts with different separation distances. From the plot of resistance versus contact separation distance,

contact resistance is extracted from the y-intercept and the sheet resistance is extracted from the slope.

The four point probe technique is another simple approach to extract sheet resistance from the semiconductor interface. Current is applied to the outer contact points and voltage is measured across the inner contact points. The sheet resistance is linearly related to the current voltage ratio in the following relationship [23],

$$R_S = \frac{\pi}{\ln 2}\frac{V}{I} \tag{12}$$

where R_S is the sheet resistivity, I is the current applied across the outer probes, and V is the voltage measured in the inner probes.

Another important design feature includes varying pillar areas by scalable factors. Two array patterns with pillar areas of 8μ m x 8μm and 12μ m x 12μm were added along the sides of the die. The object of this additional design feature is to determine the relationship between the cross-sectional area and the current flow of a single pillar. Figure 15 shows this design feature in detail.

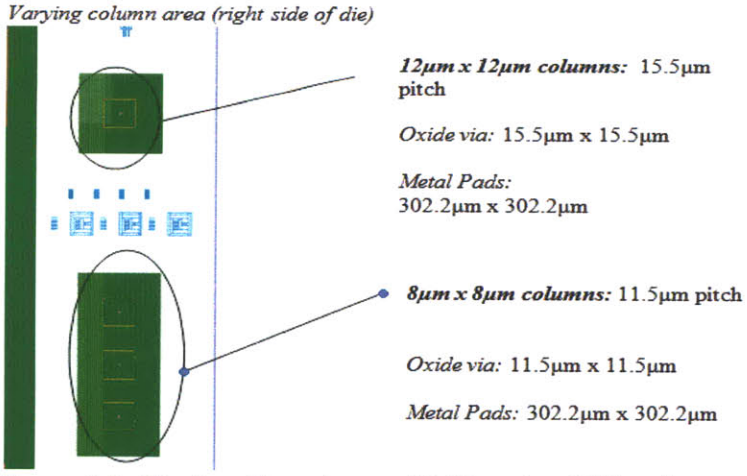

Figure 15. Design Structure with Varying Pillar Area
Two array pattern with cross-sectional areas of 8μ m x 8μm and 12μ m x 12μm were added along the sides of the die.

3.3 Process Outline

A fabrication process using three photolithography mask steps was used to create the un-gated FET devices. Process simulations were conducted using SILVACO software to develop and optimize the design flow of each process step. Process simulation results generally agreed with the fabrication processes and served as a good guideline to investigate the fabrication methodologies. The fabrication process flow and the simulation results of the un-gated FET device are summarized in Figure 16.

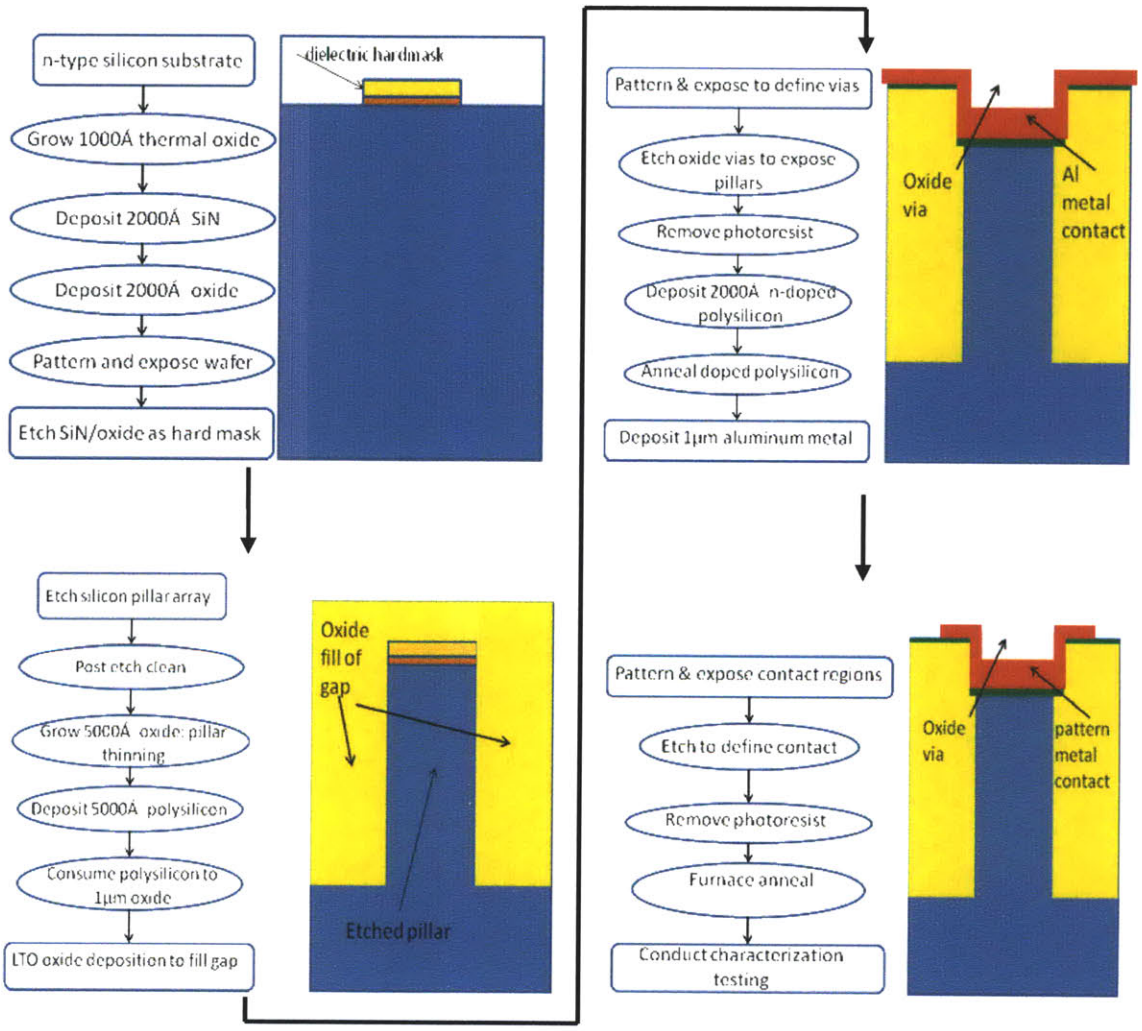

Figure 16. Un-gated FET Process Design

3.4 Device Fabrication

The un-gated FET devices were fabricated on 6" n-type substrates with sheet resistivity of approximately 5-25 Ω-cm. To begin device processing, an initial 1000 Å of thermal oxide was grown on the silicon wafer. Immediately following the thermal oxide growth, 2000Å of SiN layer and 2000Å of oxide layer were deposited onto the silicon substrate using LPCVD and PECVD low temperature deposition respectively. Figure 17 illustrates a schematic representation of the dielectric film stack used to etch the silicon pillars.

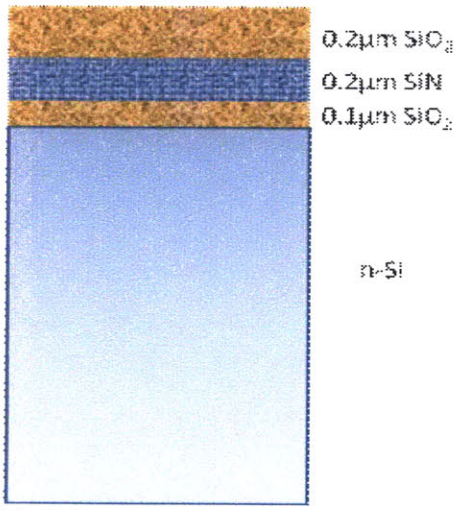

Figure 17. Thin Dielectric Film Stack
The bottom stack is a thin layer of thermal oxide, the middle layer is a thin layer of Si-rich Nitride, and the top layer is PECVD deposited oxide.

The thin dielectric film stack layers served different purposes to optimize the etching of the silicon pillars. The top oxide film was used as a hard mask for etching silicon pillars. The Si-rich Nitride layer serves as a diffusion barrier for oxygen during subsequent oxidation steps and prevents the formation of a bird's beak [24]. And finally, the bottom oxide dielectric film is used to relieve stress that develops at the interface between silicon nitride and silicon.

Following the deposition of thin dielectric films, substrate was coated with photoresist and patterned using projection photolithography. In contrast to contact

photolithography, projection photolithography defines smaller features with better precision.

Once the photoresist is patterned, reactive ion-etching with low pressure CHF_3 and CF_4 plasma was used to define the dielectric stack to form a hard mask for the silicon pillar arrays. After the definition of the hard mask, silicon pillar arrays were etched using deep reactive ion etching (DRIE). Deep reactive ion etching is a MEMS-based technology specifically used to an-isotropically etch high aspect ratio structures. In order to achieve very high aspect ratio of 100:1 etched silicon pillars, the deep reactive ion etch technology uses a two step time-multiplexed plasma recipe known as the Bosch process [25]. The Bosch process uses SF_6 plasma to increase the anisotropy of silicon etching, and deposits a polymer passivation layer in between two consecutive etch cycles. Post-etch scanning electron micrographs of the pillar etch are shown in Figure 18 and 19.

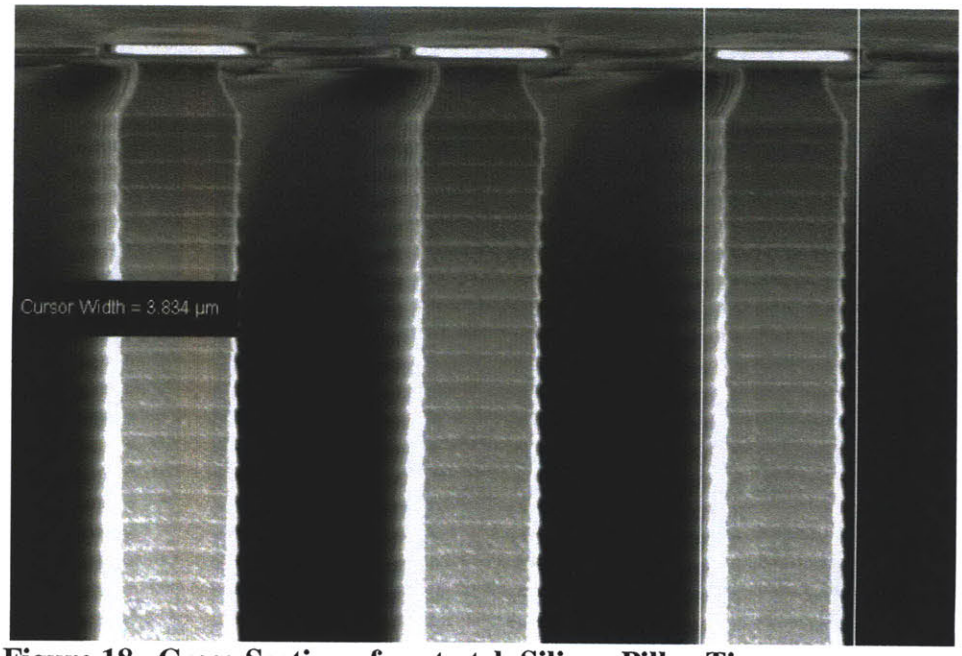

Figure 18. Cross-Section of post-etch Silicon Pillar Tips
Close-up scanning electron micrograph of the vertically etched silicon pillars shows that the side-walls suffer from scalloping roughness.

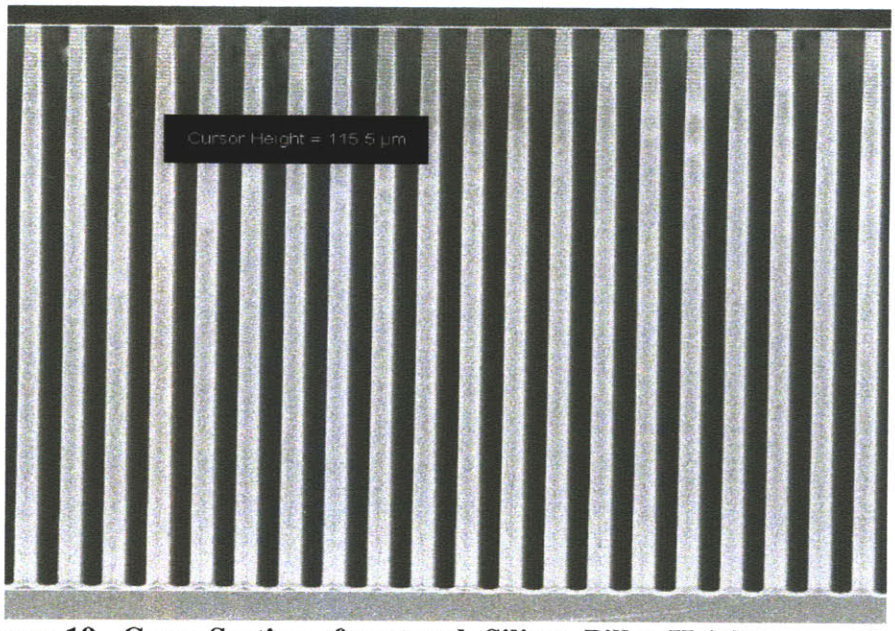

Figure 19. Cross-Section of post-etch Silicon Pillar Height
Scanning electron micrograph shows the vertical height of 115.5µm for the post-etch silicon pillars. A slight tapering of the side-wall is observed.

Once the silicon pillar arrays were formed, wet oxidation was used to reduce the silicon pillar width. The resulting silicon pillars were 115 µm tall and 2µm wide.

In order to pattern and expose selective silicon pillars, oxide must be filled in-between the high aspect ratio gaps of adjacent silicon pillars. The gap filling process proved to be quite a challenge for high aspect ratio of 100:1. In the first step of the filling process, poly-silicon of 0.5 µm was deposited at low pressure in a SiH_4 ambient at 620 $^{\circ}C$ to partially fill in the high aspect ratio gaps. Figure 20 (a) illustrates a scanning electron micrograph after the low pressure poly-silicon deposition. The gap between the silicon pillars is noticeably smaller and partially filled in. Low temperature chemical vapor deposition (LPCVD) of poly-silicon provided excellent step coverage for the side walls along gaps of the silicon pillars. Figure 20 (b) illustrates a close-up scanning electron micrograph with anisotropic etched side wall clearly showing the poly-silicon layer deposited on top of the thermally grown oxide.

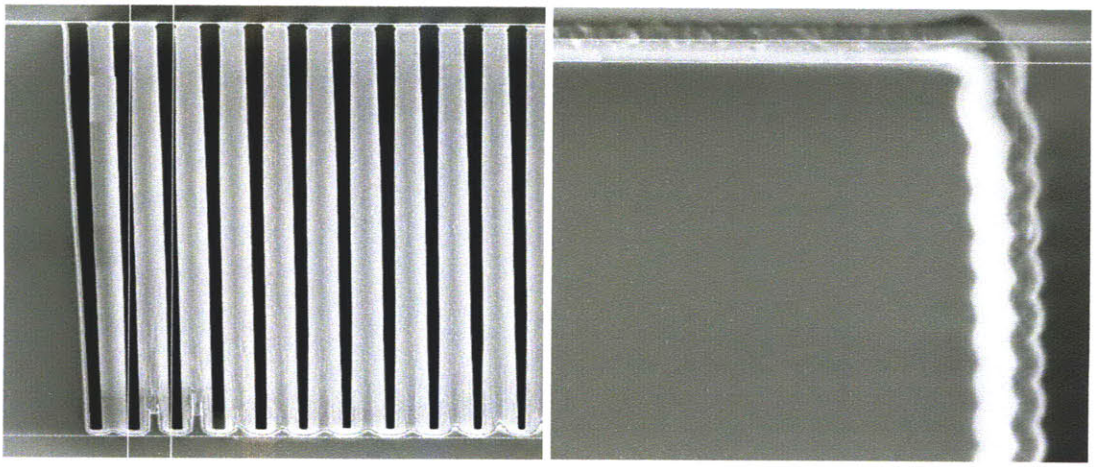

Figure 20. Silicon pillars post LPCVD polysilicon gap fill
(a) Cross-sectional view of the silicon pillars with partially filled gap, after low pressure chemical vapor deposition of 0.5μm polysilicon. (b) close-up view of the side-wall step coverage from the low pressure polysilicon deposition.

Following the low pressure poly-silicon deposition, the substrate was wet oxidized at 1050°C until all the deposited poly-silicon was consumed as SiO_2. The Deal-Grove model [26] for the oxidation of single-crystal silicon was used to calculate the time taken to consume the poly-silicon. Because oxidant molecules diffuse rapidly along grain boundaries, poly-silicon oxidizes more rapidly than single-crystal silicon [28]. The poly-silicon material expands once oxidized. Therefore, if the gap closed before poly-silicon is fully expanded, tensile stress is put between the gaps and causes the substrate to bend or break. For this reason, the method of depositing polysilicon and thermally oxidizing cannot be used to completely close the gap between adjacent silicon pillars.

The final step for filling the high-aspect ratio gap involves depositing low temperature oxide (LTO) onto the substrate. Figure 21 (a) shows the scanning electron micrograph of silicon pillar arrays with the gaps partially filled by oxidized poly-silicon. The scanning electron micrograph in Figure 21 (b) shows oxide completely filling the high aspect ratio gaps after 4μm low temperature oxide film deposition.

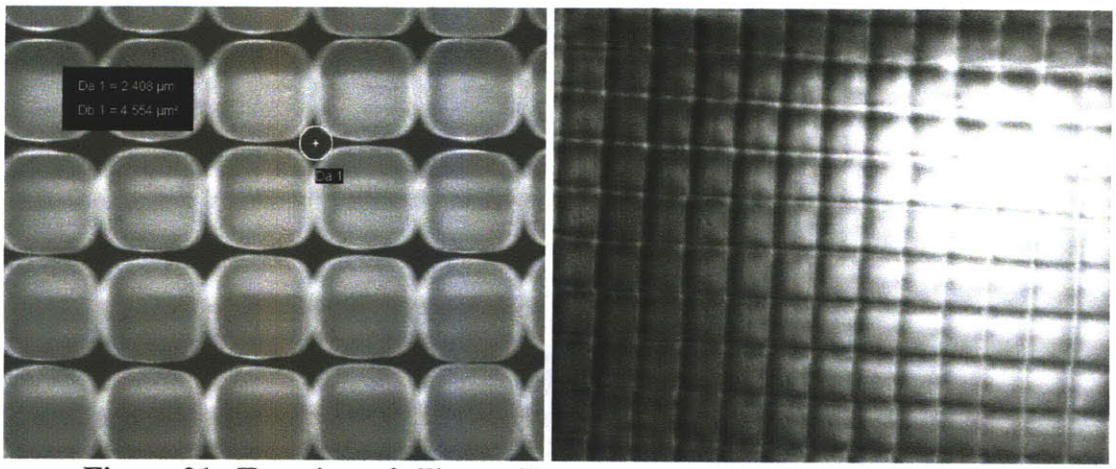

Figure 21. Top view of silicon pillar array pre- and post LTO
(a) SEM image of silicon pillar arrays showing partially filled gaps post oxidation of poly-silicon (b) oxide completely filled gaps between adjacent silicon pillar arrays after 4 μm low temperature oxide deposition.

The low temperature oxide deposition may serve as one feasible solution to fill the remaining gap after poly-silicon oxidation. However, in some instances the top of the gap closes up before deposited oxide reaches the bottom. This results in small air gaps observed in Figure 22. This defect suggests that alternative methods should be explored in place of low temperature oxide deposition. One viable solution is the use of spin-on glass (SOG) dielectric material for high aspect ratio gap filling [27].

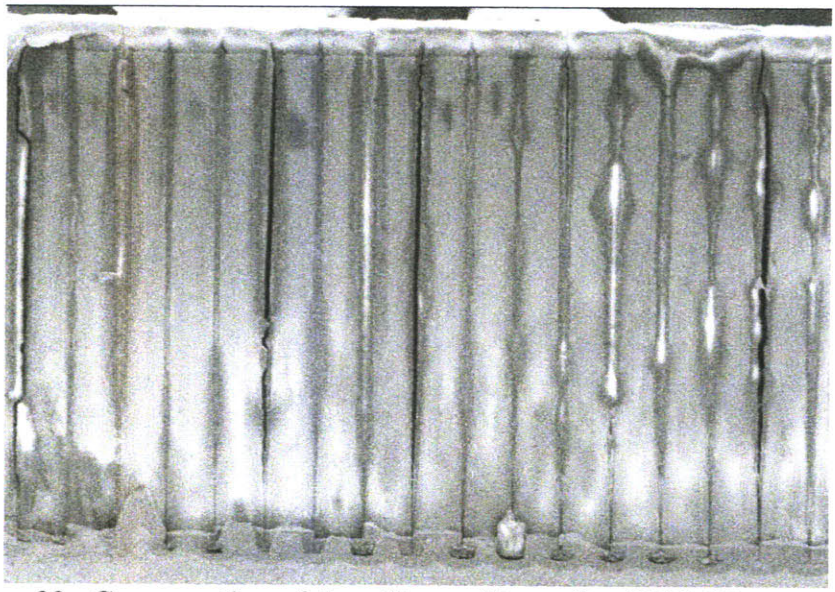

Figure 22. Cross-section of the silicon pillars after LTO fill
Several gaps filling have crevices after the oxide film deposition.

Following the low temperature oxide fill, a densification anneal at 950°C is highly desired for obtaining high oxide/silicon selectivity during a later etch step. Due to time constraints, this densification step was omitted from the process.

Once the oxide fully filled the high aspect ratio gaps, adjacent silicon pillars were electrically insulated from one another. An array of vias was patterned in the oxide with photoresist and etched in low pressure CHF_3 and CF_4 plasma. Selected arrays of insulated pillars were etched back to expose the tops of silicon pillars for metal contact. Figure 23 shows the etch-back of oxide via structure. The un-densified low temperature oxide etched faster than oxidized poly-silicon. Therefore in the etch-back images, the boundaries is clearly observed between the low temperature oxide and oxidized poly-silicon.

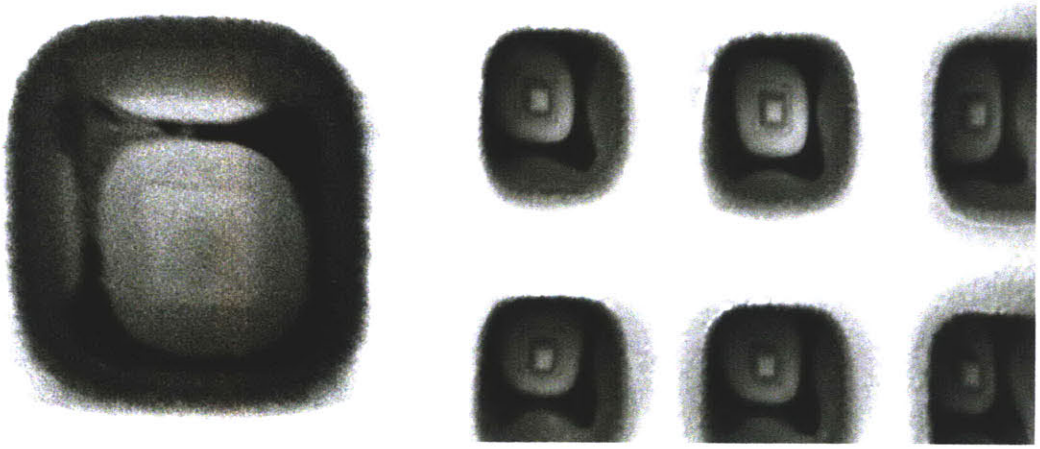

Figure 23. Contact via etch-back
(a) etch-back process using reactive ion echant with the low temperature oxide film etched through, but silicon pillar tips remain unexposed. (b) silicon pillar tips are selectively exposed in the oxide via array.

For the final processing steps, a 2000Å n-doped poly-silicon was deposited and annealed in nitrogen ambient at 950°C to form a thin layer of N^+ film and improve ohmic contact. Low pressure physical vapor deposition was used to deposit 0.1 μm titanium nitride

followed by 1μm aluminum film onto the wafer. The layer of titanium nitride was used in the deposition to prevent the aluminum from spiking into the silicon and possibly shorting the device. The wafer was patterned and etched in Cl_3/BCl_3 plasma to define metal contact regions for the un-gated FET arrays. The doped poly-silicon layer was also etched in Cl_3/BCl_3. Finally, the aluminum was annealed at 450°C in nitrogen ambient to activate the metal contact.

Chapter 4 – Device Characterization

4.1 Device Simulation

There exist two major motivations for conducting device simulation: first to validate the un-gated FET analytical expressions derived in Chapter 2; secondly to correlate numerical simulation results with actual device performance. Device modeling was conducted using SILVACO simulation tools. Semiconductor process models were used to simulate the device fabrication process. From the process simulation results, a device mesh was generated and used to characterized device behavior in response to applied voltage conditions.

Initial simulation was conducted in order to validate the analytical model derived in Equation 4 of Chapter 2.1. A single un-gated FET device with dopant concentration of 2 x 10^{14} cm^{-3} and dimensions of 1μ m x 1μm cross-sectional area and 100μm height was simulated. Figure 24 shows a 2-D plot of the simulated device. Figure 25 shows the corresponding current-voltage (I-V) characteristics.

Key parameters to characterize un-gated FET were extracted from the I-V behavior. The parameters include the linear conductance g_{lin}, output conductance, g_{out}, saturation voltage, saturation current, and maximum current. g_{lin} and g_{out} describe the transistor behavior in the linear and saturation regime respectively. Un-gated FET with a smaller output conductance corresponds to a better current limiter since an ideal current limiter has zero output conductance. V_{DSS} is the voltage when the current begins to saturate.

Saturation current is the corresponding current at which the saturation voltage V_{DSS} is observed.

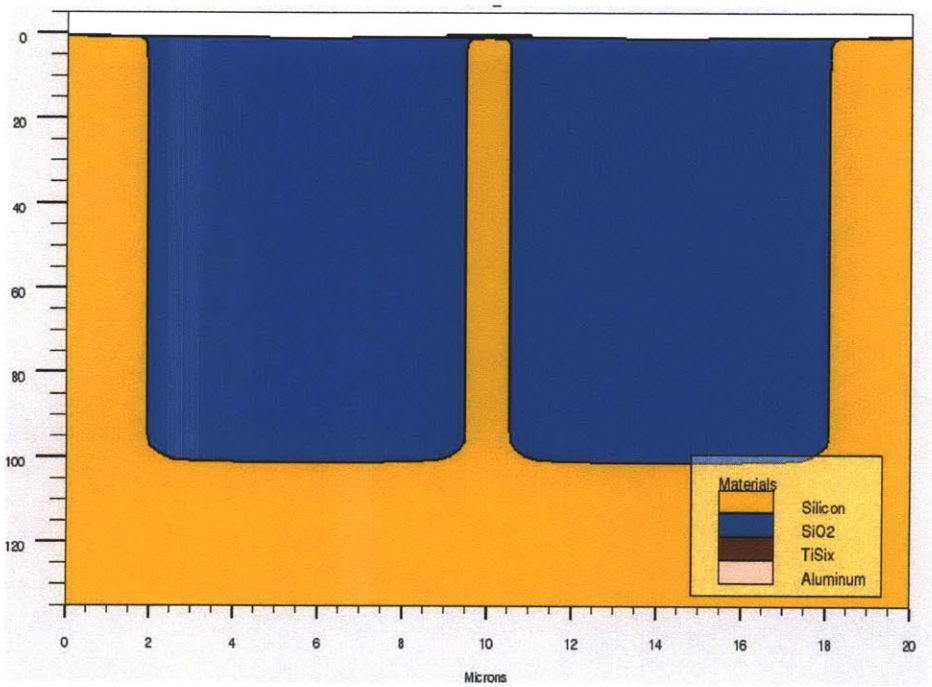

Figure 24. Initial device simulation
Silicon pillars with dimensions of 1μm x 1μm x 100μm were simulated

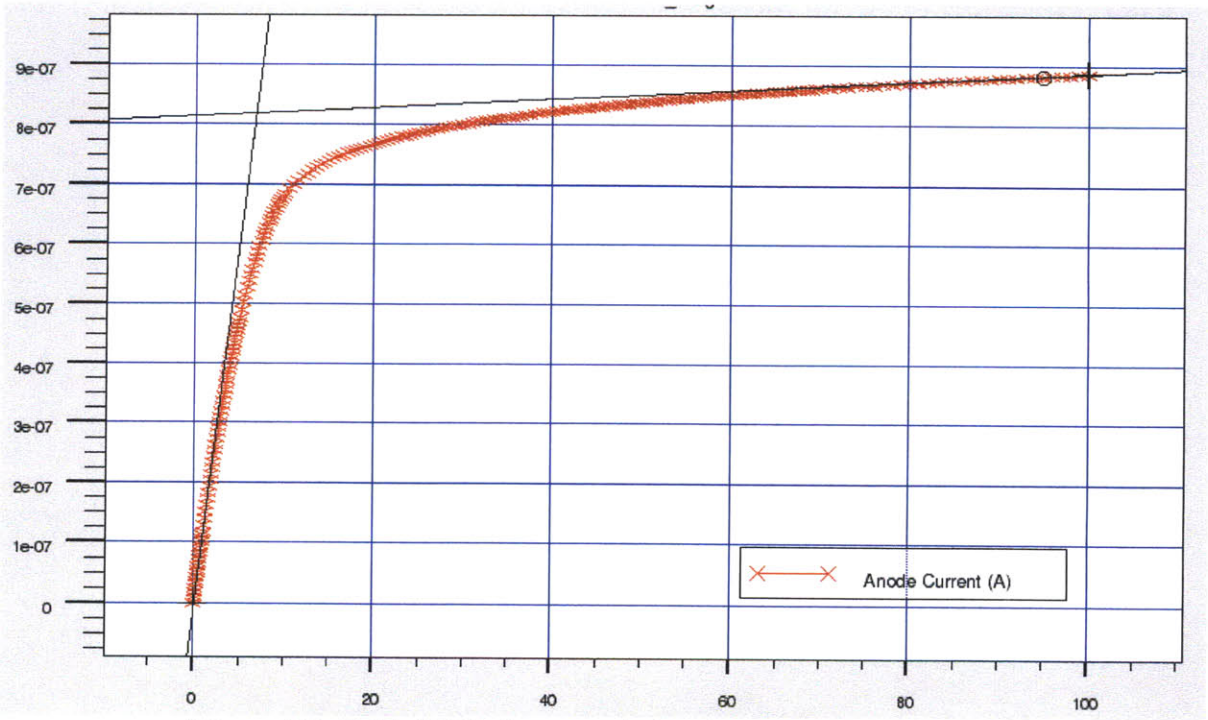

Figure 25. Initial I-V characteristics simulation
I-V behavior was simulated for silicon pillars with dimensions of 1μm x 1μm x 100μm.

Figure 26 shows a comparison between the I-V characteristics of the analytical model and the simulated un-gated FET for dopant concentration of 2×10^{14} cm^{-3}.

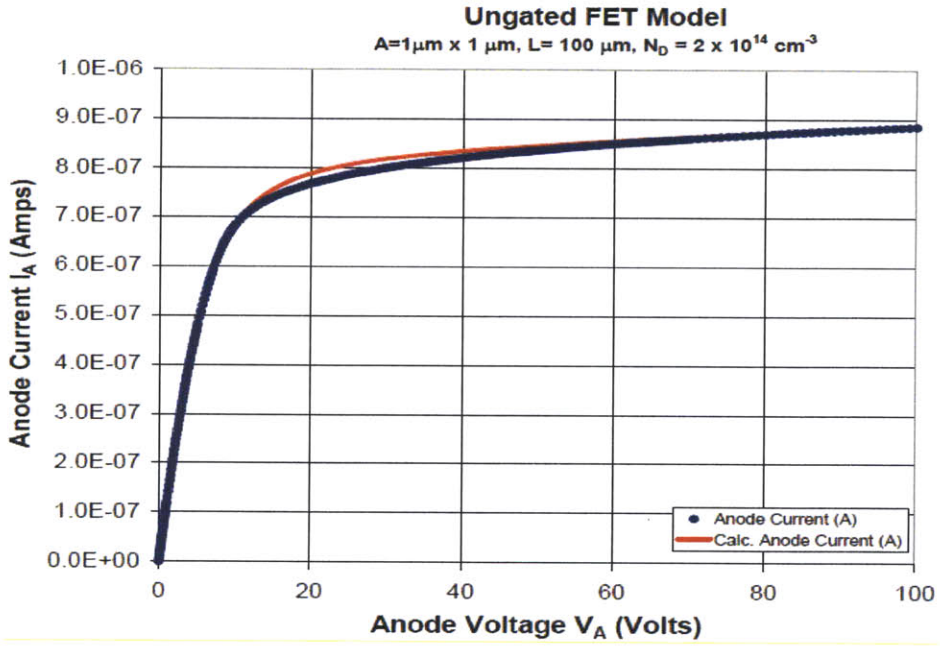

Figure 26. Comparison between analytical model and simulation
I-V Characteristics of the un-gated FET comparing the analytical model and simulation. Current saturation is observed in both cases.

This comparison showed that the current behavior in the saturation regime of analytical model differed from simulation. In the interest of time, additional analysis of the analytical model for current in saturation regime was not developed.

Once the initial simulation was completed, simulated device parameters needed to be compared with actual tested device parameters. Before an accurate comparison can be made, the simulation needs to be modified so that the dimensions and dopant concentration of the simulated device matched with the fabricated device.

Process parameters for both the initial simulation and experimental measurements are summarized in Table 3. The fabricated un-gated FETs had a 2μm x 2μm cross-sectional area, which was measured using a top view SEM image. It is noted that the un-gated FETs were originally designed with dimensions of 4μm x 4μm cross-sectional areas. Silicon pillars with 2μm x 2μm cross-sectional areas were obtained after the wet oxidation step in fabrication, which was designed to thin the sides of the pillars. The device length was measured to be 115 μm, which was determined by a cross-section from scanning electron micrograph.

The dopant concentration was determined by the sheet resistivity calculation. Sheet resistivity was measured from the Van der Pauw test structure. Equation 30 from Chapter 3.2 relates sheet resistivity from the resistance measurements taken. Based on the experimental data, $R_{12,43}$ =51.5Ω and $R_{14,23}$ =51.2Ω and sheet resistivity was calculated to be 15.13 Ω-cm. The corresponding dopant concentration is 2.9 x 10^{14} cm^{-3}.

Process Parameters	**Initial Process Simulation**	**Experiment**
Cross-sectional area	1μm x 1μm	2μm x 2μm
Channel length	100μm	115μm
Doping concentration	2 x 10^{14} cm^{-3}	2.9 x 10^{14} cm^{-3}

Table 3. Comparison of process parameters between simulation and fabricated device

Simulations were modified so that the process parameters matched with those of the fabricated device. A single un-gated FET with dopant concentration of 2.9 x 10^{14} cm^{-3} and dimensions of 2μ m x 2μm cross-sectional area and 115μm height was simulated and shown in Figure 27. The corresponding I-V characterization is shown in Figure 28.

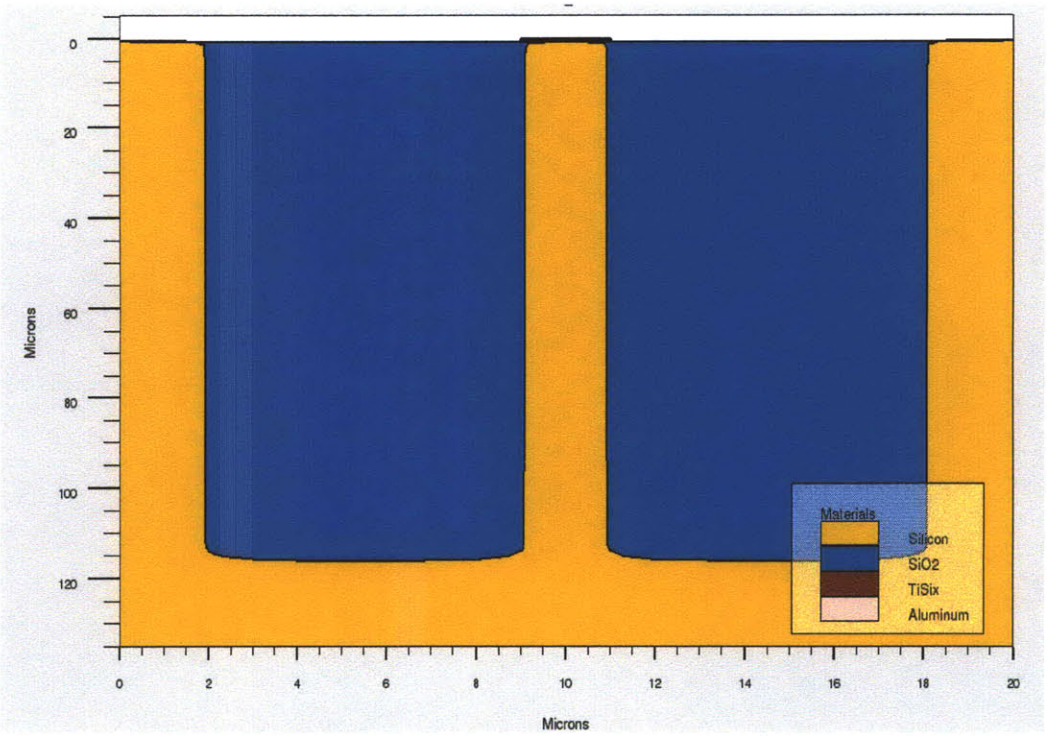

Figure 27. Modified device simulation
Silicon pillars with dimensions of 2µm x 2µm x 115µm were simulated

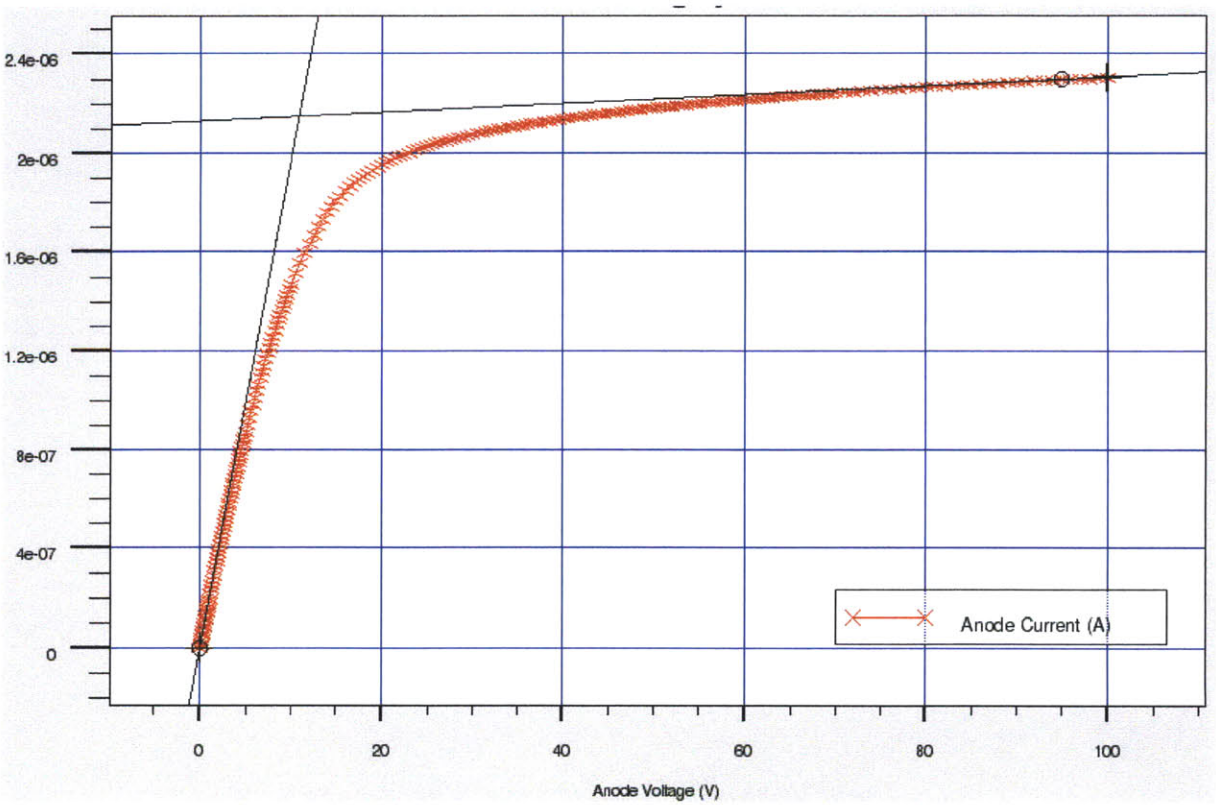

Figure 28. I-V characteristics for modified simulation
I-V behavior was simulated for silicon pillars with dimensions of 2µm x 2µm x 115µm.

As mentioned in Chapter 3.1, un-gated FETs with 8μm x 8μm and 12μm x 12μm cross-sectional areas were also built. In order to compare with the actual device, simulation was conducted for the un-gated FET with corresponding cross-sectional area. It is assumed that the same pillar thinning effect is observed: the un-gated FETs designed with cross-sectional area of 8μm x 8μm will have an effective cross-sectional area of 6μm x 6μm. A single un-gated FET with dopant concentration of 2.9 x 10^{14} cm^{-3} and dimensions of 6μ m x 6μm cross-sectional area and 115μm height was simulated and shown in Figure 29. The corresponding I-V characterization is shown in Figure 30.

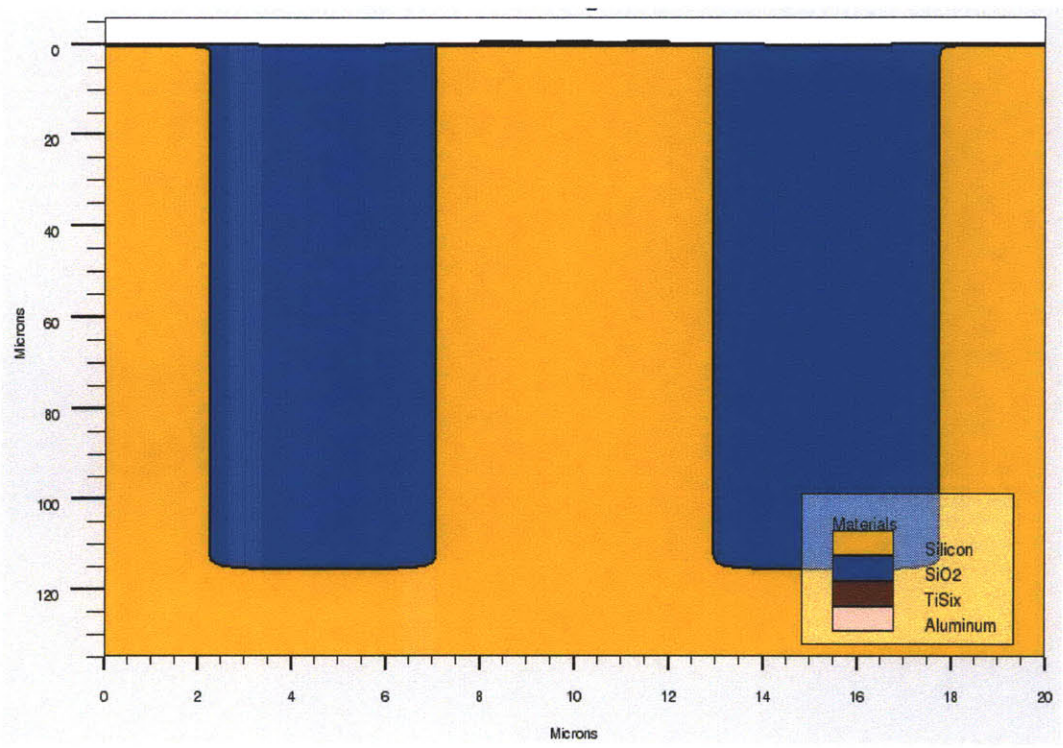

Figure 29. Device simulation for varying cross-sectional area
Silicon pillars with dimensions of 6μm x 6μm x 115μm were simulated

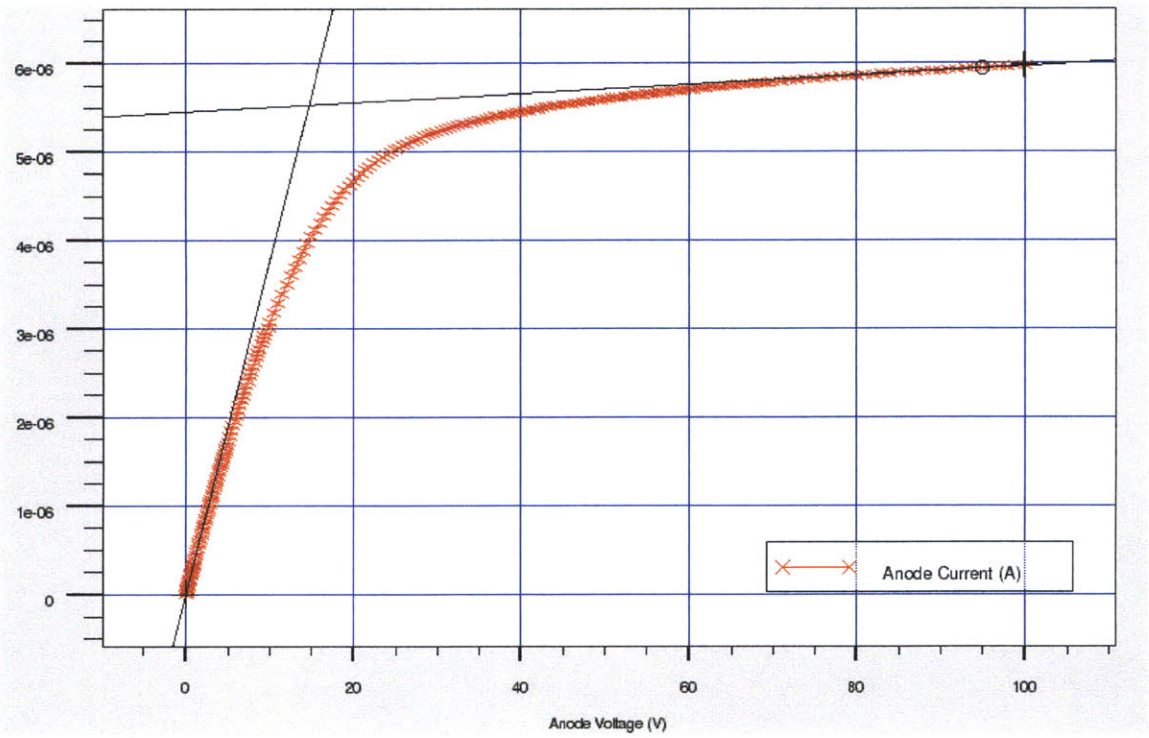

Figure 30. I-V characteristics for varying cross-sectional area
I-V behavior was simulated for silicon pillars with dimensions of 6μm x 6μm x 115μm.

Table 4 specifies the key device parameters, described earlier in this section. The parameters were extracted from the I-V characteristics of the three different simulations. These values will be used to compare with actual device parameters.

	g_{lin} (μS)	g_{out} (nS)	I_{DSS} (μA)	V_{DSS} (V)	I_{max} (μA)
1 μm x 1μm x 100μm	0.121	0.72	0.818	6.75	0.89
2 μm x 2μm x 115μm	0.198	1.73	2.16	10.8	2.31
6 μm x 6μm x 115μm	0.378	5.23	5.53	14.6	5.98

Table 4. Key device parameter for simulations
Note that device with 1 μm x 1μm x 100μm were simulated with 2.0 x 10^{14} cm^{-3} dopant concentration. Devices with dimensions were simulated with 2.9 x 10^{14} cm^{-3} dopant concentration

4.2 Test set-up

Once simulations for the un-gated FET were conducted, the next step was to characterize the fabricated device. In order to obtain consistent and reliable data, testing of the un-gated FET device structure was approached systematically. Figure 31 shows a map of the wafer with the die numbered.

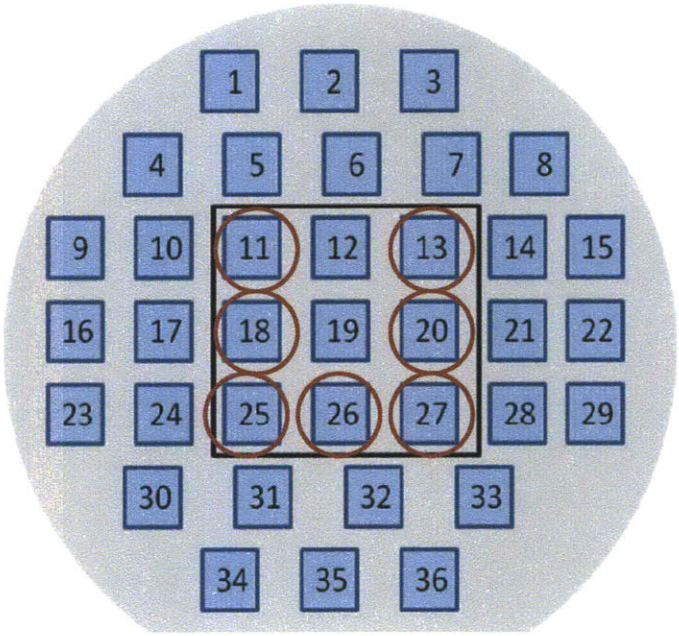

Figure 31. Wafer map
Die within the wafer is numbered for easy data tracing. I-V characterization took place in the center region, which is encircled by a black square box.

Devices were characterized within the center region of the die. For clarity purposes this center region is encircled by a black square box. Dies which were characterized are identified by marked circles.

The setup of the test probes is shown in Figure 32. Test probes were placed on the metal contact to silicon pillar arrays and a metal contact to the substrate. Voltage is applied

across the contact points and current through the channel formed by the silicon pillars is measured.

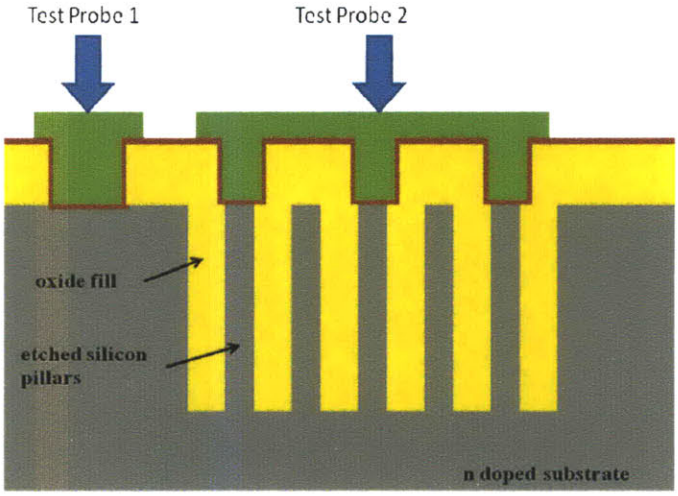

Figure 32. Test setup
Contact is made to the un-gated FET arrays. Test probe 1 makes contact to the substrate. Voltage is applied across the two terminals, and current is measured across.

4.3 Electrical Testing

I-V characterizations of completed un-gated devices were conducted using the HP4156 probe station. Key figures of merit were measured and compared to the predicted values from simulations. In general, actual device data matched very well with predicted metrics.

Current saturation is observed in the current-voltage (I-V) characteristics, to show that un-gated FETs based on Si pillar structures act as current limiters. Figure 33 illustrates device characterization for different sized arrays of silicon pillars described in Chapter 3.1. Currents versus voltage plots were taken for 1 by 1, 3 by 3, 9 by 9, 15 by 15 array sizes of the un-gated FET test structure.

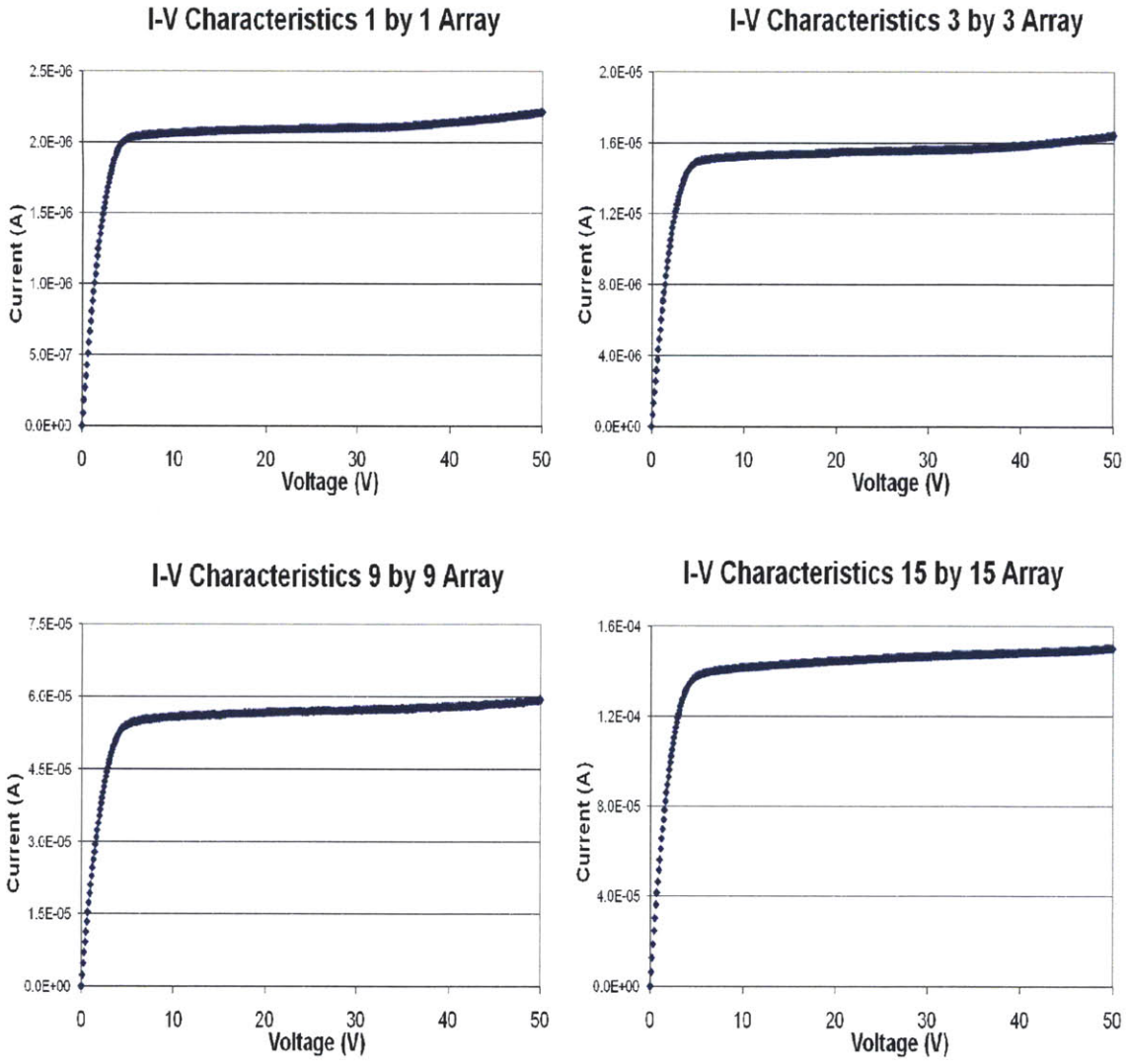

Figure 33. I-V Characteristics of different array size
I-V Characteristics were taken from un-gated FET structures with dimensions of 2μm x 2μm x 115μm for array sizes of 1 by 1, 3 by 3, 9 by 9, 15 by 15.

For un-gated FET with device dimensions of 2μm x 2μm x 115μm, different sized arrays were characterized and plotted. From the trends of the I-V characterization, a non-zero slope is observed for output conductance g_{out}. In particular, from the characterization of the 15 by 15 array in Figure 33, drain current continues to increase as the drain-to-source voltage is increased above the saturation voltage. This is most likely due to channel

length modulation effects discussed in Chapter 2.1. Channel length modulation in a transistor is caused by the increase of the depletion layer width at the drain as the drain voltage increases [29]. The change in the depletion width at the drain leads to a shorter channel length. As the drain-to-source voltage is increased beyond the saturation voltage, pinch-off effect becomes more pronounced and the effective channel length is reduced. The drain current, which is proportional to $(1/L_{eff})$, increases due to increasing drain voltage.

Another observation made from the I-V characteristics of the different sized arrays is that device breakdown begins at higher operating voltage (> 50V), above which current limiting ceases. Device breakdown was also observed in the early works of high-speed current limiters based on high-field saturation of electron drift velocity in germanium [2]. This effect is possibly dependent upon junction breakdown voltage or impact ionization in the conduction paths. Another possibility is that high doping from the doped poly-silicon layer diffused into the channel, causing current limiting to cease.

After characterizing the un-gated FET for different sized arrays, I-V characterizations for varying cross-sectional channel areas were also conducted. Un-gated FETs with 8μm x 8μm and 12μm x 12μm cross-sectional areas were characterized and plotted in Figure 34. The same pillar thinning effect mentioned in Chapter 4.1 is assumed: un-gated FETs designed with cross-sectional areas of 8μm x 8μm and 12μm x 12μm will have effective cross-sectional areas of 6μm x 6μm and 10μm x 10μm respectively.

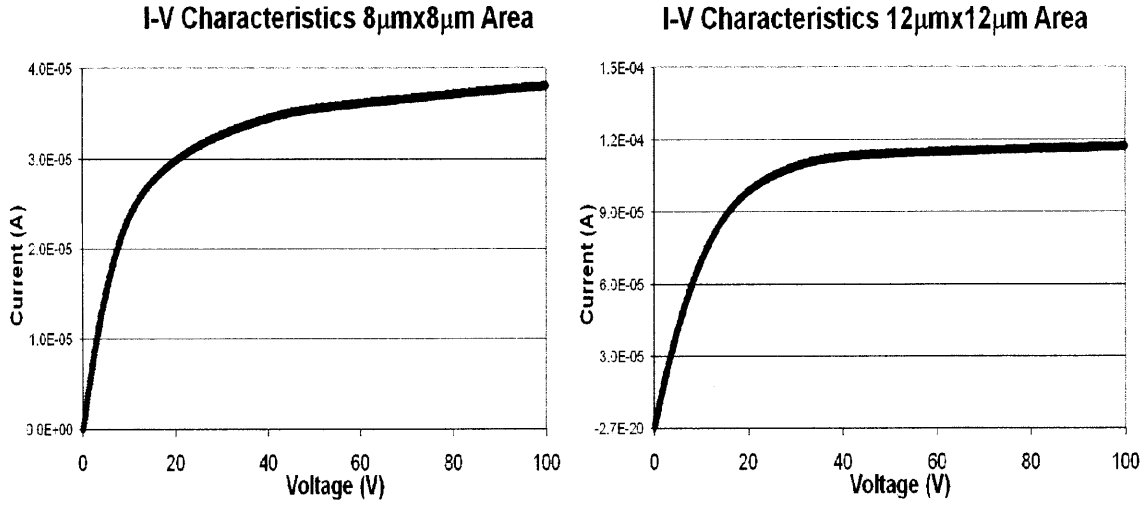

Figure 34. I-V Characteristics for varying cross-sectional areas
I-V Characteristics were taken for un-gated FET structures with dimensions of 6μm x 6μm x 115μm and 10μm x 10μm x 115μm.

Comparisons between the I-V characteristics for varying cross-sectional area show that the saturation voltage occurs at a higher voltage for un-gated FETs with larger cross-sectional areas. From Table 6, the saturation voltage V_{DSS} were 13.5 V and 10.7 V for the un-gated FETs with effective cross-sectional areas of 10μm x 10μm and 6μm x 6μm respectively.

This data trend can be explained by looking back at the velocity saturation at high electrostatic field model in Chapter 2.1. High electrostatic field is achieved by applying voltage across a high aspect ratio structure. Device with the larger cross-sectional area will have a smaller aspect ratio. To compensate the decrease in aspect ratio, more voltage needs to be applied in order to reach high electrostatic field in which velocity saturation occurs.

Once the I-V characteristics were obtained, key device parameters were extracted. The parameters for linear conductance g_{lin}, output conductance, g_{out}, saturation voltage, saturation current, and maximum current were described in Chapter 4.1. Table 6 summarizes the extracted parameters for un-gated FETs with different sized arrays and varying cross-sectional areas within Die 13. The position of Die 13 on the wafer is seen in Figure 31.

Size	Die #	g_{lin} (μS)	g_{out} (nS)	V_{DSS} (V)	I_{DSS} (μA)	I_{max} (μA)
6μmx6μm	13	0.68	8.46	11.8	7.90	8.65
1 by 1	13	0.79	1.95	2.7	2.05	2.20
1 by 1	13	0.67	1.72	2.7	1.55	1.83
3 by 3	13	0.55	2.31	2.1	1.06	1.18
3 by 3	13	0.51	1.84	1.9	0.94	0.99
15 by 15	13	0.39	0.76	2.6	0.63	0.71
Simulation: 1μm x 1μm x 100μm	-	0.12	0.72	6.75	0.82	0.89
Simulation: 2μm x 2μm x 115μm	-	0.198	1.73	10.8	2.16	2.31
Simulation: 6μm x 6μm x 115μm	-	0.378	5.23	14.6	5.53	5.98

Table 5. Comparison of key device parameters

The parameter values were normalized for one silicon pillar from 1 by 1, 3 by 3, 15 by 15 arrays of the un-gated FETs. Parameters extracted from simulations were compared with the device parameters. Observations were drawn from the trends seen in the data.

For consistency, device parameters from 1 by 1, 3 by 3, 15 by 15 arrays of un-gated FETs were compared with simulation values corresponding to its process dimensions of 2μm x

2μm x 115μm. Values from the device parameters were consistent with the simulated parameters, deviating only by a factor of 2 or 3. The deviation of device parameters from the simulation could be explained by fabrication non-idealities not predicted in the simulation. During trench forming step for the deep reactive ion etch described in Chapter 3.4, tapering of the side walls of the silicon pillars were observed in the scanning electron image captured in Figure 19. This means that there are different cross-sectional areas at the drain and source ends.

A comparison is made between the data for the un-gated FET with a 6μmx6μm cross-sectional area and the simulated device with the same cross-sectional area. Again, the device parameters extracted from the fabricated device is consistent with the simulation. In both parameters extracted from the un-gated FETs and the simulation, the parameters did not scale linearly with parameters from un-gated FETs with a different cross-sectional area.

For the different sized arrays of un-gated FETs, normalized parameters were consistent with one another. Another observation is that the normalized parameter values for larger sized arrays, i.e. 15 by 15 arrays, were also smaller than the smaller sized arrays. It signifies that to accurately characterize a single un-gated FET, smaller sized arrays are preferred in place of the larger sized arrays.

To solidify the observations and trends seen in this set of data, more device parameters were extracted and taken at different die locations for 1 by 1 and 3 by 3 un-gated FET

arrays. 1 by 1 and 3 by 3 sized arrays were chosen because limiting the exposed silicon pillars could give a better and more precise characterization of the un-gated device. Table 5 shows a summary of the device parameters extracted from different die located at the center of the wafer.

Size	Die	g_{lin} (μS)	g_{out} (nS)	V_T (V)	I_{DSS} (μA)	I_{max} (μA)
1 by 1	13	0.79	1.95	2.65	2.05	2.20
1 by 1	13	0.67	1.72	2.71	1.55	1.83
1 by 1	20	0.71	1.69	2.78	1.99	2.13
1 by 1	20	0.58	1.74	2.53	1.55	1.73
1 by 1	27	0.63	1.82	2.59	1.64	1.86
1 by 1	27	0.54	2.27	2.68	1.53	1.77
1 by 1	25	0.65	2.82	2.75	2.13	2.35
3 by 3	13	0.55	2.31	2.10	1.06	1.18
3 by 3	13	0.51	1.84	1.90	0.94	0.99
3 by 3	20	0.63	1.71	2.65	1.14	1.28
3 by 3	20	0.49	2.48	2.44	0.93	1.08
3 by 3	27	0.42	2.11	2.38	1.09	1.25
3 by 3	27	0.54	2.38	2.54	1.20	1.38
Simulation: 1μm x 1μm x 100μm	-	0.12	0.72	6.75	0.82	0.89
Simulation: 2μm x 2μm x 115μm	-	0.198	1.73	10.8	2.16	2.31

Table 6. Comparison of key figures of merit (cont.)

Chapter 5 – Conclusion

A process to create silicon pillar arrays to act as vertical current limiters was developed and verified using SILVACO simulation. Test structures of the vertical un-gated FETs were fabricated and tested in the Microsystems Technology Laboratories at MIT. Analytical models to describe current-voltage behavior were derived. Thorough testing of the un-gated FET structures corroborated the anticipated characteristics from simulation runs. To verify the device performance, key device parameters were extracted and compared with simulation.

The use of projection photolithography instead of contact photolithography made it possible to fabricate test structures that exposed selective arrays of silicon pillars for precise characterization. A major challenge in fabricating this test structure was filling of very high-aspect ratio gaps with oxide. Future work is anticipated to develop better fabrication methods to fill the high-aspect ratio gaps. Other anticipated works for improvements in the un-gated FET design include the reduction in dimension of the transistor as well as increase in aspect ratio dimensions.

Recommendations for future work based on experiences learned in this research include exploring spin-on glass or BPSG material as silicon dioxide to fill high aspect ratio gaps. Another recommendation for future work is replacing thin layer deposition of doped poly-silicon with ion implantation.

Appendix – Derivation of the Analytical Model

Velocity saturation model (Parallel Electric Field-dependent Mobility Caughey and Thomas Expression)

$$\mu(E) = \frac{\mu_{n_o}}{\sqrt{1+\left(\frac{\mu_{n_o} E}{v_{satn}}\right)^2}} \qquad \text{and} \qquad v_{satn} = \frac{2.4*10^7}{1+0.8\exp(T_L/600)}$$

v_{satn} saturation velocity of electron
μ_{n_o} low electric field electron mobility
E electric field
T_L lattice temperature.

Electron velocity

$$v(E) = \mu_n(E) * E$$

$$v(E) = \frac{\mu_{n_o} E}{\sqrt{1+\left(\frac{\mu_{n_o} E}{v_{satn}}\right)^2}}$$

Electric Field

$$E = \frac{dV}{dy}$$

Current at any point y

$$I(y) = Aqnv = Aqn\mu_n(E) * E(y) = Aqn\mu_{n_o} \frac{dV}{dy} * \frac{1}{\sqrt{1+\left(\frac{\mu_{n_o}}{v_{satn}} \frac{dV}{dy}\right)^2}}$$

A cross-sectional area
L channel length
q electron charge
n electron concentration
y distance along the current path
V channel potential at y

Device model derivation

Solving the non-linear differential equation with boundary conditions V(0) = 0 and V(L)=V_{DS}

Assume I(y) is constant at any point y, because there is no charge accumulation or storage.

$$\frac{I^2}{\left(Aqn\mu_{n_o}\right)^2\left(\frac{dV}{dy}\right)^2} = \frac{1}{1+\left(\frac{\mu_{n_o}}{v_{satn}}\right)^2\left(\frac{dV}{dy}\right)^2}$$

$$I^2 * \left[1+\left(\frac{\mu_{n_o}}{v_{satn}}\right)^2\left(\frac{dV}{dy}\right)^2\right] = \left(Aqn\mu_{n_o}\right)^2\left(\frac{dV}{dy}\right)^2$$

$$I^2 + \left(\frac{\mu_{n_o}}{v_{satn}}\right)^2\left(\frac{dV}{dy}\right)^2 I^2 = \left(Aqn\mu_{n_o}\right)^2\left(\frac{dV}{dy}\right)^2$$

$$I^2 = \left(\frac{dV}{dy}\right)^2\left[\left(Aqn\mu_{n_o}\right)^2 - \left(\frac{\mu_{n_o}}{v_{satn}}\right)^2 I^2\right]$$

$$I = \left[\left(Aqn\mu_{n_o}\right)^2 - \left(\frac{\mu_{n_o}}{v_{satn}}\right)^2 I^2\right]^{1/2}\frac{dV}{dy}$$

$$\int_0^L Idy = \left[\left(Aqn\mu_{n_o}\right)^2 - \left(\frac{\mu_{n_o}}{v_{satn}}\right)^2 I^2\right]^{1/2}\int_0^{V_{DS}} dV$$

$$I \bullet L = V_{DS}\left[\left(Aqn\mu_{n_o}\right)^2 - \left(\frac{\mu_{n_o}}{v_{satn}}\right)^2 I^2\right]^{1/2}$$

$$I^2 \bullet L^2 = V_{DS}{}^2\left[\left(Aqn\mu_{n_o}\right)^2 - \left(\frac{\mu_{n_o}}{v_{satn}}\right)^2 I^2\right]$$

$$I^2\left[L^2+V_{DS}{}^2\left(\frac{\mu_{n_o}}{v_{satn}}\right)^2\right]=V_{DS}{}^2\left(Aqn\mu_{n_o}\right)^2$$

$$I^2=\frac{V_{DS}{}^2\left(Aqn\mu_{n_o}\right)^2}{L^2+V_{DS}{}^2\left(\frac{\mu_{n_o}}{v_{satn}}\right)^2}$$

$$I=\frac{V_{DS}Aqn\mu_{n_o}}{\sqrt{L^2+V_{DS}{}^2\left(\frac{\mu_{n_o}}{v_{satn}}\right)^2}}=\frac{Aqn\mu_{n_o}}{L}\frac{V_{DS}}{\sqrt{1+\left(V_{DS}\frac{\mu_{n_o}}{Lv_{satn}}\right)^2}}$$

Note that saturation velocity $V_{DSS}=E_{Sat_n}L=\left(\frac{v_{satn}}{\mu_{n_o}}\right)L$

Thus,

$$I=\left(\frac{Aqn\mu_{n_o}}{L}\right)\frac{V_{DS}}{\sqrt{1+\left(\frac{V_{DS}}{V_{DSS}}\right)^2}}$$

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