High Performance Zero-crossing Based Pipelined Analog-to-Digtal Converters

by

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Abstract

As CMOS processes continue to scale to smaller dimensions, the increased f_T of the devices and smaller parasitic capacitance allow for more power efficient and faster digital circuits to be made. But at the same time, output impedance of transistors has gone down, as have the power supply voltages, and leakage currents have increased. These changes in the technology have made analog design more difficult. More specifically, the design of a high gain op-amp, a fundamental analog building block, has become more difficult in scaled processes.

In this work, op-amps in pipelined ADCs are replaced with zero-crossing detectors(ZCD). Without the closed-loop feedback provided by the op-amp, a new set of design constraints for Zero-Crossing Based Circuits (ZCBC) is explored.

Thesis Supervisor: Hae-Seung Lee
Title: Professor

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Chapter 1

Introduction and Background

As CMOS processes continue to scale to smaller dimensions, the increased f_T of the devices and smaller parasitic capacitance allow for more power efficient and faster digital circuits to be made. But at the same time, scaling has increased the design challenges in analog design. Lower output impedance of the transistors, lower power supply voltages, and increased leakage currents have made analog design extremely difficult. More specifically, the design of high gain op-amps, a fundamental analog building block, has become the main bottle-neck in many designs.

In this work, op-amps in pipelined ADCs are replaced with zero-crossing detectors (ZCD). Without the closed-loop feedback provided by the op-amp, a new set of design constraints for Zero-Crossing Based Circuits (ZCBC) is explored.

1.1 Motivations

In traditional pipelined ADC designs, op-amps are used in the switched-capacitor circuit to transfer charge between capacitors. The accuracy and speed of the charge transfer operation is limited by the gain and bandwidth of the op-amp used. But as technology scales, it has become extremely difficult to build high performance op-amps due to limitations of the technology.

First, the intrinsic gain of transistors, the $g_m r_o$ product, is much lower in the smaller technology nodes. This decreases the inherent gain for any given amplifier

topology. It is possible to increase the intrinsic gain of the device by using longer channel lengths. For example, at 32 nm, the intrinsic gain of the NMOS device can be improved from 6 to 9 by doubling the channel length [8]. However, the capacitance added is higher compared to previous technology nodes due to the lower oxide thickness. The increase in capacitance will limit the bandwidth of our operation.

In addition, as technology scales, the power supply voltages are reduced. Lower power supply reduces the power consumption for digital circuits but it also decreases the available signal range for analog signal processing. A lower power supply makes it very difficult to implement cascode structures to achieve higher gain. In addition, to maintain the same signal-to-noise ratio (SNR) in analog circuits, the noise must be reduced proportionally. This requires using bigger capacitors and consuming more power to maintain the speed of operation. For example, if the input range is reduced by a factor 2, then the signal power becomes 4 times smaller. To maintain the same SNR, the noise power also needs to be 4 times smaller. To lower the noise power by 4 times requires using capacitors that are 4 times bigger since noise power is proportional to $\frac{kT}{C}$. In switch-capacitor circuit designs, the bandwidth of the circuit is typically set by the $\frac{g_m}{C}$ ratio. If the C value increases, we must also increase the g_m to maintain the bandwidth. If 4 times the capacitance is used, then 4 times the power must be used to maintain the bandwidth of the circuit. Thus, when the input signal range is reduced by a factor 2, the power consumption needs to be increased to 4x in order to maintain the same SNR and the same speed of operation.

An alternative approach, the Comparator Based Switched-Circuits (CBSC), has been introduced to replace op-amps in switch-capacitor circuits [9]. In this new structure, the high-gain op-amp is replaced by a comparator and a current source. The closed loop operation of the op-amp is substituted with a semi-open-loop structure that achieves the same analog operation. The comparator based switched-capacitor circuit has been shown to be more power efficient than op-amp based designs [9]. Upon further investigation, a more power efficient zero-crossing detector was used to replace the generic comparator used in earlier designs [3]. The zero-crossing based circuits (ZCBC) proved to be much more power efficient compared to traditional

op-amp based ADC designs [3, 4, 10].

The ZCBC technique is not limited to ADCs. It can be applied to many other switched-capacitor circuits including filters [6], integrators in sigma-delta converters [5], and switched-capacitor DACs.

In this work, new circuit techniques are applied to improve the performance of ZCBC. The results are demonstrated through a 12-bit 100MS/s pipeline ADC and a 10-bit 450 MS/s time interleaved ADC. In the design of the 100 MS/s ADC, a new type of current source which has better linearity compared to the traditional cascoded current source is explored. The Decision Boundary Gap Estimation (DBGE) techinique was used to correct for systematic capacitor mismatch in the 12-bit 100 MS/s ADC. This is the first hardware demonstration of the DBGE. A new reference precharging technique was introduced to reduce the disburbance on the reference voltages in both of the ADC designs.

Chapter 2

Traditional Pipelined ADCs

There are many types of analog-to-digital converters. The performance space of various ADC architectures is shown in Figure 2-1. Each architecture is best suited for a specific range of resolution and speed. As shown in Figure 2-1, Flash ADCs are the best choice for low resolution and high speed applications. Sigma Delta ADCs are used in slower speed and higher resolution applications.

The pipelined ADC is well suited for medium to high resolution and high speed applications. There are a few clock cycles of latency due to the pipelined operation of this structure. However, in many applications, the latency is well tolerated. Commericial pipelined ADCs provide resolutions from 8b to 16b and have sampling rates between 1MS/s to 250 MS/s. They are used in many applications including wireless systems, wireline systems, medical electronics, video capture, and test equipments. This chapter will provide an overview of the pipelined ADC's architecture and operation.

2.1 Circuit architecture and operation

The pipelined ADC, shown in 2-2, consists of a number of nearly identical stages. Each stage resolves n bits and produces a residue voltage to pass to the next stage. Each ADC stage alternates between sampling the input from the previous stage and producing a residue voltage for the next stage. The digital bits of all the stages are

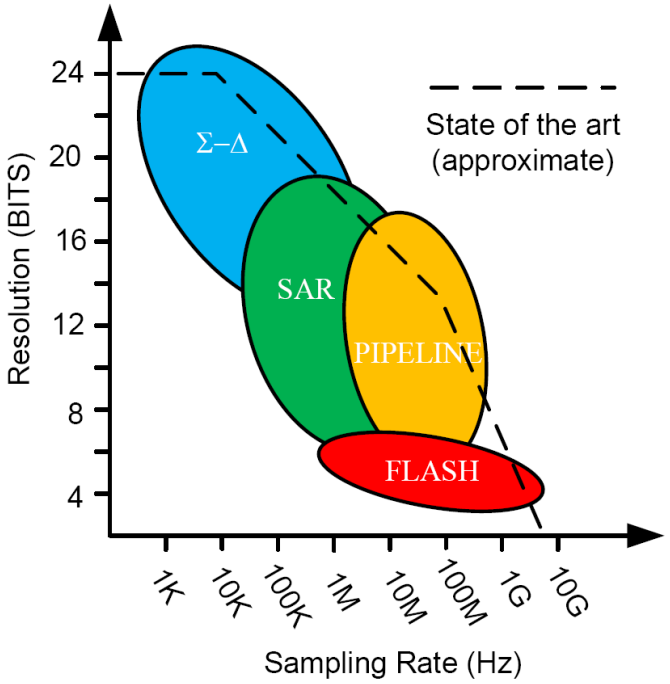


Figure 2-1: ADC architectures

time-aligned using a shift-register and the ADC outputs a total of n × M bits, where n is the number of bits resolved in each stage and M is the total number of stages.

Figure 2-3 shows the structure of a single stage of the pipelined ADC. It is comprised of an n-bit ADC, an n-bit digital-to-analog converter (DAC), and a residue amplifier. The n-bit ADC is typically made using a flash ADC. The DAC generates an analog signal that is proportional to the input signal. The residue amplifier subtracts out the analog representation of the quantized signal from the analog input signal, and then amplifies the residue voltage by 2^n. The amplified residue voltage is further quantized in the following stages.

For the case of a 1 bit per stage pipelined ADC, each stage first determines weather the input signal is above or below the middle level. Then it amplifies and shifts the residue so the output range takes up the entire range in the next stage. This operation continues down the pipeline until the analog signal quantization is complete. The number of quantization levels in the ADC can be increased by increasing the number of pipelined stages. However, the resolution of the ADC will be limited by thermal

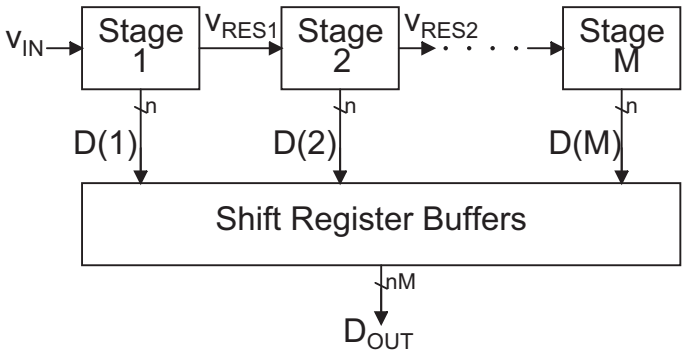


Figure 2-2: Pipelined ADC architecture [1]

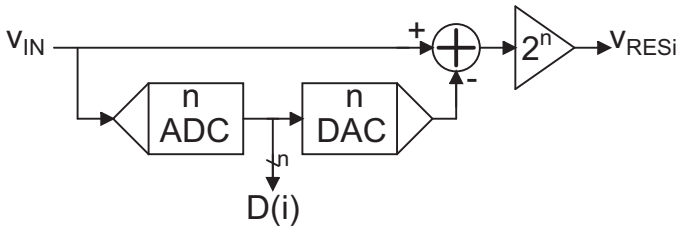


Figure 2-3: Pipelined ADC Stage [1]

noise and errors due to finite op-amp gain and capacitor mismatch.

2.2 Op-amp Based Circuit Implementation

Traditional pipelined ADCs use op-amps placed in feedback configurations to perform the residue amplification. The DAC and the subraction operation are integrated with the op-amp to perform this function. The circuit implementation of a 1-bit per stage pipelined ADC is shown as an example in 2-4. In Figure 2-4, the switched-capacitor circuit consisting of C_1, C_2, and the op-amp is commonly referred to as a Multiplying Digital-to-Analog Converter (MDAC).

This circuit operates in two phases. In the first phase, the input is sampled on C1 and C2. In addition, the 1-bit flash ADC's decision is latched at the end of the first

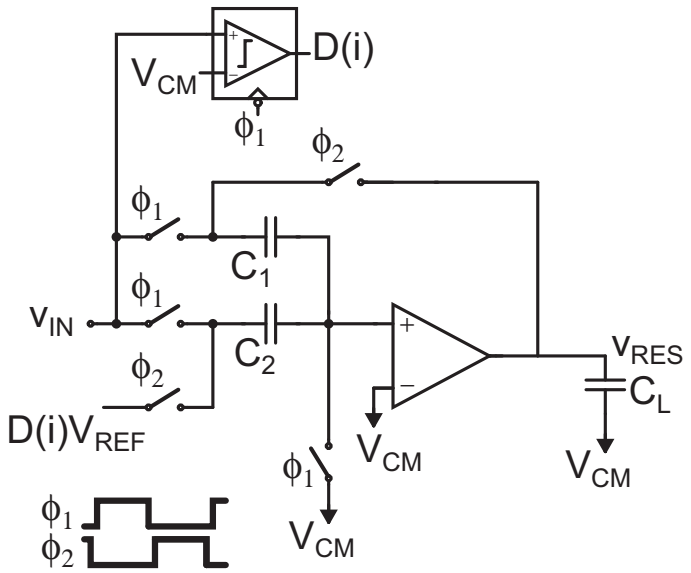


Figure 2-4: Traditional op-amp based 1 bit per stage pipelined ADC stage [1]

phase, Φ_1. During the second phase, when Φ_2 is high, the op-amp forces the voltage on its non-inverting input to equal that on its inverting input. When this condition is reached, the output of the op-amp settles to the correct output voltage. For a 1 bit per stage implementation, the output voltage settles to

$$v_{RES} = \frac{C_2 + C_1}{C_1} v_{IN} - D(i)\frac{C_2}{C_1} V_{REF} \tag{2.1}$$

where $D(i)$ is either +1 or -1 depending on the bit decision from the comparator. If there is an offset in the bit decision, as shown in the dotted line in figure 2-5, the output residue will exceed the maximum range of subsequent stages. The subsequent stages will then be saturated and information about the signal will be lost. Once a stage is saturated, a wider range of analog input voltage will produce the same digital code. This is called a wide code and it adds Differential Nonlinearity (DNL) to the ADC. The DNL of a particular ADC code is defined to be the difference between the size of the bin compared to the ideal width of the ADC bin.

A common way to protect the ADC from comparator offsets is to add redundant comparators. Extra bit-decision comparators are used in the flash ADC to divide the residue into smaller pieces. This prevents the residue from going out of range when

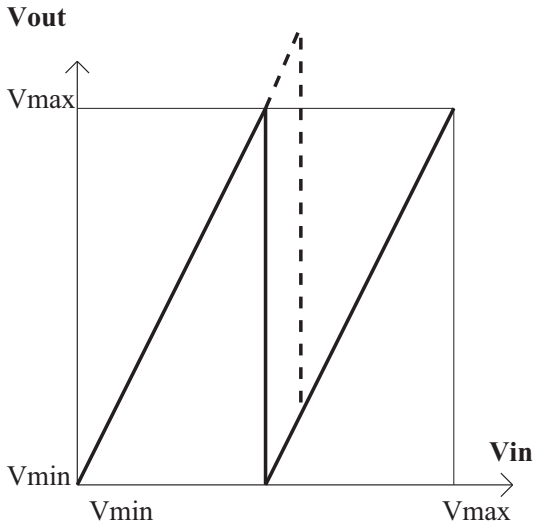


Figure 2-5: Single pipeline stage residue plot

there is a limited amount offset. The 1.5b per stage algorithm uses two comparators in the flash ADC [11–13]. The redundancy allows the circuit to correct for offsets up to 1/8 of the input range. A more detailed description of the general pipelined ADC structure can be found in Abo's thesis [14].

2.3 Op-amp Design Requirements

The op-amp is a fundamental building block in traditional pipelined ADCs. Shown in Figure 2-4, the op-amp is a part of a switched-capacitor circuit used to transfer the residue between the pipelined stages. The accuracy of the ADC is often limited by the performance of the op-amp used. In this section, the op-amp's effect on the ADC's accuracy is discussed.

2.3.1 Op-amp Gain Requirement

The residue amplifier consists of capacitors and an op-amp placed in feedback. Assuming that the op-amp has enough time to settle completely and that the capacitors are perfectly matched, the accuracy of the charge transfer is limited by the DC gain of the op-amp. The model shown in Figure 2-6 is used to model the op-amp with

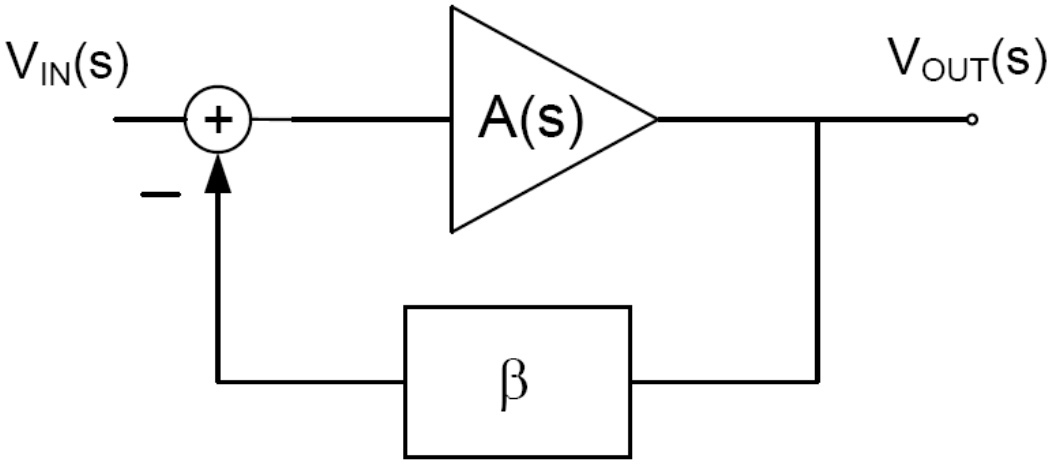


Figure 2-6: Model of the op-amp and the feedback network

feedback. A(s) is the op-amp's open loop transfer function and β is the feedback factor.

The closed loop transfer function of the op-amp circuit shown in Figure 2-6 can be written as

$$\begin{aligned} A_{CL}(s) &= \frac{A(s)}{1 + A(s)\beta} \\ &= \frac{1}{\beta}\frac{A(s)\beta}{1 + A(s)\beta}. \end{aligned} \tag{2.2}$$

The ideal DC gain is $\frac{1}{\beta}$. If we assume that the op-amp is fully settled, the actual gain is smaller than the ideal gain by a factor of $\frac{1}{1+A_{DC}\beta}$, where A_{DC} is the DC gain. Thus, the amplification factor of the stage will be slightly smaller than the desired value. The effect of the this gain error on the residue amplifier can be seen in the residue plot shown in Figure 2-7.

If the DC gain is known, it is possible to remove this gain error in the digital domain using gain-error calibration techniques. However, the exact DC gain may be difficult to measure because it varies with the output voltage, process, and tempera-

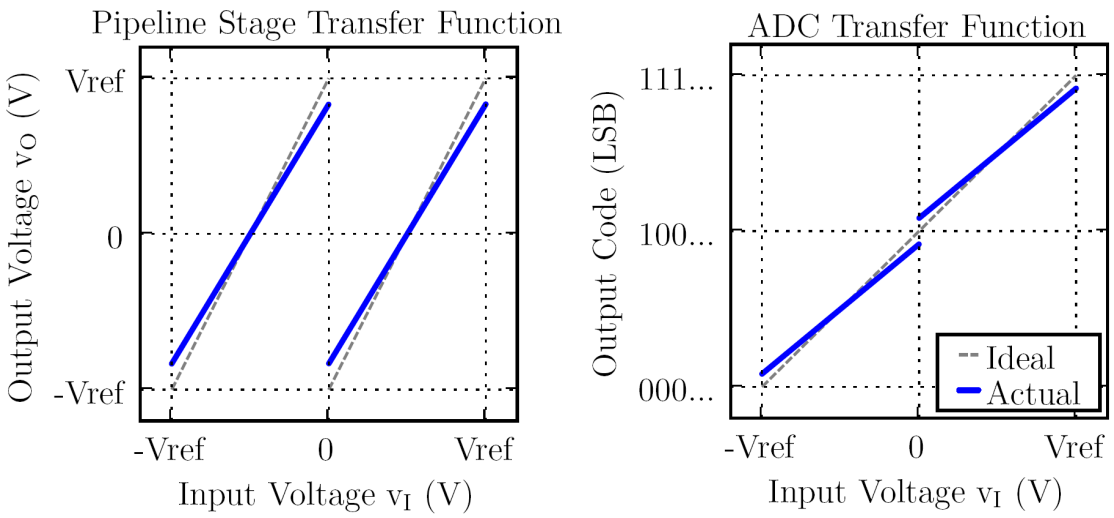


Figure 2-7: Effects of gain error on the pipelined stage transfer function [2]

ture. Thus, high gain in the op-amp is desired to minimize the gain error.

2.3.2 Op-amp Stability

Shown in Figure 2-4, the op-amp is used in a feedback network. Thus, the stability and phase margin of the system is important. The op-amp with feedback is modeled in Figure 2-6. A(s) represents the op-amp's open loop transfer function and β is the feedback factor. The loop transmission L(s) is equal to A(s)β. L(s) is used to determine the phase margin and the stability of the feedback circuit [15].

In the telescopic op-amp and the folded cascode op-amp, the dominant pole is typically at a much lower frequency compared to the other poles in the circuit [15]. Thus, the phase margin is usually high and the circuit is very stable. However, in a 2-stage op-amp design, the second pole loction is often too close to the first pole location and compensation techniques are required to ensure that the phase margin is sufficient [16]. Insufficient phase margin will result in ringing in the output step response and increased settling time, or even oscillation.

2.3.3 Op-amp Bandwidth and Settling Time

When there is only one dominant pole, the op-amp's transfer function can be modeled as

$$A(s) = \frac{A_{DC}}{1 + s/\omega_{p1}}, \tag{2.3}$$

where ω_{p1} is the dominant pole frequency. In this case, using the closed loop model shown in Figure 2-6, the closed loop transfer function can be written as

$$A_{CL}(s) = \frac{1}{\beta} \cdot \frac{1}{1 + s/\beta\omega_u}, \tag{2.4}$$

where ω_u, which is equal to $A_{DC}\omega_{p1}$, is the unity gain frequency of the op-amp [16]. The -3 dB frequency ω_{3dB} of the closed-loop transfer function is given by $\beta\omega_u$. The error voltage of the step-response is a decaying exponential, and the settling time constant τ of the closed-loop amplifier is then given by $\frac{1}{\omega_{3dB}}$. While the amplifier is settling, the error voltage of the step response for this amplifier is proportional to $e^{-t/\tau}$. For example, if 0.1 percent accuracy is required, then one must allow $e^{-t/\tau}$ to settle to 0.001, which corresponds to approximately $\frac{t}{\tau} = 7$.

2.3.4 Op-amp Noise

For the single-stage amplifiers such as the differential pair, telescopic amplifier, and folded cascode, the input-referred noise spectral density N can be found by using the ratios of the transconductances in the op-amp [15]. In the case when there is only one dominant pole, the noise bandwidth f_N can be shown to be $\frac{\pi}{2} \cdot \omega_{3dB} \cdot \frac{1}{2\pi}$, where ω_{3dB} is the -3 dB frequency of the closed loop transfer function (Appendix C). The input referred noise power of the op-amp is then given by $N \cdot f_N$ if we assume that the noise spectral density is constant within the circuit's bandwidth.

For the two-stage op-amp, the first stage and the second stage both contribute noise. The simplified half circuit shown in Figure 2-8 can be used to model a fully differential 2-stage op-amp with the capactive feedback network. The first stage of

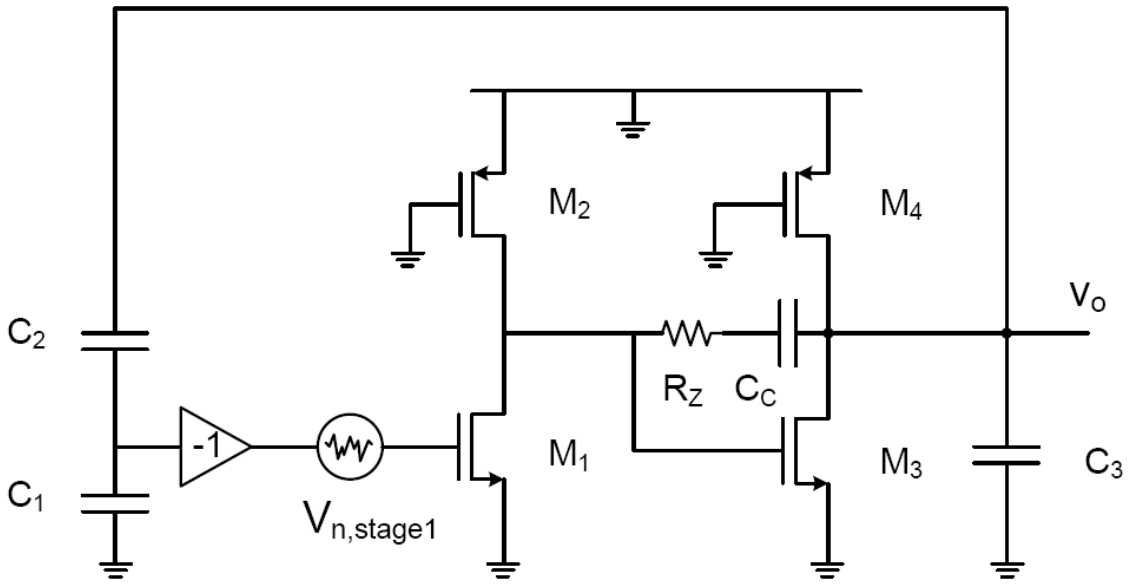


Figure 2-8: Simplified circuit model of a 2-stage op-amp with feedback

the 2-stage op-amp is modeled by M_1 and M_2. R_z, and C_c are the nulling resistor and the compensation capacitor, respectively.

The total noise contribution of each stage can be caculated by multiplying the noise spectral density and the noise bandwidth. For the first stage, M1 contributes a current noise power thats given by $4kT\gamma \cdot g_{m1}$ and M2 contributes a current noise power thats given by $4kT\gamma \cdot g_{m2}$. Thus the input referred noise spectral density is given by Equation 2.5. In this equation, k is the Boltzmann's constant, T is the temperature in Kelvin, and γ is a constant that is approximately 2/3 for MOS devices in strong inversion and saturation.

$$N_1 = 4kT\gamma \cdot \frac{g_{m2} + g_{m1}}{(g_{m1})^2} \tag{2.5}$$

In Figure 2-8, the input-referred noise of the first stage is added to the voltage from the feedback network. Thus, the noise transfer function (NTF) of the input referred noise of the first stage can be modeled by the feedback block diagram shown in Figure 2-6. The NTF of the input-referred noise $H_1(s)$ is given by equation 2.6.

$$\begin{aligned} H_1(s) &= \frac{A(s)}{1+A(s)\beta} \\ &= \frac{1}{\beta}\frac{A(s)\beta}{1+A(s)\beta}. \end{aligned} \tag{2.6}$$

And if we assume that the second pole frequency ω_{p2} is much greater than the unity gain frequency, we can approximate A(s) as $\frac{A_{DC}}{1+s/\omega_{p1}}$. By applying this A(s) in Equation 2.6, the following expression for the NTF of the first stage's input referred noise is derived.

$$H_1(s) = \frac{1}{\beta} \cdot \frac{1}{1+s/\beta\omega_u}, \tag{2.7}$$

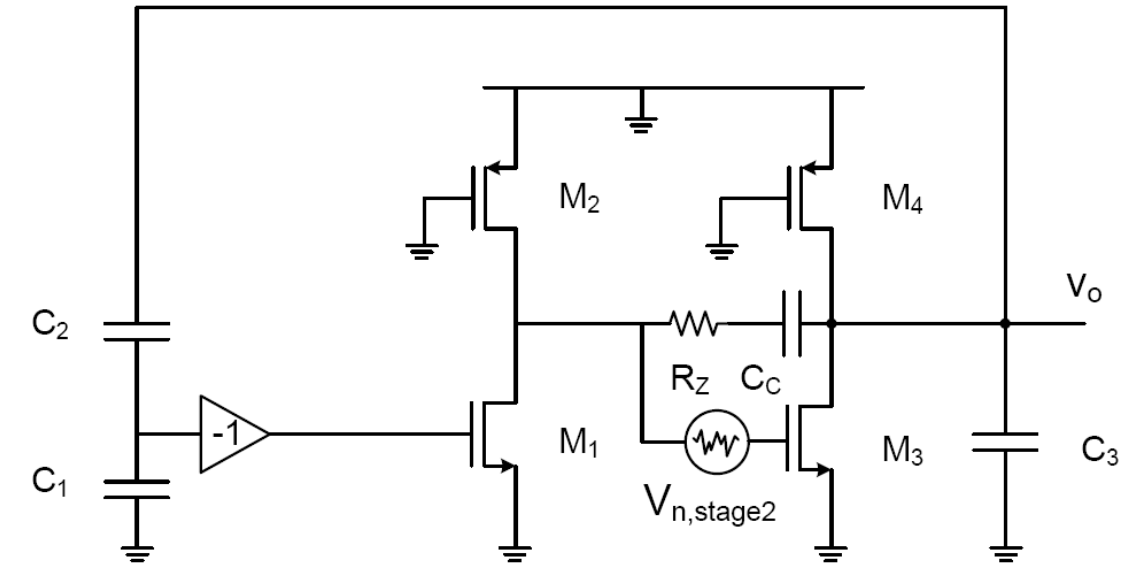
where the unity gain frequency of the op-amp is given by ω_u, which is equal to $A_{DC}\omega_{p1}$. From Equation 2.7, the noise bandwidth f_{N1} can be derived. The expression of the noise bandwidth of the first stage noise is shown in Equation 2.8.

$$\begin{aligned} f_{N1} &= \beta\omega_u \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi} \\ &= \frac{\beta\omega_u}{4}, \end{aligned} \tag{2.8}$$

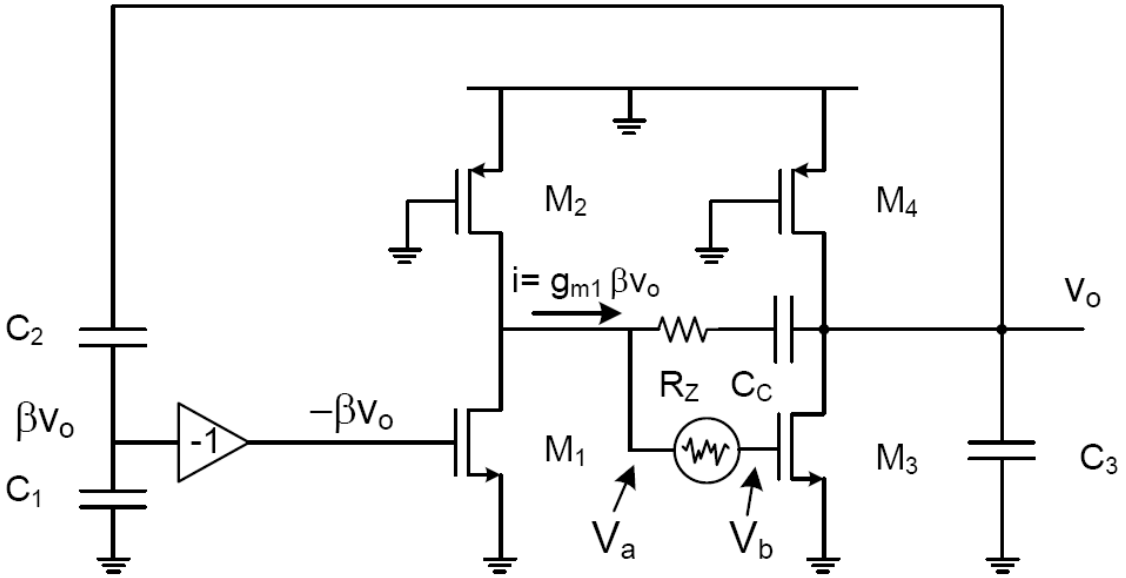
Similarly, the noise spectral density of the second stage's noise referred to the input of the second stage can by described by Equation 2.9.

$$N_2 = 4kT\gamma \cdot \frac{g_{m3}+g_{m4}}{(g_{m3})^2} + 4kTR_z \tag{2.9}$$

The noise transfer functions of the second stage noise can be calculated using the circuit shown in Figure 2-9. The voltage source attached to the gate of M_3 represents the input-referred noise of the second stage. KCL and KVL can be applied to derive



(a)



(b)

Figure 2-9: Second stage noise model
(a) Second stage noise model (b) Illustration of the second-stage NTF calculation

the NTF of the input-referred noise of the second stage.

In Figure 2-9(b), the nodes around the input-referred noise source are labeled V_a and V_b. The output resistance of the transistors is assumed to be infinite for this calculation. By applying KCL and KVL, the following equations can be written.

$$\begin{aligned} V_a &= V_o + \beta V_o g_{m1} \left(R_z + 1/sC_C\right) \\ &= V_o \left(1 + \beta g_{m1} \left(R_z + 1/sC_C\right)\right) \end{aligned} \tag{2.10}$$

KVL can be applied the output node V_o to derive an expression for V_b.

$$V_o = \frac{1}{sC_T} \left(g_{m1}\beta V_o - g_{m3} V_b\right) \tag{2.11}$$

Equation 2.11 can be rearranged to produce Equation 2.12. C_T represents the total capacitance seen at the V_o node.

$$V_b = V_o \left(\frac{\beta g_{m1}}{g_{m3}} - \frac{sC_T}{g_{m3}}\right) \tag{2.12}$$

The NTF of the second stage is given by

$$\begin{aligned} H_2(s) &= Vo/V_{n,stage2} \\ &= Vo/(V_a - V_b) \end{aligned} \tag{2.13}$$

By using the expresions from Equations 2.10 and 2.12, and if we assume that the nulling resistor Rz is equal to $1/g_{m3}$, then $H_2(s)$ can be reduced to

$$H_2(s) = \frac{sg_{m3}C_C}{s^2 C_T C_C + sC_C g_{m3} + \beta g_{m1} g_{m3}}$$

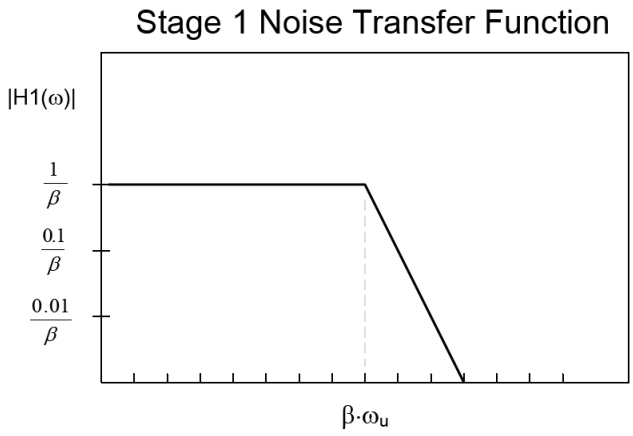


Figure 2-10: Noise transfer function of the first stage

$$= \frac{sC_C/\beta g_{m1}}{\frac{C_T C_C}{\beta g_{m1} g_{m3}} s^2 + \frac{C_C}{\beta g_{m1}} s + 1}$$

$$= \frac{s/\beta\omega_u}{\frac{s^2}{\beta\omega_u \omega_{p2}} + \frac{s}{\beta\omega_u} + 1} \tag{2.14}$$

where, the unity gain frequency of the op-amp ω_u is given by g_{m1}/C_c and second pole frequency ω_{p2} is given by g_{m3}/C_T. If we assume that ω_{p2} is at a much higher frequency than ω_u, the noise transfer function $H_2(s)$ can be approximated by Equation 2.15.

$$H_2(s) \approx \frac{s/\beta\omega_u}{(1 + s/\beta\omega_u)(1 + s/\omega_{p2})} \tag{2.15}$$

The noise transfer function of the first stage and second stage are plotted in Figures 2-10 and 2-11. The noise transfer function of the first stage is shaped by the transfer function of the op-amp with feedback which is a low pass system. The -3 dB frequency is set by the closed-loop bandwidth of the system. The noise transfer function of the second stage is bandpass. At very high frequencies, the noise of the second stage is filtered by the pole of the second stage ω_{p2}. At low frequencies, the noise of the second stage is rejected by the loop gain of the system.

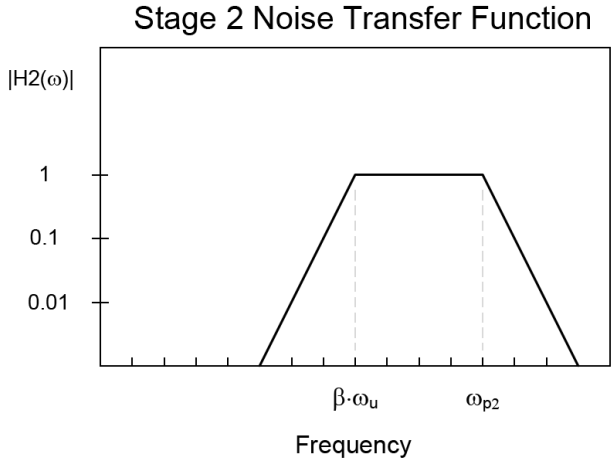


Figure 2-11: Noise transfer function of the second stage

The noise bandwidth of the second stage's noise transfer function is shown in Equation 2.16. The derivation for the noise bandwidth of a bandpass transfer function is derived in Appendix C of this thesis.

$$\begin{aligned} f_{N2} &\approx (\omega_{p2} - \beta\omega_u) \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi} \\ &\approx \frac{(\omega_{p2} - \beta\omega_u)}{4} \end{aligned} \tag{2.16}$$

Using the noise spectral density and the noise transfer function, we can compare the second stage's noise contribution to the output compared to the first stage's noise contribution. The noise at the output that is contributed by the first stage is given by

$$\begin{aligned} {v_{o1}}^2 &= \int_0^\infty N_1 |H_1(\omega)|^2 d\omega \\ &= N_1 \cdot \frac{1}{\beta^2} \cdot \frac{\beta\omega_u}{4} \\ &= N_1 \cdot \frac{\omega_u}{4\beta} \end{aligned} \tag{2.17}$$

and the noise at output that is contributed by the second stage is given by

$$
\begin{aligned}
{v_{o2}}^2 &= \int_0^\infty N_2 |H_2(\omega)|^2 d\omega \\
&\approx N_2 \cdot \frac{(\omega_{p2} - \beta\omega_u)}{4}.
\end{aligned} \tag{2.18}
$$

According to Equation 2.5, g_{m2} should be made to be smaller than g_{m1} in order to reduce the input-referred noise spectral density. In the design of the first stage, g_{m2} is set to $\frac{g_{m1}}{2}$. In the second stage, the V_{DSAT} of M_3 and M_4 are assumed to be equal to achieve a balanced output swing. And since g_m is equal to $\frac{2I_D}{V_{DSAT}}$, g_{m3} and g_{m4} are assumed to be equal.

To make a simple comparison between the first stage and the second stage, the power consumption is made equal and thus g_{m1} is equal to g_{m3}. In the second stage, the nulling resistor R_z is made to equal $\frac{1}{g_{m3}}$ to cancel out the right half plane zero [15]. Using the expressions in Equations 2.5 and 2.9, we can see that the input-referred noise spectral density of the second stage is equal to 7/3 times the input-referred the noise spectral density of the first stage.

$$
\begin{aligned}
\frac{N_2}{N_1} &= \frac{4kT\gamma \cdot \frac{g_{m3}+g_{m4}}{(g_{m3})^2} + 4kTR_z}{4kT\gamma \cdot \frac{g_{m2}+g_{m1}}{(g_{m1})^2}} \\
&= \frac{4kT\gamma \cdot \frac{g_{m3}+g_{m3}}{(g_{m3})^2} + \frac{4kT}{g_{m3}}}{4kT\gamma \cdot \frac{0.5g_{m1}+g_{m1}}{(g_{m1})^2}} \\
&= 7/3
\end{aligned} \tag{2.19}
$$

As the settling accuracy requirement is made more stringent, the fastest settling response is a critically damped response [14]. To achieve critical damping, the second pole location ω_{p2} is set to be 4x of the unity gain frequency of the loop transmission, which is at $\beta\omega_u$. When the two pole op-amp is critically damped, it has a phase margin of 76.3 degrees. In this case, when ω_{p2} is equal to $4\beta\omega_u$, the noise bandwidth of the NTF of the second stage is approximately equal to $\frac{4\beta\omega_u - \beta\omega_u}{4}$ according to Equation

2.16. The second stage noise bandwidth is equal to $\frac{3\beta\omega_u}{4}$, which is 3 times as large as the first stage noise bandwidth, which is given by $\frac{\beta\omega_u}{4}$.

In general, if ω_{p2} is set to be M times higher fequency compared to $\beta\omega_u$, then the noise bandwidth of the second stage is approximately M-1 times that of the first stage according to Equation 2.8 and 2.16. The ratio of the output referred noise contribution between the first stage and the second stage can be written as

$$\begin{aligned} \frac{v_{o2}^2}{v_{o1}^2} &= \frac{N_2 f_{N2}}{N_1 f_{N1} \cdot \frac{1}{\beta^2}} \\ &= \frac{N_2}{N_1}\beta^2\frac{f_{N2}}{f_{N1}} \\ &= \frac{7}{3}\beta^2\,(M-1) \end{aligned} \tag{2.20}$$

With M set to 4, the ratio between the output-referred noise from the second stage compared to that of the first stage is plotted versus the feedback factor β in Figure 2-12. As Figure 2-12 shows, the noise contribution of the second stage can be 7 times as large as the first stage noise under unity-gain feedback. When the feedback factor is smaller, the output-referred noise from the first-stage becomes more dominant compared to the noise contributed by the second stage. For example, when the feedback factor is 1/2, the second stage's noise contribution is 1.75 times that of the first stage.

In the example above, the power consumption in the second stage is assumed to be equal to the power used in the first stage. However, this may not be the optimal bias condition in terms of noise and power efficiency. Instead using the same amount of power in both stages, suppose that the second stage power used is K times that of the first stage. Then g_{m3} is equal to Kg_{m1}. By using this value of g_{m3} in Equation 2.19, the $\frac{N_2}{N_1}$ ratio is given by $\frac{7}{3K}$. To maintain the same settling time-constant, we assume that the pole locations are fixed. And by applying this result to Equation 2.20, we can write

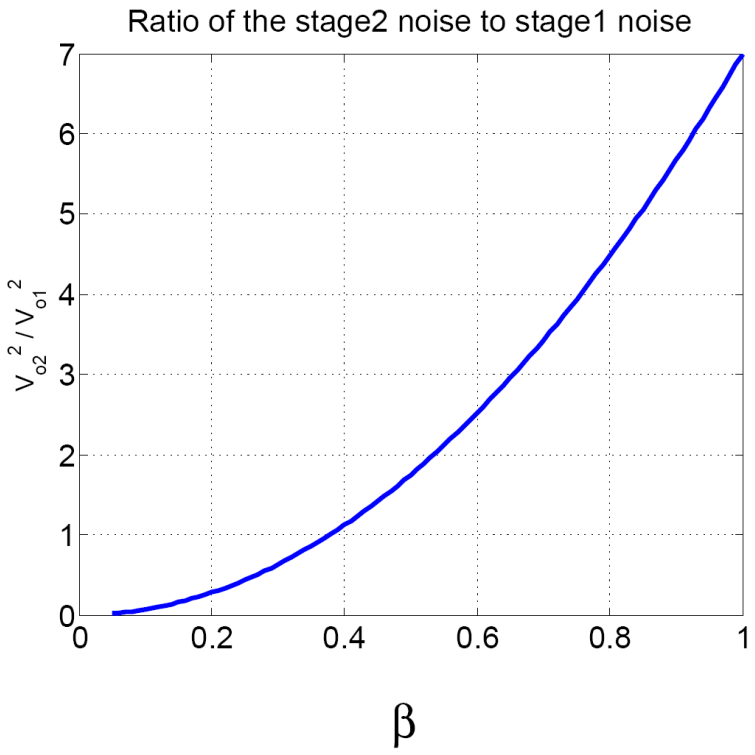


Figure 2-12: Ratio of the second stage noise compared to the first stage noise

$$\begin{aligned} \frac{v_{o2}^2}{v_{o1}^2} &= \frac{N_2}{N_1}\beta^2\frac{f_{N2}}{f_{N1}} \\ &= \frac{7}{3K}\beta^2\left(M-1\right). \end{aligned} \tag{2.21}$$

The total noise at the output is the sum between v_{o1}^2 and v_{o2}^2. As the value of K increases, the second stage's noise contribution v_{o2}^2 is reduced at the cost of more power. Given a power budget, it is efficient to distribute the power in a way such that minimizes the total noise. If we fix the power and noise of the first stage, K can be varied to minimize the total noise and power product. Thus, it is desirable to minimize the normalized noise and power product NP which is shown in equation 2.22.

$$NP = \left(1 + \frac{v_{o2}^2}{v_{o1}^2}\right)(1+K) \tag{2.22}$$

The ratio of v_{o2}^2 and v_{o1}^2 is given by Equation 2.21, thus the expression of the noise and power product NP can be re-written as

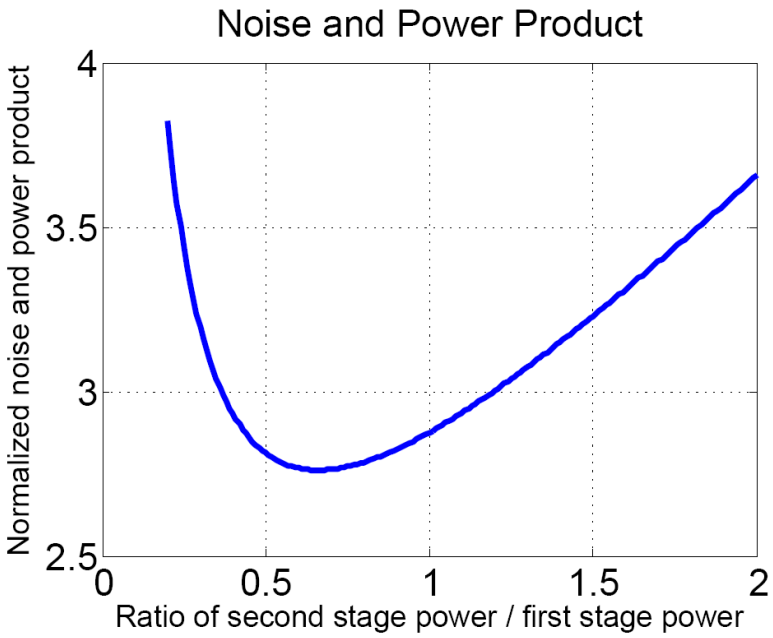
$$NP = \left(1 + \frac{7}{3K}\beta^2 (M-1)\right)(1+K) \tag{2.23}$$

For a given M, and β, there is a value of K that minimizes NP. By setting the derivative of NP as a function of K to 0, we can find the value of K that minimizes NP. In this case, the choice of K = $\sqrt{\frac{7}{3K}\beta^2 (M-1)}$ minimizes NP.

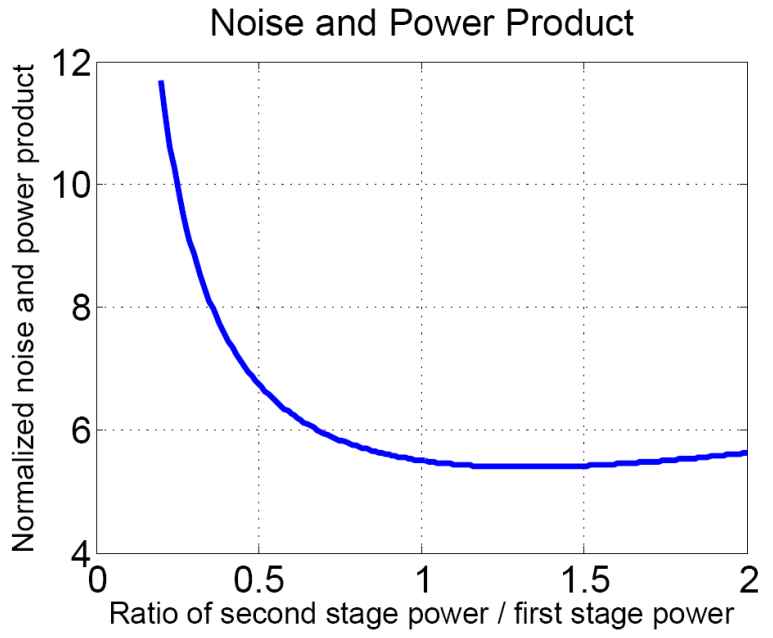
NP can also be plotted as a function of K when given M and β. In Figure 2-13(a), M is set to 4, and β is set to 1/4. In optimal value of K is 0.66. In Figure 2-13(b), M is set to 4, and β is set to 0.5. In this case the optimal value of K is 1.32. This is expected since for $\beta = 0.5$, the second stage noise becomes more dominant compared to the first stage noise, thus higher power helps to reduce the total noise at the output.

2.4 Summary

In a high speed, high-accuracy pipelined ADC using op-amp based circuits, the op-amp's performance is the key to achieving the desired design target. However, as technology continues to scale, it has become extremely difficult to design high performance op-amps. In addition, high-performance op-amps cost significant power, making such circuits unattractive in low-power applications. The focus of this works is to demonstrate an alternative approach for switched-capacitor circuit design.



(a)



(b)

(a) M is set to 4 and β is set to 1/4 (b) M is set to 4 and β is set to 1/2

Figure 2-13: The normalized product of noise power and power consumption

Chapter 3

Zero-Crossing Based Pipelined ADC Design

Zero-crossing Based Circuits(ZCBC) were introduced as a low power alternative for building switched capacitor circuits [3, 9]. The closed-loop op-amp structure used in switched-capacitor circuits is replaced with a semi open-loop topology to achieve the same analog operation. ZCBC can be used in many different switched-capacitor circuits including filters, DACs, integrators, and ADCs. It has been shown that ZCBC is more power efficient compared to traditional op-amp based switched-capacitor circuits [3, 4, 9]. This chapter will describe the circuit implementation of ZCBC and the operation and also describe the recent work in zero-crossing based circuits.

3.1 ZCBC Architecture and Operation

A simplified schematic of a zero-crossing based 1 bit per stage pipelined ADC stage is shown in 3-1. ZCBC maintain the same basic switched-capacitor structures used in traditional op-amp based switched-capacitor circuits. The switches and the capacitor array configurations are maintained while the op-amp is replaced with a zero-crossing detector and a current source.

In the case of a pipelined ADC design, the zero-crossing based residue amplifier stage operates on a similar two phase cycle as an op-amp based switched-capacitor

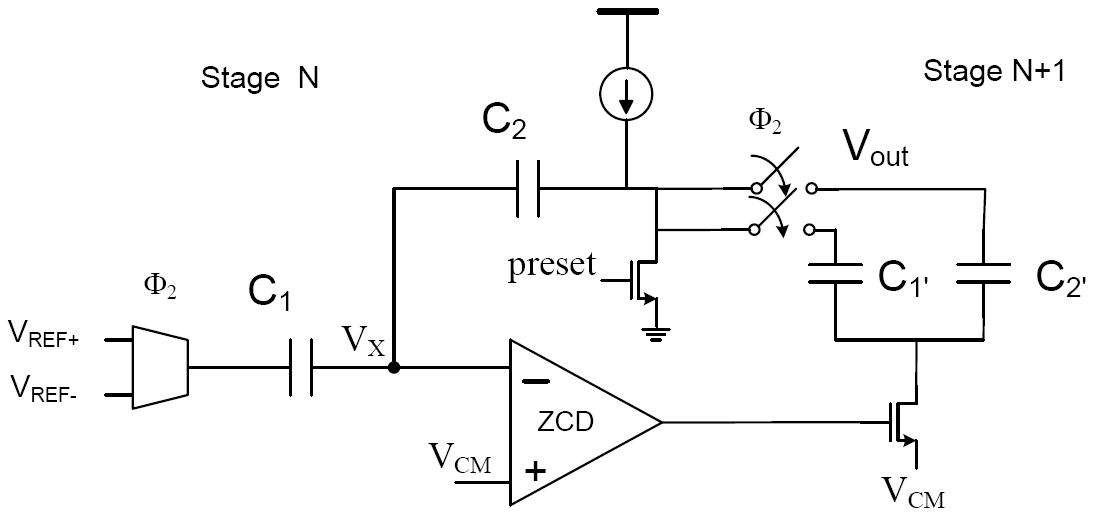


Figure 3-1: Simplified schematic of the zero-crossing based charge transfer

residue amplifier stage. During the sampling phase, the operation of ZCBC is identical to the sampling phase of the op-amp based circuit. Bottom plate sampling is used to reduce input dependent charge injection which degrades linearity [17].

During the charge transfer phase ϕ_2 , the output node is initially preset to the lowest potential in the system. After the preset phase, the current source charges the output capacitors and the output voltage increases linearly at the rate of $\frac{I}{C_T}$ where C_T is the effective capacitive loading at the output node and I is the current generated by the current source. The voltage at the output node capacitively couples to the V_X node, which also ramps up linearly. In an op-amp based gain stage, the charge transfer is complete once the op-amp forces the voltage on the V_X node to equal V_{CM}. In the ZCBC implementation, rather than forcing this virtual ground condition, a zero-crossing detector (ZCD) is used to detect the virtual ground condition. When the voltage on the V_X node reaches V_{CM}, the ZCD turns off the sampling switch of the next stage and the charge transfer is complete. The analog voltage sampled on the output capacitors is the same as the output voltage of the op-amp in an op-amp based switched capacitor circuit if the sampling occurs exactly at zero-crossing. The finite delay of the ZCD and the nonlinearity of the ramp contribute errors that are

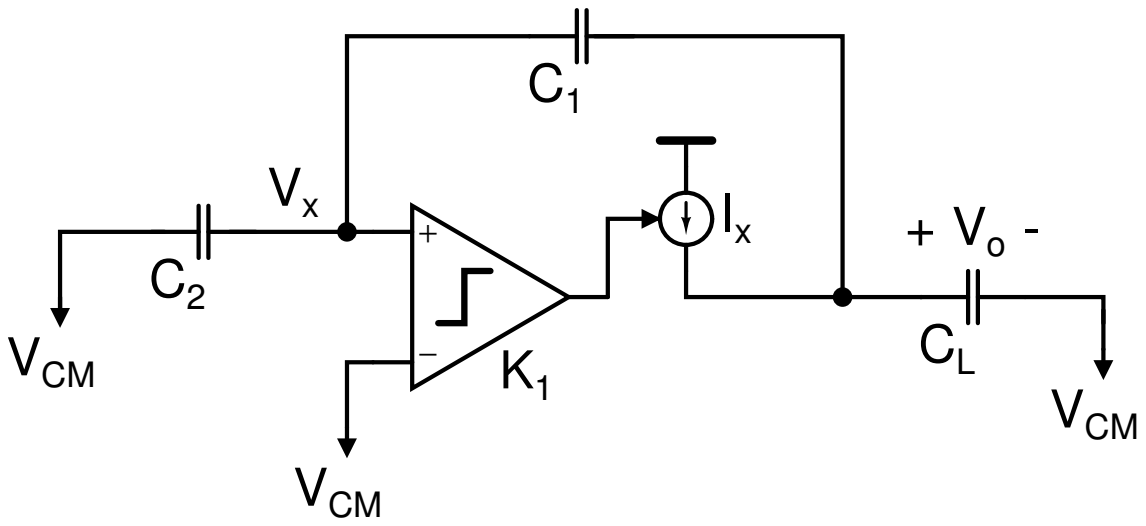


Figure 3-2: Schematic of the comparator based switched-capacitor residue amplifier

decribed in the next chapter.

3.2 Prior Work

There have been a few previous works in ZCBC [3–6, 9, 10]. They have demonstrated the functionality as well as the power efficiency of this new circuit topology. This section will give a brief description of the innovations presented in the recent work related to ZCBC.

3.2.1 First Prototype

The first prototype was a pipelined ADC implemented in 0.18 um CMOS process [9]. In this first prototype, a comparator was used instead of the zero-crossing detector which was introduced later. This comparator based-switched capacitor ADC was the first to prove the functionality of zero-crossing based circuits. The comparator based circuit was used in the residue amplifier of the pipelined ADC as shown in Figure 3-2. The ADC achieved 8.6 ENOB while sampling at 10 MS/s. The figure of merit was 0.8 pJ per step.

3.2.2 Dynamic ZCD design

In the second prototype, a more power efficient zero-crossing detector is used to replace the comparator. A comparator is designed to compare two arbitrary voltages. However, in ZCBC, the input voltages are always linear ramp signals approaching from one direction. In addition, the detection is only required during an interval of time close to the zero-crossing; thus, only a zero-crossing function is needed from the comparator. In the second prototype, a dynamic zero-crossing detector replaced the comparator [3]. The dynamic zero-crossing detector, shown in the dotted box in Figure 3-3, only consumes power when it is needed during the time interval close to the zero-crossing of the inputs. This dynamic ZCD is used to implement a pipelined ADC in 0.18 um CMOS. This ADC consumed only dynamic switching power since there are no amplifiers or circuits that required constant bias currents. The ADC achieved 6.4 ENOB at 200 MS/s. The ADC was designed to achieve higher resolution; however, the ENOB of this single-ended implementation of ZCBC was limited by substrate noise injected by the IO drivers due to the single-ended implementation. The resulting figure of merit was 0.5 pJ per step.

3.2.3 Differential Zero-Crossing Based ADC

In the following design, a differential topology is used to improve the circuit's robustness against substrate noise and power supply noise [4]. Dummy transistors are used to improve the high frequency noise rejection. The symmetric dummy structures provide similar capacitive coupling paths to reduce the effects of power supply noise and substrate noise. This ZCB pipelined ADC achieved 10.0 ENOB at 50 MS/s with a figure of merit of 88 fJ per conversion step.

3.2.4 ZCB Sigma Delta ADC

The zero-crossing based circuit was also used in the design of a 4th order sigma delta ADC [5]. The ZCBC technique is applied to implement the integrators used in a 4th order chain-of-resonators feedforward (CRFF) delta-sigma modulator which is shown

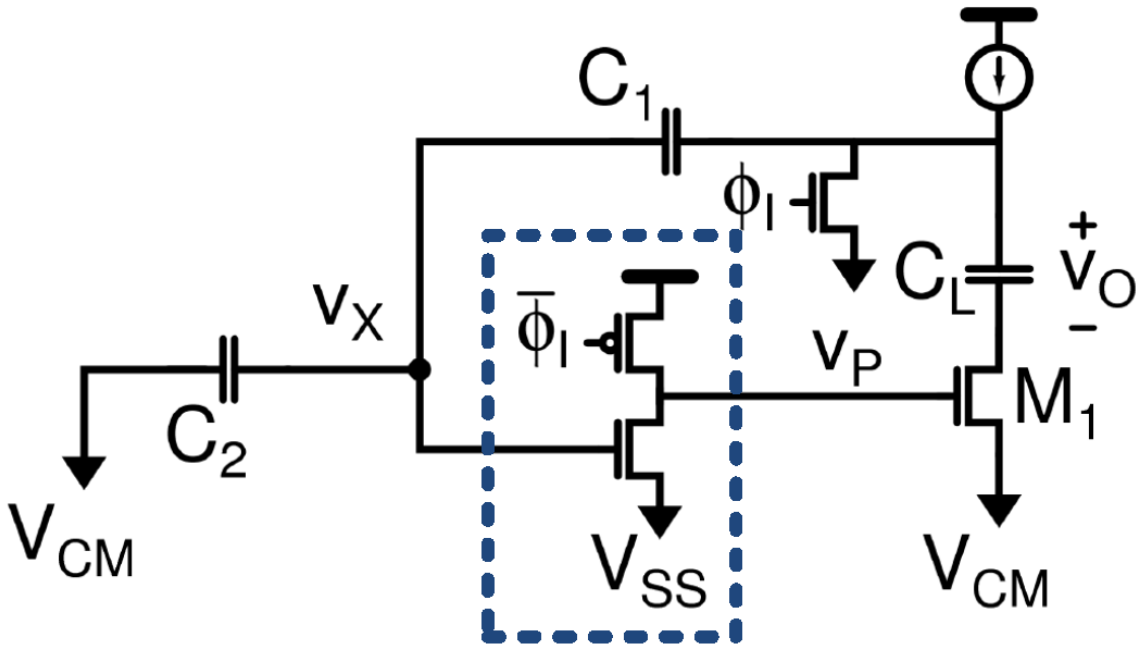


Figure 3-3: Dynamic zero-crossing detector used in the residue amplifier [3]

in Figure 3-5. This work is designed to operate under low power supply voltages without gate boosting. The correlated level-shifting technique is used to increase the effective output impedance of the current sources in order to improve the accuracy of the integrators [18]. The prototype ADC was implemented in 0.13 um CMOS and achieves 11.9 ENOB for 60 kHz input bandwidth while dissipating 1.2 mW power. This is the first work demonstrating the use of zero-crossing based circuits in a sigma delta converter.

3.2.5 Reconfigurable Analog System

One of the advantages of ZCBC is that there are no stability concerns. This is a particularly useful advantage for a reconfigurable analog circuit. In an op-amp based design, if the capacitive loading changes due to reconfiguration, there are stability issues. The output stage of the op-amp may need extra power in order to ensure stability for the worst case loading.

A highly-configurable analog system shown in Figure 3-6 is designed using ZCBC

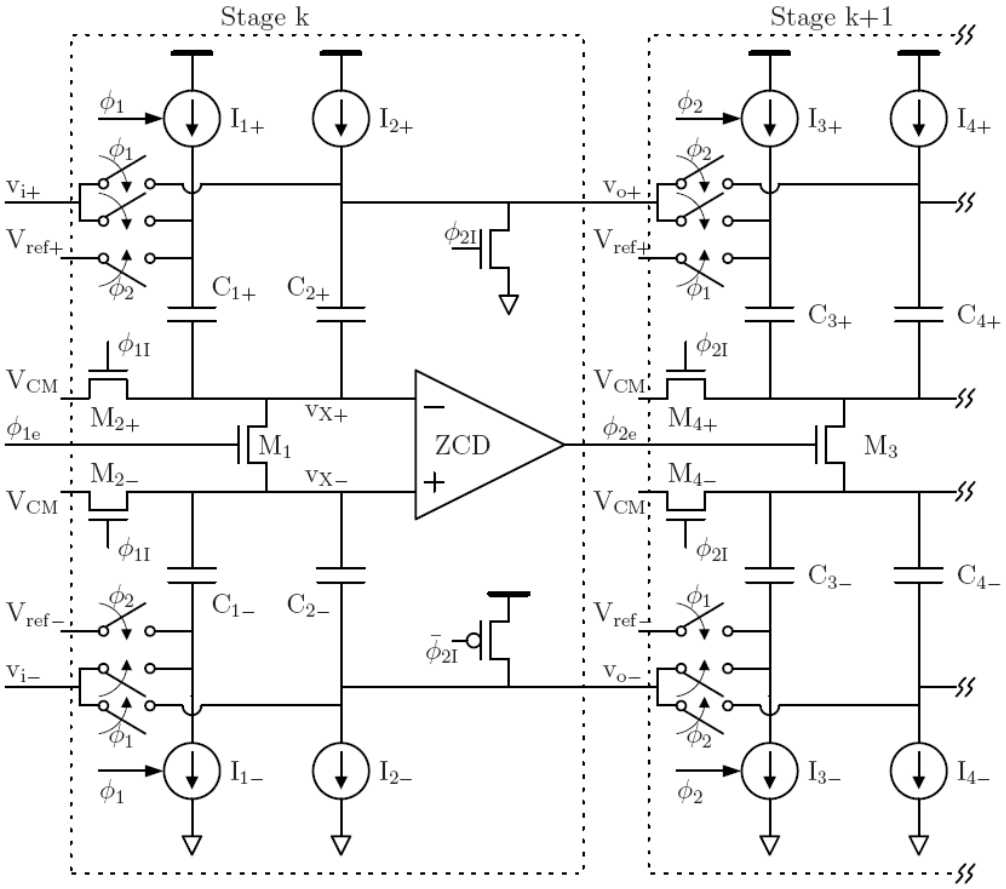


Figure 3-4: First fully differential implementation of the zero-crossing based circuit [4]

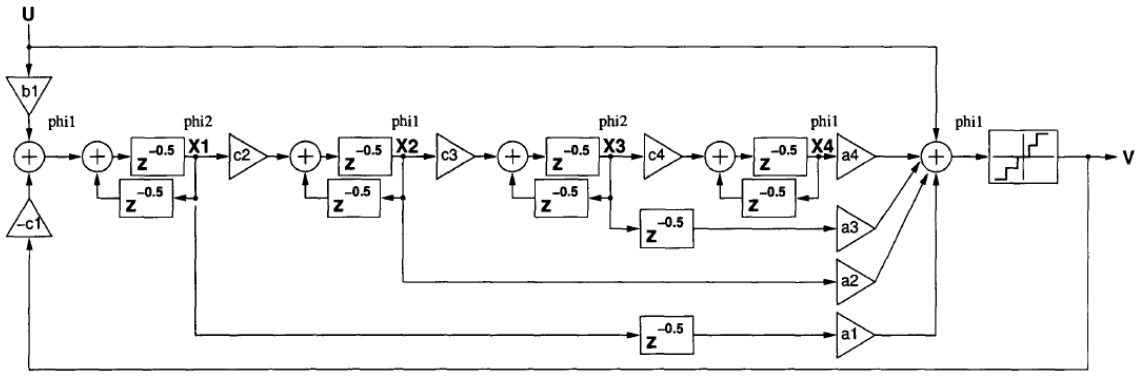


Figure 3-5: A 4th order chain-of-resonators feedforward (CRFF) delta-sigma modulator [5]

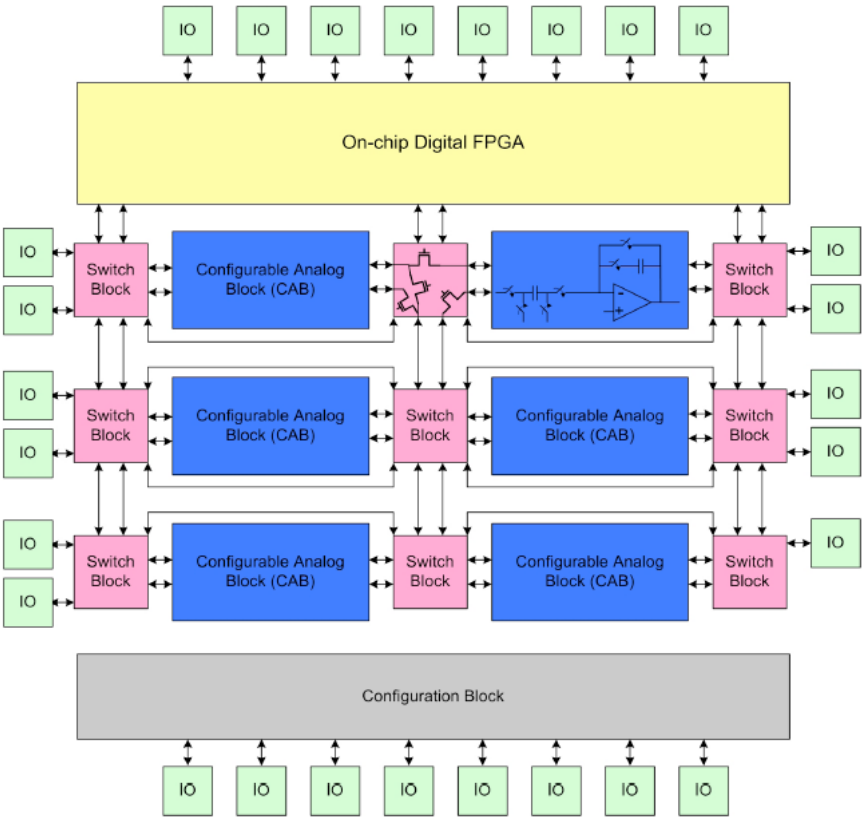


Figure 3-6: Reconfigurable analog FPGA [6]

[6]. This programmable analog circuit can be configured as an ADC, a programmable gain amplifier (PGA), or a filter. In the ADC configuration, a 10-bit pipelined ADC is implemented. The ADC has ENOB of 8 bits at 50 MSPS and has an FOM of 150fJ/conversion-step. In the filter mode, the chip can be configured as a second order Butterworth filter or a third order Butterworth filter. The desired filter responses are demonstrated in both configurations.

3.2.6 Hybrid Op-amp and ZCBC design

A hybrid ZCBC and op-amp based circuit has also been introduced [7]. Zero-crossing based circuits and an op-amp is combined in a two phase charge transfer operation. The combined structure, shown in Figure 3-7, is used in a pipelined ADC to transfer the residue voltage from one stage to another. During the first phase, the zero-crossing circuit is used to charge the output node to a voltage close to the final value.

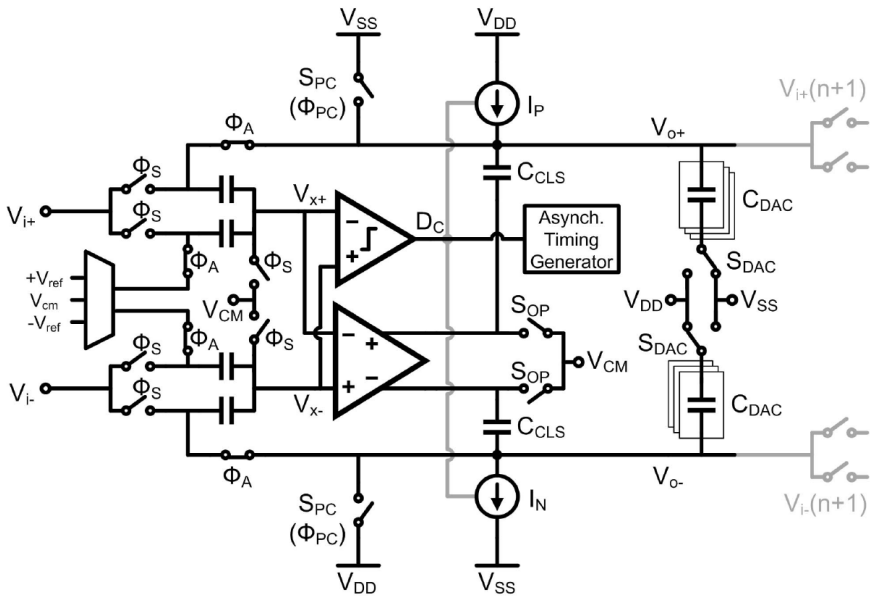


Figure 3-7: Hybrid CLS-opamp/ZCBC residue amplifier [7]

In the second phase, an op-amp drives the output node to its final value through a level shifting capacitor. The correlated level shifting technique is applied to greatly enhance the accuracy of the circuit [18]. The level shifting capacitor isolates the DC level of the op-amp output from the output node; thus, only a limited output swing is required for the op-amp. Thus, a power efficient telescopic op-amp was used. This ADC achieved higher than 11 ENOBs while sampling at 20 MS/s.

3.3 Summary

There have been many recent publications of zero-crossing based circuits. Although there are many new design challenges, ZCBCs have shown potential as a promising new circuit architecture that could revolutionize the way switched-capacitor circuits are designed in the future. Especially in scale technology nodes, this new structure has potential to achieve high resolution and high sampling rates with very good figure of merits.

Chapter 4

Zero-Crossing Based Circuit's Linearity and Noise Limitations

In the traditional op-amp based switched-capacitor circuit design, the accuracy is limited by capacitor matching and the op-amp gain. The operating speed is limited by the op-amp's settling time. In ZCBC, since the capacitor array used is unchanged, the capacitor matching requirement is the same. However, the accuracy of the system no longer depends on the loop gain of a closed loop system. There is a new set of design constraints that determines the accuracy of the zero-crossing based switched-capacitor circuits that is discussed in this chapter.

4.1 The Overshoot Voltage

In a switch capacitor gain stage shown in Figure 4-1, the accuracy of the charge transfer operation is directly related to the final voltage on the V_X node. The charge transfer is perfectly accurate if the potential of the V_X node is exactly equal to V_{CM} at the sampling instant. In ZCBC, a zero-crossing detector is used to detect this virtual ground condition. However, the zero-crossing detector has finite delay. As a result, the final value overshoots the ideal output value. The overshoot voltage is shown as V_{OS} in Figure 4-1. The delay of the ZCD is labeled as t_{delay}. The delay of the zero-crossing detector causes V_X to overshoot V_{CM} and causes the output voltage

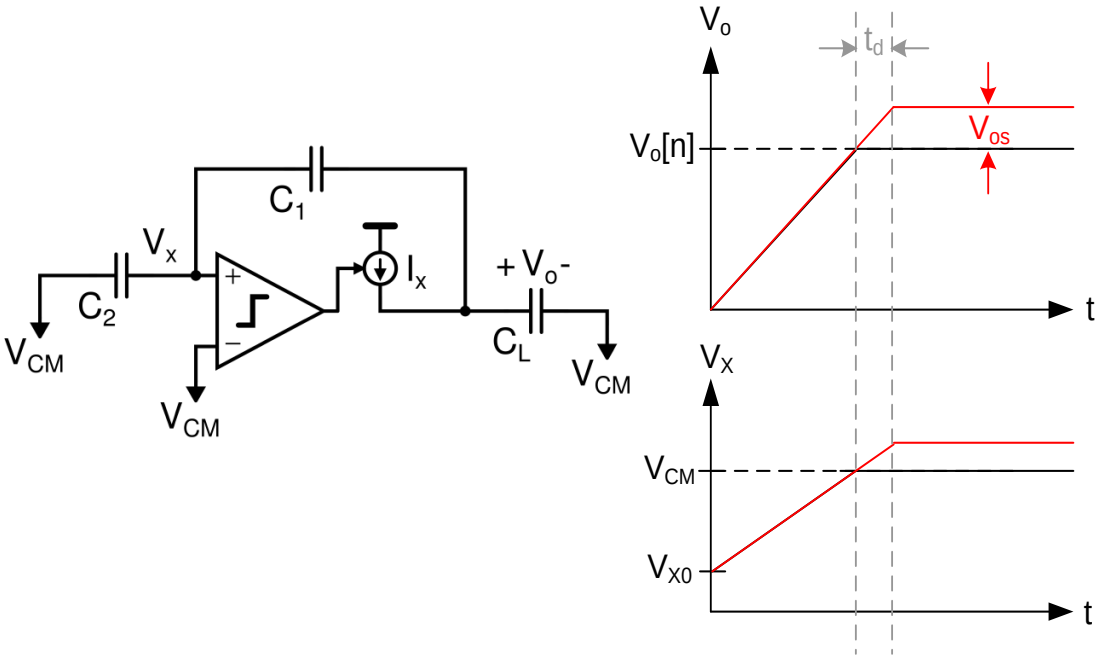


Figure 4-1: The overshoot voltage

to overshoot the ideal value. The overshoot voltage is described by Equation 4.1. The overshoot voltage is equal to the product between the delay of the ZCD and the ramp rate.

$$V_{overshoot} = t_{delay} \cdot \frac{dV}{dt} \tag{4.1}$$

To the first order, the ZCD delay is approximately constant and does not depend on the input ramp rate [2]. Thus, the overshoot voltage is constant if the ramp slope is constant. However, due to finite output resistance and non-linear parasitic junction capacitance, the ramp slope is not constant. The variation in the ramp rate causes the amount of overshoot to vary. This ultimately causes the Differential Non-Linearity

(DNL) and Integral Non-Linearity (INL) in an ADC.

The constant part of the overshoot adds offset to the ADC. This offset can be canceled out in the analog domain or removed digitally [19–21]. The input referred variation of the overshoot voltage should be limited to less than $\frac{1}{2}$ LSB to gurantee that the INL of the ADC will be less than 1 LSB.

4.1.1 Ramp Non-Linearity

In ZCBC, the output ramp is typically generated by charging a capacitor with a constant current source. The ramp rate is given by the Equation 4.2. I is the current from the current source and C_T is the total capacitance at the output node. Finite output resistance of the transistors causes the current source to vary while parasitic junction capacitance of transistors causes the load capacitance to vary. The finite resistance of the current sources and the non-linear junction capacitance both contribute to the non-linearity of the ramp.

$$Ramp\ rate \quad = \quad \frac{I}{C_T} \tag{4.2}$$

For a current source, its current value can be modeled by

$$I_{DS} \quad = \quad I_o(1 + \lambda V_{DS}), \tag{4.3}$$

where I_o is the nominal current value and λ models the finite output resistance of the current source. By Equation 4.3, the variation in the current value is given by $I_o \lambda V_{DS}$.

The total load capacitance, C_T, also varies with the output voltage due to the transistors' PN junctions between the drain nodes and the body node. For example, in a PMOS, the drain node is p-type while the body is n-type. This reverse biased junction has depletion capacitance which varies with the bias voltage. As the reverse

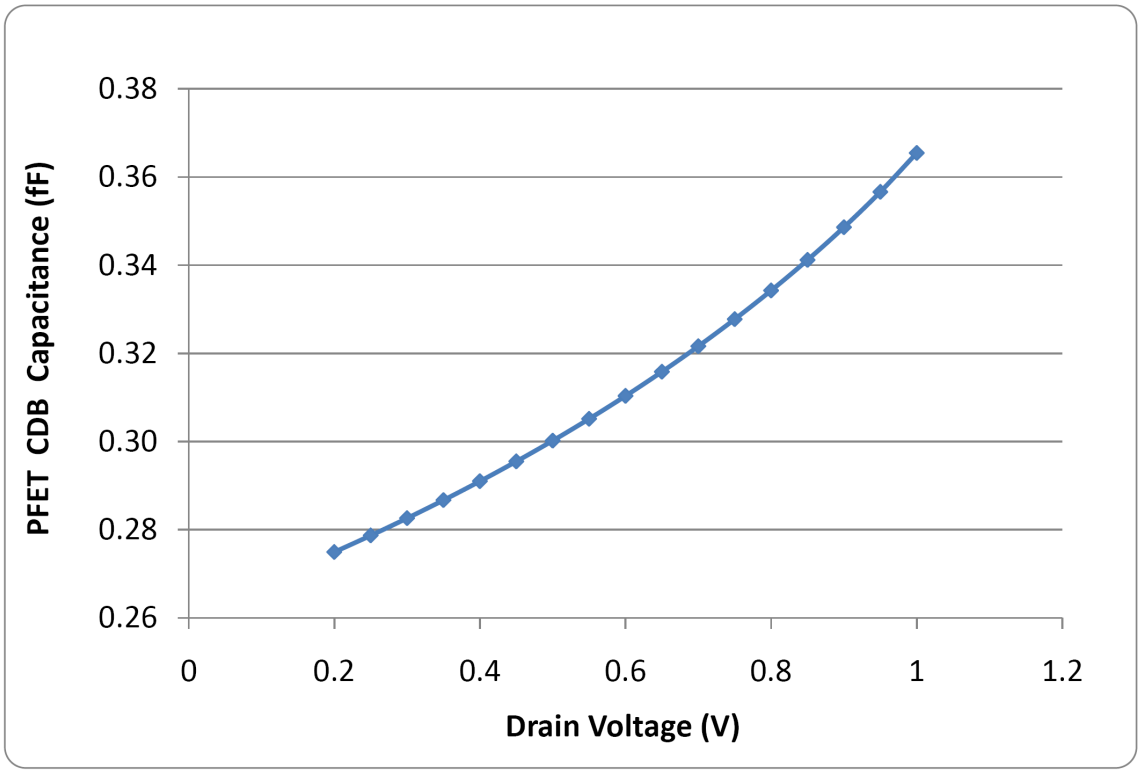


Figure 4-2: C_{db} of a 1 μm wide PMOS vs drain voltage

bias voltage across the junction increases , the depletion width increases and reduces the value of the junction capacitance. However, the change in the depletion width is a non-linear function of the reverse bias voltage. The non-linear change in capacitance adds non-linearity to the ramp rate.

For a 1 μm wide PMOS device, the junction capacitance as a function of Vout is plotted in 4-2. The junction 1 μm wide NMOS device is plotted in 4-3. The parasitic capacitance from the transistors adds non-linearity to the total load capacitance C_T.

In a typical design, it is advantageous to include dummy transistors of the opposite polarity so that the junction capacitance variation is partially canceled. Although the two parasitic capacitors won't cancel out perfectly, the combination of the NMOS and PMOS junctions will have less variation in its junction capacitance. The combined parasitic C_{db} of the NMOS and the PMOS is plotted in Figure 4-4.

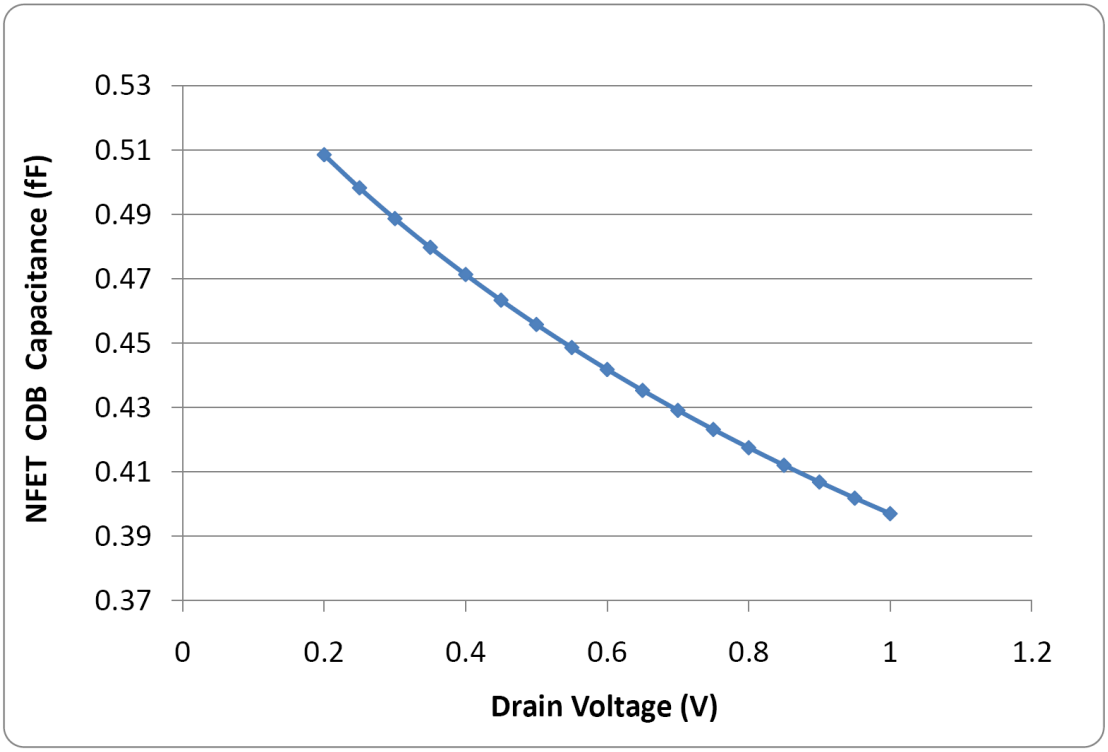


Figure 4-3: C_{db} of a 1 μm wide NMOS vs drain voltage

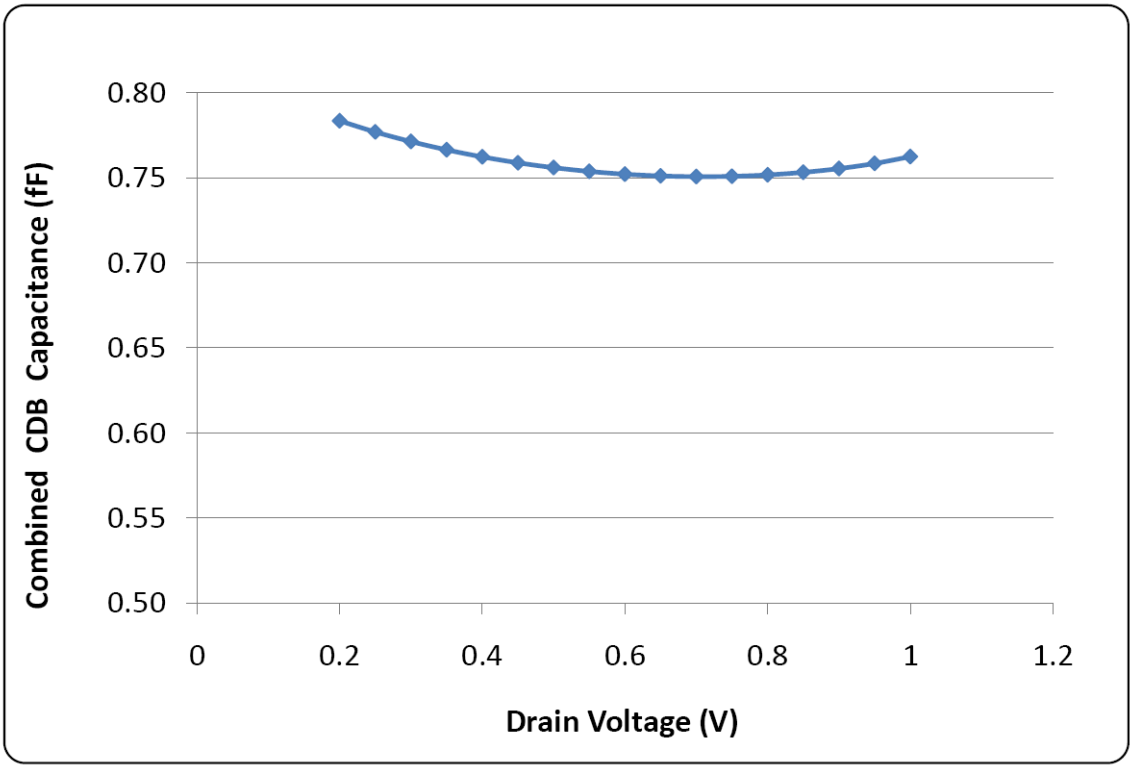


Figure 4-4: C_{db} of a 1 μm wide NMOS and a 1 μm wide PMOS

4.1.2 ZCBC Linearity Calculation

Given the operating speed, the ZCD delay, and the accuracy requirement, the required linearity of the ramp can be calculated. The overshoot voltage is given by Equation 4.1. The average ramp rate $\overline{\frac{dV}{dt}}$ is determined by the maximum output voltage V_{max} divided by the time alloted to the charge transfer. However, as the output voltage increases, the ramp rate decreases due to the finite output resistance of the current sources and the parasitic junction capacitance. The difference in the ramp rate between when V_{out} is at the minimum output voltage and when V_{out} reaches the maximum output voltage can be expressed as

$$\Delta\frac{dV}{dt} = \frac{dV}{dt}\Big|_{V_{out}=V_{max}} - \frac{dV}{dt}\Big|_{V_{out}=V_{min}} \tag{4.4}$$

where V_{max} is the maximum output voltage and V_{min} is the minimum output voltage. For the purpose of this analysis, lets define α as the ratio between $\Delta\frac{dV}{dt}$ and $\overline{\frac{dV}{dt}}$. This α parameter models the variation in the ramp rate.

$$\alpha = \frac{\Delta\frac{dV}{dt}}{\overline{\frac{dV}{dt}}} \tag{4.5}$$

The variation in the overshoot voltage causes an voltage error; this error voltage is equal to the product of the delay of $\Delta\frac{dV}{dt}$ and the ZCD delay , which can be appoximated by its open circuit time constant τ [2].

$$V_{error} = t_{delay}\Delta\frac{dV}{dt} \tag{4.6}$$

$$= \tau\alpha\overline{\frac{dV}{dt}} \tag{4.7}$$

As an calculation example, we can set the sampling rate to 100 MS/s; The feedback factor β is set to 1/2 and the ZCD delay is designed to be 200 ps. If the maximum

output voltage is 0.8 V and the half clock period is 5 ns, then the required average ramp rate $\overline{\frac{dV}{dt}}$ can be calculated to be 0.16 V per ns. If the input voltage range is 1 V, the LSB size at the 10-bit resolution is given by $\frac{1}{2^{10}}$ which is approximately equal to 1 mV. Given a feedback factor β of 1/2 and a ZCD delay of 200 ps, the required α paramter is equal to 0.03 in order to achieve an V_{error} of 1 mV according to Equation 4.7. This error at the output of the ADC stage can be referred back to the input by dividing it by $\frac{1}{\beta}$, and the resulting error voltage is equal to 500 μV which is approximately the size of a $\frac{1}{2}$ LSB.

4.2 Capacitor Matching Requirements

Zero-crossing based pipelined ADCs use the same capacitor arrays as the traditional op-amp based pipelined ADCs. Thus, the capacitor matching requirement for ZCBC is the same as the requirements for an op-amp based switched-capacitor circuits. In the ADC's capacitor array, the individual capacitors must match to certain accuracy to ensure the ADC's linearity performance. The matching requirement depends on the target resolution of the ADC, the total capacitance value, and the resolutions of the first stage of the pipeline. The differential nonlinearity (DNL) caused by capacitor mismatch can be shown to be

$$DNL = \frac{\Delta C_i 2^N}{C_{total}}, \tag{4.8}$$

where ΔC_i is the error of each individual capacitor in the first stage, C_{total} is the total capacitance of the first stage, and N is the resolution of the entire ADC [22]. If we assume that the matching of the capacitor improves with the square root of the capacitance value, the DNL can be minimized by increasing the size of C_{total}. However, a bigger C_{total} will cost more power and area. The settling time-constant of an op-amp based switched-capacitor circuit is proportional to the unity gain frequency of the amplifier, which is proportional to the load capacitance. Thus, to maintain the

speed of operation, if C_{total} increased, power must also be increased proportionally to maintain the unity gain frequency.

Another way to minimize the DNL contribution due to capacitor mismatch is use a large resolution for the first ADC stage. The value of the unit capacitor C_i for each stage is equal to $\frac{C_{total}}{2^m}$, where m is the resolution of the ADC stage. The value of the variation of each unit capacitor, ΔC_i, can be made smaller if m is increased. This is because ΔC_i is proportional to the product between the capacitance value and the variation percentage [22]. As each C_i is made smaller, the capacitance value is reduced linearly while the variation percentage increases with the square root of $\frac{1}{\sqrt{C_i}}$; thus ΔC_i is proportional to $\sqrt{C_i}$ and reduces as the value of C_i becomes smaller. It is very typical to use 3-bit, 4-bit, or even 5-bit resolution for the first stage designs in high resolution pipelined ADC [22–24]. The disadvantage of using a high resolution first stage is that more comparators are needed in the flash ADC. The total number of comparators required is 2^m. In addition, the flash ADC's comparator offset tolerance margin is reduced by $2^{(m-1)}$ compared to the 1 bit per stage design because the decision levels are closer.

The layout of the capacitor array is also very important. Any mismatch in the metal routing may lead to unwanted parastic capacitance. In general, each capacitor in the array should be made so that the surrounding environment is identical. Dummy capacitors around the outer edge is important for elminating any edge effects. There are other layout techniques to enhance the matching of the capacitors arrays [23].

4.3 ZCB Noise Analysis

Since transistors generate flicker and thermal noise, their effects must be taken into account when designing a circuit. The effects of noise in a zero-crossing based switch capacitor circuit are discussed in this section. The current source, switches, and the zero-crossing detector all contribute noise to the system. The zero-crossing detector has been shown to be the dominant noise source [2, 25].

4.3.1 Current Source Noise

Current sources used in zero-crossing based circuits generate noise at all times when they are on. However, they only contribute noise to the sampled output voltage in a specific window of time. Before the zero-crossing detector trips, the noise added by the current sources does not affect the final voltage sampled. This is because the any charge added before the zero-crossing does not affect the total charge sampled after the zero-crossing detection. The current sources only contribute noise during the delay time of the zero-crossing detector after the zero-crossing point [25]. The amount of noise added by the current source follow a random walk pattern [25]. The noise contribution from the current source has been shown to be insignificant compared to the ZCD noise in ZCBC [3, 4, 9].

4.3.2 Zero-crossing Detector Noise

The dominant noise source for zero-crossing based circuits has been shown to be the zero-crossing detector [2,25]. The thermal noise of the ZCD contributes to the timing jitter and changes the sampling time. The error in the sampling time translates to a voltage error that is sampled. For a zero-crossing detector with high bandwidth, the traditional steady state noise analysis can be applied [2] because the dynamics of the zero-crossing detector has settled during the zero-crossing instant. For zero-crossing detectors with low bandwidth, transient noise analysis must be used to determine the noise contribution [25].

The zero-crossing detector noise contributions will be discussed here to show the noise calculations. Figure 4-5 shows the circuit level implementation of the zero-crossing detector. The noise contributed from the differential pair is the dominant noise source. The input referred noise spectral density of the differential pair is given by Equation 4.9.

$$Noise\ Spectral\ Density = 4kT\gamma\frac{gm_1 + gm_2 + gm_3 + gm_4}{{gm_1}^2} \tag{4.9}$$

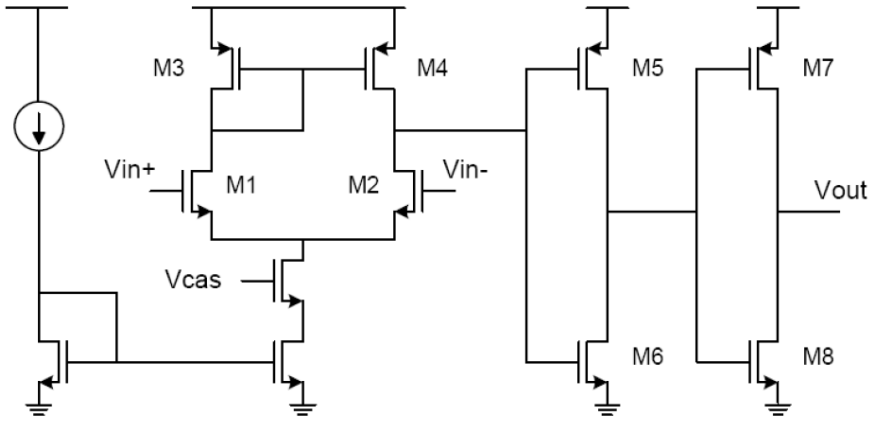


Figure 4-5: Zero-crossing detector implementation

Since the differential pair is symmetric, gm_1 is equal to gm_2 and gm_3 is equal to gm_4. The transconductance of the input pair , gm_1, should be designed to be bigger than gm_3 to minimize the input referred noise.

The noise bandwidth is set by the bandwidth of the differential pair. The effective noise bandwidth can be expressed as

$$\begin{aligned} \textit{Noise Bandwidth} &= \frac{1}{R_{out}C_{eff}} \cdot \frac{1}{2\pi} \cdot \frac{\pi}{2} \\ &= \frac{1}{4R_{out}C_{eff}}, \end{aligned} \tag{4.10}$$

where R_{out} is the output resistance of the differential pair and C_{eff} is the effective capacitance at the output of the differential pair. The factor of $\frac{1}{2\pi}$ converts Radians to Hertz and the factor of $\frac{\pi}{2}$ is the bandwidth adjustment factor which takes into account the fact that some noise exists beyond the 3 dB frequency [15]. The noise power can be calculated by taking the product between the noise bandwidth and the noise spectral density.

The transistors M5-M8 also add noise, but their contribution is much smaller to the overall input referred noise. The gain of the differential pair greatly reduces their input referred noise. At the zero-crossing instant, M5 and M6 are both in saturation

and the inverter stage can be modeled as a single pole amplifier. The noise spectral density of M5 and M6 is given by Equation 4.11 and the noise bandwidth is given by equation 4.12. R_{out2} is the output resistance of inverter made by M5 and M6; and C_{eff2} is the effective load capacitance of the inverter. The noise added can be calculated by taking the product between the noise bandwidth and the noise spectral density.

$$Noise\ Spectral\ Density = 4kT\gamma \frac{gm_5 + gm_6}{(gm_5 + gm_6)^2} \tag{4.11}$$

$$\begin{aligned} Noise\ Bandwidth &= \frac{1}{R_{out2}C_{eff2}} \cdot \frac{1}{2\pi} \cdot \frac{\pi}{2} \\ &= \frac{1}{4R_{out2}C_{eff2}}, \end{aligned} \tag{4.12}$$

The exact values for the noise added by M5 and M6 is design dependent. In this design, M5 is sized to be 20x larger compared to M6 in order to minimize the delay of the ZCD. The transconductance of M5 is much larger compared to that of M6; According to Equation 4.11, the noise contribution of the inverter stage is dominated by M5. In this design, the transconductance of M5 during the zero-crossing instant is approximately 3 times smaller compared to the transconductance of the first stage. Thus according to Equations 4.9 and 4.11, the noise spectral density of inverter stage is comparable to that of the differential pair. The noise bandwidth is also similar in this design. The noise power generated by M5 and M6 may be comparable to that of the differential pair; however, when referred to the input, the noise power of this inverter stage is divided by A^2 where A is the gain of the differential pair. In this differential pair design, A is approximately 15 and A^2 is approximately 225. Thus, the input referred noise contributed by M5 and M6 is negligible compared to that of the differential pair.

4.4 ZCD Noise Compared With Op-amp Noise

For a given accuracy requirement,the required bandwidths for the ZCD and op-amp are different and they are determined by two different sets of equations. In addition, the required bandwidth for the ZCD depends on the number of ramps used in the ZCBC operation [1]. The analysis presented will describe the single ramp ZCBC.

4.4.1 Bandwidth Requirement for ZCBC

In ZCBC, the accuracy of the charge transfer operation is limited by the variation in the overshoot voltage, which is caused by the non-linearity of the ramp rate. The required open loop time constant τ of the ZCD preamplifier for a given accuracy is given by Equation 4.7. The corresponding 3-dB bandwidth of the ZCD is given by $\frac{1}{2\pi}\frac{1}{\tau}$.

For the zero-crossing detector, the operation is open-loop. Thus, the noise bandwidth is set by the 3-dB bandwidth of the input stage. In addition, the noise is dominated by first stage of the zero-crossing detector as shown in the previous section.

4.4.2 Bandwidth Requirement for Op-amp Based Switched-Capacitor Circuits

For the op-amp based switched-capacitor circuit, the finite gain of the op-amp and the settling time both contribute to the error voltage. The finite gain error term can be shown to be be $\frac{1}{1+A\beta}$ where β is the feedback factor of the switch-capacitor circuit. The settling error is proportional to $e^{-T/\tau}$, where T is the amount of time allowed for settling, which is typically half of the clock period, and τ can be approximated by $\frac{1}{\beta\omega_u}$, where ω_u is the unity gain frequency of the op-amp [16]. The total error budget should be divided between the error due to finite gain and the error due to settling. The maximum settling error can be decribed by Equation 4.13,

$$V_{error} = V_R e^{-T/\tau} \tag{4.13}$$

where V_R is size of the output range which is given by $V_{out,max} - V_{out,min}$. V_R is determined based on the residue scheme used in the pipelined stage and the head room required for op-amp. The settling time constant τ is set by the closed loop pole in the case when there is only one dominant pole in the op-amp. In this case, τ is equal to $\frac{1}{\beta\omega_u}$ and the noise bandwidth is given by $\frac{1}{2\pi}\frac{1}{\tau}$.

However, in the two-stage op-amp design, the amount of phase margin also affects the settling evelope decay time. The optimal phase margin depends on the accuracy requirement.

4.4.3 An Example Noise Bandwidth Comparison

This section includes a numerical example to compare the bandwidth required for a ZCB circuit compared to an 2-stage op-amp used in a pipelined ADC design. The operating speed is chosen to be 100 MS/s. At this frequency, the half clock period T is 5 nS. With an input range of 1 V, the LSB size is approximately 1 mV at the 10-bit resolution. In this example, the feedback factor β is 1/2. The second pole frequency ω_{p2} of the op-amp is set to 4x of the asymtotic unity gain frequency of the loop transmission. This choice of ω_{p2} allows for approximately 70 degree phase margin. The ramp non-linearity factor α is assumed to be 0.03. The output voltage range V_R is set to 0.4 V. The maximum error voltage should be less than 1 mV so that the input-referred error is less than 1/2 of an LSB.

For the zero-crossing detector, the error voltage is given by Equation 4.7, and thus it follows that the required time constant τ is equal to approximately 200 ps and the bandwidth of the ZCD is given by

$$f_{3dB,ZCD} = \frac{1}{2\pi}\frac{1}{\tau}$$

$$= \quad 800MHz. \tag{4.14}$$

The noise bandwidth of the ZCD is also set by $f_{3dB,ZCD}$.

For the op-amp based design in this example, half of the error budget is allocated to the DC gain error term and half the error budget is allocated to the settling error. Since the maximum allowable error at the output is 1 mV, the DC gain error contribution should not exceed 500 μV. The gain error factor can be shown to be $\frac{1}{1+A\beta}$. The maximum output voltage error due to this term is given by the product between the output voltage range V_R and the gain error factor. In this case, the required DC gain can be calculated to be 1600 from Equation 4.15.

$$\begin{aligned} V_{error,DC} &= V_R \cdot \frac{1}{1+A\beta} \\ &\approx 500\mu V \end{aligned} \tag{4.15}$$

The settling bandwidth requirement can be computed using Equation 4.13. The required settling time constant τ is approximately equal to $\frac{T}{6.7}$. The settling error can be written as

$$\begin{aligned} V_{error,settling} &= V_R \cdot e^{-T/\tau} \\ &= V_R \cdot e^{-6.7} \\ &\approx 500\mu V. \end{aligned} \tag{4.16}$$

Thus, the combined error term is approximately 1 mV. In this case, when the second pole frequency ω_{p2} of the op-amp is set to 4x of the asymtotic unity gain frequency of the loop transmission, the settling time is close to that of a single pole amplifier. The closed-loop bandwidth required in this case is given by

$$
\begin{aligned}
f_{3dB,opamp} &= \frac{1}{2\pi}\frac{1}{\tau} \\
&= \frac{1}{2\pi}\frac{6.7}{T} \\
&= 213MHz
\end{aligned} \tag{4.17}
$$

In this example, the noise bandwidth of the single-phase ZCBC is larger by a approximately 3.75x, there are some other factors that must be accounted for. First, the 2-stage op-amp uses about twice the power because the 2nd stage of the op-amp consumes the same amount of power as the first stage. The second stage of the zero-crossing based circuit does not consume any DC power and only draws a small amount of dynamic power when switching. In addition, ZCBC is open-loop. Thus, the noise of the second stage in ZCBC is neglible when input referred. However, based on the equations given in section 2.3 of Chapter 2, the second stage of the op-amp's noise contribution is 1.75x compared to that of the first stage noise. Thus, the total power efficiency of the op-amp is approximately 1.5x worse compared to the single-phase ZCBC when the circuits are noise limited.

For a dual-slope ZCB design, the ramp rate of the second slope can be made to be much lower compared to the first phase. If we assume that the delay of the ZCD remains unchanged, the overshoot voltage, which is proportional to the ramp rate, will be much smaller. For example, if the rate rate in the second phase is lower by a factor of 5 compared to the ramp rate in the single slope ZCB design, then according to Equation 4.7, the delay of the zero-crossing detector can be 5 times as long as the delay required in the single slope ZCB design to maintain the same linearity. Thus, in this case, the ZCD pre-amp's bandwidth requirement can be reduced by a factor of 5. If we maintain the same amount of power while lowering the bandwidth, the noise contribution of the ZCD can be lower by a factor of 5. In this case, the total power efficiency of the 2-stage op-amp is 7.5x worse compared to the dual-slope ZCBC when the circuits are noise limited.

4.5 Summary

Another consideration is that it may be much more difficult to design the op-amp which requires high gain and high bandwidth. In addition, the op-amp's feedback loop must be stable and must have sufficient phase to achieve a good settling time. The differential amplifier used in the ZCD will perform the zero-crossing detection well with a relatively low gain and additional gain can be easily achieved by cascading more gain stages. There are no stability concerns in ZCBC because the circuit is open-loop. In addition, the op-amp must drive the load capacitor which makes it costly in power to achieve high bandwidth when the load capacitance is large. In contrast, the ZCD only needs to drive the sampling switch of the load capacitor which has much less capacitance compared to the load capacitor itself.

Chapter 5

High Performance Differential Zero-Crossing Based ADC

In this work, a high performance zero-crossing based pipelined ADC is developed [3]. To improve its robustness against power supply and substrate noise, a differential topology is used. Using a differential structure increases the input signal range by a factor of two while the power consumption is increased by less than a factor of two since many circuit blocks are shared. The signal power is increased by a factor of 4 while the sampling noise power, which is equal to $\frac{kT}{C}$, is only increased by a factor of 2. In addition, the op-amp's noise is essentially unchanged if a differential pair is also used in the single-ended implementation. Thus, using a differential structure greatly improves the overall power efficiency of the ADC. The ADC uses a multi-bit 1st stage to improve the pipelined ADC's overall power efficiency [22].The ADC consists of 6 pipelined stages with digital error correction. The nominal resolution of the ADC is: 3+2+2+2+2+2 = 13 b.

5.1 Circuit Topology and Operation

The ZCB pipelined ADC stage has the same switched-capacitor array as conventional pipelined ADCs. Figure 5-1 shows a simplified schematic of a ZCB pipelined ADC stage. The timing diagram for the sampling phase and charge transfer phase is shown

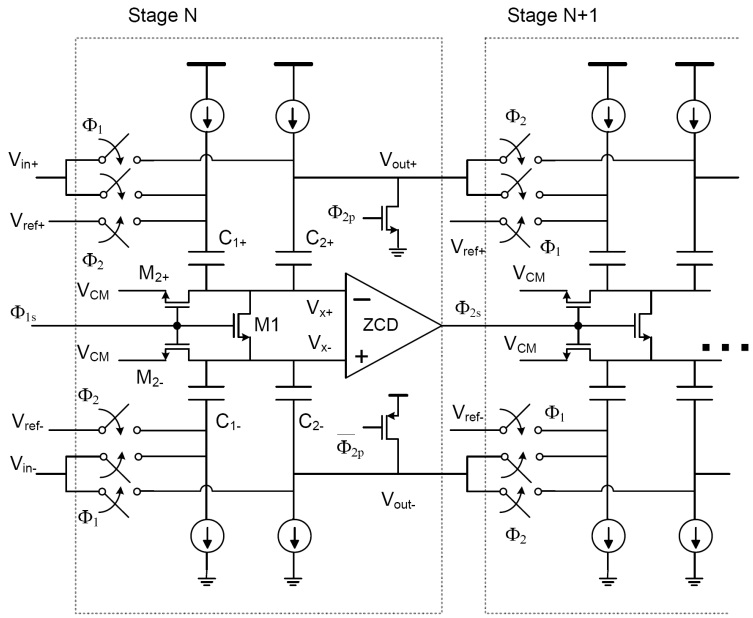


Figure 5-1: ZCB pipelined ADC stage

in Figure 5-2. During the sampling phase, the input signal is sampled differentially across C1 and C2 . Bottom plate sampling is used to minimize the amount of signal dependent charge injection. During the charge transfer phase Φ_2, the residue charge is transferred onto the sampling capacitors of the next stage. At the start of Φ_2, a brief preset phase resets the initial conditions. As the current sources charge the output capacitors, the V_{x+} and V_{x-} nodes ramp in opposite directions as shown in Figure 5-2. The ZCD detects the zero-crossing when V_{x+} equals V_{x-} and locks in the charge on the output capacitors by turning off the sampling switch, completing the charge transfer. The current sources are then turned off.

5.1.1 Residue of the Pipelined ADC Stages

In a pipelined ADC, component matching requirements and other design requirements of the later stages are significantly reduced by using a multi-bit MDAC in the first stage. A bigger gain factor in the first stage helps to reduce the capacitor matching requirements [22]. As shown in Figure 5-1, the gain factor in the pipelined stage is set by the ratio of $\frac{C_1+C_2}{C_2}$. As explained in Section 4.2,a bigger gain factor in the first

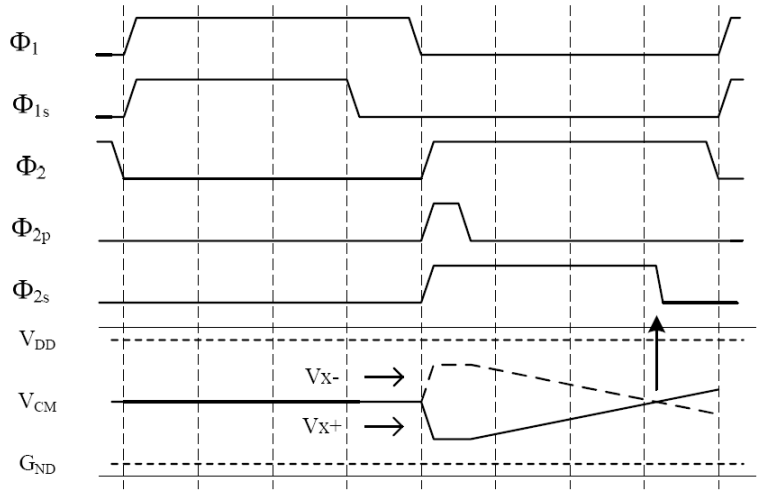


Figure 5-2: ZCB pipelined stage timing diagram

stage will reduce the amount of DNL and INL.

In this design, the first stage resolves 3.3 bits by using 9 bit-decision comparators. The first stage gain factor is 4. This residue scheme is demonstrated in a previous work [2]. The residue of the first stage is shown in Figure 5-3. The ADC uses a 1.2 V power supply and the ground potential is 0 V. By using a differential implementation, the input range of +1 V to -1 V is achieved. The differential output voltage range is limited between +0.4 V and -0.4 V. On each side of the differential structure, the output range is limited between 0.4 V to 0.8 V.

The relationship between the stage's gain factor K, the input range, the number of comparators N, and the output range is given by Equation 5.1.

$$(Output\ Range)\,(N+1) = K\,(Input\ Range) \tag{5.1}$$

In this design, 9 comparators are used in the first stage. By using a large number of comparators, it helps to limit the output range for a given gain factor and input range. A limited output range is desirable since it reduces the voltage dependent non-linearity. For example, the current source variation is smaller if the output voltage is restricted to a narrow range. Also, for a fixed output range, the input range can be

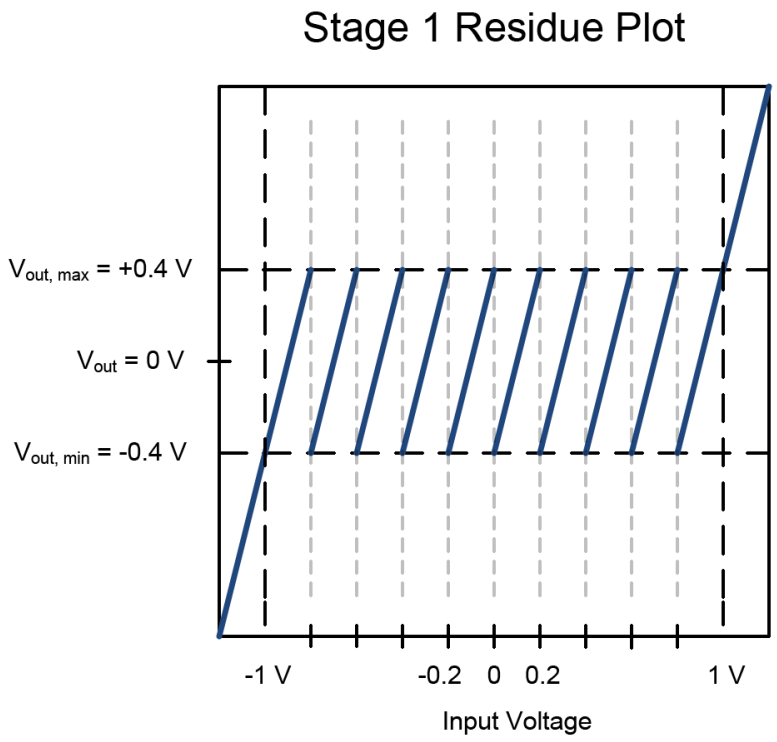


Figure 5-3: Residue plot of the Stage 1

expanded according to Equation 5.1. A large input range is desirable since it increases the signal power and thus increases the SNR.

Each of the subsequent ADC stages uses five bit-decision comparators. The two bit-decision comparators on the edge are redundant comparators used for over-range detection. The gain factor of the following stages is also 4. This scheme has a limited output range of 0.4 V to 0.8 V. This limited output voltage range helps to improve the current source linearity.

5.1.2 Noise Budget and SNR Calculation

The SNR is an important design parameter in ADC design. The SNR is calculated by applying a full-scale sine wave input signal. The corresponding signal power is $\frac{A^2}{2}$ where A is the amplitude of the sine wave input. The noise component is the combination of the device noise and quantization noise from the ADC. The SNR is the ratio between the signal power and the total input referred noise power.

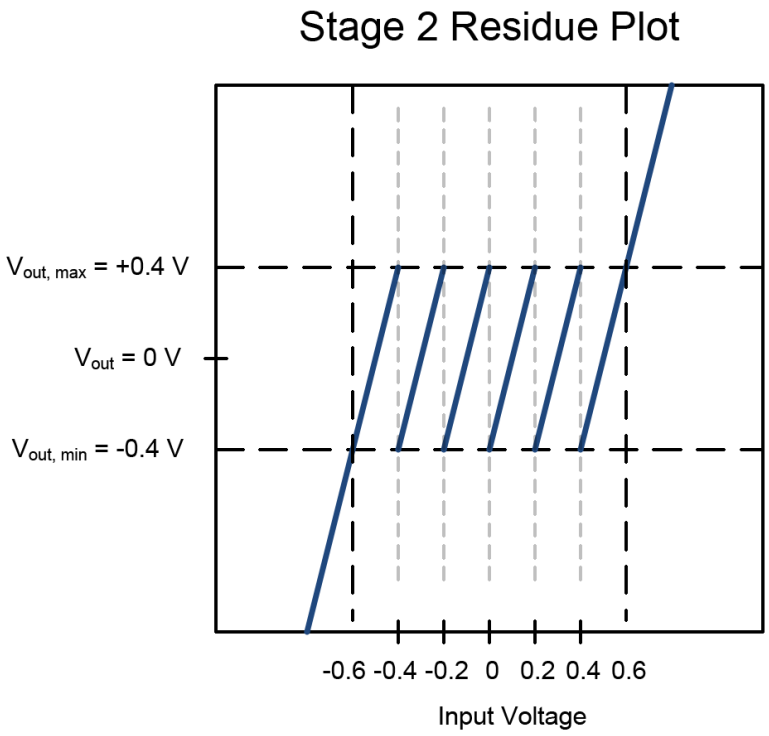


Figure 5-4: Residue plot of the Stage 2

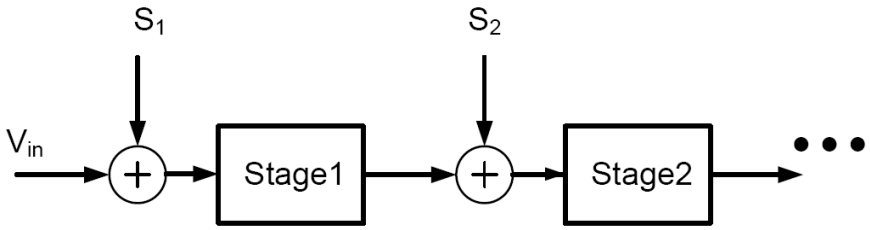


Figure 5-5: Noise contribution from ADC stages

The thermal noise of the ADC stage is dominated by the noise from the ZCD [1, 2, 25]. The noise contribution of the ZCD is described in detail in Chapter 4. The input-referred noise density of ZCD is given by Equation 4.9 and the noise bandwidth is given by Equation 4.10. The total input referred noise power of the ZCD is given by the product between the input-referred noise density and the noise bandwidth.

In addition to the noise from the ZCD, noise is also added from the switch resistance during the sampling operation. The sampled noise power is equal to kT/C where C is the value of the sampling capacitor. In a differential ADC, there are two sets of capacitors that samples the input signal. The sampled noise on each set of capacitors are independent and thus the total noise due to sampling is equal to $\frac{2kT}{C}$, where C is the value of the capacitance on each side.

Since the sampling noise and the ZCD noise are independent, the combined noise power is the sum of the two noise powers. In a pipelined ADC, every stage contributes noise to the output value. The later stages contribute less input-referred noise due to the inter-stage gain. Figure 5-5 shows the model of the pipelined ADC stage. S_i represents the noise power added by stage i of the pipelined ADC. Thus the combined input referred noise power generated by the circuit elements is given by

$$S_{circuits} = \sum_{i=0}^{M-1} \frac{S_i}{K^{2i}}, \tag{5.2}$$

where M is the total number of stages and K is the inter-stage gain. Equation

5.2 assumes that the inter-stage gain K is the same for all of the pipelined stages; if the inter-stage gain is different, then the input referred noise of each stage should be calculated with its own inter-stage gain.

The total input referred noise can be calculated by adding the input referred circuits noise and quantization noise which is given by $\frac{\Delta^2}{12}$ where Δ is the size of the least significant bit (LSB). The SNR of the ADC is given by ratio of signal power to the total input referred noise power.

In this design, 1 pF capacitors are used in the first stage to sample the input on both sides. The resulting differential RMS noise due to sampling is 91 μV. In the first stage ZCD design, the input-referred ZCD noise is limited to approximately 100 μV. The noise of contribution of the ZCD can be calculated using Equations 4.9 and 4.10. Thus, the total noise input-referred noise power of the first stage is given by $(91\mu V)^2 + (100\mu V)^2$.

The second stage and the following stages of the ADC contribute additional noise. The second stage is scaled by exactly a factor of 2 compared to the first stage. The capacitors used are 1/2 of the size of the capacitors in the first stage. Thus, the kT/C sampling noise is increased by a factor of 2. The ZCD size of the second stage is scaled down by 1/2 compared to the first stage ZCD. The transconductance of the input-pair is 1/2 that of the first stage. Since the noise power is inversely proportional to the transconductance, the second stage ZCD's noise power is exactly 2x that of the first stage. The noise added at the input of the second stage is given by $2\,(91\mu V)^2 + 2\,(100\mu V)^2$.

The contributions from each stage can be input-referred. Their sum is calculated using equation 5.2. In this design, the inter-stage gain K is set to 4 in all of the pipelined stages. The LSB size in this design is approximately 244 μV which results from a 2 V differential input range and 13 bit level quantization. The corresponding quantization noise is equal to $(70\mu V)^2$. Thus, the total input referred noise can be calculated to be approximately $(160\mu V)^2$.

In this design, the input range spans from -1 V to 1 V, and thus the signal power is given by $\frac{(1V)^2}{2}$. The SNR is given by

$$
\begin{aligned}
SNR &= \frac{Signal\ Power}{Noise\ power} \\
&= 10 \log \left(\frac{1^2}{2} / (160\mu V)^2 \right) \\
&= 72.9 \text{ dB}.
\end{aligned} \tag{5.3}
$$

The effective number of bits (ENOB) of an ADC is given by

$$
ENOB = \frac{SNDR - 1.76}{6.02}. \tag{5.4}
$$

If we assume that the ADC is limited by SNR, then the ENOB we can achieve is given by $\frac{72.9-1.76}{6.02}$, which is approximately equal to 12 bits.

5.2 Sampling Network

In this design, there is no dedicated front-end sample-and-hold circuit. Instead, the analog signal is sampled passively on two sets of capacitors at the same time, one for the main signal path, and one for the flash ADC of the first stage. The matching of the two sampling paths is important for the dynamic performance of the ADC. Any mismatch between the two paths will reduce the amount of safety range offered by the over-range protection added by the extra comparators.

The front end of the ADC consists of boot-strapped switches and capacitors as shown in Fig. 5-6. The boot-strapped switches reduces the on-resistance of the switches [26]. In addition, they also help to maintain a more constant resistance over the signal range which improves the dynamic linearity. Cross-coupled dummy switches are added to reduce the feed-through from the switches at high frequencies [27].

In this design, bottom plate sampling is used to reduce the effect of signal dependent charge injection [26]. Even with bottom plate sampling, the bottom plate switch's charge injection is still not constant. The top-plate sampling switch resis-

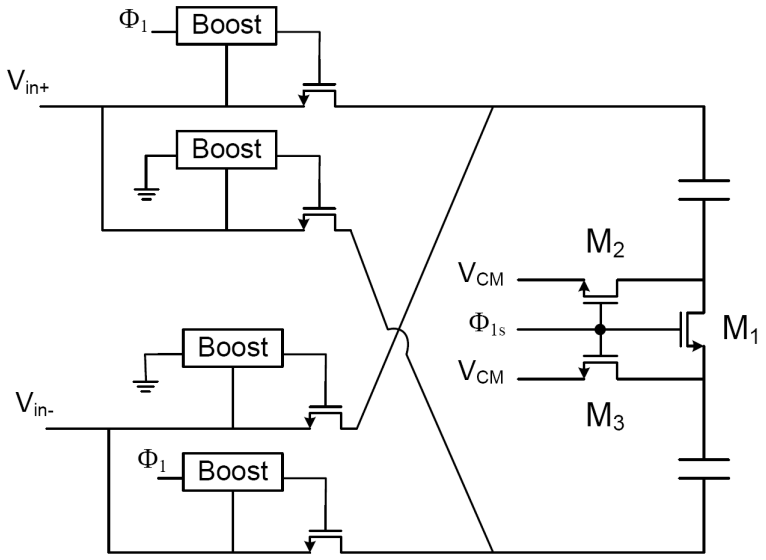


Figure 5-6: Differential sampling network

tance depends on the input voltage due to the body effect. Thus, given a non-zero diferrential input voltage, the on-resistance of the sampling switch will be different and this causes the charge on the bottom plate to distribute unevenly at the sampling instant. In the first stage, the mismatch of the charge injection varies from 0 V for a 0 V differential signal to 70 μV signal for a +1 V differential signal as shown in Figure 5-7. This variation is mostly linear so its effect is to simply scales the input signal by $\frac{1V}{1V+70\mu V}$. The non-linear variation in the charge injection is less than 1μ which is approximately 1/488 of an LSB size at the 12 bit level. The scaling of the input signal by a linear gain of $\frac{1V}{1V+70\mu V}$ does not effect the SNDR.

During the sampling phase, a differential shorting switch M_1, shown in Figure 5-6, connects the bottom plates of the two sampling capacitors [2]. The middle of the channel of the shorting switch can be considered to be virtual ground. Thus, the shorting switch can be represented using two transistors with length L/2, where L is the length of the shorting switch. As a result of using the shorting switch, the effective conductance to the virtual ground node is increased by a factor of 2 compared to using two separate switches to connect to the common mode voltage. In addition,

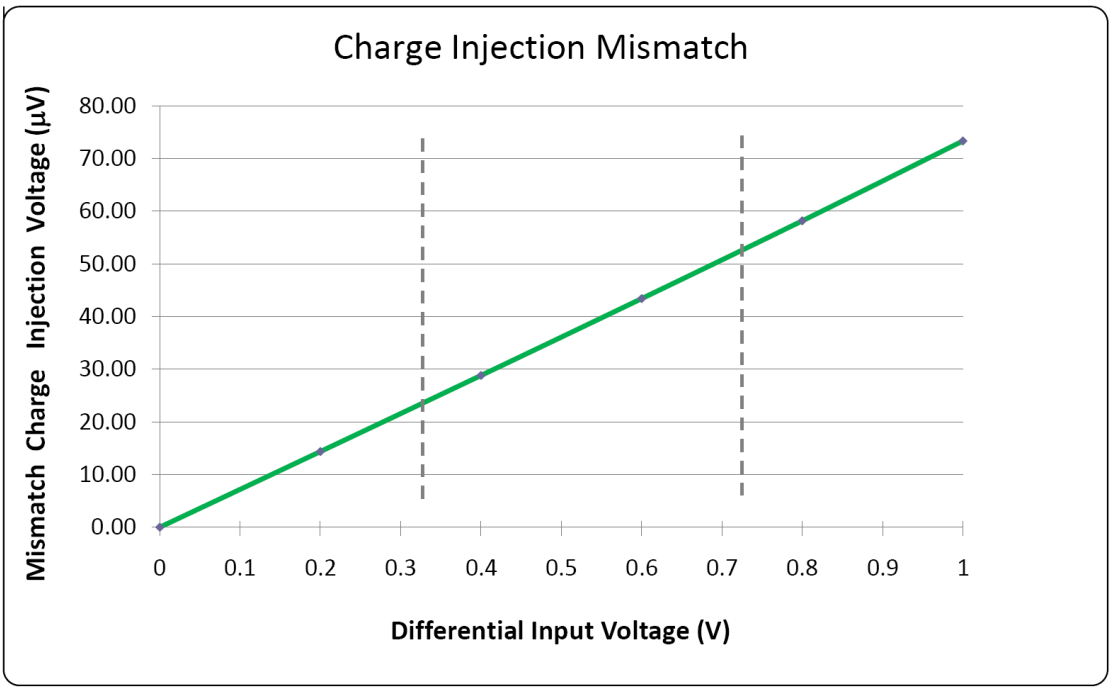


Figure 5-7: Bottom-plate charge injection mismatch

area is reduced by a factor of 2 compared to using two separate switches. In terms of its conductance per area ratio, the shorting switch M_1 is 4 times as efficient as M_2 or M_3. Since charge injection is proportional to the area of the device, charge injection from shorting switch M_1 is 4 times smaller compared to M_2 or M_3 for the same level of conductance.

In Figure 5-6, the two switches M_2 and M_3 connect the bottom plate to the common mode voltage and they are used to prevent the common mode level from drifting away from the desired voltage. The mismatch current between the PMOS current source and the NMOS current source will cause the internal node voltage to drift away from the common mode voltage with time. By adding these two small switches that connect to the common mode voltage, the amount of voltage drift is bounded by the product of the mismatch current and the parallel on-resistance of these two switches. In this design, the shorting switch M_1 is chosen to be 4x bigger than M_2 since it is much more efficient in its conductance to parasitic capacitance ratio.

5.3 Flash ADCs

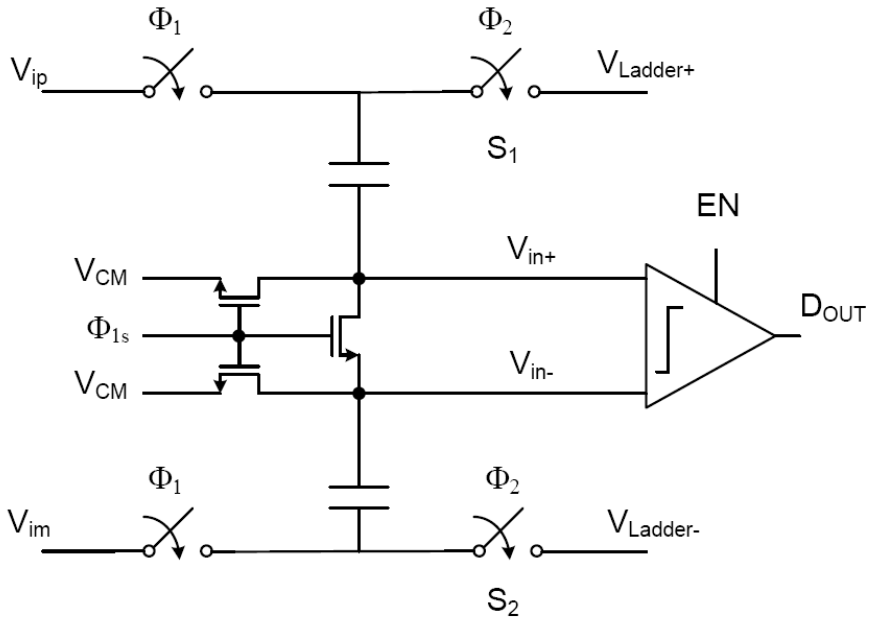
In a pipelined ADC design, a flash ADC is used in each stage to make bit decisions. The bit decisions are used during the charge transfer phase to determine the correct configuration for the DAC. In this pipelined ADC, the structure shown in Fig. 5-8 is used as the flash ADC.

In this design, the input signal is sampled onto capacitors of the flash ADC during the first phase. Once the sampling phase finishes, two reference voltages, which are generated from a resistor ladder, are applied to the top plates of the capacitors. After approximately 100 ps, the latch is enabled and a digital decision is made. The sampling switches and the capacitors in the flash ADC are designed to match the input path to minimize the difference between the flash ADC's input and the actual value sampled. Any mismatch between the flash ADC and the main path will cut into the amount of over range protection gained through using redundant bit decision comparators.

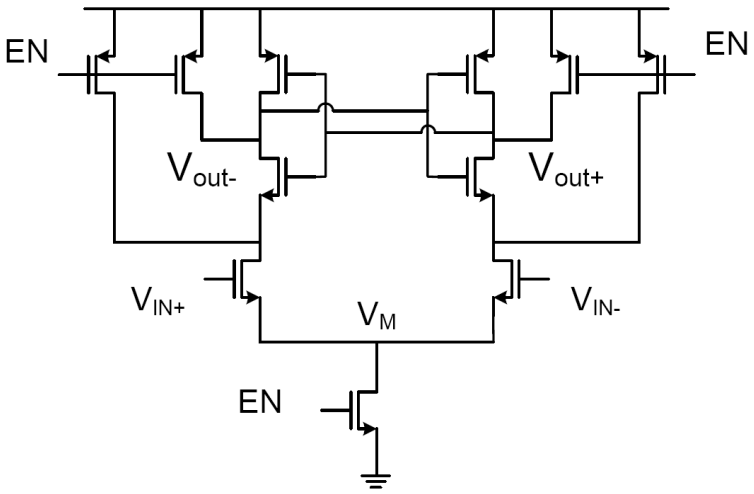
The comparator used in the flash ADC is shown in Fig. 5-8(b). It consists of a differential pair with two cross-coupled inverters. PMOS switches are used to reset the latch. When the enable signal is low, the latch is turned off and the internal nodes are preset to VDD. When the enable signal turns on, depending on which input transistor has a higher gate voltage, the cross-coupled inverters will regenerate in one direction.

The speed of the comparator is directly proportional to the $\frac{gm}{C}$ ratio, where the gm is the effective transconductance of the latch and the C is the parasitic capacitance of the internal latch node [16]. Thus, from a speed perspective, it is desirable to use the minimum channel length in order to minimize capacitance and maximize gm.

However, as the area of the transistor becomes smaller, mismatch increases. Mismatch of the transistors causes offset in the comparator. Although the over-range protection in this design allows for up to 50 mV of offset, the performance of the system will be less than optimal if the offset is large. Large offsets can cause the output voltage to get closer to the supply rails, causing the output resistance of the



(a)



(b)

Figure 5-8: Flash ADC building blocks
(a) Comparator structure used to generate bit decisions. (b) Circuit implementation for the comparator used in Fig. 5-8(a).

current sources to drop.

To improve matching between the devices, the channel length and width is made 25% larger than the minimum size. The increase in area reduces the offset by approximately 25% since the offset is inversely proportional to the square root of the area of the device [28]. The layout of the device is made to be as symmetrical as possible. The simulated RMS offset voltage is less than 1 mV from Monte Carlo simulations. As the offset voltage increases, the decision boundary shifts away from the ideal location and the output voltage will reach beyond the nominal range. When the output voltage is too high or too low, the ramp rate will become very non-linear due to the transistors in the current source falling into the triode region.

After Φ_2 goes high, the enable signal EN rises, and it pulls the middle node, labeled V_M in Figure 5-8(b), towards ground. The rapid voltage change on the V_M node capacitively couples to both input nodes, which are label V_{in+} and V_{in-} in Figures 5-8(a) and 5-8(b). The disturbance of the inputs of the comparator due to the rapid changes in voltage on the internal nodes of the comparator is called kickback. If the on-resistance of the reference switches S_1 and S_2 are mismatched, the kickback will cause the input voltages V_{in+} and V_{in-} to move by different amounts due to the mismatch in the impedance looking into V_{in+} and V_{in-}; this causes an undesired offset in the latch.

If the on-resistance of the switches connecting the reference voltages to the top plates of the capacitors are similar enough, the kickback disturbance from the latch will affect the input voltages equally. Since the two reference voltages are different, it not possible to guarantee that the on-resistance of switches is well matched under process and temperature variations. To avoid this issue, the switches should be sized to have low enough on-resistance such that the reference voltages on the top plates of the capacitors are held close to their ideal value when the latch is enabled. This will ensure that the coupling to the two input terminals is approximately equal.

In order to minimize the offset, the layout of the latch comparator is made to be as symmetric as possible. There are two strips of dummy poly-silicon blocks attached on the edge of the cell. These dummy poly lines increases the nearby poly density, which

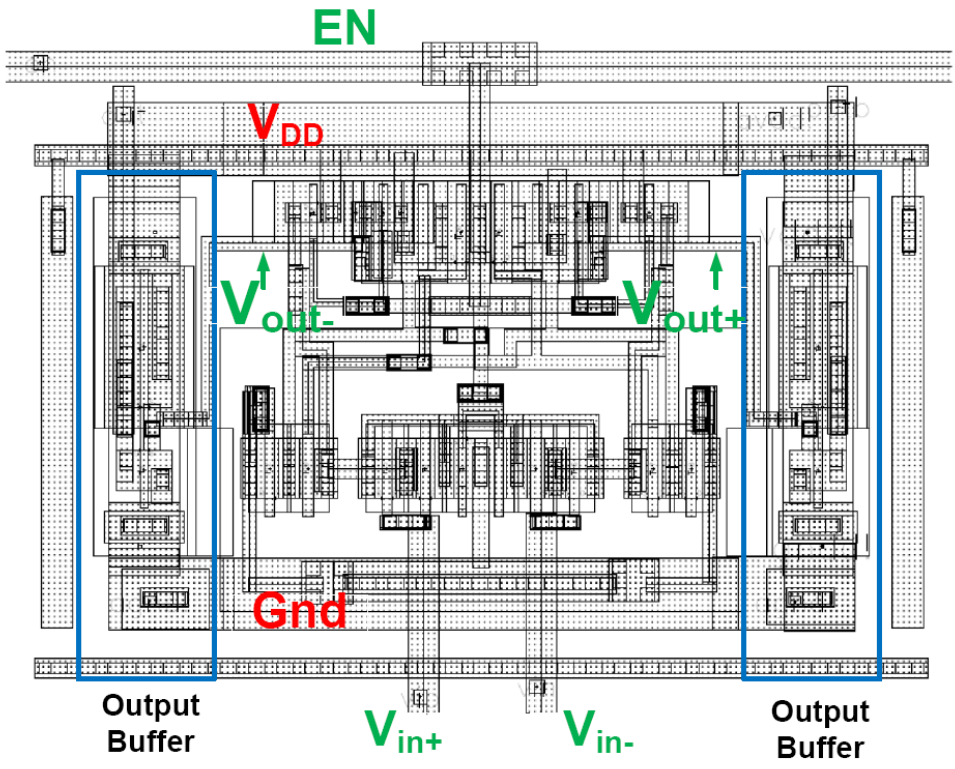


Figure 5-9: Layout of the latch comparator

helps to reduce mismatch in gate lengths due to etching variation [29]. As shown in Figure 5-9, the enable signal EN is routed into the middle of the comparator so that the capacitive coupling to each side of the comparator is equal. Unbalanced coupling would induce offset in the comparator. In addition, a triple well is used to isolate the noise generated by this block from the substrate.

5.4 Dynamically Biased Current Source

The linearity of the current sources used in ZCBC directly affects the linearity of the ADC. The non-linearity comes from the finite output resistance of the transistors and the non-linear junction capacitance of the transistors. The contribution of non-linear errors is also dependent on the delay of the zero-crossing detector as described in Chapter 4. The output resistance can be approximated by the following equation.

$$r_o = \frac{1}{\lambda I_{ds}} \tag{5.5}$$

The output impedance r_o is inversely proportional to the product of the drain current and λ, which is the inverse of the Early Voltage. For high speed designs, the linearity problem is worsened due to the higher ramp rate required to reach the entire output range. If the delay of the zero-crossing detector remains approximately fixed, then the overshoot will be larger. Given the non-linearity of the ramp, the variation overshoot will increase accordingly. In addition, larger transistors are needed to generate higher current values for high speed operation. The additional non-linear junction capacitance from the transistors further degrades the linearity of ramp rate.

A new type of current source is explored in this work to achieve the desired ramp linearity at an operating frequency of 200 MHz. The dynamically biased current source is shown in Figure 5-10. The devices M2 and M3 form the core part of the current source. M3 acts as a cascode device, which helps to improve the output resistance by a factor of gm_3ro_3, where gm_3 and ro_3 are the transconductance and output resistance of M3.

For a standard current source, the output current always decreases when the V_{DS}

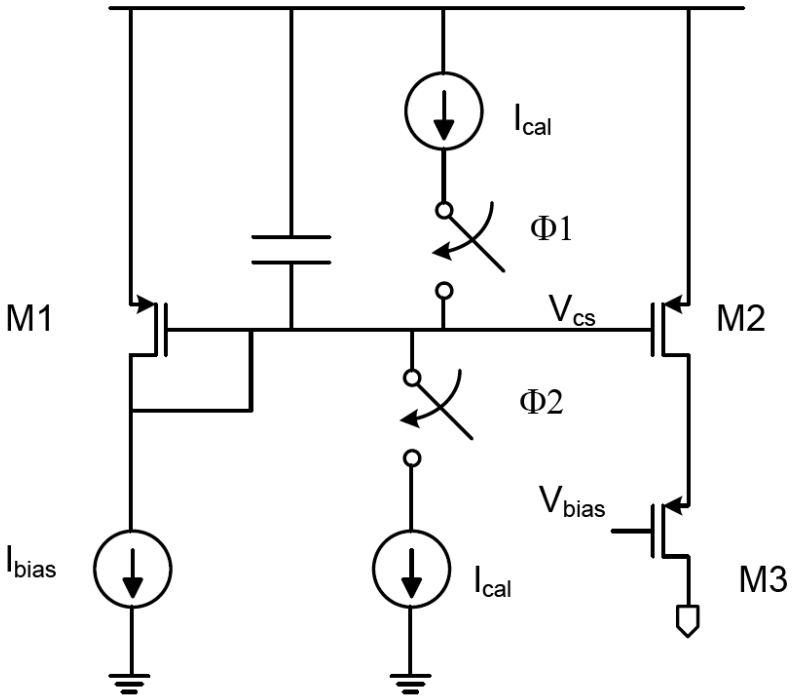


Figure 5-10: Dynamically Biased Current Source (DBCS)

is smaller. Thus, as the output voltage rises, the current value through a PMOS current source will decrease. In ZCBC, the reduced current changes the ramp-rate and causes non-linearity in the ADC.

Instead of biasing the gate of M2 with a static voltage from a current mirror, a dynamic bias voltage is generated on the gate of M2 to compensate for the decreasing ramp rate at the output node. As the output voltage rises, the bias voltage on the gate of M2 is reduced. This increase the overdrive voltage of M2 and increases the amount of current sourced by M2 to compensate for the reduction of current due to the smaller V_{DS}.

The dynamically biased current source (DBCS) operates in two phases. During the charge transfer phase, when the current source is active, ϕ_1 is low and ϕ_2 is high. When ϕ_2 is high, a small current source with value I_{cal} gradually lowers the bias voltage V_{cs}. The decreasing bias voltage on the gate of M2 increases its overdrive voltage and helps to compensate for the reduction in the ramp rate. During the follow phase ϕ_1, the previous bias voltage for V_{cs} is restored.

The value of I_{cal} needed for optimal correction is dependent on the process parameters and temperature variation. A calibration step is needed periodically to determine the optimal I_{cal} value. In this design, a 4-bit current DAC can control the value of I_{cal} digitally. The calibration code can be set in a range from 0 to 15. The 0 calibration code disables the dynamic biasing circuit and the current source becomes a traditional current mirror current source. To calibrate I_{cal}, a test sine wave needs to be applied to the ADC. For each possible value of I_{cal}, ranging from 0 to 15, a FFT can be applied to the output ADC data to determine its SNDR. I_{cal} should be chosen to maximize the SNDR. The optimal calibration value depends on temperature; thus, the calibration needs to be done periodically to achieve optimal performance.

Figure 5-11 shows the ramp rate variation as a function of the output voltage when the rate is set for 200 MS/s operation. The ramp rate decreases as the output voltage increases. As the output voltage moves higher, the transistors are eventually pushed into triode and the ramp rate reduces drastically. As Figure 5-11 shows, there is a significant improvement in the ramp rate linearity with the correct calibration code,

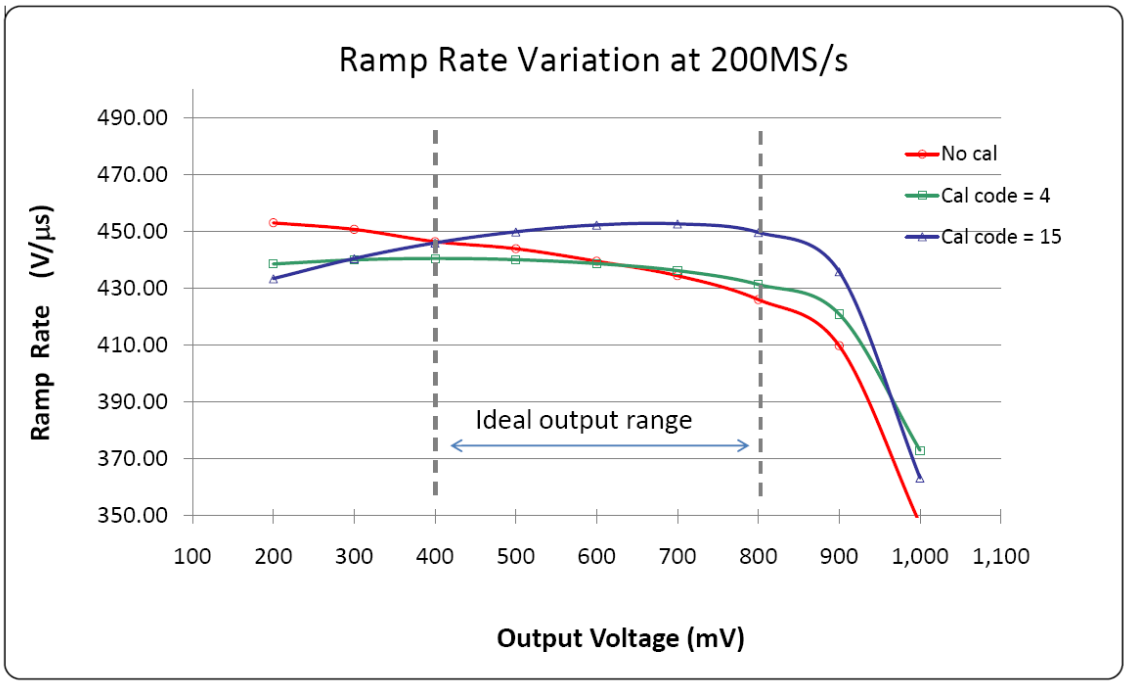


Figure 5-11: PMOS current source ramp linearity at 200 MS/s

but is there is also a possibility of over-correcting the non-linearity. For example, as shown in Figure 5-11, when the calibration code 15 is applied, the ramp rate changes as the output voltage increases. Figure 5-12 shows the ramp rate variation when the ADC is set for 100 MS/s operation.

This technique can greatly improve the linearity of the ramp rate when the sampling rate is very fast. However, for the measurements of the 12 bit prototype ADC at 100MS/s, using this technique did not show any improvement because the ADC performance was limited by capacitor matching.

5.5 Zero-Crossing Detector

The zero-crossing detector is the core part of the MDAC. Its output voltage controls the sampling switch in the next stage. As the input to the zero-crossing detector crosses its threshold, it will trip and turn off the sampling switch to capture the output voltage on the output capacitors.

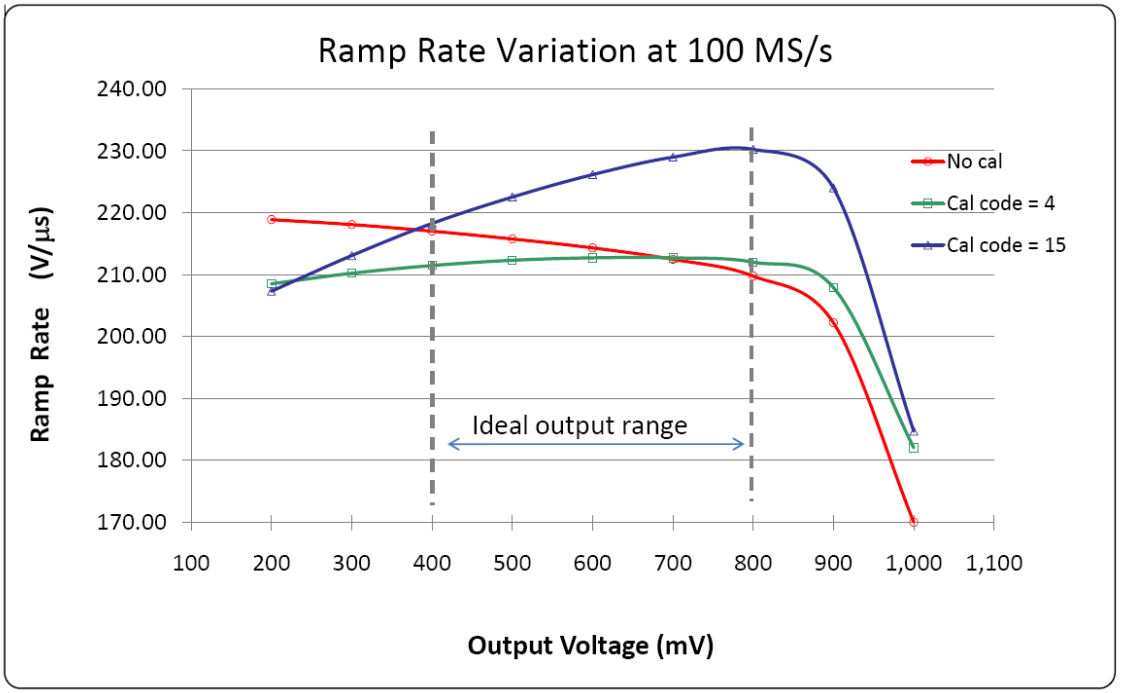


Figure 5-12: PMOS current source ramp linearity at 100 MS/s

The zero-crossing detector's delay directly affects the linearity of the circuit. Let t_{delay} be the delay of the zero-crossing detector. After the zero-crossing condition happens, the zero-crossing detector does not turn off the sampling switch until t_{delay} later. During this time, the output continues to ramp at the same rate. The resulting overshoot can be expressed as the product of the delay with the ramp rate at the output.

$$V_{overshoot} = t_{delay}\frac{dV}{dt} \tag{5.6}$$

If the output ramp rate is always constant, the resulting overshoot term will be constant. The resulting overshoot term will result in a constant input referred offset error, which can be corrected by an offset cancellation circuit. However, due to the non-linear ramp rate, this overshoot term will vary with the final output voltage, and thus cause non-linearity. This $\Delta V_{overshoot}$ causes non-linearity and its contribution should be limited to less than 1/2 LSB. This error can be minimized by decreasing

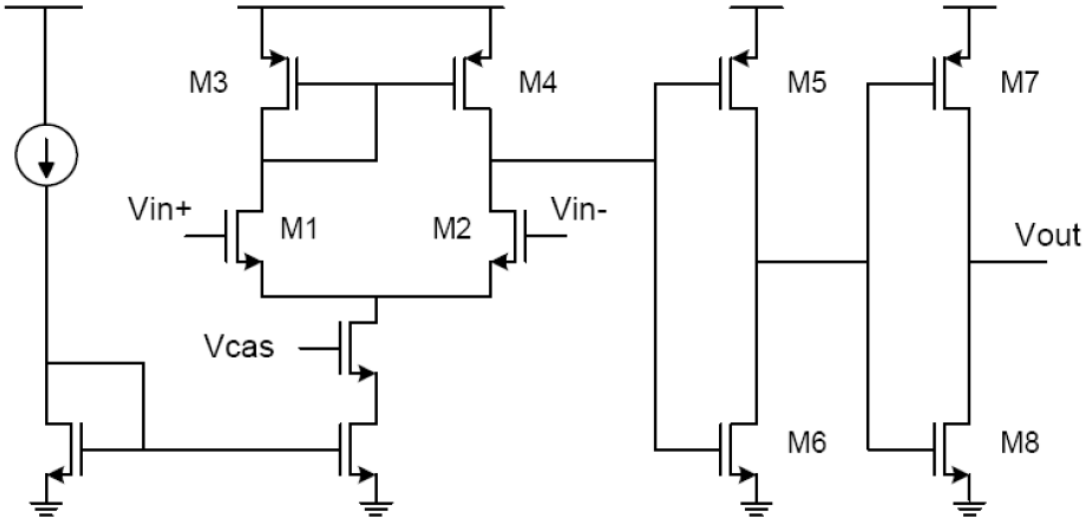


Figure 5-13: Zero-Crossing Detector

the delay of the ZCD or increasing the linearity of the ramp rate.

$$\Delta V_{overshoot} = t_{delay} \Delta \frac{dV}{dt} \tag{5.7}$$

The zero-crossing detector is implemented using a differential pre-amp followed by digital logic. The pre-amp is comprised of a differential pair as shown in figure 5-13. The input pair M1 and M2 is made wide to maximize their transconductance so that the input referred noise of the circuit is minimized. The devices M3 and M4 have smaller W/L ratios, which limits their transconductance values. This helps to reduce the input referred noise that they contribute. The pre-amp's tail current source is cascoded to improve its common mode rejection [15].

There are two inverters following the preamp that are used to amplify the pre-amp's output voltage to a full rail-to-rail signal. Since the input to the zero-crossing detector always moves in the same direction during the ramping, the inverters are heavily skewed to minimize the delay in one direction. In this design, the W/L ratio of M5 is made to be 20x larger than that of M6 and the W/L ratio of M8 is made to be 28x larger than that of M7. There are additional switches (not shown) used in

the preset phase to preset the zero-crossing detector's output to V_{DD}, which turns on the sampling switch in the next stage.

The layout of the zero-crossing detector is made as symmetric as possible to minimize offset and improve common mode rejection. The input differential pair is laid out using a Common Centroid pattern. To isolate it from substrate noise, the zero-crossing detector sits in its own well. The NMOS devices sit inside a P-well which is inside the N-well. Also, a P+ guard ring surrounds the zero-crossing detector's N-well to shield it from unwanted disturbances in the substrate.

5.6 Switches

For switches, their on-resistance can be expressed by the following formula.

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)} \tag{5.8}$$

The μ_n, V_t, and C_{ox} are process dependent parameters. The channel length is typically chosen to be the minimum size to minimize the on-resistance. The design parameters are W and V_{gs} . Increasing the width increases the amount of parasitic junction capacitance which increases the amount of coupling from the clock signal. In addition, larger W will cause more charge injection when the switch is turned off. Another way to lower a switch's on-resistance is by increasing its gate to source voltage through boot-strapping [26]. This technique has become very common in scaled CMOS processes for low resistance switches. The bootstrapped switch's on-resistance is more linear over the entire output voltage range compared to CMOS switches. This is especially important for ZCBC since current is flowing through the switches at the sampling instant. Variation in the resistance would add a non-linearity to the sampled value [1]. The circuit implementation of the bootstrapped switch is shown in Figure 5-14

For the sampling network, boot-strapping is used to lower the on-resistance and to keep the on-resistance constant. This is done in a way such that the gate oxide voltages do not exceed V_{DD}. This ensures that there is no reliability problem.

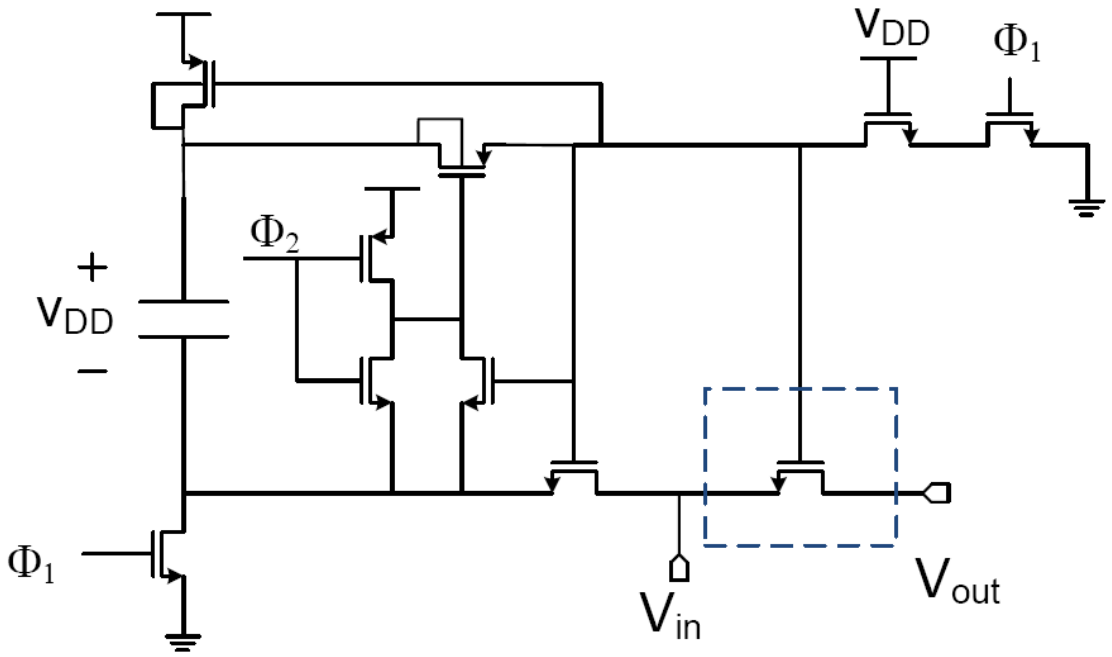


Figure 5-14: Bootstrapped Switch

The common mode voltage in this design is set at mid rail. At this voltage, the NMOS conductance is much better than the PMOS conductance. Thus, NMOS switches are used for the switches that connect the bottom plates of capacitors to the common mode voltage.

The series switches that connect one stage to the following stage also use boot-strapping to ensure that the on-resistance is constant. The current source splitting technique [3] is used to reduce the non-linear effects from these switches. A plot of various switch on-resistance characteristics is shown in Figure 5-15, 5-16, 5-17, and 5-18 . The transistors are turn on and the input voltage is connected to the source and the drain of the switch for this simulation.

As shown in 5-18, the NMOS boot-strapped switch's resistance is the most constant. However, there is still a gradual increase in the resistance value as the output voltage rises due to the back gate effect. As the output voltage rises, the source-to-bulk potential increases, causing the threshold of the device to rise. This causes an

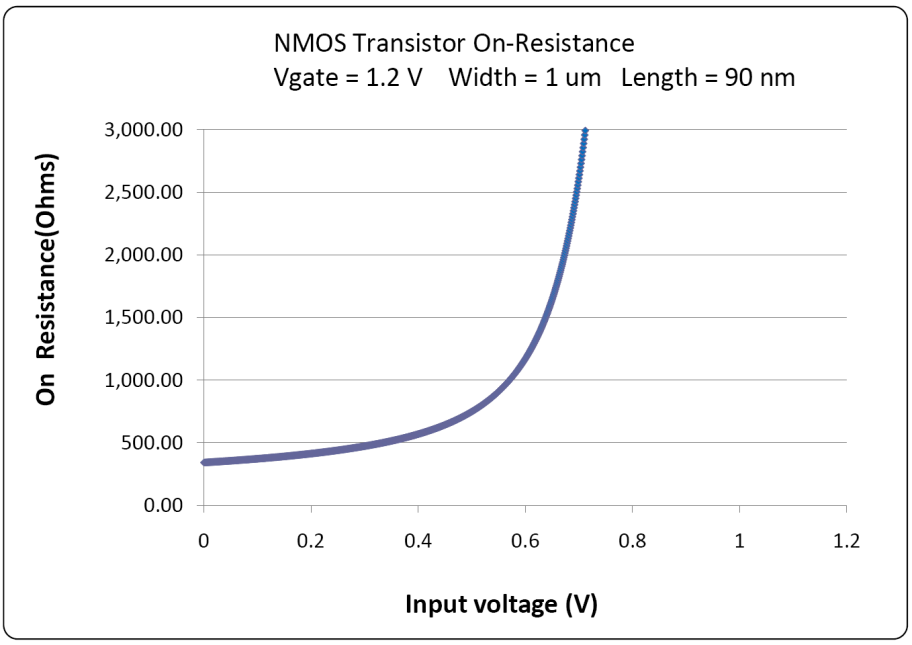


Figure 5-15: NMOS switch on-resistance

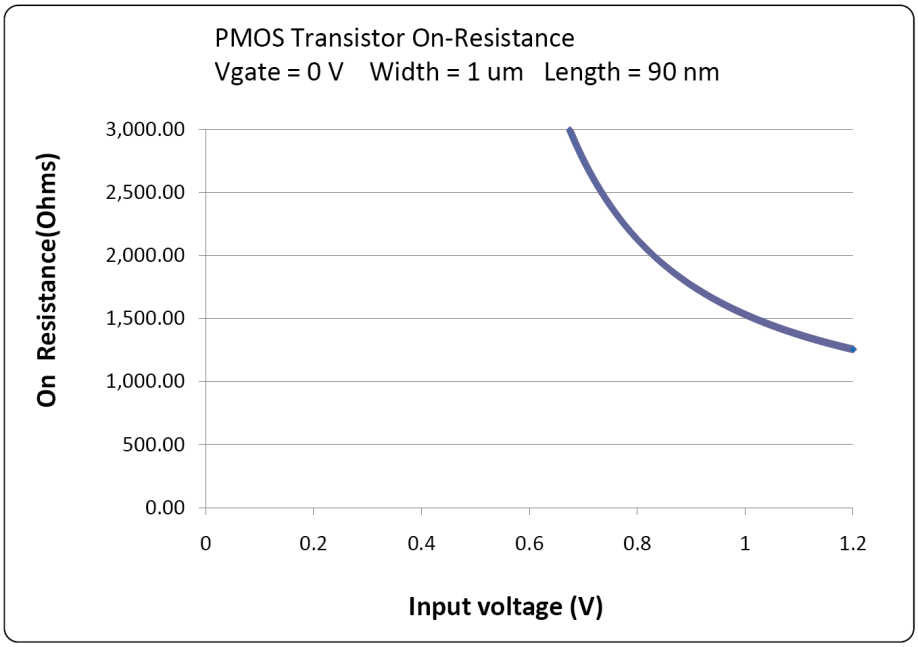


Figure 5-16: PMOS switch on-resistance

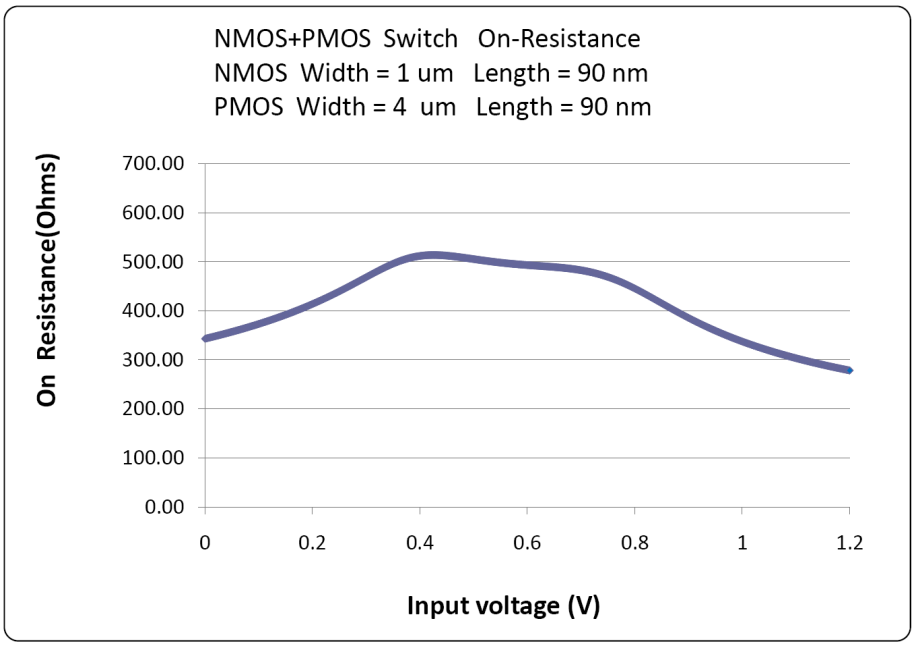


Figure 5-17: Complementary switch on-resistance

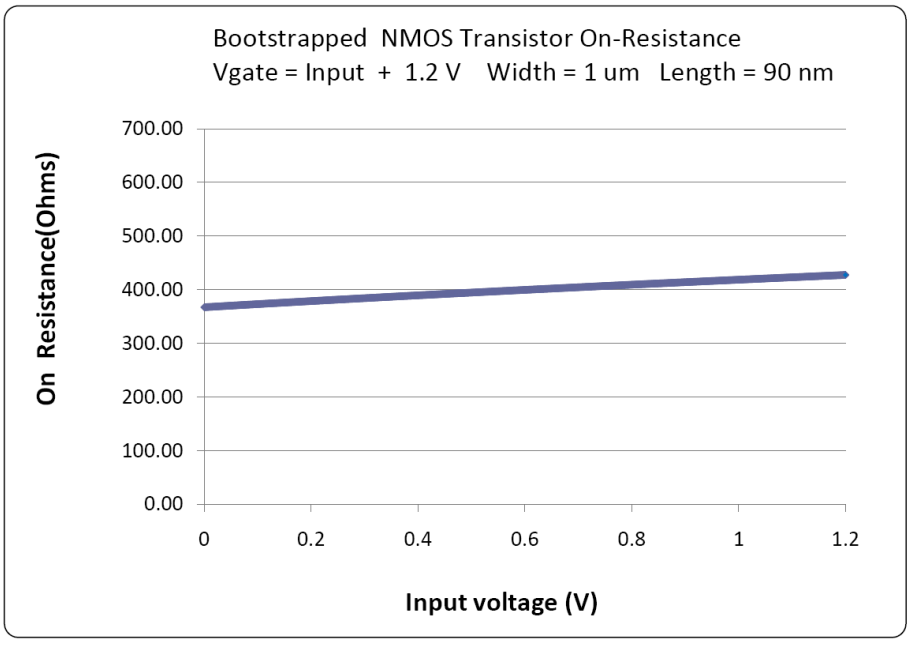


Figure 5-18: Bootstrapped NMOS switch on-resistance

increase in on-resistance. In a triple-well process, it's possible to isolate the bulk of the boosted switch from the global substrate and tie its bulk to the source during the phase when the switch is turned on. The resulting on-resistance becomes much more linear.

In Figure 5-1, the switches that connect stage N to stage N+1 are implemented by the bootstrapped NMOS switch. By using splitting the first stage and second stage current sources, the linearity requirement of the switch resistance is relaxed since the switches only need to carry mismatch current [3]. At 100 MS/s, the nominal current of the second stage is set at 100 μA. Given an effective load capacitor of 0.5 pF, the ramp rate is equal to 0.2V per ns. If there is a 15% mismatch between the second stage current source and the first stage current source, there can be up to 15 μA of current flowing through the switch that connects the first stage to the second. By using 12 1μ wide bootstrapped switches connected in parallel, the variation in the resistance is limited to 5 Ω over the output voltage range. The variation in the output voltage caused by the variation in the switch resistance is given by

$$\begin{aligned} \Delta V &= I_{mismatch}\Delta R \\ &= 15\mu A \cdot 5 \\ &= 75\mu V. \end{aligned} \tag{5.9}$$

This output voltage error of $75\mu V$ is equivalent to $18.75\mu V$ of input referred error since the inter-stage gain of the pipelined stage is 4. At the 12 bit resolution, the LSB size is given by $\frac{2}{2^{12}}$ which is equal to 488 μV. Thus this error is equivalent to approximately to 0.04 of an LSB.

5.7 Reference Ripple Reduction Technique

The reference voltages are used to charge the capacitors in the pipelined ADC stages during the amplification phase. The reference voltages need to be clean in order

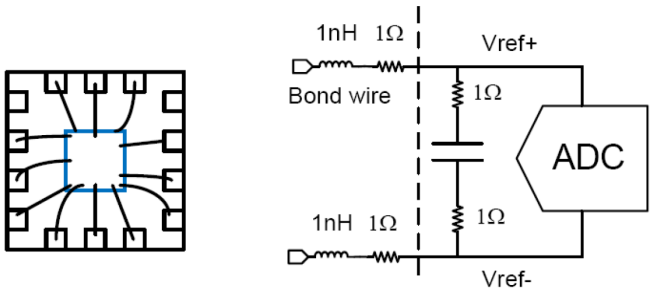


Figure 5-19: Model of the bondwire and the on-chip circuitry

to ensure accurate ADC operation. Figure 5-19 shows the die, drawn in blue, wire bonded to the package. The bondwire connecting the die to the external pad can be modeled by a resistor in series with an inductor, as shown on the right of Figure 5-19. The circuit on the right of the dotted line represent the on-chip circuit. On-chip by pass capacitors can be added to reduce the ripples on the reference voltages. However, large by-pass capacitors cost area, which may not be available. In addition, any series resistance in the capacitor or from the routing will limit its ability to cancel out sharp transients.

In a pipelined ADC design, reference voltages V_{ref+} and V_{ref-} are used to drive capacitors in the switched-capacitor circuit during the charge transfer operation. In Figure 5-1, V_{ref+} and V_{ref-} is connected to the top plates of C_{1+} and C_{1-} during the charge transfer operation. For op-amp based designs, the output voltage is always sampled at the end of the phase, giving the V_{ref+} and V_{ref-} voltages almost the entire period to settle. However, for zero-crossing based ADCs, the charge transfer is finished before the end of the half clock period. If the reference voltage is not settled by the sampling time, its deviation from the ideal value will add an error term at the output. In this aspect, the single-phase ZCBC is at a disadvantage compared to op-amp based designs. Care must be taken to ensure that the reference voltages are sufficiently settled by the earliest possible end time of the charge transfer operation. However, the dual-phase ZCBC [9], the sampling time occurs close to the end of the clock period thus allowing more time for the reference voltages to settle.

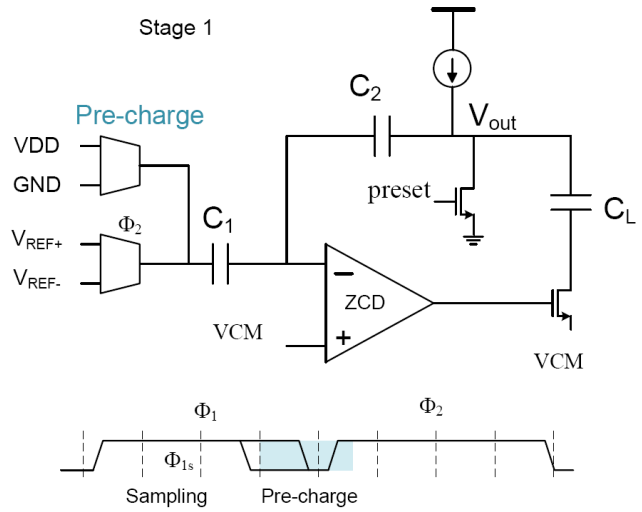


Figure 5-20: MDAC with reference pre-charge circuit

For the single-phase ZCBC,it is possible to increas time by increasing the time of the preset phase. By increasing the preset time, the start time of the charge-transfer operation is delayed. This allows more time for the reference voltages to settle. However, the system will need a faster ramp for a given ADC operating speed. The faster ramp rate will cause more overshoot and thus degrade the linearity.

In this design, a coarse reference pre-charge phase is added to the first stage of the ADC, where the accuracy is the most important. This stage usually contributes the most disturbance on the reference nodes because its MDAC capacitors are the largest. The new reference pre-charge circuit is attached in parallel to the regular analog mux circuits used in the MDAC as shown in Figure 5-20. The pre-charge reference circuit is only used in the first stage because there is extra time that can be allocated for this operation in the first stage. The time is borrowed from the input sampling time. In addition, two additional pins are used to connect two separate voltages, which is equal to V_{DD} and GND, to the additional reference pre-charge circuit. The pre-charge reference circuit drives the nodes that need to be driven by V_{ref+} and V_{ref-} to within tens of mili-volts before the actual V_{ref+} and V_{ref-} are connected. This greatly reduces the disturbance on the reference nodes and allows the system to meet its accuracy requirement. In this design, the voltages attached to

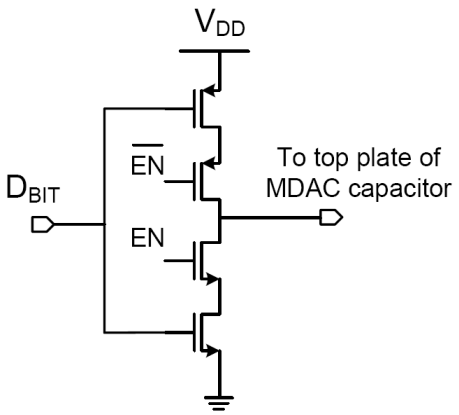


Figure 5-21: Reference Pre-charge Circuit implementation

the pre-charge circuit are at the same potential as V_{ref+} and V_{ref-}.

After the input voltage is sampled, there is some time given for the flash ADCs to generate the bit decisions. Once the bit decisions are ready, the reference pre-charge circuit is enabled. The top plates of the capacitors are pulled toward either V_{DD} or GND. During the preset time of the following phase, the reference pre-charge circuit is disabled. The EN and $\overline{EN}$ signal isolates the pre-charge voltages from the output node and the actual reference voltage is then applied to the top plates of the MDAC capacitors.

The pre-charge circuit significantly reduces the bounce on the V_{ref+} and V_{ref-} nodes. This helps to ensure that the ADC's performance is not limited by the settling of the reference voltages.

To test this circuit in simulation, a 1 ohm resistor in series with a 1 nH inductor is used to model the bondwire. An on-chip decoupling capacitor is added. 1 ohm resistors are added in series with the capacitor to model metal routing resistance. In this simulation, a 150 pF decoupling capacitor is used. The Figures 5-22 and 5-23 show the reference voltage disturbance on the V_{REF+} and V_{REF-} node. The blue trace in 5-22 shows the disturbance without pre-charging. The green trace shows the same reference voltage when the pre-charge circuit is activated. The disturbance on the V_{REF+} node is similar to that on the V_{REF-} node and is shown in Figures 5-22 and 5-23. The differential error voltage between V_{REF+} and V_{REF-} is ploted in Figures

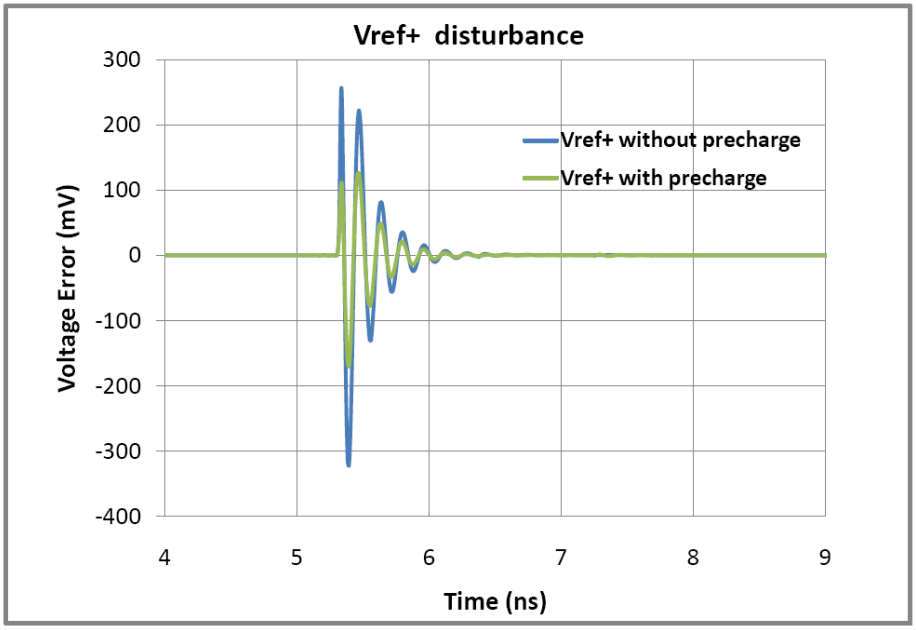


Figure 5-22: Transient simulation of reference voltage disturbance with 150 pF of on-chip decoupling

5-24 and 5-25. There is a significant reduction in the amount of disturbance when the precharge circuitry is activated. In Figure 5-25, the differential reference voltage error settles to within 250 μV which is equal to the 1/2 LSB size in this design within approximately 1.0 ns of the start of the preset phase.

Another benefit of the pre-charge circuit is that it greatly reduces the magnitude of the initial disturbance as shown in Figures 5-24 and 5-25. This is especially helpful in a time-interleaved ADCs since different sub-ADCs are constantly active. One ADC may need an accurate reference voltage while the other ADCs are generating large transients on the reference voltages. As Figures 5-24 and 5-25 shows, the size of the initial disturbance is reduced by approximately a factor of 3 when the reference pre-charge circuit is enabled.

5.8 Offset Cancellation

Due to the finite delay of the zero-crossing detector, the ADC inherently has offset caused by the overshoot. If left alone, this offset will reduce the effective input range.

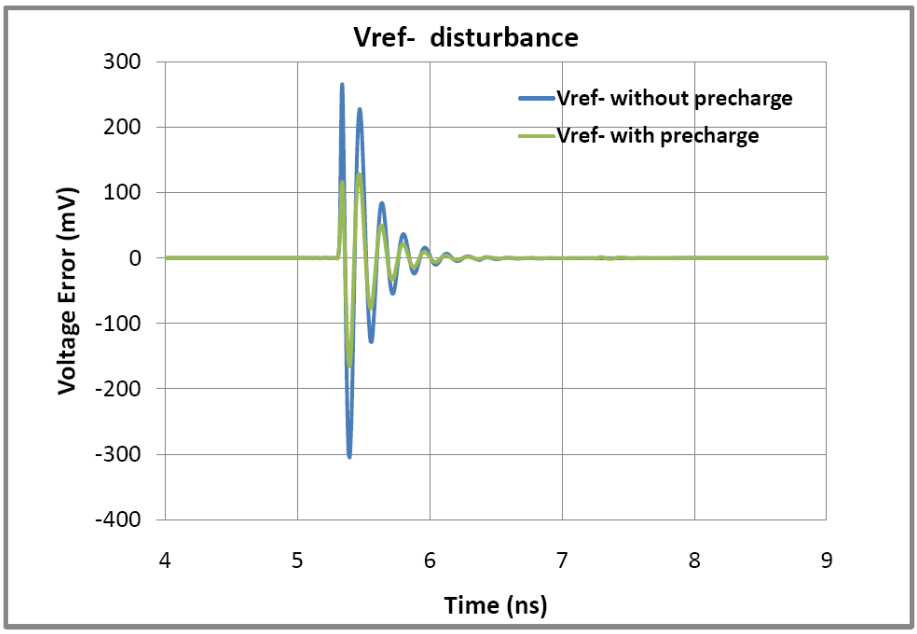


Figure 5-23: Transient simulation of reference voltage disturbance with 150 pF of on-chip decoupling

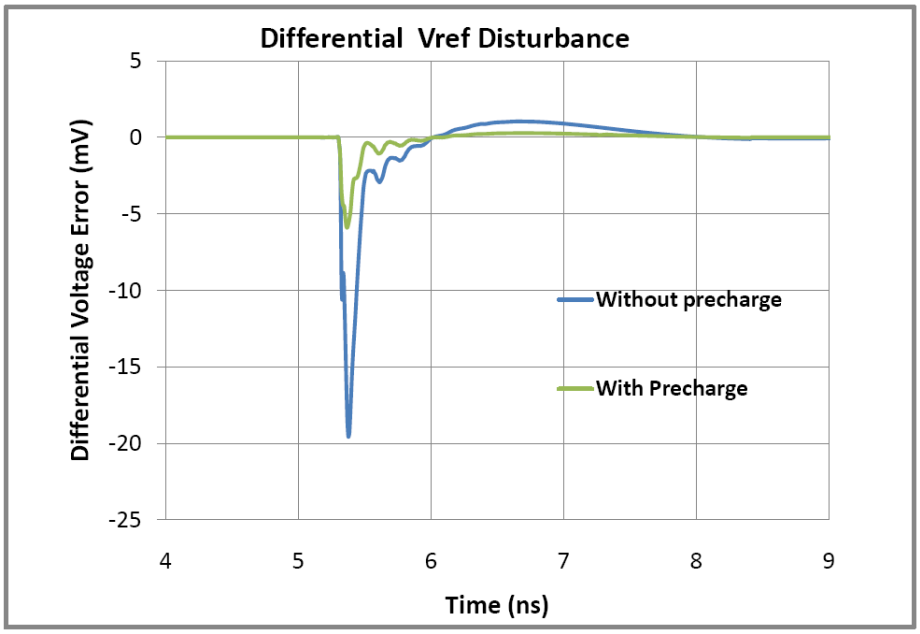


Figure 5-24: Transient simulation of reference voltage disturbance with 150 pF of on-chip decoupling

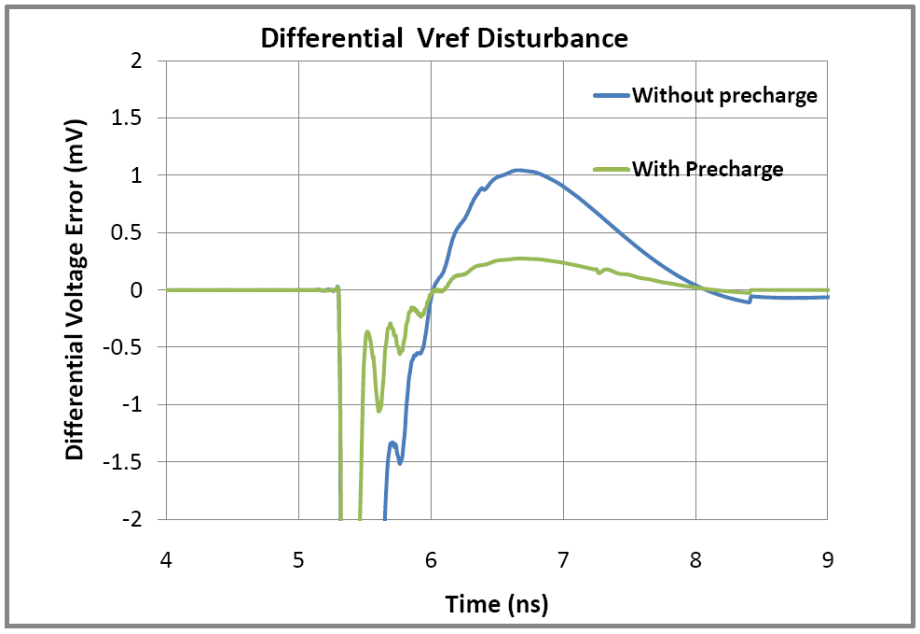


Figure 5-25: Transient simulation of reference voltage disturbance with 150 pF of on-chip decoupling

In this design, an offset correction circuit was added to the MDAC to help correct for offset as shown in Figure 5-26.

The offset correction circuit shown in Figure 5-26 injects addition charge ΔQ during the charge transfer operation into the virtual ground node. ΔQ is equal to $V_{DD}C_{offset}$ where C_{offset} is the offset correction capacitor. C_{offset} is digitally modified to change the ΔQ injected. The amount of input-referred offset canceled is given by $\frac{\Delta Q}{C_1+C_2}$.

The implementation of the offset correction circuit is also shown in Figure 5-26. The digital control bits $CAL[3:0]$ are used to select an array of binary weighted capacitors. If $CAL[i]$ is selected, then $C[i]$ will add charge equal to $V_{DD}C[i]$ to the virtual ground node during the charge transfer. Any combination of the $C[i]$ capacitors may be selected to cancel out the offset. The total size of this offset correction capacitor bank is approximately 1.5% of the sampling capacitors in the array, C_1 and C_2. Thus given a differential implementation, the maximum offset that can be corrected using this circuit is given by $2V_{DD}\frac{C_{offset}}{C_1+C_2}$ which is equal to $0.03V_{DD}$.

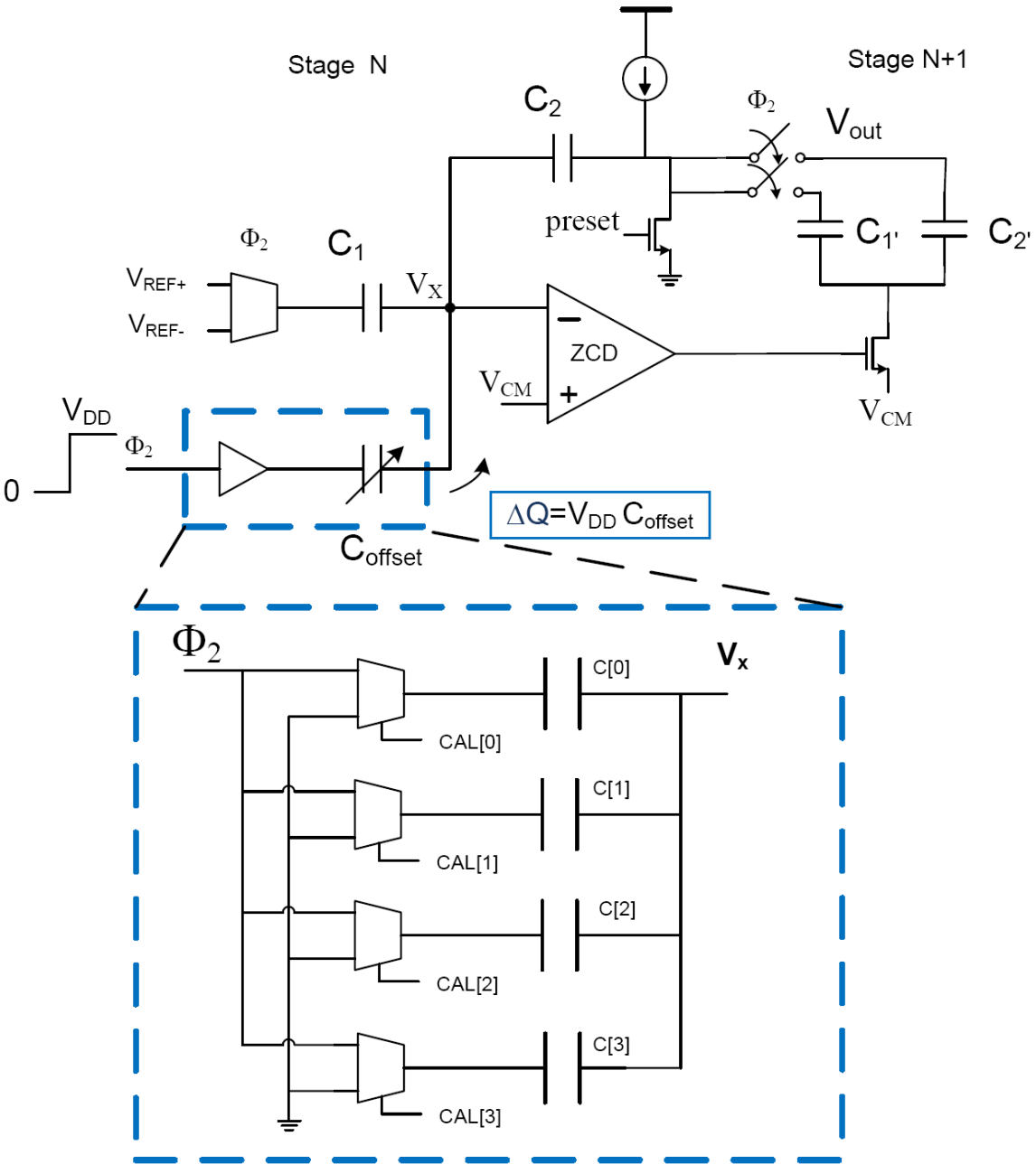


Figure 5-26: Offset Correction Circuit

For a 1.2 V V_{DD}, the maximum offset that can be corrected is 36 mV. The feedback factor β is 1/4 in this design. The amount of overshoot at the output that can be corrected is equal to $\frac{1}{\beta}36mV$ which is equal to 144 mV.

Calibration is required to correct for the offset. By observing the output digital code given a zero differential input voltage, the offset due to the overshoot can be estimated and corrected. The calibration bits can be adjusted until the output digital code is the expected value without overshoot.

5.9 Decision Boundary Gap Estimation

Mismatch in the capacitor array causes unwanted gaps or overlaps in the ADC transfer function as shown in Figure 5-27. The size of the gap, labeled K in the figure, depends on the amount of mismatch in the capacitor array. The error caused by this capacitor mismatch is correctable in the digital domain as long as the size of the gap is known. In this work, the Decision Boundary Gap Estimation (DBGE) was used to estimate the size of the gap [30]. Using the estimated gap value, digital correction can be applied to correct the errors. The correction procedure is simple and straightforward once K is known. As shown in Figure 5-27, when capacitor mismatches exist, there will be gaps in the ADC transfer function at the major decision boundaries. If the value K is added to all of the ADC codes to the right of the decision boundary, the corrected ADC characteristic shown in the solid line can be achieved.

The DBGE calibration is digital calibration technique that operates in the background and does not interrupt the regular ADC operation. DBGE calibration requires no modification in the analog circuitry, and automatically calibrates errors due to capacitor mismatch, finite gain (in op-amp based circuits), and ramp nonlinearity in ZCB circuits, which causes INL jumps at bit decision boundaries.

The operation of DBGE begins with collecting ADC data from a sufficiently active signal. No training signal is required as long as input signal to the ADC lands in the bins close to the digital decision boundaries. An ADC histogram around each major bit decision boundary is collected. Since the gap spans a small portion of the input

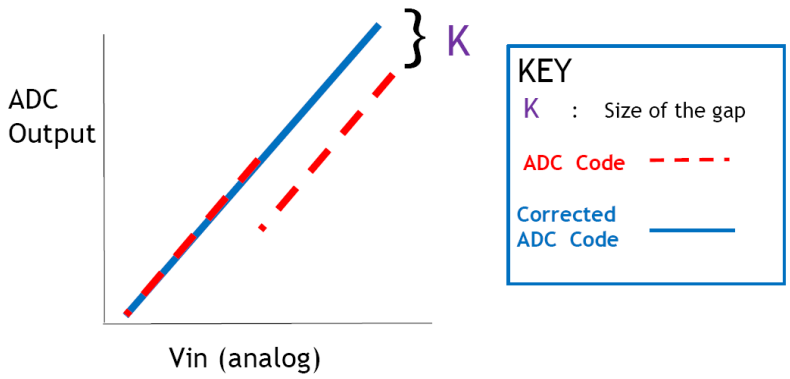


Figure 5-27: Effects of capacitor mismatch in pipelined ADCs

range, the ideal ADC output code histogram should be uniform around the decision boundaries. For example, the Figure 5-28 shows the histogram of ADC data given a sine wave input signal. However, for most signals, any small section of codes should have nearly uniform distribution as shown in the bottom plot in Figure 5-28.

When there are gaps or overlaps at the decision boundaries, the local ADC histogram will no longer be uniform. An example is shown using data collected from this ADC in Figure 5-29 and Figure 5-30. The gaps and overlaps have been exaggerated for clarity. In Figure 5-29 and Figure 5-30, there are two blocks of data that are separated based on a digital bit.

To estimate the size of the gap, one of the groups of data is shifted relative to the other group until the variance of the combined histogram is minimized. For a perfectly uniform distribution, the variance approaches zero as for large number of samples. By calculating the variance as one block of data is shifted relative to another, the optimal shift value that gives the most uniform distribution can be found. By minimizing the variance of the histogram, the error caused by the gap is minimized. This correction method minimizes the INL and the DNL. As shown in Figure 5-31, the variance for this particular boundary is found to be 11. The large periodic jumps in the variance plot is believed to be caused by the last stage of the ADC saturating. The saturation of the last stage causes oversaturated bins to occur periodically. When shifting one block of data, the variance of the data spikes when the saturated bins

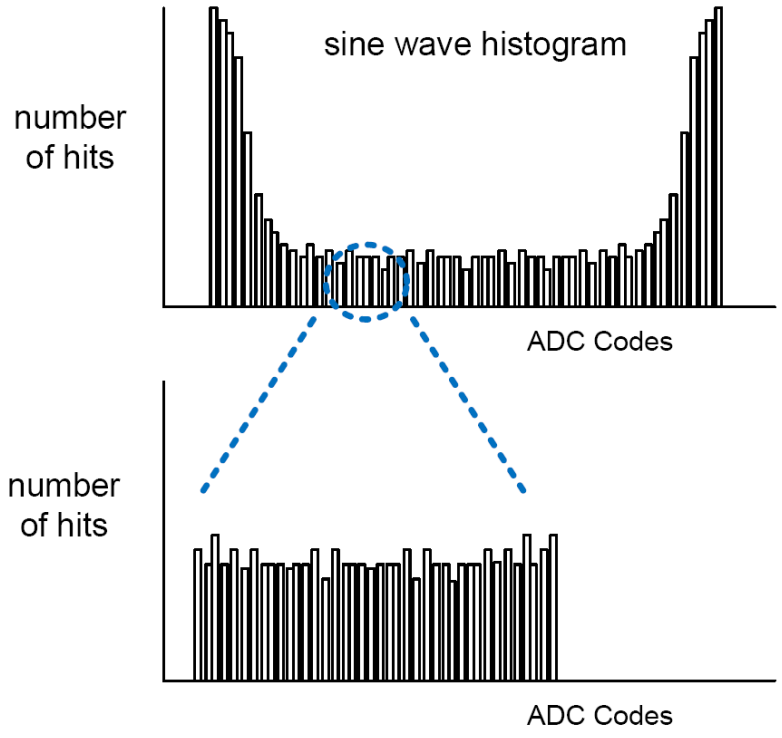


Figure 5-28: ADC histogram with a sine wave input

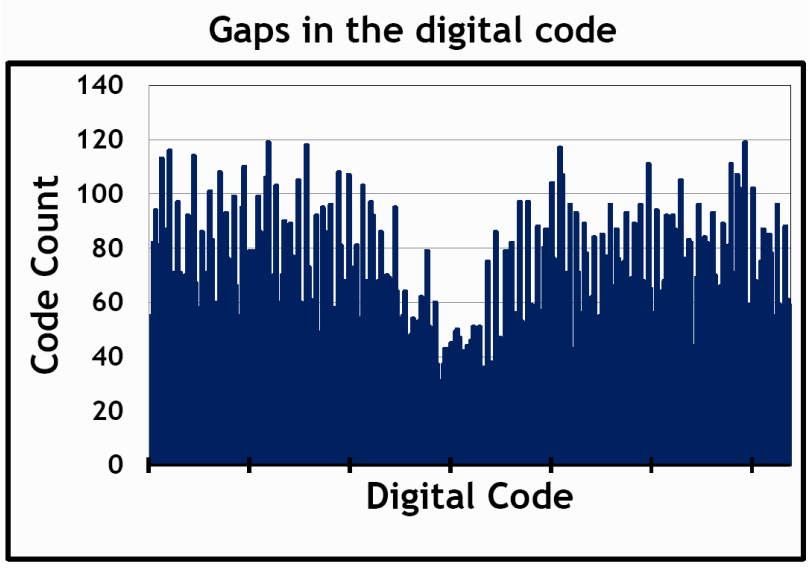


Figure 5-29: Local ADC histogram with a gap

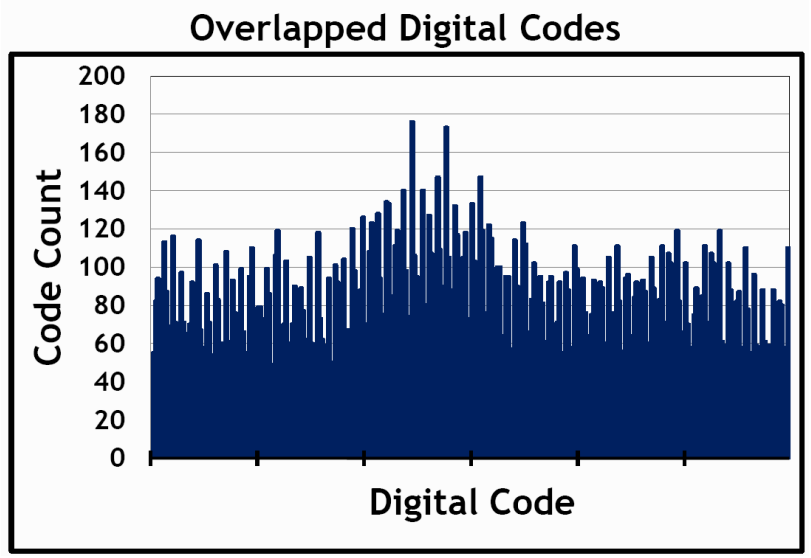


Figure 5-30: Local ADC histogram with overlap

are overlapped.

Since DBGE is a statistics based calibration, a large number of samples are required for the calibration. Furthermore, the DBGE can only applied if the input signal is sufficiently active around the major decision boundaries. Also, it relies on the fact that the distribution of the input signal is uniform around the decision boundary; so DBGE may not be suitable for all possible input signals.

This work presents the first hardware demonstration of the DBGE calibration for ADCs. In order to reduce the truncation error, the ADC is built with 13b raw resolution. For the calibration of first two stages, 819,200 input samples are collected . A full-scale sine wave around 24 MHz is used while the ADC samples at 100MS/s. DBGE works as long as the input signal fills the ADC bins near the boundary points. For each decision boundary, a code span of $+-$ 50 LSB_{12} is used for the computation of the optimal shift. Since the dominant source of nonlinearity in this ADC was capacitive mismatch, which stays constant, it's only necessary to run the calibration once. However, if desired, the calibration can run in the background periodically to compensate for time and temperature dependent errors such as insufficient gain and settling (op-amp based circuits) or ramp nonlinearity (ZCB circuits). The DBGE is applied to the first 2 stages of this ADC. To correct the data digitally, additional

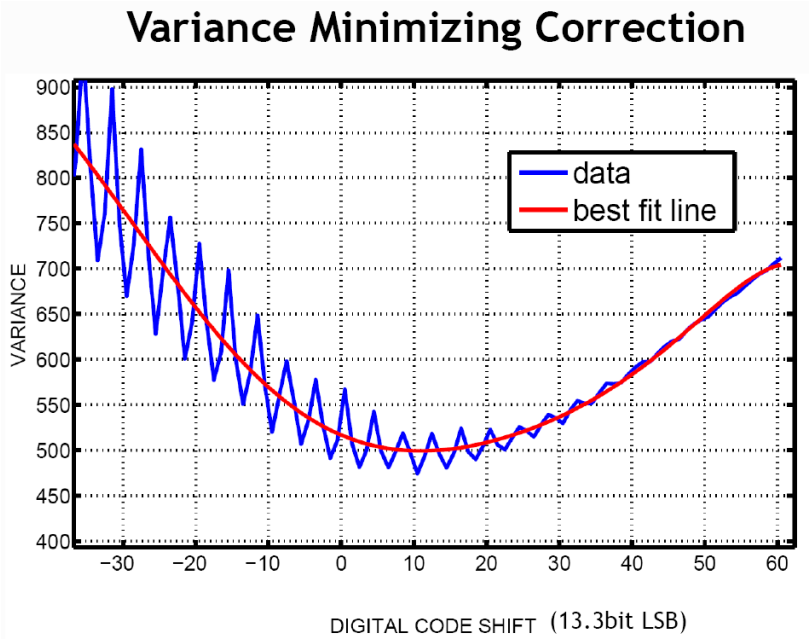


Figure 5-31: Variance minimizing curve

digital circuitry is required. During the normal operation after the calibration is complete, digital adders and a MUX are the only active calibration circuitry. For each stage, a decoder which reads the bit decisions drives a MUX that selects the specific correction value. A 14 bit adder is needed to add the ADC's output and the optimal correction value stored in a register. The estimated power consumption for these digital circuits operating at 100MHz is 30μW.

5.10 SRAM for Testing

An SRAM block is included on chip to store the ADC output data. The I/O drivers operating at 100 MHz could potentially inject substantial amounts of substrate noise. The use of the SRAM blocks allows the I/O drivers to be disabled while data is collected in the SRAM. The SRAM is organized in 8192 x 20 bits and occupies 0.4 mm^2. The controller for the SRAM has two states: read and write. When the SRAM is in write mode, the ADC continuously writes data to the SRAM. The data within the SRAM is periodically over-written. The data from the SRAM can be extracted during the read mode. A double date rate (DDR) scheme is used for the digital IO

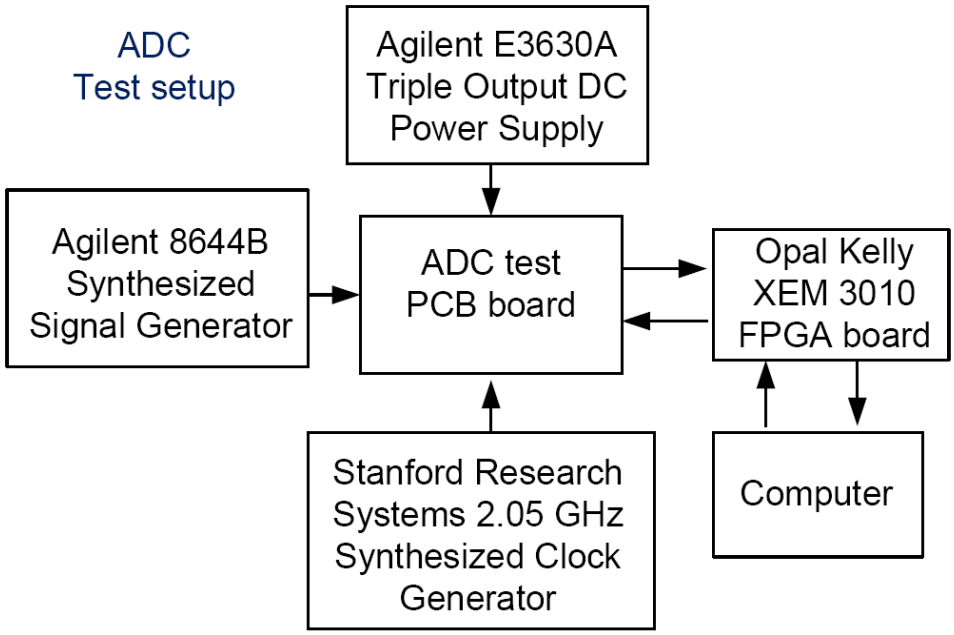


Figure 5-32: ADC evaluation test setup

interface to reduce the number of pins required.

During the testing, it was found that the ADC SNDR remained the same with the I/O drivers enabled or disabled.

5.11 Test Setup and Measurement Results

The ADC was designed with an on-chip programmable shift register to provide the ADC with various bias conditions. The ADC is programmed with the XEM-3010 FPGA board made by Opal-Kelly. The input source was generated by an arbitrary waveform generator. This single ended input signal is transformed into a differential input signal for the ADC by a transformer. The Stanford Research Systems Model CG 635 2.05 GHz Synthesized Clock generator was used as the clock source. A block diagram of the test setup is shown in figure 5-32. A band-pass filter is used at the output of the signal generator to improve the signal quality.

While the ADC operated at 100 MS/s, a 49 MHz sine wave input was used to test the ADC's dynamic performance. Before calibration, the ADC achieves 68 dB

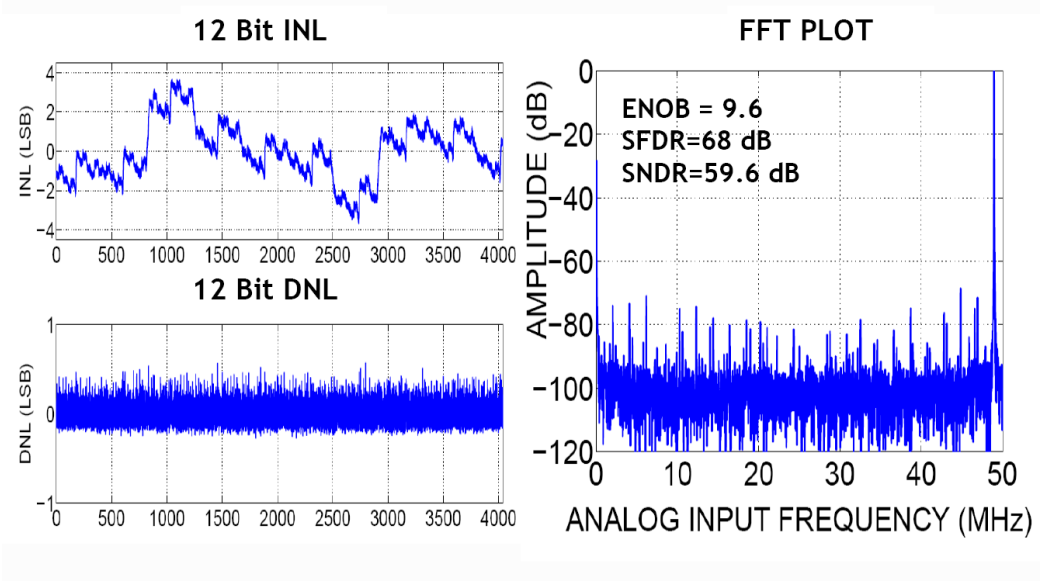


Figure 5-33: ZCB pipelined ADC measurement results before calibration

SFDR, 59 dB SNDR, and +/- 4 LSB_{12} INL. The linearity of the ADC was limited by systematic capacitor mismatch that resulted from asymmetric layout routing. Systematic capacitor mismatches caused large jumps in INL and limited the SNDR of the ADC. The measurement results before calibration is shown in Figure 5-33. Without any calibration, the ADC achieved 9.6 ENOB at 100 MS/s.

The Decision Boundary Gap Estimation technique was applied to digitally correct the gaps and overlaps in the ADC codes. After the DBGE calibration, the SFDR, SNDR, and INL are improved to 74 dB, 63 dB, and +/- 1.2 LSB_{12} respectively. The ADC, built in a 90 nm CMOS, occupies 0.32 mm^2 die area and consumes 6.2 mW (including the estimated digital calibration power) from a 1.2V supply. At 100MS/s, it achieves 10.2 ENOB with a 49MHz input signal for a figure of merit (FOM) of 53 fJ per step. The measurement results after calibration is shown in Figure 5-34.

The figure of merit of this work is compared to some recent publications in Figure 5-35. This work has a much lower figure of merit compared to previous pipelined ADC designs which used op-amps. The figure of merit of this ADC shows that zero-crossing based circuits is a more power efficient method for building switched capacitor circuits compared to op-amps for this speed and accuracy.

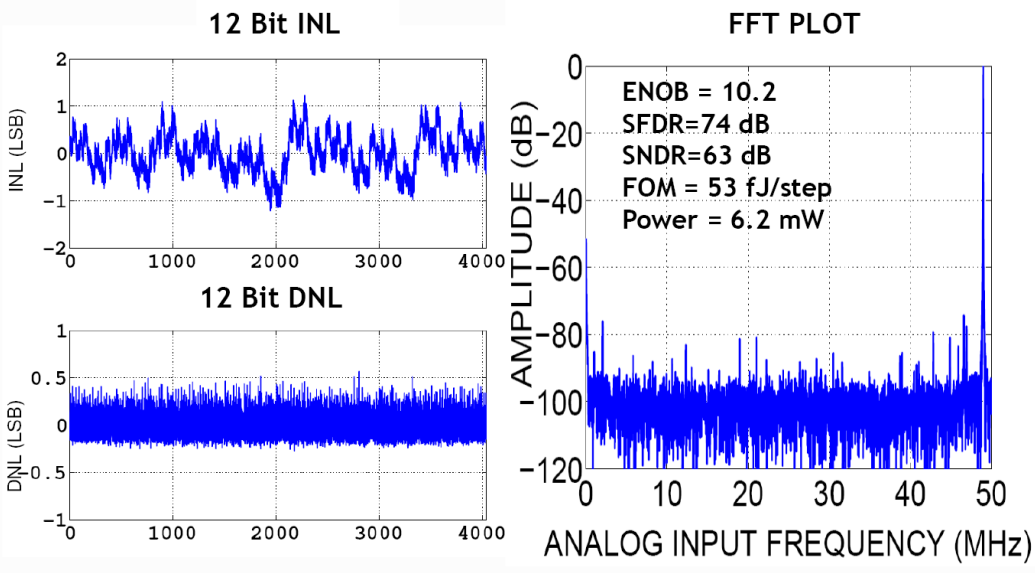


Figure 5-34: ZCB pipelined ADC measurement results after calibration

Figure of merit comparison

Author	ADC Type	Fsample	ENOB	FOM (fJ/step)
Choi, VLSI 08	Pipelined	50MS/s	10.3	284
Anthony, VLSI 08	BBD	250MS/s	10.6	350
Devarajan, ISSCC 09	Pipelined	125 MS/s	12.6	438
Brooks, ISSCC 09	ZCB Pipelined	50MS/s	10.0	88
Liu, ISSCC 10	SAR	45MS/s	10.8	36
This Work	ZCB Pipelined	100MS/s	10.2	53

* Select ADCs with ≥ 45 MS/s , ENOB ≥ 10 are included for comparison

Figure 5-35: Figure of merit comparison with recent ADCs in publications

Chapter 6

Time Interleaved Zero-Crossing Based ADCs

A trend in receiver design for digital TV and telecommunication systems is moving towards software-defined radios, where the embedded ADC is moved closer to the antenna [31]. Such an ADC requires 10-12 bit resolution, a high sampling rate up to multi-GHz, and low power for embedded applications. Time-interleaved converters, which were first introduced by Black and Hodges, are well suited for achieving these bandwidth and resolution requirements.

In addition, a high speed ADC can be used in a mm-wave imaging system to acquire the amplitude and the phase information of the incoming signal [32]. A power efficient ADC is desired since there are many receiver nodes in the mm-wave imaging system. The zero-crossing based time-interleaved ADC is a very power efficient method for achieving the high sampling rate required.

Time-interleaving can be applied to most ADC architectures to improve the overall sampling rate. By time-interleaving N ADCs, the combined sampling rate is increased by N compared to that of the individual ADC. The combined ADC's accuracy and dynamic performance will be limited by the matching between the different ADC channels. Mismatch in the offset, gain, and sampling times of the ADC channels will degrade the combined signal to noise and distortion ratio (SNDR).

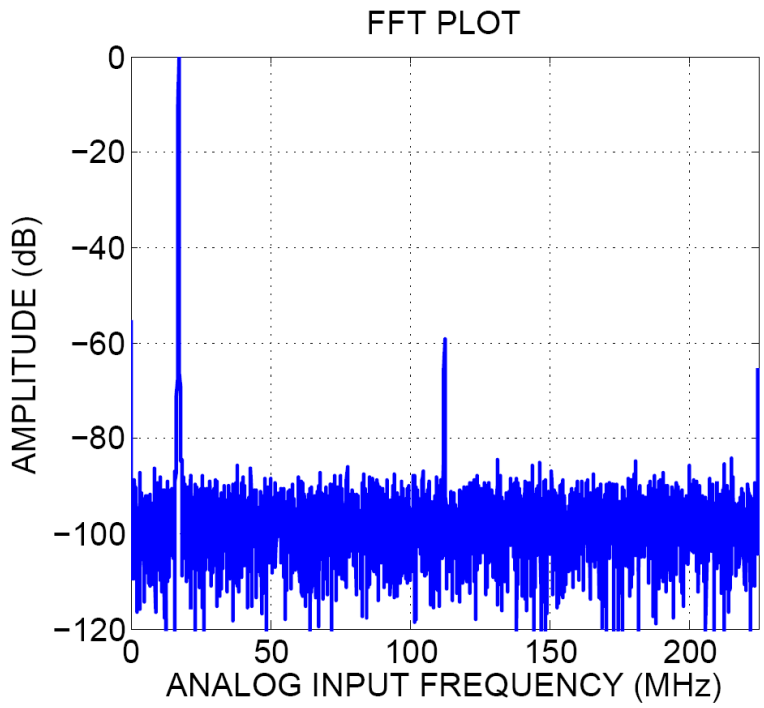


Figure 6-1: Frequency response of 1 LSB offset in a 4-way time-interleaved ADC

6.1 Time-Interleaved ADC Accuracy Limitations

Mismatch between the time-interleaved ADC channels will generate spurs in the frequency domain. Offset error, gain error, and timing skew generates tones that degrade the SFDR and the SNDR of the combined ADC. The effects of each type of mismatch will be discussed in this section.

6.1.1 Offset Mismatch

Offset refers to the static offset mismatch between the ADC channels. Different ADCs will have different DC offsets relative to each other due to device mismatch. The offset mismatch generates tones at frequencies that are multiples of $\frac{F_s}{N}$ where F_s is the sampling frequency and N is the number of interleaved channels. The power of the spurs generated by the offset mismatch is equal to the variance of the offsets [33].

The simulated plot in Figure 6-1 shows the frequency response of a 10-bit four-way time-interleaved ADC where one of the ADCs has a 1 LSB offset. This offset

corresponds to a 0.1% of the full scale. In this simulated ADC, the combined sampling rate is 450 MS/s. The input being sampled is a sine wave at 17.2 MHz. The tones generated by the offset occur at DC, 112.5 MHz, and 225 MHz. The resulting SFDR is limited to 60 dB from this 0.1% offset error in 1 ADC.

The offset error can be removed by digital calibration. Once the offset error is measured, digital addition or subtraction can be used to remove the offset from the mismatched ADC.

6.1.2 Gain Mismatch

Gain mismatch between the ADCs causes the amplitude of the output signals to vary depending on the ADC channel. The amplitude of the error depends on the amplitude of the input signal. In a time interleaved ADC, the gain error occurs periodically as the data from the mismatched ADC is periodically used. A simulated example of the effects of gain error on a sampled sine wave is shown in Figure 6-2. In this example, four ADCs are time-interleaved, and one of the four ADCs is given a large gain error of 25 percent to show its effect.

Gain mismatch among the interleaved ADCs generates tones in the frequency domain since the error terms are generated periodically. The tones occur at frequences of $\frac{Fs}{N} \pm F_{IN}$. The tones are the result of the product of the input frequency and ADC gain mismatch. Thus, the tones due to gain error occurs at a modulated frequency. The power of the tones can be shown to be $\frac{V_{pp}^2 {\sigma_\alpha}^2}{8}$ where ${\sigma_\alpha}^2$ is the variance of the gain and V_{pp} is the peak-to-peak voltage of the input signal [33].

The frequency domain plot in Figure 6-3 shows the effect of a 0.1% gain error on 1 ADC in a four-way interleaved ADC. The tones occur at 112.5MHz ± 10.2 MHz and 225 MHz ± 10.2 MHz.

Like offset mismatch, gain-error mismatch can also be removed in the digital domain by scaling the ADC output by the correct amount [34, 35]. The gain error can be measured by applying a full-scale sine wave or by applying the maximum input voltage. After gain error measurement, digital calibration can be used to remove this error.

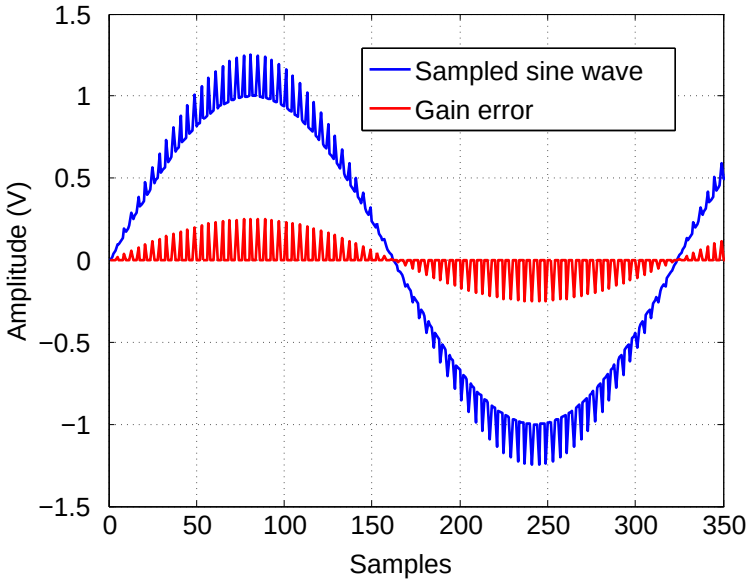


Figure 6-2: Effects of gain error on a sine wave input

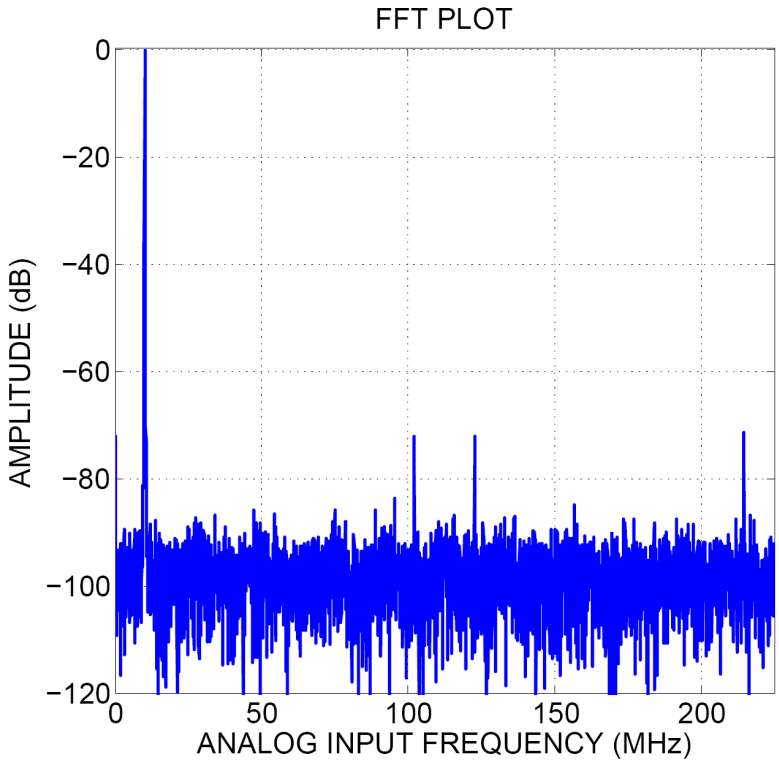


Figure 6-3: Frequency response of a 0.1% gain error in 1 ADC of a 4-way interleaved ADC

6.1.3 Timing Mismatch

In time-interleaved ADCs, timing skews between the interleaved ADCs cause errors because the sampling time is shifted from the ideal sampling time due to mismatch in sampling clock edges. The mismatches are often caused by the random mismatch of the inverters driving the sampling clocks. But its also possible to introduce systematic timing mismatches due to the asymmetric layout of the clock routing paths. In Figure 6-4, a sine wave is sampled by a time-interleaved ADC. A timing skew of ΔT of the n-th channel is shown. The amount of error resulting from timing skew can be described by the following set of equations.

$$v_{IN}(t) = A \cdot sin(2\pi ft) \tag{6.1}$$

$$\frac{dv_{IN}(t)}{dt} = 2\pi fA \cdot cos(2\pi ft) \tag{6.2}$$

$$\frac{dv_{IN}(t)}{dt}\Big|_{MAX} = 2\pi fA \tag{6.3}$$

$$v_{error,max} = \frac{dv_{IN}(t)}{dt}\Big|_{MAX} \cdot \Delta T \tag{6.4}$$

The maximum error happens when the signal is sampled near the zero crossing points, where the slope of the input signal is highest. For a skew of ΔT, the error is given by Equation 6.4. The timing skew ΔT should be minimized to reduce the skew dependent errors.

As Equation 6.4 shows, the voltage error depends on how quickly the input signal moves. The skew error term is similar compared to the gain error term since the magnitude of the error voltage depends on the input signal's amplitude. The skew error term also generates tones at frequencies of $\frac{Fs}{N} \pm F_{IN}$, which are at the same frequencies as the tones generated by gain error. The difference between the error generated by skew and gain error is that the magnitude of the error generated by skew also depends on the input frequency. The power of the tones can be shown to be $\frac{V_{pp}^2 {\sigma_s}^2 \omega^2}{8}$ where ${\sigma_s}^2$ is the variance of the skew , V_{pp} is the peak-to-peak voltage of the input signal and ω is frequency of the input signal [33].

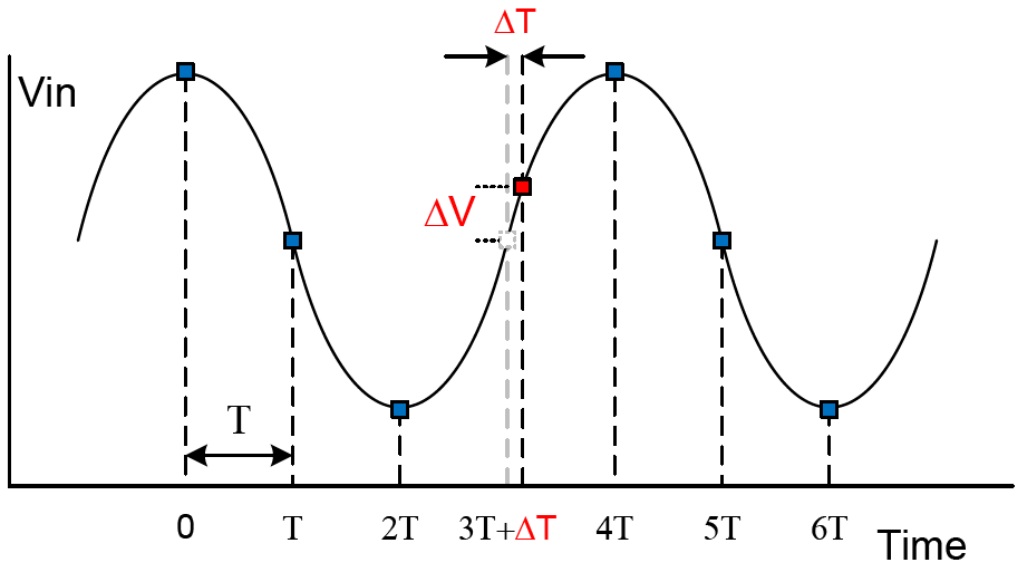


Figure 6-4: Voltage error caused by timing-skew

When the input frequency is low, the $\frac{dV}{dt}$ of the input signal is small, thus the skew-generated error term is small. This can be seen in Figure 6-5, which shows a simulated 4-way time-interleaved ADC sampling at 450MS/s. One of the four ADCs has been assigned 10 ps of skew for this simulation. When a 10.2 MHz sine wave is used as the input signal, the tones generated by skew are about 75 dB below the signal level. However, if the frequency of the input signal is increased to 201 MHz, the magnitude of the error increases proportionally. As shown in Figure 6-6, the tones generated by skew are only 50 dB below the signal level when the input frequency is 201 MHz.

It is possible to remove the effects of timing-skew through foreground calibration. The time skew can be measured and then removed by using variable delay elements in the ADC channels [36]. There are also digital background calibration techinques used to removed the effects of timing skew [37]. In addition, there are techniques to remove the timing-skew error without the need to measure the timing error [38].

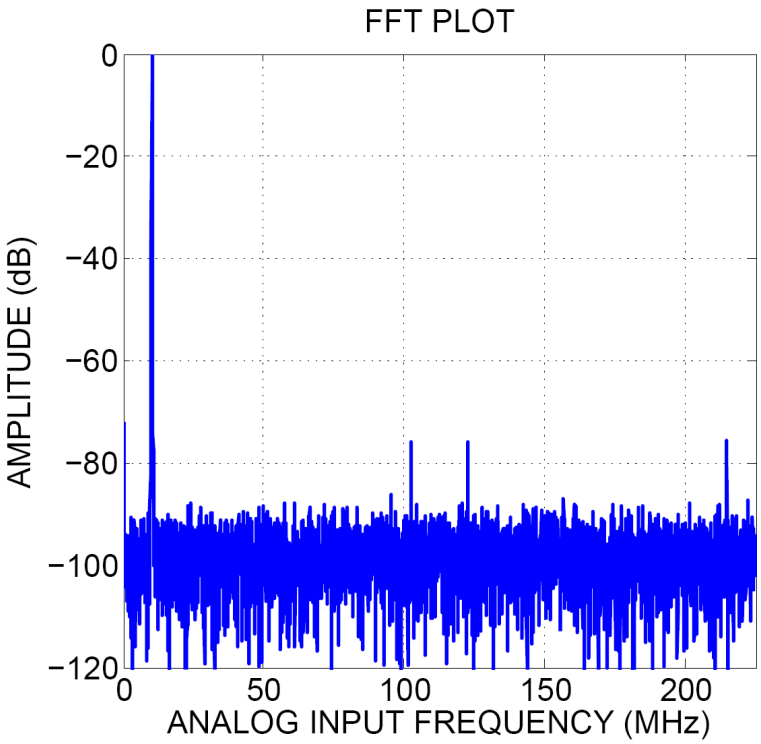


Figure 6-5: Frequency response with 10 pS skew for a 10MHz sine wave input

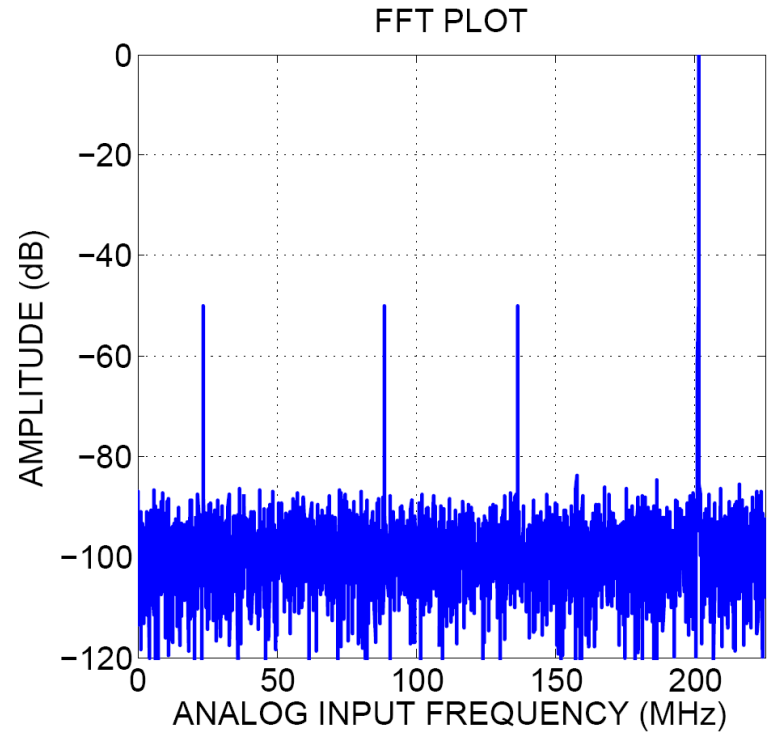


Figure 6-6: Frequency response with 10 pS skew for a 201 MHz sine wave input

6.1.4 Effects of Jitter

Jitter of the sampling clock signal will create noise in the values sampled. The uncertainty of the sampling time creates uncertainty in the voltages sampled. Jitter affects all ADCs but its effect is most limiting when the input signal is of high frequency. Many time-interleaved ADCs are designed for high frequency applications where jitter may be a dominant noise source. The effects from jitter can be calculated by using the following set of equations. σ_t is used to denote the RMS jitter of the clock source.

$$
\begin{aligned}
v_{IN}(t) &= A \cdot sin(2\pi ft) && (6.5)\\
\frac{dv_{IN}(t)}{dt} &= 2\pi fA \cdot cos(2\pi ft) && (6.6)\\
v_{error} &= \frac{dv_{IN}(t)}{dt} \cdot \Delta T && (6.7)\\
error\ power &= E[(v_{error})^2] \\
&= E[(\frac{dv_{IN}(t)}{dt})^2] \cdot E[\Delta T^2] \\
&= 2\pi^2 f^2 A^2 \cdot {\sigma_t}^2 && (6.8)\\
signal\ power &= E[(v_{IN})^2] \\
&= \frac{A^2}{2} && (6.9)\\
SNR &= \frac{1}{(2\pi f\sigma_t)^2} && (6.10)\\
SNR_{dB} &= -20log_{10}(2\pi f\sigma_t) && (6.11)
\end{aligned}
$$

As shown in Equation 6.11, the maximum achievable SNR is directly related the amount of jitter and the frequency of the input signal. In Figure 6-7, the maximum achievable SNR given certain levels of jitter is plotted. As the input frequency moves higher, jitter causes more noise and degrades the SNR.

For a given accuracy requirement, the jitter requirement can be calculated from Equation 6.11. For example, if the input signal is at 225 MHz for a 450 MS/s ADC, a RMS jitter of 565 fs is required to achieve 10.0 ENOBs if jitter is the only noise source.

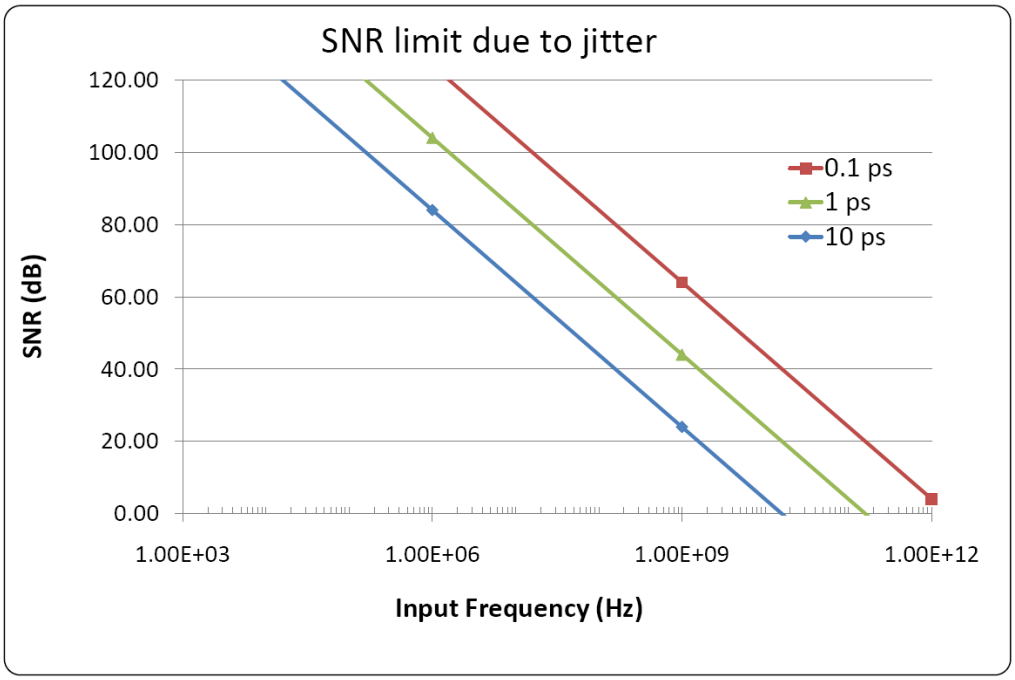


Figure 6-7: SNR limit due to clock jitter

6.2 ZCB Time Interleaved ADC

In this work, four pipelined ADCs are interleaved on a 3mm by 3mm chip. The circuit block diagram is shown in Figure 6-8. The ADCs are sampled using four non-overlapped 25 percent duty cycle clock signals. The ADCs being interleaved are the same design presented in Chapter 5, with some modifications. The accuracy of time-interleaved ADCs is limited by timing skew, gain-error mismatch, offset mismatch, and jitter [39]. The gain error and offset mismatch can be easily removed through digital calibration, but errors caused by timing skew require is more complicated to remove digitally. In this work, a skew correction circuit is added to remove the timing skew in the analog domain.

6.3 Clock Receiver and Timing Generation

A differential clocking scheme is used to supply the clock signal. A differential clock is more robust against power supply and substrate noise compared to single ended

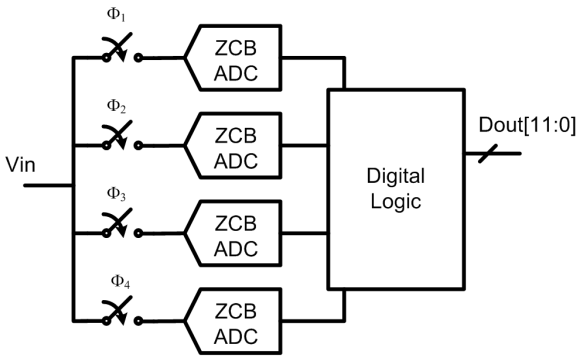


Figure 6-8: 4 Time-interleaved ADC

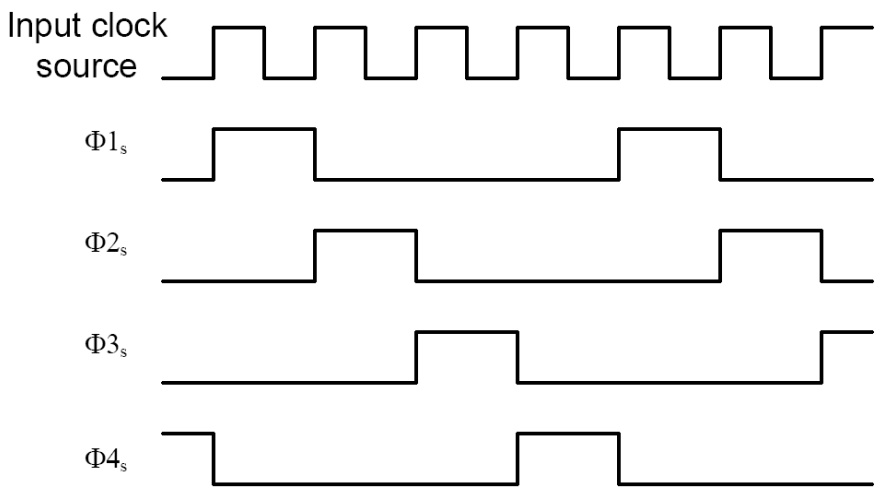


Figure 6-9: Clocks for time-interleaved sampling

signals. The input clock source used is a differential low swing signal that has a voltage swing of 200 mV peak-to-peak. A differential pair is used to convert the differential clock input to a single ended full swing signal that is used as the clock source for the ADCs.

The individual ADCs are driven with four different sets of clock signals. Shown in Figure 6-9, the signals that control the sampling switch of each ADC are non-overlapped. This guarantees that the input source only needs to drive the load of one ADC at any given time. The sampling signals, labeled Φ_s are derived from the input clock source. The digital logic used to determine the falling edge of each of the sampling signals is minimized to limit the amount of jitter and skew added by extra devices. The rising edge of the sampling clock can tolerate more skew and jitter

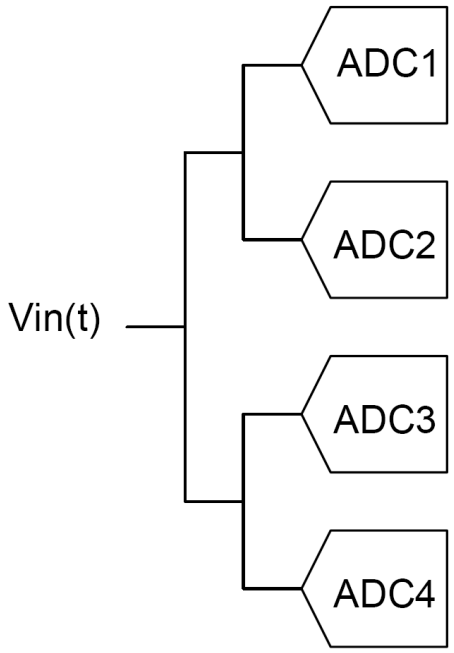


Figure 6-10: H-tree routing structure

without affecting the quality of the ADC because the final voltage is sampled on the falling edge.

The layout for the four ADCs is placed in a symmetric pattern so that the routing distance between the input source to each of the ADCs is exactly the same. The routing of the input source to each ADC must be symmetric to limit the amount of sampling-time mismatch between the ADCs. In addition, the clock routing must also be symmetric to avoid adding skew to the system. In this design, a H-tree structure shown in Figure 6-10 is used to route the input signal and the clock signals to each ADC.

6.4 Timing Skew Measurement and Correction

In this work, timing skew is first measured and then corrected by a variable delay element. To measure the timing skew, an input sine wave at the same frequency as the sampling frequency is used. The input signal and the clock signals are aligned so

that the ADC samples the zero crossing points of the sine wave. Because of timing skew, the ADCs will sample the sine wave either above or below the zero crossing. The timing-skew is calibrated such that all channels produce identical digital outputs.

To correct the timing skew, a variable delay element is added to each ADC. The circuit diagram is shown in Figure 6-11. The 8-bit R2R digital-to-analog converter (DAC) generates a control voltage that drives the gate of the NMOS switch. The capacitor is implemented using a MOS-capacitor. The resistance of the NMOS switch varies with the applied control voltage. This creates a variable RC load that is used to delay the clock signal. When the NMOS switch is completely off, the inverter's output is isolated from the capacitor. In this case, the delay is minimized. When the NMOS switch is turned on, the delay is increased since the inverter now needs to charge an additional load capacitor. The amount of delay added can range from 0 ps to 15 ps. There is 8-bit control on the DAC. However, the NMOS switch is completely off when the gate voltage is between 0 V to 0.3 V. The change in the control voltage does not affect the delay in this range. Thus, the resolution of the of variable delay element is approximately $\frac{15\ ps}{\frac{3}{4}2^8}$ which is equal to 80 fs. This is sufficient to cover the timing mismatch between the channels in this design.

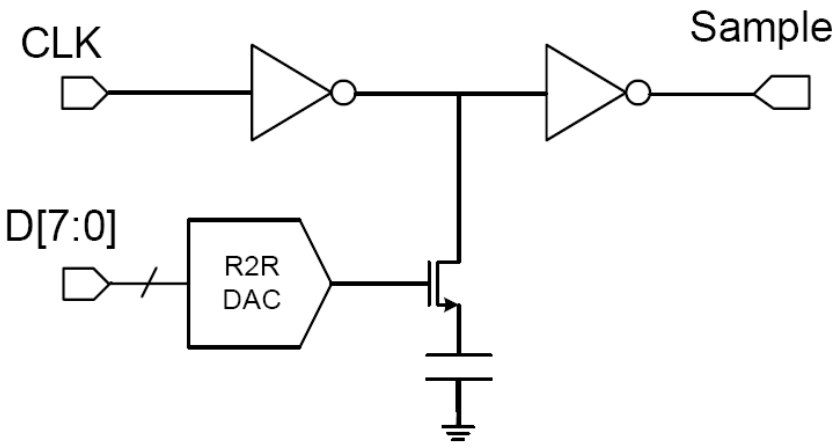


Figure 6-11: Timing skew correction circuit

6.5 Measurement Results

The single ADC achieves 9.35 ENOB for low frequency input signals and achieves 9.0 ENOB for a 211 MHz input signal. The time-interleaved ADC achieves 8.07 ENOB without calibration and achieves 8.7 ENOB after calibration. The time-interleaved ADC operates at 450 MS/s and consumes 34 mW. This ADC achieves a figure of merit of 182 fJ per conversion step. The figure of merit is defined by the following equation:

$$FOM = \frac{Power}{2 \cdot f_{in} \cdot 2^{ENOB}} \tag{6.12}$$

In Equation 6.12, f_{in} is the maximum input frequency, and ENOB is the effective number of bits calculated from the signal to noise and distortion ratio (SNDR) for a Nyquist rate input signal.

6.5.1 Single ADC Tests

The ADCs within the time-interleaved array were designed so that they can be tested individually. Although the core ADC is the same design as the ADC presented in chapter 5, there was a design error that limited the performance of this chip. Instead of thick-oxide MOS capacitors, thin-oxide MOS-capacitors were used for decoupling in the resistor ladder used to generate reference voltages for the flash ADC. The leakage currents from the MOS-capacitors were large enough to greatly change the reference values. Without the correct reference voltages on the resistor ladder, the flash ADCs' decision boundaries are shifted from the ideal points. This causes some ADC stages to go out of range of the digital correction. The saturation of some ADC stages greatly increases non-linearity as can be seen in the INL and DNL plots in Figure 6-12.

The amount of leakage current through the gate oxide of a MOS-capacitor is voltage dependent. Reducing the gate voltage reduces the leakage current exponentially.

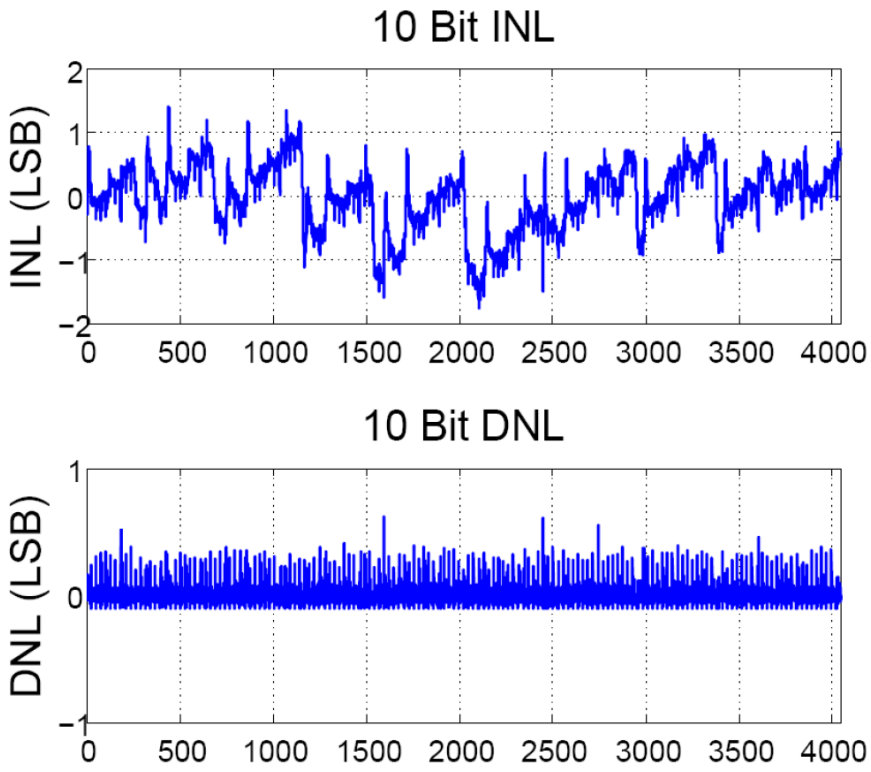


Figure 6-12: ADC INL and DNL test for 112.5 MHz sampling frequency

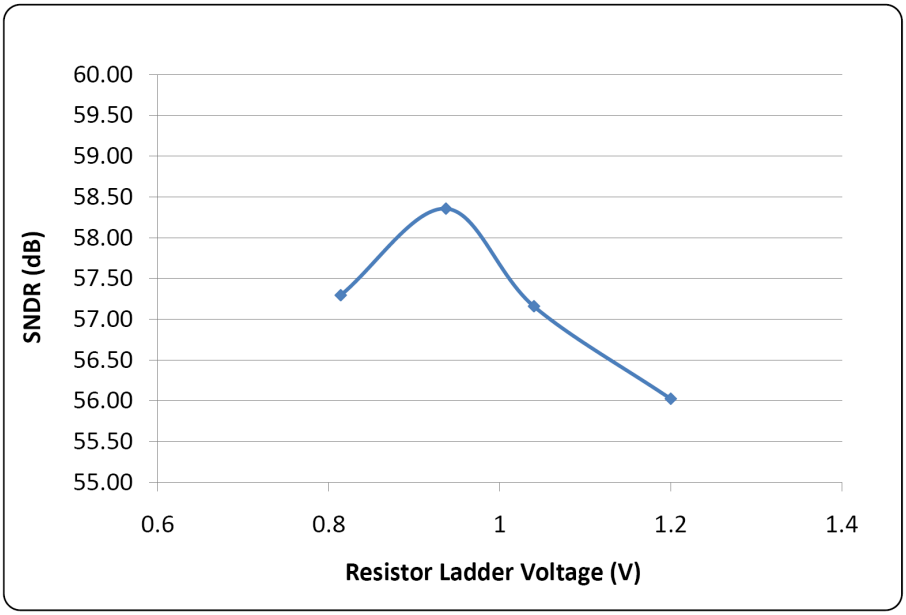


Figure 6-13: ADC SNDR vs resistor ladder voltage

In the measurement, the resistor ladder and reference voltages were lowered to reduce reference voltage errors due to leakage. The resistor ladder is designed nominally for 1.2V. With reduced voltage for the resistor ladder, the SNDR of the ADC improves. However, as we lower the resistor ladder voltage below 0.9 V the SNDR decreases because higher voltage is required by the comparator and the reference voltage switches. The reference switches connect to V_{ref+} are implemented using PMOS transistors. As V_{ref+} is lowered, the resistance through the switches increases. The increase in the resistance in the reference switches is undesirable since it may prevent the reference voltage used in the MDAC from settling accurately. In addition, the lower reference voltages lowers the common-mode level to the input of the flash ADC comparator. This can cause a significant amount of offset in the comparator which makes non-linearity worse. The plot of the ADC SNDR versus the resistor ladder voltage is shown in Figure 6-13.

Figure 6-14 shows the FFT plot of a single ADC in the time-interleaved array operating at 112.5 MS/s. The input signal is a 10 MHz sine wave. The other ADCs in the interleaved array are active during this measurement. For this low frequency signal, the ADC achieves 9.4 ENOB.

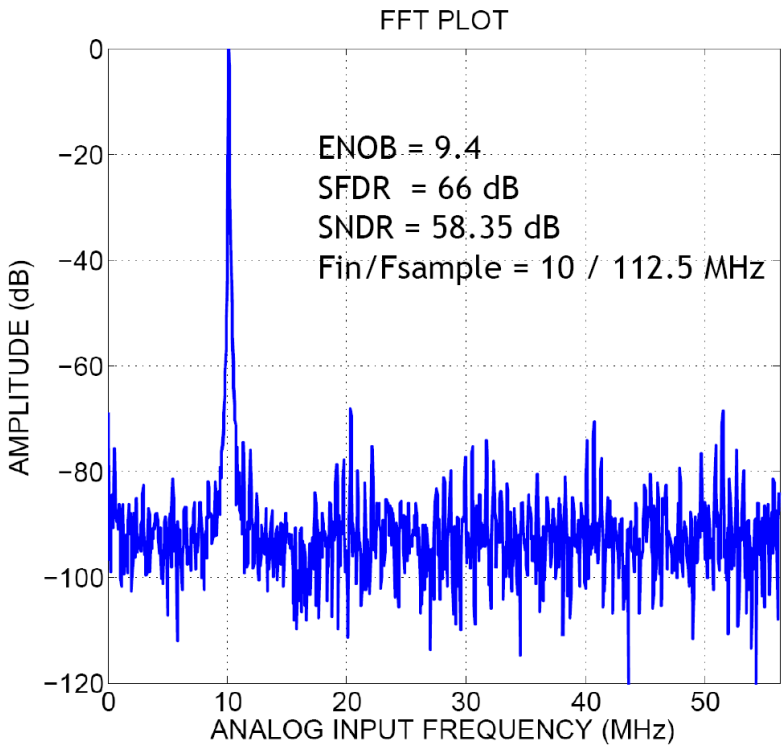


Figure 6-14: FFT with a 10 MHz sine wave input for single ADC

Figure 6-15 shows the FFT plot when the ADC is driven with a 211.5 MHz sine wave. Since the input signal is of higher frequency compared to the sampling frequency of each individual ADC, the signal is aliased down to 13.5 MHz as shown in the FFT plot. At this input frequency, the ADC achieves 9.0 ENOB. The degradation in the ENOB at higher input frequency is believed to be due to a combination of jitter from the clock generating equipment and the increased distortion in the sampling network.

6.5.2 Time-Interleaved Testing

The time-interleaved ADC samples at 450 MS/s. The ADC is driven with a low swing differential clock signal. A band-pass filter is added at the output of the signal generator to eliminate the harmonics of the source.

To facilitate the recording of the digital data, each ADC is connected to a dedicated on-chip SRAM block. The SRAM controller has two modes of operation: read

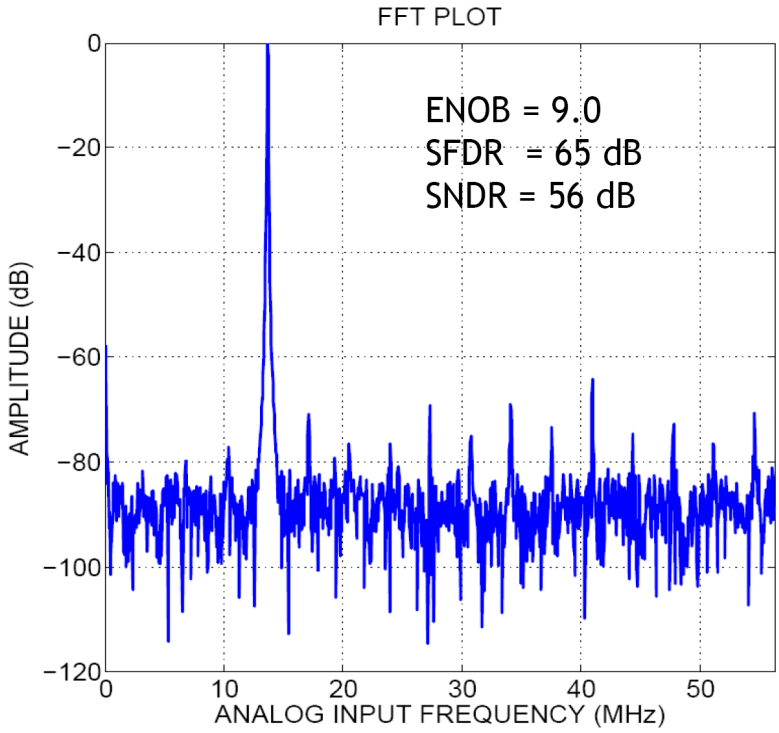


Figure 6-15: FFT with a 211 MHz sine wave input for single ADC

mode and write mode. During the write mode, the ADC continuously writes to the SRAM. The ADC data is overwritten periodically. During the read mode, data stored in the SRAMs are read out in sequence since the output pins are shared by the SRAMs.

Figure 6-16 shows the FFT plot of the time-interleaved ADC when driven with a 211 MHz input signal. Without any calibration, the ADC achieves 8.07 ENOB. The Tones at 112.5 MHz and 250 MHz are due to offset mismatch between the ADCs. The tones generated by timing-skew and gain error occur at 14 MHz, 98.5 MHz, and 126.5 MHz. The second harmonic of the ADC is aliased to 28 MHz and the third harmonic occurs at 183 MHz.

The offset for each ADC is measured with a 0 DC input voltage. The measured offset error was then subtracted out in the digital domain. The gain error is measured by comparing the ADCs' outputs when driven with a full scale sine wave input. Gain error is also corrected in the digital domain by scaling the ADC's output by the appropriate gain factor.

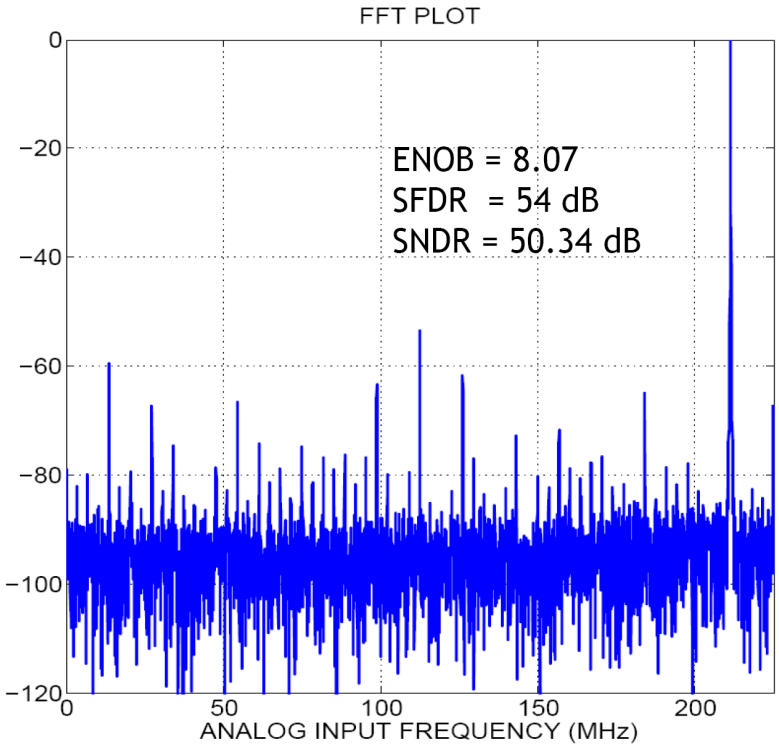


Figure 6-16: Measurement results of the time-interleaved ADC without calibration

The timing skew is measured by driving the ADC with a sine wave that is of the same frequency as the sampling clock. The sine wave and the sampling clock are phase aligned so that the ADC samples the zero-crossing point of the sine-wave. In the ideal case with no skew, every ADC samples exactly at the zero-crossing instant. However, due to timing skew between the ADCs' sampling clock signals, the sample may be taken too early or too late. Thus the sampled values that deviate from zero are due to skew. The ADCs sampling clock edge is adjusted using a variable delay element. The ADCs are calibrated so that all of the ADCs sample the zero-crossing point.

Figure 6-17 shows the measurement results after calibration. The SNDR improved from 50.34 dB to 54.2 dB. The effective number of bits with a 211 MHz input signal is 8.7. The time-interleaved ADC achieves an SFDR of 61 dB.

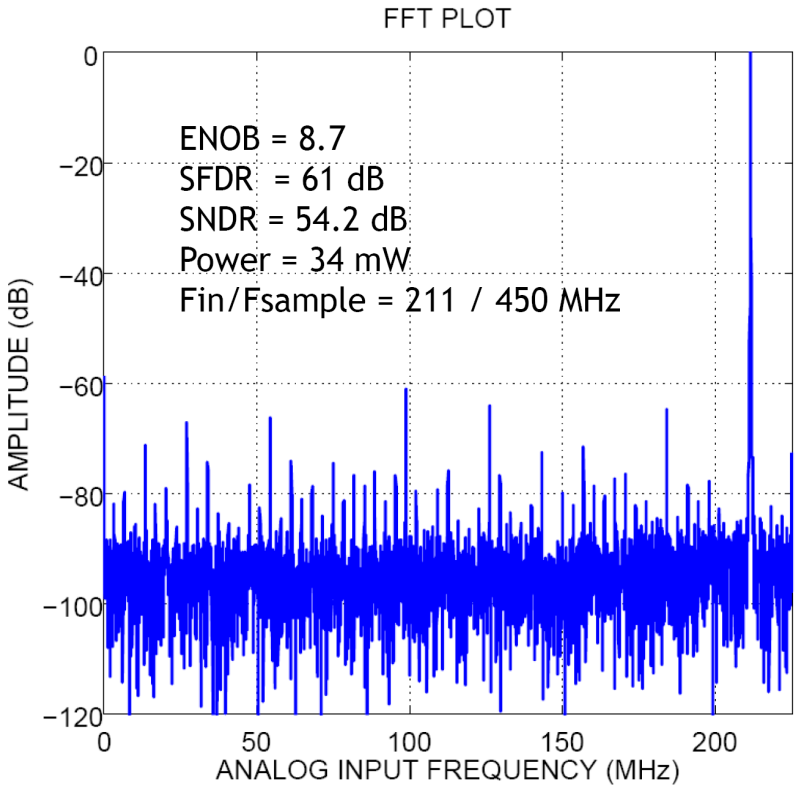


Figure 6-17: Measurement results of the time-interleaved ADC after calibration

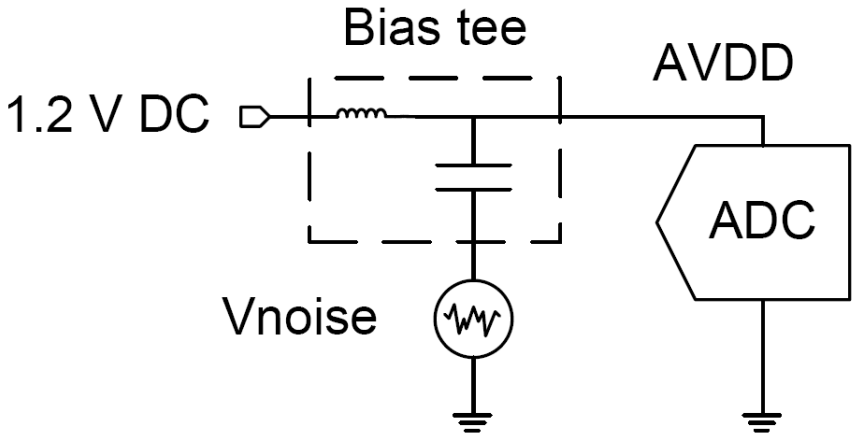


Figure 6-18: ADC power supply rejection test setup

6.5.3 Power Supply Rejection Measurement

Earlier works in zero-crossing based circuits were implemented using single ended topologies [3,9]. However, they have been found to be sensitive to power supply noise and substrate noise [3]. The differential implementation of zero-crossing based ADCs has been shown to be more robust to substrate noise [4, 10].

The power supply rejection of this time-interleaved ADC was measured by injecting noise onto the power supply. As shown in Figure 6-18, a bias tee is used to add noise onto the analog V_{DD} of the ADC. The bias tee uses an inductor to isolate the DC bias voltage. This allows noise or other signals to be AC coupled onto the power supply. An active probe was used to measure the amplitude of the power supply noise at the ADC. The on-chip bypass capacitor does not filter out the low frequency noise added.

A Tektronix AFG3102 arbitrary waveform generator was used to generate a noise signal with 25 MHz bandwidth. The degradation in the ADC SNR is shown in Figure 6-19. The ADC performance is also tested when a sine wave is added onto the analog power supply voltage. As the amplitude of the sine wave increases, the ADC performance decreases.

From the amount of decrease in the ADC SNDR, the power supply rejection ratio can be calculated. The power supply rejection ratio for an ADC is defined as

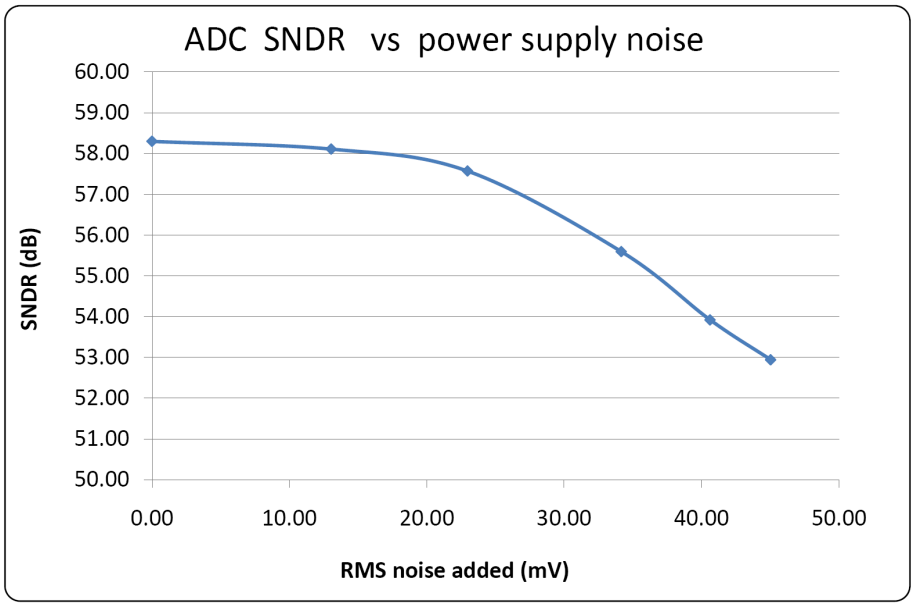


Figure 6-19: ADC test with added power supply noise

$$PSRR = \frac{added\ power\ supply\ noise}{added\ input\ referred\ noise}. \tag{6.13}$$

Without any noise added, the ADC achieves an SNDR of 58.3 dB. When there is a 34 mV RMS noise added with 25 MHz bandwidth, the ADC SNDR degrades to 55.5 dB. The added input-referred noise power can be calculated by taking the total noise present when the SNDR is at 55.5 dB and subtracting out the noise that was already present in the ADC without the additional power supply noise. By taking the ratio of added power supply noise to the added input-referred noise, the PSRR is computed. For this case, the measured ADC PSRR is 32 dB. The ADC shows similar levels of PSRR when a sinusoid voltage is added to the power supply. The measurements for the 3MHz test and the 27 MHz test are shown in Figures 6-20 and 6-21.

The poor PSRR performance may be due to the asymmetries in the ZCD. The gain stages following differential pair in the ZCD are single-ended circuits and are sensitive to power supply and substrate noise. To improve the PSRR performance, differential

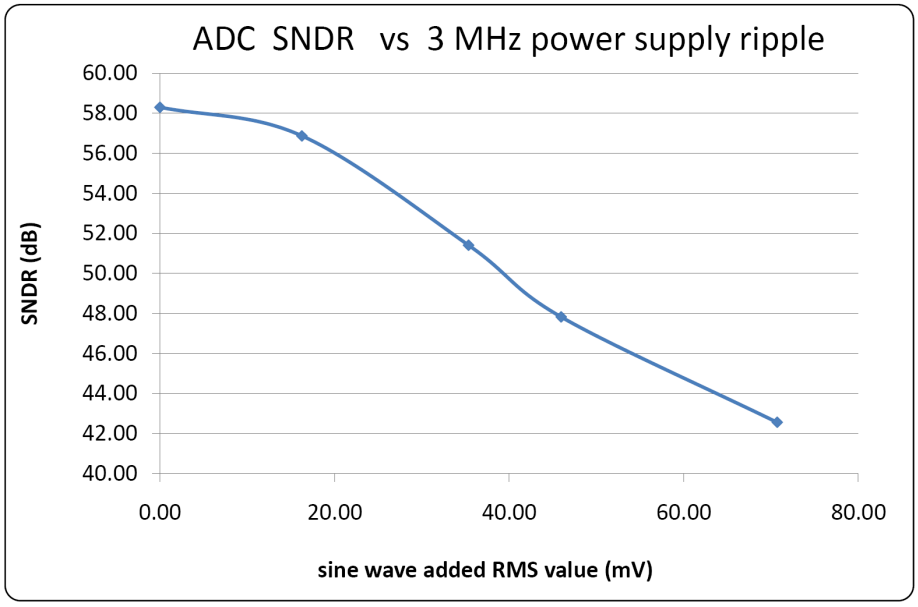


Figure 6-20: ADC test with added 3 MHz power supply ripple

gain stages should be used instead. Also, additional local decoupling capacitors close to the ZCD should be added to reduce the ripple on the power supply.

6.6 Summary

Power consumption is a key design parameter in many different SoCs, especially in mobile applications. The zero-crossing based ADC is a highly power efficient circuit structure. By time-interleaving multiple zero-crossing based ADC, their power efficiency can be exploited to achieve very high sampling rates without using a lot of power. This time-interleaved ADC achieves 8.7 ENOB with 450MS/s sampling rate while consuming only 34.2 mW of power. The power efficiency of this design is compared to other published works in figure 6-22.

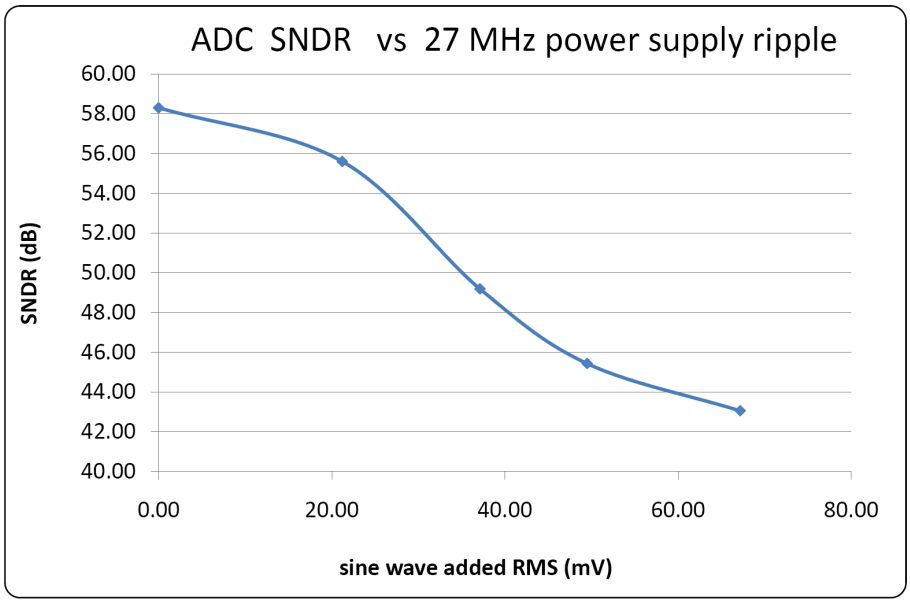


Figure 6-21: ADC test with added 27 MHz power supply ripple

Figure of merit comparison

Author	ADC Type	Fsample	ENOB	FOM (fJ/step)
Geelen, ISSCC 2004	TI-Folding	600 MS/s	7.5	2800
Gupta, ISSCC 2006	TI-Pipelined	1 GS/s	8.4	740
Hsu, ISSCC 2007	TI-Pipelined	800 MS/s	8.7	1060
Tu, VLSI 2008	TI-Pipelined	800 MS/s	7.06	285
This Work	TI-ZCB Pipelined	450MS/s	8.7	182

* Select ADCs with ≥ 400 MS/s , ENOB ≥ 7 are included for comparison

Figure 6-22: Figure of merit comparison table

Chapter 7

Conclusion

7.1 Conclusions

A differential zero-crossing based pipelined ADC and a time-interleaved zero-crossing based ADC have been presented. The pipelined ADC, which has 10.2 ENOB at 100 MS/s, achieves a figure of merit of 53 fJ per step. The time-interleaved ADC achieves 8.7 ENOB at 450 MS/s and achieves a figure of merit of 182 fJ per step. The ADCs achieve very good figure of merits, demonstrating the power efficiency of the zero-crossing based architecture. The figure of merit achieved has shown that zero-crossing based switched-capacitor circuits are more power efficient compared to op-amp based switched-capacitor circuits.

7.2 Thesis Contributions

In this work, we have designed very power efficient pipelined ADCs without the use of op-amps and feedback. There have been many circuit level improvements to the performance ZCBC. The dynamic bias current source has been shown to be a possible method to improve ramp rate linearity in ZCBC. The reference pre-charging was also used to reduce the disturbance on the ADC reference voltages. In the first design, DBGE was applied to remove the systematic mismatch. This was this first hardware application of DBGE. This ZCB ADC achieved a figure of merit of 53 fJ per conversion

step. This FOM was the best figure of merit in published pipelined ADCs with over 100 MS/s and over 10 ENOB at the time of publication. In addition, the zero-crossing technique was leveraged to design a very power efficient ZCB ADC that achieves 8.7 ENOB at 450 MS/s. The figure of merit of the time-interleaved ADC was 182 fJ per step.

7.3 Future Work

Although the zero-crossing circuits have shown impressive results, there are still many opportunities for improvement. The ZCBC architecture in this work and in previous works require manual tuning for optimal circuit operation. For example, the overshoot voltage which depends on the speed of operation causes a large offset for each ADC stage. This offset must be canceled so that this offset does not saturate the later stages. In addition, the ramp rate must be adjusted according to the operation speed. If there is a mismatch between the PMOS current sources and the NMOS current sources, there will be a common-mode drift in the charge transfer operation. The common-mode drift does not disturb the differential signal directly, but it creates an undesired non-linearity in the following stage due to the finite common-mode rejection of the ZCD. It would be ideal to automate this process to make the circuit more robust to process, temperature, and voltage variations.

7.3.1 Cancellation of the Overshoot Voltage

The overshoot voltage is inherent to the ZCBC architecture. Especially in the single phase ZCBC designs, overshoot voltage may be large and needs to be removed. The offset cancellation does not need to be perfect since any residual overshoot will become a tolerably small input-referred offset.

A possible overshoot cancellation scheme is presented in a previous ZCBC work [40]. The zero-crossing detector is configured to measure the overshoot voltage during the half of the clock cycle that it is not needed. The overshoot voltage is then stored on a capacitor to be used in the charge transfer phase. However, the method used

requires extra switches at the virtual ground node. The added parasitic effects will degrade the ADC's linearity and add additional noise. The switches at the virtual ground node add signal-dependent charge injection that may not be canceled perfectly by dummy switches. The extra switches at the virtual ground node also adds its own thermal noise. In addition, the added parastics at the virtual ground node increases the noise transfer function from the ZCD [2]. This technique is well suited for 8-bit resolution or lower. However, a better automated overshoot cancellation scheme is needed for ADCs with higher resolutions.

7.3.2 Current Source Value and Scalability

For a zero-crossing based ADC, one of the key bias conditions that needs to be set is the current source values. The current value should be set so that the ramp is able to sweep the entire output range before the end of the clock cycle. If the current value is too low, the ramp will not be able to sweep through all of the possible output values. However, if the current value is increased beyond what is required, the ramp will be faster, thus the overshoot voltage will be larger. The larger overshoot introduces more non-linearity to the ADC. This is also undesirable. For a given clock period, there is an optimal current value. It would be useful to have some additional circuitry used to automatically generate the ideal current value.

In addition, some ADCs are used in applications where the sampling frequency can change. In this case, each time after a change in the sampling frequency, the current source values should be automatically readjusted to accommodate the change in the sampling frequency. At lower sampling frequencies, lower current is required to maintain the circuit operation while at higher sampling frequency, more current is needed.

7.3.3 Current Source Linearity

The key limitation to the linearity of ZCBC is the delay of the zero-crossing detector and the linearity of the ramp generated by the current source. A fast ZCD is desired

for linearity, but it comes at the cost of more power. With a more linear current source, the bandwidth and power requirement of the ZCD can be relaxed. It may be useful to use local feedback to generate linear ramps. In doing so, high resolution zero-crossing based ADCs can be achieved.

7.3.4 Hybrid Structures

There have been many recent publications of new ADC structures made by combining traditional ADC architectures [7, 41, 42]. For example, in [7], ZCBC, op-amps, and the Correlated Level Shifting (CLS) technique was combined to build a pipelined ADC. By combining different ADC architectures, their strengths can be leveraged to achieve higher performance and power efficiency. There may be other interesting combinations of other ADC topologies that could incorporate zero-crossing based circuits to create very power efficient ADCs.

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Appendix A

ADC Test Setup

The ADC test setup is an important part to getting accurate measurement results. In this section, the ADC test setup used and the circuit blocks used on the PCB will be described.

A.1 Overview

After the chip is fabricated, the first step is to select a suitable package. To minimize the parasitic inductance of the package, QFN packages were used for both chips. The die can be placed off-center in the package to minimize the inductance for critical signals. For example, it is advantageous to minimize the inductance to the reference voltage pins.

Regulators should be used to generated the power supplys for ADCs. Linear regulators help to ensure that the power supply to the ADC is clean. Separate regulators should be used to generated different power supplies. The separation of the digital power supply and the analog power supply ensures that noise coupling between the two is minimized.

There is an on-chip shift register that stores the configuration bits used by the ADC to set various bias voltages and bias currents. During start-up, a data sequence is shifted into the shift registor. In this test setup, an FPGA is used to generate the data pattern.

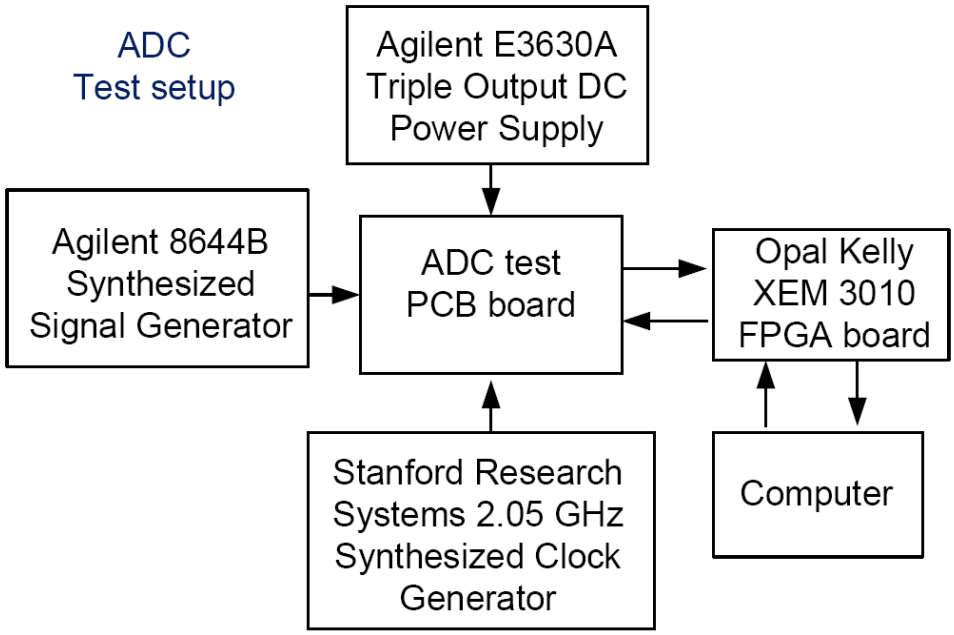

Figure A-1: ADC evaluation test setup

The input source was generated by a arbitrary wave-form generator. This single ended input signal is transformed into a differential input signal for the ADC by a balun. The Stanford Research Systems Model CG 635 2.05 GHz Synthesized Clock generator was used as the clock source. A block diagram of the test setup is shown in figure A-1. A band-pass filter is used at the output of the signal generator to improve the signal's linearity.

A.2 Power Supply Generation Circuit

The power supply used is generated using the LT3021 regulator from Linear Technology. This linear regular uses an internal 200 mV reference voltage to generate the appropriate output voltage. The feedback loop of the regulator forces the voltage of "SENSE" node to 200 mV. The output voltage is then set by the ratio of R1 and R2. R1 can be made to be a variable resistor in order to allow chages to the power supply voltage. A 10 μF capacitor is added at the input of each regulator to reduce the ripple from power supply noise. A 3.3 μF capacitor is added at the output of the

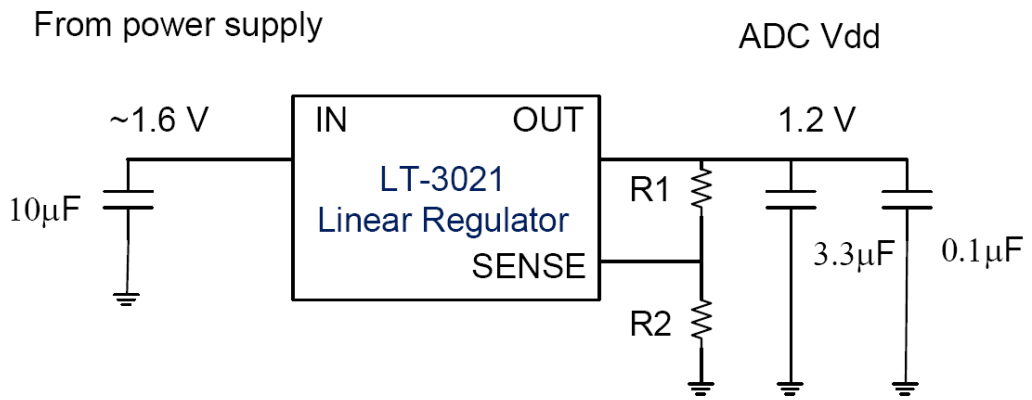

Figure A-2: Power supply generation

regulator to ensure stability. An additional 100 nF capacitor is added at the output of the regulator to reduce high frequency noise.

There are multiple regulators used on the PCB to isolate the different power supplies. This prevents noise from coupling from one to another and it faciliates the measurement of power consumption.

A.3 Input Signal

The input signal can be generated using an arbitrary wave-form generator. A band-pass filter is required at the desired frequency to eliminate the harmonics from the signal generator. Two back-to-back baluns are used to transform the single-ended signal from the signal generator to a differential signal [43]. The use of two baluns helps to reduce the second order distortion caused by the baluns.

A.4 Digital Processing

The Opal Kelly XEM3010 FPGA board is used as a digital interface to the ADC test chip. The FPGA implements a state machine that programs the test chip and acquires the digital data from the on-chip SRAM. The xilinx core generator software was used to synthesize a FIFO using the on-chip block-ram to store the ADC data.

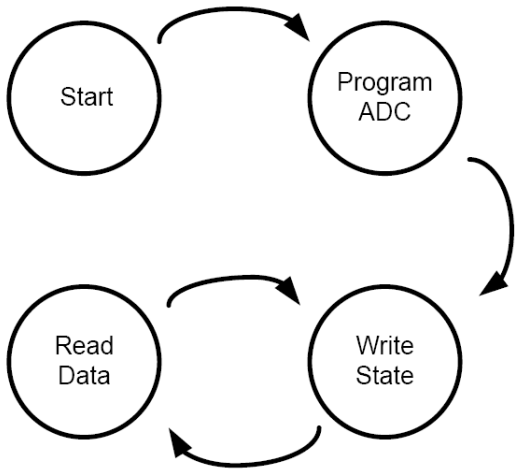

Figure A-3: State diagram for the digital control interface

The state diagram shown in Figure A-3 describes the state machine of the digital interface.

Upon startup, the FPGA reads a text file from the computer containing the configuration bits. The FPGA then generates the data pattern to input the configuration bits into the ADC chip's on-chip shift register. After the completion of this sequence, the ADC's SRAM controller is put into WRITE mode where the SRAM continously writes ADC data into its SRAM cells. The clock signal used by the SRAM and SRAM controller is generated from the ADC so that the operation of writing into the SRAM is synchronized with the ADC. The address for the SRAM is generated using a simple counter. As the counter reaches the maximum value, it simply loops around to 0 so that the writing is continous.

During the read mode, the FPGA generates a clock signal that drives the SRAM circuit to acquire the data from the SRAM. The ADC code is read from the SRAM and stored on the computer for further processing.

Appendix B

Matlab Time-interleaved ADC simulator

In the design of a time-interleaved ADC system, the effects of offset, gain, and timing skew errors are often the limiting factors in performance. It is useful to know how much mismatch can be tolerated for a given design target.

The sections decribes a matlab applet that can be used to simulate effects of offset, gain, and skew mismatch in time-interleaved ADCs. Four ADCs are used in this simulation but the code can be adjusted to simulate other numbers of time-interleaved ADCs.

B.1 User interface

The user interface for the applet is shown in Figure B-1. There are parameters that can be used to adjust the amount of mismatch between the ADCs. The "PLOT!" button plots the FFT given a sine wave input. The applet also computes the effective number of bits based on the SNDR. The sampling frequency can be set by changing the number in the "Fsample" box. The input frequency box "Fin" sets the frequency of the input sine wave.

The resolution of the ADCs is set by changing the field labeled "N bit"'. Changing the resolution of the ADC will change the noise floor due to quantization. Given the

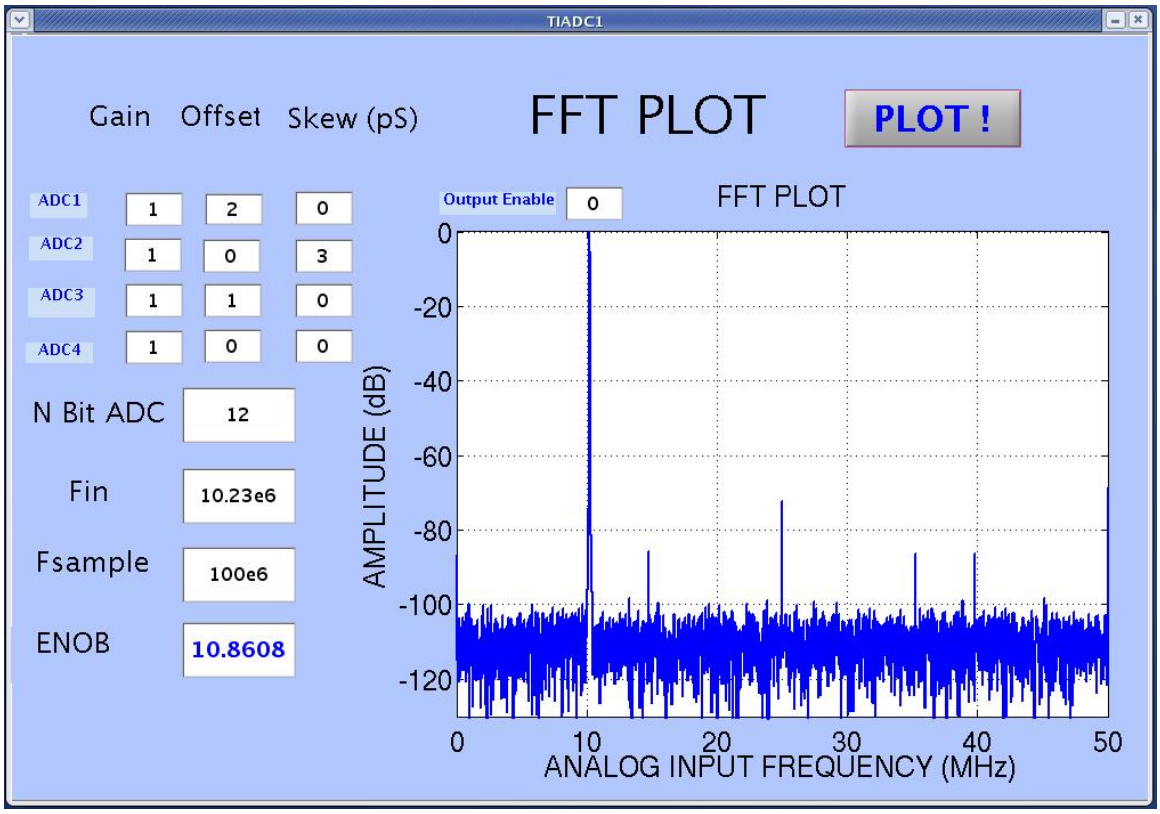

Figure B-1: Time-interleaved ADC mismatch simulator

level of quantization, the offset parameter can be set for each ADC. The units of the offset is 1 LSB. However, fractional LSB offset is also acceptable.

The gain of each ADC is nominally 1.0 . To simulate a 0.1% mismatch in ADC 3, the gain parameter of ADC 3 should be set to 1.001.

The timing skew paramter can be used to set the skew for each ADC channel. The units are in pico seconds. In the case with no skew, the four skew paramters should be set to 0.

This applet can be a useful tool for estimating the effects of mismatch in a time-interleaved ADC. It could be used in design to determine the matching requirements between various ADCs.

B.2 Matlab code

The following matlab code is used to generate the matlab applet. The code can be generated using matlab's applet functions. The core part of the code is included for reference.

```
function varargout = TIADC1(varargin)

%The default matlab code has been omitted

o1 = str2double(get(handles.offset1,'String'));
o2 = str2num(get(handles.offset2,'String'));
o3 = str2num(get(handles.offset3,'String'));
o4 = str2num(get(handles.offset4,'String'));

g1 = str2num(get(handles.gain1,'String'));
g2 = str2num(get(handles.gain2,'String'));
g3 = str2num(get(handles.gain3,'String'));
g4 = str2num(get(handles.gain4,'String'));

s1 = str2num(get(handles.skew1,'String'));
s2 = str2num(get(handles.skew2,'String'));
s3 = str2num(get(handles.skew3,'String'));
s4 = str2num(get(handles.skew4,'String'));

N = str2num(get(handles.N,'String'));
fin = str2num(get(handles.fin,'String'));
fsample= str2num(get(handles.fsample,'String'));
Tsample=1/fsample;
tstart=1/fsample*0.5+5e-12; %*rand()


t=[1:2048]*Tsample*4 + tstart; %tstarts samples the sinewave at a different point ↩
    each time
tc=[1:8192]*Tsample+tstart;
t1= t+s1*1e-12;
t2= t+Tsample+s2*1e-12;
t3= t+2*Tsample+s3*1e-12;
t4= t+3*Tsample+s4*1e-12;

data1=g1*sin(2*pi*fin*t1)+o1*2/(2^N);
data2=g2*sin(2*pi*fin*t2)+o2*2/(2^N);
data3=g3*sin(2*pi*fin*t3)+o3*2/(2^N);
```

```
data4=g4*sin(2*pi*fin*t4)+o4*2/(2^N);

datac=ones(length(data1)*4,1);

for i=1:length(datac)
    cycle= ceil(i/4);
    if mod(i,4) == 1
        datac(i)=data1(cycle);
    elseif mod(i,4)==2
        datac(i)=data2(cycle);
    elseif mod(i,4)==3
        datac(i)=data3(cycle);
    else
        datac(i)=data4(cycle);
    end
end

% Quantize datac
datac=floor((datac+1)/(2/2^N));
numpt = length(datac);

fsample=fsample/1e6; %% X axis is already in MHz

[Dout_dB, myENOB] = computeffth(datac'-mean(datac),fsample);

flag1 = str2num(get(handles.edit20,'String'));

fclk=fsample;
axis([0, fsample/2, -130, 0]);
axes(handles.axes1)
axis([0, fsample/2, -130, 0]);
maxdB=max(Dout_dB(1:numpt/2));

%For TTIMD, use the following short routine, normalized to ?6.5dB full-scale.
%plot([0:numpt/2-1].*fclk/numpt,Dout_dB(1:numpt/2)-maxdB-6.5);
set(gca,'Fontsize',18);
plot([0:numpt/2-1].*fclk/numpt,Dout_dB(1:numpt/2)-maxdB, 'LineWidth', 2);
%plot([0:numpt-1].*fclk/numpt,Dout_dB(1:numpt)-maxdB);
grid on;
axis([0, fsample/2, -130, 0]);
title('FFT PLOT', 'Fontsize',18);
xlabel('ANALOG INPUT FREQUENCY (MHz)', 'Fontsize',18);
ylabel('AMPLITUDE (dB)', 'Fontsize',18);

set(handles.enob,'String',myENOB);
```

```
if (flag1 > 0)
    plotfffth(datac'-mean(datac),fsample);
%plotfffth is a function which i wrote to plot the fft of the data

guidata(hObject, handles);
end
```

Appendix C

Noise Bandwidth Calculation

This chapter of the Appendix covers the noise bandwidth calculation for low-pass and bandpass transfer functions.

C.1 Overview

For the noise transfer function(NTF) of this amplifier, the output referred noise can be calculated by using Equation C.1 [15]. In this Equation, N is the input-referred noise spectral density.

$$\begin{aligned} {v_o}^2 &= \frac{1}{2\pi}\int_0^\infty N|H(\omega)|^2 d\omega \\ &= \frac{N}{2\pi}\int_0^\infty |H(\omega)|^2 d\omega \end{aligned} \tag{C.1}$$

It is useful to know the result of the integral in Equation C.1 so that the output-referred noise can be computed quickly. It is possible to use tools such as MATLAB or MathCad to evaluate the integral; but sometimes, an analytic solution is desired. In the following sections, the Cauchy Residue Theorem is applied to evaluate the integral for lowpass and bandpass transfer functions.

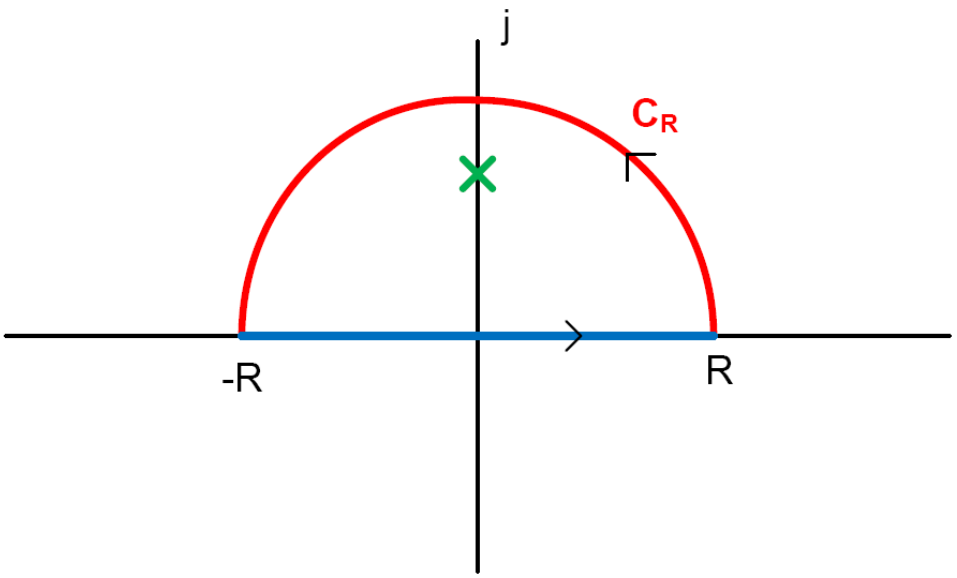

Figure C-1: Contour integral

C.2 Cauchy Residue Theorem

The Cauchy's Residue Theorem can be used to evaluate the integral to compute the noise bandwidth. In all real circuits, there are more poles than zeros, thus the transfer function will always approach 0 for very high frequencies. And the integral of the noise bandwidth will converge to a finite number.

The Cauchy Residue Theorem states that for a simple closed contour C, if the function f is analytic inside and on C except for a finite number of singular points $z_1, z_2, ..., z_n$ inside C, then the contour integral of f on C is equal to $2\pi i$ times the sum of the residues of f within the contour C [44]. The residue of the function f(z) is the coefficient of the 1/z term in the Laurent series expansion of f(z).

$$\int_C f(z)dz \quad = \quad 2\pi j \sum_{k=1}^{n} Res f(z) \ at \ z{=}z_k \tag{C.2}$$

The contour integral of f(z) along the contour C can be written as the sum of the integral of f(z) along the blue line and the the integral on the red line as shown in Figure C-1.

$$\int_C f(z)dz \;=\; \int_{-R}^{R} f(z)dz + \int_{C_R} f(z)dz \tag{C.3}$$

As we take the limit as R goes to ∞, $\int_{-R}^{R} f(z)dz$ is equal to $\int_{-\infty}^{\infty} f(x)dx$. And the $\int_{C_R} f(z)dz$ term goes to 0 as R approaches ∞ if the circuits transfer function that we are integrating has more poles than zeros.

The residue of f(z) can be computed using a theorem 69.2 from the Complex Variables and Applications [44], which states that if f(z)= g(z)/h(z), and f(z) has a singularity at z_0, and h'(z_0) $\neq 0$, then the residue of f(z) at z_0 is given by

$$\textit{Res f(z) at } z{=}z_0 \;=\; g\left(z_0\right)/h'\left(z_0\right) \tag{C.4}$$

By computing the residues of f(z), we can evaluate the contour integral $\int_C f(z)dz$ by the Cauchy residue theorem. And the integral $\int_{-\infty}^{\infty} f(x)dx$ is equal to $\int_C f(z)dz$. Since we are integrating $|H\left(\omega\right)^2|$, the function f(x) will be even, thus $\int_0^{\infty} f(x)dx$ will be equal to $\frac{1}{2}\int_{-\infty}^{\infty} f(x)dx$.

C.3 Example Calculations

In this section, the noise bandwidth calcuation is done for a low pass transfer function and a bandpass transfer function.

C.3.1 Low-Pass Transfer Function

The R-C network shown in Figure C-2 has a low pass transfer function which is given by $\frac{1}{1+j\omega RC}$. And the output noise power is given by Equation C.5. The $\frac{1}{2\pi}$ factor is used to convert the Radians to Hertz. The resistor has a voltage noise spectral density is given by 4kTR [16].

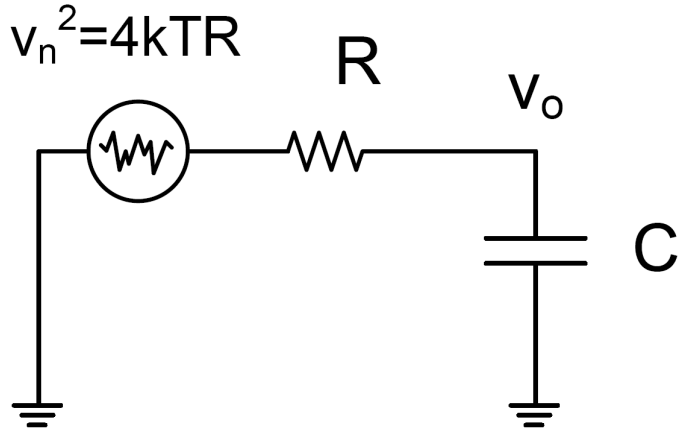

Figure C-2: RC circuit

$$
\begin{aligned}
{v_o}^2 &= \frac{1}{2\pi}\int_0^\infty 4kTR\left|\frac{1}{1+j\omega RC}\right|^2 d\omega \\
&= \frac{4kTR}{2\pi}\int_0^\infty \frac{1}{1+(RC)^2\omega^2} d\omega
\end{aligned}
\tag{C.5}
$$

To evaluate this integral, f(z) is defined to be $\frac{1}{1+(RC)^2 z^2}$. The singularities of f(z) are located at $\omega = \pm j/RC$. Thus, if we draw a contour C that is the same shape as the contour shown in Figure C-1, the singularity located at $\omega = j/RC$ will be enclosed by C.

The residue at this point can be computed by using Equation C.4. f(z) can be written as g(z)/h(z) where g(z)=1 and h(z) $= 1 + (RC)^2 z^2$. And h'(z) is equal to $2(RC)^2 z$.

$$
\begin{aligned}
\textit{Res f(z) at } j/RC &= \frac{g(j/RC)}{h'(j/RC)} \\
&= \frac{1}{j2RC}
\end{aligned}
\tag{C.6}
$$

Now we can apply Cauchy's Residue Theorem:

$$\begin{aligned}\int_C f(z)dz &= 2\pi j \cdot \ Res\ f(z)\ at\ j/RC \\ &= \frac{2\pi j}{j2RC} \\ &= \frac{\pi}{RC}.\end{aligned} \tag{C.7}$$

Thus , it follows that

$$\int_{-\infty}^{\infty} f(x)dx = \frac{\pi}{RC} \tag{C.8}$$

$$\int_{0}^{\infty} f(x)dx = \frac{\pi}{2}\frac{1}{RC}. \tag{C.9}$$

The total noise power at the output can now be computed.

$$\begin{aligned}{v_o}^2 &= \frac{1}{2\pi}\int_0^\infty 4kTR|\frac{1}{1+j\omega RC}|^2 d\omega \\ &= \frac{4kTR}{2\pi}\int_0^\infty \frac{1}{1+(RC)^2\omega^2}d\omega \\ &= \frac{4kTR}{2\pi}\frac{\pi}{2}\frac{1}{RC} \\ &= \frac{kT}{C}\end{aligned} \tag{C.10}$$

The total noise is equal to kT/C and the noise bandwidth is given by $\frac{\pi}{2}\frac{1}{RC}$.

C.3.2 Bandpass Transfer Function

A simple bandpass transfer function a transfer function given by Equation C.11. ω_1 and ω_2 are the 3 db corner frequencies of the bandpass transfer function. The transfer

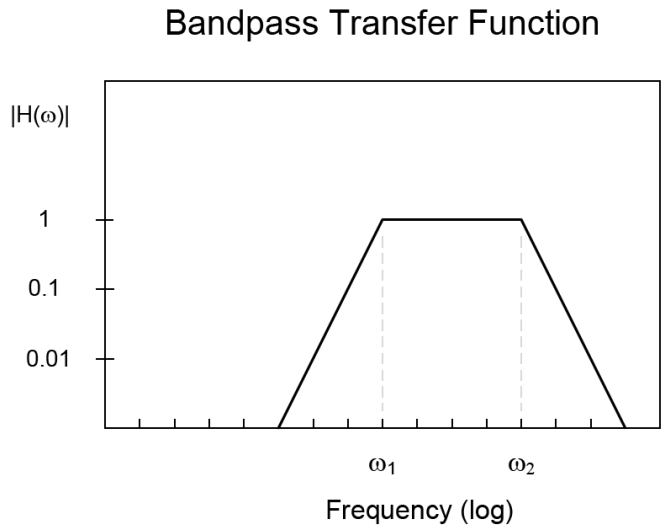

Figure C-3: Bandpass transfer function

function is plotted in Figure C-3.

$$\begin{aligned} H(\omega) &= \frac{\frac{j\omega}{\omega_1}}{\left(1+\frac{j\omega}{\omega_1}\right)\left(1+\frac{j\omega}{\omega_2}\right)} \\ &= \frac{j\omega\omega_2}{(\omega_2+j\omega)(\omega_1+j\omega)} \end{aligned} \tag{C.11}$$

The magnitude of H(ω) squared is given by:

$$|H(\omega)|^2 = \frac{\omega^2{\omega_2}^2}{({\omega_2}^2+\omega^2)({\omega_1}^2+\omega^2)} \tag{C.12}$$

To compute the integral of the transfer function we can let f(z) = $\frac{z^2{\omega_2}^2}{({\omega_2}^2+z^2)({\omega_1}^2+z^2)}$. By observation, the singularities of f(z) occur at $\pm j\omega_1$ and $\pm j\omega_2$. The contour we draw is the same shape as the the contour in Figure C-1. Thus, the singularities enclosed by the contour are $j\omega_1$ and $j\omega_2$. To compute the residue at these singularities, we can write f(z)= g(z)/h(z) where g(z) = $z^2{\omega_2}^2$ and h(z) = $({\omega_2}^2+z^2)({\omega_1}^2+z^2)$.

$$h'(z) = 4z^3 + 2\left({\omega_1}^2 + {\omega_2}^2\right) z \tag{C.13}$$

The residues at $j\omega_1$ and $j\omega_2$ can be evaluated by using Theorem 69.2 from Complex Variables and Applications [44].

$$\begin{aligned} \textit{Res f(z) at } z = j\omega_1 &= g\left(j\omega_1\right)/h'\left(j\omega_1\right) \\ &= \frac{-{\omega_1}^2{\omega_2}^2}{-4j{\omega_1}^3 + 2\left({\omega_1}^2 + {\omega_2}^2\right) j\omega_1} \\ &= \frac{-\omega_1{\omega_2}^2}{j2\left({\omega_2}^2 - {\omega_1}^2\right)} \end{aligned} \tag{C.14}$$

$$\begin{aligned} \textit{Res f(z) at } z = j\omega_2 &= g\left(j\omega_2\right)/h'\left(j\omega_2\right) \\ &= \frac{-{\omega_2}^4}{-4j\omega_2^3 + 2\left({\omega_1}^2 + {\omega_2}^2\right) j\omega_2} \\ &= \frac{-{\omega_2}^3}{j2\left({\omega_1}^2 - {\omega_2}^2\right)} \end{aligned} \tag{C.15}$$

The sum of the residues is given by :

$$\begin{aligned} \sum \textit{Res f(z)} &= \frac{-\omega_1{\omega_2}^2}{j2\left({\omega_2}^2 - {\omega_1}^2\right)} + \frac{-{\omega_2}^3}{j2\left({\omega_1}^2 - {\omega_2}^2\right)} \\ &= \frac{{\omega_2}^2\left(\omega_2 - \omega_1\right)}{j2\left({\omega_2}^2 - {\omega_1}^2\right)} \end{aligned} \tag{C.16}$$

We can apply Cauchy's Residue Theorem to compute the integral.

$$\begin{aligned}\int_C f(z)dz &= 2\pi j \cdot \sum Res\, f(z) \\ &= 2\pi j \cdot \frac{{\omega_2}^2 (\omega_2 - \omega_1)}{j2 ({\omega_2}^2 - {\omega_1}^2)} \\ &= \pi (\omega_2 - \omega_1) \frac{{\omega_2}^2}{{\omega_2}^2 - {\omega_1}^2} \end{aligned} \tag{C.17}$$

Thus,

$$\int_{-\infty}^{\infty} f(x)dx = \pi (\omega_2 - \omega_1) \frac{{\omega_2}^2}{{\omega_2}^2 - {\omega_1}^2} \tag{C.18}$$

and

$$\int_{0}^{\infty} f(x)dx = \frac{\pi}{2} (\omega_2 - \omega_1) \frac{{\omega_2}^2}{{\omega_2}^2 - {\omega_1}^2}. \tag{C.19}$$

The noise bandwidth of a bandpass transfer function is given by Equation C.19. If ω_2 is much greater than ω_1, the noise bandwidth approaches $\frac{\pi}{2} (\omega_2 - \omega_1)$.

By using Equation C.19, we can compute the noise bandwidth of the bandpass transfer function as a function of ω_2 and ω_1. A few example comparisions is shown in Figure C-4. The example used in Chapter 2 is when ω_2 is set to 4x of ω_1. In this case the noise bandwidth is given by $\frac{8\pi}{15} (\omega_2 - \omega_1)$ which is approximately equal to $\frac{\pi}{2} (\omega_2 - \omega_1)$.

Ratio of ω_2 to ω_1	Noise bandwidth
$\omega_2 = \sqrt{2}\,\omega_1$	$\pi\ (\omega_2 - \omega_1)$
$\omega_2 = 4\,\omega_1$	$8\pi/15\ (\omega_2 - \omega_1)$
$\omega_2 = 10\,\omega_1$	$50\pi/99\ (\omega_2 - \omega_1)$
$\omega_2 >> \omega_1$	$\pi/2\ (\omega_2 - \omega_1)$

Figure C-4: Noise bandwidth of a bandpass transfer function