Multi-Channel Ultra-Low-Power Receiver Architecture for Body Area Networks

by

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B.A.Sc. in Electrical Engineering, University of Waterloo, 2009

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

In recently published integrated medical monitoring systems, a common thread is the high power consumption of the radio compared to the other system components. This observation is indicative of a natural place to attempt a reduction in system power. Narrowband receivers in-particular can enjoy significant power reduction by employing high-Q bulk acoustic resonators as channel select filters directly at RF, allowing down-stream analog processing to be simplified, resulting in better energy efficiency. But for communications in the ISM bands, it is important to employ multiple frequency channels to permit frequency-division-multiplexing and provide frequency diversity in the face of narrowband interferers. The high-Q nature of the resonators means that frequency tuning to other channels in the same band is nearly impossible; hence, a new architecture is required to address this challenge.

A multi-channel ultra-low power OOK receiver for Body Area Networks (BANs) has been designed and tested. The receiver multiplexes three Film Bulk Acoustic Resonators (FBARs) to provide three channels of frequency discrimination, while at the same time offering competitive sensitivity and superior energy efficiency in this class of BAN receivers. The high-Q parallel resonance of each resonator determines the passband. The resonator's Q is on the order of 1000 and its center frequency is approximately 2.5 GHz, resulting in a -3 dB bandwidth of roughly 2.5 MHz with a very steep rolloff. Channels are selected by enabling the corresponding LNA and mixer pathway with switches, but a key benefit of this architecture is that the switches are not in series with the resonator and do not de-Q the resonance. The measured 1E-3 sensitivity is -64 dBm at 1 Mbps for an energy efficiency of 180 pJ/bit. The resonators are packaged beside the CMOS using wirebonds for the prototype.

Thesis Supervisor: Anantha P. Chadrakasan
Title: Professor

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Chapter 1

Background

1.1 Introduction

Over the last five decades, computing has continuously progressed to smaller scales and ever more powerful platforms. Today's wireless handsets, for example, contain more computing power than the average room-sized computing machine of the 1960s. As a result of this dramatic trend in miniaturization, human-computer interaction continues to become more affordable, fluid, and pervasive in our daily lives.

Personal health monitoring is an area that has benefited significantly from these advances in electronics and computing. Whereas health monitoring is traditionally performed with bulky equipment and is usually confined to doctor's offices and hospitals, new unobtrusive on-body monitoring systems aim to capture biological signals in a relaxed and natural setting and communicate this information to health-care providers automatically via the Internet. Not only does this improve the frequency and the quality of the data gathered, but it also enhances the ability to react quickly to unexpected medical events. Moreover, this same technology has applications in many related areas such as fitness and entertainment.

With the potential for on-body medical monitoring to reach a large market in the coming years, the IEEE 802.15 Task Group 6 was formed in 2007 to create a new RF

infrastructure for Wireless Body Area Networks (WBANs). The aim is to promote interoperability between equipment vendors, and address the challenge of ultra low energy consumption for the on-body nodes. From a radio hardware perspective, the latest draft of the standard [1] proposes an energy-efficient Media Access Control (MAC) layer and three energy-efficient RF Physical layers (PHYs) including body coupled communication, ultra-wideband, and low power narrowband. The hope is that the standard provides new tools to system designers that will lead to a host of new applications in the near future.

1.2 Motiviation

Today's advanced on-body sensors can cover a wide range of biological signals in small form factors, including EEG, ECG, blood pressure, glucose, oxygenation, breathing, body temperature, and limb motion, to name a few. In addition, CMOS technology is helping to ease integration of the various parts of these systems onto a single silicon die. But despite the impressive progress in sensor technology and integration, key challenges still remain communicating this information around the body in a coordinated and energy efficient way.

One challenge in particular is the design of an ultra-low power receiver for on-body wireless nodes. While much research has focused on transmitting data from on-body sensor nodes to a central basestation, there are a number of applications where it would be useful for data to travel in the opposite direction. Whether it is for streaming audio to a cochlear implant, stimulating an insulin pump, or simply for coordinating media access among wireless nodes, the low power on-body receiver should play an important role in body area networks.

Secondly, radio communication is currently the dominant power consumer in most integrated wireless body nodes. Recently published health monitoring Systems-on-Chip (SoCs) [2, 3, 4, 5] show how the radios currently consume a significant fraction,

about 80%, of the system budget. This indicates that power reductions in the radio architectures have the potential to directly impact the overall system energy.

Finally, for communication in unlicensed frequency bands, it is often important to employ multiple frequency channels to permit frequency-division-multiplexing and provide frequency diversity in the face of narrowband interferers. Unfortunately, many of the lowest power receivers in the literature have traded the ability to select channels for their ultra low power consumption.

1.3 Scope and contributions

This thesis addresses the simultaneous challenges of energy efficiency and frequency selectivity in low power receivers destined for use in body-worn nodes in a Wireless Body Area Network scenario.

Compared to commercial low-power peer-to-peer technologies such as Bluetooth and Zigbee, it will be shown that the typical Body Area Network scenario offers important opportunities for energy reduction. One such opportunity is the shorter communication distance—on the order of 1 to 2 meters—compared to today's commercial technology, allowing for a sensitivity reduction in the receiver. Another is the notion that most scenarios will involve low-rate medical information that can be buffered and transmitted in bursts at higher data rates, thus reducing the circuit and MAC-layer energy overhead. A final opportunity is the use of a star-network topology in which all of the energy-starved nodes communicate with an energy-abundant basestation. With the pervasiveness of low-cost multi-standard wireless devices in today's society, it is not unreasonable to assume that the user's cellular handset could serve as such a basestation and be capable of transmitting on the order of typical Bluetooth power levels.

By exploring the design space enabled by the above assumptions, a new multi-channel low-power wireless receiver has been designed and tested. The key features

and contributions of this design are:

1. **A new combined LNA/mixer architecture** that allows three channels of frequency discrimination by multiplexing three high-Q resonators. The circuits designed for this task avoid the use of series voltage switches that would otherwise impact the quality factor, and the architecture as a whole can be extended to many additional channels.

2. The capability to transmit at **high** (1 Mbps) **data rates and duty cycle the radio quickly** (within 6 bit periods) in order to maintain a low average power without sacrificing in wasted overhead.

3. **A competitive energy efficiency** (180 pJ/bit for -65 dBm sensitivity) compared to previously published radios in this space.

4. And finally, narrowband **operation in the 2.4 GHz ISM band** underneath regulatory operating limits and suitable for use in most jurisdictions around the world.

1.4 Organization of this thesis

After discussing background information on Body Area Networks and reviewing previous work, this thesis will present the detailed design and measurement results for the above-mentioned ultra low power receiver architecture. It will then conclude with a summary and ideas for future research directions.

Chapter 2 provides the necessary background information on radio architectures for Body Area Networks, including a survey of previously published radios of various types, and a discussion of techniques used to reduced power consumption in radio receivers. Next, Chapter 3 describes the high-Q resonators that were used as filtering elements in this project. Afterwards, Chapter 4 presents the detailed design of each of the receiver blocks, and a simulation of the noise performance for the system as a

whole. Finally, Chapter 5 presents the main simulation and measurement results, and Chapter 6 presents a summary and a discussion of potential future research directions.

Chapter 2

Design considerations

The previous chapter introduced Wireless Body Area Networks (WBANs) and discussed the need for a multi-channel transceiver. This chapter begins by presenting a high-level comparison of WBANs to a related technology, Wireless Sensor Networks (WSNs). Next, the focus will shift to the channel model for WBAN, and to previously designed low power receivers. Finally, general techniques for designing ultra-low power receivers will be discussed, and an architecture for the multi-channel transceiver will be proposed.

2.1 WBANs versus WSNs

The vision for Wireless Body Area Networks (WBANs) is one in which a number of micro-power nodes are scattered around the human body in order to collect physiological information and relay it to a less power-constrained device for further processing.

Considerable research over the last few years has focused on a related technology, Wireless Sensor Networks (WSNs). While some portions of sensor network research can be carried into Body Area Networks, recent review papers [6, 7, 8] point out some key differences between the two. The information presented in Table 2.1 discusses some important specifications for body area networks by way of comparison

to traditional wireless sensor networks.

Table 2.1: Comparison of WSNs and WBANs

Criteria	Comparison
Transmission distance	WBANs generally have a shorter transmission distance (1 to 2 meters) than traditional WSNs (10 to 100 meters)
Energy efficiency	Both are concerned with minimizing circuit and MAC-layer overhead, with WBANs particularly concerned with achieving overall minimum energy consumption per bit for the energy constrained nodes
Redundancy	WBANs will generally have less redundancy than traditional WSNs, where redundancy is a common technique to deal with failures. Patients will expect to wear the minimum number of sensors.
Topology	In WSNs, multi-hop and and ad-hoc scenarios prevail, whereas for WBANs, a star-topology is often sufficient and optimal
Form Factor	WBAN nodes are generally smaller (eg. $< 1cm^3$) compared to traditional WSNs
Device lifetime	Similar, although the physical volume of the energy storage devices can be more of a problem in the space constrained WBAN nodes
Heterogeneity	Nodes in WBANs may not all communicate the same type of medical information, hence they may have vastly different demands in terms of bandwidth, power consumption, and reliability
Channel Loss	The body is generally lossier than the channel seen by traditional sensor nodes
Movement	Since the human body could be in motion, body sensor transceivers must be robust to channel variations

Perhaps most importantly, both the review papers and the proposed WBAN standard [1] point to the star network topology as the most popular configuration for Body Area Networks. In this configuration, all of the on-body nodes communicate with a central basestation. This allows the complexity and power consumption of a transceiver system to be transfered onto the power abundant basestation and away from the energy-starved nodes.

2.2 Receiver specifications

In peer-to-peer communication among energy constrained nodes, both the receiver sensitivity and the transmitter output power need to be co-optimized to obtain the best energy efficiency for the end-to-end link. The asymmetric link enabled by the star topology, however, allows the specs on the body-node receiver to be relaxed compared to the peer-to-peer case.

For this scenario, two important transmitter metrics should be taken into account when designing the energy constrained receiver. The first concerns the maximum permissible radiated power of the transmitter due to regulations. If we take the FCC limit on radiation in the 2.4 GHz ISM band as an example, the maximum is 30 dBm effective isotropic radiated power [9] . The second is the expected radiated power of a typical basestation transmitter. As an example, 802.15.1 (eg. Bluetooth) sets a power range between 0 dBm minimum and +20 dBm maximum for Class 1 devices [10].

Using the modified Friis transmission formula [11, 12, 13], one can estimate the required sensitivity for a receiver design under the above assumptions:

$$P_r = G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \left(\frac{1}{d}\right)^n P_t, \tag{2.1}$$

where P_t and P_r are the transmit and receive powers, G_t and G_r are the transmitter and receiver antenna directivity gains, λ is the wavelength, d is the path length, and n is an experimentally determined path loss factor, usually between 2 and 4, that models fading and multi-path losses that occur for the channel under consideration. It should be noted that $n = 2$ only for an ideal line-of-sight scenario, therefore, a worst-case value of 4 is assumed for the obstructed propagation around the body. Assuming omnidirectional radiation and reception from the antennas, G_t and G_r can

be set to 1. At 2.4 GHz, this equation can be rewritten in terms of dBm:

$$P_r = P_t - 40 \log d - 40 \text{ [dBm]}. \tag{2.2}$$

For 2 meters of propagation, and a moderate basestation radiated power (10 dBm), the received power is -42 dBm, for a path loss of 52 dBm.

Recently published path loss measurements of the wireless channel around the human body [14, 15] provide estimates of "average" path loss ranging from 40 to 60 dB depending on the transmission distance and antenna positions on the body. However, both studies did not examine how body movement affects the path loss.

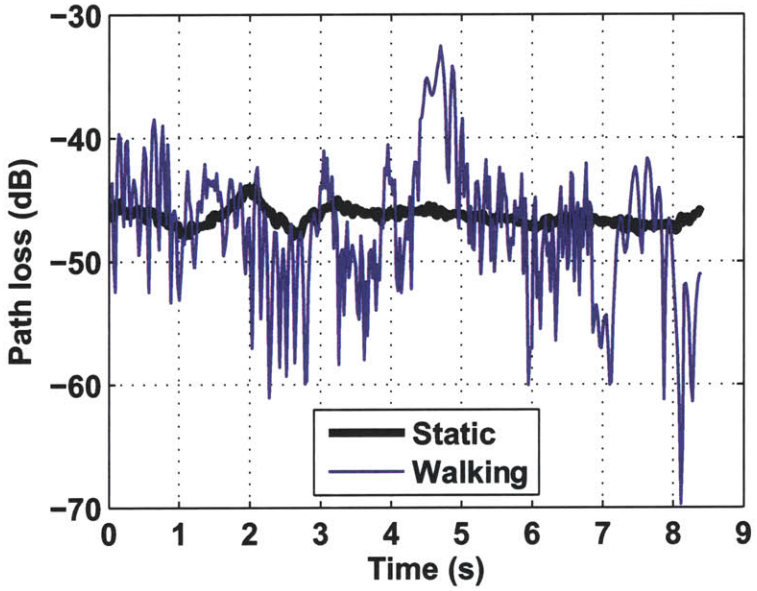


Figure 2-1: On-body path loss measurement from the chest to the back pocket (*courtesy of Haitham Hassanieh and Dina Katabi, MIT, 2011)

A recent experiment conducted by a group at MIT suggests large deviations from the baseline "average" loss due to body movement, as depicted in Figure 2-1. These plots were created using 2.4 GHz Software Defined Radios which took measurements of the path loss over time. Both stationary and walking measurements of the path loss around the human body were taken in an office environment, with the transmitter

placed on the subject's chest, and the receiver placed in the subject's back pocket. The study concluded that substantial variations in path loss due to movement are possible, and across many combinations of receiver and transmitter positions, the maximum observed losses were on the order of 80 dBm. Therefore, given a +10 dBm Bluetooth-style transmitter, receiver sensitivities on the order of -70 dBm are preferable

Using the noise bandwidth of the receiver front end (BW_{noise}), the receiver noise figure (NF), and the required SNR to achieve the target bit error rate (SNR_{BER}), the receiver sensitivity can be expanded into the following form:

$$P_{sens} = -174\text{dBc/Hz} + 10\log_{10}(BW_{noise}) + NF + SNR_{BER}. \quad (2.3)$$

Assuming a received power of -70 dBm, a reasonable demodulation SNR of about 10 dB, and a noise bandwidth of 2 MHz (for a 1 Mbps data rate), then (2.3) suggests the required noise figure is about 30 dB. This is a significantly relaxed requirement compared to state of the art receivers, and a key ingredient in reducing the receiver power consumption.

Finally, Table 2.2 sets out definitions for additional receiver specifications that will be considered in this thesis. Where it is useful to associate a specification to a particular unit, the unit has been specified in square brackets.

2.3 Previously published low-power receivers

With the enormous number of ways that a wireless receiver can be constructed for various power levels, spectral efficiencies, channel conditions, and interference scenarios, it is very challenging to formulate a single figure of merit that fairly and accurately compares two receivers. However, since this thesis deals with energy efficient receivers, and since the power consumption noise performance of a receiver

Table 2.2: Definitions for common receiver specifications referred to in this thesis

Name	Unit	Description
Center frequency	[GHz]	Center of the transmitted spectrum
Energy efficiency	[pJ/bit]	Energy required to receive one raw bit
Front-end bandwidth	[MHz]	Width of spectrum used in demodulation
Modulation scheme		Method used to convert bits to continuous-time RF signals
Raw bit rate	[Mbps]	Uncoded bit rate
Sensitivity	[dBm]	Receiver input power that generates a raw bit error rate of 10^{-3}
Spectral efficiency	[bit/Hz]	Raw bit rate divided by the font-end bandwidth
Startup time	[μs]	Time required to start the radio from the its off state

are strongly correlated, the primary metrics that will be considered in this thesis are energy efficiency and sensitivity. A simple way of thinking about the relationship between the two metrics is as follows: the more energy spent capturing a bit, the higher quality that bit should be.

A literature survey of previously published low power receivers was conducted. The survey focused on the three main physical layer types found in the proposed WBAN standard, namely Human Body Communication, ultra-wideband, and narrowband. The survey is presented in Figure 2-2 and Table 2.3. The narrowband case considered 2.4 GHz ISM receivers and was further divided into three subtypes: 802.15.4 (Zigbee) quadrature down-conversion architectures, super-regerative architectures, and other non-coherent techniques.

The selected data are from recently published receivers in ISSCC and JSSC in the last 5 years. In general, where multiple operating points were specified, the one with the best energy efficiency was selected. In the case of Zigbee front-ends, where noise figure is usually published instead of sensitivity, equation (2.3) was applied with a

[1]sensitivity is 350 μV_{pp} referenced to 50 Ω
[2]sensitivity given for BER = 10^{-8}

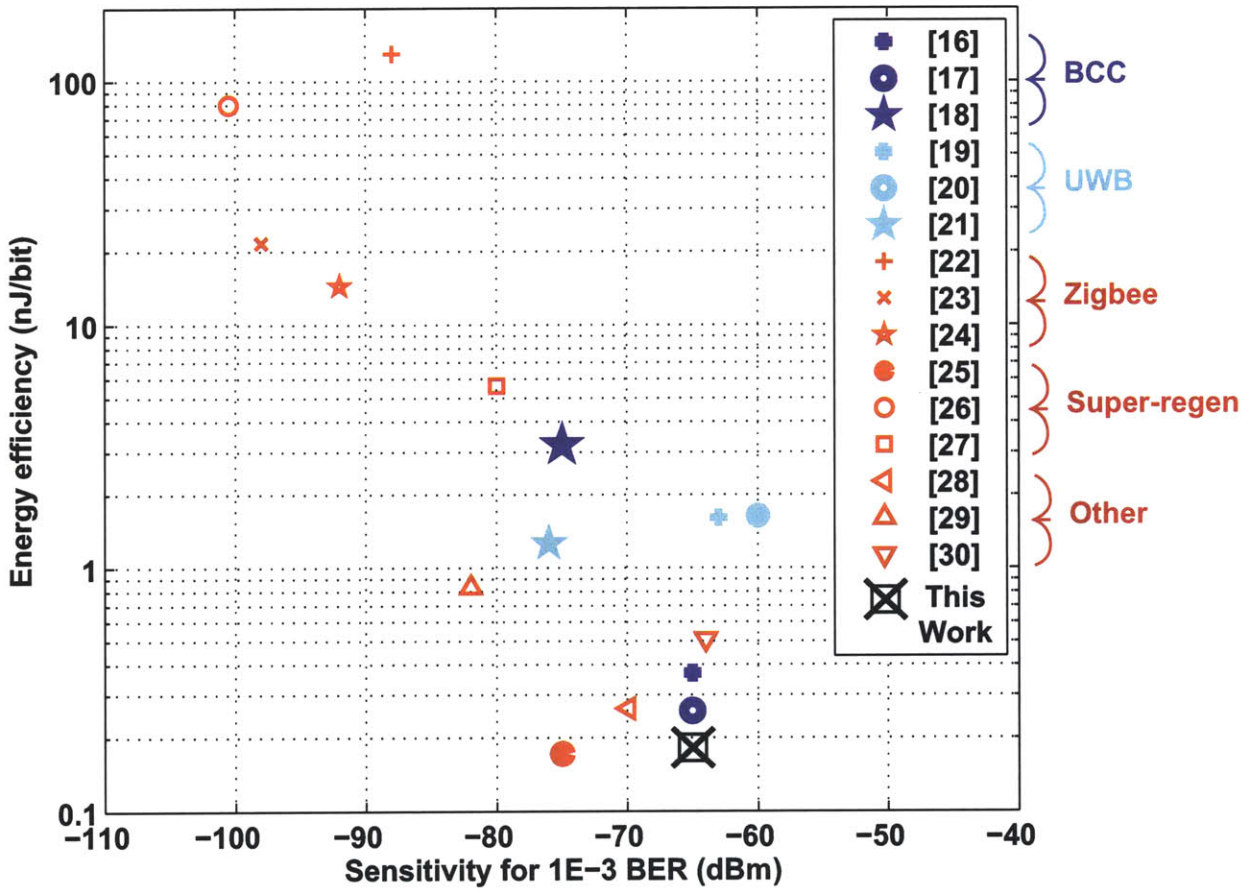


Figure 2-2: Chart of related low power receivers in ISSCC and JSSC in the last 5 years

Table 2.3: Table of related low power receivers

Ref	Type	Data rate (kbps)	Power (μW)	Efficiency (pJ/bit)	Sensitivity (dBm)
[16]	BCC	10000	3700	370	-65
[17]	BCC	8500	2200	260	-65[1]
[18]	BCC	1000	3200	3200	-75[2]
[19]	UWB	2604	4200	1610	-63
[20]	UWB	1000	1640	1640	-60
[21]	UWB	16000	20200	1260	-76
[22]	NB-Zigbee	250	32500	130000	-88
[23]	NB-Zigbee	250	5400	21600	-98
[24]	NB-Zigbee	250	3600	14400	-92
[25]	NB-Super-regen	3000	516	170	-75
[26]	NB-Super-regen	5	400	80000	-101
[27]	NB-Super-regen	500	2800	5600	-80
[28]	NB-Other	200	52	260	-70
[29]	NB-Other	500	415	830	-82
[30]	NB-Other	100	51	510	-64
	This work	**1000**	**180**	**180**	**-65**

noise bandwidth of 2 MHz and a typical required SNR of 7 dB.

There is a clear trend towards the bottom right of the plot due to the notion of a tradeoff between sensitivity and energy per bit. There is also, however, considerable overlap between the techniques. Since the receivers were constructed under varying sets of assumptions about channel rejection, availability of reference clocks, interference scenarios, and modulation schemes, no explicit trend line can be drawn. Therefore, in order to explore some of the more subtle differences between the architectures, the following subsections present a brief overview of the receivers, highlighting the main tradeoffs discussed in the research publications.

2.3.1 Human Body Communication

Human Body Communication, also known as Body Coupled Communication (BCC), is a technique used to transmit information using the human body as a communication medium. These transceivers enable low power communication that does not itself interfere with FCC regulations or existing systems, but is nevertheless susceptible to interference from such systems, especially in the proximity of high-powered broadcasting stations.

Previous studies has shown that the optimal frequency for BCC communication is somewhere between 10 and 100 MHz [31, 32], the lower end limited by propagation losses, and the upper-end limited by a body antenna effect whereby the RF energy is no longer confined to the body and is radiated into the environment. Therefore, BCC signals are typically modulated to a sub- 100 MHz carrier before they are capacitively coupled to the body via electrodes on or near the surface of the skin.

Recently published BCC transceivers [16, 17, 18] have shown receiver energy efficiencies on the order of 1 nJ/bit, data rates on the order of 1 Mbps, and receiver sensitivities of roughly -60 to -70 dBm. A key benefit to intra-body signaling is the low amount of power that radiates outside the body, making it easier to meet FCC regulations, providing a layer of inherent security to the user, and allowing spectrum

reuse between adjacent users without requiring an explicit cellularized structure. A major concern however, is interference rejection due to the substantial presence of high-powered television and radio stations that occupy the same bandwidth. Two of the BCC receivers attempt to explicitly address this problem: one adopts a cognitive Frequency Shift Keying (FSK) modulation to avoid frequencies with high interference [16], whereas the other employs a high RX input resistance to reject offending spectrum above 30 MHz, and a correlation-based scheme to reject signals with poor correlation to the expected one [17].

2.3.2 Ultra-Wideband

In situations where capacitively coupling to the body is not appropriate or feasible, a pulse-based ultra-wideband (UWB) approach can be used. These systems achieve ultra low energy consumption per transmitted and received pulse, but with considerable tradeoffs in sensitivity and susceptibility to interferers.

UWB architectures use narrow (nanosecond) pulses in the time-domain to spread the transmission spectrum over a wide frequency bandwidth of several hundred megahertz, maintaining the same total signal power while transmitting considerably lower power spectral density. In fact, the power spectral density is so low that it is under the FCC limit for unintended radiators such as personal or laptop computers. The transmitters in such systems are highly amenable to all-digital architectures that eliminate power-expensive components such as frequency synthesizers and phase locked loops (PLLs), leading to ultra low power consumption.

The past few years have seen a large amount of research dedicated to developing energy efficient UWB transceiver architectures with considerable success. The 18 pJ/pulse transmitter in [33] and the 108 pJ/pulse receiver in [19] provide excellent representative samples, and also show how the receiver generally consumes more power than the transmitter, due to the transmitter's comparatively simpler implementation. Behind this energy efficiency however, there are considerable tradeoffs in

sensitivity and robustness to interferers.

As an example, the 108 pJ/pulse receiver in [19] achieves a -63 dBm average sensitivity only after 15 pulses are integrated together to construct the received bit. The energy efficiency is then 1.6 nJ/bit for -63 dBm operation, which is comparable to the previously discussed BCC transceivers. Moreover, since the UWB spectrum covers wide swaths of bandwidth from DC all the way up to 10 GHz and beyond, narrowband interference from the countless services that occupy this bandwidth is an important and well-studied consideration [34, 35]. UWB systems must employ clever coding and modulation techniques to enable robust signaling, with an ultimate tradeoff against throughput and energy efficiency.

2.3.3 Narrowband

Finally, three main classes of narrowband receivers were considered. The first class are low power Zigbee receivers, which are equipped with quadrature mixers that support Quadrature Phase Shift Keying (QPSK) as a modulation scheme. In general, these have a worse energy efficiency than the BCC and UWB transceivers due to power expensive PLLs and quadrature oscillators, but are more capable of peer-to-peer communication due to their excellent sensitivity.

The second class consists of super-regenerative receivers that use regenerative positive-feedback to achieve gain and non-coherent detection to reduce power. These schemes support simple amplitude-based signaling schemes like On-Off-Keying (OOK). As pointed out by [27], a classic concern with superregenerative receivers, is poor selectivity, since unwanted signals that are too close to the tank frequency may start up the oscillation.

The final category includes some additional low power narrowband architectures that use clever techniques to reduce the power consumption. In particular, [30] uses a double-sampling technique to avoid 1/f noise at DC. Also, [28, 29] use a clever frequency plan that reduces the specification on the frequency stability of the oscil-

lator, and [28] in particular makes use of an-off chip resonator to greatly improve the frequency selectivity. Finally, two of the receivers [28, 30] achieve the lowest reported power consumption of all the surveyed radios at 52 and 51 μW respectively.

2.4 Low power narrowband receiver techniques

2.4.1 CMOS scaling

Historically, scaling has achieved important power reductions in ultra-low power receivers due to switching loss reduction and subthreshold operation.

Firstly, decreasing supply voltages and smaller transistors have led to a reduction is CV^2 switching losses. This leads to lower power consumption in high-activity blocks like oscillators.

Secondly, CMOS f_t's have continued to scale, with some of the most recent maximum f_t's reaching as high as 400 GHz at the 32-nm process node [36]. In general, f_t scaling has allowed designers, with careful verification, to bias devices in the subthreshold region, where the highest $\frac{g_m}{I_D}$ efficiency can be obtained, without significantly compromising device performance at low GHz frequencies [37].

Challenges still remain for RF-CMOS however, as scaling trends have also introduced higher subthreshold leakage, reduced small signal r_{ds} output resistance, and higher gate parasitics [38]. The 65-nm technology used for this thesis project represents a good compromise between these competing factors, and does not suffer extensively from the most recent scaling challenges for RF-CMOS. In certain key transistors, however, the gate length should be doubled to increase the small signal output resistance.

2.4.2 Low Power Oscillators

A high-level survey of the most recently published low power oscillators designed for near-2.4-GHz operation is presented in Table 2.4. One representative oscillator for each type is selected, and some of the major tradeoffs are contrasted. The ring oscillator power measurement was taken from the oscillator implemented in this thesis.

In high performance transceivers, oscillators are typically locked to very precise crystals to enable complex modulation schemes with increasingly dense constellation points. The biggest power savings occurs by eliminating the phase-locking requirement, however this is at the expense of spectral efficiency since lower-order modulation schemes must be used when phase drift starts to become problematic.

The next step in power savings is obtained by relaxing phase noise and frequency stability requirements. At the lowest end of this spectrum, modulation schemes become almost exclusively amplitude-based since the phase is no longer stable enough to convey information. The ring oscillator typically obtains the best power consumption, but with severe tradeoffs in frequency stability and phase noise. When choosing a ring oscillator for *LO* generation, the frequency planning and modulation scheme must take these tradeoffs into account.

2.4.3 Modulation

The use of high-order complex modulation types such as QAM and QPSK is often motivated by the need to increase the spectral efficiency and throughput of a transmission system. Unfortunately, this comes at the expense of hardware power consumption due to tighter specifications for the oscillator and more stringent noise figure requirement. Though the increased throughput could potentially amortize these extra power costs to achieve an overall better energy *per bit*, previous studies and radio designs suggest that simpler modulations schemes can be optimal.

In particular, [42] suggests that simple modulation schemes like OOK are optimal

Table 2.4: Comparison of low power oscillator architectures

Name	Power	Advantages	Drawbacks
All-Digital PLL [39]	8 mW	- No off-chip components - Tunable (2.29 to 2.92 GHz) - Phase locked to a reference - Low phase noise (-112 dBc/Hz)	- mW power consumption - Long startup time (30 us)
BAW [40]	600 uW	- Precise frequency generation - Ultra-low phase noise (-144 dBc/Hz)	- Off-chip BAW required - Low tuning range (< 0.1 %) - No phase locking
LC-tank [41]	180 uW*	- No off-chip components - Tunable (typically 10s of MHz) - Low power consumption - Low phase noise (-113 dBc/Hz)	- No phase locking
Ring oscillator	70 uW	- No off-chip components - No integrated inductors (very small area consumption) - Wide tuning range (several GHz) - Very fast startup time (< 1 μs) - Ultra-low power consumption	- Poor phase noise - No phase locking - Frequency instability

* simulated

since they reduce the synchronization overhead of the wireless system. Another study [43] concluded that for M-QAM transmitters, the lowest order M modulation is optimal when reducing the constellation size leads to a linear decrease in throughput but an exponential savings in power consumption, leading to an overall better energy per bit. Such a situation is present in a power constrained receiver if, for example, reducing the constellation size allows a power expensive frequency synthesizer (eg. 8 mW) to be reduced to a simpler architecture such as a ring oscillator (eg. 70 μW). Another example is the case where the LNA dominates the power consumption. In this case, reducing the constellation size leads to a linear decrease in throughput, but due to the relaxed SNR requirement, the LNA power consumption decreases substantially.

Finally, in the representative narrowband receivers presented in Figure 2-2, the QPSK-based Zigbee architectures generally had worse energy efficiencies than the super-regenerative and"other" categories, all of which relied on simpler schemes such as on-off-keying (OOK) and pulse position modulation (PPM) that are compatible with non-coherent detection.

One big advantage of OOK and PPM is the opportunity to use a simple non-coherent envelope detector for demodulation. This leads to a very low power hardware implementation since it relaxes the requirements on the local oscillator, or in some cases, eliminates the requirement for oscillators altogether.

2.4.4 High-Q resonators

For a receiver design, the high quality factor of electromechanical resonators enables very sharp passive filters with low loss, and can enable very simple energy-efficient architectures. These resonators have stable resonance frequencies and a vastly improved quality factor compared to traditional LC-based tanks. In typical receiver applications, resonators are used in ladder filters in order to select an entire RF band, such as the 2.4 to 2.4835 GHz ISM band. Afterwards, individual channel selection within the band is accomplished at IF. More recently, designs such as [28, 44, 45]

have used single resonators to filter the desired channel directly at RF, simplifying the down-stream hardware and thereby reducing power consumption.

The resonators are physical devices that vibrate in the mechanical domain at specific frequencies. The vibrating resonance modes are excited by electrical signals that are transduced into the mechanical domain by piezoelectric or electrostatic forces. The mechanical vibrations themselves then inject electrical energy back into the electrical circuit, and the result, at resonance, is the conversion of energy back and forth between the electrical and mechanical domains with very high quality factor and low loss. Since special materials and geometric structures are often required, the main challenge is integrating these devices into CMOS-compatible processing in order to leverage the existing foundry infrastructure to reduce cost.

Research on electromechanical resonators continues to improve the performance of these devices, and significant progress is being made on the integration front [46] which could one day provide access to 100's of resonators on a single silicon wafer. For now, if the designer is willing to tolerate an off-chip component, then resonator technology is still an excellent way to build ultra low power receivers by using the resonance for frequency selectivity. As will be shown in Section 3.5 however, one disadvantage of single-resonator approaches, integrated or otherwise, is that they are typically forced to operate at the single high-Q resonance frequency of the resonator.

Therefore, while single high-Q resonators can breed very simple and energy efficient receiver architectures, they are typically not well suited to a low power multi-channel receiver that employs channel selection directly at RF.

2.5 Receiver Architecture

The frequency plan for the mult-channel transceiver is based on an idea presented in previous receivers [28, 29], and uses the concepts discussed above. The plan calls for an ultra-low-power ring oscillator as the *LO*, and compensates for the uncertainty

in the downconverted IF frequency by designing wideband IF gain followed a simple envelope detector. The frequency plan is presented in Figure 2-3. The key to obtaining channel selectivity is to use the high-Q resonance of a MEMS resonator to filter the incoming RF and select the desired channel.

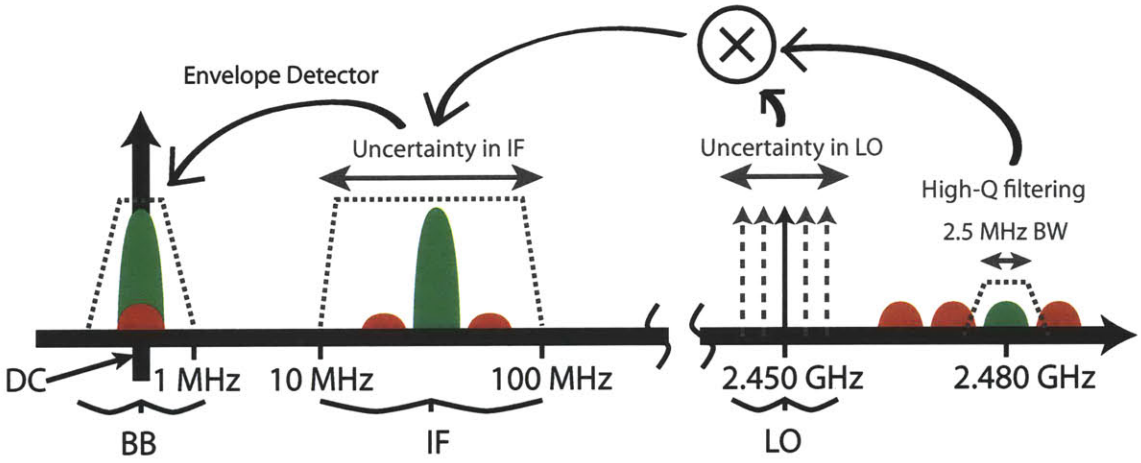


Figure 2-3: Frequency plan

As will be discussed in Chapter 3, the resonators have only a few megahertz of capacitive tuning capability without degrading the resonance. Therefore, to extend the frequency plan to multiple channels, an architecture is required to multiplex many resonators into a single design. Such an architecture was developed for this thesis and is presented in Figure 2-4.

The architecture is based on the premise that multiplexing the resonators with series voltage switches will serve to de-Q the resonance and severely restrict the filtering capability. Instead, the architecture uses the LNA cascode transistors as current steering devices to select which receiver pathway to enable. Multiplexing at the mixer is achieved by sharing a single wideband resistive load and tri-stating the unused mixers. Though the architecture is shown with three channels, it can be scaled to many additional channels. The subsequent portion of the receiver consists of energy efficient IF amplifiers and a low-power envelope detector.

The discussion in the next chapter will highlight the high-Q resonators used in

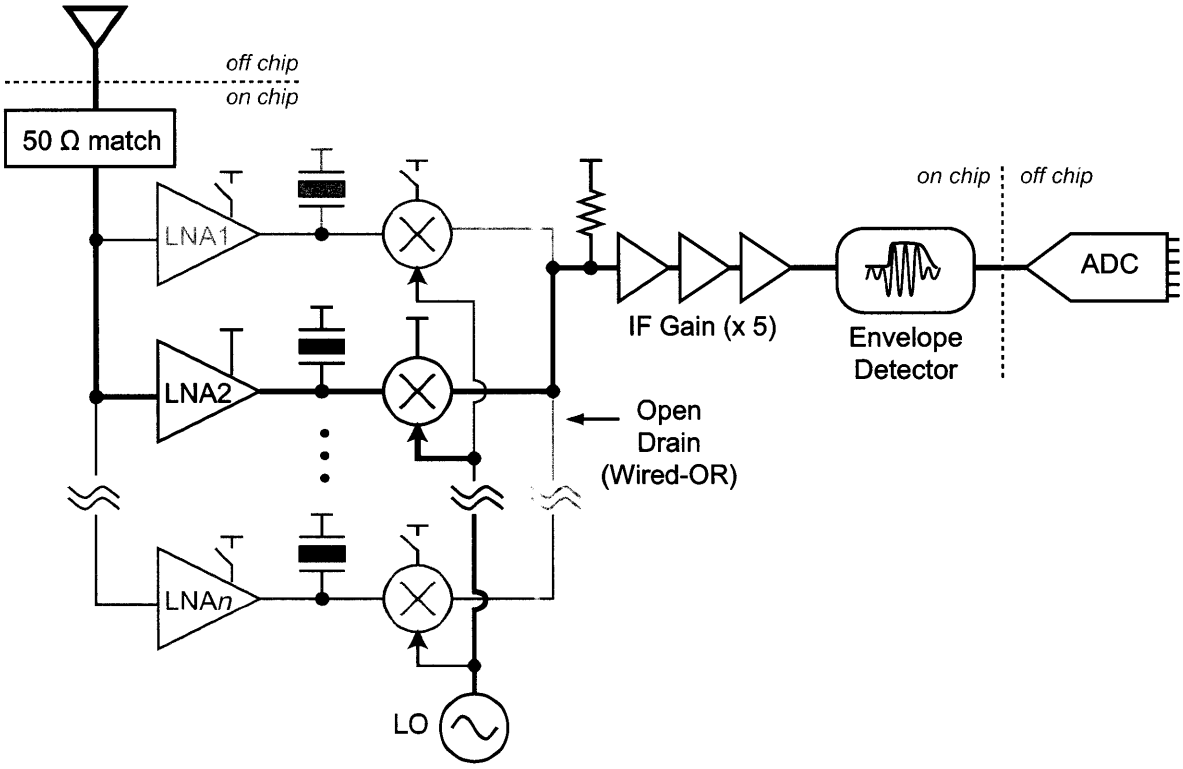


Figure 2-4: Receiver block diagram

this project. Afterwards, the design of the multi-channel CMOS receiver (Chapter 4), and measurement results (Chapter 5) will be presented.

Chapter 3

FBAR Resonators

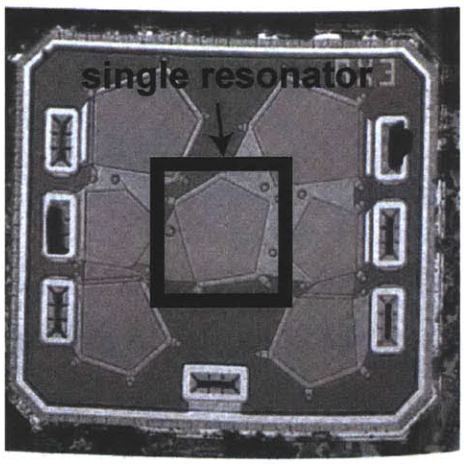
The previous chapter introduced an architecture for the multi-channel ultra-low power receiver and specified that RF-MEMS resonators would be used to provide channel selection at RF. The current chapter provides necessary background information on Film Bulk Acoustic Resonators (FBARs)—the particular type of MEMS resonator used for channel selection in this prototype. This information is presented in order to enable the subsequent discussion in Chapter 4 on the detailed design of the receiver circuits.

3.1 Introduction to FBARs

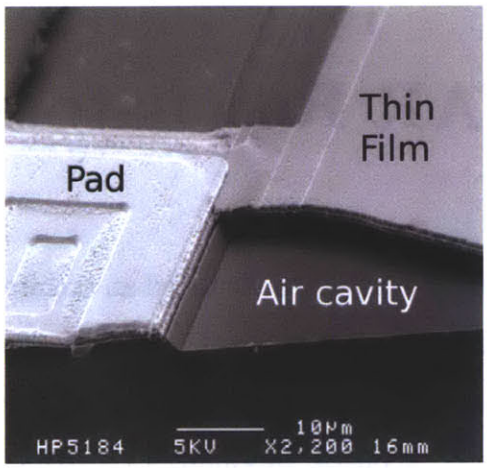
Work on commercializing piezoelectric thin-film bulk acoustic resonators (FBARs) began at Hewlett Packard in 1993. Over the course of a decade, HP and later, Agilent developed the technology into a very commercially successful duplexer product for the celluar PCS band [47]

Commercial FBAR products fabricated by Avago Technologies such as the RX filter shown in Figure 3-1a [47] typically consist of a number of resonators arranged in a ladder filter configuration. A close-up of a single resonator's structure in Figure 3-1b, and the cross section in Figure 3-1c, show how the resonator consists of a

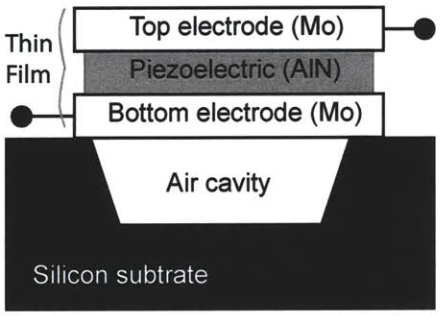
thin piezoelectric film sandwiched between two electrodes and then suspended over an air cavity. For this project, single-resonator process-control-monitoring (PCM) dies were used, as opposed to the standard multi-resonator filters of Figure 3-1a. These resonators were packaged with an all-silicon wafer-level packaging technique, the result of which is shown in Figure 3-1d.



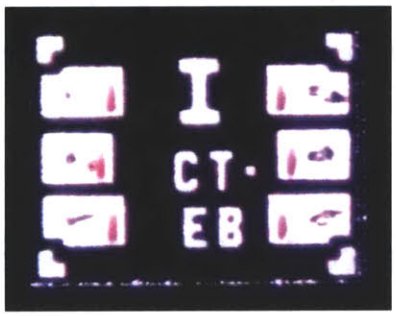
(a) Multiple FBARs in a ladder filter



(b) Close-up of a single FBAR



(c) Typical FBAR stackup



(d) Capped FBAR die

Figure 3-1: Introduction to FBAR

3.2 Modeling

Complete resonator modeling can be accomplished with the Mason model [48], though in the case of the FBAR, it is frequently simplified to a compact 4-element Butter-

worth Van Dyke (BVD) model. More recently, the Modified-Butterworth-Van-Dyke (mBVD) model was introduced by Larson et al. [49] by adding R_p to capture additional resistive losses caused by charges circulating internally to the device. The complete model is shown in Figure 3-2a, with yet another additional resistor, R_s, included to capture electrical terminal losses.

Excellent references on the electro-mechanical interaction that occurs in piezoelectric resonators are found in the literature [50, 51, 52]. The series R_m-L_m-C_m portion of the model represents the motional branch, which can be derived from fundamental physics by using electrostatic forces and the piezoelectric coefficients to relate the resonator's motion to it's terminal voltages and currents. One of the circuit elements, R_m represents the motional losses in the mechanical system, such as heating losses and leakage motion though the anchor points. Also, the large capacitor C_p is the physical parallel-plate capacitance formed across the piezoelectric layer.

Current injection on the capacitor sets the resonator into a thickness mode oscillation where energy is converted back and forth between elastic, kinetic, and electrostatic forms, before it is ultimately dissipated by the motional and electrical losses. Depending on the frequency and the loading condition, two main types of oscillations can be excited. The first type is the series resonance, where large currents can circulate freely in to and out of the device while developing only a small voltage at the terminals. This makes the overall device appear as a short circuit. The second type is the parallel resonance, where the large currents circulate internally between the motional branch and the device capacitance C_p, developing a larger voltage at the terminals, but drawing little current from the external circuitry. This makes the overall device appear as an open-circuit.

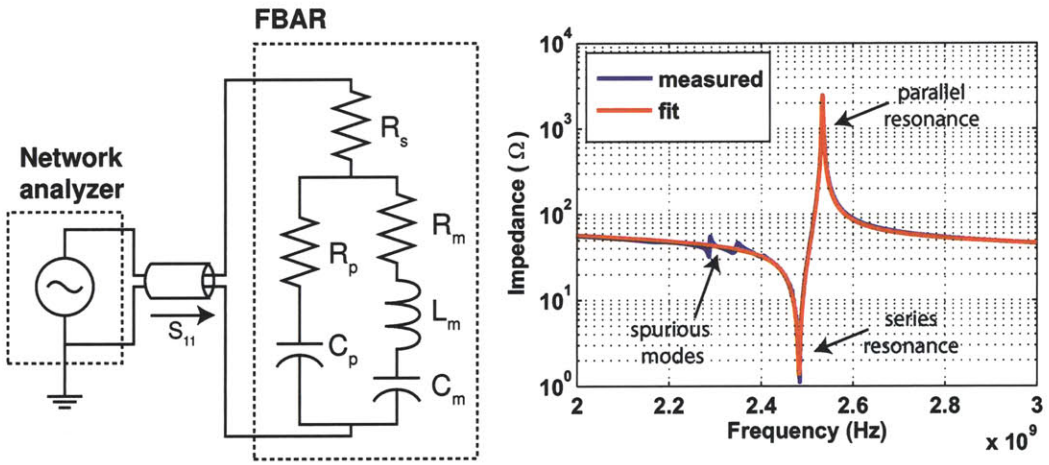
The frequencies of the parallel and series resonances can be computed from the mBVD model parameters:

$$\omega_{series} = \sqrt{\frac{1}{L_m C_m}} \tag{3.1}$$

$$\omega_{parallel} = w_{series}\sqrt{1+\frac{C_m}{C_p}}. \tag{3.2}$$

3.3 Measurement and fitting

The resonators used in this thesis were experimentally measured to obtain the S-parameters, after which a least-squares fitting operation was performed to determine the mBVD model parameters. The measurements were performed on a Cascade probe-station with 150-GSG probes, and the raw S-parameter data were captured by an Agilent Network Analyzer. The measurement setup is presented in Figure 3-2a.



(a) FBAR S_{11} measurement setup and mBVD model

(b) FBAR impedance magnitude response

Figure 3-2: FBAR modeling and measurement

The first step in fitting was to convert the S-parameter data into impedance magnitude and phase: $\log(|Z_{FBAR}|)$ and $\angle Z_{FBAR}$. The impedance scale was preferred in order to most accurately fit the high-impedance parallel resonance, and the logarithmic axis was used to help spread the fitting accuracy more evenly at lower impedances. The fitting was performed using a MATLAB® least squares fitting routine. Since the desired model parameters differed by many orders of magnitude (C_p in pF, C_m in fF, L_m in nH, and the R's in Ω), it was crucial to scale all of the parameters to be on the

same order of magnitude, for example, between 1 and 10, in order to obtain a good fit. The results of the fitting operation are shown in Figure 3-2b.

3.4 Quality Factor

The quality factor of a resonance determines its fractional frequency bandwidth and hence, its filtering capability. There are a number of methods to calculate the Q of piezoelectric resonators, four of which are listed below:

$$Q_{series} = \frac{\omega_{series} L_m}{R_m + R_s} \tag{3.3}$$

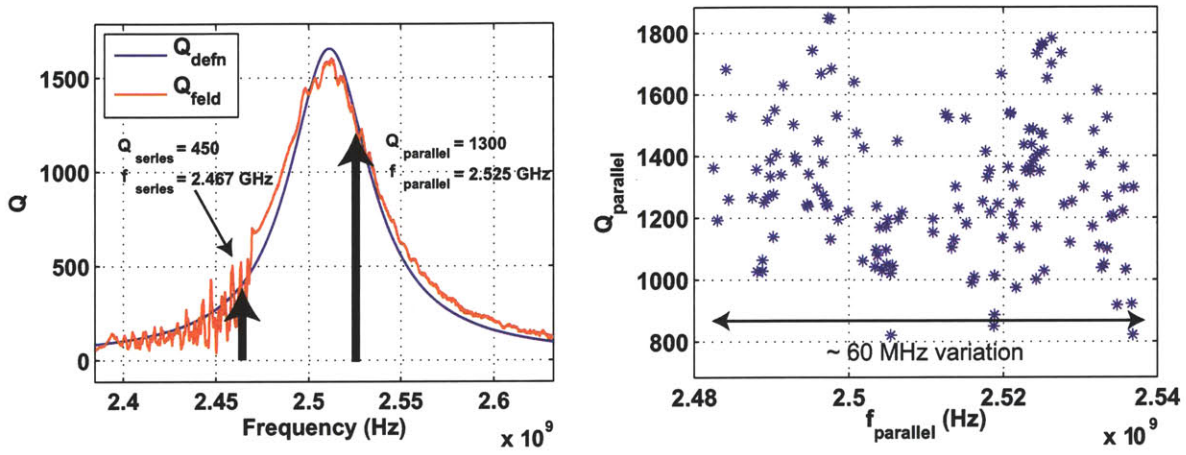
$$Q_{parallel} = \frac{\omega_{parallel} L_m}{R_m + R_p} \tag{3.4}$$

$$Q_{defn} = \omega \frac{\text{energy stored in the reactive elements}}{\text{average power dissipated}} \tag{3.5}$$

$$Q_{Feld} = \omega \frac{d(\angle S_{11})}{d\omega} \frac{|S_{11}|}{1 - |S_{11}|^2}. \tag{3.6}$$

Equations (3.3) and (3.4) are computed directly from the model parameters, and are valid only at the series and parallel resonances respectively. Equation (3.5) is the basic definition for quality factor [53], which can be used to simulate the Q at all frequencies, also by using the model parameters. Finally, (3.6) was developed by Feld et. al [54] to compute the Q at all frequencies directly from the measured S_{11}.

Though only Q_{series} and $Q_{parallel}$ are required, all four formulas were computed for a particular resonator in order to verify the accuracy of the model. The results are presented in Figure 3-3a. It should be noted that the much higher Q between the two resonances is representative of extra energy storage due to both resonances being partially activated, though this is not representative of the two resonance bandwidths. At the series and parallel resonances however, the Q's match almost perfectly.



(a) Q determined from the model fit and the measured S_{11}

(b) Scatter plot of the parallel resonance frequency and Q for 140 resonators

Figure 3-3: FBAR parallel resonance frequency and Q

3.5 Frequency Variation and Loading Effects

For the prototype, approximately 140 resonators from an untuned wafer were received, measured, and characterized using the above techniques. A scatter plot of $Q_{parallel}$ versus the parallel resonance frequency $f_{parallel}$ is presented in Figure 3-3b.

The resonators show approximately 60 MHz of frequency variation that can be leveraged to design a multi-channel receiver prototype. In a production application, the FBARs can be tuned to achieve better tolerance [55]. The average unloaded parallel resonance Q is 1300, for a -3 dB bandwidth of 1.9 MHz in these particular prototypes; though Q's in excess of 2500 are not uncommon [56].

A particularly dangerous type of loading for a filtering application is capacitive loading. The effect is presented via a simulation in Figure 3-4 for parallel capacitive loading. As the capacitive loading increases, the parallel resonance frequency shifts lower according to (3.2). However, the closer it approaches ω_{series}, the more the series RLC branch starts to looks like a short circuit, smearing out the sharp high-Q resonance. The design must minimize the capacitive loading or else live with the

reduced filtering capability.

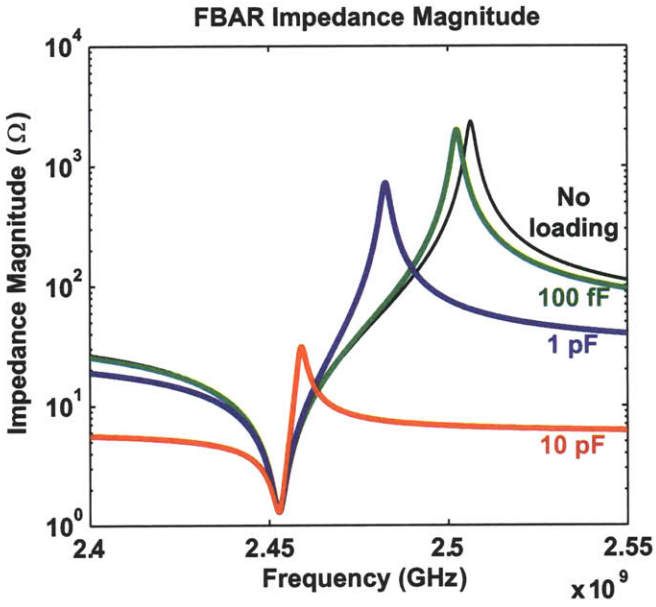


Figure 3-4: FBAR capacitive loading effect

Chapter 4

Detailed Receiver Design

This chapter presents the detailed design of the multi-channel receiver circuitry broken down into five major circuit blocks, namely, the LNA, Mixer, Oscillator, IF Gain, and Envelope detector blocks. Afterwards, block-level noise simulations will be described in order to create a picture of the overall system noise. This exercise will suggest that the noise performance of the system is LNA-gain-limited and can be improved by increasing the LNA's power consumption.

4.1 LNA

4.1.1 Tank

In the standard common-source LNA design, a transconductance stage provides g_m conversion of voltage to current, which is later converted to an output voltage by passing it through a high-impedance load. Ideally the load should have the shape of the desired frequency response. A cascode is normally employed to reduce output resistance and mitigate the Miller effect. The magnitude of the small signal voltage

gain from gate to output is given by:

$$\left|\frac{v_{lna}}{v_g}\right| = g_m|Z_o|. \tag{4.1}$$

In this design, the FBAR was included in the LNA tank to provide the $|Z_o|$; the reasons for doing so are two-fold.

Firstly, the magnitude of the FBAR impedance response, $|Z_{FBAR}|$, already has the desired filter shape at the parallel resonance. Therefore the magnitude of the voltage gain will have the shape of the desired filtering characteristic via equation (4.1).

Secondly, the parallel resonance provides a very high tank impedance at 2.5 GHz. By way of comparison, the standard LC-tank tuned load can be analyzed assuming some reasonable on-chip parameters and the parallel version of the Q formula for reactive components. Assuming an on-chip inductor with $L = 5$ nH and $Q = 10$, the equivalent parallel resistance of the inductor can be calculated:

$$\begin{aligned} Q_{parallel} &= \frac{R_{parallel}}{\omega L} \\ \Leftrightarrow R_{parallel} &= Q_{parallel}\omega L \\ &= 10 \times 2\pi \times 2.5 \text{ GHz} \times 5 \text{ nH} = 785\ \Omega. \end{aligned} \tag{4.2}$$

By contrast, the FBAR offers a parallel resonance impedance of roughly 2 to 3 kΩ, or about 2.5 to 3.8$\times$ of the tuned LC tank. This directly translates into 8 to 12 dB of additional voltage gain.

The next step is to design the LNA for multiplexing many center frequencies.

4.1.2 Design for multiplexing

In general, it is difficult to insert switches in series with very high Q resonators because they cause power dissipation that de-Q's the resonance. With this in mind, an initial

design that avoids series switches is shown in Figure 4-1.

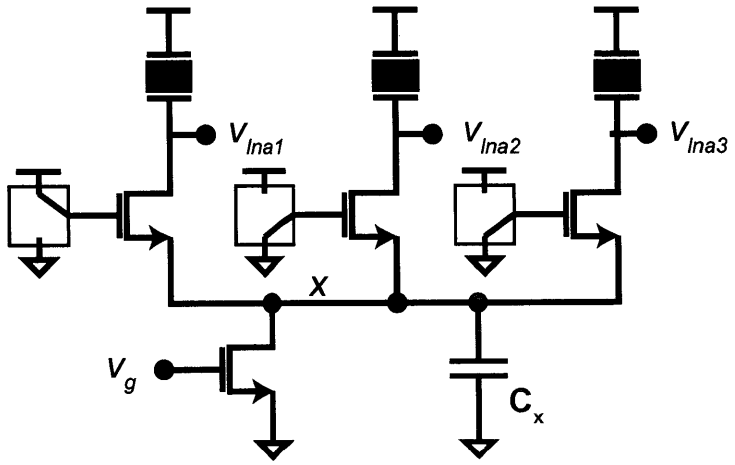


Figure 4-1: Initial LNA multiplexing scheme (biasing omitted)

The cascode transistors are used as current steering switches, but they do not impact the parallel resonance Q since only the injected current passes through the switches - the circulating parallel resonance currents do not. Therefore, this first pass design shows how multiplexing can be obtained, though it creates an input pole that degrades the response at 2.5 GHz due to the extra capacitance at node x. Using some simulated values for the transistors and n as the number of cascode devices, the pole location is given approximately by:

$$\begin{aligned} & f_{pole,x} = \frac{g_m}{2\pi(C_{gd} + nC_{gs,casc})}, \\ \text{for } n = 1 \rightarrow \quad & f_{pole,x} = \frac{2 \text{ mS}}{2\pi(10 \text{ fF} + 1 \times 12 \text{ fF})} = 17 \text{ GHz}. \end{aligned} \tag{4.3}$$

Clearly this solution is not scalable to additional cascode devices (n) due to the capacitive load.

Instead a scheme shown in Figure 4-2 is used, where both the cascode device *and* the input transistor can be replicated, with the additional capacitive loading absorbed into the 50 Ω input matching network. The next section will describe the design of the matching network.

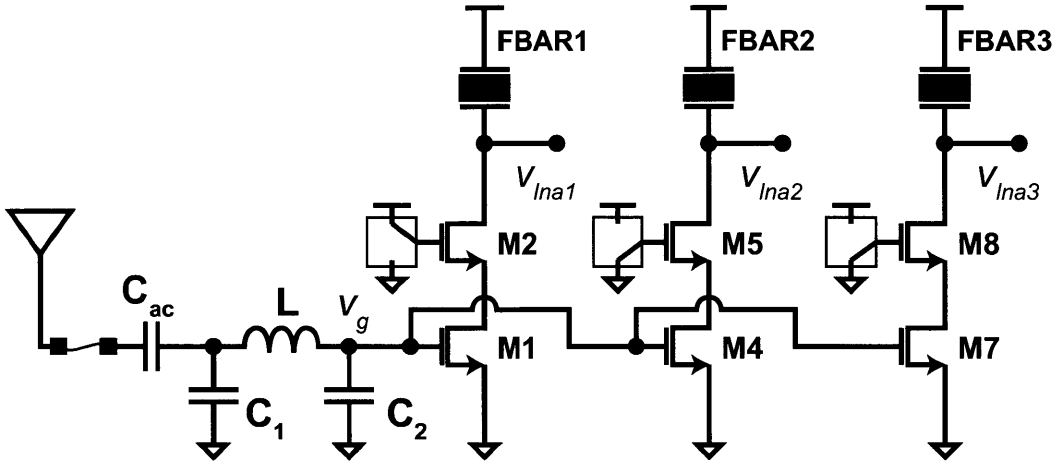


Figure 4-2: Final LNA multiplexing scheme (biasing omitted)

4.1.3 Matching network

Since the design will be tested with 50 Ω standard equipment, maximum power should captured by designing a 50 Ω match for the LNA. The input impedance before matching was simulated to be approximately $Z_{LNAs,in} = R_{LNA} + \frac{1}{j\omega C_{LNA}} = 40 - j400\ \Omega$.

One simple way to accomplish a reasonable match would be to directly tune out the $-j400$ Ω capacitance with 25 nH inductor (eg. $+j400$ Ω @ 2.5 GHz). However, this does not allow much room for post-fabrication tuning, and also represents a fairly large on-chip inductance.

Instead, a π-match network was designed with regard to the simplified network shown in Figure 4-3. For simplicity, R_{LNA} can be ignored since its inclusion does not significantly affect the calculations. First, a "large" capacitance C_2 is assumed in parallel to the LNA gates to help reduce the reactance that needs to be cancelled. Next, a reasonable on-chip inductor is chosen with $L = 5$ nH and $Q = 13$ (R_{series} @ 2.5 GHz $\approx 6\ \Omega$). Finally, C_1 is added to tune out any leftover inductance after the real part is matched to 50 Ω.

The matching proceeds by calculating the input admittance of the series RLC

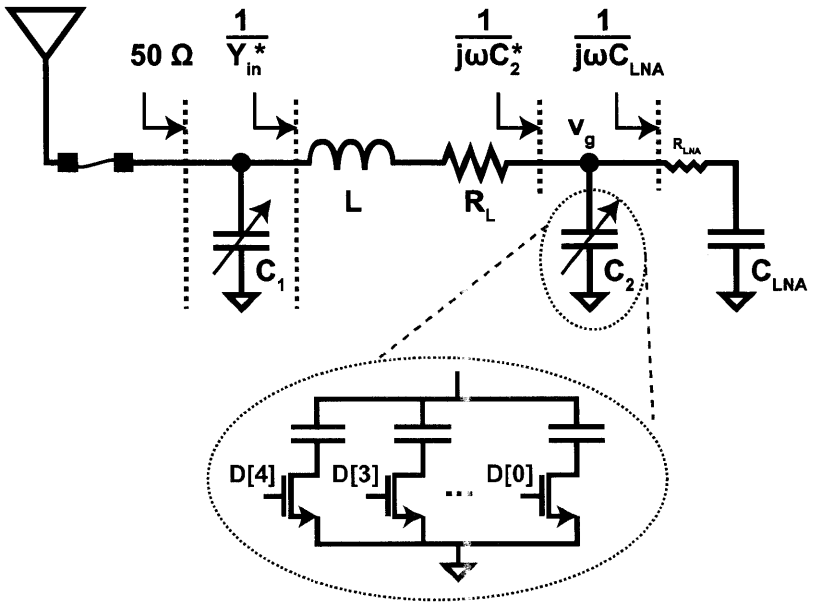


Figure 4-3: π-match network

branch, which yields:

$$\begin{aligned} Y_{in}^* &= \frac{1}{R + j(\omega L - \frac{1}{\omega C_2^*})} \\ &= \underbrace{\frac{R}{R^2 + (\omega L - \frac{1}{\omega C_2^*})^2}}_{G_{in}^*} + j \underbrace{\frac{-(\omega L - \frac{1}{\omega C_2^*})}{R^2 + (\omega L - \frac{1}{\omega C_2^*})^2}}_{B_{in}^*}. \end{aligned} \tag{4.4}$$

By setting $B_{in}^* = \frac{1}{50\ \Omega}$, C_2^* is calculated to be 1.0 pF, which can easily absorb the gate capacitance of the LNAs. C_1 is chosen as 3.4 pF in order to cancel the susceptance from B_{in}^*. C_1 can absorb the pad and package capacitance, and can be adjusted slightly to account for the bondwire inductance. In general C_2 adjusts the real part and C_1 compensates the imaginary part, hence the network was made tunable with binary weighted capacitors in order to adjust the match after fabrication. Additionally, an extracted simulation was performed along with packaging parasitics to fine-tune the match.

The final matching network will be shown in Figure 4-4 along with the biasing

details presented in the next section.

4.1.4 Biasing

Two factors require special consideration when biasing the LNA.

Firstly, the low supply voltage of 0.7 V presents a headroom challenge. In weak inversion, V_{DSAT} is approximately $4V_{thermal} \approx 100$ mV. Despite this, simulation dictates that $V_{DS} = 200$ mV is more comfortable to maintain high enough r_o, limiting the stack height to about 3 transistors. It is therefore not desirable to have a current source directly biasing the LNA as is traditionally done. Instead, the RF signal is ac-coupled to the LNA gate, and the gate's dc-bias voltage is set via a large resistor as shown in Figure 4-4.

The resistor was chosen by examining the RF input impedance of the LNA input transistor, and sizing the resistor to be much larger that the LNA impedance. From simulation, $C_{gs} = 16$ fF and $C_{gd} = 5$ fF. At 2.5 GHz, the impedance is $\frac{1}{j\omega C} \approx -j3$ kΩ. Thus the resistor was chosen to be 100 kΩ so as not to disturb the circuit. The bias voltage is generated by injecting current from an on-chip current DAC into a diode connected transistor in the same fashion as a usual current mirror. The DAC is tunable over a wide range of current for experimentation purposes, from roughly 10 μA to 1 mA.

The second factor in biasing the LNA is that the FBAR acts like a capacitor at all frequencies other than in the immediate vicinity of the resonance. This means that a bias circuit is required in order to allow DC current to flow down the LNA stack. A PMOS transistor current source could be used, with feedback employed in order to equalize the PMOS and NMOS currents and set a stable bias voltage at the output. However, these feedback techniques could be costly to the power budget. Instead, a nice solution is to use a diode-connected PMOS "active inductor" similar to that presented in [44, 45]. Doing so allows the NMOS current mirror to set the bias, however, the frequency response of the active inductor should be tuned to improve

the $\frac{1}{g_{m,p}}$ output impedance to a higher value at 2.5 GHz. The final LNA design is presented in Figure 4-4.

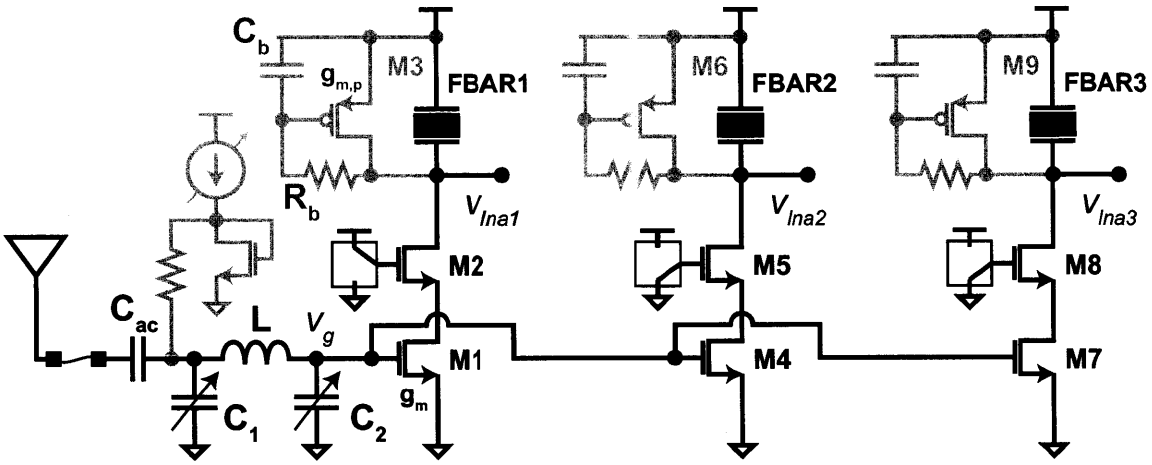


Figure 4-4: Final LNA design with biasing shown in grey

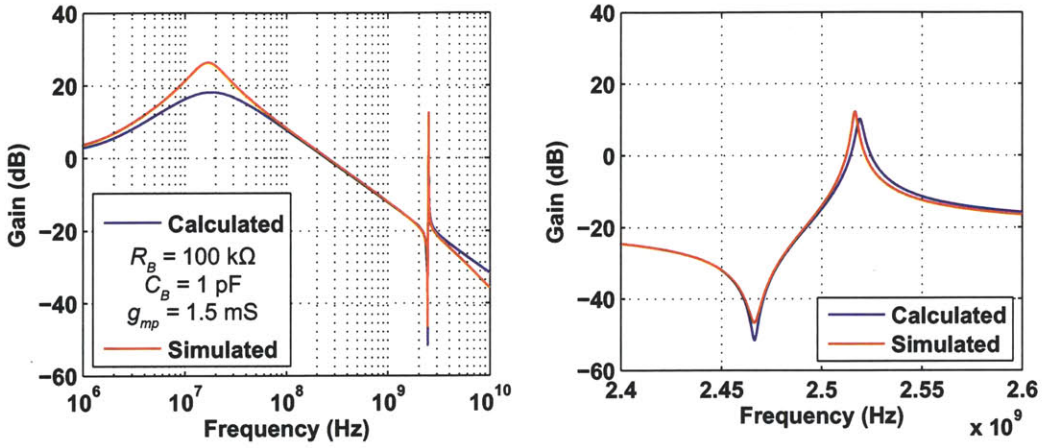
Important tradeoffs were considered when sizing the components. Firstly, since R_B is in parallel with the tank impedance, it must be considerably larger to avoid reducing the tank gain; hence R_B was chosen as 100 kΩ. Next, the DC bias at the LNA output must leave enough headroom for the two transistors underneath. Therefore M3 must be sized large enough to keep the bias point high, but not so large that it's output resistance impacts the response. An example value of $g_{m,p} = 1.5$ mS is chosen for illustrative purposes.

The small signal frequency response of the impedance was derived by considering a test voltage v_t and dividing by the test current i_t:

$$Z_{bias} = \frac{v_t}{i_t} = \frac{1}{g_{m,p}} \left(\frac{1 + sC_B R_B}{1 + s\frac{C_B}{g_{m,p}}} \right). \tag{4.5}$$

A plot of the parallel combination of Z_{bias}, Z_{FBAR}, and $r_{o,bias}$ multiplied by g_m shows that the circuit generates undesirable gain below 1 GHz. In fact, the gain for some frequencies is higher than the 2.5 GHz RF gain!

Some insight can be gained by examining the ratio of the zero and pole location



(a) Wideband calculated and simulated LNA gain

(b) LNA gain zoomed to the FBAR's resonance frequency

Figure 4-5: Calculated and simulated LNA gain

in Z_{bias}:

$$\frac{f_{pole}}{f_{zero}} = g_{m,p}R_B = (1.5 \text{ mS})(100 \text{ k}\Omega) = 150. \tag{4.6}$$

Ideally the pole should take effect at a lower frequency than the zero to minimize the undesired impedance, however, $g_{m,p}$ and R_B cannot be significantly reduced for the reasons discussed above. The solution is to employ a differential mixer structure to reject signals at frequencies below 1 GHz, and this will be described in the next section.

4.2 Mixer

Because a single phase clock minimizes power consumption, a single-ended mixer was analyzed first. In the final mixer design of Figure 4-6, M1, M2 and R_+ form a single phase mixer, where M1 is the input transistor and M2 is driven by the clock. In effect, M1's g_m is modulated by a square wave oscillating between 0 and 1. The gain

is therefore:

$$\frac{v_{mix}(t)}{v_{lna}(t)} = g_m\Big[\underbrace{0.5}_{\text{DC feedthrough}} + \underbrace{\frac{2}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\sin(n\omega_{LO}t)}_{\text{harmonics}}\Big]R_L. \tag{4.7}$$

Incoming RF signals between $\omega_{LO}+\omega_{IF,low}$ and $\omega_{LO}+\omega_{IF,high}$ are down-converted to the IF band by the desired n = 1 harmonic term with a conversion gain of $\frac{1}{\pi}g_mR_L$, where an additional $\frac{1}{2}$ gain has been included due to the multiplication of the RF sinusoid with the LO harmonic sinusoid. The image frequency range between $\omega_{LO}+\omega_{IF,high}$ and $\omega_{LO}-\omega_{IF,low}$ has been rejected by the FBAR filtering and is therefore not considered.

The DC feedthrough term, however, is highly undesirable because of the large amount of IF-band noise from the LNA that it allows to propagate to the IF amplifiers. Therefore, a balanced mixer structure must be used, along with the both the LO and $\overline{LO}$ signals, in order to reject this noise.

In the balanced structure, v^+_{mix} is the same as in (4.7) while v^-_{mix} is also the same except with the sinusoids phase-shifed by 180° (eg. they have minus signs). The differential gain is therefore:

$$\frac{v^+_{mix}(t)-v^-_{mix}(t)}{v_{lna}(t)} = g_m\Big[\frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\sin(n\omega_{LO}t)\Big]R_L, \tag{4.8}$$

where the DC term has been eliminated and the conversion gain is doubled.

Multiplexing of the three mixers can be achieved by sharing a common resistive load in a wired-OR structure. The circuit is shown in Figure 4-6

Since the transistors will be biased in subthreshold, the maximum gain achievable from a resistively loaded amplifier is limited by the voltage headroom as seen by the following relation:

$$A = g_mR_L = \left(\frac{I_D}{nV_T}\right)R_L = \frac{V_{swing}}{nV_T}. \tag{4.9}$$

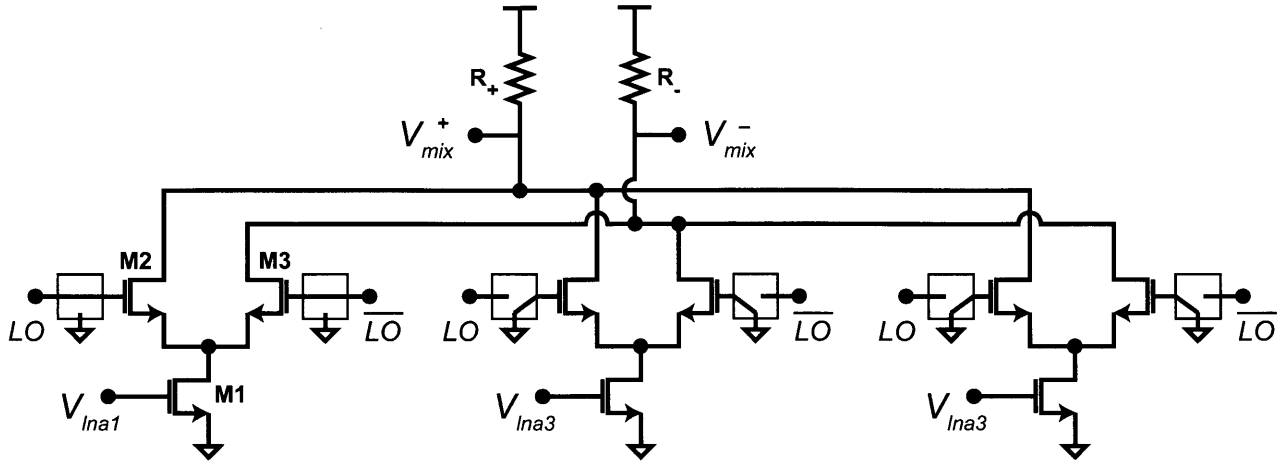


Figure 4-6: Three mixers with a wired-OR connection

The value of the resistor is set so that the high frequency pole at the output of the mixer is at 100 MHz. Assuming a 60 fF fixed capacitance from all the mixer drains plus the routing, the resistor is therefore 25 kΩ. With a voltage headroom of roughly $V_{swing} \approx 200$ mV, the bias current is therefore set to 8 μA per resistor, or 16 μA total for the mixer. Assuming a typical value for the subthreshold slope factor ($n = 1.5$), the theoretical conversion gain for the desired -1 sideband calculated using (4.8) and (4.9) is 16 dB.

In order to reject the DC feedthrough, it is essential for LO and $\overline{LO}$ to have matched duty cycles. For matched 50% duty cycles, the DC term is perfectly rejected (simulated to -70 dB). Figure 4-7 shows the effect of slight mismatches. While the desired sideband's gain is relatively unaffected by small differences in duty cycle, the DC feedthrough gain starts to become significant even for a 1% mismatch. Therefore, the oscillator topology should generate matched duty cycles for LO and $\overline{LO}$ as much as possible.

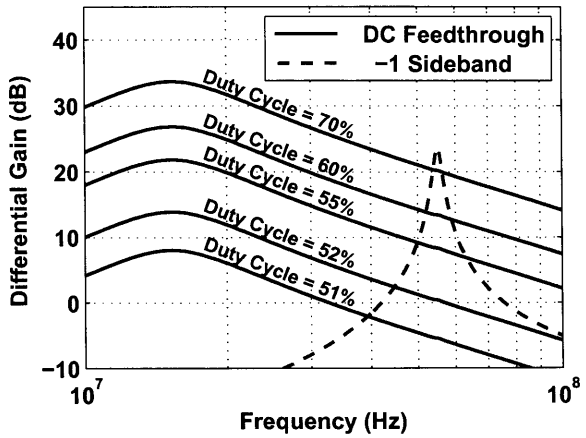


Figure 4-7: Conversion gain from the LNA gate to the differential mixer output showing the effect of duty cycle mismatch on the DC feedthrough gain

4.3 Oscillator

A three-stage ring oscillator was designed to operate at 2.5 GHz, where three stages were selected to minimize CV^2 losses. The circuit and its buffers are presented in Figure 4-8. The main considerations in designing the oscillator were frequency tunability, duty cycle control, and $\overline{LO}$ generation.

Ring oscillators are typically tuned by current starving, either with tunable resistors or tunable current sources. Both of these methods were analyzed via simulation. For less than 50 MHz tuning accuracy, resistance tuning steps of less than 3%, or current source tuning steps of less than 2.5% are required. Though in current source tuning, a small amount of overhead power consumption is required due to mirroring, this method was selected because on-chip resistors are known to be poorly controlled in CMOS processes (typically $\approx$ 25% accuracy).

The duty cycle is a function of the finite rise time of the oscillator signal at node x, and the midpoint of the virtual supply rail voltages with respect to inverter $I1$'s switching threshold. By adjusting the relative current difference between the top and bottom current sources, the virtual supply rails can be simultaneously shifted

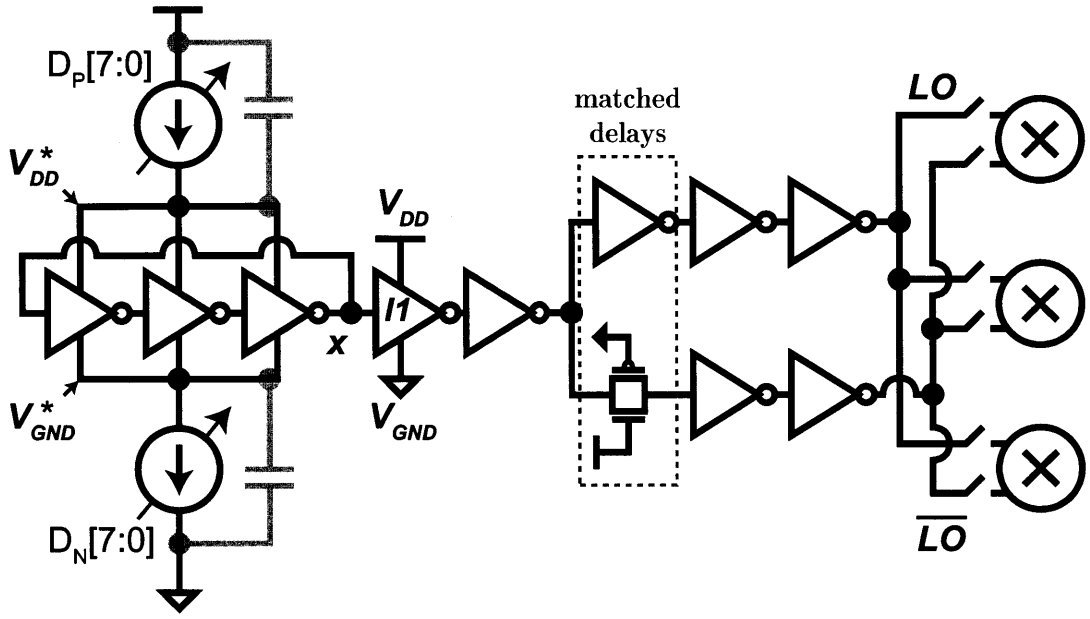


Figure 4-8: Three-stage ring oscillator with current starving and $\overline{LO}$ generation

upwards or downwards in voltage without significantly affecting the frequency of the oscillation. This adjusts the time at which the oscillator crosses the inverter's switching threshold, and hence, tunes the duty cycle. The adjustment of the duty cycle versus the current difference between the top and bottom current sources is illustrated in Figure 4-9.

The inverse LO was generated by matching the delay of a pass transistor with an inverter [57]. Sizing of the pass-gate was achieved via simulation over all process corners. The worst case deviation from a perfect 180° phase was 13° in the slow-slow corner.

4.4 IF gain

This project uses a differential bandpass resistively-loaded amplifier shown in Figure 4-10 [58]. The key design considerations in this work are the passband gain, and the bandwidth.

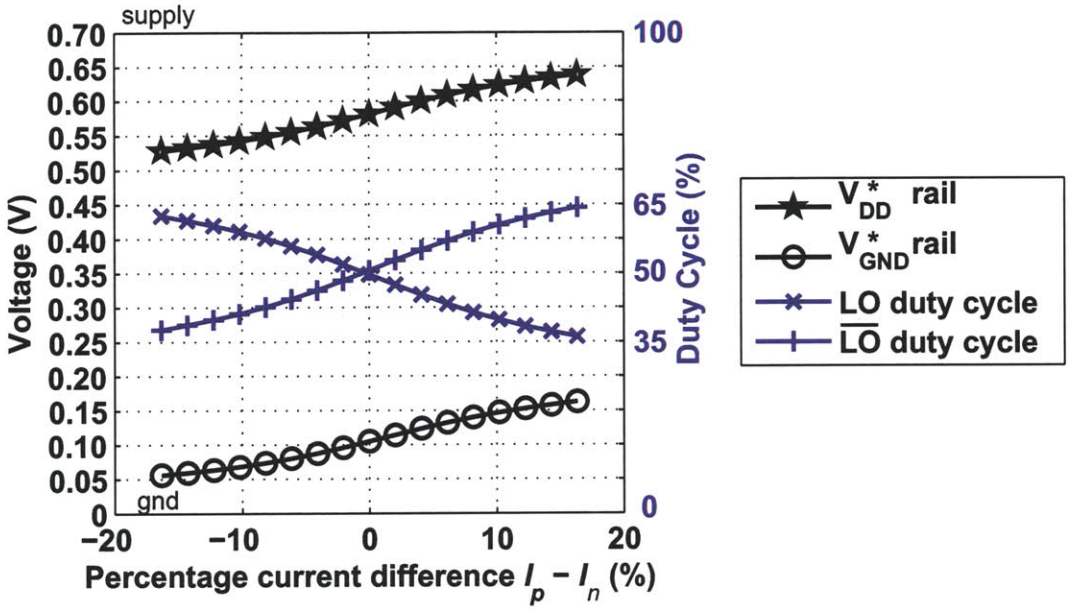


Figure 4-9: Tuning the LO and $\overline{LO}$ duty cycles using mismatch in the current sources

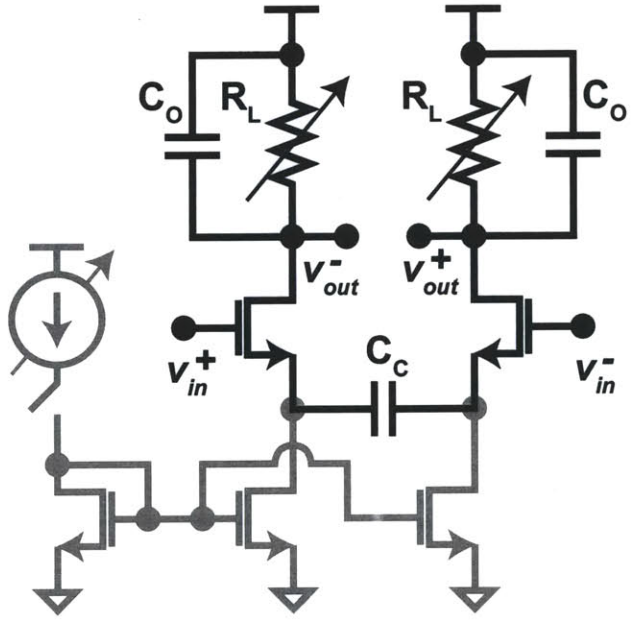


Figure 4-10: Offset-compensated resistively-loaded IF amplifier

Since the transistors are biased in subthreshold for maximum g_m over I_D efficiency, the overall gain for each stage is again limited by the available swing as expressed previously in (4.9). The theoretical maximum gain, assuming $V_{swing} = 200$ mV, typical $n = 1.5$, and $V_T = 26$ mV, is 14 dB per stage.

The differential frequency response for a single IF stage was derived with r_o ignored for simplicity:

$$\frac{v_{od}}{v_{id}} = g_m R_L \left(\frac{s\frac{C_C}{g_m}}{s\frac{C_C}{g_m} + 1} \right) \left(\frac{1}{1 + sR_L C_O} \right). \tag{4.10}$$

The upper pole is set by the fixed capacitance at the drain of each IF stage, comprising the output capacitance of the current stage, the input capacitance of the next stage, the envelope detector capacitance, and the routing. A fixed capacitance from all sources of 40 fF is assumed, setting the resistor to 40 kΩ for a low-pass corner at 100 MHz. This sets the drain current $I_{B,IF}$ to 5 μA, after which the high-pass corner $\frac{g_m}{C_C}$ is placed at 10 MHz by choosing C_C.

The simulated passband frequency response is shown in Figure 4-11. The maxi-

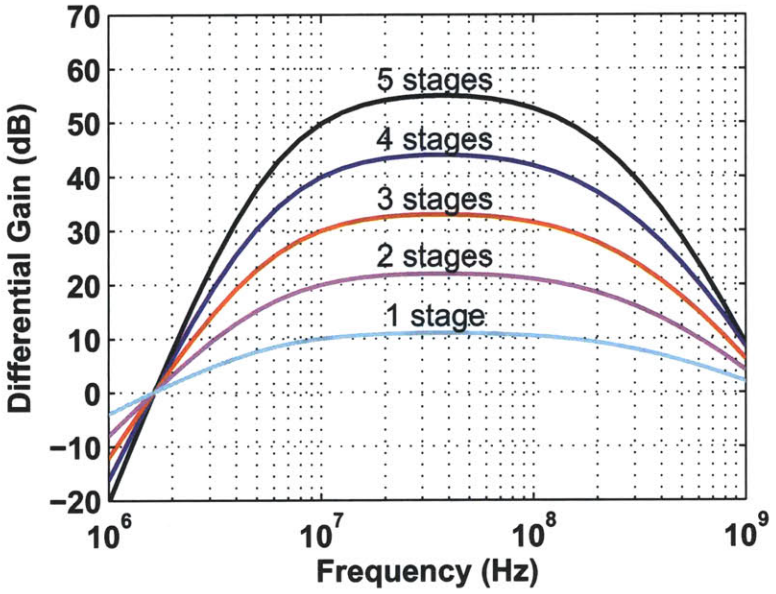


Figure 4-11: IF frequency response for various stage lengths

mum gain when all 5 stages are active is 54 dB or about 10.8 dB per stage. The -3 dB bandwidth is approximately 10 to 100 MHz for all of the configurations.

4.5 Envelope detector

The final analog processing block of the design is the envelope detector. The classic envelope detector, consisting of a diode rectifier in series with a capacitor, cannot be implemented here due to the lack of headroom. However, an envelope detector can still be constructed by substituting the diode with the exponential response of a subthreshold-biased MOSFET. The circuit is shown in Figure 4-12.

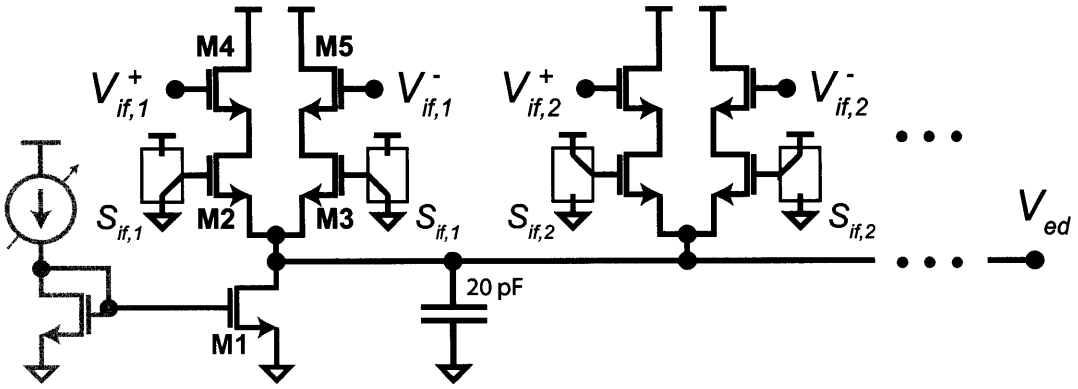


Figure 4-12: Envelope detector circuit for selecting an IF stage

The architecture allows multiple IF-gain stages to be multiplexed onto a single 20 pF output capacitor. A similar approach to [58] was used here, keeping in mind that instead of multiple IF-gain paths with varying lengths, there is a single chain of IF amplifiers from which the IF signal can be extracted from the output of any one stage.

This fact meant that careful co-layout of the IF and envelope detector stages was required. Metal lines operating at the IF frequency needed to be kept extremely short to minimize capacitance (< 20 fF) and maintain the 100 MHz frequency response. By contrast, lines connecting the envelope detector transistor to it's 20 pF output

capacitor could be much longer.

4.6 Noise simulation

Though an exact modeling of the total receiver noise is complicated by the presence of the non-linear envelope detector and the wideband IF stages, an approximate analysis can be performed by simulating the noise output of each of the blocks, and referring the noise to the antenna input.

The first step is to determine how the noise from each stage will be filtered before reaching the output. In the case of the antenna and LNA, only noise contained within the noise bandwidth of the FBAR will be propagated to the output, whereas for the mixer and IF stages, all noise in the 10 to 100 MHz will be propagated. Next, the spectral densities for each block can be determined via SPECTRE® noise and pnoise simulations. Finally the input referred contributions from each block can be calculated using the following formula:

$$P_{n,in} = \underbrace{kTB_{n,lna}}_{P_{n,in,ant}} + \underbrace{\frac{N_{lna}B_{n,lna}}{A_{lna}(50\ \Omega)}}_{P_{n,in,lna}} + \underbrace{\frac{N_{mix}B_{n,mix}}{A_{mix}A_{lna}(50\ \Omega)}}_{P_{n,in,mix}} + \underbrace{\frac{N_{if1}B_{n,if1}}{A_{if1}A_{mix}A_{lna}(50\ \Omega)}}_{P_{n,in,if1}} + \cdots. \quad (4.11)$$

The results of this analysis are presented in Table 4.1.

The analysis calculates the total input referred noise to be -82.5 dBm. Accounting for the 10 dB SNR required for OOK demodulation, plus some additional margin, the analysis suggests that a sensitivity on the order of -70 dBm should be expected. The analysis also confirms that the first wideband block, eg. the mixer, is the limiting block for noise performance. It also suggests that the receiver sensitivity should trade off proportionally with LNA gain since doubling the LNA gain reduces the input referred noise by $\frac{1}{2}$. Relating this to LNA power consumption, a doubling of the LNA current should increase the LNA gain by 6 dB, and hence reduce the input

Table 4.1: Simulation of noise sources in the receive chain

Block	Gain A_{block} (dB)	Noise PSD N_{block} (V^2_{rms})	Noise Bandwidth $B_{n,block}$ (MHz)	Input Referred Noise $P_{n,in,block}$ (fW)
Antenna	0	4.1×10^{-21}	5	0.4
LNA	20.6	9.6×10^{-17}	5	83.6
Mixer	13.2	7.0×10^{-15}	90	5250.0
IF Stage 1	10.8	4.0×10^{-15}	90	250.0
IF Stage 2	10.8	4.0×10^{-15}	90	20.8
IF Stage 3	10.8	4.0×10^{-15}	90	1.7
Total noise (in dBm)				**5606.5 -82.5 dBm**

referred noise by 6 dBm. The can be used to adapt the receiver sensitivity to the channel conditions if required.

Chapter 5

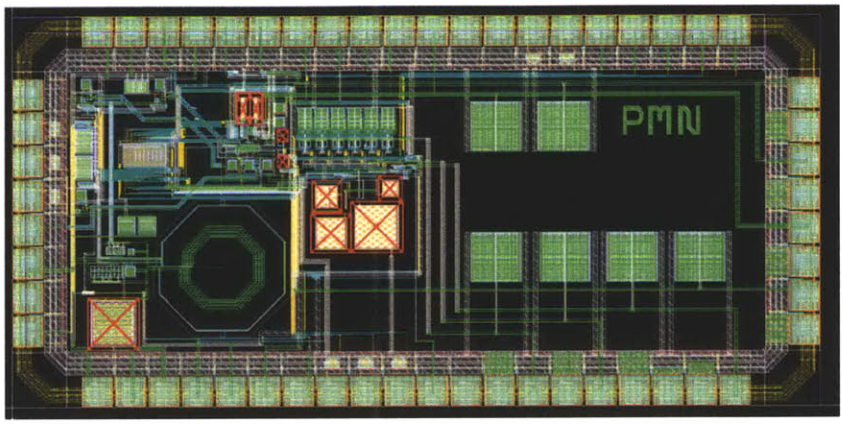
Results

This chapter presents simulation and measurement results for the ultra-low power multi-channel receiver designed in this thesis. First the CMOS implementation, packaging, and measurement set-up will be described. Next, measurement results will be provided including the power consumption, BER, frequency response, input return loss, and scalability of the sensitivity with LNA efficiency. These measurements will confirm that an excellent energy efficiency has been obtained due to the low power consumption and high data rate.

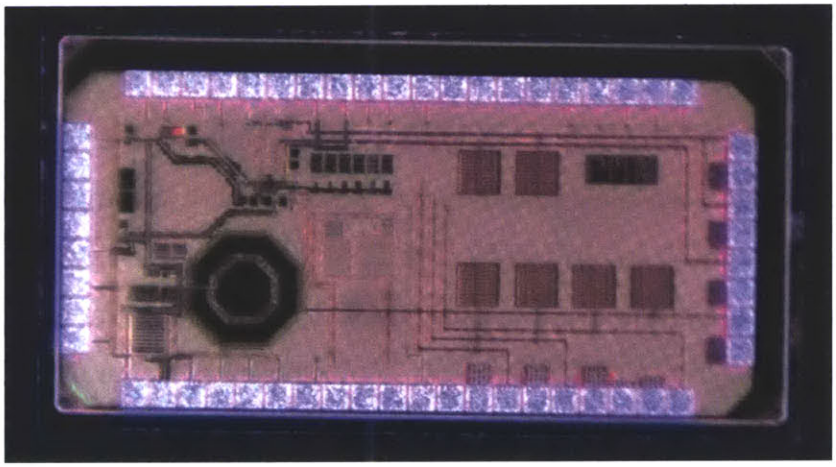
5.1 CMOS Implementation and packaging

The receiver prototype was designed and implemented in a 65 nm standard CMOS technology. A detailed layout screenshot and a die photo of the 2 mm x 2 mm fabricated IC are presented in Figure 5-1a and 5-1b respectively. For RF-specific components, the process featured Metal-Insulator-Metal (MiM) capacitors and a thick top-layer metal for the on-chip inductor in the matching network.

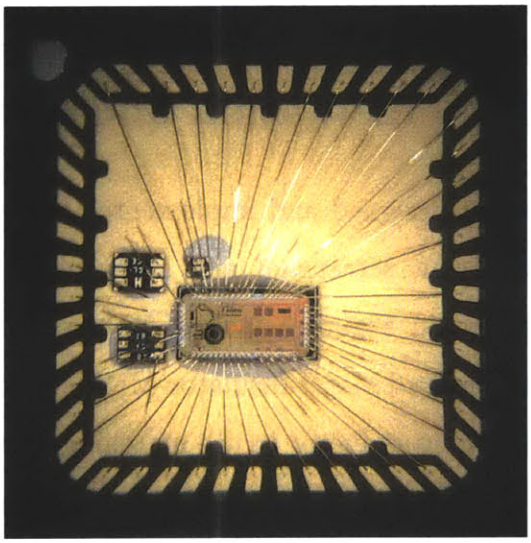
Aspects of the final design were influenced by testing and experimentation concerns, and some additional testing circuitry has been added to aid in the characterization of it's performance:



(a) Layout screenshot



(b) Die photo



(c) Packaging with three FBAR resonators

Figure 5-1: Prototype layout, CMOS die photo, and packaging

1. A **serial shift register** is used to configure all of the internal tunable components including capacitors, resistors, and the bias currents and shutdown state of all the main circuit blocks.

2. Each circuit block features a **binary-weighted current DAC** to adjust it's DC bias point. An on-chip current mirror network supplies reference currents to all of the on-chip DACs, and is referenced to a single off-chip resistor. The DACs can also be individually overridden by external resistors if required.

3. Each main block features it's own **separate supply rail** with 20 pF of on-chip supply decoupling per rail.

4. A series of flip flops operate as a **clock divider** to divide down the *LO* by 128× so that its frequency can be measured off-chip.

5. A **unity-gain opamp buffer** is used to drive the envelope detector output to an off-chip.

Finally the design was packaged in a QFN48 package along with three FBAR resonators supplied by Avago technologies (Figure 5-1c).

The next section details the measurement set-up used to obtain the results in Section 5.3.

5.2 Measurement Set-up

Two boards were fabricated for the purposes of the testing the IC and are shown in Figure 5-2. The IC itself is mounted on a small daughterboard that contains an SMA connector and a 50 Ω transmission line for the RF input. The daugherboard also contains a simple opamp circuit configured to provide gain to the envelope detector output so that it fills a majority of the full-scale range of the ADC. The daughterboard interfaces to a mainboard that contains support circuitry. Most notably, the

mainboard contains the ADC, some level shifters and voltage regulators, and a series of jumpers that provide the capability to power each of the design blocks from either the on-board 0.7 V regulator or an external source connected via BNC cable. Finally, the mainboard plugs into an Opal Kelly® XEM3001v2 which contains a Xilinx® FPGA capable of implementing custom logic.

The measurement set-up used to quantify the BER is presented in Figure 5-3. An Agilent® 8267C Vector Signal Generator (VSG) was used to modulate OOK data on to a 2.5 GHz carrier for transmission over a 50 Ω coaxial cable to the RF test board. The Real-Time I/Q baseband mode is used, with a custom I/Q constellation for OOK, and an internal control loop that ensures the average modulated output power matches the power level demanded by the PC. A linear feedback shift register (LFSR) configured as a Pseudo-Noise (PN) generator supplies continuous random data to the signal generator's baseband. At the time a measurement is to be performed, a trigger from the PC enables the FIFO and captures the current state of the PN generator. On the PC, the captured state is used to seed an identical software-based PN generator which reconstructs the PN-sequence and compares it to the demodulated OOK data. The OOK demodulation threshold is taken as the average of the incoming digital codes given that the PN-sequence generates approximately equal quantities of 1s and 0s.

5.3 Measured and Simulated Results

This section will present the measurement and simulation results for the multi-channel receiver. Since there is some flexibility in trading off the power consumption for sensitivity, the data will be presented at the default power and gain settings shown in Figure 5-4. Finally, this section will conclude with a plot showing how the energy efficiency can be traded for sensitivity.

Figure 5-4 shows the measured power consumption and the simulated gain for

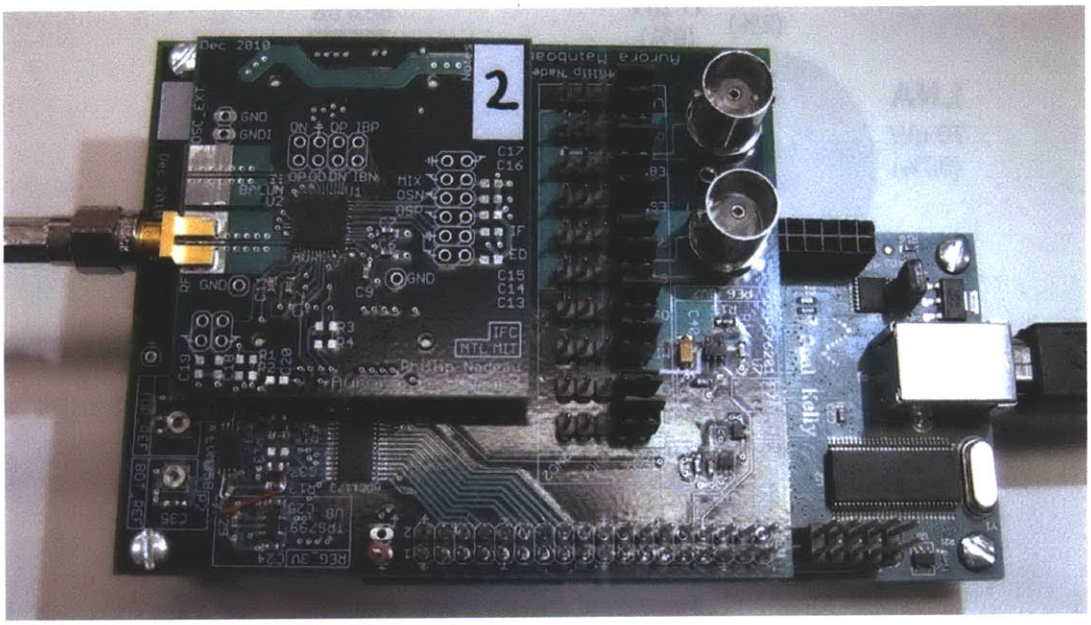


Figure 5-2: Test boards

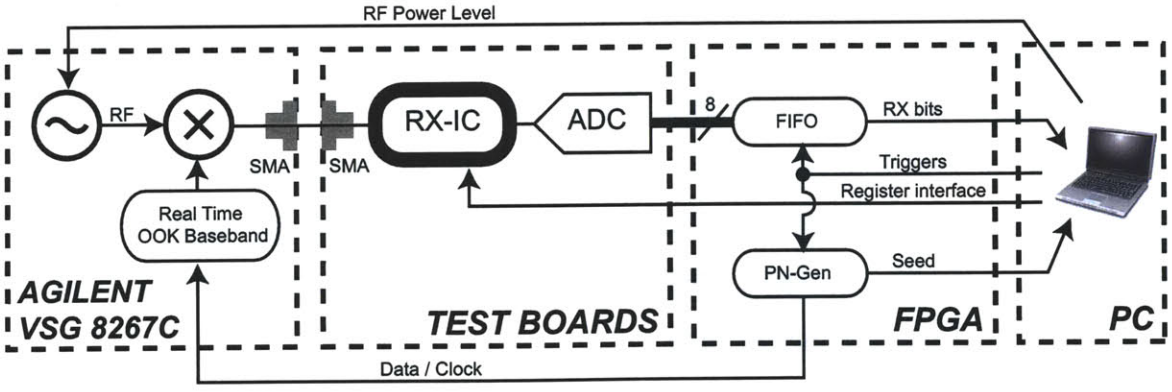
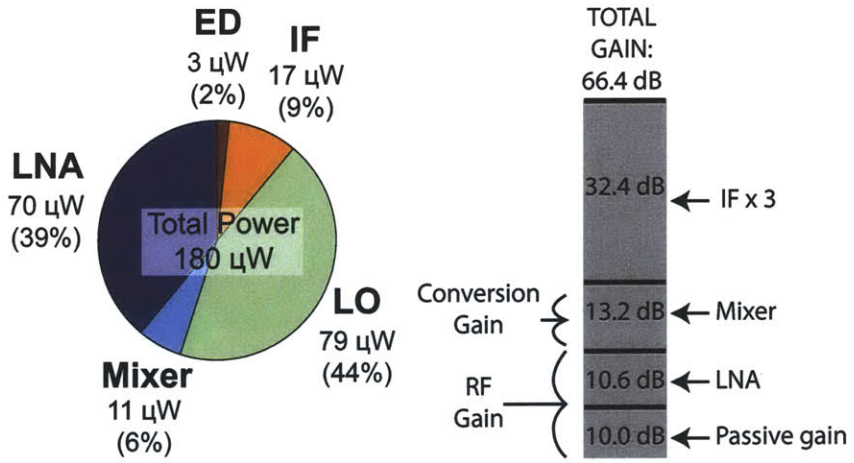


Figure 5-3: Measurement setup



(a) Measured power consumption by block

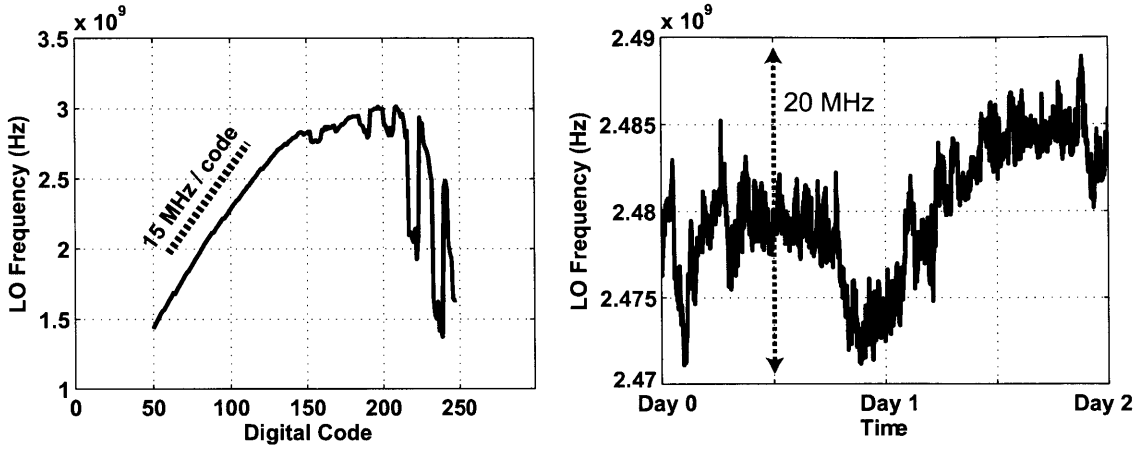
(b) Simulated gain by block

Figure 5-4: System power consumption and gain by block

each of the blocks for the default setting. The total power consumption for all the blocks is 180 uW and the total simulated signal gain prior to the envelope detector is 66.2 dB. It should be noted that these figures reflect only three stages of IF gain since, as will be shown shortly, three stages are optimum from a noise performance perspective.

Figure 5-5 shows some of the measured characteristics of the ring oscillator. First, the ring oscillator digital codes (D_N and D_P) were varied together over their eight bits of tuning range from 0 to 255. Figure 5-5a shows how the frequency increases and then crests at roughly 3 GHz. At this point, it is likely that one of the nodes in LO chain or testing circuit is no longer able to switch fast enough, and therefore the frequency no longer increases. The mean frequency step in the monotonic region of the plot is 15 MHz per digital code.

Next, the oscillator was set at roughly 2.48 GHz and was allowed to run freely at room temperature for two uninterrupted days. Frequency measurements were recorded for every minute, and the results of the two-day test are shown in Figure 5-5b. The frequency variation was no more than 20 MHz over the course of the test,



(a) Tuning the ring oscillator frequency

(b) Variation in the ring oscillator frequency over the course of 2 days

Figure 5-5: Ring oscillator characteristics

which indicates that only periodic frequency calibration is required in slow-changing temperature conditions.

Figure 5-6 shows a family of BER waterfall curves, each measured with a different number of IF gain stages enabled as indicated in the legend. With both four and five gain stages enabled, the BER no longer decreases monotonically with increasing input power. This is likely due to the envelope detector becoming saturated, firstly, by the output noise, and secondly, at higher power levels, from the gained input signal itself. In fact, based on the noise simulation results presented in Table 4.1, the noise level referred to the envelope detector input for five IF gain stages can be tabulated as 400 mV_{rms}, which is very near to the saturation regime for the envelope detector.

Figure 5-7a presents the frequency response of the receiver over the three channels. The channel center frequencies are a result of the parallel resonance of the FBARs selected in the packaging. To generate the plot, a -50 dBm RF input was swept over the frequency range while the envelope detector's output was measured and normalized to the DC bias level. The average -3 dB bandwidth across three packaged dies is 6.4 MHz as measured at the detector output. The packaging parasitics and

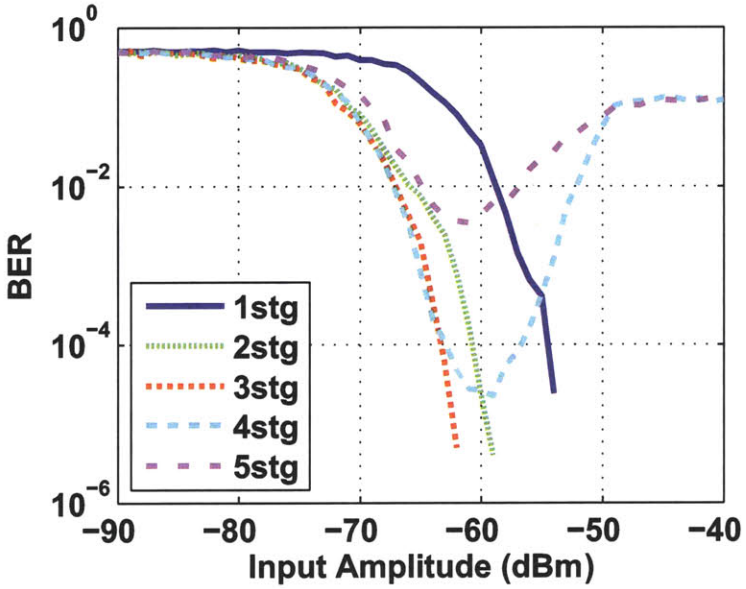
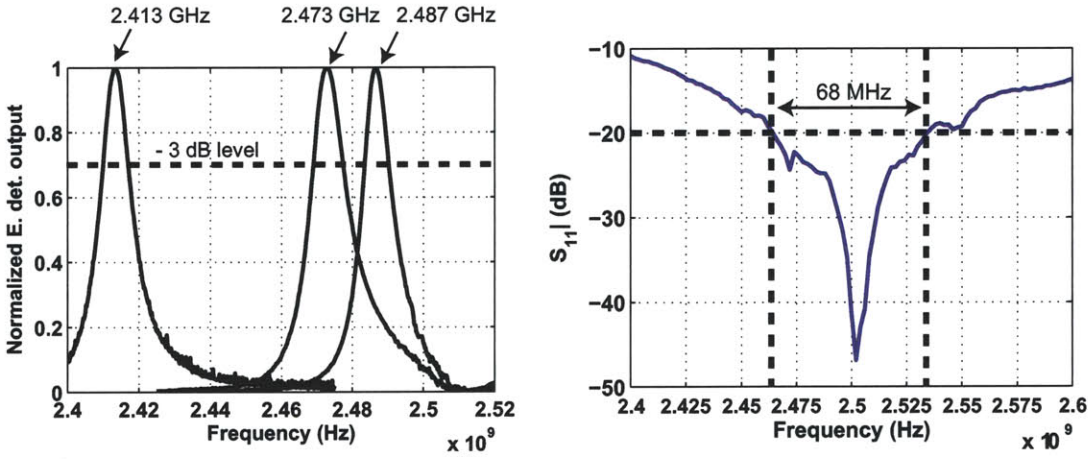


Figure 5-6: BER waterfall curves for varying number of IF gain stages



(a) Receive chain frequency response

(b) Insertion loss versus frequency

Figure 5-7: Frequency response measurements

the non-linear nature of the envelope detector are responsible for the degradation in the 3 dB bandwidth from the ideal 1.9 MHz discussed in Chapter 3. In Figure 5-7b, the return loss (S_{11}) was measured with the on-chip matching network configured to place the notch at 2.5 GHz. The plot shows better than -20 dB return loss across a bandwidth of 68 MHz.

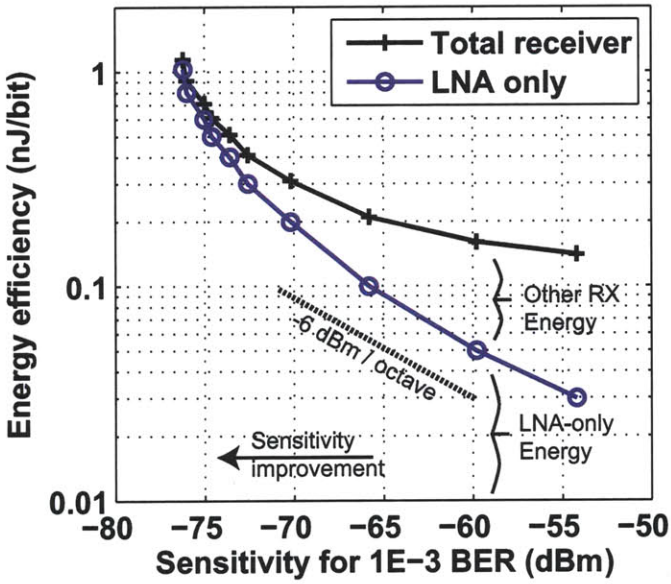


Figure 5-8: Tradeoff between energy per bit and sensitivity

Next, the tradeoff between energy efficiency and receiver sensitivity for this particular architecture was measured (Figure 5-8). In order to perform the measurement, the LNA power supply was boosted from 0.7 V to 1.0 V to provide sufficient headroom to the transistors at the highest power settings. As the LNA current varied from 30 μA to 1 mA, BER measurements were taken and the 10^{-3} sensitivity point was used to create a plot of energy per bit versus sensitivity. Both the LNA-only and total receiver energies are shown.

The noise simulation results presented in Table 4.1 suggested that the mixer was the limiting stage for sensitivity, and that additional LNA gain should improve the sensitivity at a rate of -6 dBm per octave of LNA power consumption. Below 100

pJ/bit LNA-only energy, the tradeoff follows the predicted trend very closely. At higher power levels, the LNA gain begins to saturate due to a worsening output resistance from transistor M3 in Figure 4-4 which in turn causes a reduced resonance quality factor. This effect serves to dampen the sensitivity improvement at higher power levels.

Finally, the startup time of the receiver was measured as 6 μs from the rising edge of the shift register interface's strobe signal until the time at which the first bits appear at the output of the envelope detector.

5.4 Results Summary

The measured and simulated results reported above have been summarized and presented in Table 5.1 alongside the most relevant previously published low-power receivers.

Table 5.1: Summary and comparison to related work

Ref	Freq. (GHz)	Rate (kbps)	Power (μW)	E/bit (pJ/bit)	Sens. (dBm)	-3 dB BW (MHz)	no. chan.
[44]	1.9	80	3600	45000	-78	3	2
[28]	2	200	52	260	-70	< 10	1
[29]	2.4	500	415	830	-82	~ 40	1
[30]	2.4	100	51	510	-64	59	1
This work							
(Low E)	2.4	1000	140	140	-55	6	3
(Med. E)	2.4	1000	180	180	-65	6	3
(High E)	2.4	1000	1140	1140	-77	6	3

In general, the results show the architecture is very competitive with recently published designs in terms of its energy per bit and sensitivity.

In particular, compared to the multi-channel MEMS-based receiver in [44], this work represents a substantial improvement in energy efficiency. Also, compared to

[29] and [30], this design has an improved bandwidth efficiency due to the use of MEMS resonators.

Chapter 6

Conclusions

6.1 Thesis summary

In wireless body-worn medical systems, a key bottleneck is the high power consumption of the radio components. This leads to shortened device lifetimes, bulky energy storage requirements, and the inability to power the system from scavenged energy. In addition, for operation in unlicensed frequencies bands, a key challenge is the presence of multiple users transmitting simultaneously at different frequencies within the allocated spectrum. This can lead to very unreliable operation if the transceiver system operates only at a single fixed frequency.

To address both of these challenges, a highly energy efficient multi-channel receiver has been presented. The design leverages some of the main opportunities in Body Area Networks to improve energy efficiency, including reduced communication distances, buffered low rate medical data for high rate transmission, and a star network topology. The design also leverages the benefits of MEMS resonator technology in order to provide better frequency selectivity at low power.

The presented non-coherent narrowband receiver is capable of operating in the 2.4 GHz ISM band and achieves 180 pJ/bit at -65 dBm sensitivity while providing three selectable frequency channels of operation. The use of MEMS resonators, a low power

ring oscillator, simple envelope detection, and a low V_{dd} of 0.7 V have all contributed to the low power consumption. The channel selection has been enabled by the use of multiple MEMS resonators and an architecture to select them dynamically. With a startup time of 6 bit periods and a maximum data rate of 1 Mbps, the design is also highly amenable to duty cycling in order to achieve a very low average power while minimizing waste energy.

6.2 Future Directions

With the upcoming IEEE 802.15.6 Wireless Body Area Network standard, and a potential future market for body-worn wireless medical systems, there are a number of exciting potential directions for this research. Two areas that will be specifically highlighted are directions in MEMS integration, and directions for integrated low power on-body health systems.

Over the last two decades, Micro-Electro-Mechanical Systems have revolutionized electronics in such diverse applications as television, gaming, and communications. It is worth noting however, that in many applications, including the receiver in this project, the MEMS devices and the CMOS are fabricated on separate substrates to take advantage of specialized materials and processing steps. With FBARs in particular, a number of techniques are helping to ease integration, including above-IC fabrication [59], flip-chip bonding [60], and through-silicon-vias [45]. But with an eye on cost and size minimization, an imporant direction for research in MEMS-based transceivers is total integration of RF-MEMS resonators with standard CMOS processes [61, 62]. Integration brings some key advantages including reduced cost from off-chip components, reduced parasitic loading from pads and bondwires, and the opportunity to employ redundancy to combat variation since many devices could be fabricated very inexpensively. Two key challenges should be overcome in order to realize more opportunities for integrated resonators. The first is the development

of new techniques to help reduce or handle the high motional impedance of silicon resonators. Currently, the motional impedance presents a challenge to filtering with low insertion loss. The second is a reduced dependence on specialized processing steps, which would bring about additional cost savings compared to today's technology.

With separate advances in ultra low power transmitters [63], efficient biomedical signal processors [64], and energy harvesting circuits [65], another exciting direction is integration of all of these components into an energy-efficient on-body sensor node. When creating such a system, size and overall energy efficiency are the goals, and therefore, important system-level concerns should be addressed. Bringing together a system would require work on power management for each of the components to control peak demand and to duty cycle components that are not in use. It would also require an energy-efficient medium access protocol that minimizes the transceiver overhead. Finally, integration into a small form-factor poses unique challenges for the energy harvester and energy storage components, and the power electronics circuitry.

In summary, an energy efficient multi-channel narrowband receiver has been presented in this thesis. However, a number of important integration challenges still remain, including integration with MEMS filters, and the development of a self-powered on-body medical system that brings together research on the various components into a single integrated system.

Appendix A

List of Acronyms

150-GSG: 150 μm-pitch, Ground-Signal-Ground probe

BAN: Body Area Network

BAR: Bulk Acoustic Resonator

BCC: Body Coupled Communication

BER: Bit Error Rate

DAC: Digital to Analog Converter

FBAR: Film Bulk Acoustic Resonator

FCC: Federal Communications Commission

FIFO: First-In First-Out

FSK: Frequency Shift Keying

IEEE: Institute of Electrical and Electronics Engineers

IF: Intermediate Frequency

ISM: Industrial-Scientific-Medical

ISSCC: International Solid-State Circuits Conference

JSSC: Journal of Solid-State Circuits

LFSR: Linear Feedback Shift Register

LNA: Low Noise Amplifier

LO: Local Oscillator

MAC: Medium Access Control

mBVD: Modified Butterworth-Van-Dyke model

MEMS: Micro-Electro-Mechanical Systems

OOK: On-Off Keying

Q: Quality Factor

QAM: Quadrature Amplitude Modulation

QPSK: Quadrature Phase-Shift Keying

PCM: Process Control Monitoring

PHY: Physical Layer

PLL: Phase-locked loop

PN: Pseudo-Noise

PPM: Pulse-Position Modulation

RF: Radio Frequency

SoC: System on Chip

UWB: Ultra-Wideband

VSG: Vector Signal Generator

WBAN: Wireless Body Area Network

WSN: Wireless Sensor Network

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