6.061 / 6.690 Introduction to Electric Power Systems
Spring 2007

Massachusetts Institute of Technology

Department of Electrical Engineering and Computer Science

6.061 and 6.690 Introduction to Power Systems

Problem Set 3

Issued: Ses #5

Due: Ses #9

Problem 1: Here is a simple transmission line problem, shown in Figure 1.

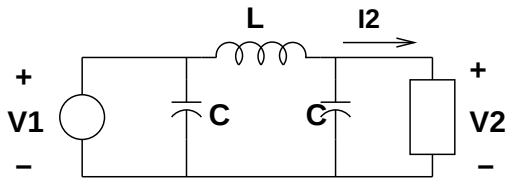

Figure 1: Transmission Line

Assume the transmission line reactance $X_L = \omega L = 5\Omega$. The voltage source at the left end maintains the voltage at 10 kV, RMS. This is a 60 Hz system. The load (represented by a rectangular box) draws a constant load of 10 MW at unity power factor, indepenent of voltage (well, independent of voltage within the range of voltages to be encountered in this problem).

1. Assume the two capacitors are sized so that the terminal voltage across the load has the same magnitude as the source $V_2 = 10$kV. Draw a phasor diagram showing the relationship between the voltages of the two sources and the voltage drop across the transmission line inductance. Try to get the angle about right and label it.
2. Estimate the value of capacitance C that must be used at the load end so that voltage at that end is the same as that of the source.
3. If the same value of capacitance is used at the source end, what is the power factor seen by the source?
4. Draw a phasor diagram showing the current out of the left hand source, into the right hand source, through the line and through each of the two capacitances.

Problem 2: This, too, is a transmission line problem. The situation is shown in Figure 2. The 8 kV (RMS) source is feeding a 64Ω load through a transmission line which may be represented as a simple inductance.

1. Assuming both capacitances to be zero, draw a phasor diagram showing sending and receiving end voltages and voltage across the transmission line. What is power dissipated in the resistance?
2. Size the receiving end capacitance C_r so that receiving end voltage is equal in magnitude to sending end voltage.

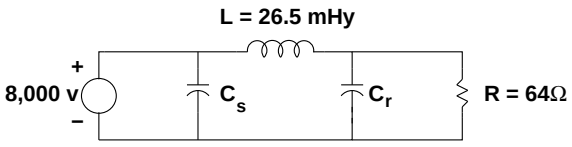

Figure 2: Compensated Load

3. Calculate and plot, over the range of $1\mu F < C_r < 6\mu F$, receiving end voltage. You will probably want to use MATLAB to do the grunge work here.

Problem 3: Figure 3 shows the buck converter you analyzed in Problem Set 2, but with a large-ish capacitance connected across the output. Assume the thing is switching with a frequency of $100kHz$ and a duty cycle of 50%. Assume also that the capacitance is large enough that, as far as computing inductor current is concerned, you can assume output voltage is *about* constant.

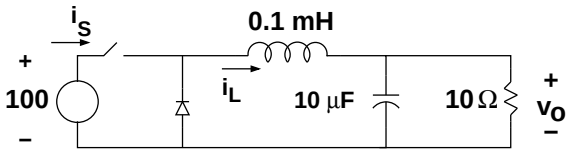

Figure 3: Buck Converter

1. Estimate the minimum and maximum values of inductor current. Sketch and dimension your sketch for inductor current i_L as a function of time.
2. Do the same for source current i_S.
3. Now, following the same assumption about voltage, the load current may be assumed to be about constant. Use this and the for you have established for inductor current to assume voltage variation on the capacitor (ripple voltage). How good was our original assumption?
4. For 6.690 – Optional for 6.061: Get out MATLAB and simulate this system. (Note it will take quite a few cycles to get to steady state).

Problem 4: Figure 4 shows a simple boost converter. Assume the transistor is operated as a simple switch, turned ON with a duty cycle α. The switch is operated with a basic frequency of 100 kHz and the components have values $V_s = 50v$, $L = 100\mu Hy$, $C = 10\mu F, R = 10\Omega$.

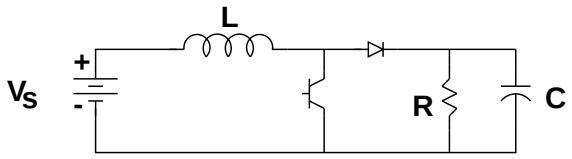

Figure 4: Boost Converter

1. If the duty cycle $\alpha = .5$, what is the average value of the output voltage?
2. Can you estimate the value of ripple voltage at the output?
3. For 6.690 – optional for 6.061: Using MATLAB, simulate this circuit. Are your estimates about right?