Dislocation Density Reduction in Multicrystalline Silicon through Cyclic Annealing

by

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Submitted to the Department of Mechanical Engineering
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ABSTRACT

Multicrystalline silicon solar cells are an important renewable energy technology that have the potential to provide the world with much of its energy. While they are relatively inexpensive, their efficiency is limited by material defects, and in particular by dislocations. Reducing dislocation densities in multicrystalline silicon solar cells could greatly increase their efficiency while only marginally increasing their manufacturing cost, making solar energy much more affordable. Previous studies have shown that applying stress during high temperature annealing can reduce dislocation densities in multicrystalline silicon.

One way to apply stress to blocks of silicon is through cyclic annealing. In this work, small blocks of multicrystalline silicon were subjected to thermal cycling at high temperatures. The stress levels induced by the thermal cycling were modeled using finite element analysis (FEA) on Abaqus CAE and compared to the dislocation density reductions observed in the lab. As too low of stress will have no effect on dislocation density reduction and too high of stress will cause dislocations to multiply, it is important to find the proper intermediate stress level for dislocation density reduction. By comparing the dislocation density reductions observed in the lab to the stress levels predicted by the FEA modeling, this intermediate stress level is determined.

Thesis Supervisor: Tonio Buonassisi
Title: Assistant Professor of Mechanical Engineering

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I would also like to thank my colleagues at MIT, both inside and outside of the Buonassisi group, for the great conversations, help in the lab, and fond memories: Sarah Bernardis, Rupak Chakraborty, Katy Hartman, Eric Johlin, Yun Seog Lee, Sin Cheng Siah, Joe Sullivan, David Needleman, Yaron Segal, Christie Simmons, Mark Winkler, Andre Augusto, Bonna Newman, Steve Hudelson, Sebastian Castro, Vidya Ganapati, Sabine Langkau, Keith Richtman, Jim Serdy, Alison Greenlee, and Erik Verlage. Not only are they great scientists, but they are wonderful people.

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Chapter 1

Introduction

1.1 Multicrystalline silicon solar cells

As environmental and political concerns over energy production have increased in recent years, the search for cheap, abundant renewable energy sources has intensified. Solar energy has the potential to be a large supplier of the world's energy, but the costs have kept it from attaining widespread use. The amount of energy Earth receives from the sun is enormous, totaling 5.5×10^{17} kWh (1,980,000 exajoules) per year [1], ~3800 times the world's total consumption in 2007 (495 quadrillion Btu, or 522 exajoules [2]). The solar resource is greater than any other renewable energy resource [3]. However, solar energy amounted to only 0.15% of energy production in the U.S., as of 2007 [2]. Cost reductions are necessary for solar energy to become more widespread as an energy source.

Crystalline silicon makes up over 90% of the solar industry [4], which is divided roughly evenly between multicrystalline and monocrystalline silicon. Monocrystalline

silicon is produced by a slow, energy-intensive process of drawing a large single crystal from a pool of molten silicon. Multicrystalline silicon, on the other hand, is cast by pouring molten silicon into an ingot, in a much faster but less controlled process [5]. While the monocrystalline silicon production process yields a single perfect crystal, the casting process of multicrystalline silicon leads to many deleterious defects within the material, primarily grain boundaries, dislocations, and impurities, all of which decrease the efficiency of the resulting solar cell. Multicrystalline silicon solar cells are cheaper to produce than monocrystalline silicon cells, but the efficiency losses of multicrystalline silicon cells tend to offset the cheaper production costs. To decrease the cost of solar energy from existing solar technologies, two paths are apparent: higher-efficiency materials could be made cheaper, or cheaper materials could be made more efficient. This work chooses the latter option. By removing or reducing the impact of the defects that make multicrystalline silicon solar cells less efficient than monocrystalline silicon cells, at only a small increase in production cost, the overall cost of electricity from mc-Si solar cells can be reduced.

1.2 Dislocations in multicrystalline silicon

The structure of silicon has been well-studied, thanks to interest from the integrated circuits industry. Silicon has a diamond cubic structure, as shown in Figure 1.1. The diamond cubic structure is a superposition of two fcc lattices, with an (a/4, a/4, a/4) offset. The main dislocation glide plane is the 111 plane, as pictured in the figure. The significant types of dislocations are screw dislocations and 60° dislocations [6].

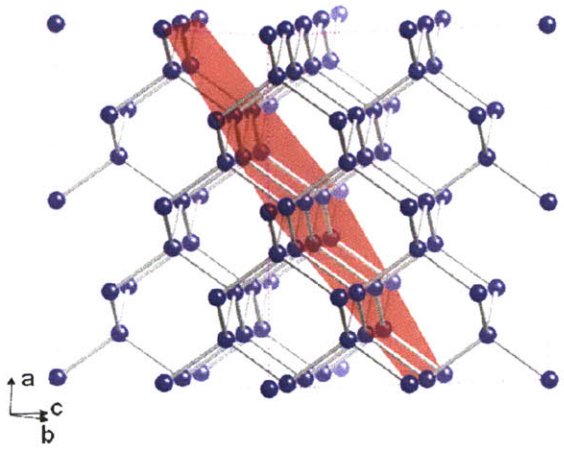


Figure 1.1: Diamond cubic lattice, with 111 glide plane shown. From [7].

Dislocations move through the lattice by glide and climb. They create stress fields in the sample, and interact with other stress fields in the sample [8]. Certain types of dislocations (e.g. edge) of opposite sign exert attractive forces on each other. If these dislocations are mobile, they may move towards each other until they meet and mutually annihilate [8]. The velocity of dislocation motion increases with stress [6]:

$$v = \tau_{eff}^{m} B(T) \qquad 1.1$$

where v is the dislocation velocity, τ_{eff} is the effective shear stress, m is the stress exponent, and $B(T)$ is the Boltzmann factor, which depends on temperature and activation energy.

Dislocation mobility depends heavily on temperature. At low temperatures, the material is in the brittle phase and the dislocations are locked in place [9]. At intermediate temperatures (roughly 500°C - 1000°C) they are mobile on the glide planes. At high temperatures, dislocations are very mobile and move quite freely through the material [10].

1.3 Effect of dislocation density on minority carrier lifetime and cell performance

As line defects, dislocations limit minority carrier lifetime by acting as recombination centers [11]. The effective bulk minority carrier lifetime is determined by the lifetimes as limited by each type of recombination [12]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_T} + \frac{1}{\tau_A} + \frac{1}{\tau_R} \qquad 1.2$$

where τ_{eff} is the net bulk minority carrier lifetime (note the change from equation 1.1), τ_T is the lifetime for non-radiative recombination, τ_A is the lifetime for Auger recombination, and τ_n is the lifetime for radiative recombination. This could also be expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{dislocations}} + \frac{1}{\tau_{impurities}} + \ldots \qquad 1.3$$

listing all of the sources of recombination. This equation shows how important dislocations are in determining the bulk minority carrier lifetime. If a cell has low contamination and excellent properties, it can still have low lifetime if its dislocation density is high (and $\tau_{dislocations}$ is low).

Figure 1.2 shows a map of minority carrier lifetime compared to a map of dislocation density on a silicon wafer. Areas of low lifetime correspond to areas of high dislocation density, and vice versa. Figure 1.3 shows the minority carrier diffusion length (which is directly proportional to minority carrier lifetime) plotted as a function of

dislocation density. Below a certain threshold ($10^4 cm^{-2}$), dislocations have little effect, but past this threshold the diffusion length drops considerably, as does the lifetime.

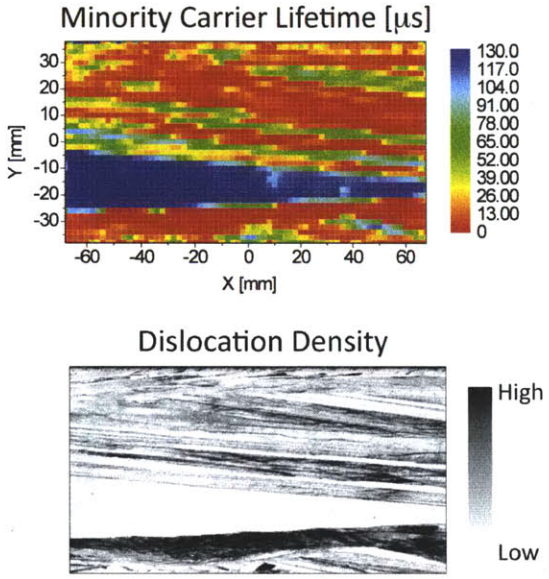


Figure 1.2: These scans of wafers show a strong correlation between low lifetime and high dislocation density. From [13].

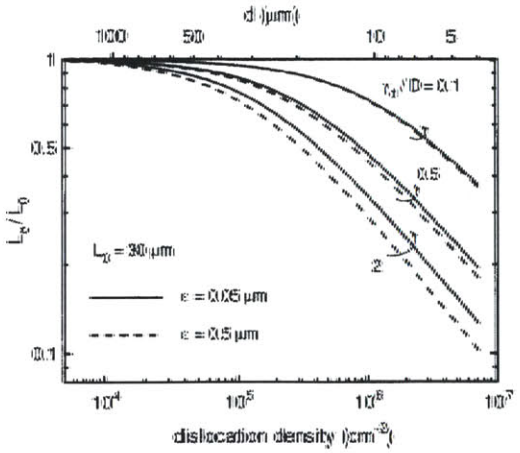


Figure 1.3: The minority carrier diffusion length, which is proportional to the minority carrier lifetime, falls off sharply for dislocation densities higher than $10^4 cm^{-2}$. From [14].

Figures 1.2 and 1.3 clearly show the deleterious effects of dislocations on the minority carrier lifetime. Minority carrier lifetime is an important parameter to the overall cell efficiency. Figure 1.4 shows how increasing the bulk minority carrier lifetime increases the overall cell efficiency proportionately, for most conditions. Therefore, by decreasing dislocation density, the minority carrier lifetime and thus the cell efficiency are increased.

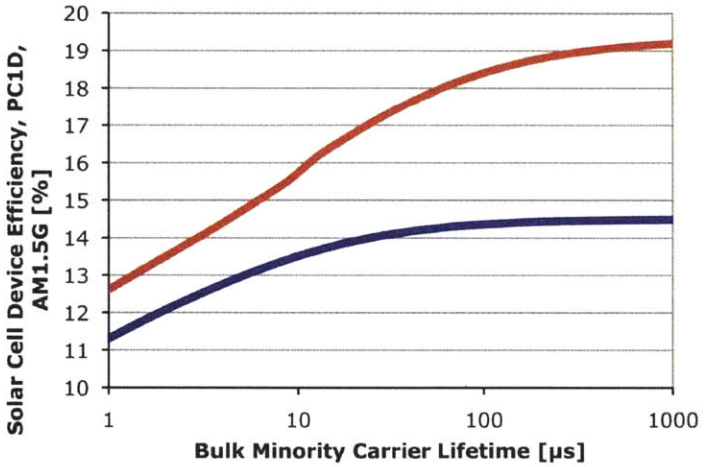


Figure 1.4: The effect of bulk minority carrier lifetime on solar cell efficiency. The red line represents a solar cell with good properties, including good light trapping, low surface recombination, low shunting, and low resistive losses. The blue line represents a solar cell with the opposite properties. From [15].

1.4 Dislocation density reduction through high temperature annealing and applied stress

Since dislocations have such a large impact on solar cell efficiency, many efforts have been made to minimize their impact. Many efforts have focused on avoiding dislocation formation during ingot growth [16, 17]. Recently, efforts have been made to remove dislocations after the ingot formation. Hartman et al. [18] tested the effects of high-temperature annealing on multicrystalline silicon wafers. By annealing at temperatures near the melting point, dislocation density reductions of >95% were achieved. A strong dependence on temperature was observed, as is shown in Figure 1.5.

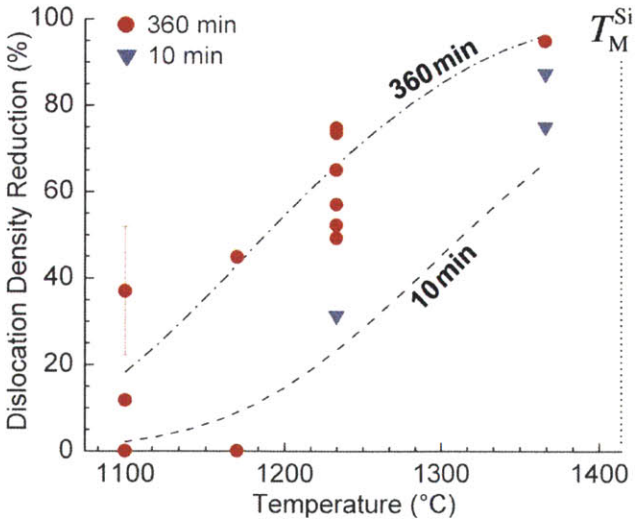


Figure 1.5: The effect of annealing temperature on dislocation density reduction. From [18].

The mechanism proposed for these significant dislocation density reductions was pairwise annihilation of dislocations of opposite sign. Further investigations into high temperature annealing of multicrystalline silicon wafers by Bertoni et al. [19] showed that the activation energy for this process was 2.1 ± 0.2 eV.

Expanding the parameter space, Bertoni et al. [20] found that stress is also an important factor in dislocation density reduction. Stress was applied to wafers at high temperatures via three-point bending, which created a variety of stress levels in both tension and compression throughout the wafer. It was found that areas with small stresses, estimated to be <5MPa, experienced large dislocation density reductions, while areas with high stresses, estimated to be >10MPa, experienced large increases in dislocation density. It was proposed that small amounts of stress may enhance dislocation motion and thus increase mutual annihilation.

1.5 Past uses of cyclic annealing for dislocation density reduction

Cyclic annealing has been used to reduce dislocations in several other materials. Brydges experimented with copper under reversed loading conditions [21]. In his experiments, the loading was applied mechanically at room temperature, and the dislocation density was measured after both compressive and tensile half-cycles. Dislocation multiplication and evidence of dislocation slip on the critical plane were observed after both compressive and tensile half-cycles.

Building upon Brydges's work, George East et al. used cyclic annealing at high temperatures to successfully reduce dislocation densities in copper [22]. He observed reductions of one or more order of magnitude with initial dislocation densities on the order of $10^6 cm^{-2}$ by cyclically annealing the samples for roughly five days. He also found cyclic annealing to be superior to static annealing for dislocation density reduction. Kitajima et al. [23] also experimented with cyclic annealing of copper. They were able to form highly perfect copper crystals using cyclic annealing. Additionally, they saw much better results for cyclic annealing than for isothermal, or static, annealing.

Chen et al. [24] used in-situ cyclic annealing to reduce dislocation densities in CdTe/Si through molecular beam epitaxy. They observed a reduction of two orders of magnitude that was proportional to the number of cycles. Halbwax et al. [25] found that cyclic annealing was effective for reducing the threading dislocation density in Ge films grown on (0 0 1) Si. Sakai et al. [26] applied thermal cycling to monocrystalline silicon crystals, and found that it effectively reduced the numbers of pure screw and 60° dislocations, but was not effective against Lomer-Cotrell dislocations. Note that the role of stress was not examined here.

1.6 Proposed use of cyclic annealing for dislocation density reduction in multicrystalline silicon

Past work indicates that applying stress to multicrystalline silicon at high temperatures can cause significant dislocation density reductions. Thermal cycling is a contact-free method of applying stress to a material, and can easily be conducted at high temperatures. A contact-free method carries the advantage of limiting the contamination. Contamination is especially a concern for high temperature processes. Additionally, the equipment for cyclic annealing is minimal; only a furnace is needed, and furnaces are already used in multicrystalline silicon ingot production facilities.

This work aims to determine if and how cyclic annealing at high temperatures can be used to reduce dislocation densities in blocks of multicrystalline silicon. First, the stress induced by cyclic annealing is examined using finite element analysis on Abaqus CAE. The stress distribution, effects of varying the annealing parameters, and effects of varying the sample geometry are examined (discussed in Chapter 3). Tests were then performed on small blocks of multicrystalline silicon. The annealing parameters used were based on the results of the FEA and the furnace capabilities. These blocks were examined for dislocation density reductions. The reductions observed in the lab were then compared to the stress levels predicted by the FEA modeling to determine what stress levels may lead to dislocation density reductions.

Chapter 2

Materials and Methods

2.1 Sample preparation

2.1.1 Sample selection and process information

Two bricks from directionally solidified multicrystalline silicon ingots were used as materials for the experiments. The bricks were donated by two industrial partners, henceforth denoted Brick #1 and Brick #2. For Brick #1, infrared imaging was used to avoid high-carbon areas. The use of materials from industry has the advantage that any processes developed using these materials can be applied industrially, since they will have already been demonstrated on industrial solar materials. Since materials from two different companies were used, it can be assumed that the results are transferrable between different multicrystalline silicon ingots, and are not due to any particular practice of one of the companies.

The sample sizes were chosen based on the capabilities of the tube furnace. The tube used for the first set of experiments had a 2.75in internal diameter, and the samples

rested on a D-tube which was approximately one third of the height of the tube. With these restrictions, a 3.5cm x 3.5cm square cross section was roughly the largest cross section that would not be too close to the edges of the tube. Avoiding contact between the sample and the tube was important in order to minimize contamination and avoid problems with thermal expansion. It also would have undesirably complicated the heat transfer to the sample. For the next set of experiments, a tube with a 2.5in internal diameter was used. The samples again sat on a D-tube that was approximately one third of the height of the tube. For these experiments, it was necessary to reduce the cross section to 3cm x 3cm.

2.1.2 Sample position within ingot

Grain structure, initial dislocation density, oxygen content, and metal impurities vary throughout mc-Si ingots, and collectively contribute to a variation in lifetime. The lifetime is highest in the center of the ingot, and low towards the top, bottom, and edges, for various reasons. On the bottom of the ingot, the low lifetimes are caused by high oxygen content. Oxygen content varies across the height of the ingot almost linearly, but is mainly deleterious in the bottom few centimeters [28]. Figure 2.1 shows the oxygen content as a function of height.

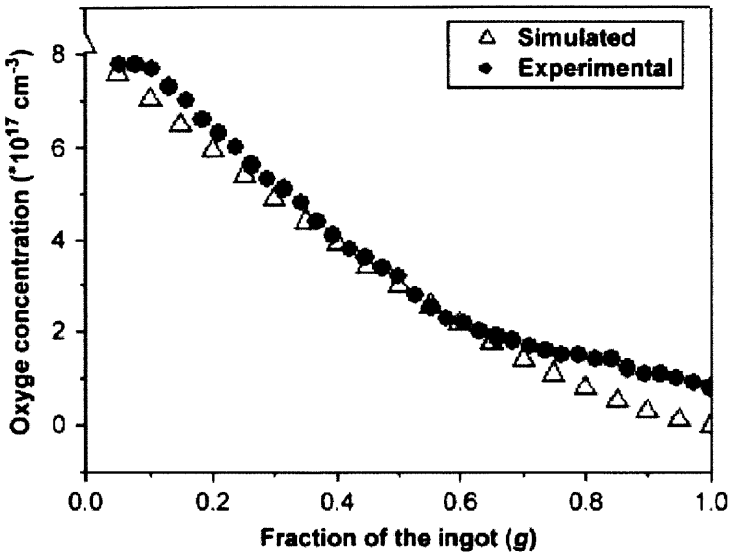


Figure 2.1: Variation of oxygen content over the height of the ingot (where g=1 corresponds to the top of the ingot). From [28].

On the sides and top of the ingot, low lifetimes are caused by metal impurities. The high concentrations of metal impurities towards the top of the ingot are shown in Figure 2.2.

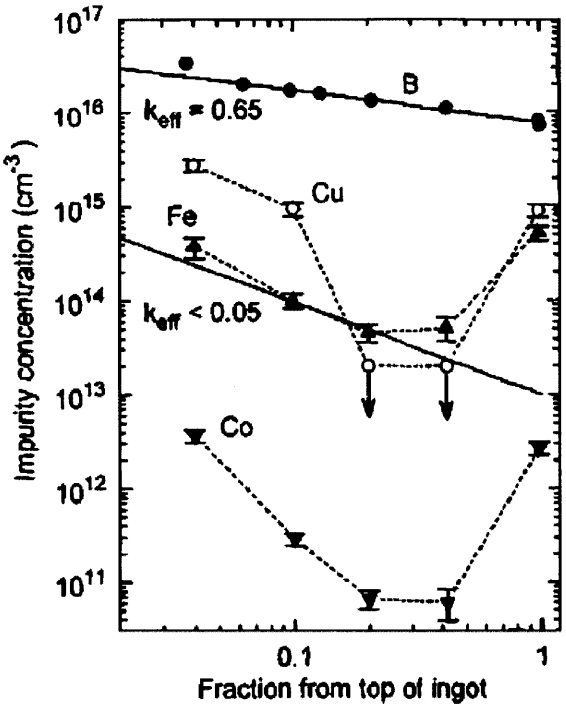


Figure 2.2: Transition metal profiles over the height of a mc-Si ingot. From [29].

To reduce the number of variables, areas of the ingot where lifetimes might be limited by oxygen content or transition metal impurities were avoided. To this end, samples were taken from the center of the ingot, avoiding the top and bottom few centimeters. In the samples from Brick #1, the carbon distribution in the ingot was also known, so high carbon areas were also avoided. The grain structure in the center region from which the samples were taken is fairly uniformly columnar, with no outstanding variations in average grain size from sample to sample. In directionally solidified multicrystalline ingots, the grain structure remains fairly uniform for horizontal cross sections, as long as the very top and bottom regions are avoided [30]. To keep the grain structure as constant as possible, samples were taken from vertical columns of the bricks,

as shown in Figures 2.3 and 2.5. The exception was with Brick #2, as shown in Figure 2.4, where samples were taken from the same height due to difficulties in sawing.

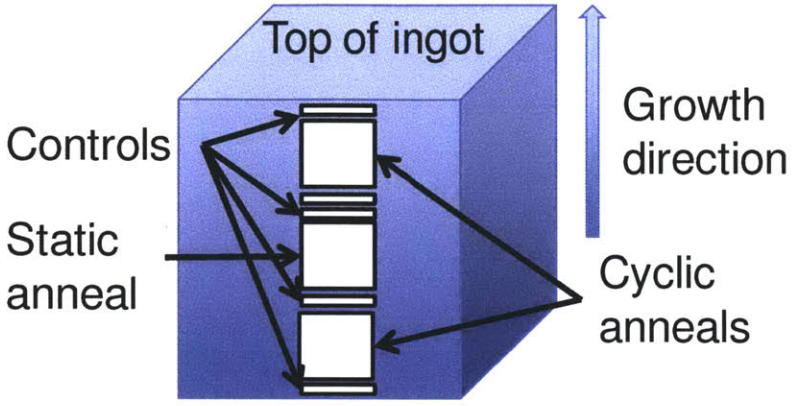


Figure 2.3: Sample arrangement in Brick #1 brick for first set of experiments

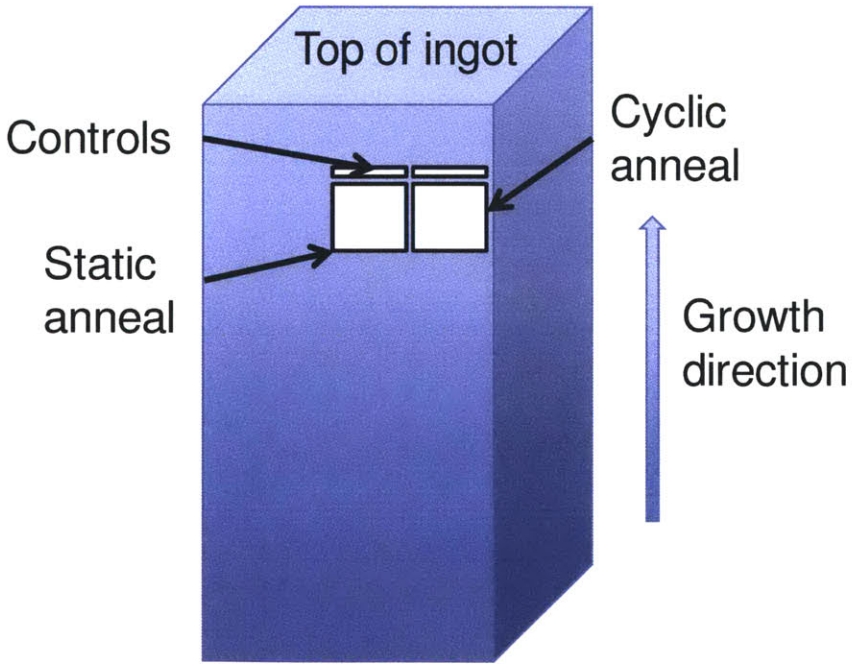


Figure 2.4: Sample arrangement in Brick #2 for first set of experiments

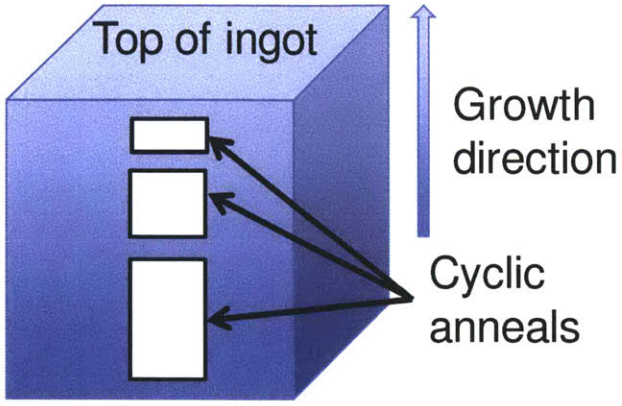


Figure 2.5: Sample arrangement in Brick #1 brick for second set of experiments

The one variable that was not controlled for in the samples was initial dislocation density. This variable was neglected in order to control for grain structure. In directionally solidified multicrystalline silicon ingots, dislocations nucleate at the bottom of the ingot and grow upwards with the growth direction of the ingot [30]. These dislocations multiply as they grow, and the dislocations formed by this multiplication also grow upwards and multiply. Thus, the dislocation density usually grows progressively from the bottom to the top of the ingot. In order to have samples from the same vertical position, these samples must necessarily have different initial dislocation densities. For the Brick #2 samples taken from the same horizontal position in the brick, the initial dislocation densities may have been similar, but were not controlled for.

2.1.3 Initial characterization

The initial characterization of the samples varied for the two sets of experiments. For the first set, the initial characterization was restricted to the control samples. The samples

were cut from the multicrystalline silicon bricks using a tile saw. The control samples were then polished (using 3μm diamond paste as the final polishing level), defect etched, and their dislocation densities were measured as described in section 2.3. For the second set of experiments, each sample was used as its own control. One face of the sample was polished and defect etched, and its dislocation density was measured, as described in section 2.3. The same face was polished again before annealing to get rid of the etch pits from the defect etch.

2.2 Annealing procedure

All Samples were annealed in a Lindberg tube furnace in a mullite tube with radiation shields on each end. The samples rested on an alumina D-tube. Two tubes were used for the experiments, as the first tube fractured due to extensive use. The information for the tubes and their corresponding accessories is given in Table 2.1.

Table 2.1: Tube information for both sets of experiments.

EXPERIMENTS	TUBE			D-TUBE	
	Material	ID (in)	OD (in)	Material	OD (in)
First set, using 3.5cm cubes	Mullite	2.75	3	Alumina	2.5
Second set, using varied geometries	Mullite	2.5	3	Alumina	2.25

Ambient air was used as the annealing atmosphere. An oxidizing atmosphere is advantageous for our purpose, since it oxidizes many metallic impurities before they can

penetrate the sample. Samples were etched prior to annealing to reduce contamination. Annealing conditions were varied to produce different stress distributions, which were ultimately limited by the capabilities of the furnace.

2.2.1 Pre-cleaning of samples

All samples were etched prior to annealing to reduce contamination of both the samples and the furnace environment. Samples were first subjected to a saw-damage etch to remove the surface layer. This removed any organic contaminants on the surface. The saw damage etch used was a variation of CP4, which consisted of 54 parts nitric acid, 20 parts hydrofluoric acid, and 20 parts acetic acid. This etch was performed for 1 minute. Samples were then rinsed and etched in a 10% hydrochloric acid solution for 3-5 minutes to remove metal contamination.

2.2.2 Pre-testing of furnace capabilities

These experiments were conducted using a Lindberg tube furnace, type 54453, with a pre-programmed time-temperature controller. Using the controller, the furnace was programmed with a series of time periods and set points to run a specific time-temperature profile. For each time period and set point, the furnace would heat or cool linearly from its current temperature to reach the set point in the prescribed time period. For example, the time-temperature profile in Figure 2.6, for a static anneal, was prescribed by the program in Table 2.2.

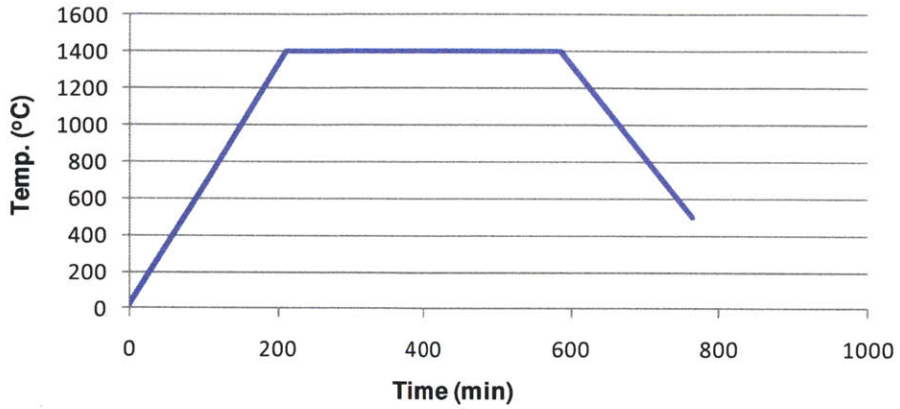


Figure 2.6: Static annealing furnace program.

Table 2.2: Furnace program for the static anneal shown in Figure 2.6.

Time Period (min)	Temperature Set Point (°C)
210	1400
15	1400
360	1400
180	500

The second step, a 15min hold at 1400°C, is not entirely necessary, but can serve as a buffer to assure that the maximum temperature has been reached before the anneal begins. After the furnace reaches 500°C, it is allowed to air cool. Figure 2.7 shows the furnace program for a cyclic anneal with a triangular wave.

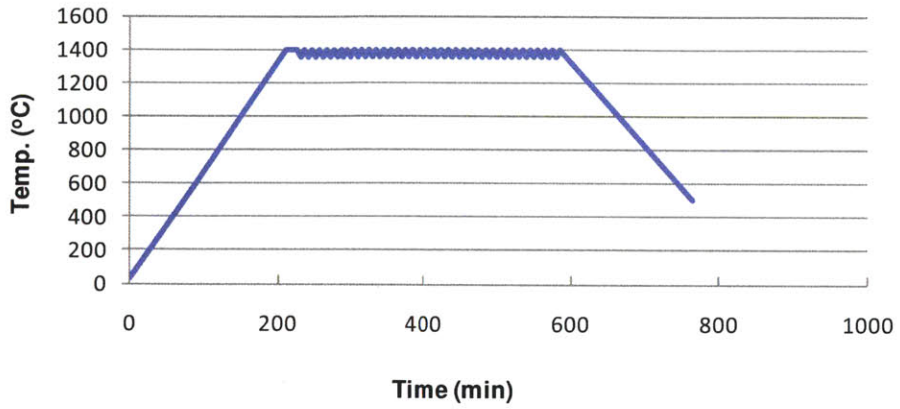


Figure 2.7: Furnace program for a cyclic anneal with a triangular wave.

The Lindberg furnace used for these experiments had several known limitations. Its maximum temperature was 1500°C, and its maximum ramping rates at high temperatures were 12°C/min ramping up and 20°C/min ramping down. However, due to the large thermal mass of the furnace and the thermal resistance of the tube, the temperature inside the tube did not match the temperature of the furnace program. The temperature inside the tube was measured with a type-R thermocouple and compared to the temperature of the furnace program and to the actual temperature inside the main body of the furnace, as measured by another thermocouple inside the furnace. For the tube used in the first set of experiments, the temperature difference between the inside of the tube and the rest of the furnace was roughly 100°C. For the second tube, which was twice as thick, the temperature difference was closer to 200°C.

With the first tube, the temperature inside the tube was able to roughly keep up with the furnace program (albeit 100°C lower), and the amplitude was close to the programmed 50°C. However, for the second tube, the lag was increased such that for a programmed amplitude of 100°C, the actual amplitude of the temperature inside the tube

was only about 50°C. Figure 2.8 shows the difference between the program temperature, the temperature measured by the thermocouple in the furnace, and the temperature measured by the thermocouple in the tube for a cyclic anneal using the thicker tube. Both the 200°C temperature difference and the decreased amplitude are observed.

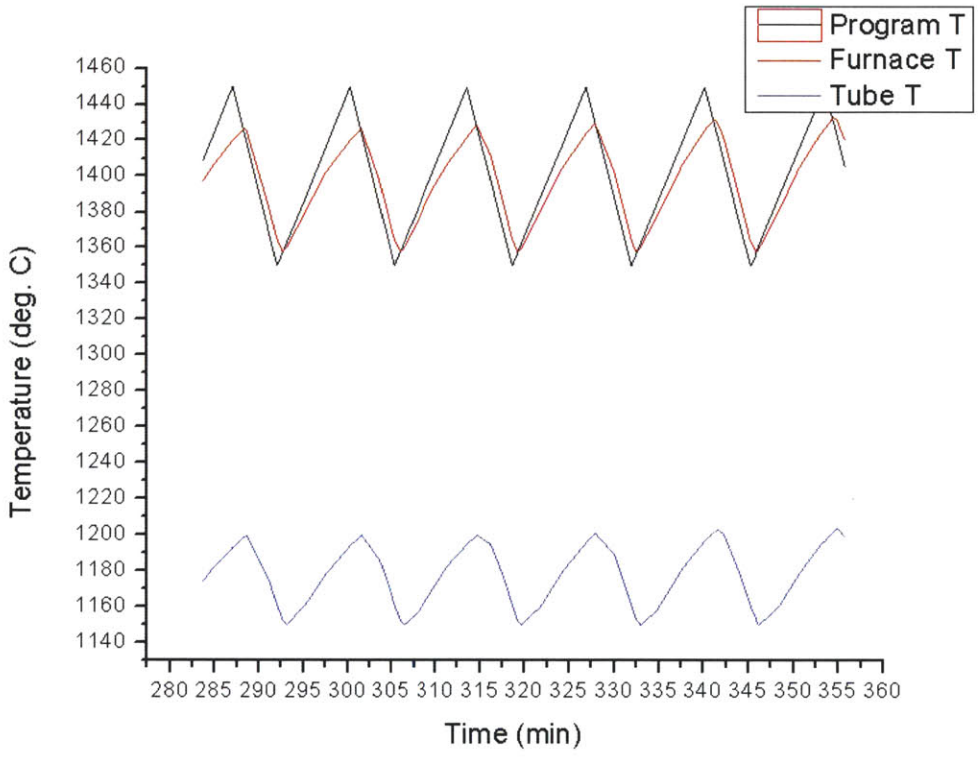


Figure 2.8: The temperature measured inside the tube compared to the temperature measured inside the furnace and the temperature of the furnace program for a cyclic anneal using the second, thicker tube.

Each furnace program used was tested before any samples were annealed. The limitations described above were found to be unavoidable. These limitations were also used to select the annealing parameters used in the lab experiments.

2.2.3 Variation of annealing parameters

Several cyclic annealing profiles were tested. They were selected based on the furnace limitations and the predictions of the FEA model. In the first set of experiments, the two annealing profiles varied the core stress of the sample, as discussed in Chapter 3. In the second set of experiments, the maximum ramp rates for heating and cooling were used to maximize the stress applied to the sample. A larger amplitude was used in the furnace program in order to keep the actual amplitude of the tube temperature roughly the same. Table 2.3 summarizes the annealing parameters for both sets of experiments. Cyclic annealing profiles A and B are defined here and will be referred to in future sections. The temperature range refers to the range during the thermal cycling; it excludes the initial heating and cooling to room temperature.

Table 2.3: Annealing parameters used in lab experiments.

Experiments	Anneal Type	Temperature Range (°C)	Heating Ramp Rate (°C/min)	Cooling Ramp Rate (°C/min)
First set of experiments	Static anneal	1300	0	0
	Cyclic annealing profile A	1250-1300	10	10
	Cyclic annealing profile B	1250-1300	10	5
Second set of experiments	Cyclic anneal	1150-1200	12	20

2.3 Initial experiment on wafers

For the initial experiment on wafers, a ribbon silicon wafer was used. Ribbon silicon has long grains stretching along the growth direction. The wafer was cut perpendicular to the growth direction so that adjacent areas of the same grains could be compared. Three strips were cut from the wafer, as shown in Figure 2.9. One strip was statically annealed, and another was cyclically annealed, with the third strip kept as a control. The control strip was made thin enough that areas on the two annealed samples could be directly compared.

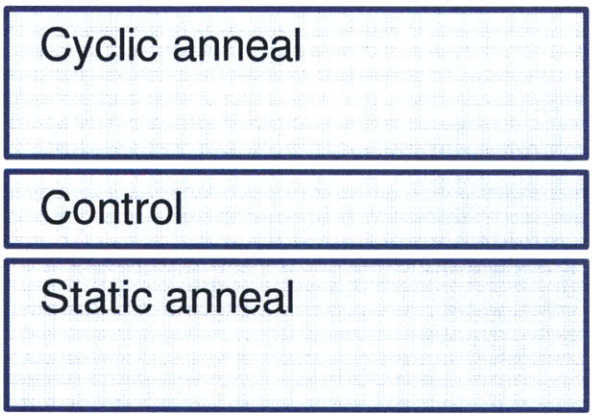


Figure 2.9: Sample arrangement for wafer experiment. A thin control strip separates the static and cyclically annealed samples.

Before annealing, a 100nm SiN_x diffusion barrier was deposited with PECVD. The samples were then annealed by the profiles shown in Figure 2.10. After annealing, the SiNx films were etched off with a 10% HF solution, then the samples were defect etched and examined for dislocation density as described in section 2.4.

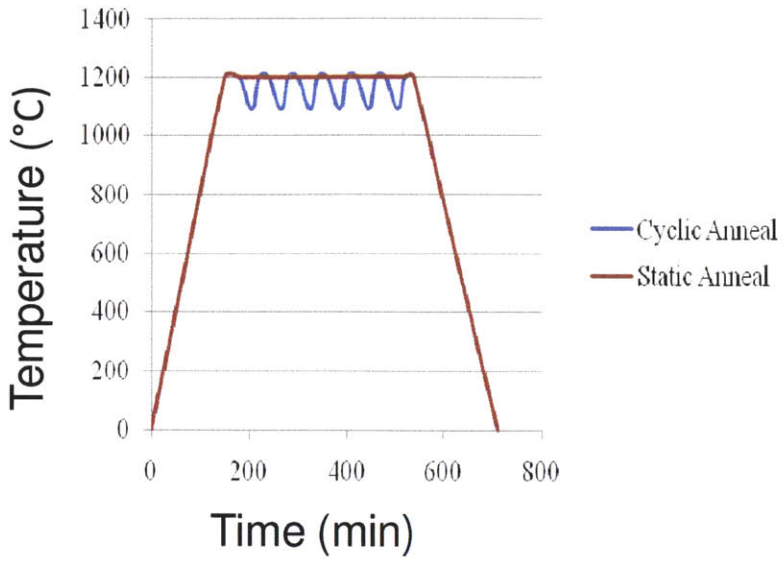


Figure 2.10: Wafer experiment annealing profiles. (This is the temperature inside the tube, not the temperature of the furnace program.)

2.4 Dislocation counting

2.4.1 Defect etching

After polishing, samples were etched using a Sopori etch, as described by Sopori [31]. The Sopori etch selectively etches the area around dislocations and grain boundaries. At each dislocation, a ~5μm etch pit was formed. When viewed in an optical microscope in bright-field imaging mode, these etch pits appear as black dots, while the rest of the surface is white or light gray. This enables the dislocations to be easily viewed and counted.

2.4.2 Etch pit counting program

The defect-etched samples were imaged in an optical microscope. Both individual micrographs of small sections of the samples and large image scans of the entire samples were taken. These images were analyzed using a program written on Matlab to count the etch pits and calculate the dislocation density.

The program starts by thresholding the image and making a matrix containing the area of every black spot on the image. The black spots may either be individual dislocations or clusters of dislocations. The matrix of areas is divided into two groups based on the approximate area of a large dislocation. All areas smaller than or equal to this large-dislocation-area are presumed to be single dislocations. A count and an average area are taken of the single dislocations. The other areas are presumed to be dislocation clusters. Their areas are summed, and the total cluster area is divided by the average area of the single dislocations to get an approximate count of the dislocations in clusters. The count of the single dislocations is added to the count of the dislocations in clusters to get a total count. To then get the dislocation density, the total count is simply divided by the area of the image. The logic of the program is organized into a flow chart in Figure 2.11. This method was partially inspired by the work of Rinio [30].

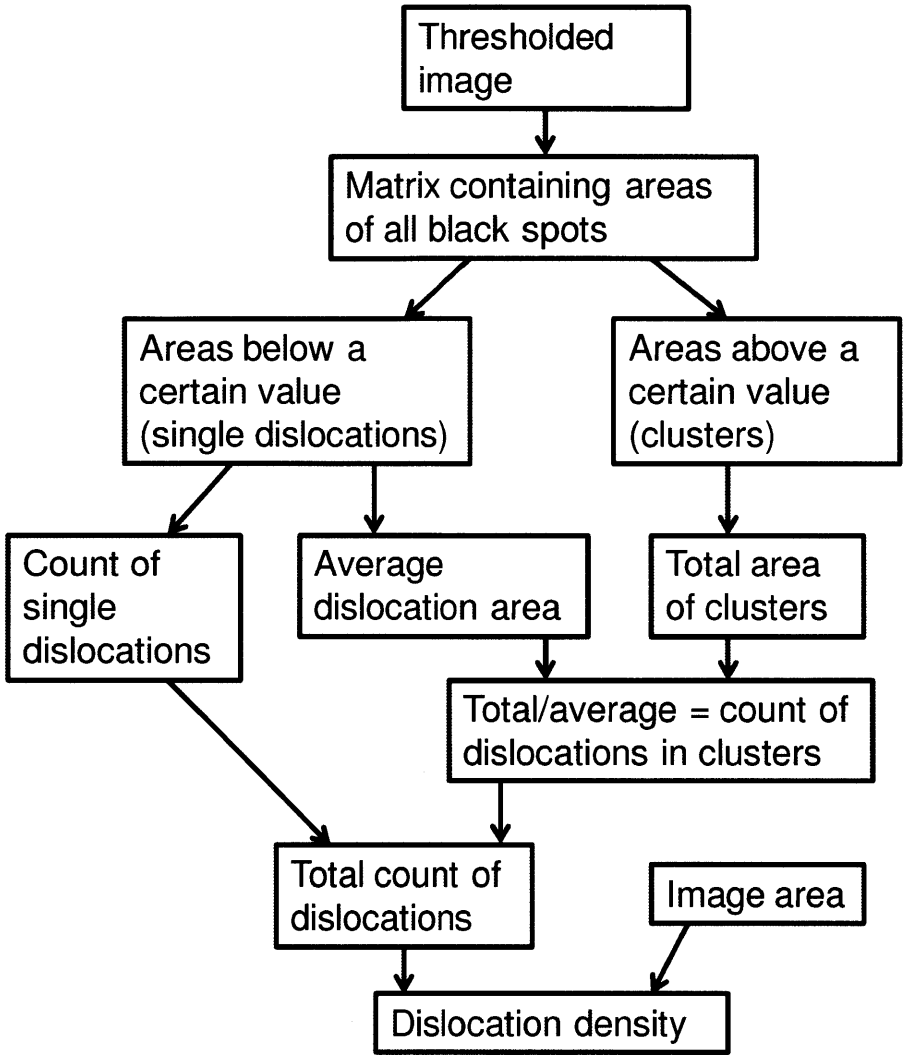
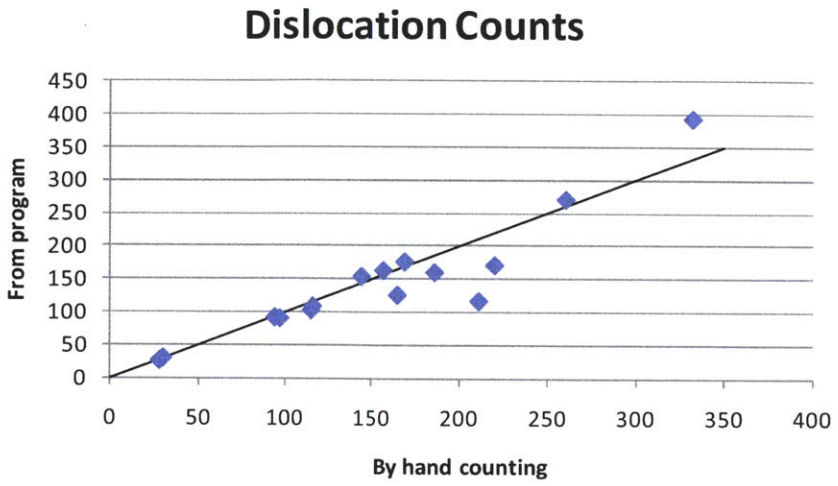


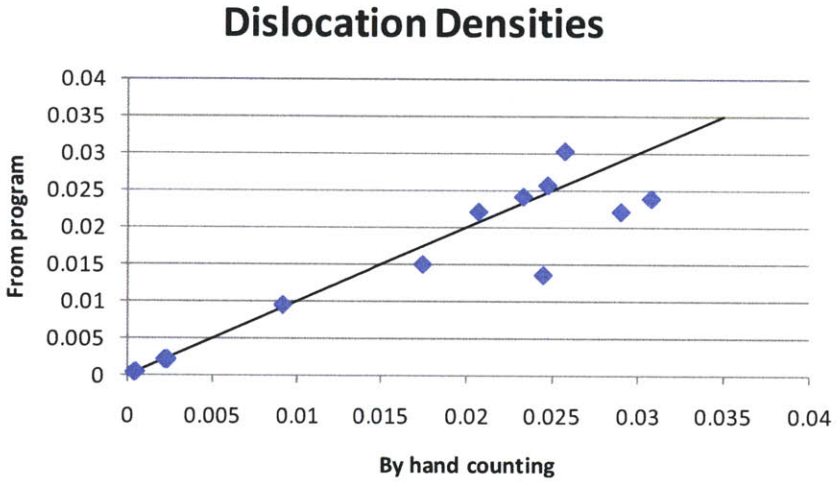
Figure 2.11: Logic of dislocation counting program.

The dislocation counting program was tested by comparing its calculated dislocation counts and dislocation densities to hand counts on a set of small test images. Hand counting is the most accurate method of determining the dislocation count and density, although it is far too time-consuming to be feasible for large images. The program counts are plotted against the hand counts in Figure 2.12, along with a line of slope=1. If the program were perfect, all dots would be on this line. As it is, most dots

are either on or very near the line. Figure 2.12 also shows a comparison of the dislocation densities calculated from these counts. For lower dislocation densities, the dots are on the line, but they diverge from the line at higher dislocation densities. This shows that the counting program is most accurate for lower dislocation densities. Overall, the program showed roughly a 20% error. This error is increased when samples are scratched, poorly thresholded, or when grain boundaries are present. The test images were cropped to avoid grain boundaries, but the large image scans did contain them, and thus had larger errors.



a)



b)

Figure 2.12: Comparison of program counts to hand counts

Chapter 3

Simulation of Stress from Cyclic Annealing

3.1 Explanation of the Abaqus FEA model

A finite element model of the cyclic annealing process was created using Abaqus CAE. The model included the silicon sample, mullite tube, and end caps of the tube furnace. A cross section of the model is shown in Figure 3.1. The temperature was controlled by setting the temperature of the tube. This temperature was set to follow the temperature of the tube, as measured during the furnace testing. The radiation between the tube, sample, and end caps was modeled. The silicon block was allowed to "float" in the tube. Though the D-tube support was not modeled, a frictional force, with a coefficient of 0.3, was applied to the bottom of the sample as a boundary condition. Gravity was also applied, and the bottom of the sample, as well as the tube and end caps, were restricted from moving in the z-direction. The Abaqus model was programmed with the temperature-

dependent material properties, including Young's modulus and coefficient of thermal expansion, of each material used (from Hull [32]).

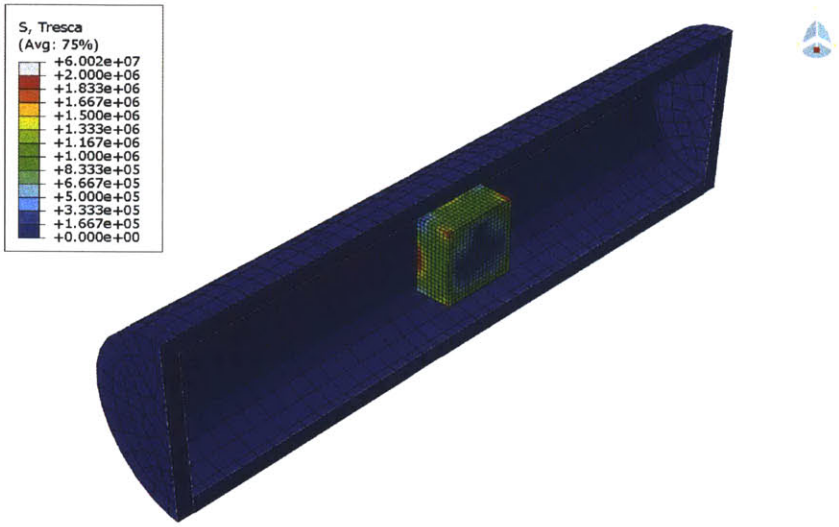


Figure 3.1: Abaqus CAE simulation of a 3.5cm cube subjected to cyclic annealing. A cross section of the model is shown with the stress distribution indicated by color. The stress shown is the Tresca stress, in units of Pa.

All stress measurements from the simulation results are reported as the Tresca stress. The Tresca stress is a standard measurement of the overall stress state at a specific point. It is similar to the von Mises stress, as it does not depend on the direction of the stress. The Tresca stress is calculated as [8]:

$$\sigma_{tresca} = \sigma_{\max} - \sigma_{\min} \tag{4.1}$$

3.2 Stress distribution of cyclically annealed Si blocks

When a block of silicon is subjected to cyclic annealing, first the outer surface heats and cools, then these temperature changes are transferred to the interior of the block. The interior temperature lags behind the outer temperature, creating thermal gradients which create differences in thermal expansion. These in turn create stress in the sample. The distribution of stress caused by thermal expansion depends on the geometry of the sample. For a block, it is concentrated at the outer edges, as is seen in Figure 3.2.

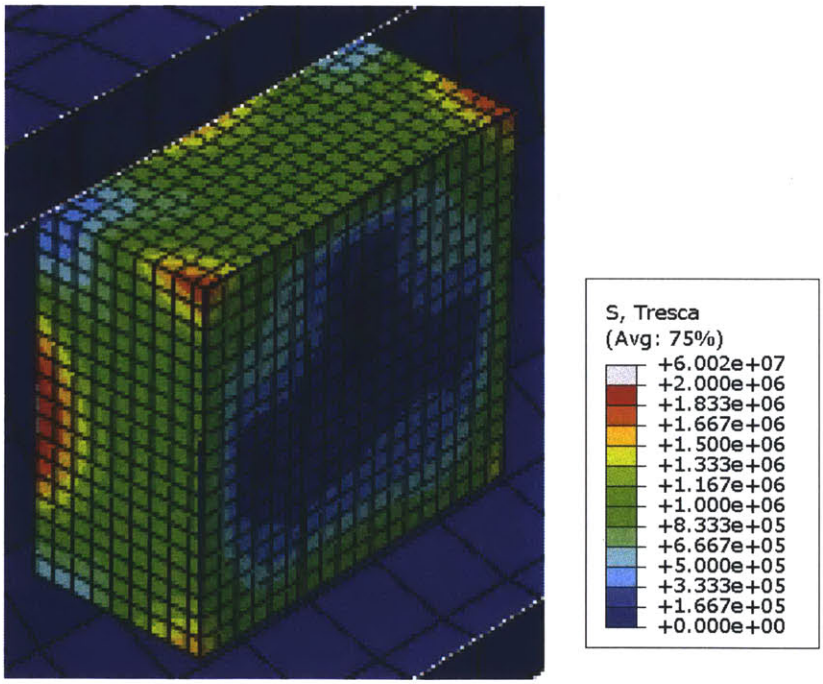


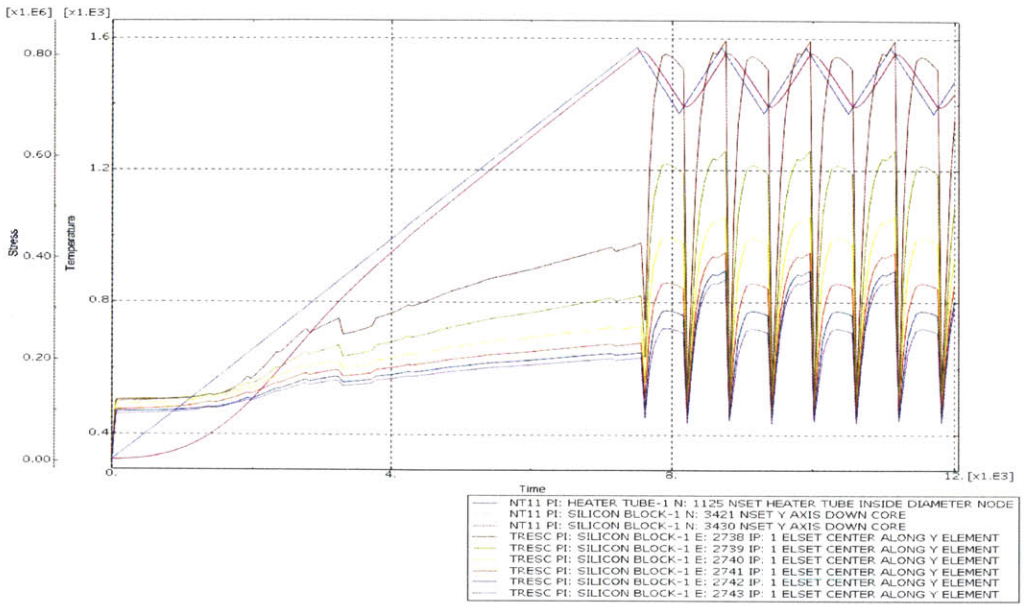
Figure 3.2: Detail of Figure 3.1, an Abaqus CAE simulation of a 3.5cm cube subjected to cyclic annealing. A close-up cross section of the silicon block is shown. The color indicates the Tresca stress in units of Pa.

Figure 3.2 shows the cross section of a cube, 3.5cm on a side, subjected to cyclic annealing. The stress is significantly higher at the outer surface than it is in the center. It is highest on the outer edges. On the center cross section, the middle is subjected to relatively low stress, while the edges of the cross section are at a higher stress, and the highest stress is at the corners. Please note that this is just an example of the stress distribution for one annealing profile. Both the magnitude of the stress and the magnitude of the stress variation throughout the sample will vary for different annealing conditions.

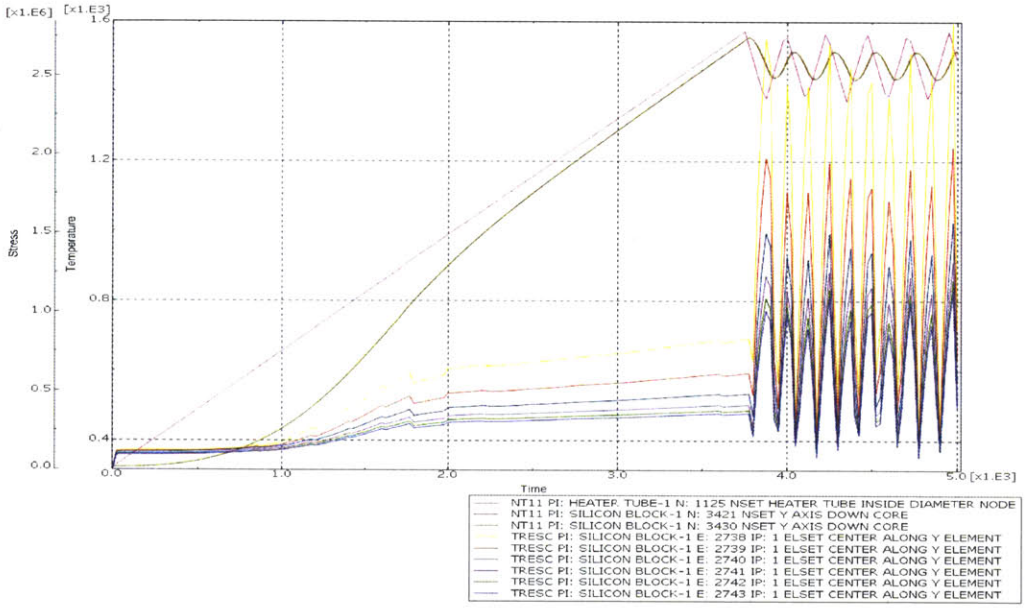
3.3 The effects of annealing parameters on stress

The amount of stress induced in a block by cyclic annealing can be varied by varying the annealing parameters. A true sinusoid is not possible in the furnace used, so a triangular wave was selected to be used in the experiments for practicality. Since this is what was tested in the lab, it was also used in the Abaqus CAE simulations. For a triangular wave, the parameters to vary are the slopes (the ramp rates of the furnace for heating and cooling) and the amplitude (the difference between the maximum and minimum temperatures during the cyclic phase of the anneal, excluding the initial heating and the slow cool to room temperature). Both of these parameters were examined.

The heating and cooling rates, or ramp rates, are an important parameter in cyclic annealing. For higher ramp rates, it is harder for the temperature in the center of the sample to keep up with the temperature on the outer edge of the sample, leading to larger temperature gradients and thus higher stresses. This is demonstrated in Figure 3.3, which shows the results of two Abaqus CAE simulations in which the ramp rates were varied.



a)



b)

Figure 3.3: Results of an Abaqus CAE simulation of a 3.5cm cube cyclically annealed with a 200°C amplitude. In (a), the ramp rates for both heating and cooling are 20°C/min and the maximum stress is ~0.8MPa. In (b), the ramp rates for both heating and cooling are 100°C/min and the maximum stress is ~2.5MPa.

Figure 3.3 shows the importance of ramp rate to the stress induced in the block. When the ramp rate is increased from 20°C/min to 100°C/min, the maximum stress increases from ~0.8MPa to ~2.5MPa. The amplitude (200°C) and sample characteristics (3.5cm cube) were kept constant; only the ramp rates were varied. Within each simulation, the ramp rate was the same for both heating and cooling.

It is interesting to compare these results to a static anneal, as shown in Figure 3.4. There is some stress induced while the sample is heated, and even some maintained while the sample is held at the maximum temperature. However, the stress induced at the maximum temperature as it is held constant is much less than the stress induced as it is heated (and also much less than the stress observed for cyclic anneals, as in Figure 3.3). It can be concluded that fluctuations in temperature are the main source of stress during cyclic annealing.

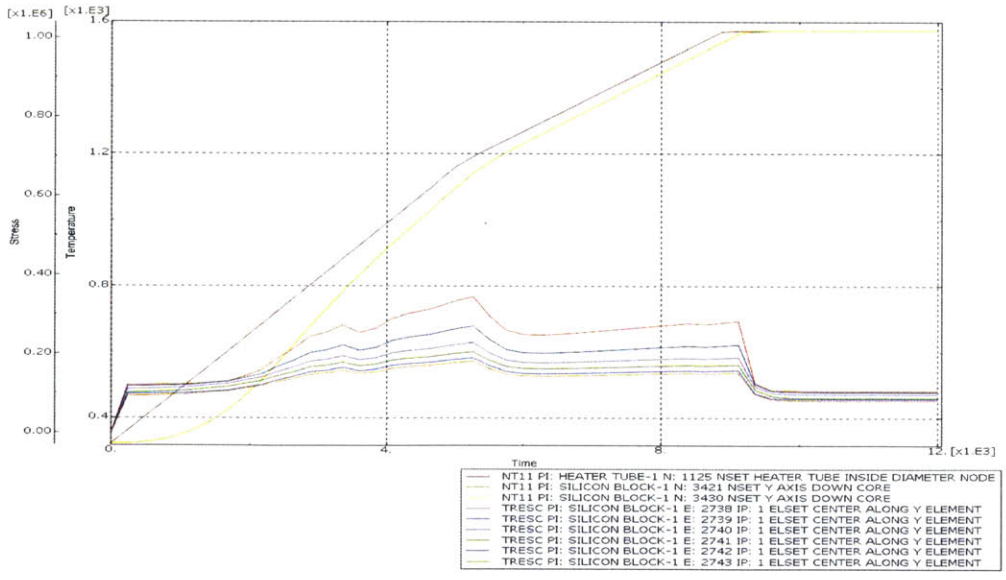
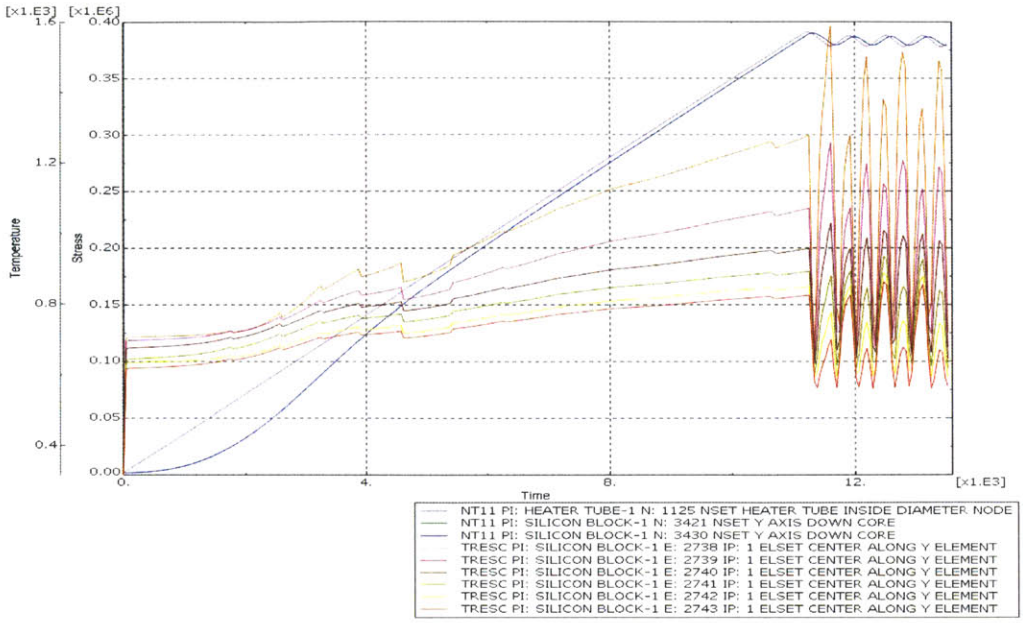
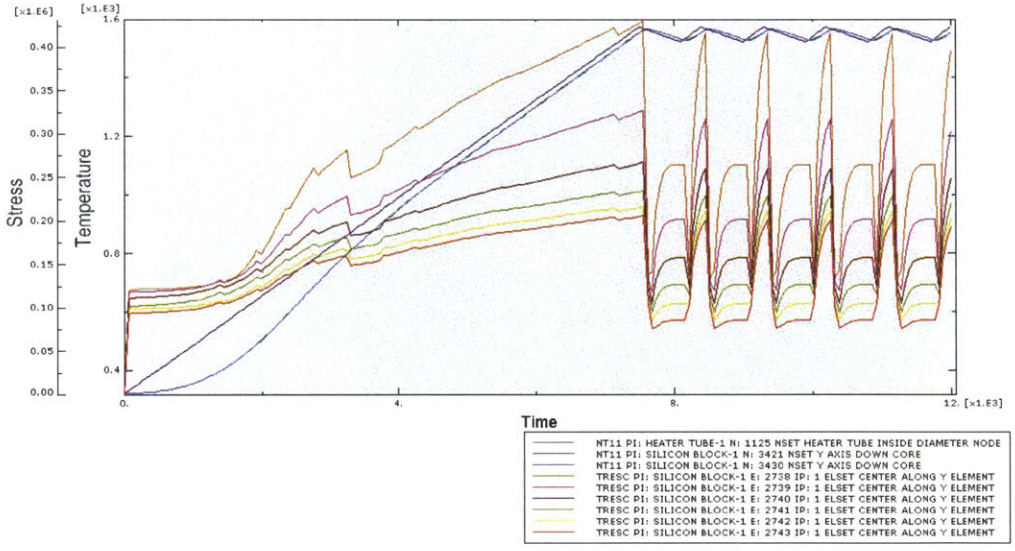


Figure 3.4: Simulation of a statically annealed 3.5cm cube during the heating and initial holding phases of the anneal.

Figure 3.5 shows the effect of varying only the cooling ramp rate. The simulations in this figure are for a 3.5cm cube cyclically annealed with a 50°C amplitude, a 10°C/min ramp rate for heating, and either a 10°C/min or 5°C/min cooling rate. These are the same parameters that were used in the first set of experiments. In both simulations, the maximum stress on the outside of the sample is ~0.4MPa. The maximum stress on the inside of the sample, however, varies slightly. For the 10°C/min cooling ramp rate, the maximum stress in the center of the sample is ~0.1MPa. For the 5°C/min ramp rate, it is ~ 0.15MPa. This appears to indicate that while the overall maximum stress is not significantly affected, the slower cooling rate causes the stress to be more evenly distributed within the block. However, the difference in stress levels between the outer edge and the center of the block is still large.



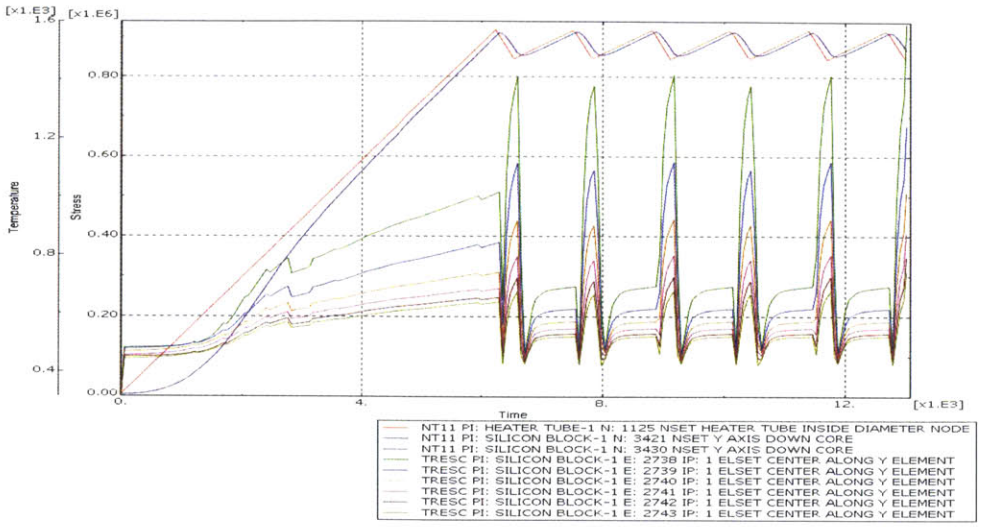
a)



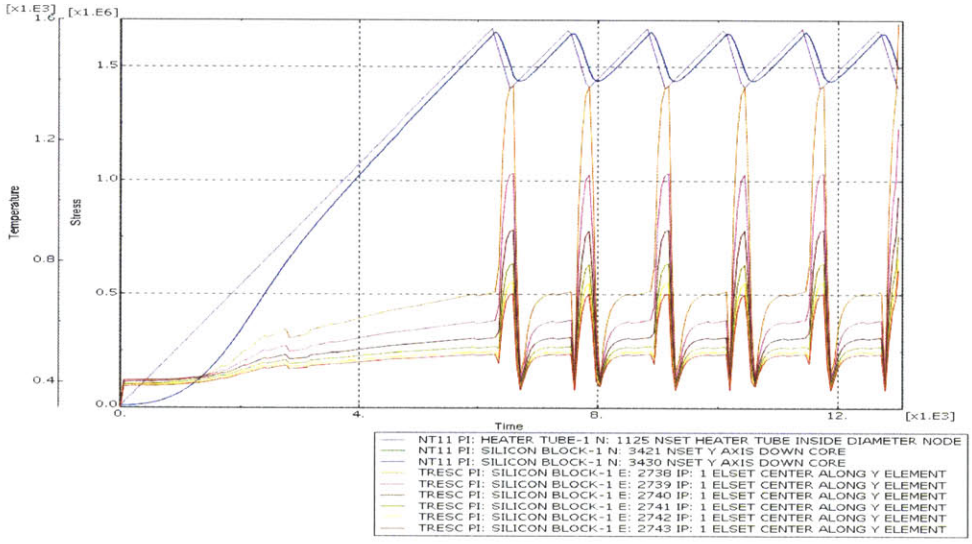
b)

Figure 3.5: Abaqus CAE results for a simulation of a 3.5cm cube cyclically annealed with an amplitude of 50˚C and a heating ramp rate of 10˚C/min. In (a), the cooling ramp rate is 10˚C/min. In (b), the cooling ramp rate is 5˚C/min.

Another annealing parameter that may affect the stress induced in a block during cyclic annealing is the amplitude. This refers to the difference between the maximum and minimum temperature during the cycling phase, excluding the initial heating and slow cooling to room temperature. The effects of different amplitudes on a cyclically annealed 3.5cm cube were modeled in Abaqus, and the results are presented in Figure 3.6.



a)



b)

Figure 3.6: Abaqus CAE results for a simulation of a 3.5cm cube cyclically annealed with ramps of 12˚C/min up and 20˚C/min down. In (a), the amplitude is 100˚C and the maximum stress is ~0.8MPa. In (b), the amplitude is 200˚C and the maximum stress is ~1.4MPa.

Comparing these two figures shows that the amplitude does indeed affect the stress on the sample. Doubling the amplitude nearly doubled the maximum stress on the sample. Though increasing the amplitude is an effective way to increase the stress, it may not be an effective way to increase dislocation density reduction. Besides stress, maintaining high temperatures throughout the anneal appears to be important to achieving a dislocation density reduction. Additionally, it is a difficult variable to decouple in an experiment. Increasing the amplitude with a set maximum temperature would mean decreasing the average temperature during the annealing process, which could introduce another important process variable and make any results difficult to interpret. If the average temperature were kept constant, the maximum temperature would have to be varied, which would also introduce another variable. For these reasons, the effects of varying the amplitude were not tested in the lab.

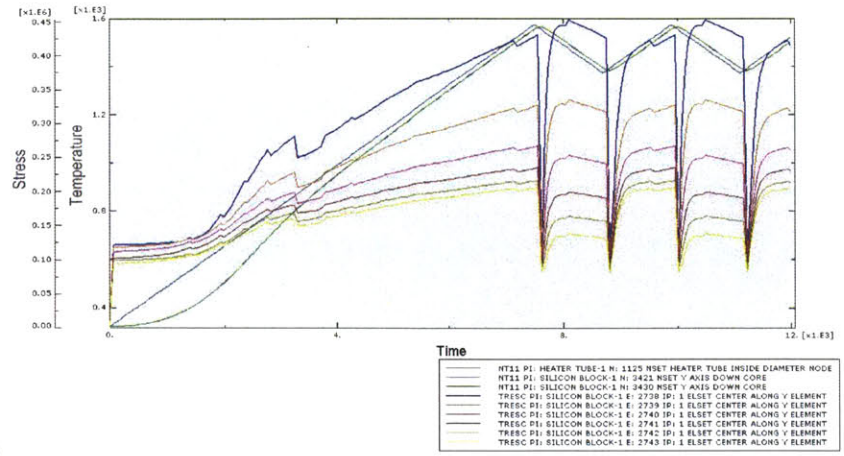
Table 3.1 shows the stress induced for various simulations, varying both amplitudes and ramp rates. The same trends are shown. Wherever ramp rates are held constant and the amplitude is increased, the stress increases. Wherever the amplitude is held constant and ramp rates are increased, the stress also increases. Note that the maximum stress refers to the maximum stress reached at the outer edge of the sample. The ramp rates of 12°C/min up and 20°C/min down were selected for modeling because they are the maximum heating and cooling rates that can be used on the tube furnace used for these experiments.

Table 3.1: The maximum tresca stress calculated by Abaqus CAE simulations for the different annealing parameters listed. The lines highlighted in pink are for annealing profiles that could not be tested in the tube furnace used in the lab.

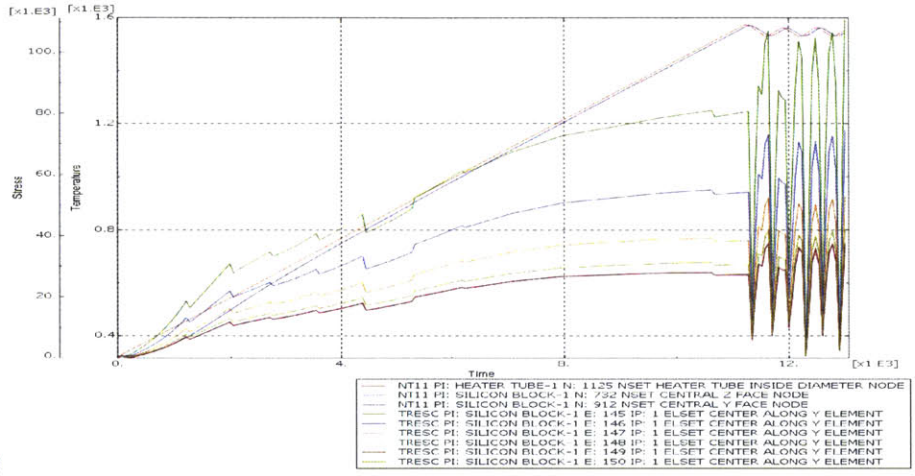
Ramp Up (°C/min)	Ramp Down (°C/min)	Amplitude (°C)	Maximum Tresca Stress (MPa)
0	0	0	0.1
10	10	50	0.37
10	5	50	0.4
10	10	200	0.45
20	20	200	0.8
100	100	200	2.8
12	20	100	0.8
12	20	200	1.4

3.4 The effects of sample geometry on stress

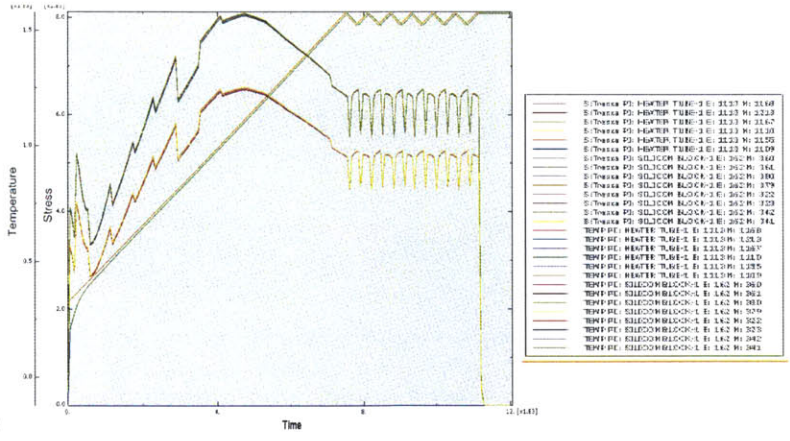
The geometry of a sample subjected to cyclic annealing also has a significant effect on the stress induced in the sample. Smaller and thinner samples reach thermal equilibrium faster, while larger and thicker samples have a greater lag between the core temperature and the outer temperature of the sample. Figure 3.7 shows the simulation results for three very different geometries. All three cases have a 3.5cm square cross section, but the thickness varies from a 400μm thick wafer to a 0.5cm thick slab to a 3.5cm cube. The annealing parameters are held constant, with 10°C/min ramps and a 50°C amplitude.



a)



b)



c)

Figure 3.7: Abaqus CAE results for a simulation of (a) a 3.5cm cube; (b) a 0.5cm thick slab; and (c) a 400μm thick wafer.

Figure 3.7 shows the significance of sample geometry to the stress levels induced in the sample. For the 3.5cm cube in (a), the maximum stress is ~0.37MPa. For the 0.5cm slab, it is ~0.11MPa. This is a significant difference, but still on the same order of magnitude. For the 400μm thick wafer, the maximum stress is 0.005MPa. As the thickness changes by two orders of magnitude, so does the stress level. The results of further simulations, in which the annealing profiles are also varied, are presented in Table 3.2. All results clearly show that larger, thicker samples experience greater stresses.

Table 3.2: The maximum tresca stress calculated by Abaqus CAE simulations for various sample sizes and annealing parameters.

Ramp Up (°C/min)	Ramp Down (°C/min)	Amplitude (°C)	Max. Tresca Stress in 3.5cm Cube (MPa)	Max. Tresca Stress in 0.5cm Slab (MPa)	Max. Tresca Stress in 400μm Wafer (MPa)
10	10	50	0.37	0.11	0.005
12	20	100	0.8	0.25	-
12	20	200	1.4	0.45	-

Chapter 4: Dislocation Density Reduction from Cyclic Annealing

4.1 Initial results on wafers

Despite the very low stresses created in wafers by cyclic annealing (see Figure 3.7 and Table 4.2), a significant dislocation density reduction is observed in the cyclically annealed wafer, as shown in Figure 4.1. The cyclically annealed wafer also had lower dislocation densities than the statically annealed wafer, indicating that it experienced a greater reduction than the statically annealed wafer. These positive initial results inspired the more detailed study on blocks of multicrystalline silicon.

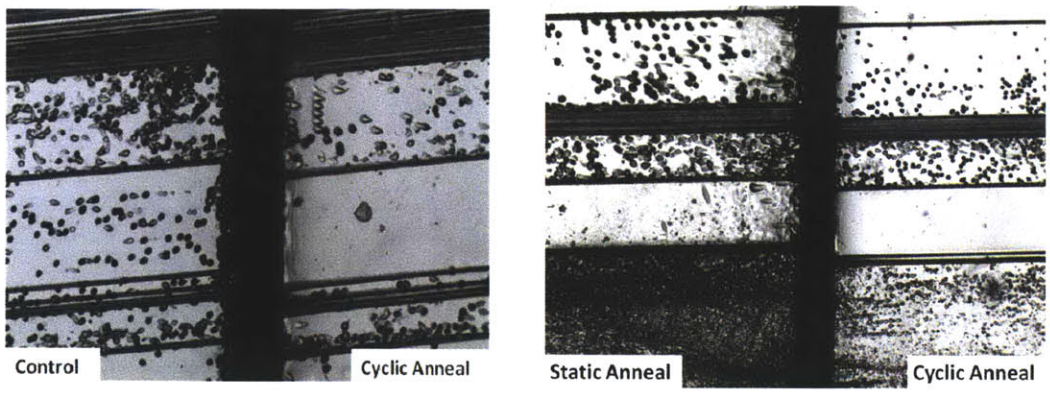


Figure 4.1: Micrographs of defect-etched wafers. Corresponding grains are lined up for comparison. Etch pits are approximately 5μm in diameter.

4.2 Dislocation density reduction for varied annealing profiles

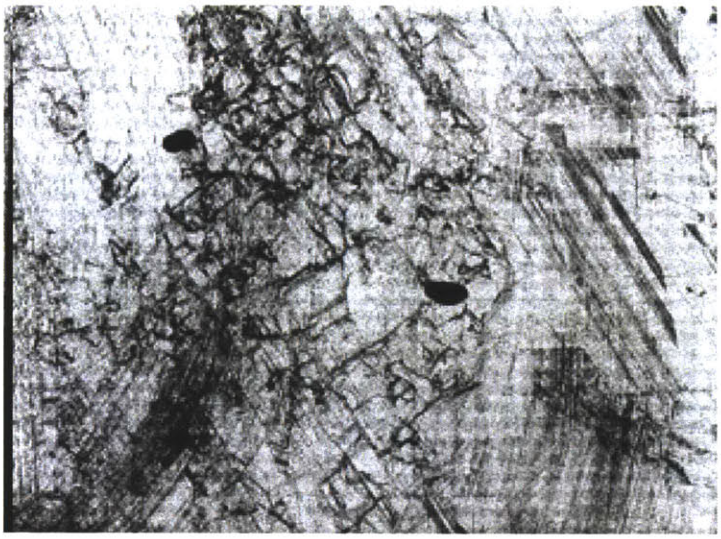
4.2.1 Dislocation density reduction in the core of the sample

Three different annealing profiles were used in the first set of experiments, while other variables including sample geometry were held constant. In the second set of experiments, a different annealing profile was used; however, because other variables were not kept constant, these results may not be compared to the first set of experiments, and only the first set of experiments will be discussed here. Samples in these experiments were drawn from both Brick #1 and Brick #2. In the Brick #1 samples, all three different profiles were tested. In the Brick #2 samples, two of the three profiles were tested.

The parameters for the annealing profiles used are given in Table 2.3, and a sample profile is shown in Figure 2.7. (Recall that cyclic annealing profile A refers to a

triangular wave with amplitude 50°C, ranging from 1250°C to 1300°C, with ramp rates of 10°C/min for both heating and cooling. Cyclic annealing profile B refers to a triangular wave with amplitude 50°C, ranging from 1250°C to 1300°C, with ramp rates of 10°C/min for heating and 5°C/min for cooling.) Large image scans taken on an optical microscope of the defect-etched samples are shown in Figures 4.2 through 4.6.

a)



b)

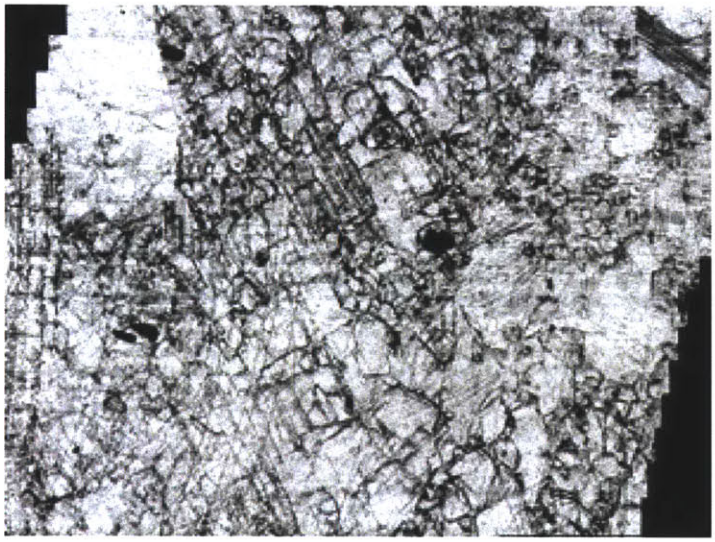
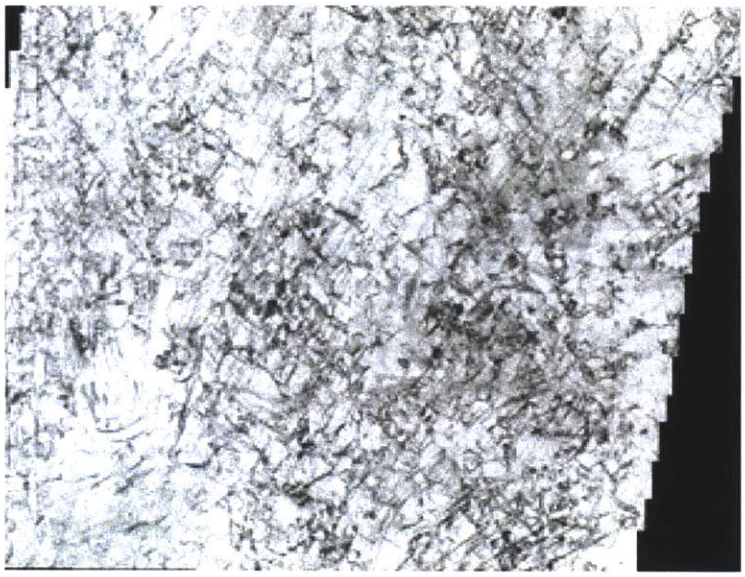


Figure 4.2: Optical microscope scans of defect etched control (a) and annealed (b) samples from Brick #1 for static annealing. Each image is approximately 17 x 25mm.

a)



b)

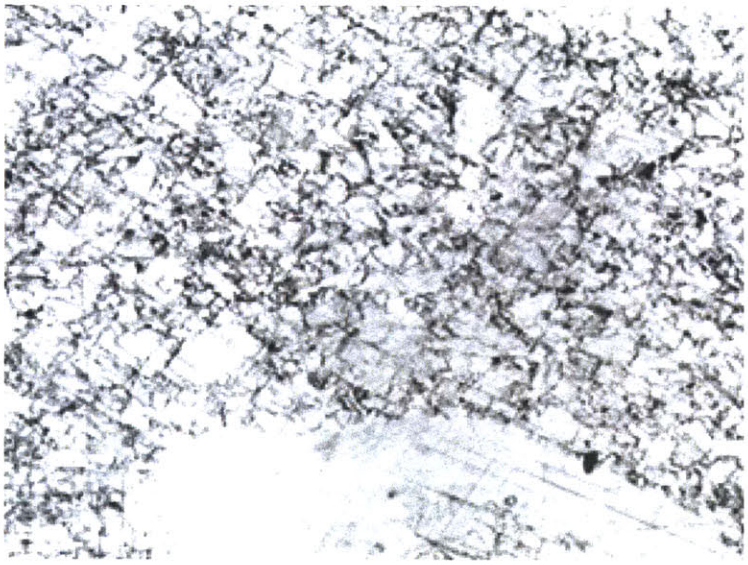
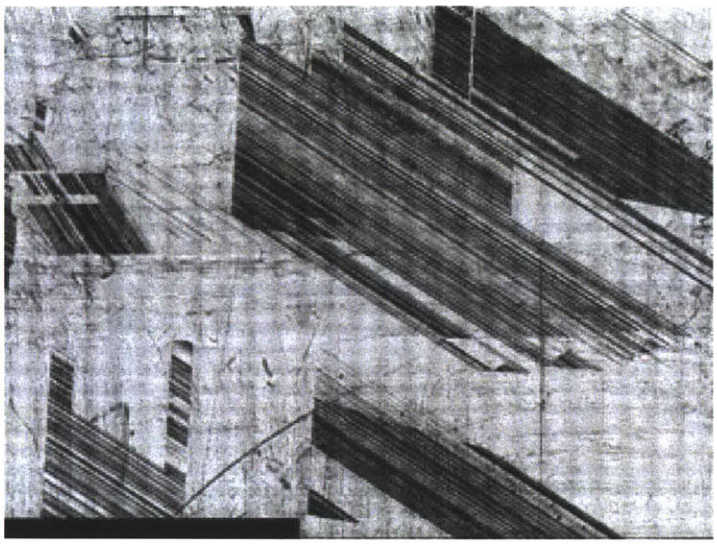


Figure 4.3: Optical microscope scans of defect etched control (a) and annealed (b) samples from Brick #1 for cyclic annealing profile A. Each image is approximately 17 x 25mm.

a)



b)

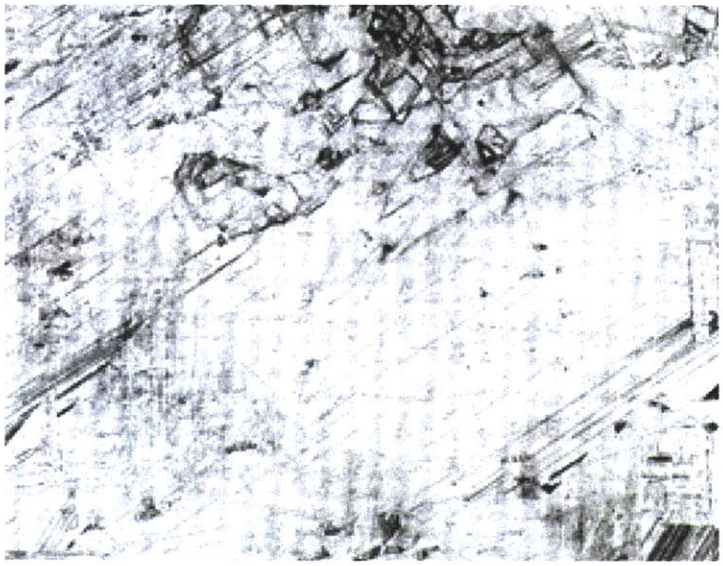
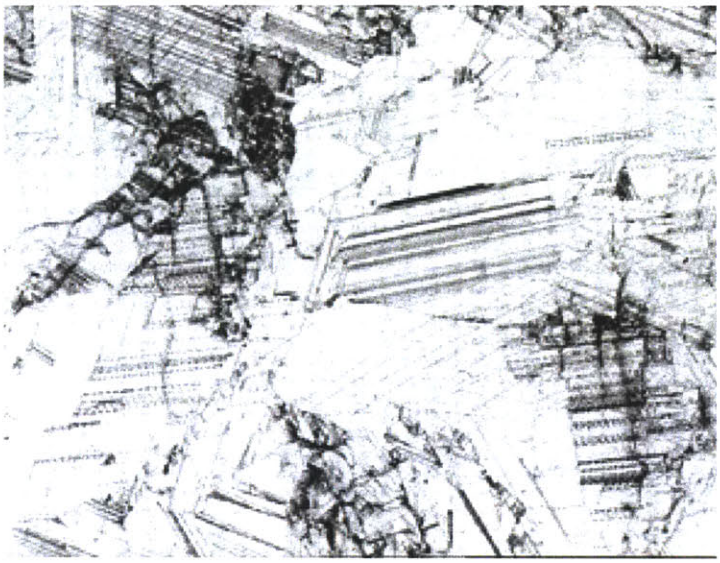


Figure 4.4: Optical microscope scans of defect etched control (a) and annealed (b) samples from Brick #1 for cyclic annealing profile B. Each image is approximately 17 x 25mm.

a)



b)

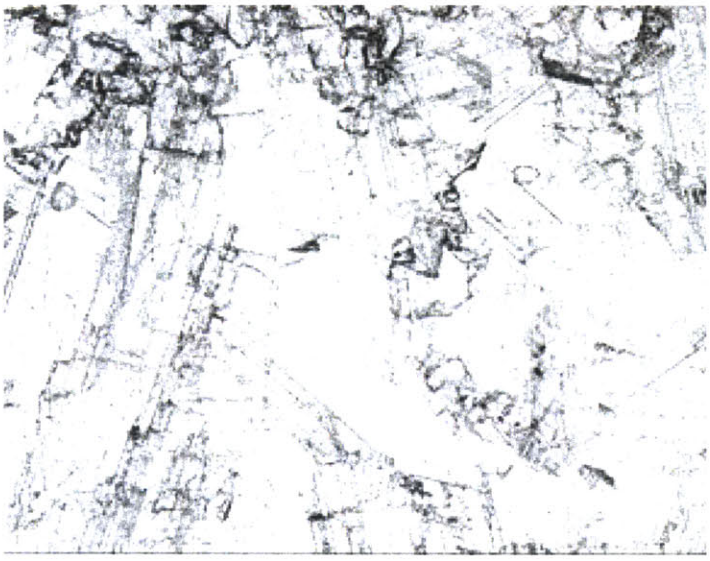
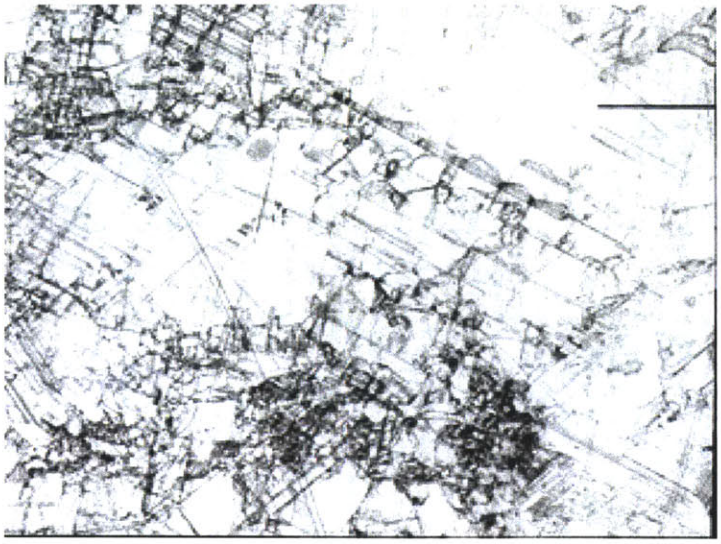


Figure 4.5: Optical microscope scans of defect etched control (a) and annealed (b) samples from Brick #2 for static annealing. Each image is approximately 17 x 25mm.

a)



b)

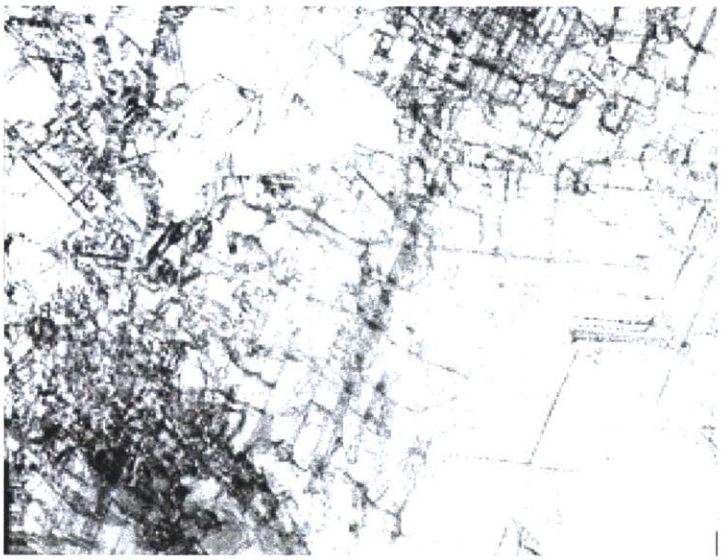


Figure 4.6: Optical microscope scans of defect etched control (a) and annealed (b) samples from Brick #2 for cyclic annealing profile B. Each image is approximately 17 x 25mm.

Little difference is observed in any of the above figures. The overall dislocation densities of the cross sections, as calculated by the Matlab code, are given in Table 4.1. While some reductions are observed, they are small and inconsistent. This may be because the stress induced at the core of the sample is too small to have an effect. This possibility is discussed further in the section.

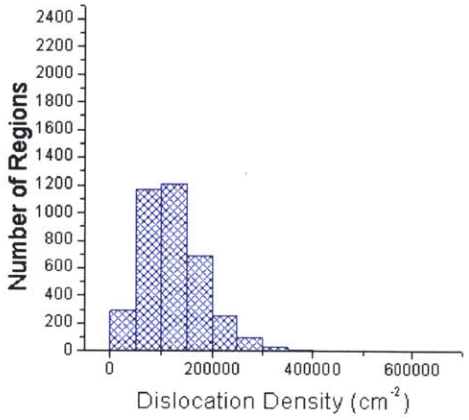
Table 4.1: Dislocation densities and reductions for Brick #1 and Brick #2 samples subjected to static and cyclic annealing. (Negative reductions indicate increases in dislocation density.)

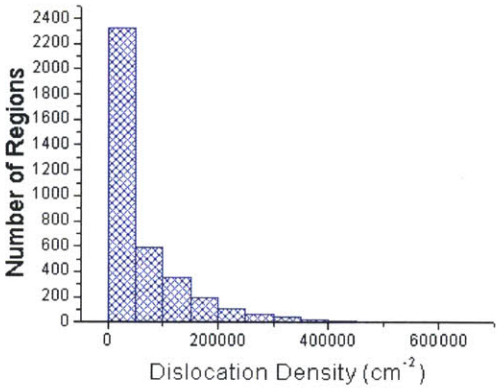
Sample Source	Annealing Profile	Dislocation Density of Control (cm^{-2})	Dislocation Density of Annealed Sample (cm^{-2})	Reduction
Brick #1	Static	2.4E+05	1.3E+05	44%
	Cyclic A	1.9E+05	1.4E+05	30%
	Cyclic B	1.3E+05	3.8E+05	-201%
Brick #2	Static	1.8E+05	2.5E+05	-39%
	Cyclic B	2.2E+05	2.9E+05	-34%

To see how the dislocation density was distributed throughout the sample (i.e., if the dislocations were mostly clustered in one section, or if they were spread more evenly throughout the sample), the Matlab code was modified to divide the large images into many small sections, calculate the dislocation density of each section, and create a histogram of the dislocation densities of the sections. These histograms are shown in Figure 4.7.

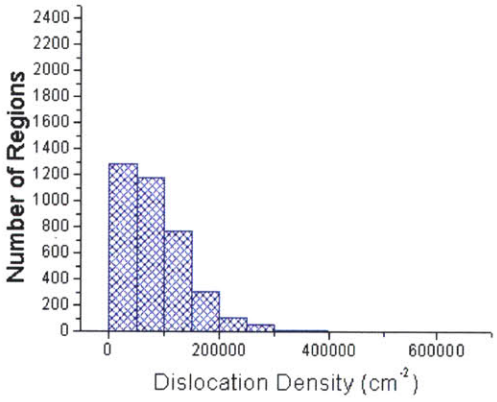
Control

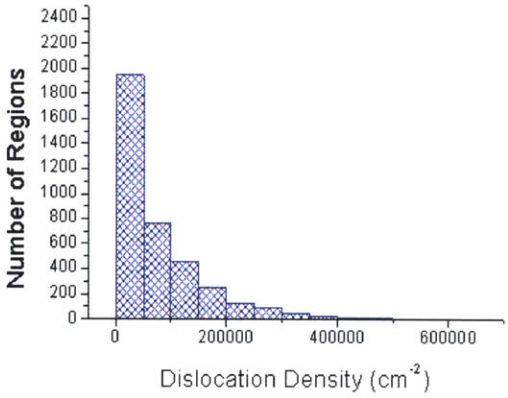
Anneal



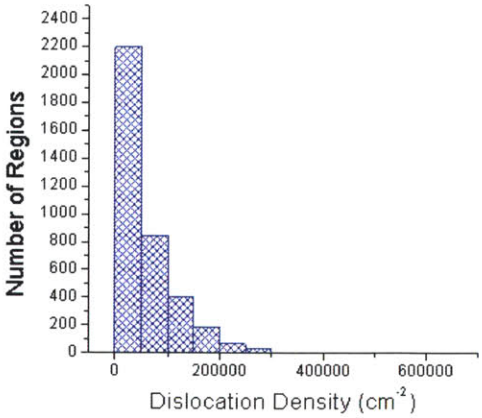


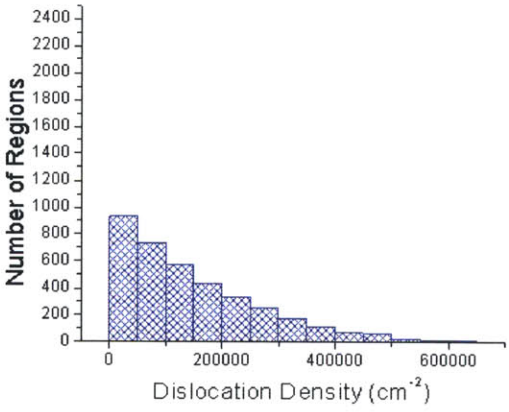
a)





b)





c)

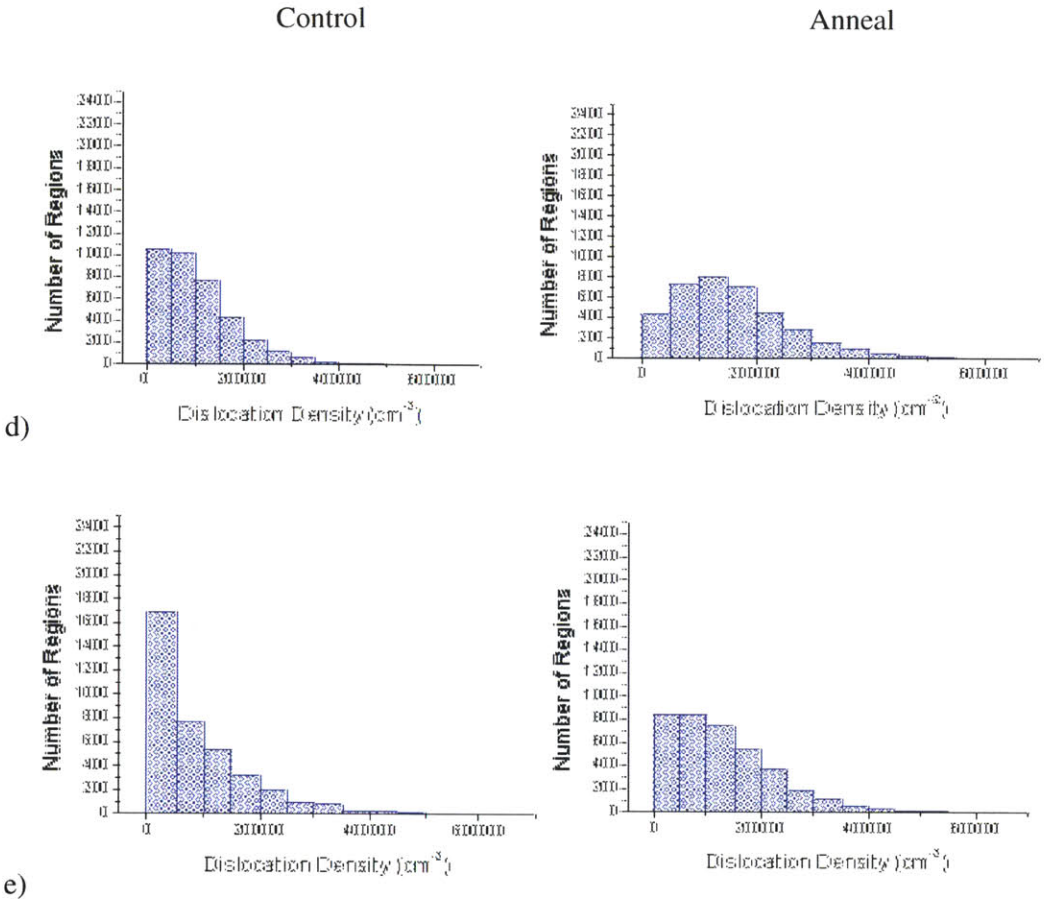


Figure 4.7: Histograms for the control and annealed samples: a) static anneal, Brick #1; b) cyclic annealing profile A, Brick #1; c) cyclic annealing profile B, Brick #1; d) static anneal, Brick #2; e) cyclic annealing profile B; Brick #2.

Although the results are not consistent, the histograms for the Brick #1 static anneal and cyclic anneal profile A do show a shift. In both of these cases, the histogram for the annealed sample is heavier on the left than the histogram for the control sample, meaning that a larger portion of the sample has a low dislocation density. This would be a promising result; however, since it is not consistent for all samples, no conclusions can be made.

4.2.2 Dislocation density reduction on the outer surface

Recall the stress distribution shown in Figure 3.2. The stress at the outer surface of the sample was considerably greater than the stress at the inner core. Figures 4.8 and 4.9 show the Abaqus simulations for a 3.5cm cube subjected to cyclic annealing profiles A and B, respectively. The stresses at the outer surface and the core are indicated. The stresses differ by roughly a factor of four for cyclic annealing profile A, and by roughly a factor of 2.7 for cyclic annealing profile B.

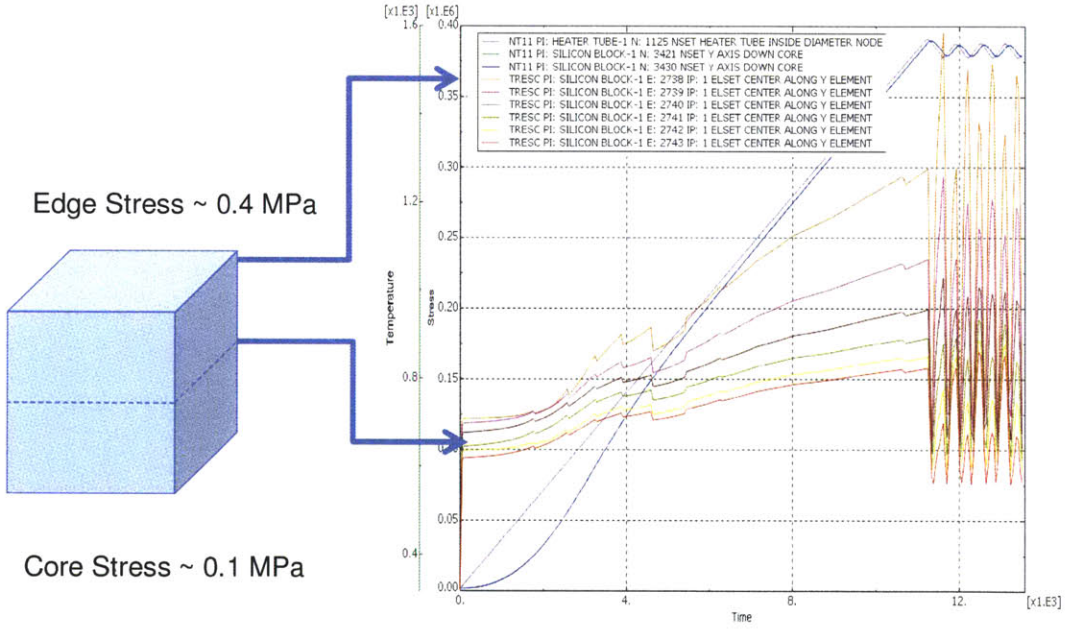


Figure 4.8: Abaqus CAE results for the stress induced in a 3.5cm cube for cyclic annealing profile A. The maximum stress is significantly higher on the outer edge than in the core of the sample.

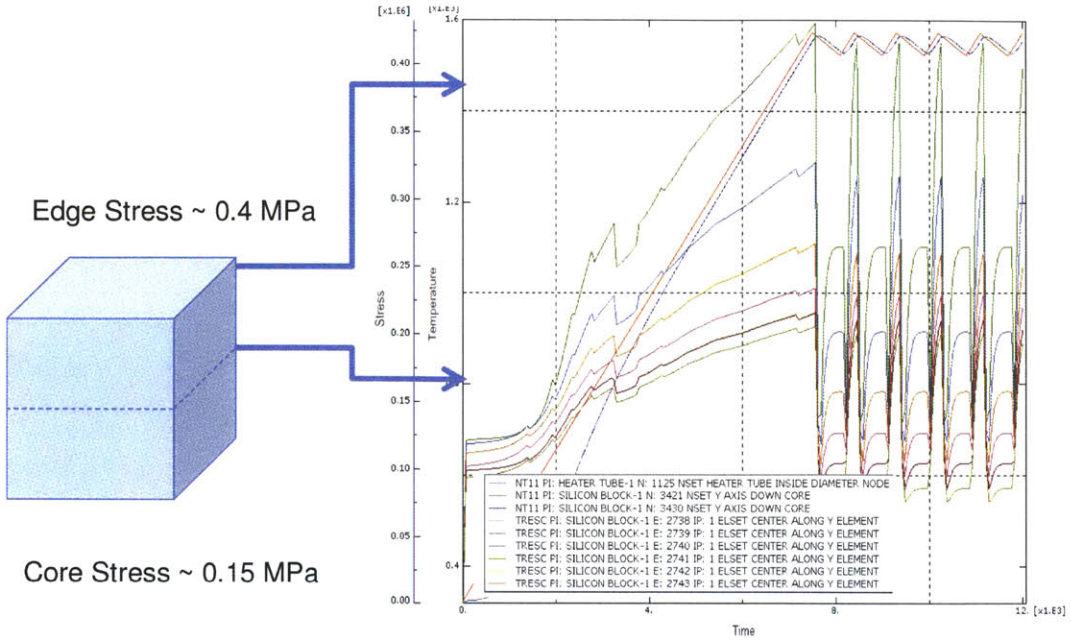
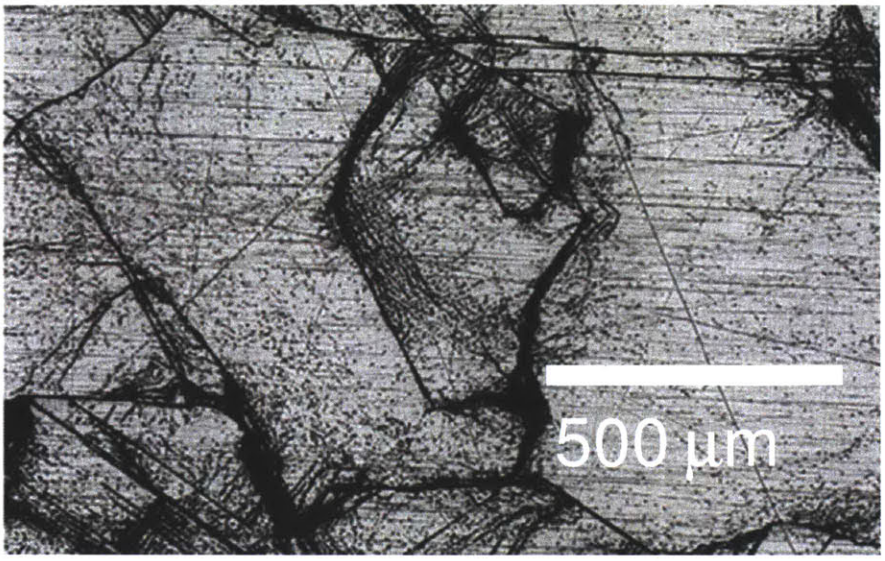


Figure 4.9: Abaqus CAE results for the stress induced in a 3.5cm cube for cyclic annealing profile B. The maximum stress is still higher on the outer edge than in the core of the sample, but not as drastically as for profile A.

To see if this stress difference was enough to have an impact on the dislocation density reduction, the outer faces of the samples from Brick #1 were also examined for dislocation density and compared to the controls. Using the outer faces, which were directly adjacent to the controls, has the additional advantage of making comparisons between the control and annealed samples much easier and more accurate. Because the surfaces are directly adjacent to each other, with only a small gap from material losses during sawing and polishing, the grain structures are similar, and it is possible to match a small area on one face to the corresponding area on the other face. Figures 4.10 through 4.12 show micrographs of such corresponding areas for each control/anneal pair.

a)



b)

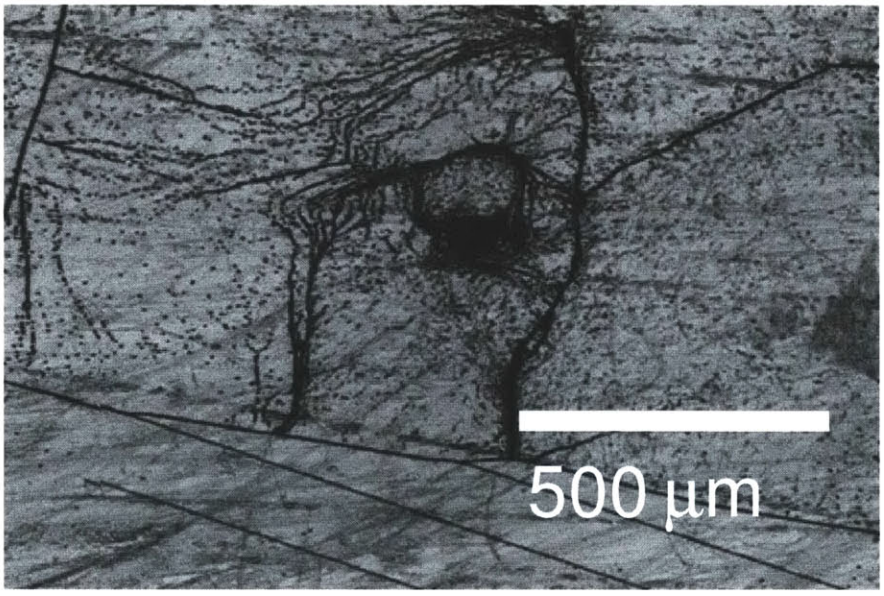
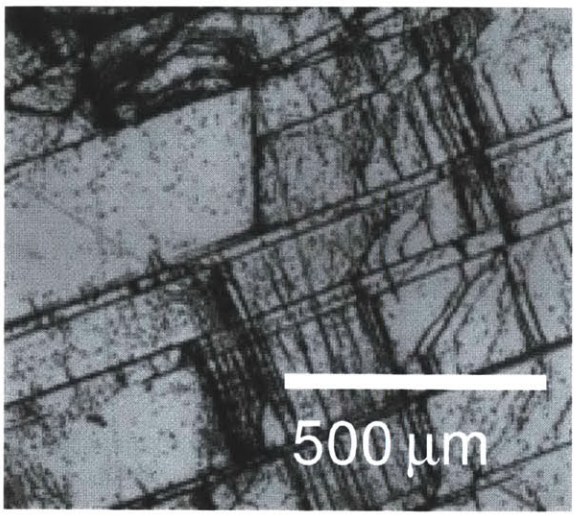


Figure 4.10: Micrographs of the outer edges of the control (a) and annealed (b) Brick #1 samples for a 6 hour static anneal at 1300˚C. Etch pits are approximately 5µm in diameter.

a)



b)

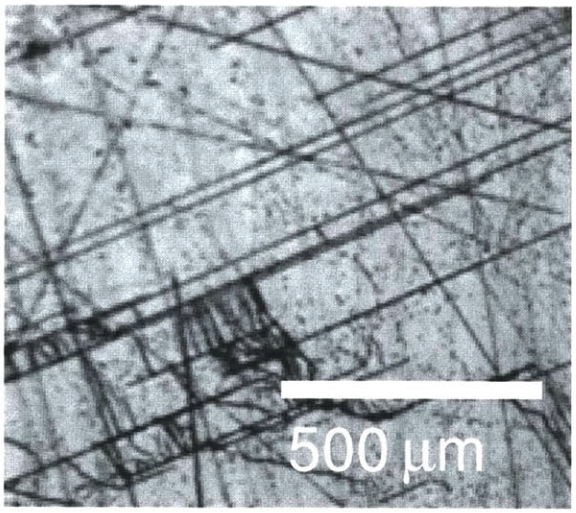
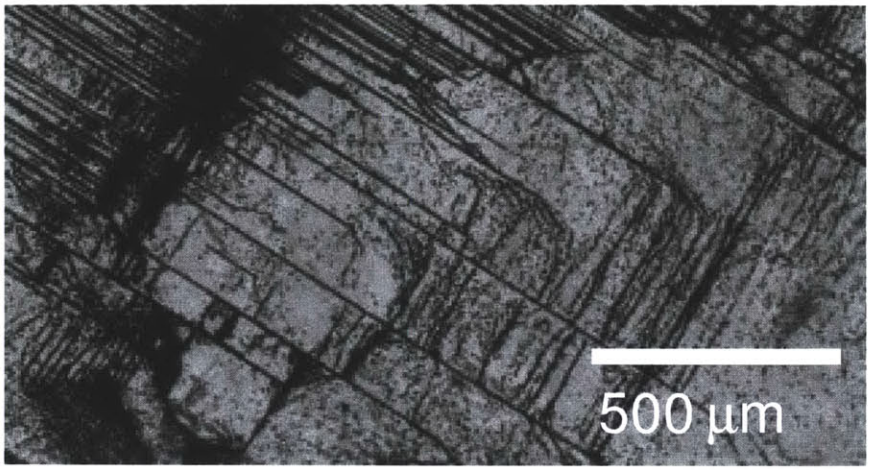


Figure 4.11: Micrographs of the outer edges of the control (a) and annealed (b) Brick #1 samples for a cyclic annealing profile A. Etch pits are approximately 5µm in diameter.

a)



b)

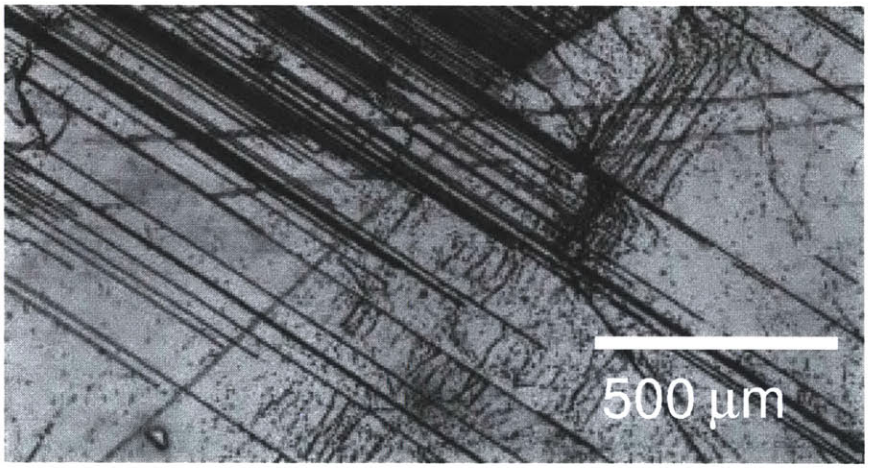


Figure 4.12: Micrographs of the outer edges of the control (a) and annealed (b) Brick #1 samples for a cyclic annealing profile B. Etch pits are approximately 5µm in diameter.

For the statically annealed sample in Figure 4.10, little reduction is seen. Referring back to Figure 3.4, it is seen that while there is some slight variation with position, the stress caused by static annealing is low throughout the sample. Both of the cyclically annealed samples, however, show significant dislocation density reductions. For cyclic annealing profile A, shown in Figure 4.11, where the stress at the sample's core was ~0.1MPa and the stress at the outer surface was ~0.4MPa, the reduction is ~63%. For cyclic annealing profile B, shown in Figure 4.12, where the stress at the sample's core was ~0.15MPa and the stress at the outer surface was ~0.4MPa the reduction is ~67%. It can be concluded that stresses of ~0.1MPa (or ~0.15MPa) are insufficient to cause dislocation density reductions, but stresses of ~0.4MPa do cause dislocation density reductions. To achieve greater reductions, stresses on the order of 1MPa would likely be necessary. This agrees with the estimates in Bertoni et al [20].

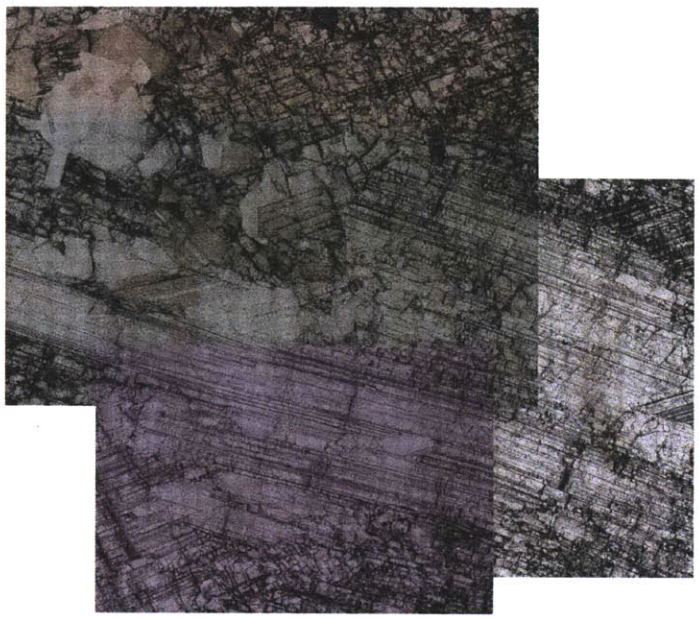
4.3 Dislocation density reduction in varied sample geometries

For the second set of experiments, the annealing profile was kept constant while sample geometry varied. All samples had a 3cm x 3cm cross section, but their length was varied as 1cm, 3cm, and 5cm. For this set of experiments, all samples were defect-etched and imaged in an optical microscope before and after annealing, making each sample its own control. At least 1mm of the surface was removed after annealing, so image forces should not be significant. The top (3cm x 3cm) face of each sample was examined. (Unlike the first experiment, only the outer surface was examined; no cross-sections were

taken. This means that the area examined experienced the largest stress that was present in the sample, and should therefore have the largest dislocation density reduction in the sample.)

The following three figures show the microscope scans before and after annealing. The images are composites of several large image scans on the optical microscope. Since the largest stress occurs on the edges, it was important to image (nearly) the whole face, not just the center. It is obvious just from a quick visual examination of the figures that the dislocation density remained the same or increased after annealing. This observation was also confirmed by closer analysis.

a)



b)

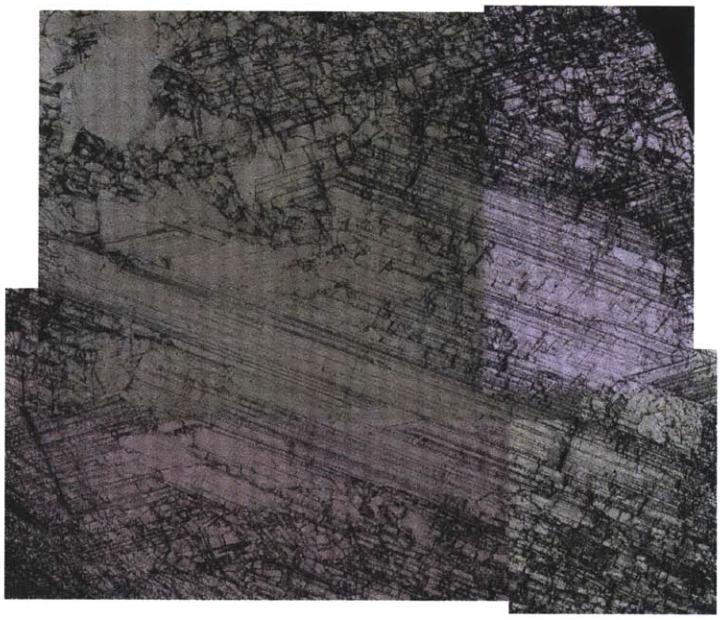
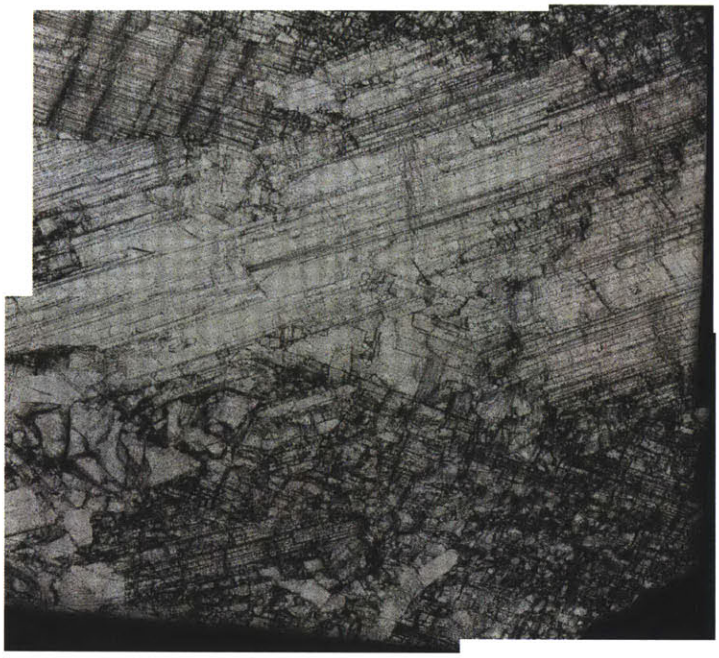


Figure 4.13: Defect-etched face of the 1cm block before (a) and after (b) annealing. Each image is approximately 30 x 30mm.

a)



b)

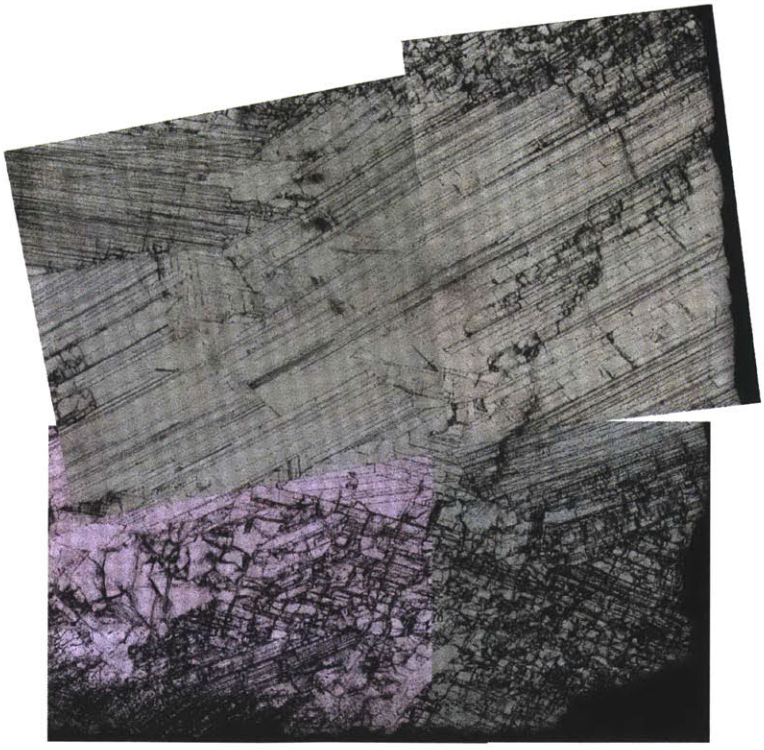
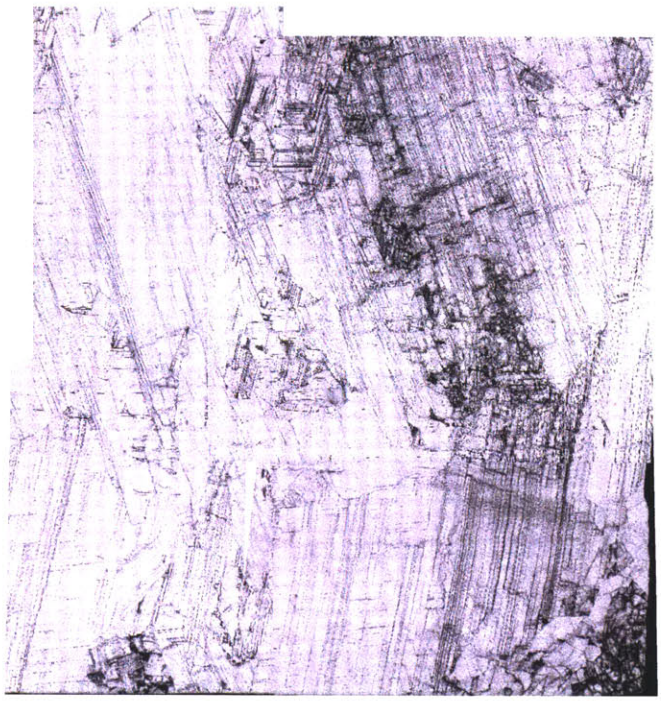


Figure 4.14: Defect-etched face of the 3cm block before (a) and after (b) annealing. Each image is approximately 30 x 30mm.

a)



b)

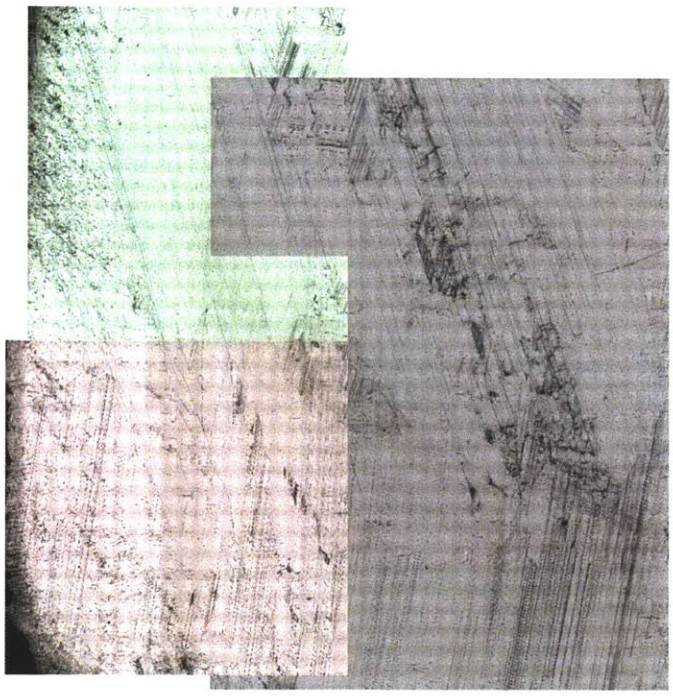


Figure 4.15: Defect-etched face of the 5cm block before (a) and after (b) annealing. Each image is approximately 30 x 30mm.

This is a troubling result, as it at first appears to conflict with the results from the first set of experiments. The expected result was that a reduction in dislocation density would occur, and that it would be greater for the larger sample sizes. However, there are several other variables in the experiment that explain why it would not have a dislocation density reduction, and why its results are not inconsistent with those of the first experiment. The key parameter is the maximum temperature, which was considerably lower in the second set of experiments.

For the first set of experiments, the temperature in the tube of the furnace ranged from roughly 1250°C to 1300°C, while in the second set of experiments it ranged from roughly 1150°C to 1200°C. (This was caused unavoidably by the use of a different tube in the second set of experiments, which was twice the thickness of the first tube. This increase in thickness roughly doubled the temperature difference between the inside of the tube and the main body of the furnace.) As determined by Hartman et al [18] for static anneals, the minimum temperature for dislocation density reduction is roughly 1200°C. In the set of experiments, the temperature was simply too low for dislocation density reduction to occur. Instead, it is possible that the thermal stresses applied to the samples caused the dislocations in the samples to multiply.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

5.1.1 Application of stress through cyclic annealing

It is clear from the FEA modeling that cyclic annealing can be used to apply stress to blocks of silicon, and that the stress level can be adjusted by adjusting the sample geometry and annealing parameters. The applied stress increases with sample size, cyclic annealing amplitude, and ramp rates.

However, it is also clear from the FEA model that the stress applied to the block is far from uniform. The stress is concentrated on the outer faces and especially the edges. The difference in stress level between the center of the block and the outer edge is significant (a factor of four for cubes at certain annealing conditions). Due to this variation, the majority of the sample is below the desired stress level.

5.1.2 Effects of stress and cyclic annealing on dislocation density

Cyclic annealing can reduce dislocation density, but only for certain stress conditions. If the stress is too low, it will have no impact on the dislocation density reduction. Stresses on the order of 0.1MPa were observed to be too low to cause a reduction. However, high stresses must also be avoided, as they cause dislocations to multiply. Stresses of roughly 0.4MPa were observed to cause a reduction on the order of 60%. It is estimated that to get a higher reduction, stresses of roughly 1MPa should be applied to the sample.

The temperature range of cyclic annealing is also important to achieving a dislocation density reduction. Hartman et al.[18] found that 1200°C was roughly the minimum temperature for a significant dislocation density reduction in static annealing (for six hour anneals). This appears to be the minimum temperature for cyclic annealing as well. For cyclic anneals conducted below this temperature (and lasting six hours), no reduction was observed.

5.2 Future work

While cyclic annealing does cause dislocation density reduction in multicrystalline silicon blocks under the right conditions, there are drawbacks that make it an undesirable method of reducing dislocation densities. The most significant flaw is its uneven application of stress to the sample. Even in small blocks, the majority of the sample is not subjected to the desired level of stress. Due to this flaw, it may be more fruitful to pursue other stress application methods.

One significant contribution this research has made to future work is in locating the proper stress level for dislocation density reduction. Too low of stress will have little to no effect, while too high of stress will cause dislocation multiplication. The proper level of stress for dislocation density reduction was found to be ~1MPa, for temperatures in the range of 1300°C. This agrees with the estimates of Bertoni et al [20]. Future studies of dislocation density reduction through contact- or non-contact methods of stress application at high temperatures may use this as a target stress level.

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