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Measuring Charge Transport in a Thin Solid Film Using Charge Sensing

Kenneth MacLean,* Tamar S. Mentzel, and Marc A. Kastner

Department of Physics, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

E-mail: kmaclean@mit.edu

Abstract

We measure charge transport in a hydrogenated amorphous silicon (a-Si:H) thin film using a nanometer scale silicon MOSFET as a charge sensor. This charge detection technique makes possible the measurement of extremely large resistances even in the presence of blocking contacts. At high temperatures, where the resistance of the a-Si:H is not too large, the charge detection measurement agrees with a direct measurement of current. The device geometry allows us to probe both the field effect and dispersive transport in the a-Si:H using charge sensing and to extract the density of states near the Fermi energy.

The dependence of electrical resistance on temperature, electric and magnetic fields, light exposure, and other variables, is one of the most important probes of novel effects in solid state physics. For materials with excessively large resistance, traditional transport measurements fail because the current at reasonable voltages becomes too small to measure, and a new method is needed. Highly resistive materials of technological importance include arrays of semiconductor nanocrystals,^{1,2} which are candidates for solar energy harvesting,³ and high dielectric constant materials,⁴ which are vital to modern microelectronics. In the study of single electron devices, charge measurement

To whom correspondence should be addressed

using a sensor integrated with the device⁵ has recently been widely utilized to probe quantum mechanical phenomena that would be impossible to observe by measuring current.^{6–10} However, a study of the charge transport properties of a resistive material using an integrated charge sensor has yet to be realized.

In this Letter, we illustrate the power of this charge sensing technique by investigating transport in hydrogenated amorphous silicon (a-Si:H). By patterning a strip of a-Si:H thin film adjacent to a nanometer scale silicon MOSFET, we are able to detect charging of the a-Si:H and measure extremely high resistances ($\sim 10^{17} \Omega$) using moderate voltages (~ 1 V). Our device geometry, in which the MOSFET sensor and a-Si:H can be gated independently, allows us to investigate the field effect¹¹ and dispersive transport,^{12,13} and we use these techniques to measure the density of localized states near the Fermi energy. Our method constitutes a new resistance measurement that is made possible by the extremely small input capacitances achievable with integrated charge sensors. This new resistance measurement is insensitive to the resistance of the contacts supplying the charge, and should be applicable to a wide variety of thin solid films.

Our charge sensor is an n -channel MOSFET that is electrostatically coupled to a strip of a-Si:H. An electron micrograph of the structure is shown in Figure 1a. The MOSFET is fabricated using standard techniques on a p -type silicon substrate. The n^+ polysilicon gate of the MOSFET is patterned using electron beam lithography and reactive ion etching and tapers down to a width of ≈ 60 nm. For all of the measurements reported here, a positive voltage is applied to the gate so that the MOSFET is in inversion. The characteristics of this narrow channel MOSFET are similar to those reported previously.¹⁴ Because of its narrow width, the MOSFET is extremely sensitive to its electrostatic environment.¹⁵ Approximately 70 nm away from the narrowest portion of the MOSFET, we pattern a strip of a-Si:H.

The a-Si:H is deposited by plasma enhanced chemical vapor deposition,¹⁶ with a gas phase doping ratio and hydrogen dilution of $[\text{PH}_3] / [\text{SiH}_4] = 2 \times 10^{-2}$ and $[\text{H}_2] / [\text{SiH}_4 + \text{H}_2] = 0.5$, respectively. Because we use a large doping level, we expect a large defect density $N_D \sim 10^{18} \text{ cm}^{-3}$.¹⁶ The deposition substrate temperature is $T_s = 200$ C, and the deposition rate is ≈ 0.17

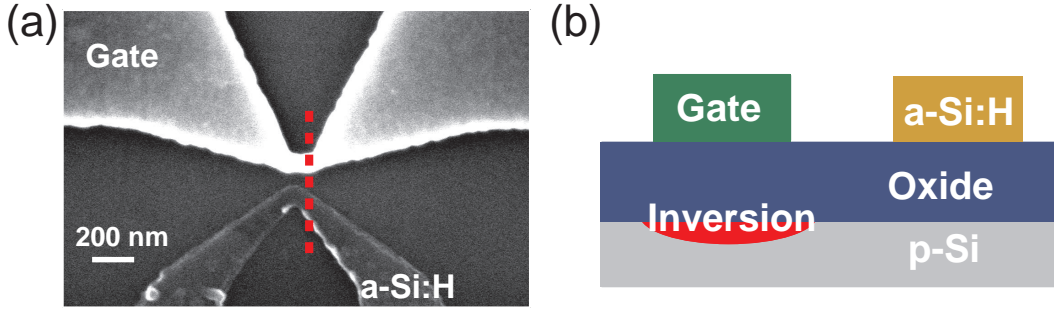


Figure 1: (a) Electron micrograph of MOSFET gate and a-Si:H strip. A positive voltage is applied to the MOSFET gate, forming an inversion layer underneath. (b) Vertical sketch of the device geometry along the dashed line in (a). The MOSFET has a relatively thick (= 100 nm) oxide, which ensures that the metallic polysilicon gate does not effectively screen the inversion layer from nearby electrostatic fluctuations.

nm/s. The a-Si:H is patterned using electron beam lithography and a lift-off technique, which will be described in a subsequent publication. The a-Si:H strip is connected to two gold contacts (separated by $\approx 2 \mu\text{m}$), and the MOSFET inversion layer is contacted through two degenerately doped n^+ regions, none of which are shown in Figure 1a.

When we deposit a-Si:H films ≈ 200 nm thick under the aforementioned conditions, the conductivity and activation energy are similar to those reported elsewhere.¹⁶ However, the sample studied in this work is nanopatterned (≈ 100 nm wide at its narrowest point) and also is only ≈ 50 nm thick. Thus, although the characteristics reported below are similar to what one would expect for thick heavily doped films, we expect that for our sample surface effects may be significant,¹⁷ and there may also be differences in morphology and hydrogen content as compared with thicker films.

Our measurement consists of monitoring the MOSFET conductance G_M as a function of time after changing the voltage applied to one a-Si:H contact (Figure 2a). At $t = 0$ we rapidly change the voltage applied to one of the a-Si:H contacts while the other contact is held at 0 V. This causes additional electrons to move onto the a-Si:H strip from the gold contacts. The MOSFET senses this change in charge electrostatically, and G_M decreases with time. This effect is shown in Figure 2a. This decrease in G_M is caused by the charging of the a-Si:H strip, and we henceforth refer to it

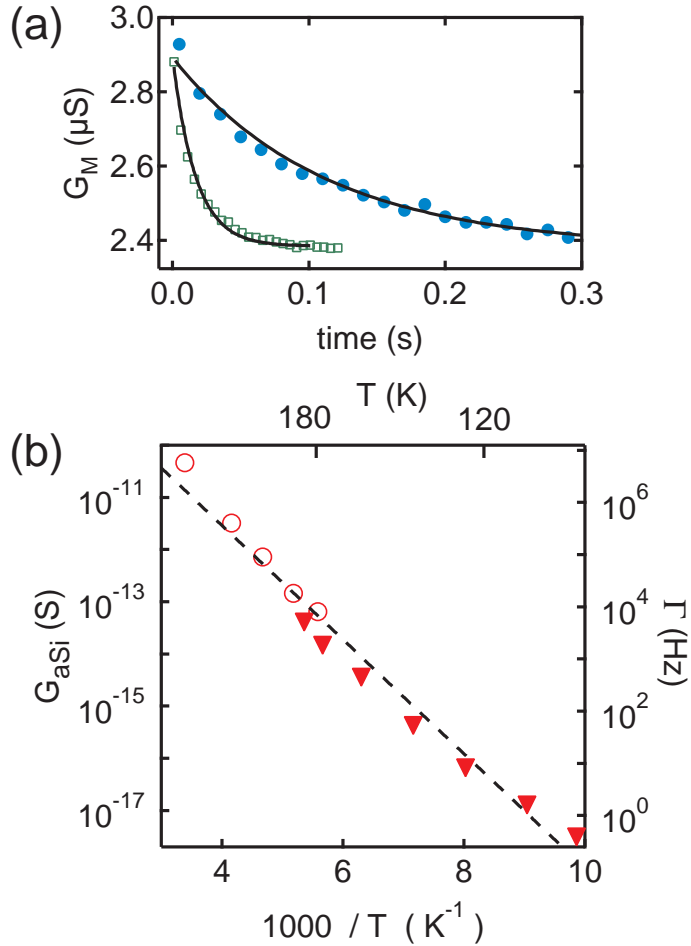


Figure 2: (a) G_M as a function of time at $T = 125\text{ K}$ (closed circles) and 140 K (open squares), the latter is offset for clarity. At $t = 0$ the voltage applied to one of the a-Si:H contacts is changed from -1.8 V to -2.7 V . A similar decrease in G_M is observed when the change in voltage is applied to the other a-Si:H contact or to both contacts simultaneously. When the voltage is changed back to its original value, the same transient is observed but with the opposite sign. For these traces multiple charge transients have been averaged to improve signal-to-noise. The solid lines are theoretical fits described in the main text. (b) Conductance through the a-Si:H G_{aSi} , obtained from charge transients (closed triangles) and from measuring current (open circles) with a voltage bias across the a-Si:H of $\approx -2.3\text{ V}$. For the charge transient measurement Γ is given on the right hand axis. The dashed line is a theoretical fit described in the main text.

as a charge transient.¹⁸ For increasing temperature, we find an increase in the rate at which G_M decreases, or a faster charge transient.

For a resistive film with a distributed capacitance, the charge stored as a function of position and time $\sigma(x, t)$ obeys the diffusion equation, with a diffusion constant given by $D^{-1} = CR_{sq}$.^{19,20} Here C is the capacitance per unit area between the a-Si:H and the underlying substrate,²¹ and R_{sq} is the resistance per square of the a-Si:H film. For a strip of material of length L , for which the potential at one end is changed from $V + \Delta V$ to V at $t = 0$, the charge at any point along the strip varies exponentially with time as $\sigma(t) \approx \sigma_\infty + \sigma_\Delta e^{-\Gamma t}$ for sufficiently large t . Here $\Gamma = \pi^2 D/L^2$, and σ_∞ and σ_Δ are constants that depend on V , ΔV , and C . For a sufficiently small voltage step G_M varies linearly with σ , so $G_M(t) \approx G_\infty + G_\Delta e^{-\Gamma t}$. The solid curves shown in Figure 2a are fits to this equation, from which we extract the rate at which the a-Si:H charges Γ .²²

From our measurement of Γ and the values of L and C for our a-Si:H strip, we extract R_{sq} , and from this compute the conductance through the a-Si:H strip $G_{aSi} = w/(R_{sq}L)$, where w is width of the a-Si:H strip. In Figure 2b we plot G_{aSi} and Γ as functions of temperature. G_M is weakly temperature dependent, so for this data we adjust the MOSFET gate voltage at each temperature to keep G_M approximately constant. At higher temperatures we can directly measure $G_{aSi} = dI/dV$, where V is the voltage between the a-Si:H contacts, and these results are also shown in Figure 2b. At $T \approx 180$ K, we measure G_{aSi} using both methods, and the results are in good agreement. The measurements are complementary, in that the charge transient method is easier to implement for smaller G_{aSi} because the charging is slower, while a measurement of current is only possible for larger values G_{aSi} . The dashed line in Figure 2b is a fit to $G_{aSi}(T) = G_0 e^{-E_a/kT}$. The data are thus consistent with an activated transport mechanism, with an activation energy $E_a \approx 200$ meV, as is typically observed for a-Si:H films heavily doped with phosphorous.¹⁶

At the lowest temperatures, we measure resistances as high as $\sim 10^{17} \Omega$. To understand the origin of this unique capability, we note that following a change in the a-Si:H contact voltage, the a-Si:H strip charges with a time constant $\tau = R_{aSi}C_E$, where here $R_{aSi} = 1/G_{aSi}$ is the resistance of the strip, and we define an effective capacitance between the a-Si:H and silicon substrate $C_E =$

CwL/π^2 . Thus τ can be regarded as the charging time for an RC circuit. In principle, to determine large resistances, a measurement of an RC charging time is superior to a measurement of current. The time required for a charging time measurement is proportional to $\tau = RC$. For a measurement of current, the time required to obtain a fixed signal-to-noise ratio is inversely proportional to the current squared, and thus is proportional to R^2 . A charging time measurement therefore requires less time than a measurement of current in the limit $R \rightarrow \infty$. However, this fundamental advantage cannot be exploited using a voltage amplifier, which introduces a large input capacitance, resulting in a large τ .

For our device we have $C_E \sim 10$ aF, which is many orders of magnitude smaller than the input capacitance of a voltage amplifier, even when great care is taken to minimize the latter.²³ Based on the geometry of our device (Figure 1b), the charge sensor input capacitance, between the a-Si:H strip and the MOSFET gate and inversion layer, is even smaller than C_E . Because C_E is so small, a result of the nanometer scale dimensions of the a-Si:H strip, τ remains measurably short, even for extremely large R_{aSi} . Aside from the requirement that τ be short, our measurement is in principle only limited by the finite resistance of the oxide: τ must be less than the oxide dielectric relaxation time.

We can also use our charge sensing technique to investigate the field effect in the a-Si:H (Figure 3). We apply the same voltage V_{aSi} to both a-Si:H contacts relative to the p -type substrate. This has the effect of gating the a-Si:H strip with the p -type substrate with an effective gate voltage $V_g = -V_{aSi}$. We then add a small voltage step $\Delta V \approx 0.5V$ to V_{aSi} to produce a charge transient, from which Γ is extracted as in Figure 2a. Unlike previous related experiments,²⁴ our geometry allows us to maintain an approximately constant value for the MOSFET conductance, and thus to maintain a high charge sensitivity, as we make large changes in V_{aSi} by applying smaller compensating voltage shifts to the MOSFET gate voltage. This allows us to perform this field effect measurement for a large range of a-Si:H conductances.

In Figure 3 we plot Γ as a function of V_g at three different temperatures. We see that Γ rises with V_g , indicating that the a-Si:H is n -type, as expected. The exponential increase in Γ with V_g is

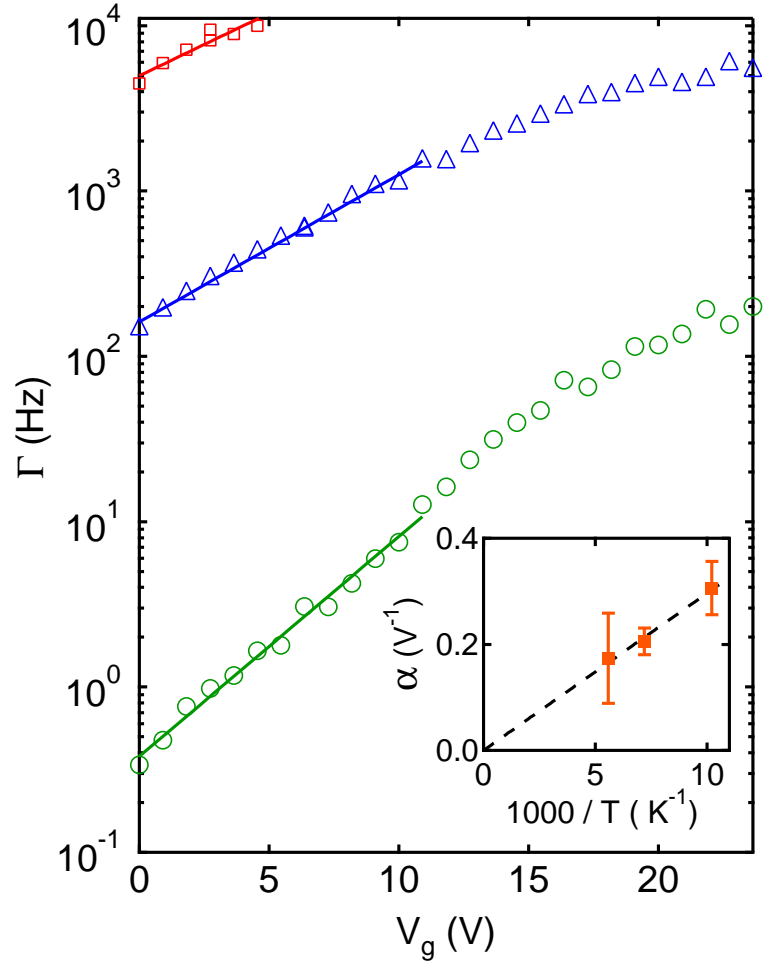


Figure 3: Γ as a function of V_g at $T = 98$ K (circles), 139 K (triangles), and 179 K (squares). The solid lines are theoretical fits described in the main text. For the range of voltages used here E_F moves by an amount comparable to values of the band tail width commonly found for a-Si:H films,¹⁶ so we expect that $\rho(E_F)$ should increase somewhat as V_g is made more positive and E_F is moved in the band tail. This may cause the observed decrease in α , as defined in the main text, for $V_g > 15$ V. (Inset) α as a function of inverse temperature. The dashed line is a theoretical fit described in the main text.

consistent with the activated conduction found in Figure 2b, for an approximately constant density of localized states. We have:

$$\Gamma = \omega_0 e^{-E_A/kT} \quad (1)$$

Here ω_0 is a prefactor that depends only weakly on temperature, and the activation energy E_A is reduced as the gate voltage moves the Fermi level closer to the mobility edge. The logarithmic slope $\alpha = \partial \ln(\Gamma)/\partial V_g$ is then given by $\alpha = \frac{1}{kT} \partial E_A/\partial V_g = C/(ekT \rho(E_F) s_{tf})$, where $\rho(E_F)$ and s_{tf} are the density of states at the Fermi energy and Thomas-Fermi Screening length, respectively.² Thus we expect an exponential increase in Γ with V_g as long as the product $\rho(E_F) s_{tf}$ is constant.

At each temperature, we fit the data to obtain α (solid lines in Figure 3), and, in the inset to Figure 3, we plot α as a function of inverse temperature. The dashed line is a linear fit (constrained to pass through zero) and is consistent with the data. From the slope of this fit we obtain $s_{tf} \rho(E_F) \approx 5 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$, and, expressing s_{tf} in terms of $\rho(E_F)$ and the a-Si:H dielectric constant,² we solve for $\rho(E_F) \sim 10^{20} \text{ eV}^{-1} \text{ cm}^{-3}$. The density of states at the Fermi level for phosphorous doped a-Si:H obtained from more commonly used transport techniques is typically $\sim 10^{19} \text{ eV}^{-1} \text{ cm}^{-3}$.¹¹ The fact that our $\rho(E_F)$ is somewhat high is not surprising, given the large gas phase doping level used in our a-Si:H film deposition.

At lower temperatures, where the time scale for charging is longer, we observe dispersive transport (Figure 4a).^{12,13} When we step V_{aSi} from 0 V to -24 V, G_M quickly drops. However, when V_{aSi} is stepped back to 0 V, G_M rises at slower rate, and does not regain its original value. This behavior can be understood as follows: After the negative V_{aSi} step the a-Si:H quickly charges, as electrons enter the a-Si:H at energies close to the conduction band. However, as time progresses, these electrons get trapped in localized states deeper in the band gap. When the voltage is returned to its original value, the a-Si:H therefore takes a much longer time to discharge: From Eq. (1), the time necessary to release electrons from states at an energy E_A below the transport energy is $t \sim \Gamma^{-1} = \omega_0^{-1} e^{-E_A/kT}$. As electrons are released from states progressively deeper in the gap, t grows, and thus the transport process becomes dispersive.^{12,13}

This can be made quantitative: At a time t after the negative voltage step, only electrons in

localized states with activation energies $E_A < E_{max} = kT \ln(\omega_0 t)^{12,13}$ are able to escape from the a-Si:H. The charge on the a-Si:H is then given by $\sigma(t) = e \int^{E_{max}} s_{tf} \rho(E_A) dE_A$ (up to an additive constant). Assuming a constant density of states and differentiating with respect to time we obtain:

$$d\sigma/dt = e s_{tf} \rho(E_F) kT / t \quad (2)$$

In Figure 4b we plot the derivative of G_M with respect to time on a log-log plot: A fit to a power law dependence (solid line) yields a power of -1 ± 0.1 as expected. Moreover, from the prefactor of this power law we obtain $\rho(E_F) \sim 10^{20} \text{ eV}^{-1} \text{ cm}^{-3}$, consistent with the value extracted from the data in Figure 3.

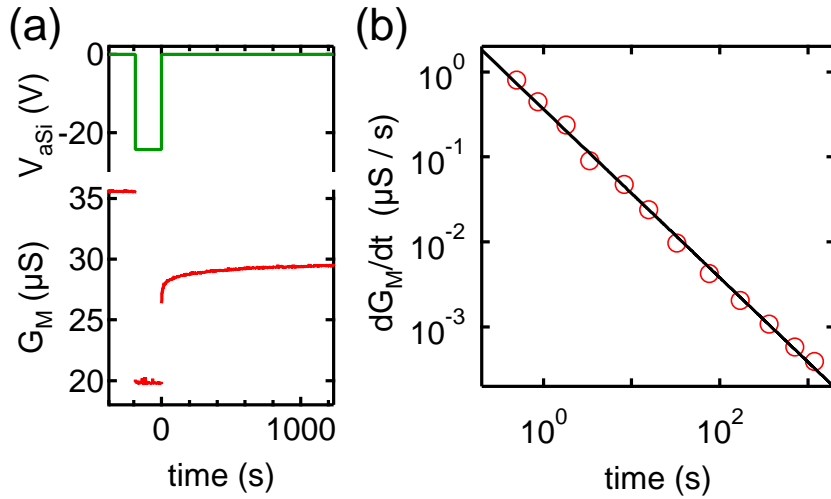


Figure 4: (a) Voltage applied (top panel) and transistor conductance (lower panel) used to measure dispersive transport at $T = 89 \text{ K}$, as discussed in the main text (b) $dG_M(t)/dt$ extracted from the data shown in (a). The solid line is a theoretical fit described in the main text.

Whereas the measurements of Γ shown in Figure 2 and Figure 3 do not depend strongly on the voltage applied between the a-Si:H contacts for voltages $< 1 \text{ V}$, we observe a large nonlinearity when we measure current as a function of voltage at room temperature at a voltage of $\approx 500 \text{ mV}$. While the source of this disagreement is unclear, it is possible that at zero bias the steady state current is limited by the narrow constriction or by the contacts. The charge detection method is not sensitive to such effects because it only requires that charge moves in the a-Si:H, and not

that the charge flows continuously through the entire sample. Indeed, our charge sensing method is effective even in the presence of blocking contacts; it can detect charge diffusing toward the contact even with infinite contact resistance as long as there is significant contact capacitance. Future work will study in detail the sensitivity of our technique to contact resistance.

In summary, integration of a charge sensor provides a new technique that makes it possible to characterize the charge transport properties of extremely resistive materials, even with poor contacts. While we have chosen a-Si:H as an example, we expect that the technique will be useful for a wide variety of materials and systems.

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