POLYCRYSTALLINE Si THIN FILMS AND DEVICES:
I. SEED SELECTION THROUGH ION CHANNELING
II. THIN-FILM TRANSISTORS

by

KENNETH TING-YUAN KUNG

Bachelor of Science
Electrical Engineering
California Institute of Technology
(1983)

Master of Science
Electrical Engineering and Computer Science
Massachusetts Institute of Technology
(1985)

Submitted to the
Department of Electrical Engineering and Computer Science
In Partial Fulfillment of the Requirements
For the Degree of

DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

January 1988

Signature of Author _____
Department of Electrical Engineering and Computer Science
January 8, 1988

Certified by _____
Rafael Reif
Thesis Supervisor

Accepted by _____
Arthur C. Smith
Chairman, Departmental Committee on Graduate Students

POLYCRYSTALLINE Si THIN FILMS AND DEVICES: I. SEED SELECTION THROUGH ION CHANNELING II. THIN-FILM TRANSISTORS

by

KENNETH TING-YUAN KUNG

Submitted to the Department of Electrical Engineering
and Computer Science on January 8, 1988 in partial fulfillment
of the requirements for the Degree of Doctor of Philosophy
in Electrical Engineering and Computer Science

ABSTRACT

Part I of this thesis investigates the "seed selection through ion channeling" process, employed to modify the grain size and crystallographic texture of polycrystalline Si thin films deposited on SiO_2. In each of the three experiments, polycrystalline Si films prepared by the low-pressure chemical-vapor deposition technique were used as the starting material. Si self-implantation, at a fixed angle and energy (normal incidence and 200 keV, or 60° from normal incidence and 350 keV) but with variable doses ($1–20\times10^{14}$ cm^{-2}), was then used to selectively amorphize the material. Ideally, the implantation step should amorphize a major fraction of the film and preserve only those crystallites that are properly oriented for ion channeling. A low-temperature furnace anneal, at 600°C for 48 h in an N_2 ambient, was then carried out to crystallize the film. Ideally, the crystallization should proceed due entirely to the growth of the surviving crystallites, and should exclude any effect due to spontaneous nucleation. The overall results obtained demonstrate that, by optimizing the implant dose, one can produce strong fiber-textured polycrystalline Si films on SiO_2. The production of restricted-fiber-textured films, on the other hand, will have to await the availability of more sophisticated implantation and annealing equipment.

Part II of this thesis investigates the metal-oxide-semiconductor thin-film transistors fabricated on the modified polycrystalline Si films. For transistors fabricated with a maximum processing temperature of 600°C, with deposited gate oxide, it was shown that the grain-size enlargement (achieved through amorphization-crystallization) can lead to significant improvements in the device characteristics. For transistors fabricated with a maximum processing temperature of 800°C, with thermally grown gate oxide, it was shown that both the

grain size and grain orientation can be important parameters in determining the device performance; for grain sizes of the order of 1–2 μm, a stronger {110} texture can, in fact, lead to better devices than a larger average grain size. These results demonstrate how the surface effects, in addition to the grain-boundary effects, can limit the performance of polycrystalline Si thin-film transistors.

Thesis Supervisor: Rafael Reif
Associate Professor
Electrical Engineering and Computer Science

ACKNOWLEDGMENTS

I would like to thank my thesis advisor, Prof. Rafael Reif, for his encouragement, guidance, and support throughout the course of this work. Working under his supervision has been a pleasant and unforgettable experience for me, and I certainly hope that he feels the same way about having me around.

I would also like to thank my thesis readers, Profs. Charles G. Sodini and Carl V. Thompson, for their patience in dealing with me, and for their helpful suggestions. Because of Charlie, I learned how to take it easy with polysilicon deposition tubes.

This work was carried out using the facilities of the MIT Center for Materials Science and Engineering (CMSE) and the MIT Microsystems Technology Laboratories (MTL). I am grateful to the various student, staff, and faculty members of CMSE and MTL, who helped me at various times, and provided me with such a stimulating environment to work in.

I am indebted to Prof. Marc-A. Nicolet of the California Institute Technology, who granted me unlimited access to their ion implantation facility; he did so even after I had left him to go to MIT. I am also indebted to my other friends at Caltech, Frank C. T. So, Tom C. Banwell, Sung-Jung Kim, and Rob Gorris, who put in their time and energy running and maintaining the ion implanter, in times of my desperation. Without their help, this thesis would not have materialized.

The x-ray diffraction work was done in the MIT Lincoln Laboratories. The generosities of Alan J. Strauss, Bor-Yeu Tsaur, Mike W. Geis, Steve H. Groves, Gerald W. Iseler, E. Larry Mastromattei, Harry R. Clark, and many others in arranging for my access are highly appreciated.

Finally, I wish to thank my parents Charles and Gloria, for their love and support, and my fiancee Shirley, for her patience, and impatience.

This work was supported by the National Science Foundation (Grant No. 83-03450ECS) and the MIT Center for Materials Science and Engineering (NSF-MRL Grant No. DMR84-18718).

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

The development of silicon thin-film transistors (TFT's) for large-area electronics applications has been a subject of intensive research since the late 1960's [1]. The term "large-area electronics" refers, in general, to the many advanced input and output devices that mediate communications between the electronic processors and the human users. A characteristic feature of these input and output devices is the fact that they must have large dimensions in order to provide an effective interface with the human users. Some good examples of these devices include the flat-panel displays, image scanners, image printers, and xerographic copiers.

The TFT's used in these input and output devices must be fabricated on large-area, transparent glass substrates; therefore, their development faces two unique constraints that are not imminent in the case of conventional integrated-circuit technology. First, the transistors must have uniform characteristics over very large areas, in order to allow functional circuits to be fabricated over very large areas. Second, the transistors must be fabricated at low temperatures, to prevent any melting or warping of the underlying glass substrates. The glass substrates that are commercially available today can withstand processing temperatures of no more than 600°C. The latest Corning 1729 glass substrates will push the temperature limit up to 800°C [2], but they are not yet available commercially. Because of these two constraints, virtually all the large-area electronics applications assembled to date have employed hydrogenated amorphous silicon as the TFT material.

Hydrogenated amorphous silicon works within the uniformity and temper-

ature constraints, but it is far from being an ideal TFT material. The high density of trap states in the material leads to a high threshold voltage. The low charge carrier mobility, on the other hand, leads to a low current-pumping capacity. Together, they impose a limitation on the speed performance of the circuits. One way to improve the speed performance is to use another TFT material with a higher crystalline order. So far, polycrystalline silicon has emerged as the most attractive candidate to replace amorphous silicon.

The presence of grain-boundary states and surface states in the active region of a polycrystalline silicon TFT will degrade the transistor's performance, compared to what would be expected if the transistor were fabricated in monocrystalline, {100}-oriented silicon. The most important degradations due to the grain-boundary effect include a higher threshold voltage, a lower effective carrier mobility, and a higher leakage current. The most important degradations due to the surface effect include a higher threshold voltage and a lower effective carrier mobility. Most of the current research efforts on polycrystalline silicon TFT's have been focused on how to reduce the grain-boundary as well as the surface effects.

There are a number of techniques by which one can reduce the grain-boundary and/or the surface effects [1]. These techniques can be grouped into the following three categories:

(1) Hydrogen passivation. Hydrogen atoms can be introduced into a polycrystalline silicon film via a number of low-temperature ($\leq 400°$) techniuqes, such as sintering with a silicon nitride capping layer, exposure in a hydrogen plasma, and hydrogen implantation. The introduced hydrogen atoms can passivate the dangling silicon bonds at the grain boundaries and the surface, and thereby reduce the densities of the grain-boundary and surface states present.

(2) Grain-size enhancement. The average grain size of a polycrystalline sil-

icon film can be increased via liquid- or solid-phase recrystallization, using a laser, a lamp, an *e*-beam, or a graphite strip heater as the energy source. An increase of the average grain size can reduce the area of grain boundaries in the film.

(3) Grain-orientation realignment. The grain orientations in a polycrystalline silicon film can also be uniformly realigned via liquid- or solid-phase recrystallization, using any of the above-mentioned energy sources. Such a realignment of the grain orientations may reduce the grain-boundary effect: grain boundaries which result from a low-angle mismatch between the adjacent crystals [3] and grain boundaries which contain a high density of coincident lattice sites [4] have both been shown to exhibit little or no degradation of the electrical characteristics. It may also reduce the surface effect: a more favorable surface orientation can lead to more favorable surface properties at the gate dielectric-silicon interface [5], and this is a major issue that has been explored in this thesis (in Chapter 7).

We have investigated, in this thesis, the relationship between the material properties of a polycrystalline silicon film and the performance of TFT's fabricated in the film. The objective is to determine how these material properties can be modified to improve the TFT performance.

We have written this thesis in two parts. Part I describes the "seed selection through ion channeling (SSIC)" process, which has been employed to modify the grain size and crystallographic texture of polycrystalline silicon thin films deposited on oxidized silicon substrates. Part II describes the metal-oxide-semiconductor (MOS) thin-film transistors that have been fabricated on the modified polycrystalline silicon films. These overall results may have a significant impact on large-area electronics technology.

PART I

SEED SELECTION THROUGH ION CHANNELING (SSIC)

CHAPTER 2 BACKGROUND ON SSIC RESEARCH

CHAPTER 3 IMPLANT-DOSE DEPENDENCE OF SSIC: 0° IMPLANT ANGLE

CHAPTER 4 IMPLANT-DOSE DEPENDENCE OF SSIC: 60° IMPLANT ANGLE

CHAPTER 2

BACKGROUND ON SSIC RESEARCH

2.1 Process Description

Seed selection through ion channeling is a novel crystal-growth process that offers the attractive potential of growing large-grain, restricted-fiber-textured polycrystalline thin films on nonseeding substrates. The three steps of this process are schematically illustrated in Fig. 1.

The first step consists of the *deposition* of a polycrystalline film of the desired material onto the desired nonseeding substrate, as shown in Fig. 1(a). In principle, any deposition technique that yields a polycrystalline material may be used. In practice, however, it may be advantageous to employ a deposition technique that can offer a certain amount of the desired crystallographic texture in the starting material.

The second step consists of the *selective amorphization* of the film by ion implantation, as shown in Fig. 1(b). This implantation step should amorphize a major fraction of the film, and preserve only grains of a single, selected orientation due to ion channeling. This is to be achieved by using the proper implantation parameters including the ion species, energy, dose, angle, and temperature. Figure 1 pictures implantation(s) at only one implant angle, but implantations at more than one angle will most likely be required in order to eliminate all but one possible orientation in the film.

The final step consists of the *seeded crystallization* of the film in solid phase, as shown in Fig. 1(c). This crystallization step should proceed due entirely to the growth of the preserved crystallites, and should be completed before the

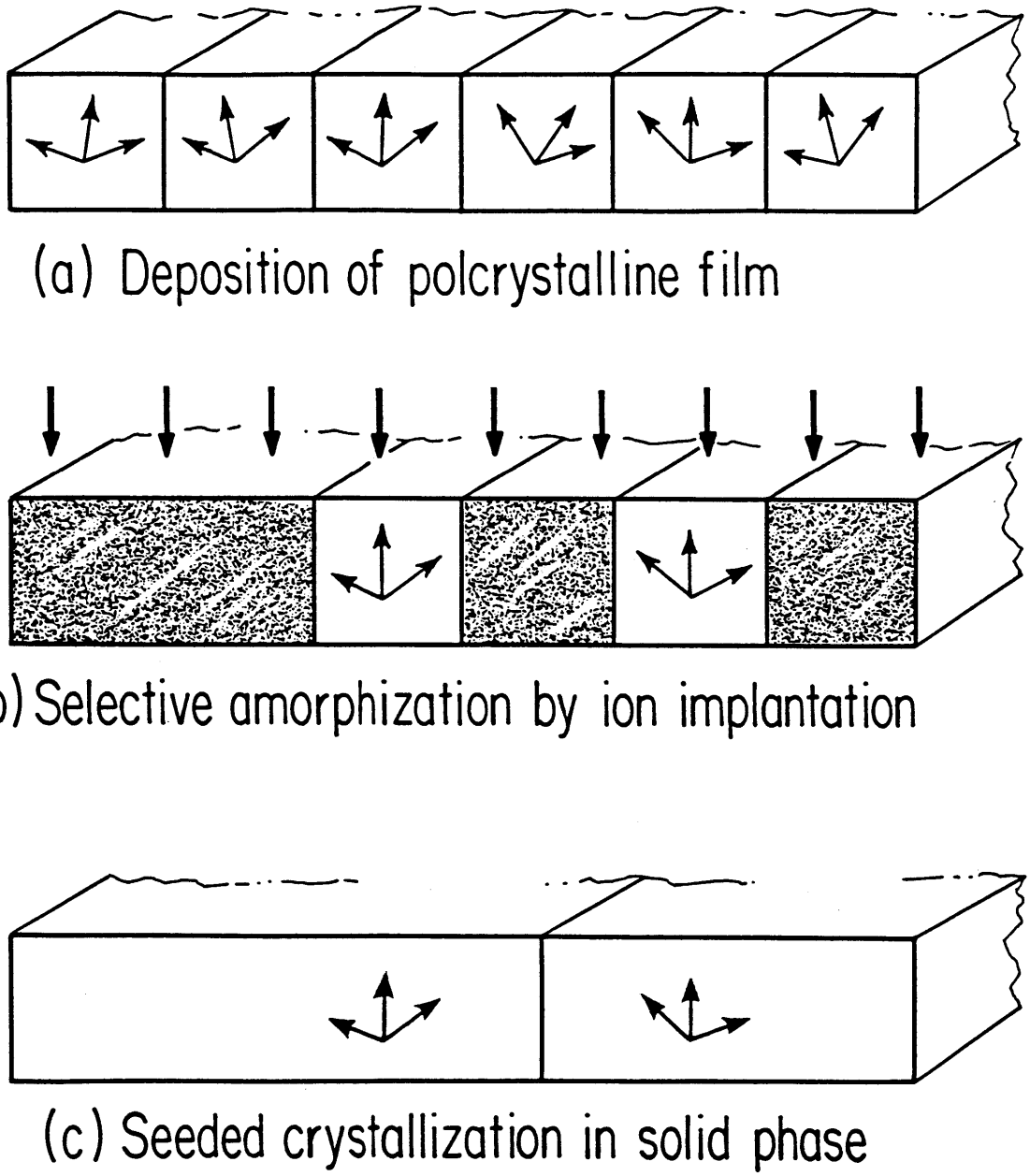


Figure 1 Schematic illustration of the seed selection through ion channeling process.

nucleation of any additional crystallites occurs. This is to be achieved by using the proper annealing parameters including the temperature, time, and ambient. At the end of the final step, a large-grain, uniformly oriented polycrystalline film should result on top of the nonseeding substrate.

The seed selection through ion channeling process offers some distinctive advantages for applications in silicon microelectronics. First, the entire process can be carried out in the solid phase. Solid-phase processes are preferred to liquid-phase processes because they lead to smoother film surfaces than liquid-phase processes. Second, the entire process can be carried out at low temperatures. The seeded crystallization in solid phase, which is presumably the process step with the highest operating temperature, is inherently a low-temperature process and can proceed at temperatures as low as around 500°C for silicon [6]. Third, the process can be carried out without the requirement of external seed crystals. The seed crystals, in this case, exist within the film and are selected via ion channeling. Together, these advantages make SSIC unique as a silicon-on-insulator technology and attractive especially for large-area electronics applications.

2.2 Overview of Previous Research

The seed selection through ion channeling process was proposed by Reif and Knott [7] in 1981, and had been investigated continuously by Reif and coworkers [8–13] at M.I.T. prior to the inception of this thesis. These previous investigations had all been performed with the objective of experimentally demonstrating the SSIC effect, and thereby confirming the existence of the SSIC process. They had employed, exclusively, polycrystalline silicon films prepared by the low-pressure chemical-vapor deposition technique at 625°C onto oxidized silicon substrates as the starting material. Such as-deposited films had been

shown [14,15] to possess a predominant {110} texture.

Depending on the analytical techniques employed, these previous investigations can be classified into two stages. The first stage of work [7–11] emphasized the crystallization behavior of ion-amorphized polycrystalline silicon films, and employed transmission electron microscopy (TEM) as the key investigative technique. They demonstrated that ion implantation followed by furnace annealing can significantly enhance the average grain size in a polycrystalline silicon film, from ≤ 0.05 μm up to ≤ 2 μm if silicon ions are implanted, or up to ≤ 7 μm if phosphorus ions are implanted. They also demonstrated, indirectly based on evidences from the crystallization behavior, the possibility of grain preservation via ion channeling and the possibility of crystallization seeded by the preserved grains. A mathematical model was also proposed [11] to describe the average grain size in an implanted and annealed film as a function of the processing parameters. This model is summarized in Appendix A.

The second stage of work [12,13] emphasized the realignment of crystalline orientations through implantation and annealing, and relied on the x-ray pole-figure technique for such analysis. They demonstrated that, as a result of a self-implant and a subsequent anneal, the <110> directions in a polycrystalline silicon film can be lined up to within $\pm 4°$ of the implant direction. These were direct observations of the SSIC effect and offered indisputable support to the existence of the SSIC process.

There are some issues regarding terminology which we must clarify before we go into the next section. Terms like "a fiber texture" and "a restricted fiber texture" have been used throughout our publications to describe two particular distributions of grain orientations that can occur in a polycrystalline film, and they will be used continually in this thesis. These two terms as well as their meanings here have been adopted from the general field of materials science, but

they may have different meanings in other disciplines. To minimize the chances for confusion, they are defined again below:

The statement that a film has "a $\{hkl\}$ fiber texture" means that the $<hkl>$ directions in the film are lined up to within an angular spread of the surface normal, but the in-plane directions in the film are still random.

The statement that a film has "a restricted $\{hkl\}$ fiber texture" means that the film has a $\{hkl\}$ fiber texture as well as a preferential in-plane orientation.

2.3 Overview of Present Research

To develop seed selecton through ion channeling into a viable silicon-on-insulator technology a comprehensive program is required, in which the materials process must be optimized and the device worthiness demonstrated. Part I of this thesis is devoted to the materials work, and Part II to the device work.

The optimization of seed selection through ion channeling requires, first, the establishment of a systematic approach. We have proposed such an approach [16]. We have also demonstrated the effectiveness of this approach in optimizing a basic process, which consists of a single implantation step performed at normal incidence and a single annealing step performed at 600°C [16,17]. A detailed discussion of these efforts is given in Chapter 3.

The growth of a restricted fiber texture via seed selection through ion channeling may require multiple-angle implantations to insure that only one orientation can remain in the film. We have used the same proposed approach to optimize another basic process, which consists of a single implantation step performed at 60° from normal incidence and a single annealing step performed at 600°C, as an alternative or an addition to the basic process of Chapter 3. The successful growth of a restricted fiber texture, as the results indicate, will have to

await the availability of a more sophisticated implantation-annealing equipment. A detailed discussion of these efforts is given in Chapter 4.

CHAPTER 3

IMPLANT-DOSE DEPENDENCE OF SSIC: 0° IMPLANT ANGLE

3.1 Introduction

The goal of our research on seed selection through ion channeling is to develop an optimized process for growing restricted-fiber-textured polycrystalline silicon films. Such films are characterized by the fact that all the crystallites in the film have essentially the same orientation, and all the grain boundaries are merely low-angle mismatches between the adjacent crystallites. Their growth via seed selection through ion channeling requires, in general, multiple-angle implantations to insure that only one crystalline orientation will remain. One possible way to formulate such an overall SSIC process that incorporates multiple-angle implantations is to employ a sequence of implant-anneal treatments, each with a different implant angle: the first treatment will fix the fiber texture, the second treatment will restrict the fiber texture, and so forth. Optimization of the overall process can then be achieved by optimizing each treatment in that order.

This chapter emphasizes the optimization of a single-implant, single-anneal, seed selection through ion channeling process which, in turn, resembles each of the implant-anneal treatments in an overall SSIC process incorporating multiple-angle implantations. The experimental procedure will be described in detail to emphasize the important issues requiring consideration. The results as well as their implications will serve as a basis for the next stage of work, to be discussed in Chapter 4.

3.2 Experimental Procedure

Starting with 2", lightly doped, <100> and <111> silicon wafers, a 0.1 μm thick SiO_2 layer was thermally grown at 1100°C in dry O_2. The use of two differently oriented substrates for each polycrystalline silicon film allowed investigation of all possible crystalline orientations in the film without interference from the substrate.

Polycrystalline silicon films of two different thicknesses, 0.35 μm and 0.44 μm, were then deposited on these oxidized wafers via the low-pressure chemical-vapor deposition technique. The deposition was carried out at 625°C, using SiH_4 as the source and N_2 as a dilutant. The combined partial pressure of SiH_4 and H_2 was 0.04 Torr, and the partial pressure of N_2 was 0.36 Torr, as measured at the output end of the reactor. The deposition rate was 0.020 μm/min, as measured from both ellipsometry and the surface profilometer technique. These as-deposited films were expected to possess a predominant but dispersed {110} texture [14,15]. (Kamins [15] had shown that one could obtain a {100} texture, instead of a {110} texture, in the as-deposited films by raising the deposition temperature to 725°C. Since {100} is the most preferable orientation of silicon for the operation of metal-oxide-semiconductor field-effect transistors MOSFET's [5], we had tried originally to obtain a {100} texture by following his work. However, we had observed nothing but a roughly constant {110} texture for the entire range of deposition temperatures attempted, which ranged from 625°C to 800°C and was limited by the maximum temperature our deposition reactor could handle. This explains why the {110}-textured films deposited at 625°C have been used consistently as the starting material in this thesis. We had also investigated the dependence of the {110} texture on the film thickness, for film thicknesses ranging from 0.10 to 0.50 μm. We had observed no crystal-

lographic texture for film thicknesses below 0.25 μm, and a {110} texture only for film thicknesses beyond 0.25 μm, the {110} texture increasing roughly with the film thickness. This explains why thicker-than-0.25 μm films have been used consistently throughout this thesis.)

These polycrystalline silicon films were then *selectively amorphized* via self-implantation. The implant was performed at normal incidence, to select crystallites with <110> directions normal to surface. The implant was performed, also, at a low temperature of 77°K, to improve the selectivity of this amorphization step: a low implant temperature would enhance the channeling phenomenon in properly oriented crystallites by reducing thermal vibrations of the crystal lattice [18], and would reduce the dynamic annealing phenomenon in the mis-oriented crystallites [19,20]. The implant energy, 200 keV for the 0.35 μm thick films and 210 keV for the 0.44 μm thick films, was chosen to position the peak of the damage energy density profile to slightly beyond one half of the film's depth. The implant doses, in the range of $5\text{–}20\times10^{14}$ cm^{-2} for the 0.35 μm thick films and $1\text{–}20\times10^{14}$ cm^{-2} for the 0.44 μm thick films, was chosen to yield damage energy densities in the vicinity of 6×10^{23} eV/cm^3, the amount needed for the critical amorphization of monocrystalline silicon [19,20]. The damage energy density profiles have been calculated using the extended Brice model [21], and are shown in Figs. 2 and 3 for the 200 keV and 210 keV implants, respectively. The implant dose was the only varying parameter in the entire seed selection through ion channeling process; it was the parameter to be optimized in this experiment.

These implanted silicon films were then crystallized via annealing in a conventional, atmospheric-pressure furnace. The annealing temperature, 600°C, was chosen under the following two constraints: it should be no higher than what is compatible with low-cost, commercial glass substrates (*i.e.*, no higher

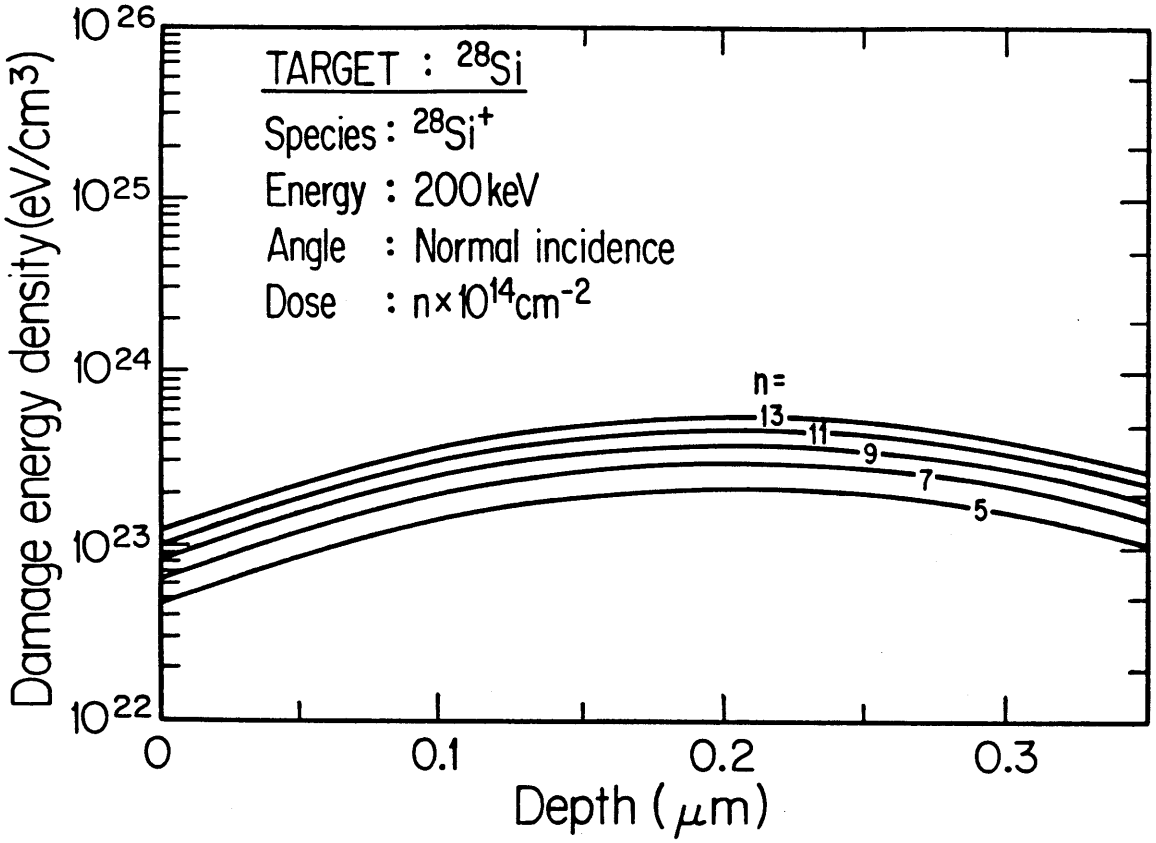


Figure 2 Theoretical damage energy density profile for a 200 keV silicon self-implant, shown for different doses. The profile has been calculated using the extended Brice model [21].

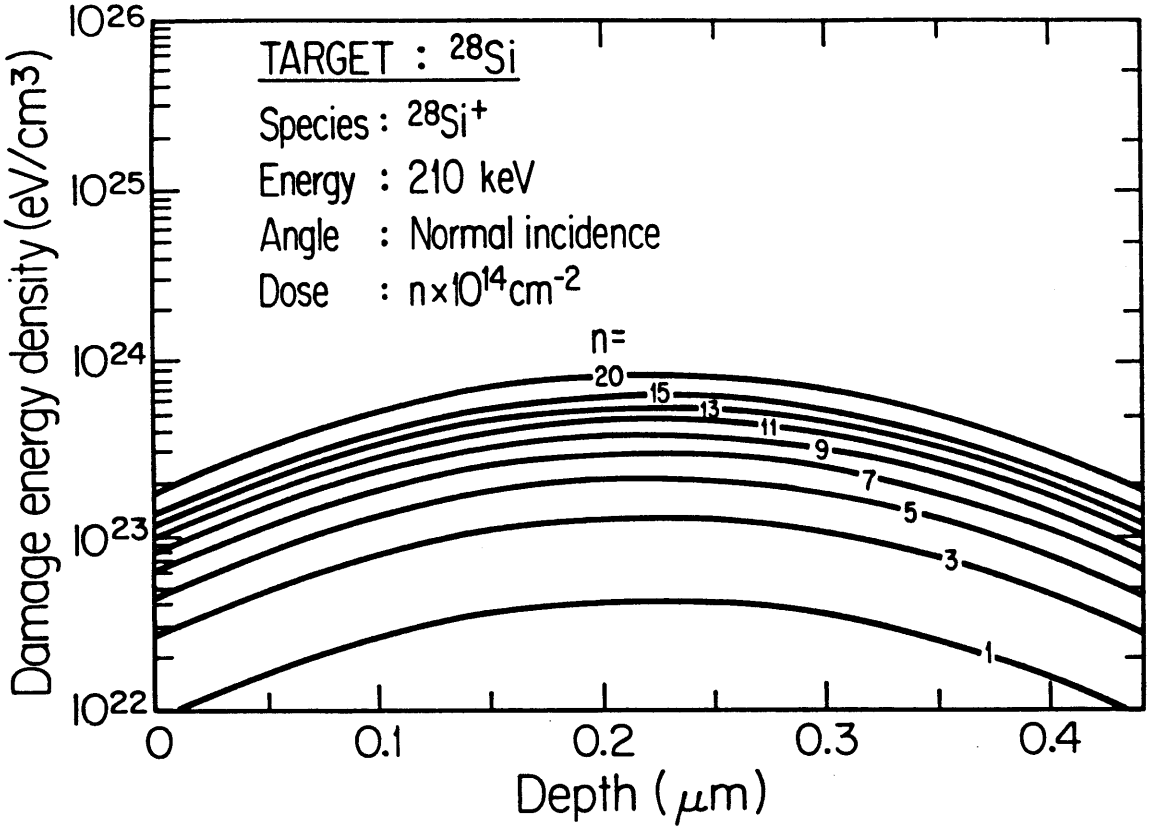


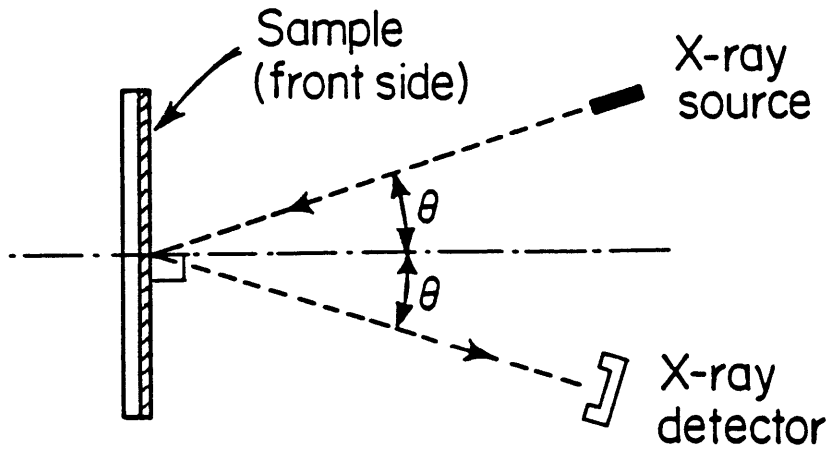
Figure 3 Theoretical damage energy density profile for a 210 keV silicon self-implant, shown for different doses. The profile has been calculated using the extended Brice model [21].

than about 600°C), but no lower than what is required to complete the crystallization within a reasonable time frame (*i.e.*, within no more than a few days). The annealing time, 48 h, was chosen correspondingly to insure the complete crystallization of the amorphized films: at 600°C, it would take approximately 24 h to crystallize a 0.5 μm thick, evaporated amorphous silicon film [22]. The annealing ambient, N_2, was chosen because it was the only inert ambient available for our furnace. The same set of annealing parameters (600°C, 48 h, and N_2) has been used consistently for all the seed selection through ion channeling processes in this thesis.

The average grain sizes of these polycrystalline silicon films were then determined via TEM. The TEM specimens were prepared by chemically etching through the backside of the silicon substrate, using mixtures of HF : HNO_3 : H_2O ($1 : 3 : n$). The etch rates were controlled by varying n, and ranged from about 10 μm/min at $n = 0$ to about 1 μm/min at $n = 10$.

The crystallographic textures of these polycrystalline silicon films were also determined via the x-ray pole-figure analysis. The x-ray pole-figure setup is schematically illustrated in Fig. 4. It consists of a hole-collimated monochromatic x-ray source, Cu$K\alpha$ at $\lambda = 1.541$ Å, and a sample rotation apparatus. It allows the measurement of the $\{hkl\}$ diffracted intensity, where the index $\{hkl\}$ is specified by the Bragg angle 2θ, as a function of ϕ, which is the angle between the surface normal and the diffracting $\{hkl\}$ planes. This is equivalent to measuring the angular distribution of the $<hkl>$ directions within the film. We have checked for diffractions from the {400}, {220}, {111}, {311}, and {331} planes for each polycrystalline silicon film. Only diffractions from the {220} planes, where present, could be discerned above the noise.

(a) Top view with $\phi = 90°$:



(b) Side view with $\phi > 90°$:

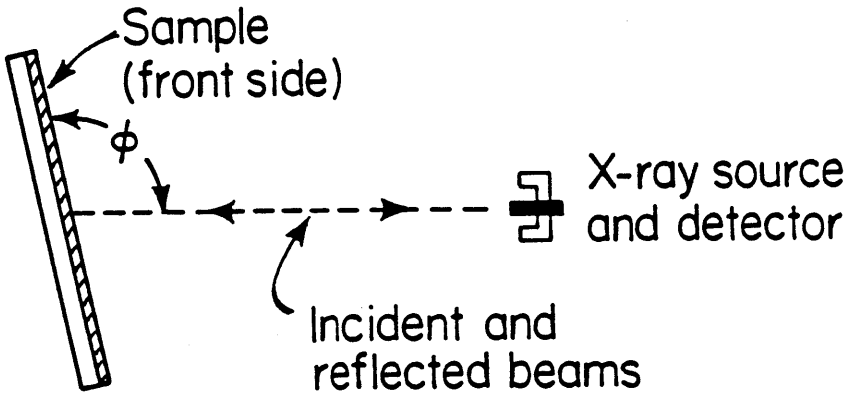


Figure 4 Schematic illustration of the x-ray pole-figure setup.

3.3 Results and Discussion

The TEM micrographs for the 0.35 μm thick films are shown in Figs. 5, 6, and 7 for three representative cases: the as-deposited case, the implanted-annealed case with a dose of 11×10^{14} cm^{-2}, and the implanted-annealed case with a dose of 20×10^{14} cm^{-2}, respectively. For each film, the bright-field and dark-field images were taken over the same film area, and the transmission electron diffraction pattern was taken through a circular aperture over a film area of about 4 μm in diameter. The average grain diameters for these three films can be measured from the bright-field and dark-field images to be 0.080, 1.0, and 2.0 μm, respectively.

The TEM micrographs for the 0.44 μm thick films are shown in Figs. 8, 9, and 10 for three representative cases: the as-deposited case, the implanted-annealed case with a dose of 11×10^{14} cm^{-2}, and the implanted-annealed case with a dose of 16×10^{14} cm^{-2}, respectively. Again, for each film, the bright-field and dark-field images were taken over the same film area, and the transmission electron diffraction pattern was taken through a circular aperture over a film area of about 4 μm in diameter. The average grain diameters for these three films can be measured from the bright-field and dark-field images to be 0.080, 0.70, and 1.4 μm, respectively.

The average grain diameter vs. implant dose curves for the 0.35 μm and 0.44 μm thick films are shown in Figs. 11 and 12, respectively. These curves exhibit two prominant features that are important to our understanding of seed selection through ion channeling. First, the average grain diameter increases with the implant dose initially, but saturates once the implant dose reaches beyond a critical value. Second, the rate at which the average grain diameter increases with the implant dose is not uniform, and the curve consists of three

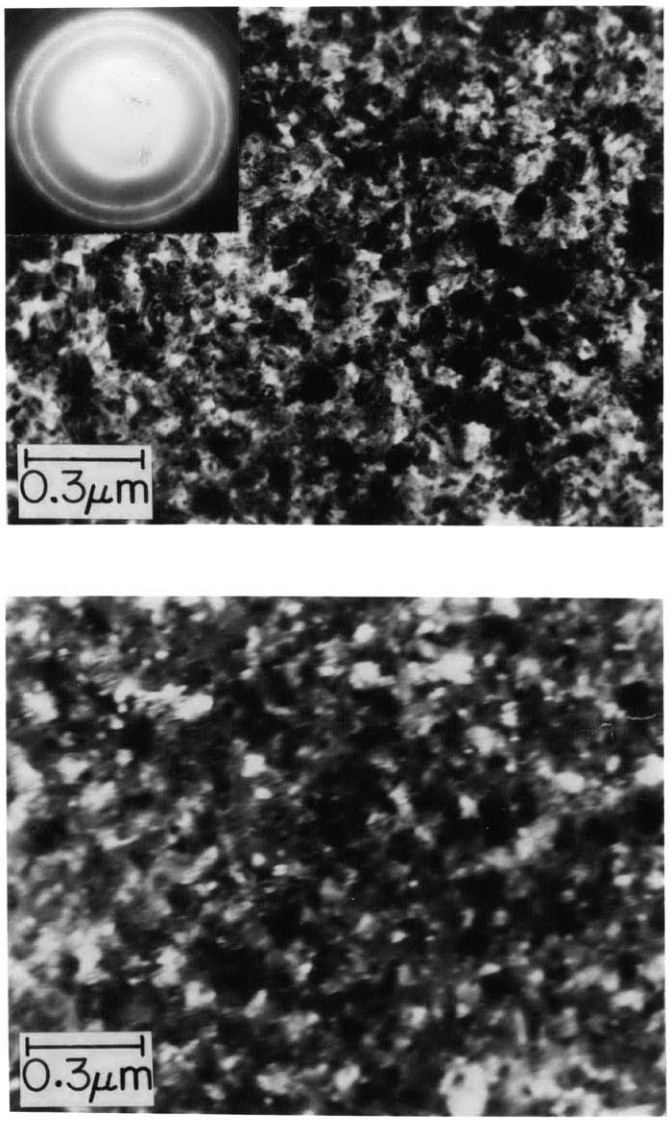


Figure 5 TEM micrographs for the 0.35 μm thick, as-deposited film. The micrographs include the bright-field image (upper), the dark-field image (lower), and the transmission electron diffraction pattern (upper inset).

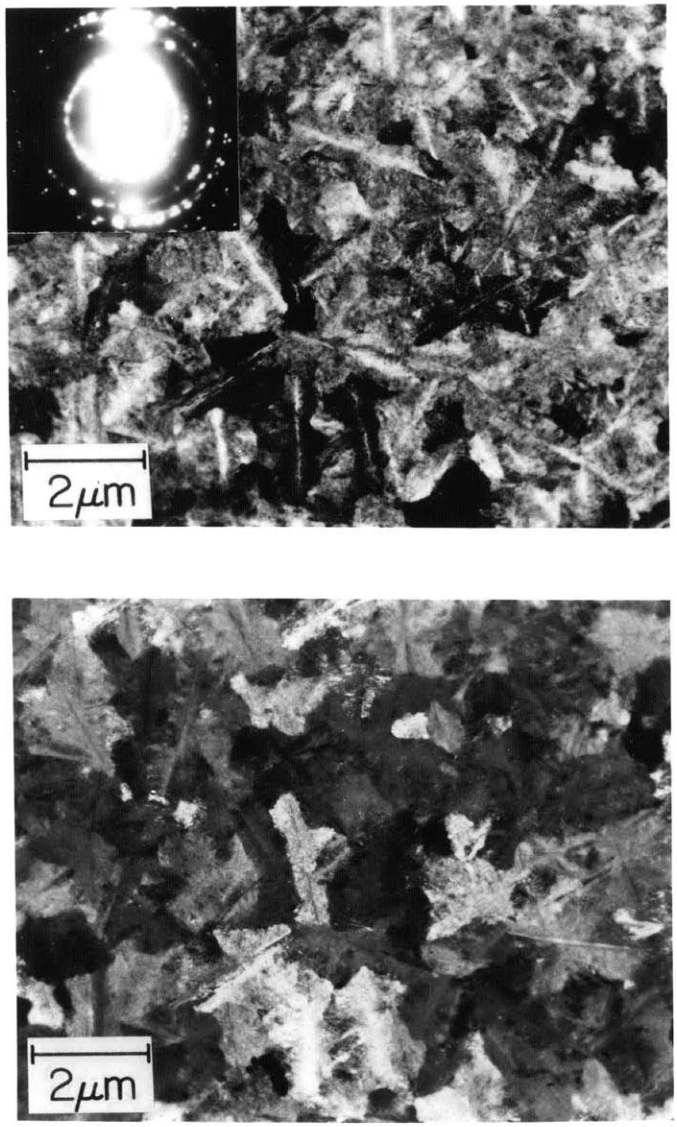


Figure 6 TEM micrographs for the 0.35 μm thick film, after implantation at normal incidence with a dose of 11×10^{14} cm^{-2} and annealing. The micrographs include the bright-field image (upper), the dark-field image (lower), and the transmission electron diffraction pattern (upper inset).

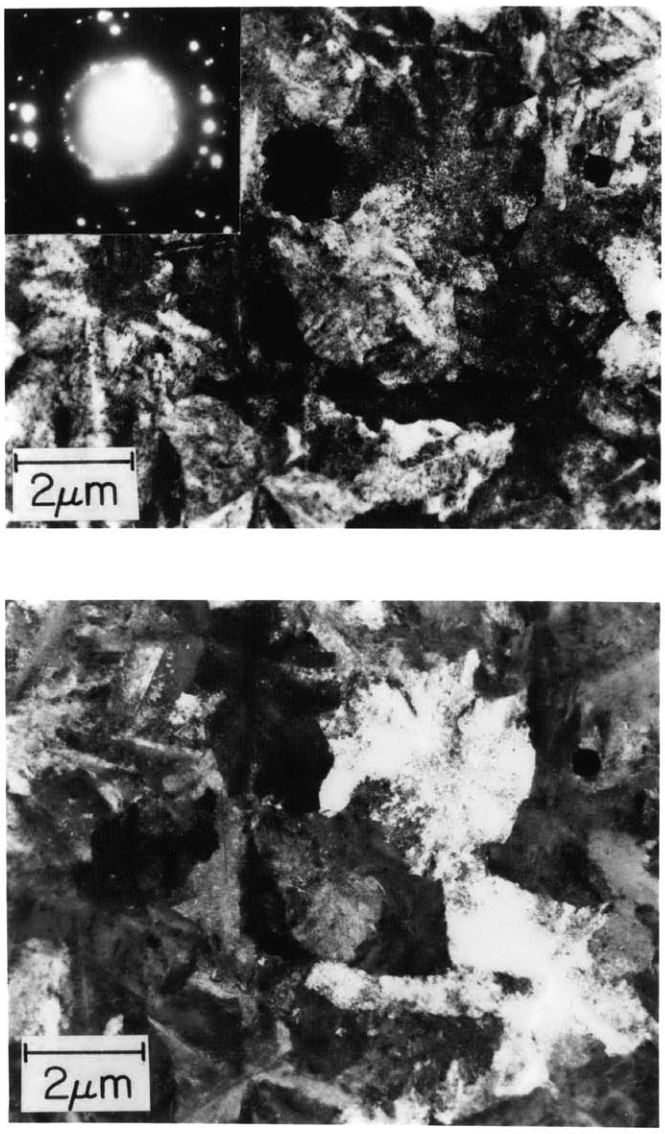


Figure 7 TEM micrographs for the 0.35 μm thick film, after implantation at normal incidence with a dose of 20×10^{14} cm^{-2} and annealing. The micrographs include the bright-field image (upper), the dark-field image (lower), and the transmission electron diffraction pattern (upper inset).

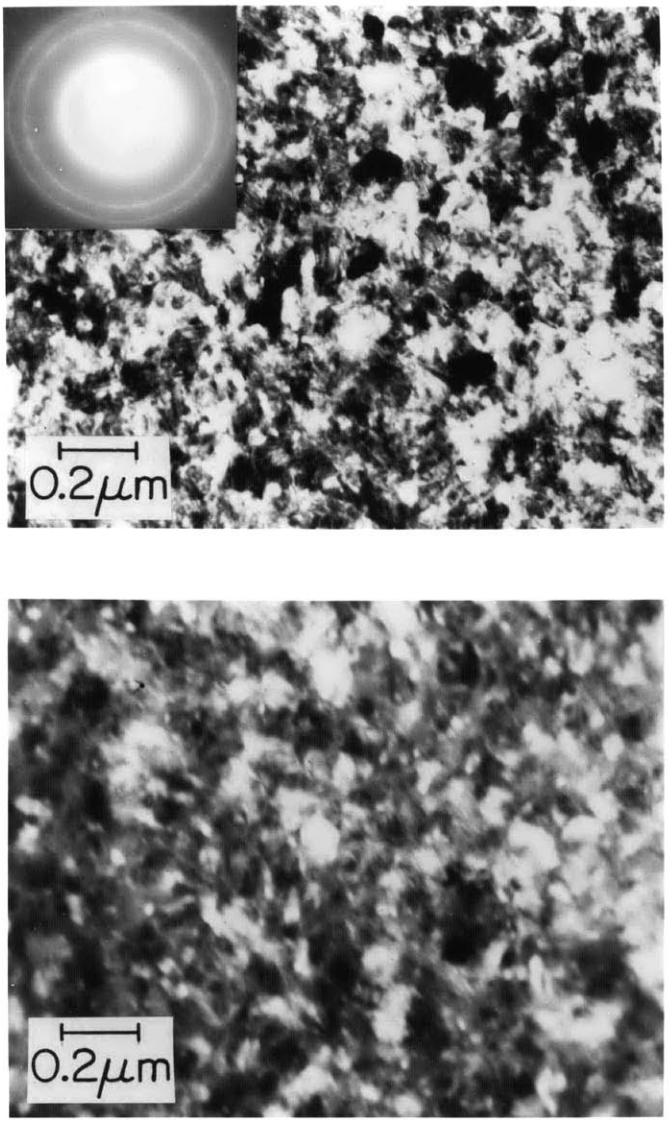


Figure 8 TEM micrographs for the 0.44 μm thick, as-deposited film. The micrographs include the bright-field image (upper), the dark-field image (lower), and the transmission electron diffraction pattern (upper inset).

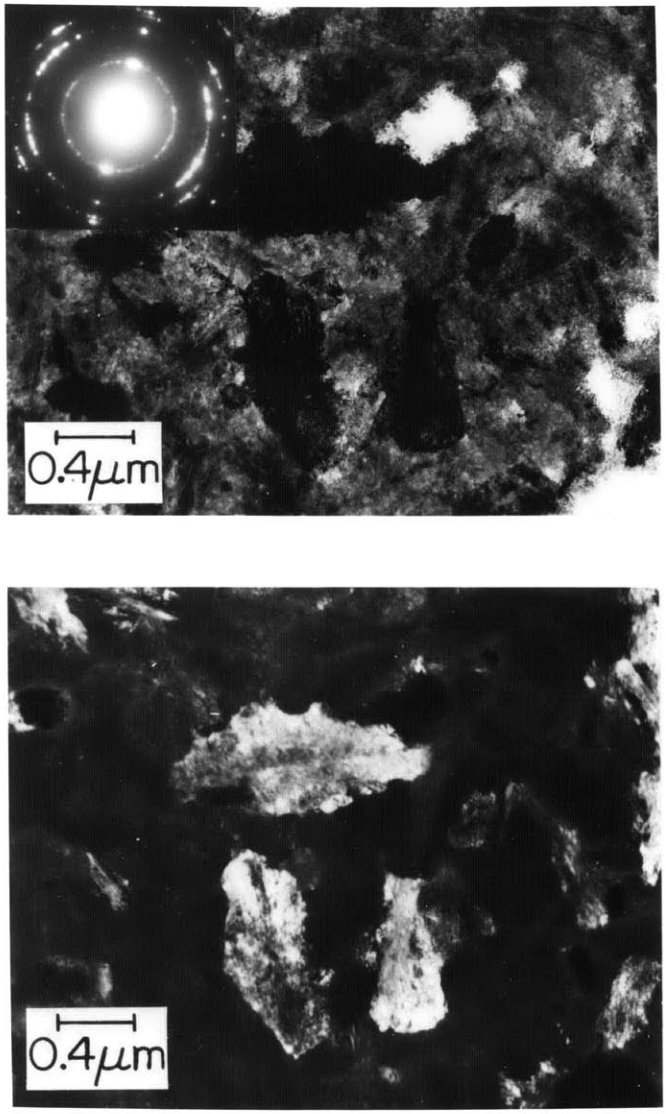


Figure 9 TEM micrographs for the 0.44 μm thick film, after implantation at normal incidence with a dose of 11×10^{14} cm^{-2} and annealing. The micrographs include the bright-field image (upper), the dark-field image (lower), and the transmission electron diffraction pattern (upper inset).

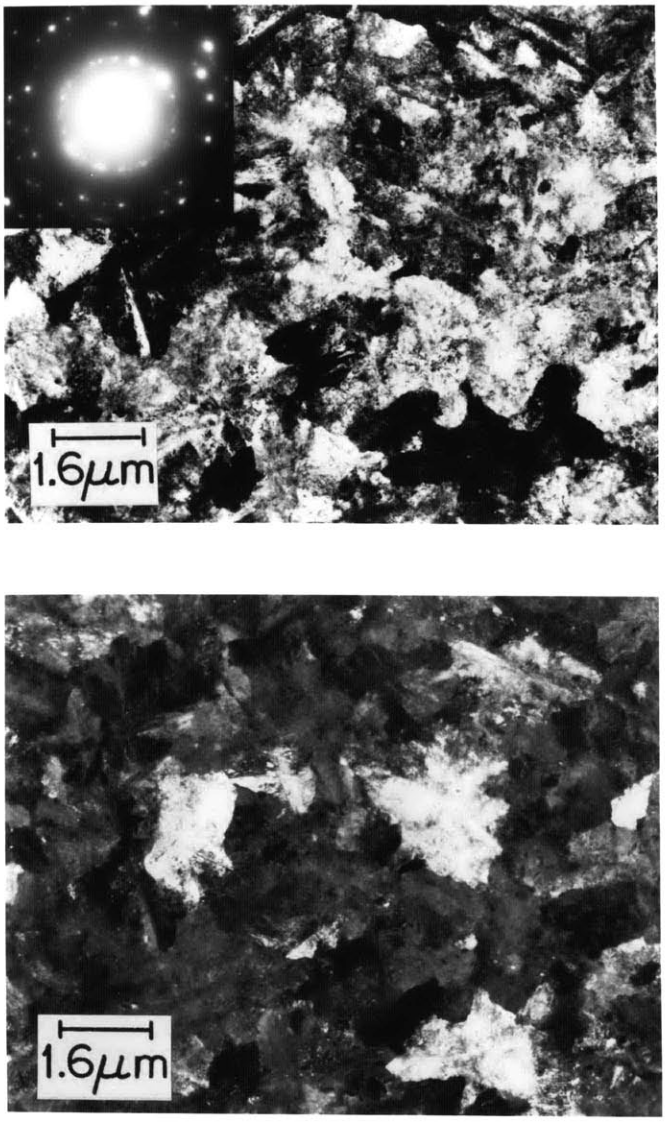


Figure 10 TEM micrographs for the 0.44 μm thick film, after implantation at normal incidence with a dose of 16×10^{14} cm^{-2} and annealing. The micrographs include the bright-field image (upper), the dark-field image (lower), and the transmission electron diffraction pattern (upper inset).

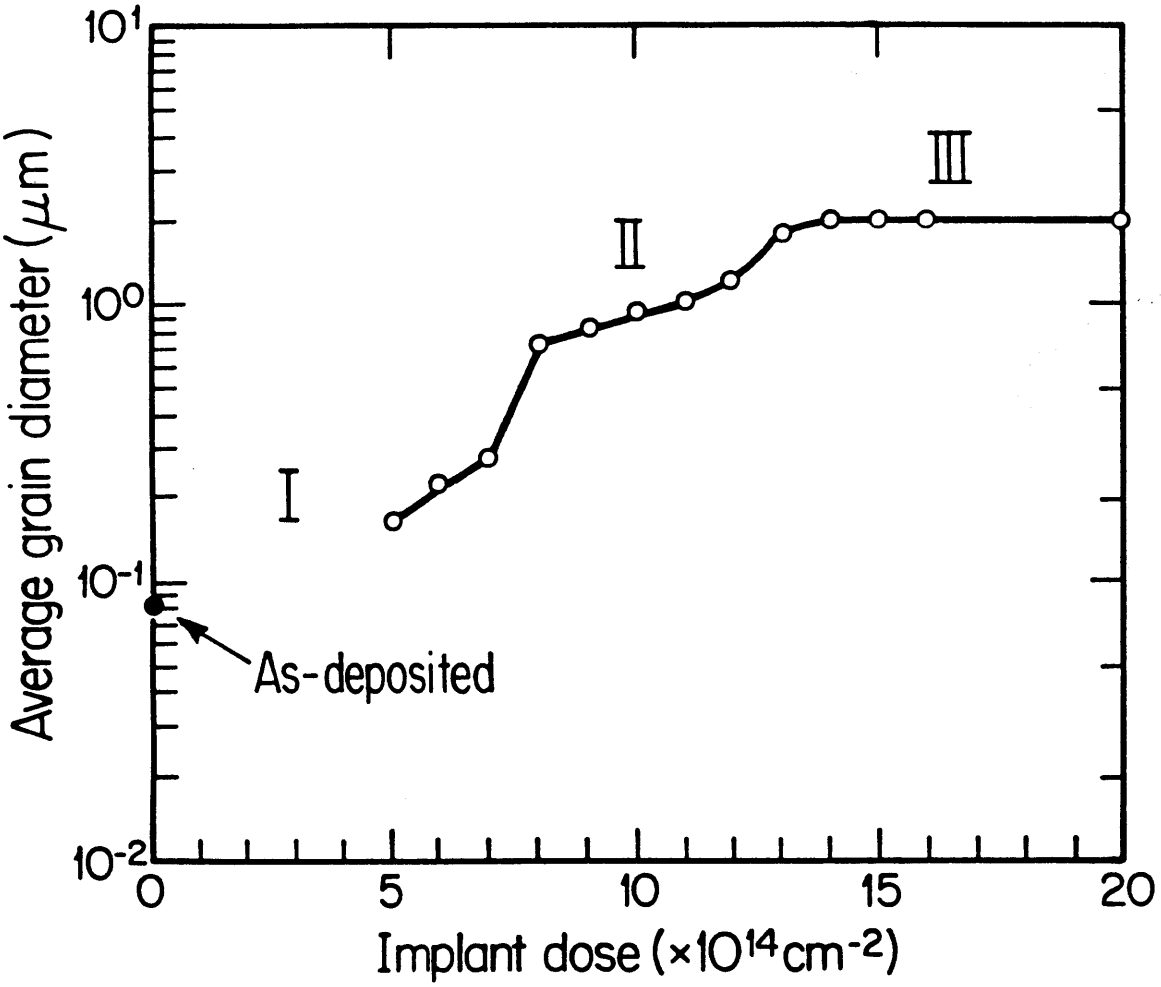


Figure 11 Average grain diameter vs. implant dose for the 0.35 μm thick films, after implantation at normal incidence and annealing.

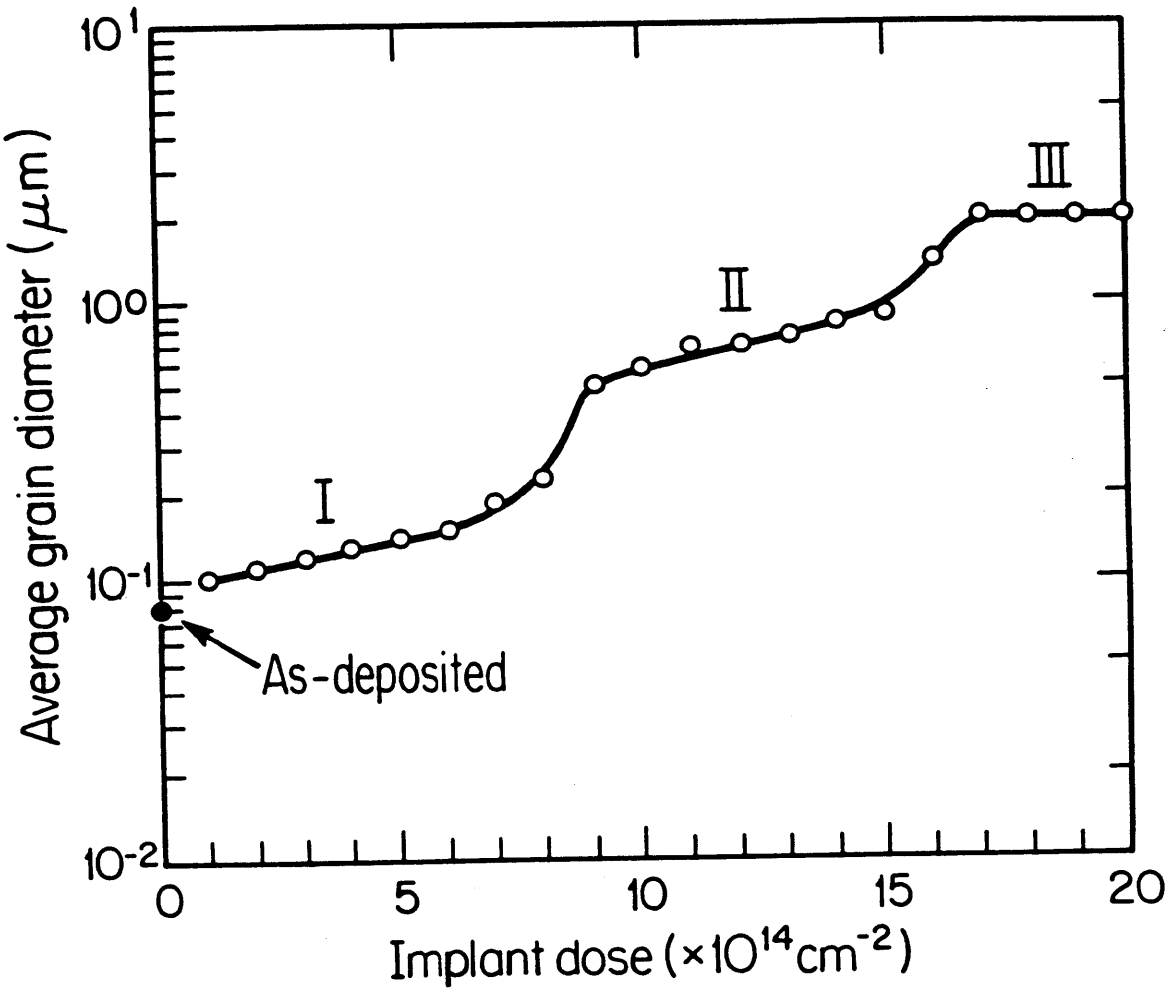


Figure 12 Average grain diameter vs. implant dose for the 0.44 μm thick films, after implantation at normal incidence and annealing.

near-plateau regions that have been labeled as I, II, and III in the figure. Both of these features have been reported in a previous study by Iverson and Reif [11], and can be interpreted on the basis of seed selection through ion channeling. Their interpretation will be presented below, together with that of the x-ray pole-figure results.

The {220} diffracted x-ray intensity vs. ϕ plots for the 0.35 μm and 0.44 μm thick films are shown in Figs. 13 and 14, respectively. For the as-deposited films, Figs. 13(a) and 14(a), the {220} diffracted intensity is weak and is visible only in the range of $\phi = 90° \pm 20°$. This means that the as-deposited films are characterized by a weak {110} texture, with the <110> directions confined to within $\pm 20°$ of the surface normal. For the implanted-annealed films, Figs. 13(b)–(j) and 14(b)–(l), the {220} diffracted intensity increases initially with the implant dose but falls off rapidly to nil after reaching a maximum. The strongest {110} texture occurs at an implant dose of 11×10^{14} cm^{-2}, Figs. 13(h) and 14(h), for both film thicknesses. This strongest {110} texture is characterized by a peak {220} intensity that is almost two orders of magnitude greater than in the as-deposited case, and by an alignment of the <110> directions to within $\pm 4°$ of the surface normal.

The correlations between the grain size and grain orientation are shown in Fig. 15 for the 0.35 μm thick films and Fig. 16 for the 0.44 μm thick films. The upper portion of each figure shows the average grain diameter as a function of the implant dose, *i.e.*, a repeat of Fig. 11 or 12. The lower portion shows the peak value of the {220} diffracted intensity as a function of the implant dose, *i.e.*, a more condensed version of Fig. 13 or 14. Both the upper curve and the lower curve can be divided into three clearly distinguishable regions, as labeled I, II, and III on the curves, at approximately the same dose intervals.

The dependence of the average grain diameter on the implant dose as shown

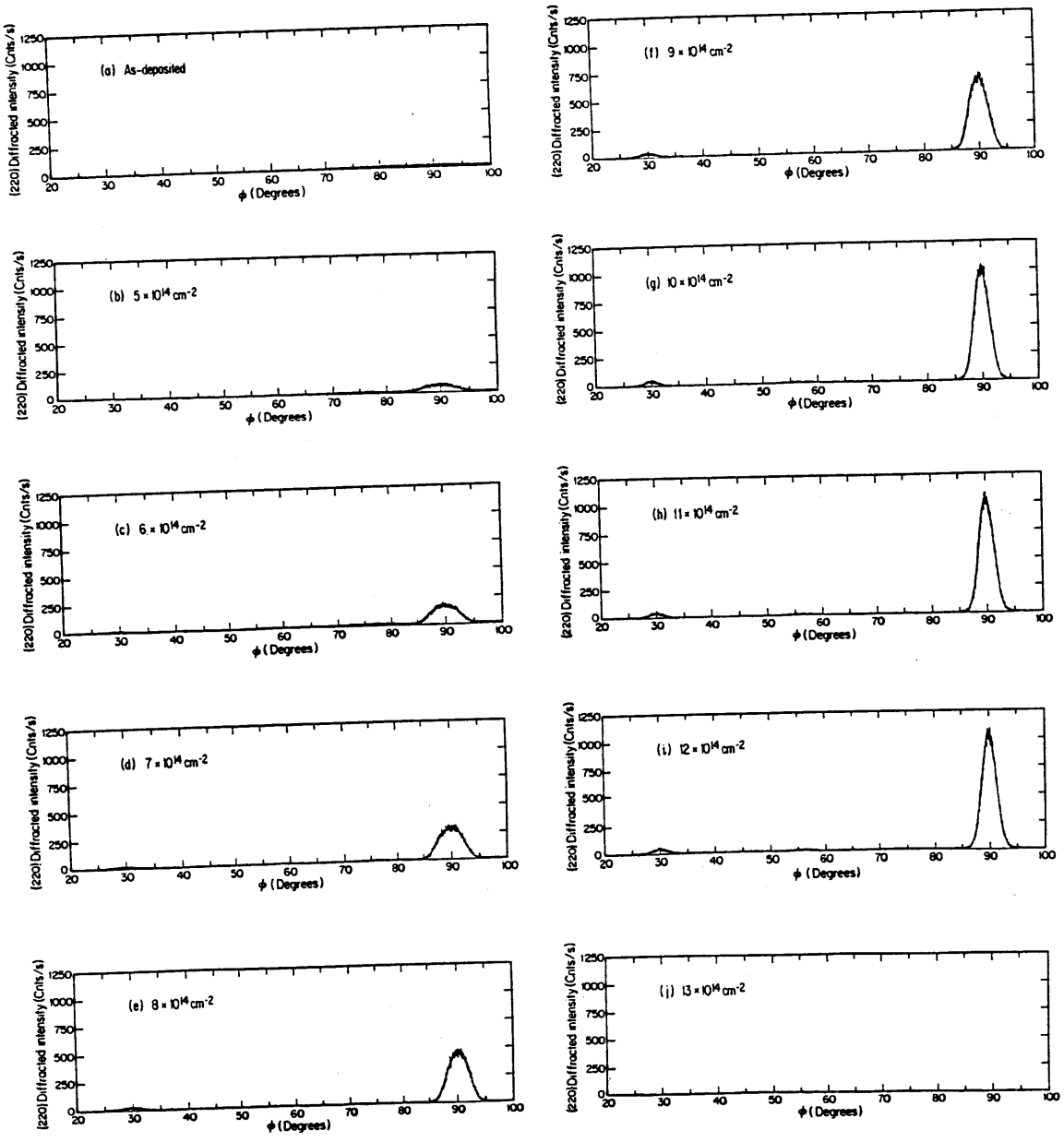


Figure 13 {220} diffracted x-ray intensity vs. ϕ for the 0.35 μm thick films, after implantation at normal incidence and annealing. The implant dose is labeled on each plot.

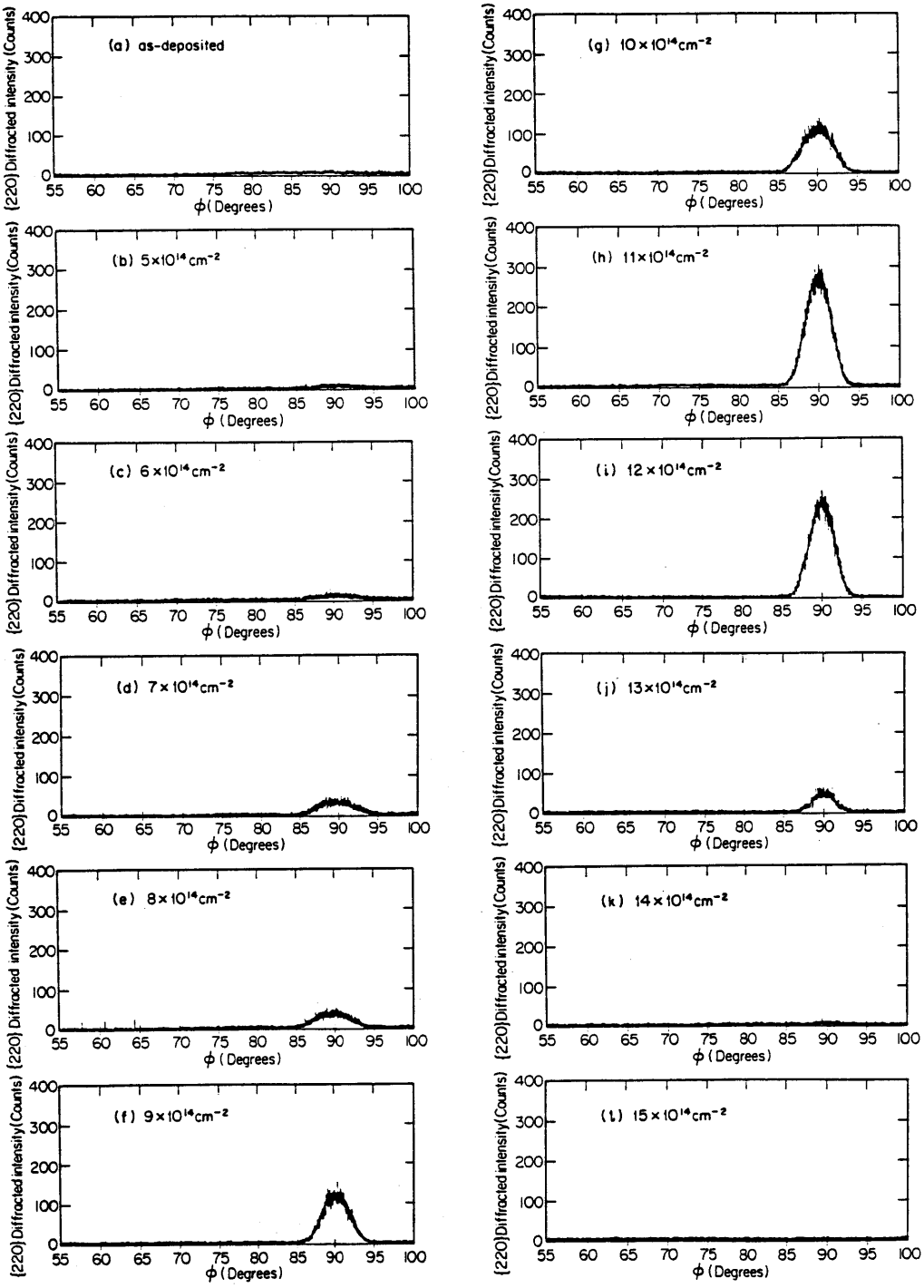


Figure 14 {220} diffracted x-ray intensity vs. ϕ for the 0.44 μm thick films, after implantation at normal incidence and annealing. The implant dose is labeled on each plot.

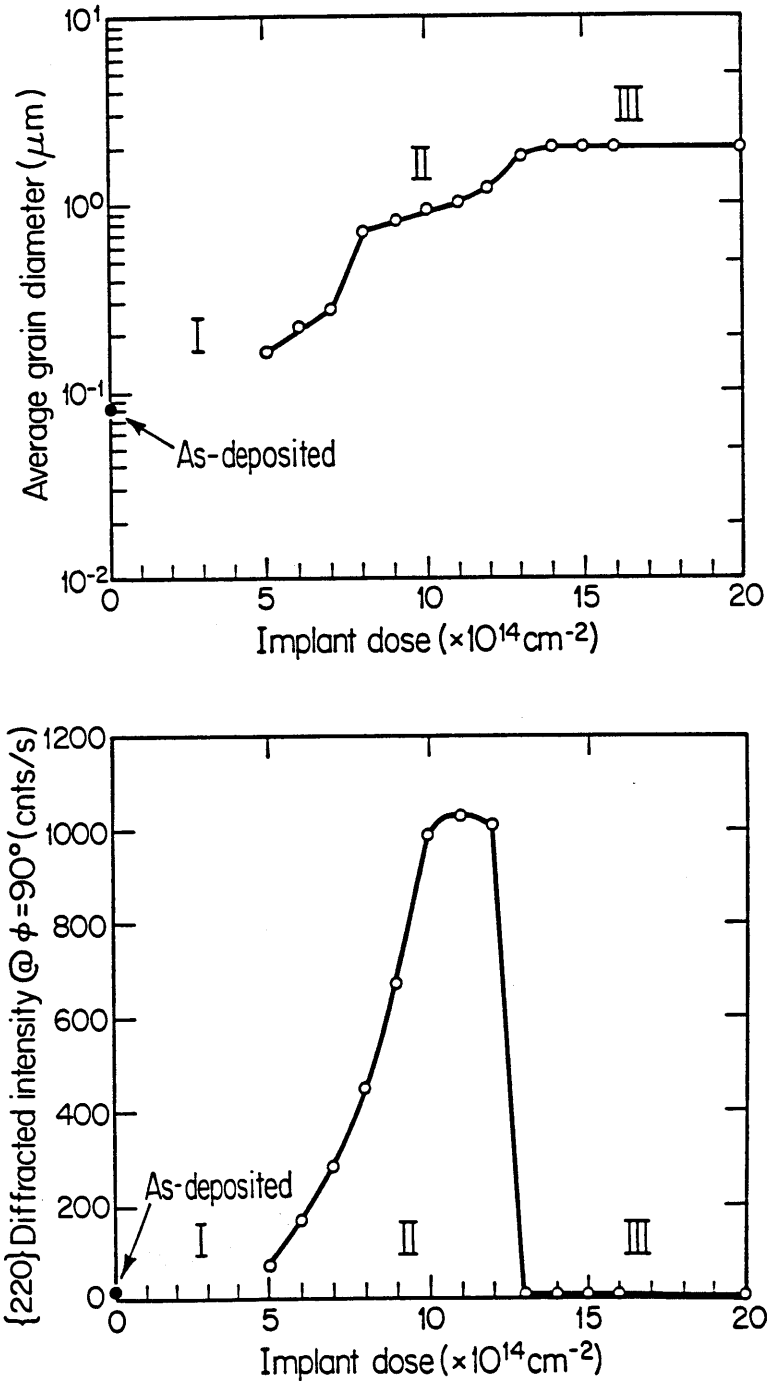


Figure 15 **Correlation between the grain size and grain orientation for the 0.35 μm thick films, after implantation at normal incidence and annealing.**

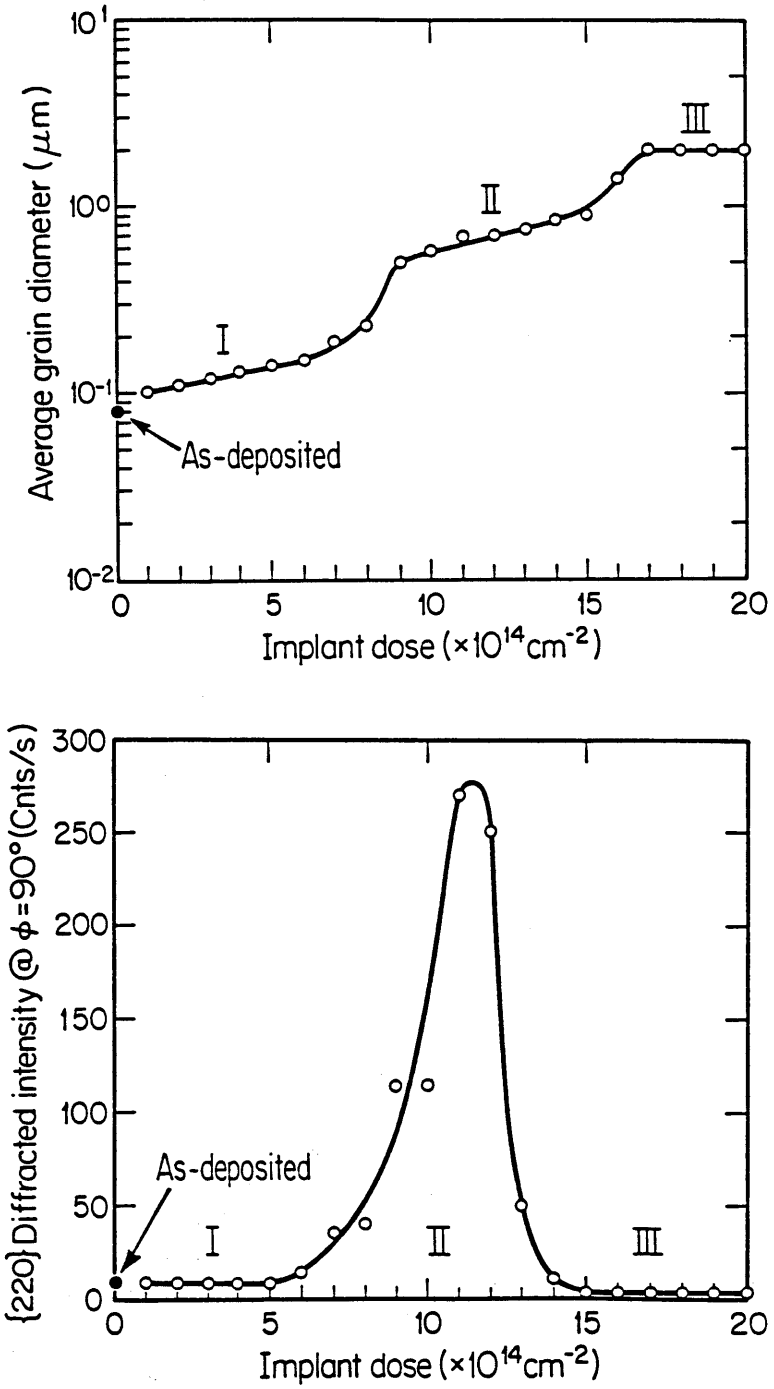


Figure 16 Correlation between the grain size and grain orientation for the 0.44 μm thick films, after implantation at normal incidence and annealing.

in Figs. 11 and 12, the dependence of the {110} fiber texture on the implant dose as shown in Figs. 13 and 14, and the correlation between these two dependences as shown in Figs. 15 and 16, can be interpreted collectively on the basis of seed selection through ion channeling:

(1) At a low implant dose, $\leq 7\times10^{14}$ cm^{-2} for a 0.35 μm and $\leq 8\times10^{14}$ cm^{-2} for a the 0.44 μm thick film, a majority of the crystallites in the film survived the implantation, and seeded the subsequent crystallization. Neither the grain size nor the {110} texture could be changed significantly from the as-deposited case because the original structure of the film was essentially preserved.

(2) At a medium implant dose, 8–12$\times10^{14}$ cm^{-2} for a 0.35 μm and 9–13$\times10^{14}$ cm^{-2} for a 0.44 μm thick film, only a few crystallites in the film, which had <110> directions parallel to the ion beam, survived the implantation due to <110> axial channeling, and seeded the subsequent crystallization. An increased average grain diameter resulted because the film now contained a reduced number of crystallites. This increased average grain diameter was approximately invariant under an increasing implant dose, because the number of remaining crystallites equalled the number of properly oriented crystallites, which was a constant. An enhanced {110} texture also resulted because the film now contained mostly crystallites with <110> directions normal to the substrate.

(3) At a high implant dose, $\geq 13\times10^{14}$ cm^{-2} for a 0.35 μm and $\geq 14\times10^{14}$ cm^{-2} for a 0.44 μm thick film, almost no crystallites survived the implantation, and the crystallization was dominated by the nucleation-induced growth rather than the seeded growth. The average grain diameter became independent of the implant dose because every implanted film now had the same, completely amorphized structure. Also, no crystallographic texture could be observed because every crystallized film contained only nucleated crystallites, which had random orientations.

The ion implantation step was the crux of the seed selection through ion channeling process: it would have been difficult, if not impossible, to alter the structure of an as-deposited polycrystalline silicon film using the low-temperature annealing step alone [14]. To confirm this, we have annealed some of the as-deposited films together with the as-implanted films, and have then investigated their structures via TEM and x-ray pole-figure analyses. As the results showed, the average grain sizes and crystallographic textures of these annealed (but unimplanted) films were indeed identical to those of the as-deposited films.

The outcome of this experiment is an optimized seed selection through ion channeling process for growing {110}-fiber-textured polycrystalline silicon films. The focus of the next experiment should be on how to restrict the {110} fiber texture. This can be achieved through further implant-anneal treatments, with the implantations directed at different channeling angles. Listed below are some alternative approaches deserving consideration:

(1) A second implant at 45° from normal incidence to select the <100> axis or the equivalent <010> axis of a {110} grain, and a subsequent anneal; or

(2) A second implant at 35.26° from normal incidence to select the <111> axis or the equivalent $<11\bar{1}>$ axis of a {110} grain, and a subsequent anneal; or

(3) A second implant at 60° from normal incidence plus a third implant at the same angle but after rotating the sample by 60°, to select the <101> and <011> axes or the equivalent $<10\bar{1}>$ and $<01\bar{1}>$ axes of a {110} grain, with an anneal following each implant.

The same optimization scheme, by optimizing the implant dose, can be employed. The power of this optimization scheme has been well demonstrated in this experiment.

3.4 Conclusion

We have proposed a systematic approach to optimize the seed selection through ion channeling process for growing restricted-fiber-textured polycrystalline silicon films. We have also demonstrated the effectiveness of this approach by optimizing a basic process for growing {110}-fiber-textured polycrystalline silicon films. This basic process consists of a single implantation step followed by a single annealing step. Its optimization is important, because it resembles each of the implant-anneal treatments of an overall process that incorporates multiple-angle implantations.

The optimization of this basic process was achieved by optimizing the implant dose while keeping all other process parameters constant. The average grain diameter increased initially with the implant dose, but saturated at a maximum of 2 μm once the implant dose increased beyond the critical-amorphization value. The {110} fiber texture increased initially with the implant dose, but fell off rapidly to nil after reaching a maximum at a dose of 11×10^{14} cm^{-2}. At this "optimal" implant dose, the peak value of the {220} diffracted x-ray intensity was almost two orders of magnitude greater than in the as-deposited case, and the <110> directions were confined to within $\pm4°$ of the surface normal. The overall results lend strong support to the potential of seed selection through ion channeling in growing restricted-fiber-textured polycrystalline silicon films.

CHAPTER 4

IMPLANT-DOSE DEPENDENCE OF SSIC: 60° IMPLANT ANGLE

4.1 Introduction

This chapter describes our attempt at growing restricted-fiber-textured polycrystalline silicon films via seed selection through ion channeling. We have demonstrated in Chapter 3 the feasibility of growing {110}-fiber-textured polycrystalline silicon films. We have also suggested the potential of *restricting* the {110} fiber texture through further implant-anneal treatment(s) at different channeling angle(s). We now try to verify this potential by optimizing a single-implant, single-anneal seed selection through ion channeling process in which the implantation is directed at 60° from normal incidence. The same optimization scheme, that is, by optimizing the implant dose, will be used. The power of this optimization scheme has been well demonstrated in the previous experiment.

4.2 Experimental Procedure

Starting with 2", lightly doped, <100> silicon wafers, a 0.1 μm thick SiO_2 layer was thermally grown at 1100°C in dry O_2.

Polycrystalline silicon films, 0.35 μm thick, were then deposited onto these oxidized wafers via the low-pressure chemical-vapor deposition technique, using the same deposition parameters as in Chapter 3. These films were subsequently divided into two batches: the "as-deposited" batch and the "11×10^{14} cm^{-2}"

batch. Before any further processing, the 11×10^{14} cm^{-2} batch of films were self-implanted at normal incidence, at a temperature of 77°K, with an accelerating voltage of 200 keV, and with a dose of 11×10^{14} cm^{-2}, and were subsequently annealed at 600°C for 48 h in N_2. Based on the results of Chapter 3, the as-deposited batch of films are characterized by a weak and dispersed {110} fiber texture, and the 11×10^{14} cm^{-2} batch of films by a strong and focused {110} fiber texture.

Both batches of polycrystalline silicon films were then selectively amorphized via self-implantation. The implantation parameters have been chosen through the same procedure as outlined in Chapter 3. The implant was performed at 60° from normal incidence, to select the equivalent <101>, <011>, $< 10\bar{1} >$, or $< 01\bar{1} >$ axis of a {110} grain. The implant was performed, also, at a low temperature of 77°K, to improve the selectivity of this amorphization step: a low implant temperature would enhance the channeling phenomenon in properly oriented crystallites by reducing thermal vibrations of the crystal lattice [18], and would reduce the dynamic annealing phenomenon in the mis-oriented crystallites [19,20]. For the purpose of calculating the damage energy density profile, implanting a 0.35 μm thick film at 60° from normal incidence is equivalent to implanting a 0.70 μm thick film at normal incidence. Since the latter case is much easier to visualize, we have chosen the energy and doses using terminologies assuming that the implantation were to be performed, instead, on a 0.70 μm thick film at normal incidence. The implant energy, 320 keV, was chosen to position the peak of the damage energy density profile to slightly beyond one half of the film's depth. The implant doses, $9\text{–}25\times10^{14}$ cm^{-2}, were chosen to yield damage energy densities in the vicinity of 6×10^{23} eV/cm^3, the amount needed for the critical amorphization of monocrystalline silicon [19,20]. The damage energy density profile has been calculated using the extended Brice

model [21], and is shown in Fig. 17. The implant dose was the only varying parameter in the entire seed selection through ion channeling process; it was the parameter to be optimized in this experiment.

The implanted silicon films were then crystallized via annealing in a conventional, atmospheric-pressure furnace. The annealing parameters (600°C, 48 h, N_2) were the same as in Chapter 3.

The crystallographic texture of the polycrystalline silicon film was determined via the x-ray pole-figure analysis. The analysis was performed using the same equipment as in Chapter 3. We have checked for diffractions from the {220}, {111}, {311}, and {331} planes for each polycrystalline silicon film. Only diffractions from the {220} planes, where present, could be discerned above the noise.

4.3 Results and Discussion

The {220} diffracted x-ray intensity vs. ϕ plots for the as-deposited batch of polycrystalline silicon films are shown in Fig. 18. The {220} diffracted intensity at $\phi = 90°$ increased initially with the implant dose, but decreased gradually to the "randomly oriented" level as the implant dose increased beyond 14×10^{14} cm^{-2}. The {220} diffracted intensity at $\phi = 30°$, however, remained at the "randomly oriented" level for the entire range of implant doses used. Both the intensity at $\phi = 90°$ and the intensity at $\phi = 30°$ remained constant as the sample was rotated by 360° with respect to the surface normal. These observations indicate that the 60° implant-anneal treatment has generated a somewhat enhanced {110} fiber texture at low implant doses, but has not generated the anticipated, preferential in-plane orientation.

The {220} diffracted x-ray intensity vs. ϕ plots for the 11×10^{14} cm^{-2} batch

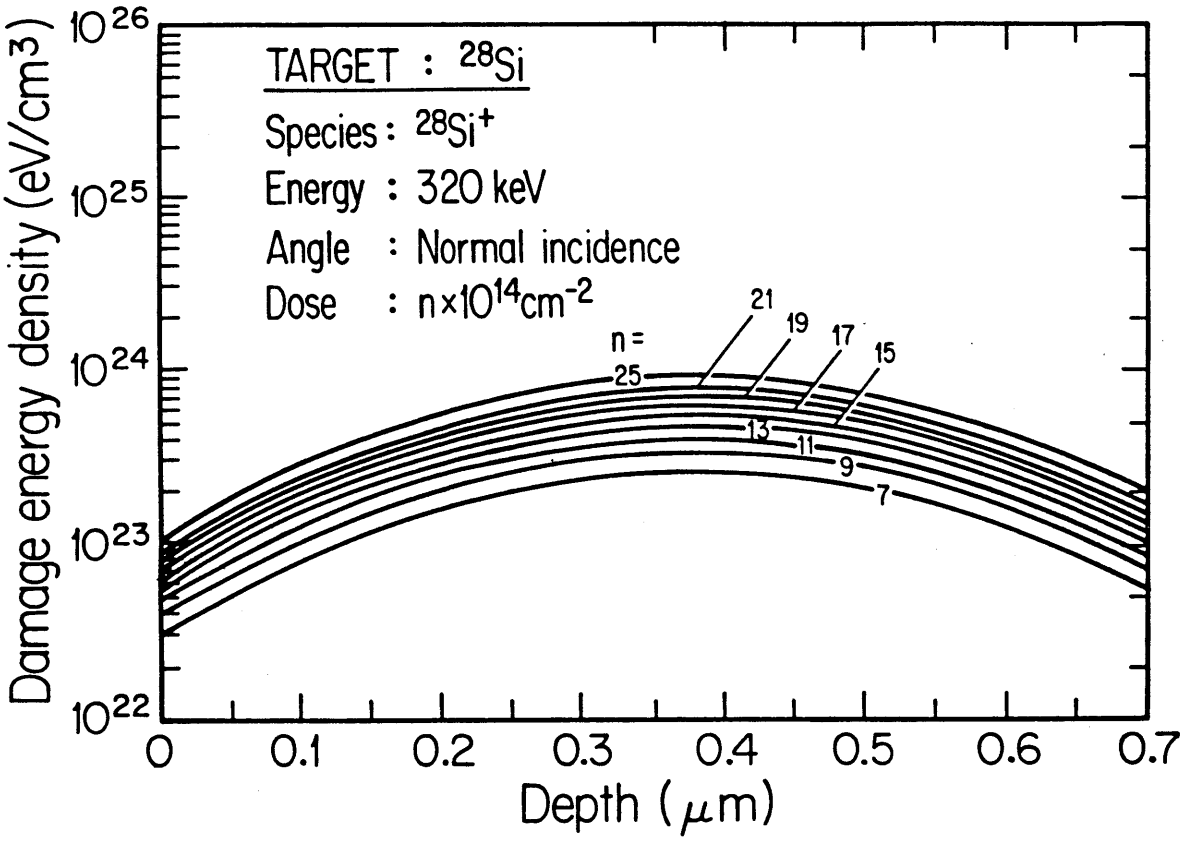


Figure 17 Theoretical damage energy density profile for a 320 keV silicon self-implant, shown for different doses. The profile has been calculated using the extended Brice model [21].

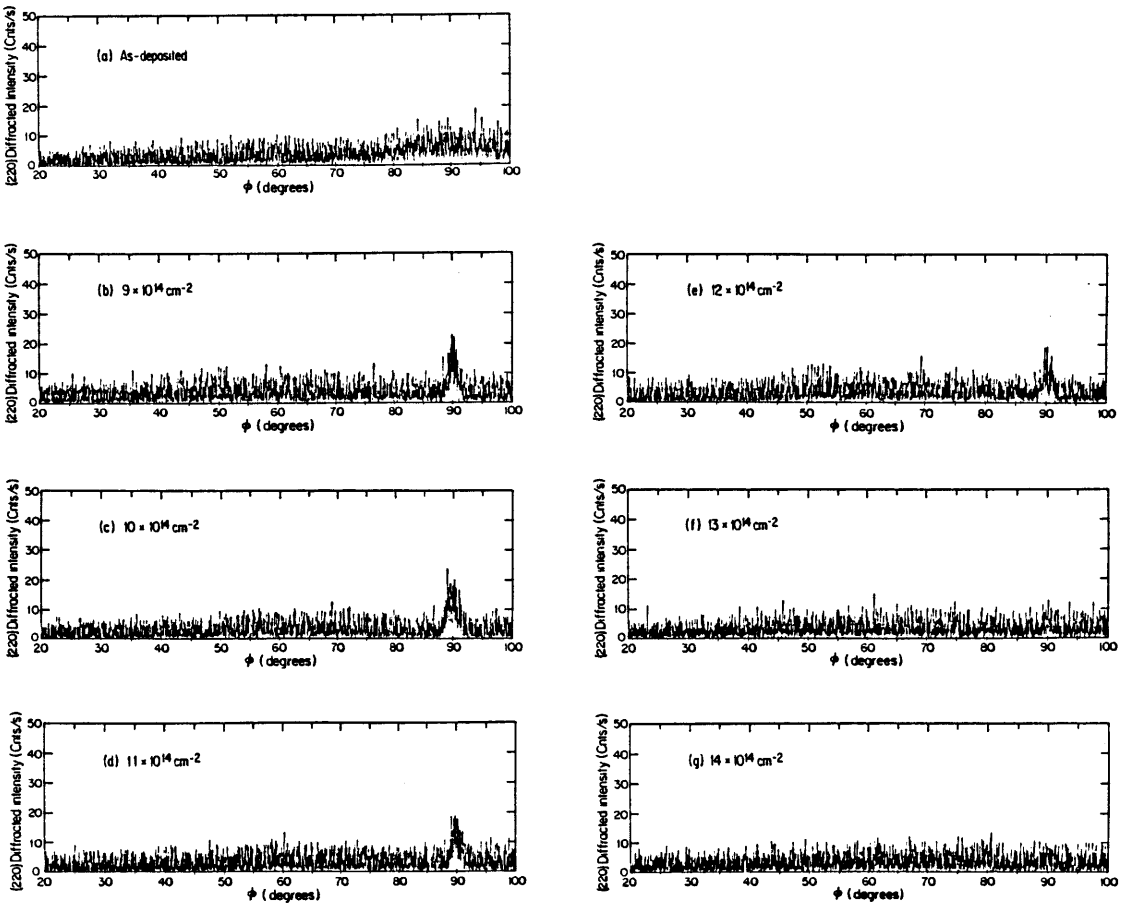


Figure 18 {220} diffracted x-ray intensity vs. ϕ for the 0.35 μm thick films, after implantation at 60° from normal incidence and annealing. The implant dose is labeled on each plot.

of polycrystalline silicon films are shown in Fig. 19. Both the {220} diffracted intensity at $\phi = 90°$ and the {220} diffracted intensity at $\phi = 30°$ increased initially with the implant dose, but decreased gradually to the "randomly oriented" level as the implant dose increased beyond 19×10^{14} cm^{-2}. Both of them reamined constant as the sample was rotated by 360° with respect to the surface normal. These observations, again, indicate that the 60° implant-anneal treatment has generated a somewhat enhanced {110} fiber texture at low implant doses, but has not generated the expected, *restricted* {110} fiber texture.

The results as shown in Figs. 18 and 19 indicate the presence of the seed selection through ion channeling process, despite its failure to restrict the {110} fiber texture. As shown in both figures, the {220} diffracted intensity at $\phi = 90°$ increased initially with the implant dose, and this was due clearly to the seed selection through ion channeling process. On the other hand, the {220} diffracted intensity at $\phi = 30°$ remained constant with the azimuthal angle of rotation, and this simply indicated the insufficiency of a single implant-anneal treatment in restricting the {110} fiber texture. The simple optimization scheme we have employed so far, which centers on fine-tuning the implant dose of a single implant-anneal treatment, works well in optimizing the {110} fiber texture. To restrict the {110} fiber texture a more sophisticated optimization scheme will be required.

One possible approach is to employ, instead, a sequence of implant-anneal treatments to achieve what we have intended via only one implant-anneal treatment. Each treatment in the sequence will have the same implantation and annealing schedules; that is, each treatment will have the same implant angle (*i.e.*, at 60° from normal incidence), the same optimal implant dose (*i.e.*, at about 10×10^{14} cm^{-2} as shown in Figs. 18 and 19), and so forth. The fiber texture will be restricted step by step through each treatment, and the restricted

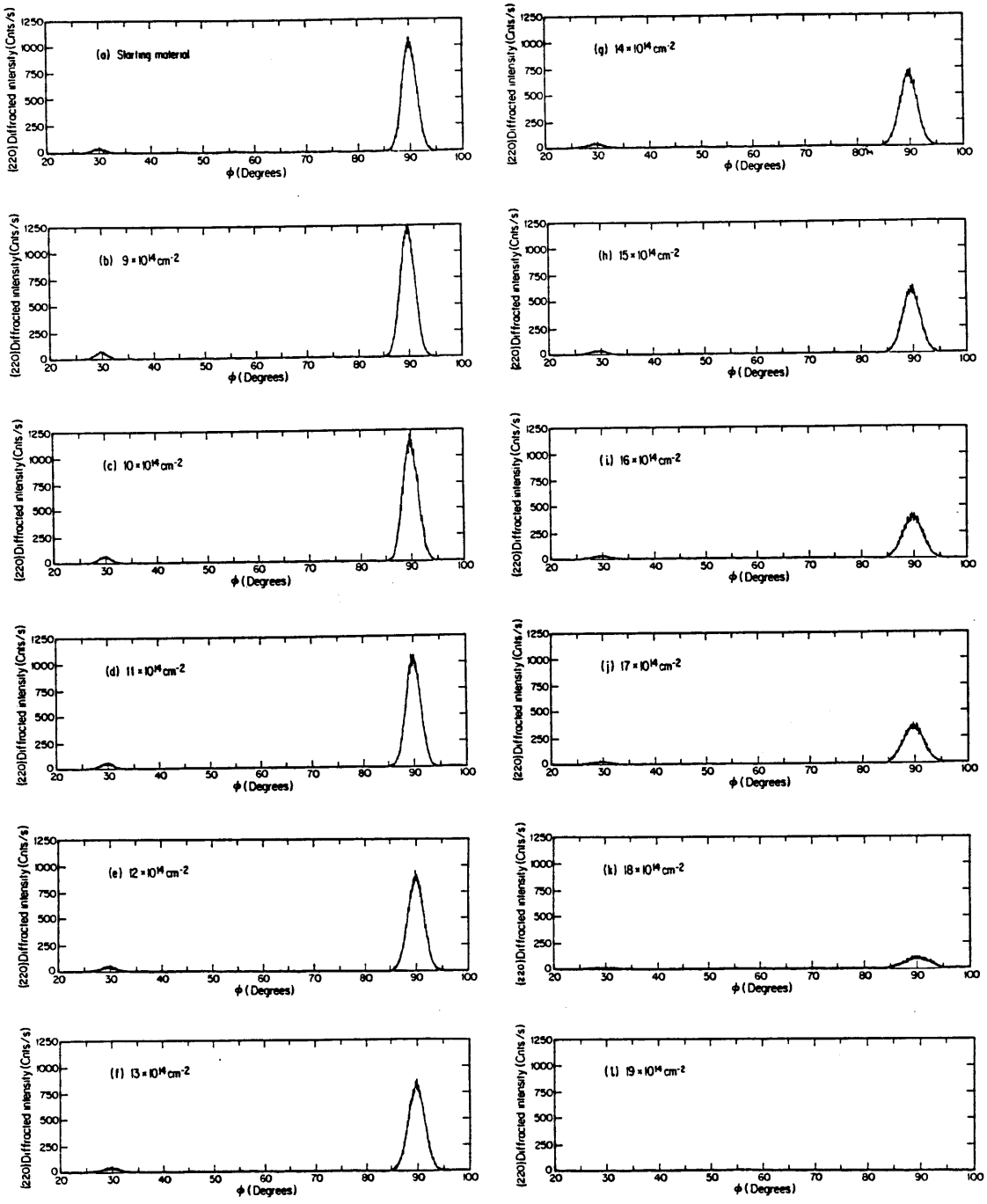


Figure 19 {220} diffracted x-ray intensity vs. ϕ for the 0.35 μm thick films, after a second implantation at 60° from normal incidence and annealing. The implant dose is labeled on each plot.

fiber texture will be realized at the end of the sequence.

This new approach, however, requires a more sophisticated implantation-annealing equipment which is not yet available in our facility. This new equipment should allow the entire sequence of implant-anneal treatments to be performed without ever unloading the sample from the target holder. Our existing equipment requires that the sample be unloaded from the target holder after each implantation for annealing in a separate furnace. The sample then must be remounted onto the target holder for the second implantation, and an error is introduced into the implant angle since it is impossible to remount the sample onto exactly the same position and orientation as before. This error is inevitable and is much greater than what the seed selection through ion channeling process can tolerate [13]. Consequently, we have never tried to use this approach for the growth of restricted-fiber-textured films, and we will not do so until the new implantation-annealing equipment becomes available.

4.4 Conclusion

We have attempted the growth of restricted-fiber-textured polycrystalline silicon films via the seed selection through ion channeling process, using the same optimization scheme as proposed and demonstrated in Chapter 3. The as-deposited batch and the 11×10^{14} cm^{-2} batch of polycrystalline silicon films were self-implanted at 60° from normal incidence, with varying doses, and were subsequently crystallized at 600°C. The results obtained through the x-ray pole-figure analysis indicate the presence of the seed selection through ion channeling process, despite its failure to restrict the {110} fiber texture.

We have subsequently proposed a modified optimizing scheme for growing the restricted-fiber-textured polycrystalline silicon films. This new approach will

employ, instead, a sequence of implant-anneal treatments to achieve what we have intended with only one implant-anneal treatment. This new approach will require a more sophisticated equipment, one that will allow the entire sequence of implant-anneal treatments to be performed without ever unloading the sample from the target holder. The success of our research in seed selection through ion channeling will depend critically on the availability of this equipment.

PART II

THIN-FILM TRANSISTORS (TFT'S)

CHAPTER 5

BACKGROUND ON TFT RESEARCH

5.1 Applications in Large-Area Electronics

Large-area electronic systems are sometimes referred to as image information systems, because they serve the primary purpose of handling image information. The system may consist of an *image sensor*, which converts analog images into digital information, and/or an *image displayer*, which converts electronic information into analog images.

Each image sensor or displayer, in turn, is composed of a driver circuit and a logic circuit:

(1) The driver circuit consists of the individual sensing or displaying elements spatially arranged in an array or matrix. The fabrication of a driver circuit faces the *uniformity* and *temperature* constraints discussed in Chapter 1: it must be fabricated with uniform characteristics over the entire system area, and it must be fabricated at low temperatures to prevent any deformation of the transparent glass substrate.

(2) The logic circuit consists of a raster scanner and other resolution-enhancement functions. Present technology requires that the logic circuit be formed separately from the driver matrix and then interfaced to the matrix through a large number of column and row connections. The future technology should allow the monolithic integration of the logic and driver circuits to minimize the number of connections coming in and out of the glass plate. The design and fabrication of such a logic circuit will face the *speed* and *temperature* constraints: it must

be able to operate at a sufficiently high speed, and it must be fabricated at low temperatures to prevent any deformation of the transparent glass substrate.

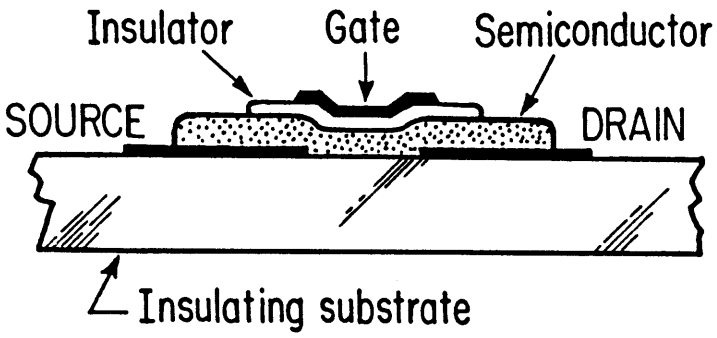
The fabrication of quality thin-film transistors on transparent glass substrates has been one of the greatest technical challenges facing the field of large-area electronics. Since the late 1960's, thin-film transistors have been investigated using a variety of semiconductor materials and fabrication techniques [23]. The most promising results have been obtained on three semiconductor materials, including cadmium selenide (CdSe), hydrogenated amorphous silicon (a-Si:H), and polycrystalline silicon. The next section summarizes these results.

5.2 Overview of Previous Research

Cadmium selenide thin-film transistors have been the focus of TFT research during the late 1960's and early 1970's. The reports of Weimer *et al.* [24] and Brody *et al.* [25] are the most representative of these efforts. Most of the CdSe TFT's reported to date have structures similar to those shown in Fig. 20. Such structures are generally formed via successive, masked depositions, and each can be inverted by reversing the deposition sequence. The major advantage of CdSe TFT's is the high value of their field-effect charge-carrier mobilities, typically around 100 $cm^2/V{\cdot}s$. The major disadvantage, however, is the non-uniformity of their leakage currents over large areas. At present, CdSe TFT's account for approximately 10% of the total number used in commercial systems.

Hydrogenated amorphous silicon thin-film transistors have been the focus of TFT research since the early 1970's. The reports of Neudeck and Malhotra [26], Snell *et al.* [27], Matsumura and Hayama [28], and Thompson and Tuan [29] are the most representative of these efforts. Most of the a-Si:H TFT's reported to date have structures similar to those shown in Fig. 20. Such structures are gen-

(a) With staggered electrodes:



(b) With coplanar electrodes:

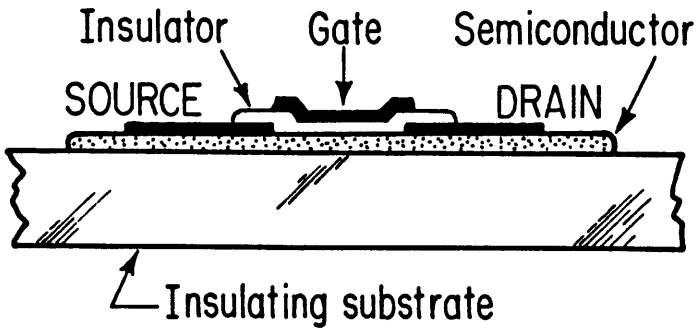


Figure 20 Schematic illustration of the two conventional TFT structures. Each structure can be inverted by deposition in the reverse sequence. (From ref. 24.)

erally formed via successive depositions and photolithography, and each can be inverted by reversing the deposition sequence. The advantage of a-Si:H TFT's is the uniformity of their leakage currents over large areas. The disadvantage, however, is the low value of their field-effect charge-carrier mobilities, typically around 1 $cm^2/V{\cdot}s$. At present, a-Si:H TFT's account for approximately 90% of the total number used in commercial systems.

Polycrystalline silicon thin-film transistors have attracted considerable attention since the late 1970's [1]. Most of the polycrystalline silicon TFT's reported to date have structures similar to either those shown in Fig. 20 or that of a standard MOSFET [5]. Such structures are generally formed by successive depositions/growths and photolithography, and each can be inverted by reversing the deposition/growth sequence. The characteristics of polycrystalline silicon TFT's fall in-between those of the CdSe TFT's and those of the a-Si:H TFT's: they have reasonably high field-effect charge-carrier mobilities, ranging from 10 to 100 $cm^2/V{\cdot}s$, and reasonably uniform leakage currents over large areas. At present, polycrystalline silicon TFT's account for no more than a small fraction of the total number used in commercial systems, but their importance is expected to grow rapidly in the future.

So far, regardless of the market share, none of these three existing technologies has emerged as the clear technological leader, and each offers advantages as well as disadvantages. In the short run, a hybrid of these technologies may be required to overcome the various constraints in building a large-area system. For instance, a flat-panel liquid-crystal display may have to employ an a-Si:H driver matrix to satisfy the uniformity constraint and a polycrystalline silicon logic circuit to satisfy the speed constraint. In the long run, polycrystalline silicon thin-film transistors will most likely dominate.

Finally, in addition to the experimental work, the modeling of thin-film tran-

sistors have also received considerable attention during the last decade. Most of the models published during this time period have been developed to describe the operations of polycrystalline silicon MOS TFT's. Some of these models, as well as their relations to our work, are summarized in Appendix B.

5.3 Overview of Present Research

To develop seed selection through ion channeling into a viable silicon-on-insulator technology a comprehensive program is required, in which the materials process must be optimized and the device worthiness demonstrated. Part I of this thesis is devoted to the materials work, and Part II to the device work.

We have fabricated MOS thin-film transistors on the as-deposited film and an amorphized-crystallized film to investigate the effects of an enhanced average grain size on TFT performance [30]. The fabrication has been carried out using a non-self-aligned, aluminum-gate process, which has a maximum temperature of 600°C and is compatible with the current generation of commercial glass substrates. The results demonstrate that an enhanced average grain size can improve both the threshold voltages and field-effect mobilities of these polycrystalline silicon TFT's. A detailed discussion of this work is given in Chapter 6.

We have also fabricated MOS thin-film transistors on the as-deposited film and two implanted-annealed films to investigate the effects of an enhanced average grain size and/or an enhanced {110} texture on TFT performance [31]. The fabrication has been carried out using a self-aligned, silicon-gate process, which has a maximum temperature of 800°C and is compatible with the next generation of commercial glass substrates [2]. The results demonstrate the importance of both the grain size and grain orientation in determining the performance of polycrystalline silicon TFT's. A detailed discussion of this work is given in

Chapter 7.

CHAPTER 6

TFT'S FABRICATED AT 600°C: EFFECTS OF GRAIN SIZE

6.1 Introduction

The results of Chapter 3, along with all the previous work on seed selection through ion channeling [7–13], have an important implication in thin-film transistor technology: they have demonstrated the fact that ion implantation followed by furnace annealing can enhance the average grain size of a pyrolytically deposited polycrystalline silicon film. This enhanced average grain size can reduce the area of grain boundaries in the film, and thereby improve the performance of TFT's fabricated in the film. Noguchi *et al.* [32] and Ohshima *et al.* [33] have combined this grain-growth technique with hydrogen passivation and super-thin (200–300 Å) polycrystalline silicon films to obtain *n*-channel TFT's with superior performances.

This chapter reports a more complete study that compares the characterisitcs of thin-film transistors fabricated on the as-deposited and the amorphized-crystallized polycrystalline silicon films. The objective is to determine the effect of an enhanced average grain size on TFT performance, in the absence of other performance-enhancement techniques such as hydrogen passivation and the use of super-thin films. Both *n*- and *p*-channel MOS TFT's have been fabricated and characterized. The entire fabrication process has been carried out at low temperatures ($\leq$ 600°C) compatible with low-cost, commercial glass substrates.

6.2 Experimental Procedure

Starting with 2", lightly doped, <100> silicon wafers, a 0.80 μm thick SiO_2 layer was thermally grown at 1100°C in dry-wet-dry oxidizing ambients. Polycrystalline silicon films, 0.35 μm thick, were then deposited onto these oxidized wafers via the low-pressure chemical-vapor deposition technique at 625°C, using the same deposition parameters as in Chapter 3. Half of these silicon films were then amorphized via self-implantation at 7° from normal incidence, at a temperature of 77°K, with an accelerating voltage of 200 keV, and with a dose of 2×10^{15} cm^{-2}. Based on the results of Chapter 3, this implantation should completely amorphize the silicon films and thereby lead to the largest possible average grain size after crystallization at 600°C. This largest possible average grain size was 2.0 μm, versus the as-deposited 0.080 μm.

Both *n*- and *p*-channel, MOS thin-film transistors were then fabricated using the process schematically illustrated in Fig. 21. Starting with the as-deposited or the as-amorphized silicon films, Fig. 21(a), the transistor islands were first delineated, Fig. 21(b). The source and drain regions were then defined by implantation of either phosphorus at 180 keV and 1×10^{16} cm^{-2} or boron at 80 keV and 1×10^{16} cm^{-2}, using a pyrolytic oxide-photoresist bilayer as the channel mask, Fig. 21(c). After removal of the channel mask, a 0.10 μm thick SiO_2 layer was deposited pyrolytically at 400°C as the gate insulator, and the samples were then annealed at 600°C for 24 h in O_2 plus 12 h in N_2, to crystallize the amorphized films as well as to activate the implanted dopants, Fig. 21(d). The source and drain contacts were then opened, and a 0.60 μm thick aluminum layer was *e*-gun evaporated and patterned, Fig. 21(e). Finally, the samples were sintered at 450°C for 60 min in an N_2:H_2 (80:20) ambient.

Thin-film transistors with the same channel width (W = 200 μm at the mask

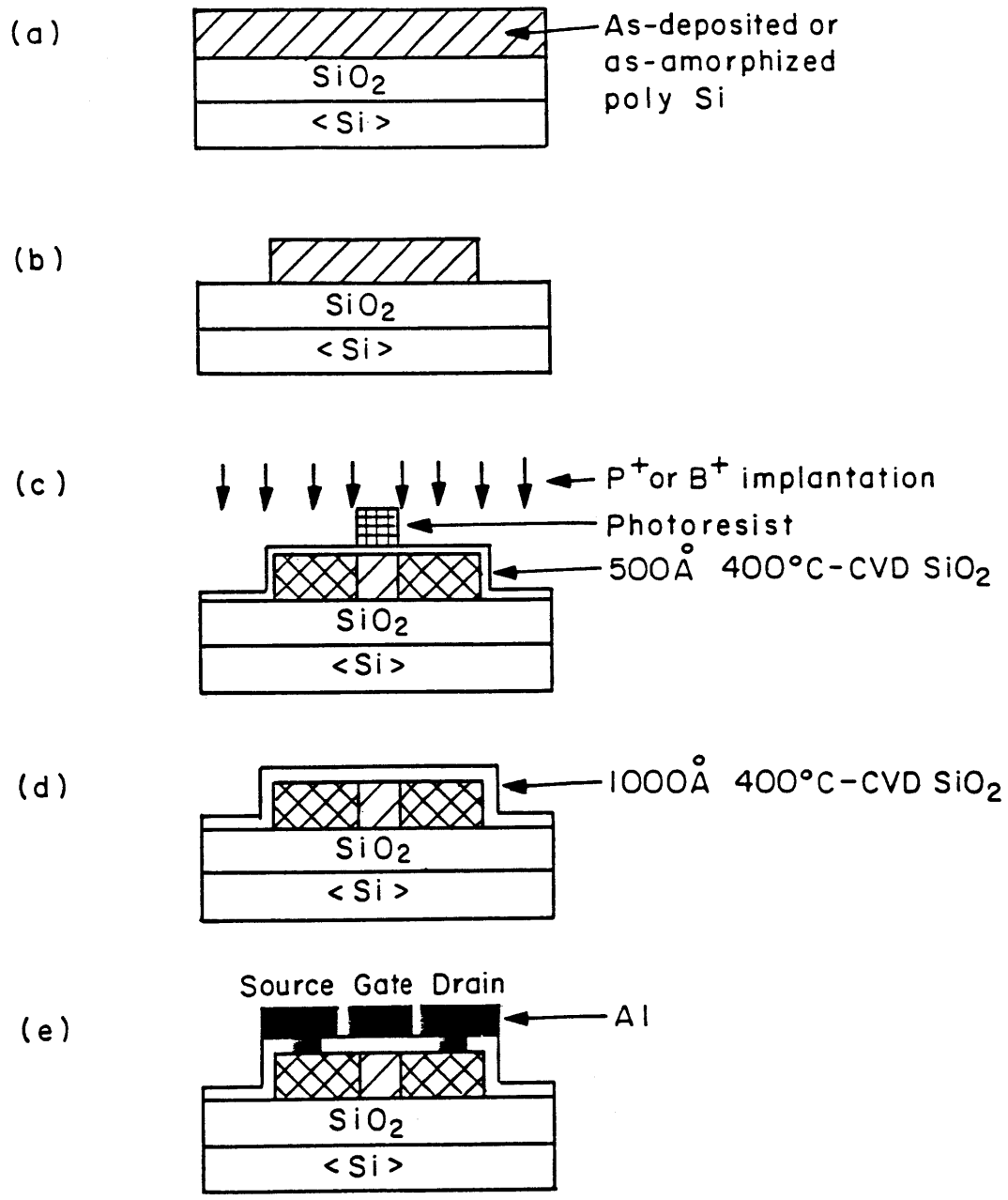


Figure 21 Schematic illustration of the 600°C TFT fabrication process.

level) but three different channel lengths (L = 20, 10, and 5 μm) were fabricated. The final gate oxide thickness (t_{ox} = 850 Å) was measured via both ellipsometry and the capacitance-voltage technique. All the electrical measurements were made with the source of the transistor grounded and the bulk of the transistor floating.

6.3 Results and Discussion

Figure 22 shows the output characteristics of typical thin-film transistors fabricated in this work. The drain current I_D is plotted as a function of the drain voltage V_D using the gate voltage V_G as a parameter. These characteristics were all measured from transistors with the same geometry, $W/L = 200/10$.

Figure 23 shows the transfer characteristics of the same transistors. The drain current I_D is plotted as a function of the gate voltage V_G using the drain voltage V_D as a parameter.

These two figures together give an order-of-magnitude indication of the relative current-driving capacities of these transistors/materials: (1) For the *n*-channel transistors, the amorphized-crystallized film offered a significantly higher current-driving capacity than the as-deposited film. (2) For the *p*-channel transistors, the amorphized-crystallized film offered a somewhat higher current-driving capacity than the as-deposited film. (3) When fabricated on the same material, the *n*-channel transistor exhibited a somewhat higher current-driving capacity than the *p*-channel transistor. Finally, Fig. 23 shows that a higher driving current was always accompanied by a higher leakage current such that the on-off current ratio would not vary much from one transistor/material to another.

Table 1 shows a summary of the characterisitcs of the thin-film transistors

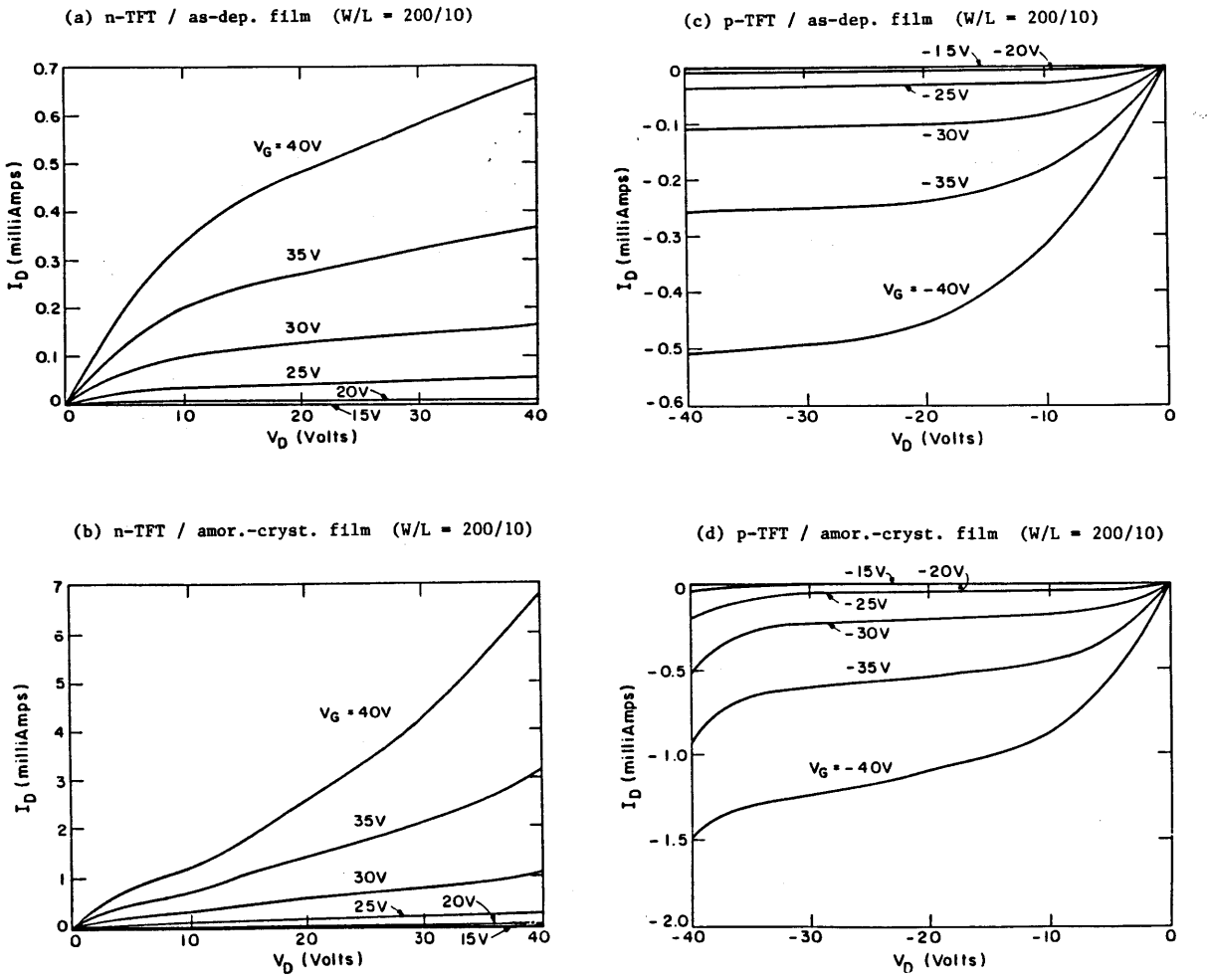


Figure 22 Output characteristics of typical TFT's fabricated at 600°C.

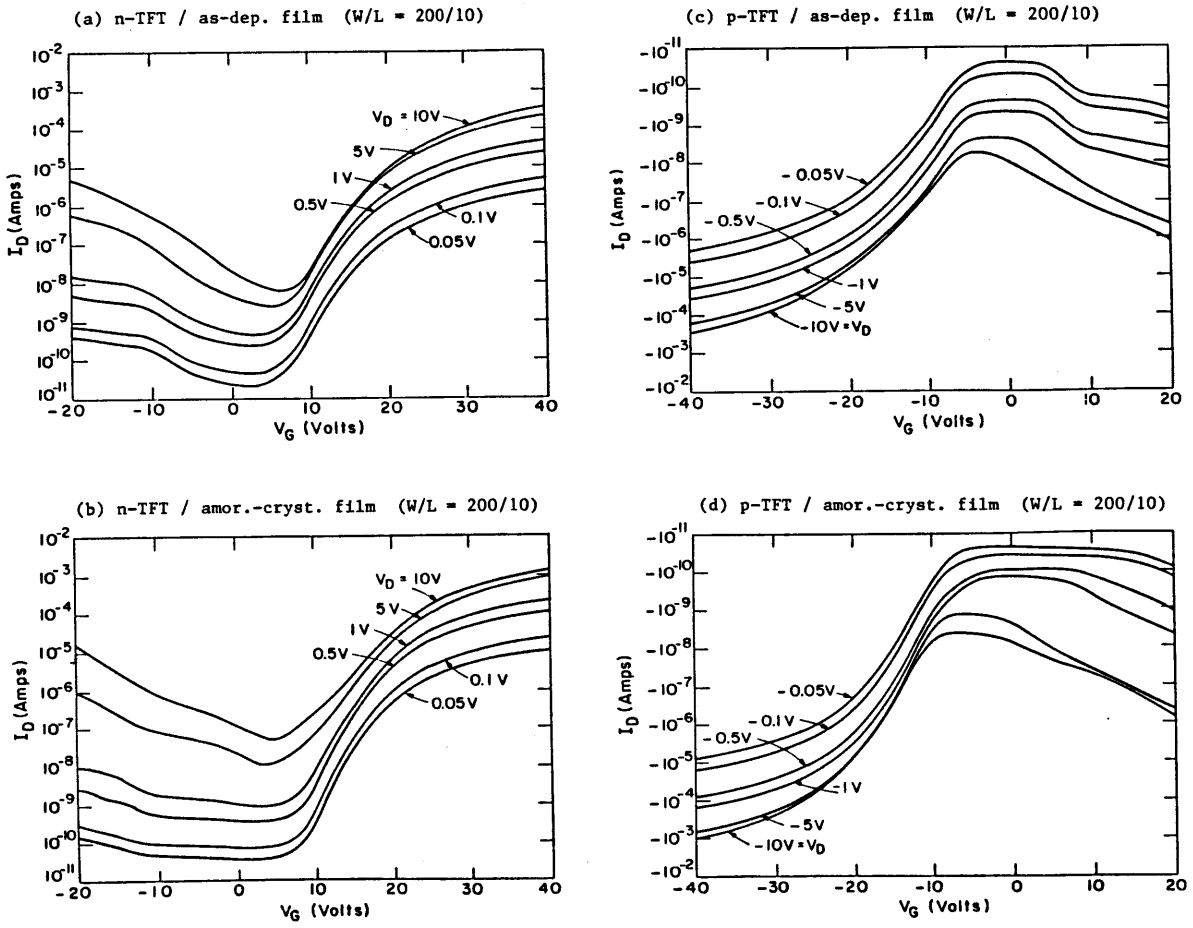


Figure 23 Transfer characteristics of typical TFT's fabricated at 600°C.

fabricated in this work. The threshold voltage, V_{th}, and the field-effect mobility, μ_{FE}, were both deduced from the linear region of the transistor characteristics [5]. Their values were independent of the transistor geometry except where indicated.

The threshold voltage was relatively independent of the material type, as shown in Table 1. For the *n*-channel transistors, it was slightly lower on the amorphized-crystallized film than on the as-deposited film. For the *p*-channel transistors, it was the same on both films. These threshold voltages had magnitudes much greater than the work function difference (typically around 1 V) between aluminum and silicon. Further, they were approximately equal in magnitude but opposite in polarity between the *n*-channel and the *p*-channel transistors. These observations imply that the Fermi level at the surface of the channel must have been pinned to mid gap due to the large densities of grain-boundary and surface states present.

The threshold voltages of the *n*-channel transistors exhibited a weak dependence on the channel length, as shown in Table 1. This weak dependence of the threshold voltage on the channel length was observed consistently for all *n*-channel transistors measured across a 2" wafer, but was not observed for the *p*-channel transistors. Since the *n*-channel and *p*-channel transistors were fabricated using the same process and differed only in the source/drain dopant (or charge carrier) type, this slight difference in their threshold behavior could imply that the grain-boundary and/or the surface states had a slightly asymmetric effect on the electrons and the holes. However, further research is required before the nature of this phenomenon can be established.

The field-effect mobility exhibited a clear dependence on the material type, as shown in Table 1. For both the *n*- and *p*-channel transistors, it was always 3–4 times higher on the amorphized-crystallized film than on the as-deposited

Table 1 Summary of the characteristics of thin-film transistors fabricated at 600°C.

Transistor / Material	V_{th} (V)	μ_{FE} (cm^2/V·s)
n-TFT / As-deposited film	23 ($L = 20$ μm) 24 ($L = 10$ μm) 25 ($L = 5$ μm)	3.5
n-TFT / Amor.-cryst. film	21 ($L = 20$ μm) 23 ($L = 10$ μm) 25 ($L = 5$ μm)	15
p-TFT / As-deposited film	−25	3.4
p-TFT / Amor.-cryst. film	−25	10.

film. This was due mainly to the larger average grain size in the amorphized-crystallized material. On the other hand, it was always higher for the *n*-channel transistor than for the *p*-channel transistor when both were fabricated on the same material, and this difference was more significant on the amorphized-crystallized film (which had a larger average grain size). This was due most likely to the higher intra-grain mobility for the electrons than for the holes.

6.4 Conclusion

This chapter reports an investigation that compares the characteristics of thin-film transistors fabricated on the as-deposited and the amorphized-crystallized polycrystalline silicon films. These polycrystalline silicon films were grown initially by the low-pressure chemical-vapor deposition technique at 625°C. The as-deposited film had an average grain size of 0.080 μm, and the amorphized-crystallized film an average grain size of 2.0 μm. The entire transistor fabrication was carried out at low temperatures ($\leq$ 600°C) compatible with low-cost, commercial glass substrates.

The results indicate that the amorphized-crystallized film is, in general, a more superior transistor material than the as-deposited film. For the *n*-channel transistors, the amorphized-crystallized film offered a slightly lower threshold voltage (21–25 versus 23–25 V) as well as a higher field-effect mobility (15 versus 3.5 $cm^2/V{\cdot}s$) than the as-deposited film. For the *p*-channel transistors, the amorphized-crystallized film offered the same threshold voltage (−25 V) but a higher field-effect mobility (10. versus 3.4 $cm^2/V{\cdot}s$) than the as-deposited film. When fabricated on the same material, the *n*-channel transistor outperforms the *p*-channel transistor in terms of a slightly lower threshold voltage and a higher field-effect mobility. These results demonstrate the effectiveness of this

implantation-annealing technique, which can enhance the average grain size of polycrystalline silicon films at low processing temperatures, in improving the performance of thin-film transistors.

CHAPTER 7

TFT'S FABRICATED AT 800°C: EFFECTS OF GRAIN SIZE AND {110} TEXTURE

7.1 Introduction

The results of Chapter 3 raised a dilemma in our efforts to optimize the seed selection through ion channeling process: the largest average grain size and the strongest {110} fiber texture were not obtained on the same processed film. As shown in Figs. 15 and 16, the average grain size increased monotonically with the implant dose, but the {110} fiber texture increased only initially with the dose, reached a maximum, and fell off quickly to nil as the dose increased beyond a critical value. The film with the largest average grain size of 2 μm (but without any crystallographic texture) had been shown in Chapter 6 to be a far more superior TFT material than the as-deposited, fine-grain polycrystalline silicon. However, the film with the strongest {110} fiber texture (but with an intermediate average grain size of 1 μm) had never been investigated with regard to its TFT performance.

This chapter investigates the effects of an enlarged average grain size and an enhanced {110} fiber texture on the electrical properties and transistor characteristics of polycrystalline silicon films. Sheet resistors with the van der Pauw configuration [34] and MOS thin-film transistors have been fabricated and characterized on the various processed polycrystalline silicon films. All the fabrication processes have been carried out at low temperatures ($\leq$ 800°C) compatible with the latest Corning 1729 glass substrates [2].

7.2 Experimental Procedure

Starting with 2", lightly doped, <100> silicon wafers, a 0.80 μm thick SiO_2 layer was thermally grown at 1100°C in dry-wet-dry oxidizing ambients. Polycrystalline silicon films, 0.35 μm thick, were then deposited onto these oxidized wafers via the low-pressure chemical-vapor deposition technique at 625°C, using the same deposition parameters as in Chapter 3. One third of these silicon films were then self-implanted at normal incidence, at a temperature of 77°K, with an accelerating voltage of 200 keV, and with a dose of 11×10^{14} cm^{-2}. Another third of these silicon films were self-implanted at normal incidence, at a temperature of 77°K, with an accelerating voltage of 200 keV, and with a dose of 20×10^{14} cm^{-2}. These implanted films were subsequently annealed at 600°C for 48 h in N_2.

The material properties of these three batches of polycrystalline silicon films have been reported in Chapter 3. The as-deposited film is characterized by the smallest average grain size, 0.080 μm, among all films as well as a weak {110} fiber texture. The 11×10^{14} cm^{-2} film has an intermediate average grain size, 1.0 μm, but is characterized by the strongest {110} fiber texture among all films. The 20×10^{14} cm^{-2} film, on the other hand, is characterized by the largest average grain size, 2.0 μm, among all films but has no crystallographic texture.

Sheet resistors with the van der Pauw configuration [34] were fabricated on these three batches of polycrystalline silicon films to investigate the electrical properties as functions of the dopant concentration. The silicon films were first doped via implantation of either phosphorus or boron, using the schedules summarized in Table 2. Simulations using SUPREM III [35] showed that, for each dopant, three separate implants at energies and doses as shown in the table were needed to achieve an essentially flat depth profile throughout the silicon

Table 2 Phosphorus and boron implantation schedules used for doping the polycrystalline Si films. For either dopant, the three separate implants were needed to achieve a flat depth profile. m and n are scaling factors that can be varied to achieve the desired dopant concentration.

Dopant	Implant Schedule	Resulting Concentration
Phosphorus	30 keV, $(1.5\times10^{14}\ \mathrm{cm^{-2}})\cdot m$ 115 keV, $(1.5\times10^{14}\ \mathrm{cm^{-2}})\cdot m$ 240 keV, $(2.6\times10^{14}\ \mathrm{cm^{-2}})\cdot m$	$(1.4\times10^{19}\ \mathrm{cm^{-3}})\cdot m$
Boron	20 keV, $(1.5\times10^{14}\ \mathrm{cm^{-2}})\cdot n$ 60 keV, $(1.5\times10^{14}\ \mathrm{cm^{-2}})\cdot n$ 110 keV, $(2.0\times10^{14}\ \mathrm{cm^{-2}})\cdot n$	$(1.1\times10^{19}\ \mathrm{cm^{-3}})\cdot n$

film. The activation anneal was performed at 800°C, for 30 min in pyrogenic steam followed by 30 min in nitrogen. An oxide layer of < 200 Å thickness was grown on the surface of the silicon film as a result of the anneal in pyrogenic steam, and it served as a surface passivation layer. The doped silicon films were then lithographically patterned into the van der Pauw configuration. The contacts were formed with a 0.50 μm thick aluminum layer, *e*-beam evaporated, patterned, and sintered at 450°C for 30 min in an N_2:H_2 (80:20) ambient. All the resistivity and Hall effect measurements were made by using an automated van der Pauw setup that could accept inter-probe resistances of up to 10 MΩ.

MOS thin-film transistors were also fabricated on these three batches of polycrystalline silicon films. Both *n*-channel and *p*-channel transistors were fabricated, using a self-aligned process schematically illustrated in Fig. 24. Starting with the (undoped) polycrystalline silicon films, Fig. 24(a), the transistor islands were first delineated, Fig. 24(b). A 200–250 Å thick gate oxide was thermally grown at 800°C in dry O_2, in 6 h. To keep the processing temperatures within 800°C, the 0.35 μm thick, degenerately doped polycrystalline silicon gate was formed in two steps: A 0.10 μm thick layer was first pyrolytically deposited and doped by phosphorus diffusion (using a P_2O_5 source, at 800°C for 6 h in N_2); a 0.25 μm thick layer was then pyrolytically deposited and doped by phosphorus implantation (at 80 keV and 1×10^{16} cm^{-2}), Fig. 24(c). The channel region was lithographically defined, and the source and drain regions were formed by implantation of either phosphorus (at 120 keV and 1×10^{16} cm^{-2}) or boron (at 40 keV and 1×10^{16} cm^{-2}), Fig. 24(d). The samples were then annealed at 800°C for 1 h in O_2 plus 1 h in N_2, to activate the implanted dopants. A 0.75 μm thick field oxide was then pyrolitically deposited at 400°C. The contact holes were opened, and a 0.75 μm thick Al:Cu:Si (1:4%:2%) layer was sputtered and patterned, Fig. 24(e). Finally, the samples were sintered at 450°C for 30 min in an

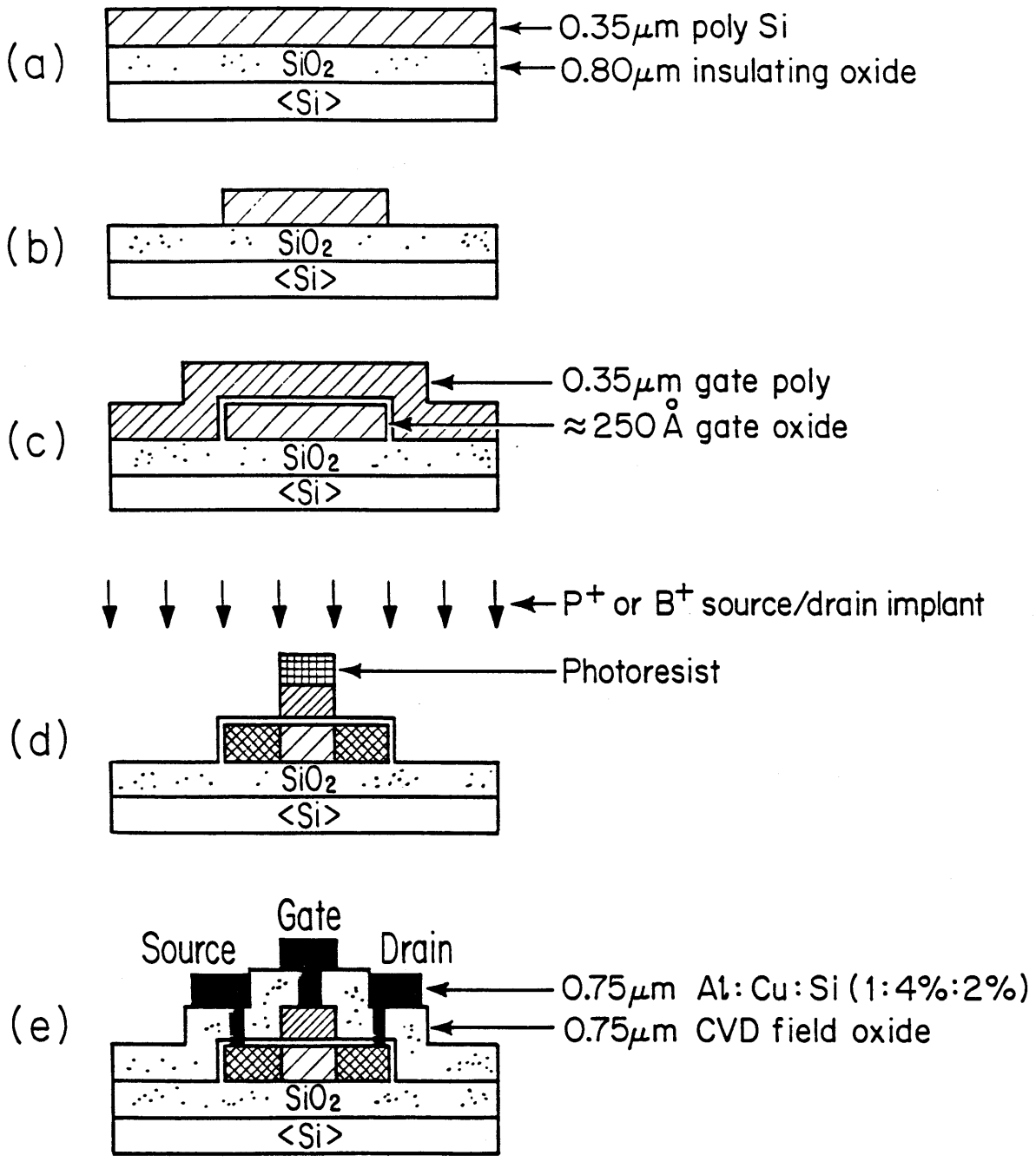


Figure 24 Schematic illustration of the 800°C TFT fabrication process.

N_2:H_2 (80:20) ambient.

Thin-film transistors with the same channel width (W = 200 μm at the mask level) but three different channel lengths (L = 20, 10, and 5 μm at the mask level) were fabricated. The gate oxide thicknesses (t_{ox} = 200, 230, and 220 Å on the as-deposited, 11×10^{14} cm^{-2}, and 20×10^{14} cm^{-2} films, respectively) were measured via the capacitance-voltage technique. All the transistor measurements were made with the source of the transistor grounded and the bulk of the transistor floating. For the purpose of this study we are interested only in transistor operations under gate and drain biases in the range from 0 to $\pm$5 V (with positive voltages for the n-channel transistors and negative voltages for the p-channel transistors), as are standard for digital integrated circuits.

It is of great importance to confirm that the doping and transistor fabrication processes have not altered significantly the structures of the polycrystalline silicon films, mainly the average grain sizes and the crystallographic textures. We have used transmission electron microscopy and x-ray pole-figure measurement to examine the following films: the ones doped with a high phosphorus concentration of 1.4×10^{19} cm^{-2}, the ones doped with a high boron concentration of 1.1×10^{19} cm^{-2}, and some monitors that have been processed identically as the channel region of the transistor. The results indicate no significant change in either the average grain sizes or the crystallographic textures of all these films.

7.3 Results and Discussion

Figures 25 and 26 demonstrate the electrical properties of the three polycrystalline silicon films investigated in this work. Figure 25 shows the resistivity, the effective Hall mobility, and the effective carrier concentration as functions of the phosphorus dopant concentration. Figure 26 shows the resistivity, the

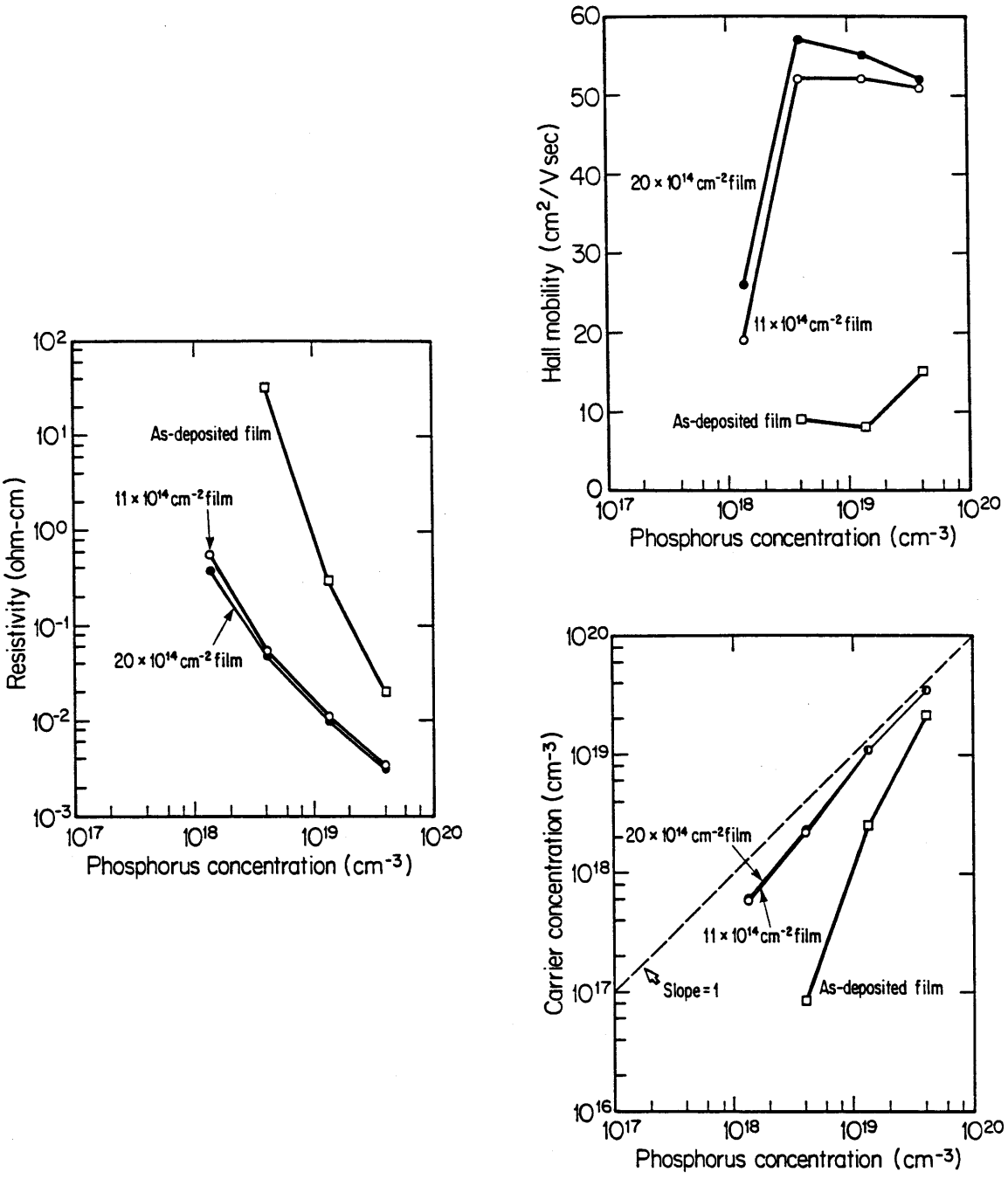


Figure 25 Resistivity, effective Hall mobility, and effective carrier concentration vs. phosphorus concentration for the three polycrystalline silicon films.

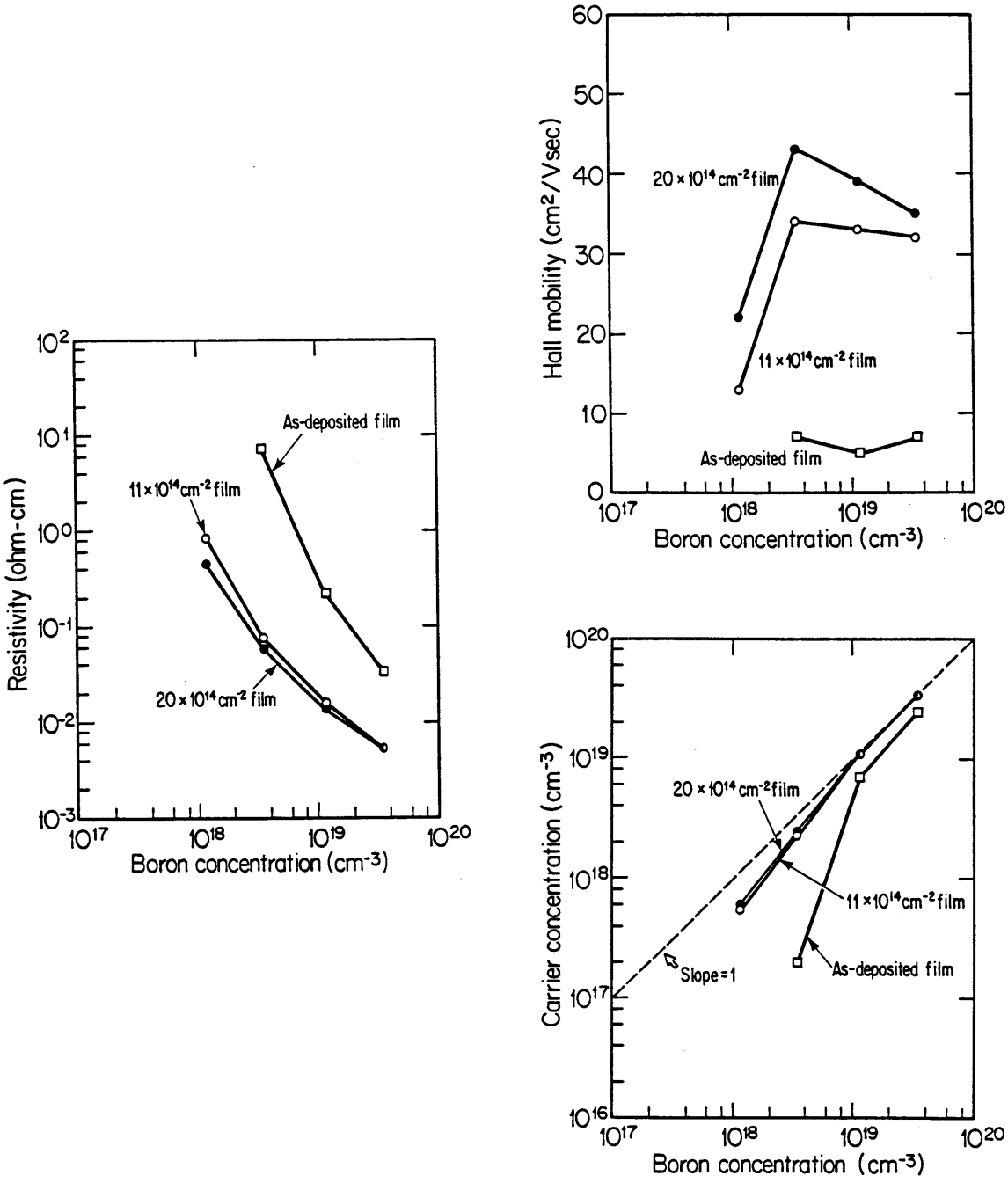


Figure 26 Resistivity, effective Hall mobility, and effective carrier concentration vs. boron concentration for the three polycrystalline silicon films.

effective Hall mobility, and the effective carrier concentration as functions of the boron dopant concentration. The dependences of these electrical properties on the dopant concentration are in good agreement with those reported in earlier studies by other researchers [36,37] and will not be elaborated on here.

Two aspects of these curves, which relate the electrical properties to the material properties of polycrystalline silicon, are of interest to us:

(1) The 20×10^{14} cm^{-2} film has exhibited the lowest resistivity, the highest Hall mobility, and the highest carrier concentration among the three films, consistently for the entire range of dopant species and concentrations investigated. The as-deposited film, on the other hand, has exhibited the highest resistivity, the lowest Hall mobility, and the lowest carrier concentration. This is because the 20×10^{14} cm^{-2} film has the largest average grain size, and the as-deposited film has the smallest average grain size, among the three films [36,37].

(2) The differences among the three films have narrowed as the dopant concentration increases beyond $\approx 4\times10^{18}$ cm^{-3}. This is because the electrical properties of polycrystalline silicon should approach those of monocrystalline silicon as the dopant concentration increases beyond a critical value [36,37].

These observations indicate that an enhanced average grain size can improve the electrical properties of these polycrystalline silicon films, in agreement with the widely accepted grain-boundary trapping model [36,37]. They also indicate that an enhanced {110} fiber texture has no apparent effect on the electrical properties.

Figures 27–29 demonstrate the current-voltage characteristics of typical thin-film transistors fabricated in this work. Figure 27 shows the output characteristics, with the drain current I_D versus the drain voltage V_D using the gate voltage V_G as a parameter. Figure 28 shows the transfer characteristics, with the drain current I_D versus the gate voltage V_G using the drain voltage V_D as a parameter.

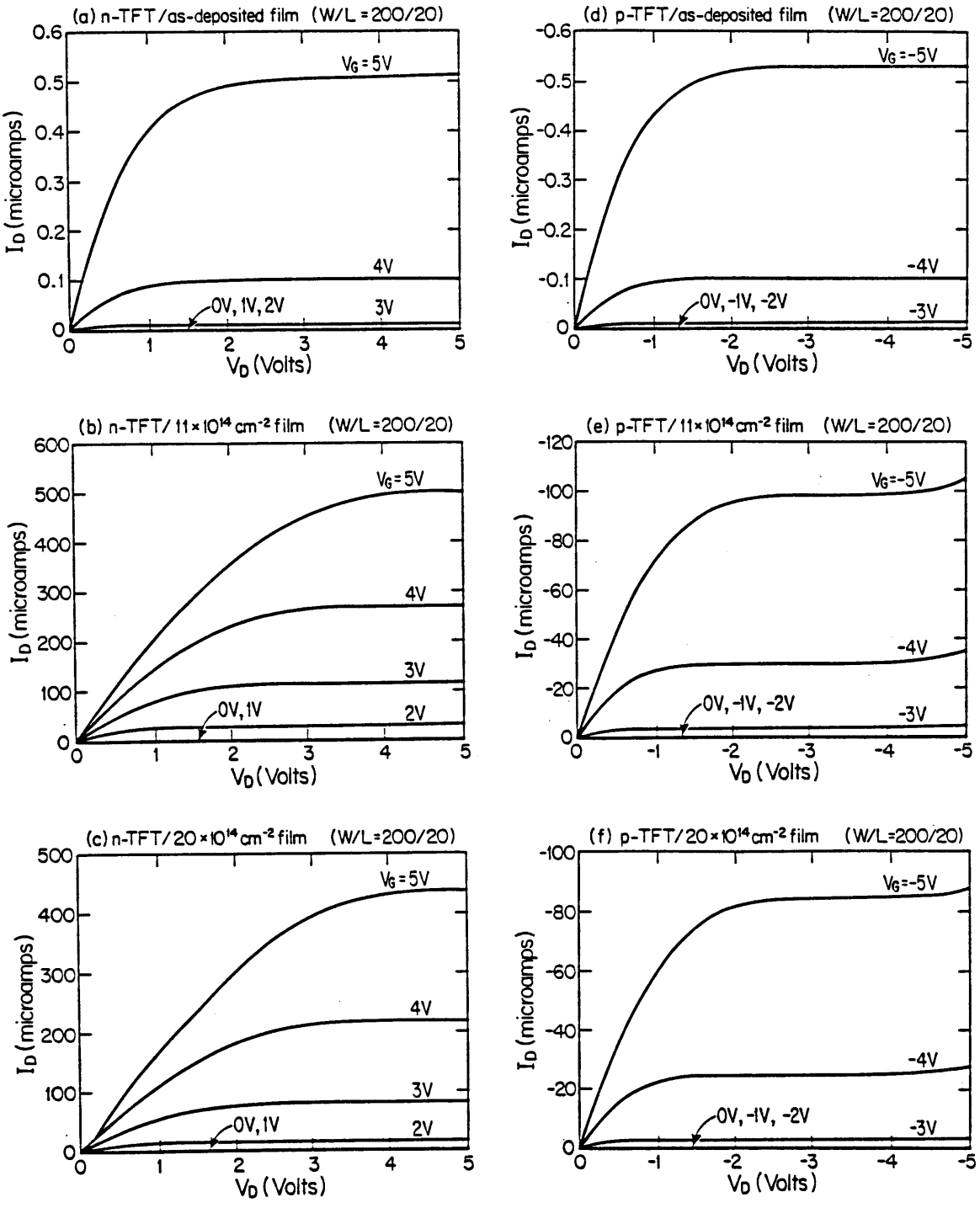


Figure 27 Output characteristics of typical TFT's fabricated at 800°C.

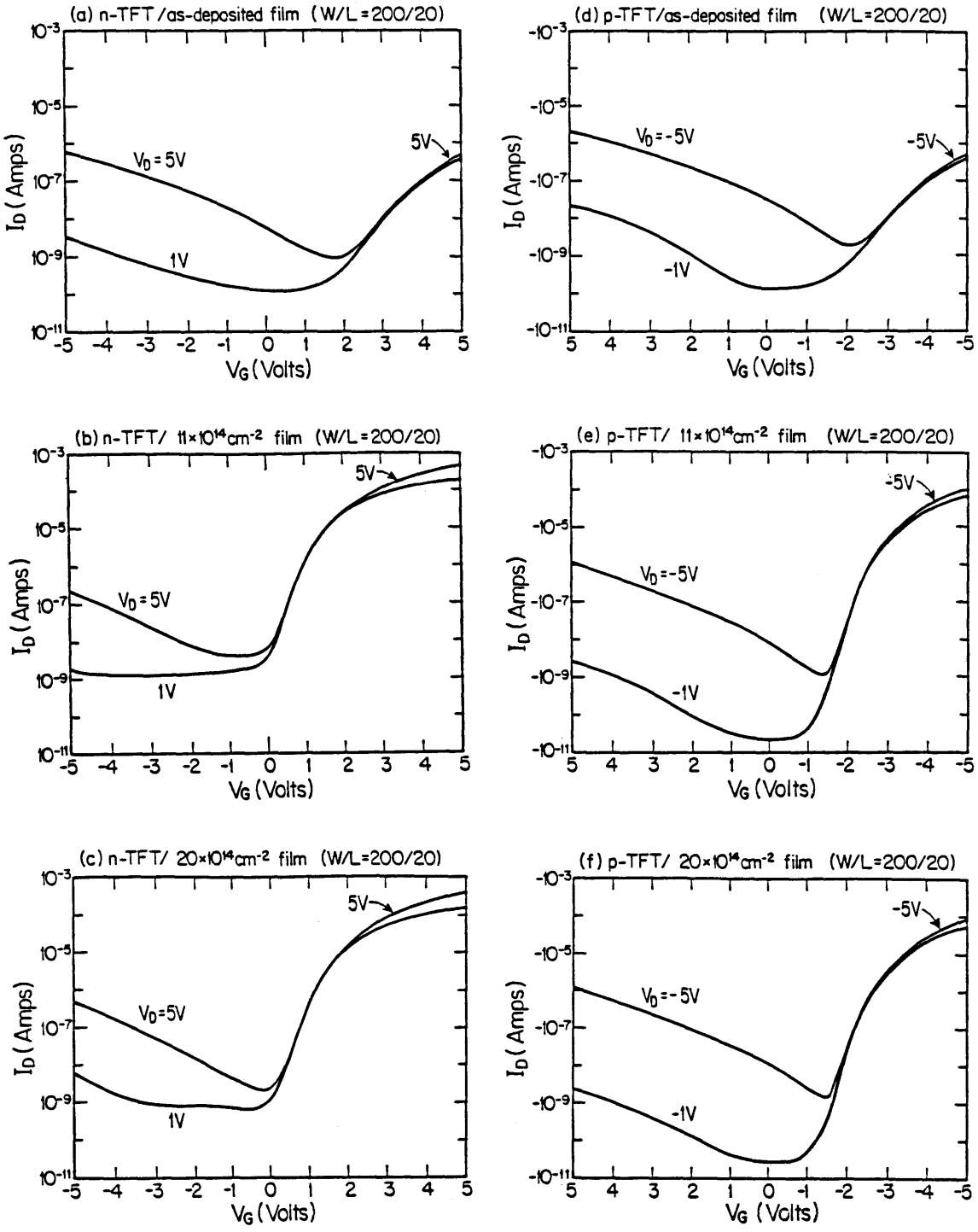


Figure 28 Transfer characteristics of typical TFT's fabricated at 800°C.

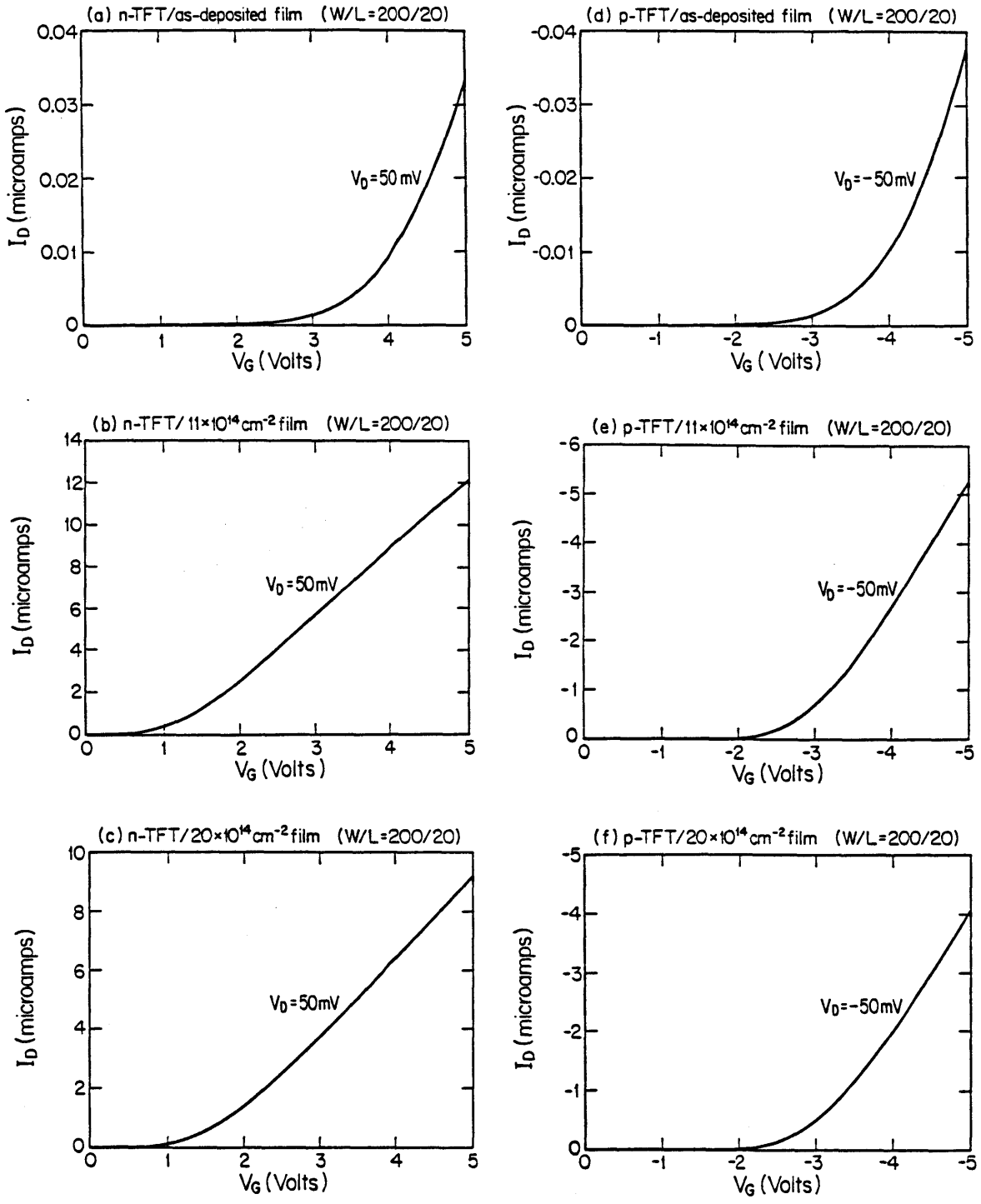


Figure 29 Turn-on characteristics of typical TFT's fabricated at 800°C.

Figure 29 shows the turn-on characteristics, with the drain current versus the gate voltage at a low-field drain voltage of 50 mV. These characteristics have been measured from transistors with the same geometry, $W/L = 200/20$.

These figures indicate that all the thin-film transistors fabricated in this work exhibit good MOSFET behavior. Together they give an order-of-magnitude indication of the relative current-driving capacities of these three transistor materials: the two implanted-annealed films offer comparable and much higher current-driving capacities than the as-deposited film.

Table 3 shows a summary of the characteristics of the thin-film transistors fabricated in this work. The threshold voltage, V_{th}, and the field-effect mobility, μ_{FE}, have been deduced from the linear region of the transistor characteristics, such as those shown in Fig. 29. Their values are independent on the transistor geometry, and are dependent only on the transistor type and material type, as shown in the table.

Table 3 shows that the 11×10^{14} cm^{-2} film is clearly the best TFT material among the three investigated in this work. It has offered the lowest threshold voltage and the highest field-effect mobility for either the *n*-channel or the *p*-channel transistors. The 20×10^{14} cm^{-2} film has offered either equal or slightly worse characteristics. The as-deposited film, on the other hand, has offered significantly worse characteristics. The superiority of the two implanted-annealed films over the as-deposited film can be explained via the grain-boundary trapping model [36,37], as they have much larger average grain sizes than the as-deposited film. The difference between the two implanted-annealed films is, however, more difficult to reconcile, because the better material is characterized by a smaller average grain size. The crystallographic texture must have played a role in determining the TFT performance.

Table 4 shows a summary of the material, electrical, and transistor proper-

Table 3 Summary of the characteristics of thin-film transistors fabricated at 800°C.

Transistor / Material	V_{th} (V)	μ_{FE} ($cm^2/V \cdot s$)
n-TFT / As-deposited film	4	0.4
n-TFT / 11×10^{14} cm^{-2} film	1.2	42
n-TFT / 20×10^{14} cm^{-2} film	1.6	35
p-TFT / As-deposited film	−4	0.5
p-TFT / 11×10^{14} cm^{-2} film	−3.0	34
p-TFT / 20×10^{14} cm^{-2} film	−3.0	24

ties of the three polycrystalline silicon films investigated in this work. We now propose a general model to interpret these results, that is, to relate the electrical properties and transistor performances to the material properties of polycrystalline silicon. This general model is formulated by considering how the average grain size and the {110} fiber texture can modify the grain-boundary and the surface effects in the polycrystalline silicon films:

(1) The grain-boundary effect. An enhanced average grain size can reduce the grain-boundary effect by reducing the area of grain-boundaries in the film. An enhanced {110} fiber texture, however, cannot reduce the grain-boundary effect because the in-plane orientations are still random. Most of our results, as summarized in Table 4, can be explained using the grain-boundary effect alone: a larger average grain size leads to better electrical properties regardless of the {110} fiber texture; and the significatly larger average grain sizes for the two implanted-annealed films lead to better transistor performances regardless of the {110} fiber texture.

(2) The surface effect. The surface properties of polycrystalline silicon can vary with the crystallographic texture, though not with the average grain size. A more favorable crystalline orientation can reduce the surface effect by reducing the density of fixed surface charge, the density of surface states, and/or the roughness of the surface morphology, at the silicon-oxide interface [38–40]. Among the major crystalline orientations of silicon, the <110> orientation exhibits a surface effect that falls in-between the best case of <100> and the worst case of <111> [38–40]. An enhanced {110} fiber texture may, therefore, lead to better surface properties than a random orientation on average. This is the most likely reason why the 11×10^{14} cm^{-2} film outperforms the 20×10^{14} cm^{-2} film as a TFT material despite its smaller average grain size.

Our general model has been formulated on the basis that both the grain-

Table 4 Summary of the material, electrical, and transistor properties of the three polycrystalline silicon films.

Film	Grain Size	Fiber Texture	Electrical Properties	Transistor Performance
As-deposited	0.080 μm	Weak {110}	Worst	Worst
11×10^{14} cm^{-2}	1.0 μm	Strong {110}	Good	Best
20×10^{14} cm^{-2}	2.0 μm	None	Best	Good

boundary and the surface effects can place limitations on the TFT performance. While an enhanced average grain size reduces the grain-boundary effect, and a more favorable crystalline orientation reduces the surface effect. To support this model, we offer two additional evidences below that show consistency.

First, consider Fig. 30, which compares the transfer characteristics of typical *n*-channel TFT's fabricated on the 11×10^{14} cm^{-2} film and the 20×10^{14} cm^{-2} film. In the linear and subthreshold regions (0 V $< V_G <$ 5 V) of the transistor characteristics, the 11×10^{14} cm^{-2} film exhibits a consistently higher conduction current than the 20×10^{14} cm^{-2} film. The conduction current in these regions is limited by both the grain-boundary and the surface effects. The 11×10^{14} cm^{-2} film is able to offer a higher conduction current because its surface properties are far more superior, despite its smaller average grain size. In the "low" leakage region (-4 V $< V_G <$ 0 V) of the transistor characteristics, the relative advantages reversed, and the 20×10^{14} cm^{-2} film exhibits a consistently lower leakage current than the 11×10^{14} cm^{-2} film. The leakage current in this region is dominated by conduction through the channel, as shown by a comparison of the simultaneously measured drain, souce, and gate currents of each transistor. It is equal to the reverse leakage current of the *p*-*n* junction at the drain end, which is under an effective reverse bias of $|V_D - V_G|$ [41]. This reverse leakage current is orders of mangitude higher in polycrystalline silicon than in monocrystalline silicon, due presumably to the high density of defects present in the polycrystalline silicon [41]. The 20×10^{14} cm^{-2} film is able to offer a lower leakage current because its defect density, associated with a larger average grain size, is lower. Finally, in the "high" leakage region (-5 V $< V_G <$ 4 V), the relative advantages reverses again. The leakage current on the 11×10^{14} cm^{-2} film remains essentially constant and is still dominated by conduction through the channel. On the other hand, the leakage current on the 20×10^{14} cm^{-2} film increases

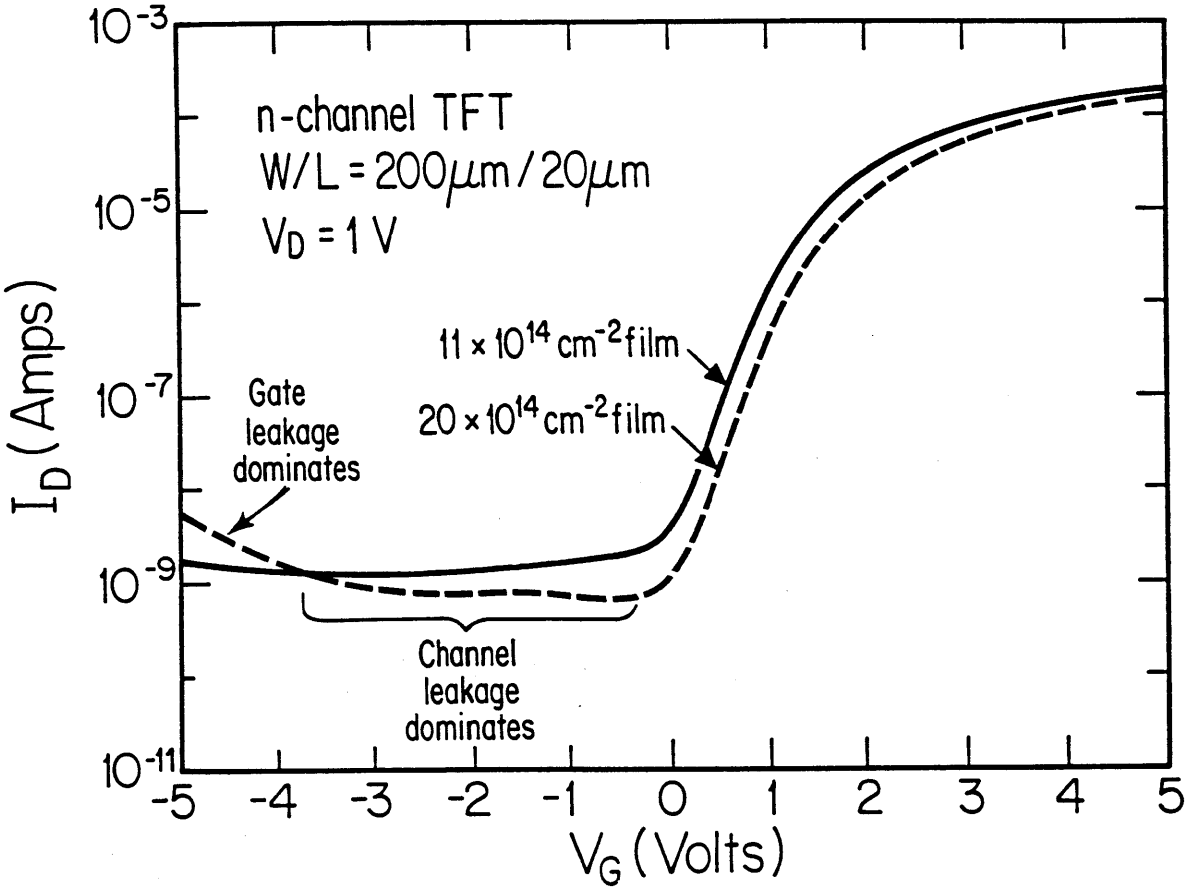


Figure 30 Transfer characteristics of typical *n*-channel TFT's fabricated at 800°C on the 11×10^{14} cm^{-2} film and the 20×10^{14} cm^{-2} film.

rapidly as the reverse gate bias increases. This rapid increase of leakage current in the latter case is due to a sharp increase in the gate current, while the source current remains essentially constant, as shown by a comparison of the simultaneously measured drain, source, and gate currents. The small difference in the gate oxide thickness, 230 Å on the 11×10^{14} cm^{-2} film and 220 Å on the 20×10^{14} cm^{-2} film, is an unlikely cause for the large difference in the gate oxide conductance between the two films. Several studies by other researchers [42–44] have shown that oxides grown on polycrystalline silicon can exhibit a higher conductance as well as a lower dielectric breakdown strength than those grown on monocrystalline silicon, and this is due to the rough surface morphology of the polycrystalline silicon-oxide interface. The lower gate oxide conductance for the 11×10^{14} cm^{-2} film, therefore, implies a smoother silicon-oxide interface for the film, which, in turn, may have originated from a more favorable crystalline orientation. All these observations from Fig. 30 are consistent with our model, that while a larger average grain size leads to better bulk properties, a more favorable crystalline orientation leads to better surface properties. Similar results have also been observed for the *p*-channel transistors.

Next, consider Fig. 31, which compares the input referred noise spectra of typical *n*-channel TFT's fabricated on these two films. These noise spectra have been measured under a large gate bias ($V_G = 4$ V), to induce a strong inversion layer, and a small drain bias ($V_D = 200$ mV), to avoid any major perturbation of the channel potential. This figure shows two important characteristics of the low-frequency noises in these transistors: (1) The input referred noises for both transistors exhibit a $1/f$ dependence; and (2) the $1/f$ noise is consistently lower on the 11×10^{14} cm^{-2} film than on the 20×10^{14} cm^{-2} film. For MOS transistors fabricated on monocrystalline silicon, the $1/f$ noise has been, in general, attributed to the statistical fluctuations of the occupancies of surface

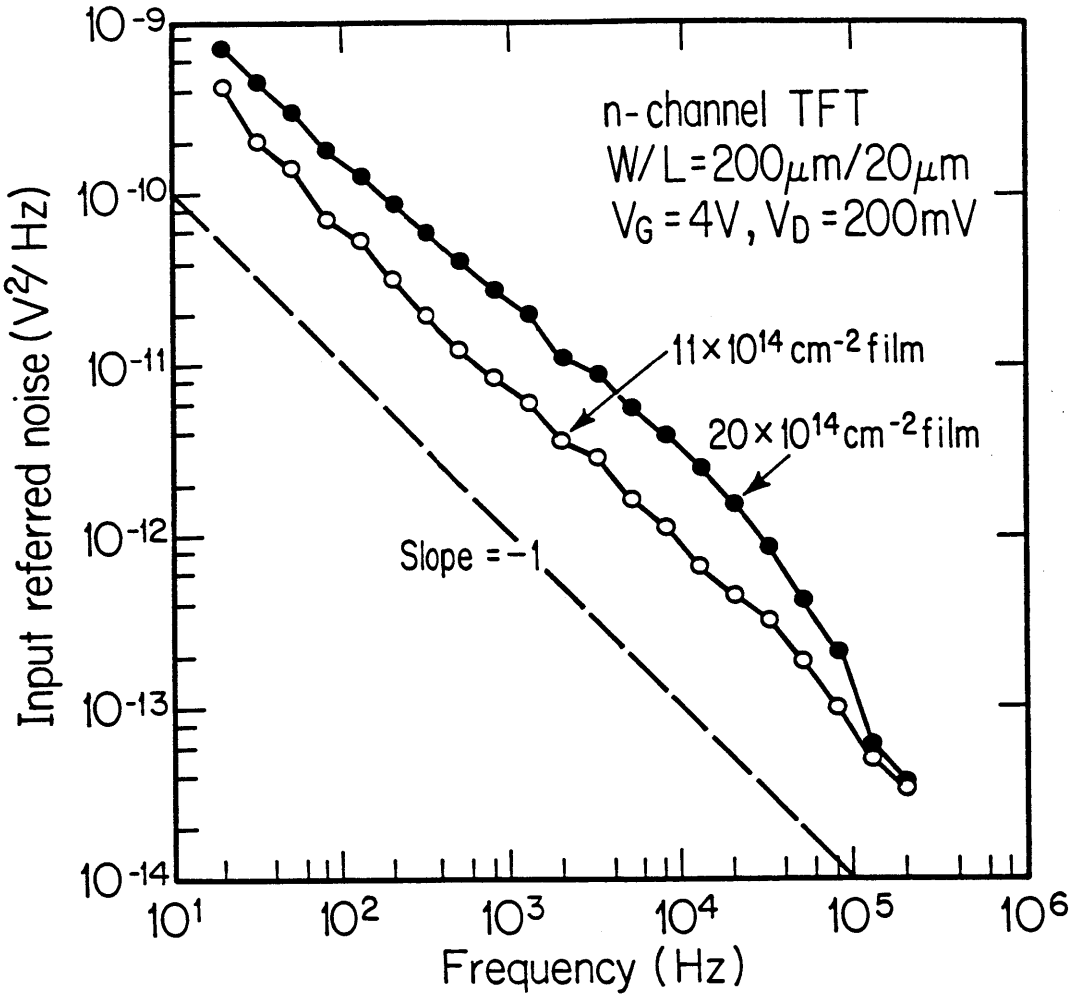


Figure 31 Input referred noise spectra of typical *n*-channel TFT's fabricated at 800°C on the 11×10^{14} cm^{-2} film and the 20×10^{14} cm^{-2} film.

states, located at or near the silicon-oxide interface [45–48]. For MOS transistors fabricated on polycrystalline silicon, the $1/f$ noise can originate from either the surface states or the grain-boundary states (or defect states). Since the density of grain-boundary states is higher in the 11×10^{14} cm^{-2} film than in the 20×10^{14} cm^{-2} film, as can be expected by comparing their average grain sizes and as confirmed by comparing their electrical properties, the lower $1/f$ in the 11×10^{14} cm^{-2} film can be reconciled only by a lower density of surface states in the film. These results imply that a {110} oriented surface exhibits a lower density of surface states than a randomly oriented surface on average, and this implication is consistent with our model. Similar results have also been observed for the *p*-channel transistors.

7.4 Conclusion

This chapter investigates the effects of an enlarged average grain size and an enhanced {110} fiber texture on the electrical properties and transistor characteristics of polycrystalline silicon films. The results demonstrate that the electrical properties, which characterize conduction along the bulk of the film, are dependent on the average grain size but independent of the {110} texture. The transistor performance, which characterizes conduction along the surface of the film, are nevertheless dependent on both the average grain size and the {110} texture.

We have proposed a general model to interpret these results, by considering how an enlarged average grain and an enhanced {110} fiber texture can affect the bulk and surface properties of a polycrystalline silicon film. An enlarged average grain size can reduce the area of grain boundaries in the film and thereby reduce the grain-boundary effect. An enhanced {110} fiber texture, on the other hand,

can reduce the surface effect (compared to a random orientation on average) by reducing the density of fixed surface charge, the density of surface states, and/or the roughness of the surface morphology, at the silicon-oxide interface. All the observations obtained in this work are consistent with this model.

CHAPTER 8

CONCLUSION

We have completed an integrated research program to investigate the potential of seed selection through ion channeling as a new silicon-on-insulator technology. The program has been carried out in two parts. Part I emphasized the materials work, and included the optimization of the seed selection through ion channeling process via a systematic approach. Part II emphasized the device work, and included the fabrication and characterization of MOS thin-film transistors on the various processed polycrystalline silicon films. The overall results are expected to have a significant impact on large-area electronics technology.

The establishment of an effective approach for optimizing the seed selection through ion channeling process is the most important accomplishment of the materials work in Part I. The previous research on SSIC had focused on several isolated experiments and on the limited objective of demonstrating the existence of the process [7–13]. This thesis research has focused, instead, on investigating the effects of varying the most critical process parameter, namely, the implant dose. The objective is to optimize the process, and to determine any fundamental limitation(s) to such an optimization approach. We have demonstrated the effectiveness of this optimization approach in growing {110}-fiber-textured polycrystalline silicon films (in Chapter 3). We have also proposed a modification of this optimization approach for growing restricted-fiber-textured polycrystalline silicon films (in Chapter 4). Unfortunately, we have not been able to work on this modified approach due to the lack of a more sophisticated implantation-annealing equipment.

The demonstration of the surface effect as a major limitation on the per-

formance of polycrystalline silicon thin-film transistors is the most important accomplishment of the device work in Part II. The previous research on TFT's had focused on the relevence of the grain-boundary effect, and had practically ignored the relevence of the surface effect [1]. We have demonstrated that both the grain size and grain orientation can be important factors in determining the TFT performance (in Chapters 6 and 7). We have also demonstrated that, for grain sizes of the order of 1–2 μm, a strong {110} fiber texture can be more effective than a larger average grain size in improving the TFT performance (in Chapter 7). These findings will have significant implications in the design, fabrication, and optimization of polycrystalline silicon TFT's in larger-area electronics technology.

The future research on seed selection through ion channeling should focus on the following two areas:

(1) The {100} orientation is the most preferable orientation of silicon for the operation of MOSFET's, since it exhibits the minimum surface effect. We have been "forced" to work with {110}-textured silicon films throughout this program because our low-pressure chemical-vapor deposition system offers no alternative. We should devote part of our future efforts to obtain {100}-textured silicon films, either by using a different deposition system [15] or by using a different deposition technique.

(2) The future of seed selection through ion channeling as a silicon-on-insulator technology will depend critically on the possibility of realizing its full potential, namely, the growth of restricted-fiber-textured silicon films. We have discussed and emphasized the necessity of a more sophisticated implantation-annealing equipment, which should allow the entire sequence of implant-anneal treatments to be performed without ever unloading the sample from the target holder. We should devote part of our future efforts to the construction of this

new equipment; the continuation of our research depends on it.

The future research on thin-film transistors can focus on a number of directions, the most important of which is probably the design and fabrication of circuits and systems using the best transistors produced in this work. Our research in TFT's has been driven, largely, by the applications of these transistors in large-area electronic systems. Our best TFT's, as shown in Table 3 in Chapter 7, have already exhibited superior characteristics that are among the best reported to date. The construction of circuits and systems using these transistors will demonstrate the worthiness of these transistors in real-life applications, and will increase the impact of our work on large-area electronics technology.

APPENDIX A

MODELING OF SSIC

The stochastic model of Iverson and Reif [11] is the only analytical model that has been published to date to describe the seed selection through ion channeling process. The model makes the following two assumptions regarding the process and the polycrystalline film:

(1) The process must be a basic process that consists of a single implantation step and a single annealing step;

(2) The polycrystalline film must be sufficiently thin so that it can be treated as a two-dimensional medium.

When these two assumptions are satisfied, an explicit expression can be derived to describe the average grain area in the processed film as a function of several material and process parameters. The key equations and parameters of the model are now summarized below.

The probability that an as-deposited grain will survive the implantation step is given by

$$P_G = (1 - r_c)P_G^r + r_c P_G^c, \tag{1}$$

where P_G^r is the probability of survival for an improperly oriented grain (where no channeling occurs), P_G^c is the probability of survival for a properly oriented grain (where channeling occurs), and r_c is the fraction of grains that are properly oriented. P_G^r can be shown, by using statistical treatments for the areas covered by the ion dose and ion damage, to follow the relation

$$-\ln(1-P_G^r) = [1 + 2Q(A_G A_D^r)^{1/2} + 2Q^2 A_G A_D^r - Q A_G] e^{-Q A_D^r}, \qquad (2)$$

where Q is the ion dose, A_G is the average grain area in the as-deposited film, and A_D^r is the effective film area amorphized by a non-channeling ion. P_G^c can be obtained by modifying Eq. (2) to incorporate the effect of ion channeling. The modification may be any one of the following:

(1) replacing Q with $Q - Q_C$, where Q_C is a critical dose below which 100% channeling occurs and above which no channeling occurs;

(2) replacing Q with $F_C Q$, where F_C is the non-channeling fraction of the ion dose;

(3) replacing A_D^r with A_D^c, which is the effective film area amorphized by a channeling ion.

The density of crystallites (per unit area) in a processed film is the sum of two components:

$$N = N_s + N_n, \qquad (3)$$

where N_s is the density of crystallites that have survived the implantation step, and N_n is the density of crystallites that have been nucleated during the annealing step. The first component is given by

$$N_s = P_G / A_G. \qquad (4)$$

The second component can be derived, using the theory of crystallization kinetics developed by Germain *et al.* [49] and the empirical parameters obtained by Zellema *et al.* [50], as

$$N_n = \int_0^\infty \epsilon r_n e^{-(t/\tau_n)^3} e^{-(t/\tau_s)^2} dt, \qquad (5)$$

where ϵ is the film thickness, r_n is the bulk nucleation rate, $\tau_n = (\pi v_g \epsilon r_n/3)^{-1/3}$ is a characteristic time constant for bulk nucleation, $\tau_s = (\pi v_g^2 N_s)^{-1/2}$ is a characteristics time constant for crystal growth, and v_g is the crystal growth velocity.

An explicit expression for the average grain area in the processed film, $1/N$, can now be derived by using Eqs. (1)–(5). This expression describes the average grain area as a function of several material and process parameters. These material and process parameters are summarized in Table 5.

To confirm the validity of the stochastic model, Iverson and Reif [11] have carried out an experiment to study the average grain area in a processed film, $1/N$, as a function of the ion dose, Q. In their experiment, 0.16 μm thick polycrystalline silicon films were grown by the low-pressure chemical-vapor deposition technique, amorphized by self-implantation, and crystallized at 700°C. The average grain area in a processed film was plotted as a function of the ion dose, and the stochastic model was used to fit the data points. An excellent agreement between the theory and the experiment was obtained, which confirmed the validity of the stochastic model.

Table 5 Summary of the material and process parameters used in the stochastic model of Iverson and Reif [11].

	Damage of Improperly Oriented Grains
A_G:	Average grain area in as-deposited film
A_D^r:	Effective area amorphized per non-channeling ion
	Damage of Properly Oriented Grains
r_c:	Fraction of grains properly oriented
Q_C:	Critical dose for channeling (1st model for channeling)
F_C:	Non-channeling fraction of ion dose (2nd model for channeling)
A_D^c:	Effective area amorphized per channeling ion (3rd model for channeling)
	Spontaneous Nucleation
r_n:	Bulk nucleation rate
v_g:	Crystal growth velocity
ϵ:	Film thickness

APPENDIX B

MODELING OF TFT'S

Many analytical models have been published to date to describe the operations of polycrystalline silicon MOS TFT's. Some good examples include:

(1) the models of Korma *et al.* [51] and Greve and Hay [52], which describe the high-frequency capacitance-voltage characteristics;

(2) the models of Fossum *et al.* [53] and Madan and Antoniadis [54], which describe the leakage region of the current-voltage characteristics;

(3) the models of Ortiz-Conde and Fossum [55] and Faughnan [56], which describe the subthreshold region of the current-voltage characteristics;

(4) the models of Depp *et al.* [57,58], Colinge *et al.* [59,60], Fossum and Ortiz-Conde [61,62], and Anwar and Khondker [63,64], which describe the strong-inversion region of the current-voltage characteristics.

We are interested primarily in the last category of models [57–64], which describe the focus of our TFT work. We will summarize these models below. We will use the standard symbols and coordinate system as defined by Sze [5]; the x- and y-axes of this coordinate system are perpendicular and parallel, respectively, to the silicon-gate oxide interface.

The modeling of polycrystalline silicon MOS TFT's operating in the strong-inversion region has been, in general, carried out in three steps [57–64]:

The first step consists of the solution of the two-dimensional Poisson's equation for the channel region, with the appropriate boundary conditions. The two-dimensional Poisson's equation for the channel region is given by

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=$$

$$-\frac{q}{\epsilon_{si}}\{p(x,y)-n(x,y)-N_A f(E_A,E_f)+N_D[1-f(E_D,E_f)]\}$$

$$-\frac{q}{\epsilon_{si}}\left\{\delta(y)\int_{E_v}^{E_c}Q_{tp}(E)[1-f(E,E_f)]dE-\delta(y)\int_{E_v}^{E_c}Q_{tn}(E)f(E,E_f)dE\right\},(6)$$

where $\phi(x,y)$ = channel potential, with respect to the floating bulk,

q = electronic charge,

ϵ_{si} = permitivity of silicon,

$p(x,y)$ = free hole concentration,

$n(x,y)$ = free electron concentration,

N_A = acceptor concentration,

N_D = donor concentration,

$f(E,E_f)$ = $1/[1+e^{(E-E_f)/kT}]$, the Fermi-Dirac distribution function with Fermi energy E_f,

E_v = valence-band edge,

E_c = conduction-band edge,

$Q_{tp}(E)$ = density of hole traps at grain boundaries (in number of hole traps per unit area per unit energy), and

$Q_{tn}(E)$ = density of electron traps at grain boundaries (in number of electron traps per unit area per unit energy).

The boundary conditions at the silicon-gate oxide interface can be obtained by using Gauss's Law:

$$\epsilon_{si}\left[-\frac{\partial\phi(0,y)}{\partial x}\right] = \frac{\epsilon_{ox}}{t_{ox}}\left[V_G - V_{FB} - \phi(0,y) - V_B(y)\right], \tag{7}$$

where ϵ_{ox} = permitivity of gate oxide,

t_{ox} = thickness of gate oxide,

V_G = gate voltage,

V_{FB} = flat-band voltage, and

$V_B(y)$ = floating bulk voltage.

The other boundary conditions must be obtained by considering the transistor geometry as well as the underlying assumptions regarding the properties of the grain boundaries.

The second step consists of the deduction of the free carrier concentrations and the free carrier mobilities, based on the the channel potential resolved in the previous step. The free carrier concentrations throughout the channel region can be obtained by using the Maxwell-Boltzmann distribution:

$$p(x,y) = p_o e^{-q\phi(x,y)/kT}, \tag{8}$$

$$n(x,y) = n_o e^{q\phi(x,y)/kT}, \tag{9}$$

where p_o = free hole concentration in the floating bulk,

n_o = free electron concentration in the floating bulk,

k = Boltzmann constant, and

T = absolute temperature.

The free carrier mobilities near the surface of the channel region can be approximated by considering both the surface effect and the grain-boundary effect:

$$\mu(x,y) = \mu_o \cdot \left(\frac{E_\perp^c}{E_\perp}\right)^c \cdot e^{-E_{gb}(x,y)/kT}, \tag{10}$$

where μ_o = maximum mobility attainable, in the absence of both surface and grain-boundary effects,

$\left(\frac{E_\perp^c}{E_\perp}\right)^c$ = factor characterizing mobility degradation due to surface effect, with normal surface field $E_\perp$ and characteristic constants $E_\perp^c$ and c, and

$e^{-E_{gb}(x,y)/kT}$ = factor characterizing mobility degradation due to grain-boundary effect, with grain-boundary barrier height $E_{gb}(x,y)$.

The third and final step consists of the deduction of the current-voltage characteristics by using the gradual channel approximation [5]. The gradual channel approximation in the basic form is given by

$$dV(y) = -\frac{I_D}{q \cdot Z \cdot \mu(y) \cdot N(y)} \cdot dy, \tag{11}$$

where $V(y)$ = voltage drop along the channel, $\simeq V_B(y)$,

I_D = drain current,

Z = channel width,

$\mu(y)$ = effective free carrier mobility along the channel, and

$N(y)$ = effective density of free carriers along the channel.

The effective free carrier mobility is given by

$$\mu(y) = \frac{\int_0^\infty \mu_p(x,y)p(x,y)dx}{\int_0^\infty p(x,y)dx} \tag{12}$$

for p-channel transistors and

$$\mu(y) = \frac{\int_0^\infty \mu_n(x,y)n(x,y)dx}{\int_0^\infty n(x,y)dx} \tag{13}$$

for n-channel transistors, where $\mu_p(x,y)$ and $\mu_n(x,y)$ are based on Eq. (10). The effective density of free carriers, in coulombs per unit area, is given by

$$N(y) = \int_0^\infty p(x,y)dx \tag{14}$$

for p-channel transistors and

$$N(y) = \int_0^\infty n(x,y)dx \tag{15}$$

for n-channel transistors. The integration of both sides of Eq. (11) from $y = 0$ to $y = L$ (L being the channel length) will yield the final answer: an explicit expression for the drain current as a function of the drain and gate voltages.

The main differences among these analytical models [57–64] are in their solutions to the two-dimensional Poisson's equation, Eq. (6). The complexity of this equation makes an exact analytical solution impossible. Either numerical methods or analytical approximations must be employed to reduce the problem to a manageable level. Depp *et al.* [57,58] and Colinge *et al.* [59,60] have chosen the numerical approach by doing all the calculations on a computer. Fossum and Ortiz-Conde [61,62] and Anwar and Khondker [63,64] have chosen the analytical approach by making approximations to reduce both the Poisson's equation and the boundary conditions. The result, in each case, is an excellent agreement between the theory and the experiment. However, in each case, such an excellent agreement is barely surprising given large number of model parameters that can be varied to fit the data points!

We will now wrap up this discussion by pointing out *the similarities as well as the differences* between what these models [57–64] have contributed and what

we have contributed to the understanding of polycystalline silicon thin-film transistors. Our work is similar to their work in the sense that we have all identified both the grain-boundary effect and the surface effect as the dominant factors in controlling TFT performance. Our work differs from their work, however, in that while they have focused on the grain-boundary effect, we have focused on both the grain-boundary and the surface effects. What we have demonstrated, experimentally for the first time ever, is the fact that when the average grain size becomes sufficiently large (of the order of 1–2 μm), the surface effect can become a more dominant factor than the grain-boundary effect in controlling TFT performance. This demonstration re-focuses the spotlight on the surface effect, and may have a significant impact on the design and optimization of the future generations of polycrystalline silicon TFT's.

REFERENCES

1. See, for example, the various related articles, and the references therein, published in the *Materials Research Society Symposia Proceedings*, (Materials Research Society, Pittsburgh, from 1981).

2. J. R. Troxell, M. I. Harrington, J. C. Erskine, W. H. Dumbaugh, F. P. Fehlner, and R. A. Miller, "Polycrystalline silicon thin-film transistors on a novel 800°C glass substrate", *IEEE Electron Dev. Lett. EDL-7*, 597 (1986).

3. E. W. Maby, M. W. Geis, Y. L. LeCoz, D. J. Silversmith, R. W. Mountain, and D. A. Antoniadis, "MOSFET's on silicon prepared by moving melt zone recrystallization of encapsulated polycrystalline silicon on an insulating substrate", *IEEE Electron Dev. Lett. EDL-2*, 241 (1981).

4. G. Poullain, B. Mercey, and G. Nouet, "Conductance of silicon grain boundaries in as-grown and annealed bicrystals", *J. Appl. Phys. 61*, 1547 (1987).

5. S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), Chap. 8.

6. L. Csepregi, E. F. Kennedy, J. Mayer, and T. W. Sigmon, "Substrate-orientation dependence of the epitaxial regrowth rate from Si-implanted amorphous Si", *J. Appl. Phys. 49*, 3906 (1978).

7. R. Reif and J. E. Knott, "Low-temperature process to increase the grain size in polysilicon films", *Electron. Lett. 17*, 586 (1981).

8. P. Kwizera and R. Reif, "Solid phase epitaxial recrystallization of thin polycrystalline films amorphized by silicon ion implantation", *Appl. Phys. Lett. 41*, 379 (1982).

9. P. Kwizera and R. Reif, "Annealing behavior of thin polycrystalline silicon films damaged by silicon ion implantation in the critical amorphization range", *Thin Solid Films 100*, 227 (1983).

10. R. B. Iverson and R. Reif, "Modifying polycrystalline films through ion channeling", *Mat. Res. Soc. Symp. Proc. 27*, 543 (1984).

11. R. B. Iverson and R. Reif, "Stochastic model for grain size versus dose in implanted and annealed polycrystalline silicon films on SiO_2", *J. Appl. Phys. 57*, 5169 (1985).

12. K. T-Y. Kung, R. B. Iverson, and R. Reif, "Seed selection through ion channeling to produce uniformly oriented polycrystalline Si films on SiO_2", *Mat. Lett. 3*, 24 (1984).

13. K. T-Y. Kung, R. B. Iverson, and R. Reif, "Seed selection through ion channeling to modify crystallographic orientations of polycrystalline Si films on SiO_2: Implant angle dependence", *Appl. Phys. Lett. 46*, 683 (1985).

14. T. I. Kamins, M. M. Mandurah, and K. C. Saraswat, "Structure and stability of low pressure chemically vapor-deposited silicon films", *J. Electrochem. Soc. 125*, 927 (1978).

15. T. I. Kamins, "Structure and properties of LPCVD silicon films", *J. Electrochem. Soc. 127*, 686 (1980).

16. K. T-Y. Kung and R. Reif, "Implant-dose dependence of grain size and {110} texture enhancements in polycrystalline Si films by seed selection through ion channeling", *J. Appl. Phys. 59*, 2422 (1986).

17. K. T-Y. Kung and R. Reif, "Polycrystalline Si thin-film transistors fabricated at $\leq$ 800°C: Effects of grain size and {110} fiber texture", *J. Appl. Phys. 62*, 1503 (1987).

18. L. C. Feldman, J. W. Mayer, and S. T. Picraux, *Materials Analysis by Ion Channeling: Submicron Crystallography* (Academic, New York, 1982), pp. 16,17.

19. J. F. Gibbons, "Ion implantation in semiconductors — Part II: Damage production and annealing", *Proc. IEEE 60*, 1062 (1972).

20. J. Narayan, D. Farhy, O. S. Oen, and O. W. Holland, "Atomic structure of ion implantation damage and process of amorphization in semiconductors", J. Vac. Sci. Technol. A 2, 1303 (1984).

21. D. K. Brice, "Recoil contribution to ion-implantation energy-deposition distributions", *J. Appl. Phys. 46*, 3385 (1975).

22. N. A. Blum and C. Feldman, "The crystallization of amorphous silicon films", *J. Non-Cryst. Solids 11*, 242 (1972).

23. See, for example, the various related articles, and the references therein, published in *Polycrystalline and Amorphous Thin Films and Devices*, L. L. Kazmerski, ed. (Academic, New York, 1980).

24. P. K. Weimer, H. Borkan, G. Sadasiv, L. Meray-Horvath, and F. V. Shallcross, "Integrated circuits incorporating thin-film active and passive elements", *Proc. IEEE 52*, 1479 (1964).

25. T. P. Brody, J. A. Asars, and G. D. Dixon, "A 6 $\times$ 6 inch 20 lines-per-inch liquid-crystal display panel", *IEEE Trans. Electron Dev. ED-20*, 995 (1973).

26. G. W. Neudeck and A. K. Malhotra, "An amorphous silicon thin film transistor: Theory and experiment", *Solid-State Electron. 19*, 721 (1976).

27. A. J. Snell, W. E. Spear, P. G. LeComber, and K. Mackenzie, "Application of amorphous silicon field effect transistors in integrated circuits", *Appl. Phys. A26*, 83 (1981).

28. M. Matsumura and H. Hayama, "Amorphous-silicon integrated circuit", *Proc. IEEE 68*, 1349 (1980).

29. M. J. Thompson and H. C. Tuan, "Amorphous Si electronic devices and their applications", *IEDM Tech. Dig.*, 192 (1986).

30. K. T-Y. Kung and R. Reif, "Comparison of thin-film transistors fabricated at low temperatures ($\leq$ 600°C) on as-deposited and amorphized-crystallized polycrystalline Si", *J. Appl. Phys. 61*, 1638 (1987).

31. K. T-Y. Kung and R. Reif, "Surface effect as a limitation on the performance of polycrystalline Si thin-film transistors", *J. Appl. Phys.* (to be published).

32. T. Noguchi, H. Hayashi, and T. Ohshima, "Low temperature polysilicon super-thin-film transistor (LSFT)", *Jpn. J. Appl. Phys. 25*, L121 (1986).

33. T. Ohshima, T. Noguchi, and H. Hayashi, "A super thin film transistor in advanced poly Si films", *Jpn. J. Appl. Phys. 25*, L291 (1986).

34. L. J. van der Pauw, "A method of measuring specific resistivity and Hall effect of discs of arbitrary shape", *Philips Res. Rep. 13*, 1 (1958).

35. C. P. Ho and S. E. Hansen, "SUPREM III — A program for integrated circuit process modeling and simulation", Technical Report No. SEL83-001, Stanford Electronics Laboratories, Stanford University, Stanford, CA (1983).

36. T. I. Kamins, "Hall mobility in chemically deposited polycrystalline silicon", *J. Appl. Phys. 42*, 4357 (1971).

37. J. Y. W. Seto, "The electrical properties of polycrystalline silicon films", *J. Appl. Phys. 46*, 5247 (1975).

38. B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, "Characteristics of the surface-state charge (Q_{ss}) of thermally oxidized silicon", *J. Electrochem. Soc. 114*, 266 (1967).

39. B. E. Deal, E. L. MacKenna, and P. L. Castro, "Characteristics of fast surface states associated with SiO_2-Si and Si_3N_4-SiO_2-Si structures", *J. Electrochem. Soc. 116*, 997 (1969).

40. S. C. Sun and J. D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces", *IEEE Trans. Electron Dev. ED-27*, 1497 (1980).

41. S. Onga, Y. Mizutani, K. Taniguchi, M. Kashiwagi, K. Shibata, and S. Kohyama, "Characterization of polycrystalline silicon MOS transistors and its film properties. I", *Jpn. J. Appl. Phys. 21*, 1472 (1982).

42. R. M. Anderson and D. R. Kerr, "Evidence for surface asperity mechanism of conductivity in oxide grown on polycrystalline silicon", *J. Appl. Phys. 48*, 4834 (1977).

43. H. S. Lee and S. P. Marin, "Electrode shape effects on oxide conduction in films thermally grown from polycrystalline silicon", *J. Appl. Phys. 51*, 3746 (1980).

44. R. B. Marcus, T. T. Sheng, and P. Lin, "Polysilicon/SiO_2 interface microstructure and dielectric breakdown", *J. Electrochem. Soc. 129*, 1282 (1982).

45. C. T. Sah and F. H. Hielscher, "Evidence of the surface origin of the *1/f* noise", *Phys. Rev. Lett. 17*, 956 (1966).

46. G. Abowitz, E. Arnold, and E. A. Leventhal, "Surface states and *1/f* noise in MOS transistors", *IEEE Trans. Electron Dev. ED-14*, 775 (1967).

47. S. T. Hsu, D. J. Fitzgerald, and A. S. Grove, "Surface-state related *1/f* noise in *p-n* junctions and MOS transistors", *Appl. Phys. Lett. 12*, 287 (1968).

48. S. Christensson, I. Lundstrom, and C. Svensson, "Low frequency noise in MOS transistors — I Theory", *Solid-State Electron. 11*, 797 (1968); S. Christensson and I. Lundstrom, "Low frequency noise in MOS transistors — II Experiments", *Solid-State Electron. 11*, 813 (1968).

49. P. Germain, S. Squelard, J. Bourgoin, and A. Gheorghiu, "Crystallization kinetics of amorphous germanium", *J. Appl. Phys. 48*, 1909 (1977).

50. K. Zellama, P. Germain, S. Squelard, J. C. Bourgoin, and P. A. Thoman, "Crystallization in amorphous silicon", *J. Appl. Phys. 50*, 6995 (1979).

51. E. J. Korma, K. Visser, J. Snijder, and J. F. Verwey, "Fast determination of the effective channel length and the gate oxide thickness in polycrystalline silicon MOSFET's", *IEEE Electron Dev. Lett. EDL-5*, 368 (1984).

52. D. W. Greve and V. R. Hay, "Interpretation of capacitance-voltage characteristics of polycrystalline silicon thin-film transistors", *J. Appl. Phys. 61*, 1176 (1987).

53. J. G. Fossum, A. Ortiz-Conde, H. Shichijo, and S. K. Banerjee, "Anomalous leakage current in LPCVD polysilicon MOSFET's", *IEEE Trans. Electron Dev. ED-32*, 1878 (1985).

54. S. K. Madan and D. A. Antoniadis, "Leakage current mechanisms in hydrogen-passivated fine-grain polycrystalline silicon on insulator MOSFET's", *IEEE Trans. Electron Dev. ED-33*, 1518 (1986).

55. A. Ortiz-Conde and J. G. Fossum, "Subthreshold behavior of thin-film LPCVD polysilicon MOSFET's", *IEEE Trans. Electron Dev. ED-33*, 1563 (1986).

56. B. Faughnan, "Subthreshold model of a polycrystalline silicon thin-film field-effect transistor", *Appl. Phys. Lett. 50*, 290 (1987).

57. S. W. Depp, A. Juliana, and B. G. Huth, "Polysilicon FET devices for large area input/output applications", *IEDM Tech. Dig.*, 703 (1980).

58. S. W. Depp, B. G. Huth, A. Juliana, and R. W. Koepcke, "Theory of MOSFET operation in small-grain polysilicon", *Mat. Res. Soc. Symp. Proc. 5*, 297 (1982).

59. J.-P. Colinge, E. Demoulin, and H. Morel, "Field-effect in large grain polysilicon transistors", *IEDM Tech. Dig.*, 444 (1982).

60. J.-P. Colinge, H. Morel, and J.-P. Chante, "Field effect in large grain polycrystalline silicon", *IEEE Trans. Electron Dev. ED-30*, 197 (1983).

61. J. G. Fossum and A. Ortiz-Conde, "Effects of grain boundaries on the channel conductance of SOI MOSFET's", *IEEE Trans. Electron Dev. ED-30*, 933 (1983).

62. J. G. Fossum and A. Ortiz-Conde, "Effects of grain boundaries on the current-voltage characteristics of SOI MOSFET's", *Mat. Res. Soc. Symp. Proc. 33*, 199 (1984).

63. A. G. M. Anwar and A. N. Khondker, "An analytical model for the threshold voltage of polysilicon MOSFET's", *Mat. Res. Soc. Symp. Proc. 53*, 441 (1986).

64. A. G. M. Anwar and A. N. Khondker, "A model for polysilicon MOSFET's", *IEEE Trans. Electron Dev. ED-34*, 1323 (1987).