

**Efficient Silicon Micro-Reactors for
Thermophotovoltaic Applications**

by

Mohammad Araghchini

Submitted to the Department of Electrical Engineering and Computer
Science

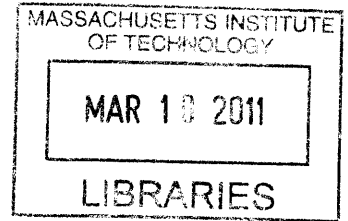
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Abstract

Thermophotovoltaic (TPV) systems passively generate electricity from the combustion of fuel. Although TPV conversion systems have advantages, they suffer from low efficiency.

This thesis investigates different ways to increase the efficiency of TPV systems. In particular the thesis details micro-fabrication of silicon micro-reactors, and two-dimensional tungsten photonic crystals (2D W PhC) for high-temperature applications such as selective thermal emitters for TPV energy conversion. Interference lithography and reactive ion etching are used to produce large-area single-crystal tungsten 2D PhC's. The fabricated PhC consists of an array of cylindrical cavities with 800nm diameter, 1.2 μm depth, and 1.2 μm period. Extensive characterization and calibration of all micro-fabrication steps for both micro-reactors and 2D PhC's are presented. Experimentally-obtained thermal emission spectra of the 2D PhC structures match well with numerical predictions.

Thesis Supervisor: Leslie Kolodziejwski
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Contents

1	Introduction	15
1.1	Motivation	15
1.2	Thesis Organization	18
2	Silicon Micro-Reactors	19
2.1	Silicon Nitride Hard Masks	20
2.2	Etching Silicon	22
2.3	Bonding and Annealing	23
2.4	Improving Bonding Quality	23
2.5	Fabrication Results	24
3	Increasing Efficiency Using Photonic Crystal Structures	27
3.1	1D Photonic Crystal Structures	27
3.1.1	Design and Simulation	27
3.2	2D Photonic Crystal Structures	29
4	Fabrication of 2D PhC structure	33
4.1	Lithography	33
4.2	Etching	39
4.2.1	ARC Etching	39
4.2.2	Chromium Etching	40
4.2.3	Tungsten Etching	42
4.3	Characterization	42

5	Micro-reactor Packaging and Testing	47
5.1	Loading Catalyst	47
5.2	Glass Brazing	48
5.3	Efficiency Measurement	49
6	Conclusion and Future Works	53
6.1	Future Works	53
A	Fabrication Process	55
B	2D Tungsten PhC Integration Process	57

List of Figures

1-1	The basic mechanism in a TPV system	15
1-2	Emitted Power vs. wavelength for Gallium Antimonide	16
1-3	Schematic of the designed TPV system	16
2-1	Summary of micro-reactors fabrication process	19
2-2	The mask used for the interface of a pair of wafers.	20
2-3	Fabrication process for creating silicon nitride hard masks	21
2-4	Alignment and diesaw marks needed on silicon nitride mask on back-side of the wafers.	22
2-5	Silicon channels etched before SiN removal and after KOH etch, (a) after 5 hrs and (b) after 6.5 hrs.	23
2-6	(a) Silicon wafer with silicon nitride mask on both sides, (b) removing silicon nitride mask in hot phosphoric acid, and (c) bonding and annealing wafers.	24
2-7	The IR image of a bonded pair with (a) high-quality bonding and (b) low-quality bonding	25
2-8	The IR image of a bonded pair (a) before the bonding improvement process and (b) after the improvement process.	25
2-9	Optical image of a wafer after striping the silicon nitride	26
3-1	Three one-dimensional structures as selective emitters: (a) a polished Si wafer, (b) a polished Si wafer with 4-bilayers of Si/SiO ₂ , and (c) a polished Si wafer with a metal layer (tungsten or platinum) on top of Si, and 4-bilayer Si/SiO ₂ structure on top of the metal layer.	28

3-2	Spectral emittance of four structures at 1000 K: a polished Si wafer, a polished Si wafer with 4-bilayer of Si/SiO ₂ , a polished Si wafer with tungsten and 4-bilayer Si/SiO ₂ PhC, and a platinum wafer with 3-bilayer 1D PhC.	29
3-3	SEM images of the 2D single crystalline W grating with period of 1.0 μm	30
4-1	General process flow for 2D tungsten photonic crystal structures. . .	34
4-2	Schematics of the laser interference lithography used in exposing the photoresist.	34
4-3	Anti-Reflection-Coating thickness calculation	35
4-4	Interference Lithography mechanism: Two plane waves produces a standing wave which is imaged into the photoresist	36
4-5	SEM images of the developed patterns in the photoresist for different exposure times, whereby the laser power is 170 μW at the sample plane.	38
4-6	The resist profile far below (left) and above (right) the crossover dose for a positive photoresist.	38
4-7	Square-Shape rods and holes	38
4-8	SEM image of sideview of the developed photoresist	39
4-9	SEM image showing successful pattern transfer to the anti-reflection coating after undergoing an oxygen-based reactive ion etching at 140 W for 3 minutes 30 seconds.	40
4-10	SEM images demonstrating the control of etch times to obtain the desired circular hole diameter on the Chromium mask.	41
4-11	Chrome mask deposited at (a) room temperature and (b) high temperature (250 °C)	41
4-12	SEM image of a 2D PhC structure in an e-beam-deposited tungsten sample	43
4-13	(a) SEM image of a 2D PhC structure in a single-crystal tungsten wafer and (b) Cross sectional profile mapped using an AFM.	44

4-14	A marked enhancement is seen in the emissivity of the 2D W PhC at wavelengths below $1.7\mu\text{m}$	45
5-1	The cross-section of micro-reactors before and after loading catalyst .	48
5-2	Glass tubes brazed to the micro-reactos	48
5-3	Micro-reactor measurement setup	49
5-4	Avarage temperature on the micro-reactor vs the input heat power . .	50
5-5	Electric power and fuel-to-electricity efficiency for a micro-reactor chip sample vs the butane input power.	51

List of Tables

3.1	Predicted efficiency, power generation, and overall product figure of merit values for multiple mTPV emitter designs at 1000 K [view factor $F = 0.4$	28
4.1	Different RIE etch parameters and their effects on etch rate and mask damage.	42
A.1	Part 1: Deposit SiN	55
A.2	Part 2: Pattern Nitride	56
A.3	Part 3: KOH Etch Channels	56
A.4	Part 4: Bond Wafers	56
B.1	Part 1: Deposit SiN	57
B.2	Part 2: Resist Lithography	57
B.3	Part 3: Nitride mask patterning and resist removal	57
B.4	Part 4: Pattern Silicon	58
B.5	Part 5: Lithography of the interface sides	58
B.6	Part 6: KOH Etch Channels	58
B.7	Part 7: Bond Wafers	58
B.8	Part 8: Tungsten Deposition	59
B.9	Part 9: Dice Wafers	59

Chapter 1

Introduction

1.1 Motivation

Thermophotovoltaic (TPV) systems passively generate electricity from the combustion of fuel [1, 2, 3]. A basic TPV system (as shown in Fig. 1-1) consists of a thermal emitter, which turns the provided heat into radiation of photons, and a photovoltaic (PV) diode (or cell) to convert thermal radiation into free charge carriers and electric current. Although TPV conversion systems have advantages including an absence of moving parts, long lifetime and low maintenance, TPV systems suffer from low efficiency [3, 4, 2]. A review of previous TPV systems can be found in Ref. [3].

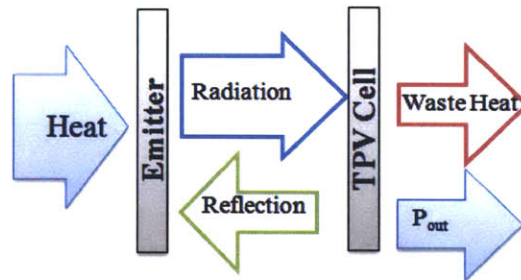


Figure 1-1: The basic mechanism in a TPV system

TPV cells are characterized by a bandgap. Photons with energies lower than the semiconductor bandgap used in the TPV cell cannot be converted into electricity.

Fig. 1-2 shows the emittance spectrum versus wavelength for different emitter temperatures, and the relevant power densities and efficiencies, using a Gallium Antimonide TPV cell.

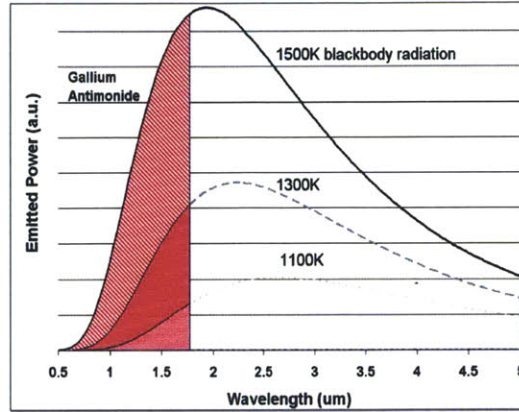


Figure 1-2: Emitted Power vs. wavelength for Gallium Antimonide (Figure by Adrian Yang)

In order to achieve high TPV efficiencies, it is necessary to have high temperature emitters. Also, we need to better match the emitted spectrum to the sensitivity spectrum of the TPV cell.

Fig. 1-3 shows a schematic of the designed TPV system. The red part shows the silicon micro-reactor. TPV cells (shown with pink color) are placed under and above the micro-reactor.

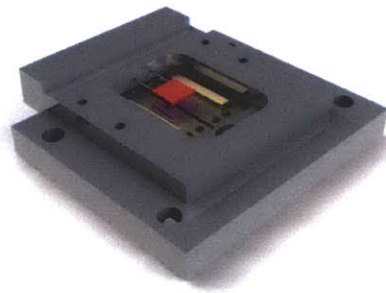


Figure 1-3: Schematic of the designed TPV system. (figure sketched by Walker Chan)

The efficiency of TPV systems includes three main components:

- 1. Efficiency of the chemical reaction in the TPV reactor:** In order to increase this efficiency, several tests with different chemical reactions can be considered by using different combustible fuels such as propane or butane.
- 2. Efficiency of thermal radiation (i.e. heat to desired radiation spectrum efficiency):** As discussed before, TPV cells are characterized by a bandgap and photons with energy lower than the bandgap cannot be converted to electricity. In order to have high efficiency TPV systems, it is important to better match the emitted spectrum to the sensitivity spectrum of the TPV cell. Several designs and structures on top of the silicon micro-reactor can be used to shape the radiation spectrum as desired.
- 3. Thermal efficiency of the reactor:** There are three pathways for the heat loss: conduction, convection, and radiation. In order to increase the total efficiency of the reactor, there needs to be an increase of radiation in the desired part of the spectrum (as discussed above in 2). Convection and conduction losses also need to be suppressed.

Heat loss is directly proportional to conductivity of the material and cross-sectional area of the tubes and is inversely proportional to the length that heat will pass. Thus, materials with low-thermal conductivity are used for the inlet and outlet tubes of the micro-reactor. Also according to Fourier's Law, thin-walled and long tubes are desirable. Suppressing convective losses can be achieved by packaging the reaction zone in a vacuum.

This thesis will mainly focus on increasing thermal radiation efficiency and the thermal efficiency of the reactor. In order to have higher thermal radiation efficiencies, one can explore spectral control via selective emission. In particular, three approaches will be discussed:

- 1- Using a multilayer structure integrated on top of the thermal emitter that includes

Silicon/Silicon Dioxide bilayers.

2- Using a multilayer structure that includes an optically thick metallic layer such as Platinum and Silicon/Silicon Oxide bilayers that can theoretically give us higher efficiencies compared to the previous structure.

3- Using two-dimensional (2D) tungsten (W) Photonic Crystal (PhC) that can withstand temperatures over 1000K.

Thin-walled and low-conductive tubes were used to suppress conduction losses and to suppress convection losses vacuum packaging of the system can be considered.

1.2 Thesis Organization

In Chapter 2, the details of the fabrication process of silicon micro-reactors are discussed. Chapter 3 investigates different designs and simulations mainly carried out by Peter Bermel. In Chapter 3.2 a review of previous work describing the fabricating 2D PhC structures for high temperature applications is given. Chapter 4 details the fabrication process of the 2D PhC structures. In Chapter 5, measurement results for the whole TPV system (e.g. fuel-to-electricity efficiency) are shown. Finally in Chapter 6, the conclusion and future work are discussed.

Chapter 2

Silicon Micro-Reactors

A major part of this project is fabricating silicon micro-reactors capable of high temperature fuel-reforming reactions. Fig. 2-1 shows the summary of the fabrication process. A 6 inch silicon wafer (a) is etched using a nitride mask to make the desired channels (b). The wafers are then bounded to create the final micro-reactor (c).

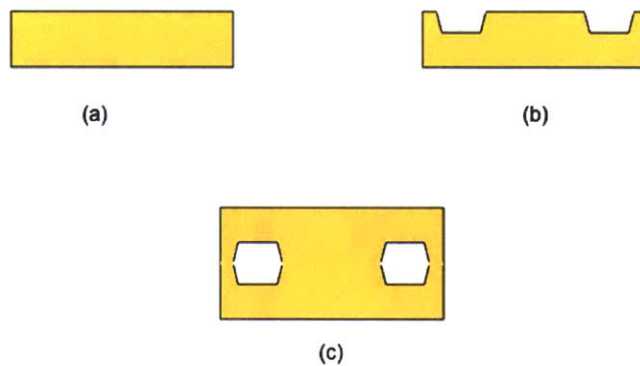


Figure 2-1: (a) 6 inch diameter wafer, (b) Using nitride mask and silicon wet etching, desired channels on each wafer are made (c) the wafers are bounded

Appendix A details the fabrication process. Fabrication of these reactors involves three main steps:

1. fabricating silicon nitride hard masks used for making channels in which gas combustion occurs,
2. etching silicon wafers to shape the channels on each wafer, and

3. bonding and annealing of the wafers.

In this process, a wet etch process is used for etching the silicon. Wet etching has advantages compared to deep reactive ion etching (DRIE), such as low cost and compatibility with batch processing, but wet etching limits the channel geometry. In fact, by using wet etching, channels with aspect ratio of almost 1:1 can be yielded. In the next sections of this chapter, each step of the fabrication process is discussed with more detail.

2.1 Silicon Nitride Hard Masks

In the fabrication of micro-reactors, one mask is needed for patterning the interface layer of two wafers (i.e. for patterning the channels) and another mask is needed for the outer side of the reactors to pattern alignment and diesaw marks. Fig. 2-2 shows the mask needed for the interface of two wafers, which is initially patterned on top of all wafers.

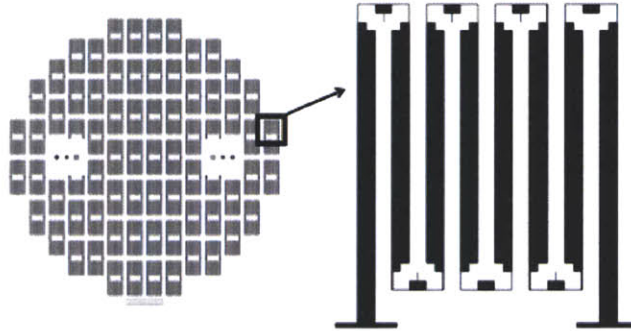


Figure 2-2: The mask used for the interface of a pair of wafers. This mask is used for patterning and etching channels in silicon wafers.

Fig. 2-3 shows the fabrication steps of nitride hard masks. The process starts with two 150 mm (100-oriented), 650 μm thick, double-side-polished (DSP) silicon wafers. RCA cleaning is needed before the silicon nitride deposition. A 250 nm length of low-stress Low-pressure chemical vapor deposition (LPCVD) silicon nitride is deposited on both sides of the wafer. Fig. 2-3 shows the process for only one side of the wafer.

Next, the silicon nitride is coated with 1 μm of OCG-825 photoresist. The resist is exposed to ultraviolet (UV) light at 360 nm for 2.5 seconds. Next, the resist is developed in OCG 934 1:1 for 1 minute and the sample is post baked at 120 °C for 30 minutes.

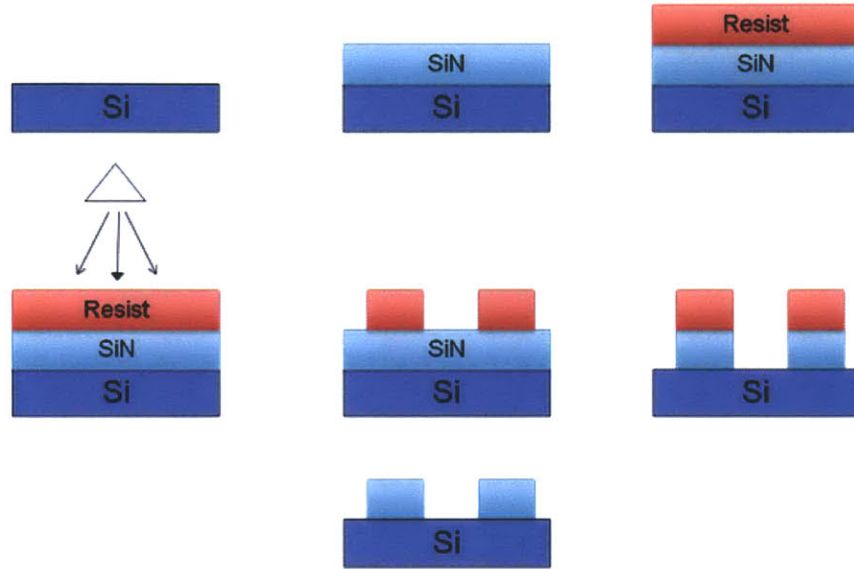


Figure 2-3: Fabrication process for creating silicon nitride hard masks.

Next by using SF_6 (190 sccm flow rate) and Oxygen (19 sccm flow rate) in an RIE chamber the nitride layer is etched at a rate of 1000 Å/min. Finally, the resist is removed using oxygen in a high-plasma asher. Ashing time of 2 min/wafer is needed in a single wafer chamber asher with 3.75 Torr, and 400 W plasma, with a chuck temperature of 220 °C. A final piranha (a mixture of sulfuric acid and hydrogen peroxide) clean step for 10 minutes is used on all wafers.

In order to align the wafers in the bonding step and to cut and separate the chips for each bonded pair, alignment marks and diesaw marks are patterned on the backside of the wafers.

Fig. 2-4 shows the mask used for the backside patterning of the wafers, which

include aligning marks and diesaw marks.

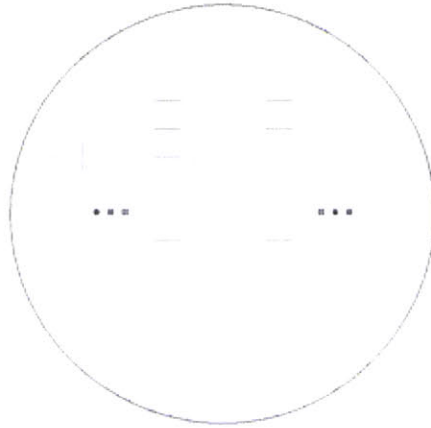


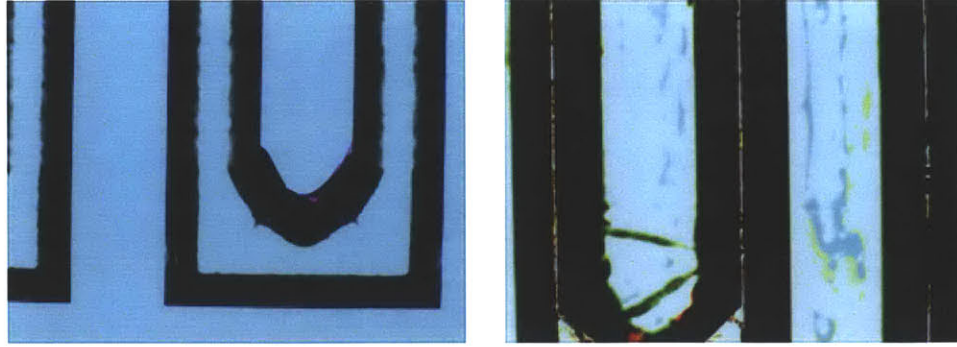
Figure 2-4: Alignment and diesaw marks needed on silicon nitride mask on the backside of the wafers.

A similar process, as described in Fig. 2-3, is used for backside mask fabrication.

2.2 Etching Silicon

The patterned silicon nitride layer serves as a hard mask for the silicon etching step. Compared to DRIE, wet etching has the advantages of parallel processing of wafers and lower cost. Here, a 25% KOH solution at 80 °C is used to etch silicon. Different etching times are tested and it is observed that after about 6.5 hours, the etching process of the channels automatically ends.

Fig. 2-5 shows optical images of the top view of the channels in silicon after KOH wet etching. As shown in Fig. 2-5 b, after 6.5 hours the sidewalls of the channel (black feature) almost reach each other, and the etching process stops.



(a)

(b)

Figure 2-5: Silicon channels etched before SiN removal and after KOH etch, (a) after 5hrs and (b) after 6.5 hrs.

2.3 Bonding and Annealing

After the KOH wet etching step, the wafers are subjected to a cleaning process. This includes rinsing the wafers thoroughly with DI water and two 10-minute piranha cleaning steps. This cleaning process removes all residual fragments of silicon. Silicon nitride mask is then removed using hot phosphoric acid. The acid temperature is 165 C, and its silicon nitride etch rate for low-stress nitride, deposited by LPCVD, is 4 nm/minute.

After removing the silicon nitride mask, the bonding process is started. The wafers are first placed in 49% HF solution for 5 minutes and rinsed. Next, the wafers are RCA cleaned, leaving out the one-minute intermediate HF dip step. The wafers are then fusion bonded using an aligner and bonder. In order to anneal the bonded wafers, they are placed in 1100°C oven with flowing nitrogen gas for 2 hours. Fig. 2-6 summarizes the fabrication steps after the KOH wet etching step.

2.4 Improving Bonding Quality

After bonding the wafers, an IR camera is used to investigate the bonding quality. One can observe fringes, if there is a gap between the two wafers, i.e. if the wafers

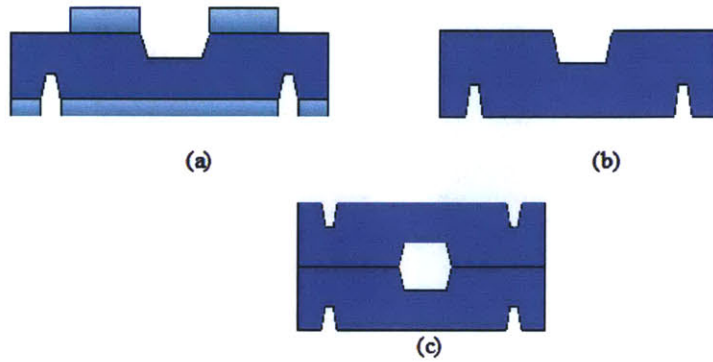


Figure 2-6: (a) Silicon wafer with silicon nitride mask on both sides, (b) removing silicon nitride mask in hot phosphoric acid, and (c) bonding and annealing wafers.

are not bonded well. Fig. 2-7(a) shows a high-quality bonded pair, in which there are no obvious fringes. However in Fig. 2-7(b) one can observe fringes due to the gap between the two wafers, which shows poor and low-quality bonding.

In an attempt to improve the bonding quality of the pairs that have not been bonded well, a couple of tests were done on the bonded pairs by applying pressure and heat.

Fig. 2-8 shows the IR image of a bonded pair before the extra bonding process and after this process. In this process, the wafers were held under pressure at 350°C for one hour in vacuum. The fringes in Fig. 2-8(a) show the low quality of the bonding and the existence of a gap between the two wafers before the bonding improvement process. Fig. 2-8(b) shows the same pair of wafers after undergoing an improvement process, which includes applying pressure and heat for 1 hour.

2.5 Fabrication Results

Fig. 2-9 shows the optical image of a wafer after removing the nitride hard mask and before bonding and annealing.

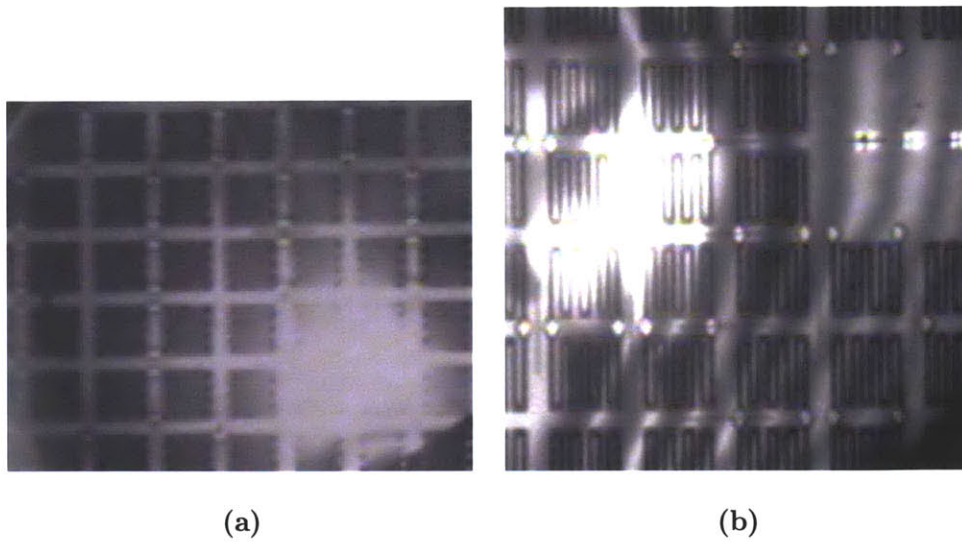


Figure 2-7: The IR image of a bonded pair with (a) high-quality bonding. There are no fringes in the image of the bonded wafer, which indicates that the wafers are bonded well. (b) Low-quality bonding: one can observe fringes in the image, which is due to the gap between the two wafers.

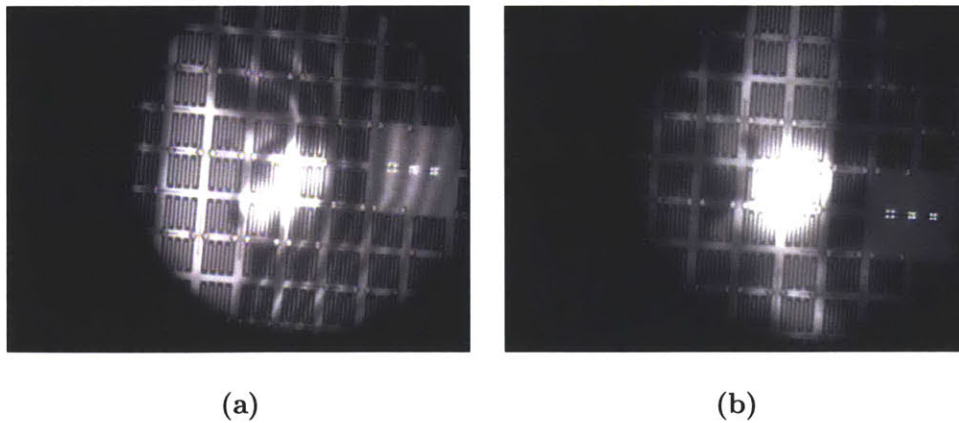


Figure 2-8: The IR image of a bonded pair (a) before the bonding improvement process and (b) after the improvement process.

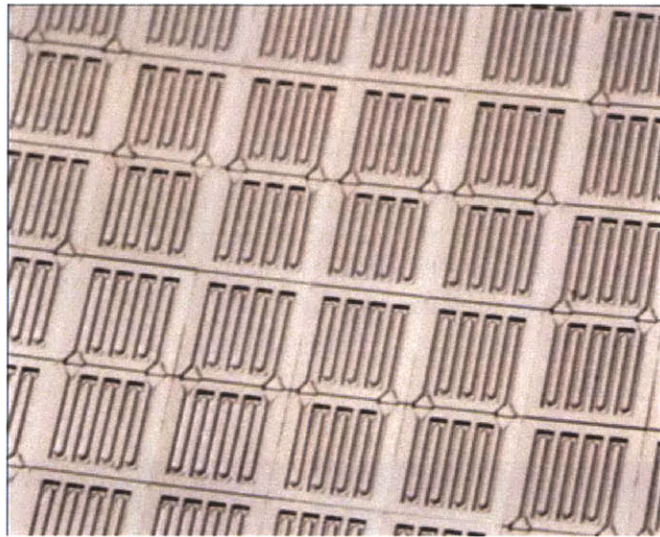


Figure 2-9: Optical image of a wafer after stripping the silicon nitride.

Chapter 3

Increasing Efficiency Using Photonic Crystal Structures

3.1 1D Photonic Crystal Structures

3.1.1 Design and Simulation

In order to optimize the efficiency of a TPV system, several designs are investigated and optimized theoretically by Peter Bermel and Michael Ghebrebrhan. These designs use one-dimensional (1D) and two-dimensional (2D) structures on top of the micro-reactors. The theoretical methods used for the design of these structures are discussed in details in Ref [5].

Fig. 3-1 (adopted from Ref [5]) shows three 1D structures on top of the silicon. The various structures include a polished Si wafer, a polished Si wafer with 4-bilayers of Si/SiO₂, and a polished Si wafer with a metal layer (tungsten or platinum) on top of Si, and a 4-bilayer Si/SiO₂ structure on top of the metal layer.

In Table 3.1, these designs are compared in terms of the predicted efficiency, power generation and overall product figure of merit values (adopted from Ref. [5]).

Fig. 3-2 (adopted from [5]) compares the spectral emittance of a polished Si wafer [Fig. 3-1(a)], a polished Si wafer with 4-bilayer of Si/SiO₂ on top of that [Fig. 3-1(b)], a polished Si wafer with tungsten and 4-bilayer Si/SiO₂ PhC similar to Fig. 3-1(c),

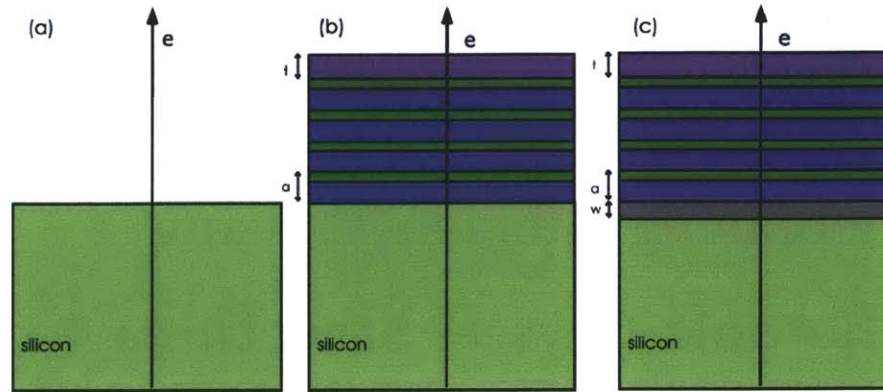


Figure 3-1: Three one-dimensional structures as selective emitters: (a) a polished Si wafer, (b) a polished Si wafer with 4-bilayers of Si/SiO₂, and (c) a polished Si wafer with a metal layer (tungsten or platinum) on top of Si, and 4-bilayer Si/SiO₂ structure on top of the metal layer (Figure adopted from Ref. [5])

Table 3.1:]

Predicted efficiency, power generation, and overall product figure of merit values for multiple TPV emitter designs at 1000 K [view factor $F = 0.4$](values adopted from Ref. [5])

Design	Power Generation	Efficiency	Figure of merit
plain silicon wafer	67.77 mW	0.975%	0.6607
Si wafer + 4 Si/SiO ₂ bilayers	83.91 mW	2.042%	1.713
Si wafer + W + 4 Si/SiO ₂ bilayers	69.01 mW	2.912%	2.010
Pt wafer + 2 Si/SiO ₂ bilayers	48.85 mW	5.289%	2.584

and a platinum wafer with 3-bilayer 1D PhC similar to Fig. 3-1(c).

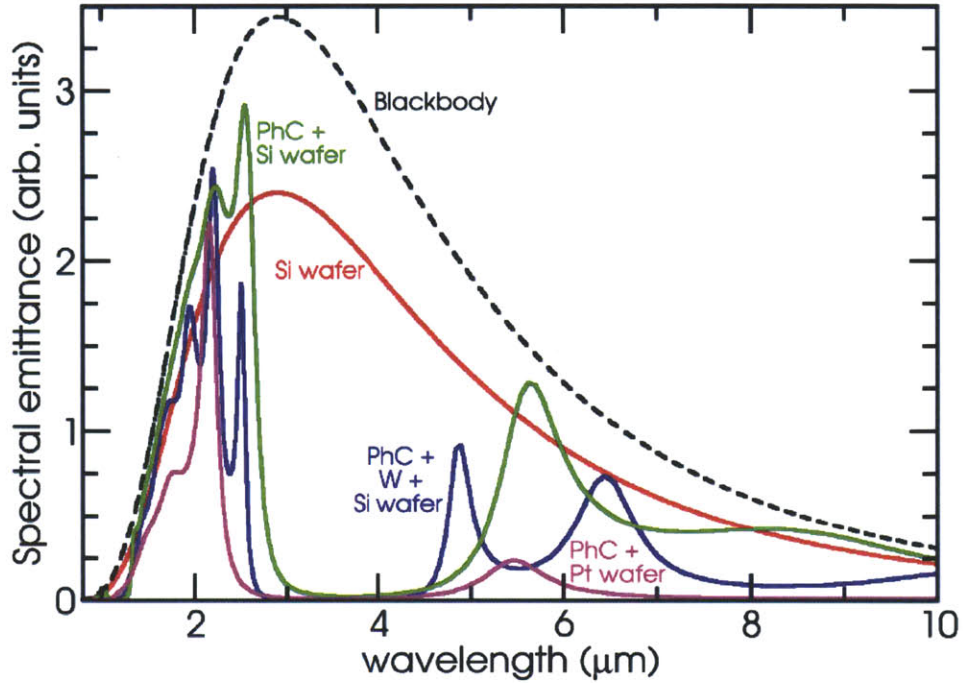


Figure 3-2: Spectral emittance of four structures at 1000 K: a polished Si wafer, a polished Si wafer with 4-bilayer of Si/SiO₂, a polished Si wafer with tungsten and 4-bilayer Si/SiO₂ PhC, and a platinum wafer with 3-bilayer 1D PhC. (Figure adopted from Ref. [5]) The efficiency, power, and overall figure of merit for each structure is listed in Table. 3.1

3.2 2D Photonic Crystal Structures

Two-dimensional metallic photonic crystals show large promise as high-performance selective thermal emitters for thermophotovoltaic energy conversion, solar-thermophotovoltaics, radioisotope-thermophotovoltaic power generators [6], and solar absorbers/reflectors [7]. Several papers have been published on different designs of tungsten (W) PhC's as selective thermal emitters [8, 9, 10, 11].

In particular, references [10, 11] reported the design and fabrication of an array of square cavities in tungsten. Fig. 3-3 from Ref [10] shows an SEM image of a 2D

single crystalline W sample.

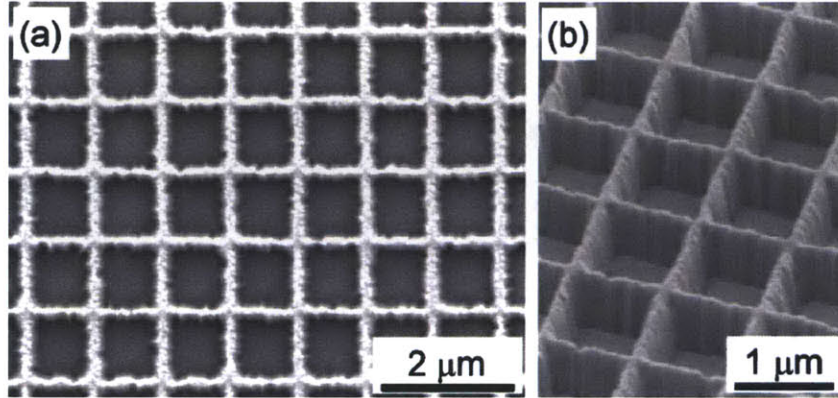


Figure 3-3: SEM images of the 2D single crystalline W grating with period of $1.0 \mu\text{m}$. (a) Top view. (b) Oblique view. Figure from Ref[10]

However, an expensive and time consuming fabrication technique based on e-beam lithography and fast atom beam etching is used to fabricate these structures. A different selective emitter has also been reported by [8, 9] based on a 3D W woodpile stack design. This design also suffers from an expensive and complex layer-by-layer fabrication method.

In contrast, this work presents a different approach towards fabrication of selective broadband emitters, based on interference lithography and reactive ion etching. This process is relatively simple, efficient, and scalable while employing standard micro- and nano-fabrication techniques. Indeed this design is based on a two-dimensional tungsten photonic crystal consisting of a square array of cylindrical holes. Key design parameters that determine thermal emission cut-off and selectivity are PhC periodicity, radius of the hole, and depth. For the purposes of demonstration, a 2D W PhC with cylindrical cavities of diameter 800nm , depth $1.2 \mu\text{m}$, and period $1.2 \mu\text{m}$ is designed and fabricated. A single crystal W as a substrate is used. This thesis focuses on key aspects of the fabrication process that achieve required dimensional reliability, repeatability and optical performance.

Previous works have demonstrated that the enhancement of the 2D W PhC's thermal emission is achieved by coupling into the resonant modes of the periodic cylindrical cavities [12]. In such a cavity, the resonant frequency is found to be strongly dependent on the radius and hole depth. By varying the radius and depth of holes, one can tailor the resonant frequencies to suit various applications. More importantly, the peak emittance can be maximized via Q-matching through the control of depth. Therefore, it is important to achieve good control over the parameters during fabrication. To demonstrate the fabrication process, a 2D W PhC thermal emitter with cutoff near the wavelength of $1.7 \mu\text{m}$ suitable for gallium antimonide-based thermophotovoltaics is designed. Finite Difference Time Domain (FDTD) simulations show that a 2D W PhC with cylindrical cavities of diameter 800nm , depth $1.2 \mu\text{m}$, and period $1.2 \mu\text{m}$ is suitable. This is fabricated following the process described in Chapter 4.

Chapter 4

Fabrication of 2D PhC structure

The fabrication process, schematically shown in Fig. 4-1 , consists of two main parts; lithography and etching. First step is the deposition of a chromium (Cr) layer on the single crystal tungsten substrate using electron-beam evaporation. This layer is used as the hard mask for patterning the underlying W layer. Next two layers needed for lithography, anti-reflection coating (ARC) and photoresist (PR), are coated using a spinning stage. After lithographic exposure, the desired pattern is transferred from one layer to the next layer by various etching processes until periodic cylindrical holes are obtained on the W substrate. The following two sections describe the lithography and etching steps in more detail.

4.1 Lithography

A bi-level resist process is used in which patterns are imaged and developed in resist over an antireflection coating (ARC) [13]. After depositing chromium (Cr) on the single crystal tungsten substrate, cyclohexanone-based BARLi ARC is spun on the sample. This is necessary to minimize scalloping of the sidewalls due to vertical reflected standing waves from the Cr layer. Reflectivity calculations were performed to determine the proper thickness of the ARC layer that results in minimum reflection, and the calculation method is similar to the one used before [14, 15, 16]. The THMRiN-PS4 photoresist by OHKA America is then spun on the sample.

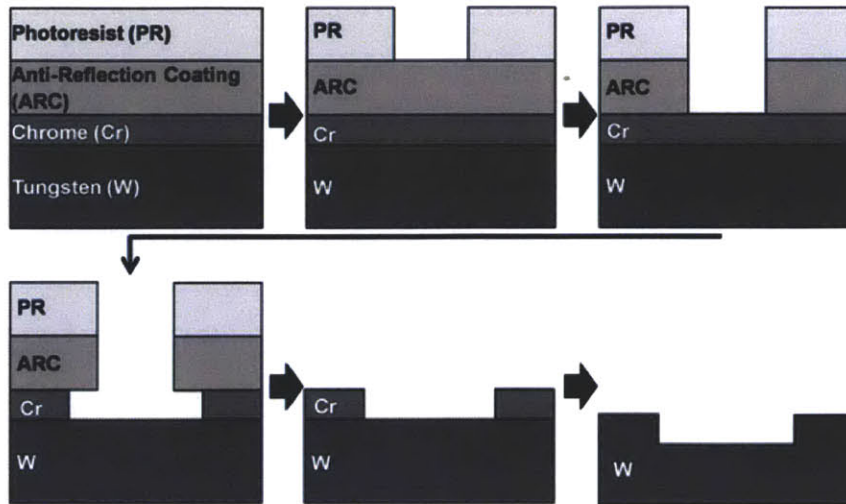


Figure 4-1: General process flow: after depositing a layer of chromium (Cr) on the tungsten substrate, two lithography layers of anti-reflection coating (ARC) and photoresist (PR) are coated on the chromium. After lithographic exposure, the desired pattern is transferred from the one layer to the next layer by various etching processes until periodic cylindrical holes on the W substrate are obtained.

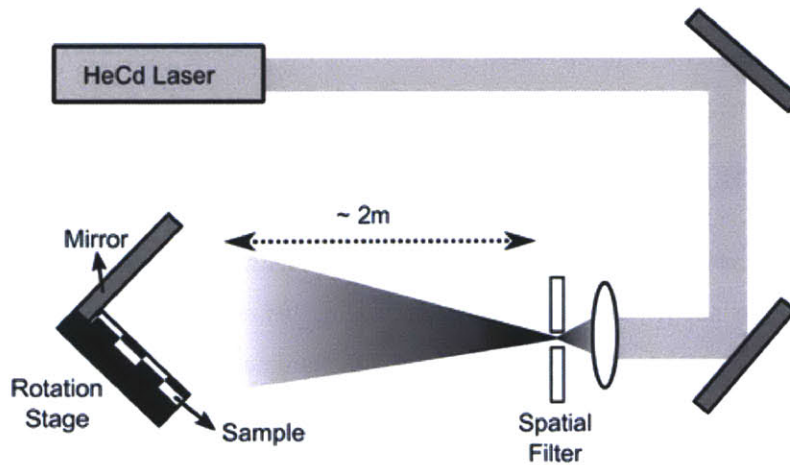


Figure 4-2: Schematics of the laser interference lithography used in exposing the photoresist.

Fig. 4-3 shows the reflectivity of the structure vs the ARC thickness. An ARC thickness of approximately 300 nm is needed to minimize the reflection.

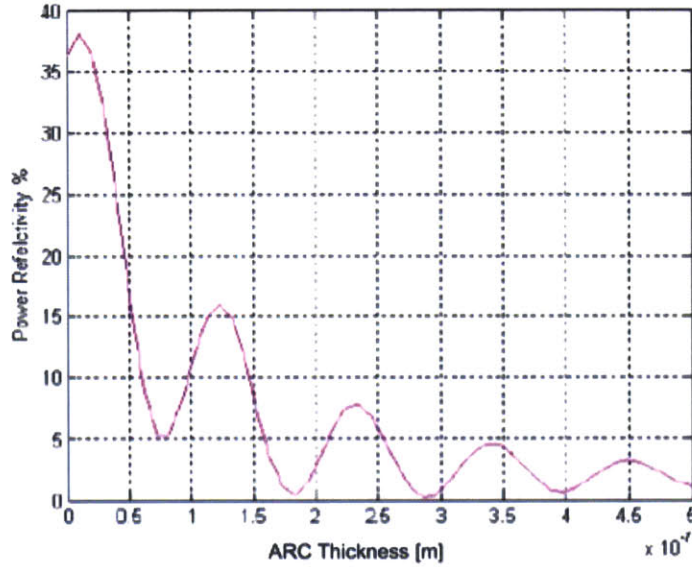


Figure 4-3: Anti-Reflection-Coating thickness calculation. The reflectivity diagram shows that a thickness of 285 nm, minimizes the reflection.

Laser interference lithography (IL) is used to make the desired pattern since it is relatively inexpensive, fast, and precise while allowing exposure of relatively large sample areas [17, 18]. In interference lithography, the interference of two plane waves produces a standing wave which is imaged into the photoresist. Fig. 4-4 illustrates this process.

Instead of having two lasers, Lloyd's mirror IL system is used, which is amongst the simplest IL systems [19], and includes a mirror at a 90° angle to the substrate to be exposed. The interference lithography setup is shown in Fig. 4-2. A helium-cadmium (HeCd) laser emitting at 325 nm is used as the source of coherent illumination as shown in Fig. 4-2. The long (2m) separation between the source and the sample provides an approximate plane wave incidence at the sample surface [19].

To achieve a 2D square lattice, two exposures at 90 degrees are performed. The

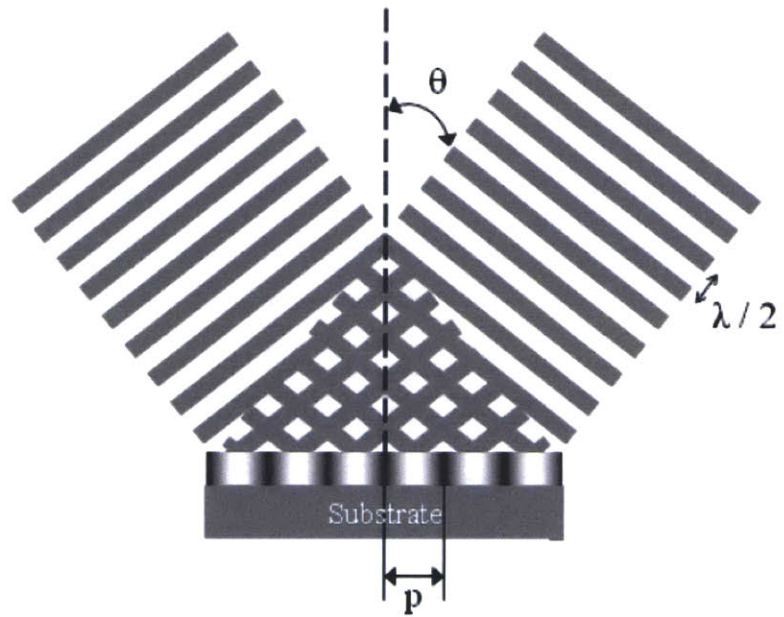


Figure 4-4: In interference lithography (IL) the interference of two plane waves produces a standing wave which is imaged into the photoresist. (Figure adapted from [17])

final shape of the holes is determined by the lithography procedure. The proximity effect is responsible for the shape of the holes [20], resulting in circular holes at longer exposure times and square-shape holes at shorter exposure times. Calibration tests were performed to determine the appropriate exposure times for the desired shape of the hole. For obtaining a square-shape hole, the minimum exposure time required to obtain a pattern was 35 seconds at a laser power of $170 \mu\text{W}$ in the plane of the sample. For a circular hole, it is necessary to have longer exposure time of 90 seconds. This is illustrated in Fig. 4-5.

Due to the use of negative tone photoresist, only round holes with thick walls or square holes with thin walls could be used as shown in Fig. 4-5. It is not possible to satisfy both at the same time. Preserving the round shape is the main priority while the diameter is insignificant since the holes are easily widened to a desired diameter in the Cr wet etch step which is detailed later. Hence, in the lithography step, overexposure is favored in producing a square array of circular holes.

We define the dose at which the rods become holes in the photoresist pattern, as the crossover dose. In practice, the dose is set by the exposure time, since the laser intensity is constant.

Fig. 4-6 shows the resist profile far below and above the crossover dose for a positive photoresist. This figure shows that the rods or holes created with these doses are circular. However calculations show that when the dose is near to the crossover dose the rods or holes become more square-shaped [21]. Fig. 4-7 shows the resist profile when the dose is near to the crossover dose.

After the lithography step, the PR is then developed in CD-26 developer. Fig. 4-8 shows the SEM image of sideview of the developed resist with an exposure time of 90 seconds and laser power of $170 \mu\text{W}$. In the next section of fabrication, the etching processes of ARC, Cr, and W are described.

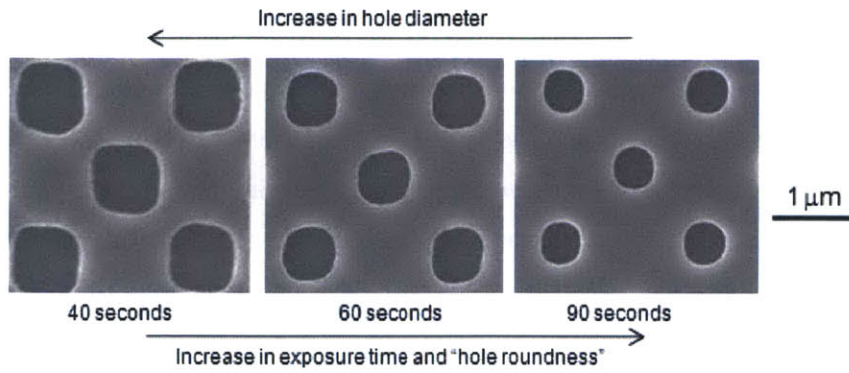


Figure 4-5: SEM images of the developed patterns in the photoresist for different exposure times, whereby the laser power is $170 \mu\text{W}$ at the sample plane.

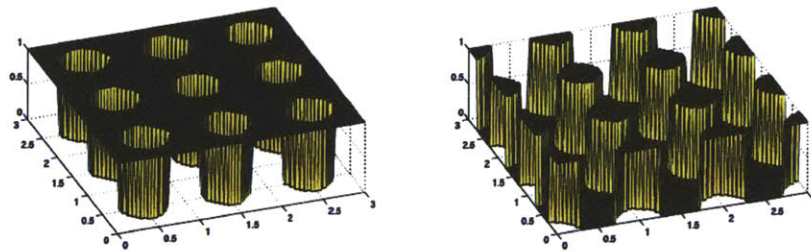


Figure 4-6: The resist profile far below (left) and above (right) the Crossover Dose for a positive photoresist. This figure shows that the rods or holes created with these doses are more circular-shape.(Figure from [21])

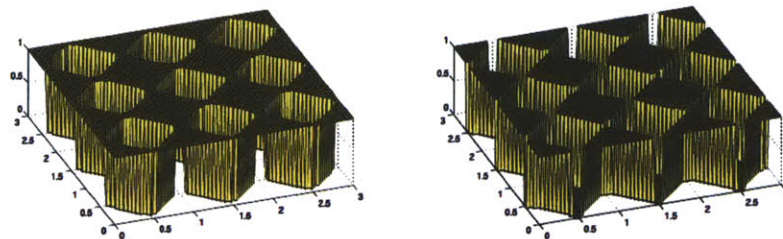


Figure 4-7: The resist profile for near the crossover dose. The holes (left) and rods (right) have more square-shape cross-sections.(Figure from [21])

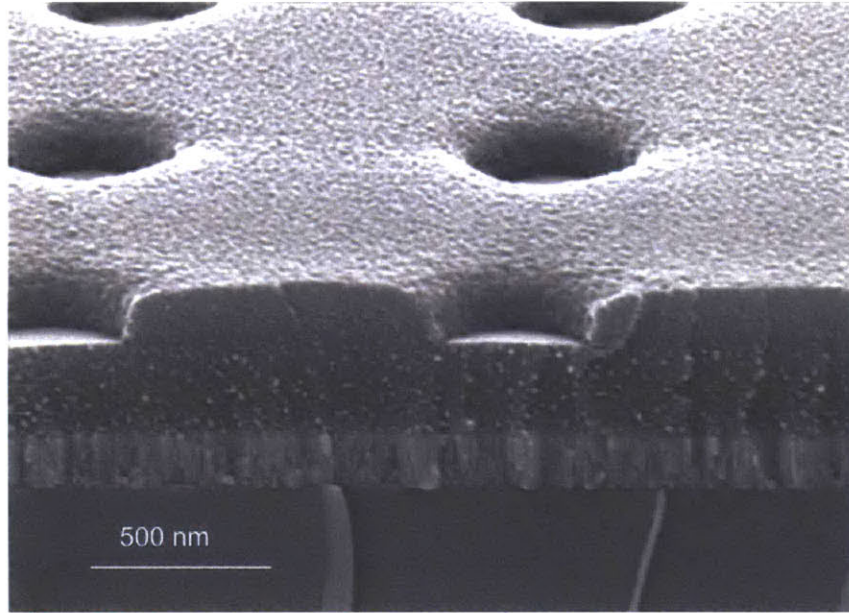


Figure 4-8: SEM image of sideview of the developed photoresist with an exposure time of 90 seconds, and laser power is $170 \mu\text{W}$ at the sample plane.

4.2 Etching

4.2.1 ARC Etching

In order to transfer the pattern from the PR to the ARC, oxygen-based reactive ion etching (RIE) is performed using the Plasma-Therm 790 Series RIE System. In order to preserve the hole size without widening the hole, it is important to only etch for the minimum required time such that no ARC remained, i.e. the Cr layer is completely exposed. Hence, a series of RIE experiments were conducted. In this process, a 2:1 (10 sccm : 5 sccm) plasma of helium and oxygen is prepared under 7 mTorr pressure, and a 250 V bias. Fig. 4-9 shows the ARC layer after RIE with RF power of 140-145W at 3 minutes and 30 seconds, which does not show any residual ARC in the holes. It is observed that a 3 minute long etch results in ARC remaining in the holes.

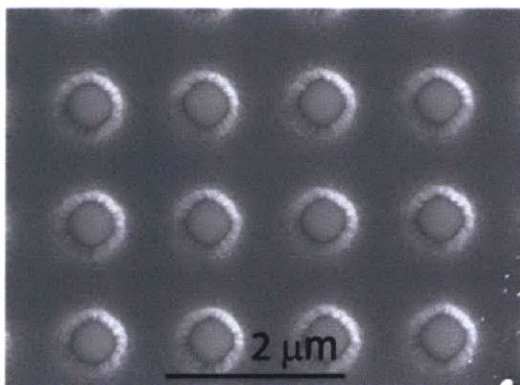


Figure 4-9: SEM image showing successful pattern transfer to the anti-reflection coating after undergoing an oxygen-based reactive ion etching at 140 W for 3 minutes 30 seconds

4.2.2 Chromium Etching

In order to etch the chromium hard mask layer, Cyantek CR-7, a commercial chromium wet etchant manufactured by Cyantek Corporation is used. The CR-7 etchant is diluted with 40% distilled water to ensure repeatability of results by slowing down the etch rate, thus allowing superior control of reaction time to adjust for the desired diameter of the hole. The result of such calibration is shown in Fig. 4-10. As can be easily seen, an etch time of 85 seconds results in the breaking of sidewalls. The ARC layer is then removed using the same ARC RIE process described in the previous section. In addition, the quality of the Cr mask is important to ensure the etch is uniform and the sidewalls are smooth. During the Cr deposition, it is important to achieve good vacuum (less than 0.01 mTorr). Also, increasing the substrate temperature to 250 °C during deposition results in a more uniform etch which is believed to be caused by better quality of deposited chromium. Fig. 4-11 shows the comparison of etched chromium mask, deposited at high temperature and at room temperature. As shown in this figure, high temperature deposition results in smoother sidewalls and a more uniform etch.

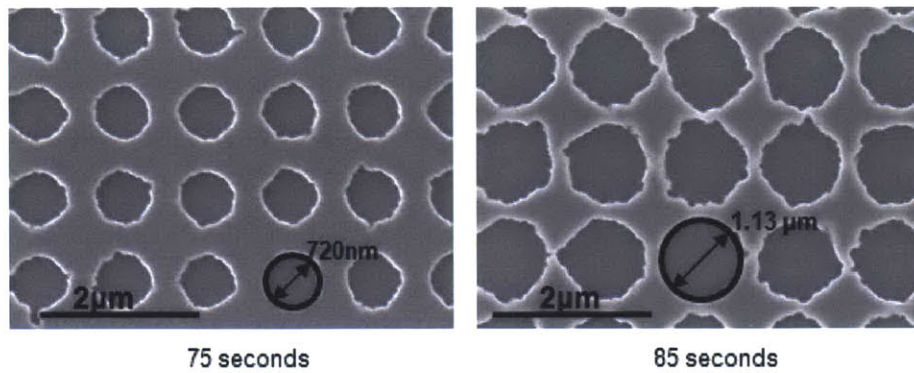


Figure 4-10: Scanning electron microscope (SEM) images demonstrating the control of etch times to obtain the desired circular hole diameter on the Chromium mask.

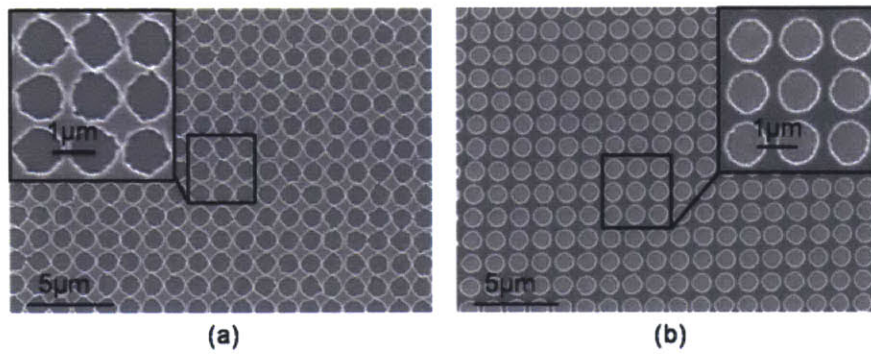


Figure 4-11: Chrome mask deposited at (a) room temperature and (b) high temperature (250 °C)

4.2.3 Tungsten Etching

The final and most important step is the tungsten etch. We used a 6.7:1 carbon tetrafluoride (CF_4) to oxygen (16 sccm: 2.4 sccm) RIE process to transfer the pattern from the Cr hard mask layer into the W substrate. The final etch depth is determined by both the etch rate and the thickness of Cr mask. The etch rate is related to the ratio of the gases, pressure and power used in the RIE process. Table. 4.1 compares the experimental observation for different power and pressures, and their advantages and disadvantages. It is observed that for etches longer than 5 minutes in one RIE run, the etch rate saturates which is due to the nature of the RIE system. Therefore, incremental etch steps of 5 minutes were used.

Table 4.1: Different RIE etch parameters and their effects on etch rate and mask damage.(percents are relative to the initial Cr mask thickness)

Power (W)	90	90	108
Pressure (mTorr)	10	7	10
Etch Depth (%)	100	84	120
Remaining Cr (%)	20	30	0
Mask Damage	Little	Little	High
Etch Rate	Medium	Low	High

The Cr mask thickness is slowly reduced during the W RIE process. Experimental results show that for every 10 nm of W, approximately 1 nm of Cr is sputtered away. However, this relationship is not exactly linear.

4.3 Characterization

In this project, both single crystalline tungsten samples and electron-beam deposited tungsten samples are used. In order to deposit tungsten using electron-beam, a buffer layer of chromium is needed. Electron-beam (e-beam) deposited tungsten samples can be used for calibration steps. Fig. 4-12 shows the scanning electron micrograph (SEM) of a 2D PhC tungsten sample, using e-beam-deposited tungsten.

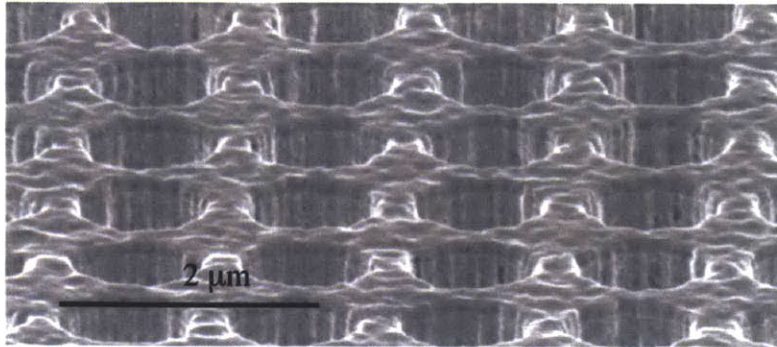


Figure 4-12: SEM image of a 2D PhC structure in an e-beam-deposited tungsten sample

Fig. 4-13 shows the scanning electron micrograph (SEM) of the final 2D PhC in single-crystal tungsten sample as well as the cross sectional profile measured using an atomic force microscopy (AFM). As can be seen, the target depth of $1.2\mu\text{m}$, diameter of 800nm (although not uniform), and period of $1.2\mu\text{m}$ are all achieved. To evaluate the performance of the fabricated 2D W PhC, a dual-beam spectrophotometer (Cary 5E UV-VIS-IR) is used to measure the room temperature reflectance. Furthermore, its absorptivity via energy conservation arguments is calculated, upon which the emissivity can then be implied to be equal to absorptivity by virtue of Kirchoff's Law. The results are shown in Fig. 4-14. As can be seen, a huge improvement in the emissivity is observed below the cutoff wavelength of $1.7\mu\text{m}$ compared to flat W. In particular, the measurements match well with the calculated spectra in terms of the resonant peaks. However, the emissivity above the cutoff wavelength is measured to be much higher. We believe that this is due to the surface contamination resulting from prolonged etching process. In addition, wall roughness contributes to increased long wavelength emittance.

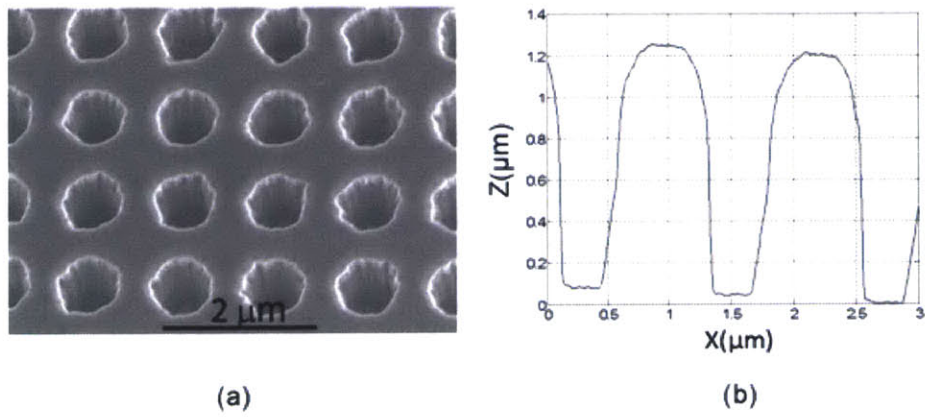


Figure 4-13: (a) SEM image of the final 2D single-crystal tungsten PhC and (b) cross-sectional profile mapped using an AFM.

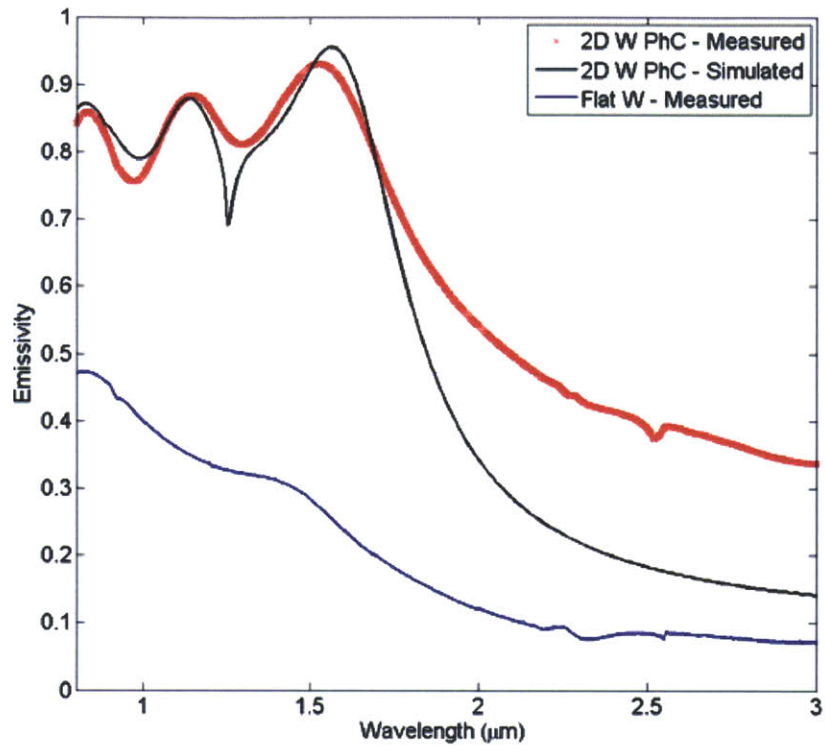


Figure 4-14: A marked enhancement is seen in the emissivity of the 2D W PhC at wavelengths below $1.7\mu\text{m}$.

Chapter 5

Micro-reactor Packaging and Testing

After fabricating the micro-reactor chips, each reactor is loaded with a catalyst and thin-walled glass tubes are connected to the reactor, as the inlet and outlet of the reactor. The glass tubes are brazed using a glass paste and high temperature. The other ends of the tubes are joined to the measurement setup using an epoxy. Loading catalyst, brazing and measurement tests were done by Walker Chan at MIT. In section 5.1 and 5.2 loading catalyst and brazing techniques are briefly discussed. More details can be found in Ref. [22] and Ref. [1].

5.1 Loading Catalyst

A wash-loading technique, which includes injecting the platinum catalyst into the microreactor and allowing it to dry inside the channel, is used for loading catalyst. The technique is described in more details in Ref. [22] and Ref. [1].

Fig. 5-1 shows a cross-section of the microreactor before and after loading the catalyst.

After injecting the catalyst, the reactors are placed in an oven horizontally at 80 °C for one hour. This process will evaporate the water out of the catalyst. The catalyst is injected inside the reactors and the same process is repeated, but this time

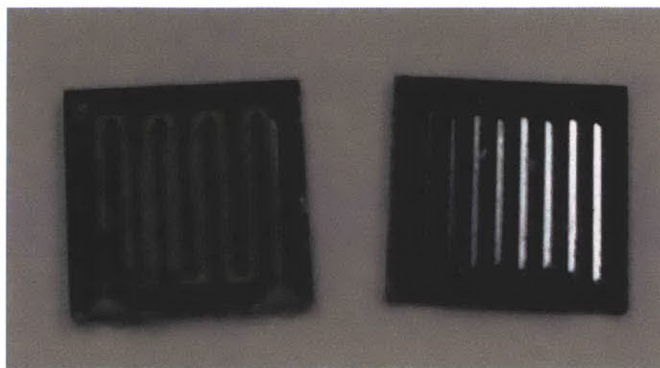


Figure 5-1: The cross-section of micro-reactors before (right) and after (left) loading catalyst (Figure from Ref. [22])

the reactors are turned over in the oven. This will ensure that the reactor channels are covered with catalyst on both the top and bottom of the channels.

5.2 Glass Brazing

After applying the brazing mixture to the joints between the micro-reactors and the tubes, the braze is allowed to dry. Next, the reactors are placed in a furnace. The temperature is ramped to 350 °C for two hours. Then, the temperature is ramped at a rate of 10 °C per minute to 690 °C. The reactors are kept at this temperature for two hours. Then, the furnace is cooled down to 400 °C with a rate of 1 °C per minute.

Fig. 5-2 shows two micro-reactors with glass tubes brazed to them.

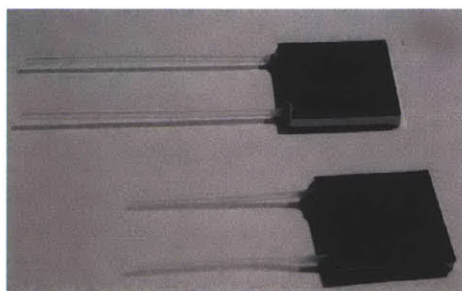


Figure 5-2: Glass tubes brazed to the micro-reactors (Figure from Ref. [22])

5.3 Efficiency Measurement

After fabricating the reactors, loading the catalyst and brazing the glass tubes, the heat-to-electricity conversion efficiency is measured.

Fig. 5-3 shows a micro-reactor chip in the measurement setup. TPV cells are placed underneath and above the reactor.

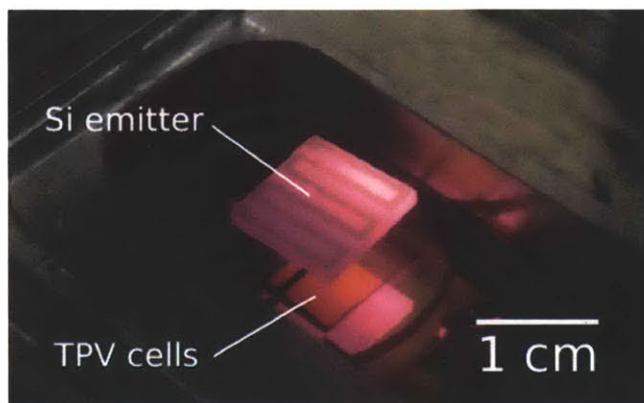


Figure 5-3: Measurement setup: Two TPV cells are placed under and above the micro-reactor.

Measurements were mainly done by Walker Chan and the details about the measurement setup is discussed in Ref. [22].

Fig. 5-4 shows the dependence of average temperature of a sample micro-reactor chip versus the input heat power and Fig. 5-5 shows the fuel-to-electricity efficiency.

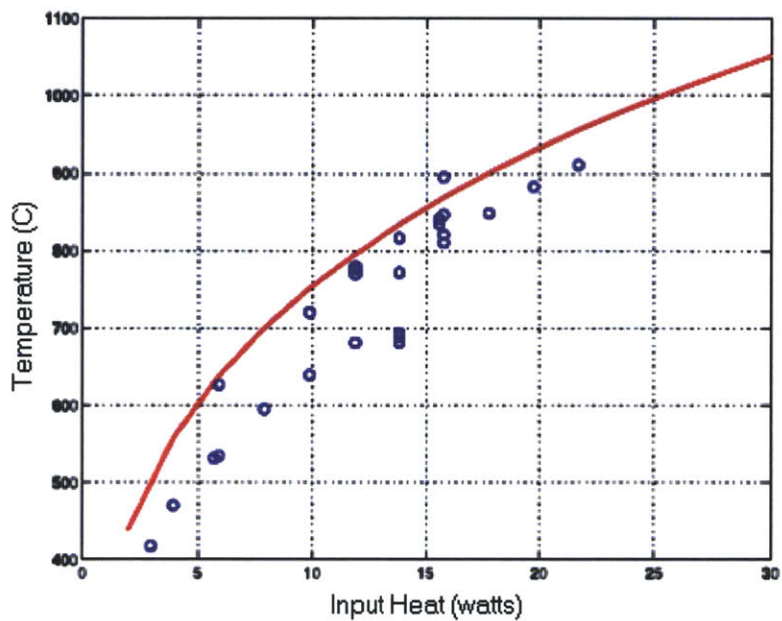


Figure 5-4: Dependence of average temperature of a sample micro-reactor chip vs. the input heat power. Solid line shows heat balance model and the points are experimental results.(Figure by Walker Chan)

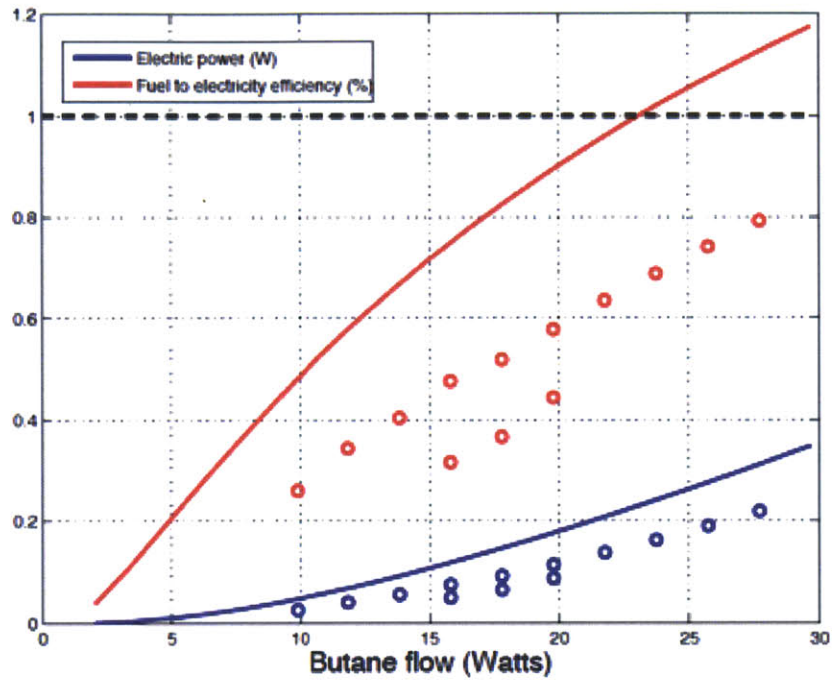


Figure 5-5: Electric power and fuel-to-electricity efficiency for a micro-reactor chip sample vs the butane input power. Solid lines show modeling results and the points are experimental results.(Figure by Walker Chan)

Chapter 6

Conclusion and Future Works

In this work, we fabricated silicon micro-reactors and demonstrated a propane-oxygen fueled catalytic micro-reactor integrated with GaInAsSb (0.53 eV bandgap) photovoltaic cells to create a fully operational millimeter-scale TPV system. The initial fuel-to-electricity efficiency of the system was 0.8%. Having a cell area of 2 by 2 cm, the system produced 200 mW of electricity from a 28W chemical input power.

A method for fabrication of two-dimensional W photonic crystals (2D W PhC) for high temperature applications was also investigated. The fabrication method is based on standard silicon processing techniques that are simple, efficient, and easily scalable. Using finite-difference time-domain simulations, 2D W PhC structures with cylindrical cavities of diameter 800nm, depth $1.2\mu\text{m}$, and period $1.2\mu\text{m}$ were designed and fabricated. This structure has a cutoff near the wavelength of $1.7\mu\text{m}$. A marked enhancement is measured in the emissivity of the 2D W PhC at wavelengths below $1.7\mu\text{m}$ compared to flat W. The measurements match well with the calculated spectra in terms of the resonant peaks.

6.1 Future Works

There are several ways to improve the efficiency of the TPV systems. The view factor can be increased by reducing the distance between the silicon micro-reactors and TPV cells. Vacuum packaging of the micro-reactors and TPV cells can increase

the efficiency by reducing convection. Also, one-dimensional and two-dimensional photonic crystals discussed in this thesis can be integrated with the micro-reactors to improve the spectral efficiency of TPV systems.

Appendix A

Fabrication Process

In the next 4 tables the fabrication process of silicon micro-reactors is detailed for fabrication at MIT.

Table A.1: Part 1: Deposit SiN

Step	Lab	Machine	Wafer Number	Action
1.1	ICL	RCA	1,2	RCA clean wafers for CVD
1.2	ICL	VTR	1,2	Deposit 250nm VTR SiN on both sides of the wafers

Table A.2: Part 2: Pattern Nitride

2.1	TRL	HMDS	1,2	Deposit HDMS
2.2	TRL	Coater	1,2	Coat wafer w/ 10 um AZ4620 resist
2.3	TRL	Prebake oven	1,2	Prebake 30 min at 90 °C
2.4	TRL	EV1	1,2	Expose 10 sec. (use reactor mask)
2.5	TRL	Postbake oven	1,2	Postbake 30 min at 120 °C
2.6	ICL	LAM490B	1,2	Remove exposed nitride using standard nitride-etch
2.7	TRL	asher	1,2	Remove polymer from LAM490B step
2.8	TRL	acidhood	1,2	Piranha clean wafer to remove resist
2.9	TRL	HMDS	2	Deposit HDMS
2.10	TRL	coater	2	Coat back side of wafer with 10 um AZ4620 resist
2.11	TRL	Prebake Oven	2	Prebake 30 min at 90 °C
2.12	TRL	EV1	2	Expose for 10 sec
2.13	TRL	Postbake oven	2	Postbake 30 min at 120 °C
2.14	ICL	LAM940B	2	Remove exposed nitride using standard nitride-etch
2.15	TRL	asher	2	Remove polymer from LAM490B
2.16	TRL	acidhood	2	Piranha clean wafer to remove resist

Table A.3: Part 3: KOH Etch Channels

3.1	ICL	TMAH-KOHhood	1,2	25% 80 °C KOH etch wafer
3.2	TRL	acidhood	1,2	Post KOH etching nitride (2 piranhas)
3.3	ICL	acidhood	1,2	Nitride removal (Hot phosphoric acid)

Table A.4: Part 4: Bond Wafers

4.1	TRL	RCA-TRL	1,2	RCA clean wafers
4.2	TRL	EV501	1,2	Align wafers for bonding
4.3	TRL	Tube B3	1,2	Fusion bond in H_2/O_2 to grow 500 A SiO_2
4.4	ICL	diesaw	(1,2 bonded)	Dice wafers

Appendix B

2D Tungsten PhC Integration Process

Table B.1: Part 1: Deposit SiN

Step	Lab	Machine	Wafer Number	Action
1.1	ICL	RCA	1,2	RCA clean wafers for CVD
1.2	ICL	VTR	1,2	Deposit 250nm VTR SiN on both sides of the wafers

Table B.2: Part 2: Resist Lithography

2.1	ICL	Coater6	1,2	Coat Resist for Photolithography
2.2	ICL	I-Stepper	1,2	Expose Resist using 2D PhC mask
2.3	ICL	Coater6	1,2	Develop Resist for next steps

Table B.3: Part 3: Nitride mask patterning and resist removal

3.1	ICL	LAM490B 1,2	Remove exposed nitride using standard nitride-etch
3.2	ICL	asher 1,2	Remove polymer from LAM490B step
3.3	ICL	acidhood 1,2	Piranha clean wafer to remove resist

Table B.4: Part 4: Pattern Silicon

4.1	ICL	AME5000	1,2	Etch exposed silicon using standard silicon-etch
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Table B.5: Part 5: Lithography of the interface sides

5.1	TRL	HMDS	1,2	Deposit HDMS
5.2	TRL	Coater	1,2	Coat wafer w/ 10 um AZ4620 resist
5.3	TRL	Prebake oven	1,2	Prebake 30 min at 90 °C
5.4	TRL	EV1	1,2	Expose 10 sec. (use reactor mask)
5.5	TRL	Postbake oven	1,2	Postbake 30 min at 120 °C
5.6	ICL	LAM490B	1,2	Remove exposed nitride using standard nitride-etch
5.7	TRL	asher	1,2	Remove polymer from LAM490B step
5.8	TRL	acidhood	1,2	Piranha clean wafer to remove resist
5.9	TRL	HMDS	2	Deposit HDMS
5.10	TRL	coater	2	Coat back side of wafer with 10 um AZ4620 resist
5.11	TRL	Prebake Oven	2	Prebake 30 min at 90 °C
5.12	TRL	EV1	2	Expose for 10 sec
5.13	TRL	Postbake oven	2	Postbake 30 min at 120 °C
5.14	ICL	LAM940B	2	Remove exposed nitride using standard nit-etch
5.15	TRL	asher	2	Remove polymer from LAM490B
5.16	TRL	acidhood	2	Piranha clean wafer to Remove resist

Table B.6: Part 6: KOH Etch Channels

6.1	ICL	TMAH-KOHhood	1,2	25% 80 °C KOH etch wafer
6.2	TRL	acidhood	1,2	Post KOH etching (2 piranhas)
6.3	ICL	acidhood	1,2	Nitride removal (Hot phosphoric acid)

Table B.7: Part 7: Bond Wafers

7.1	TRL	RCA-TRL	1,2	RCA clean wafers
7.2	TRL	EV501	1,2	Align wafers for bonding
7.3	TRL	Tube B3	1,2	fusion bond in H_2/O_2 to grow 500 Å SiO_2

Table B.8: Part 8: Tungsten Deposition

8.1	TRL	eBeamAu	1,2 bonded (on side 1)	Deposit 20 nm of Chromium
8.2	TRL	eBeamAu	1,2 bonded (on side 1)	Deposit 50 nm of Tungsten
8.3	TRL	eBeamAu	1,2 bonded (on side 2)	Deposit 20 nm of Chromium
8.4	TRL	eBeamAu	1,2 bonded (on side 2)	Deposit 50 nm of Tungsten

Table B.9: Part 9: Dice Wafers

9.1	ICL	diesaw	(1,2 bonded)	Dice wafers
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