Development of a Melting and Directional Solidification Process for Improving the Grain Structure and Electronic Properties of a Silicon Wafer

by

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Submitted to the Department of Mechanical Engineering in Partial Fulfillment of the Requirements for the Degree of Master of Engineering in Mechanical Engineering at the MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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Abstract

A manufacturing process that produces high quality, inexpensive kerfless silicon wafers for photovoltaic cells is highly desirable. The process herein described was developed to melt and directionally solidify fine-grained silicon wafers at accelerated feed rates for improved electronic properties. The proposed process encapsulates a fine grained silicon wafer which is then sandwiched between two substrates with a specialized release layer. This stack is then zone-melted and recrystallized in a novel zone-melting furnace. The innovations herein described pertain to the design of a novel radiation furnace, the substrate selection, and the process parameters required to repeatedly yield planar wafers, with several centimeter sized grains, and a low dislocation density of $\sim 10^4 \text{cm}^{-2}$.

Specifically, the phenomena that govern the thickness profile of the wafer were examined, and process modifications were made to yield a planar wafer with a $+/- 15 \mu \text{m}$ thickness range over 85% of a 6” wafer. Furthermore, a relationship between the thermal characteristics of the zone-melting furnace, the process feed rate, and the relative grain size were derived. This relationship was used to design and characterize a novel, zone-melting radiation furnace that can solidify a silicon wafer with $\sim 1^\circ$ solidification angle at 60 mm/min. Additionally, preferential nucleation sites that reduce the likelihood of large grains were identified and experimentally minimized by biasing the wafer to cool preferentially from one side. Finally, mechanisms to create dislocations were identified and minimized. This included minimizing the number of stress concentrations in the wafer and reducing the thermal resistance between the wafer and its supporting conductive substrate.
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1. Introduction

The most expensive component of a crystalline silicon solar cell is the silicon wafer, as illustrated in Figure 1.

![Figure 1: High Level Cost Breakdown of a Crystalline Solar Cell Module](image)

There are presently two competing industrial approaches to manufacture the most inexpensive silicon wafer for a photovoltaic cell. The first approach involves casting and slicing a large silicon ingot, which results in almost half of the raw silicon material going to waste from kerf-loss. The second approach involves pulling a ribbon of material directly from a melt of silicon, which yields a lower quality wafer that result in lower efficiency modules. Presently, these two approaches have comparable costs on a $/W_p$ metric. Existing wafer manufacturing technologies have achieved the capabilities shown in Table 1. A manufacturing process that could produce high performing, silicon wafers that do not require a sawing step is highly desirable.

<table>
<thead>
<tr>
<th>Manufacturing Process</th>
<th>Cast Multi/Sawing</th>
<th>CZ/Sawing</th>
<th>RGS</th>
<th>String-Ribbon</th>
<th>EFG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon (g/W_p)</td>
<td>5.44</td>
<td>4.08</td>
<td>4.24</td>
<td>3.58</td>
<td>3.58</td>
</tr>
<tr>
<td>Feed Rate (mm/min)</td>
<td>3.00</td>
<td>1.80</td>
<td>200</td>
<td>18</td>
<td>20+</td>
</tr>
</tbody>
</table>

Table 1: Table of Typical Performance Metrics for Existing Crystalline Silicon Wafering Technologies

1.1 Recrystallization (RX) Concept Description

There is substantial value in a kerfless wafer manufacturing process that cheaply and robustly produces silicon wafers that that can be processed into high efficiency solar cells. The proposed Direct Wafer/RX technology herein described is a two step process to make a high quality, inexpensive kerfless wafer. As illustrated in Figure 2, the Direct Wafer process step rapidly casts a silicon wafer with poor electronic properties. Before recrystallization the wafer is encapsulated and sandwiched between two substrates. This stack is then melted and directionally recrystallized for improved electronic properties, as shown in Figure 2.
This work focuses on the development of the RX process. This includes theoretically developing an understanding of the heat transfer involved in the melting, solidification, and cool-down of the RX wafer. This work also investigated and experimented with different high temperature materials that would both minimally contaminate the wafer and create the desired process conditions. These models and experiments guided the process design decisions for substrates, encapsulant materials, and furnace design.

1.2 Performance Metrics

The goal of the RX process is to cheaply and robustly produce silicon wafers that can be processed into high efficiency solar cells. High-level performance metrics are defined to guide the design decisions of the RX process and evaluate the quality of the wafers.

**Wafer Profile:** Because of post-processing and repeatability concerns, the planarity of the wafer is critical. A ±10% thickness profile variation will be the imposed maximum tolerance (±20 μm thickness tolerance on a 200 μm wafer).

**Economics:** As this is an economically driven project, it is important to understand that this process will not be commercially viable unless it can economically improve on already existing technologies. The manufactured cost of a solar cell is generally evaluated on a $/W_p$. This evaluation stems from two different variables: the cost of manufacturing the wafer and the efficiency of that wafer. The cost of manufacturing the wafer includes both the marginal and the fixed costs of production. Marginal costs include the energy and consumable costs, including the cost of the silicon, the crucible, and sawing consumables (when applicable), as shown Figure 3.

![Consumables for CZ Wafer](image)

**Figure 3: Typical consumable break-down for a CZ wafer[^2]**

Because RX is a kerfless process, this process does not incur the costs associated with sawing (SiC, Wire, Caustic Waste) which typically make up half the consumable costs of most
crystalline wafer manufacturing processes. Furthermore, the CAPEX for each wafer is marginalized by the process rate and thus can be reduced by higher speeds.

Although present industrial practices offer guidelines to evaluate RX’s performance, it is difficult to establish a hard line process metrics. Previous studies have determined that a process feed rate must be over 100 mm/min to be economic (personal communication with Adam Lorenz, 1366 technologies). Furthermore, this study concludes that this process must yield wafers that result in solar cells with efficiencies of over 16%. This will be the tentative performance metric to evaluate the RX process.

**Wafer Efficiency:** Modern day multi crystalline silicon solar cells have achieved efficiencies of 15-16% with industrial standard processing, and up to 17% with improved processes.[3] Wafer efficiency is denoted by the open circuit voltage across the cell ($V_{oc}$) and the short-circuit current ($J_{sc}$). Although both parameters are determined by the surface and bulk defects, each parameter is generally limited by the location and type of defect. The $V_{oc}$ is often limited by recombination and trapping specifically in the depletion region of the cell.[4] Wafer features that are associated with this limitation are grain boundaries or areas with large structural defects. Alternatively, $J_{sc}$ is directly related to the wafer’s average carrier lifetime. A wafer’s average carrier lifetime is a function of the activity of crystal defects which is largely influenced by process-induced contamination.[3]

Therefore, an RX wafer must exhibit few grain boundaries, minimal structural defects, and high average lifetimes. Quantitative insights of this performance metric are described in further detail the chapter that pertains to nucleation and grain growth.
2. Wafer Containment and Release

2.1 Background

A wafer made by the recrystallization process (RX) must be planar, have an even thickness profile, and repeatedly release from its carrier. Maintaining the planarity of a wafer is difficult because the high surface tension that is characteristic to liquid silicon causes the wafer to 'balls-up' upon melting. Figure 4 shows that when a bare silicon wafer is melted and recrystallized without any support structure, it does not maintain its original geometry.

![Figure 4: Silicon wafer recrystallized without any substrate or surface capsule](image)

Wafers that are encapsulated in either a thermally grown oxides or a thin PE-CVD layer of silicon nitride can maintain their original geometry after melting and recrystallization. Figure 5 compares different capsule materials and thicknesses.

![Figure 5: 1” silicon squares with either SiO₂ or SiN capsules of different thicknesses that were melted and recrystallized without any topside surface constraint](image)

Wafer encapsulation by itself, however, does not yield flat wafers. Encapsulated wafers demonstrated non-uniform thickness profiles which became more pronounced as the size of the wafer increased. Figure 6 shows a 200 μm thick, 4” x 1” wafer that was encapsulated with silicon dioxide, melted, and then directionally recrystallized within a tube furnace. Although this wafer did remain rectangular while molten, silicon from one region of the wafer almost completely drained into a neighboring region. This mass flow yielded a translucent section of the wafer and an unwanted 350 μm thickness gradient along the wafer length.
Front region of wafer is transparent because most of the silicon evacuated the region.

**Direction of Solidification**

Figure 6: 4"X 1" silicon wafer encapsulated in 1 μm oxide capsule melted and directionally solidified in a tube furnace

To counteract the development of a thickness profile, a top substrate can be placed on the top surface of the wafer, as illustrated in Figure 7. This substrate would theoretically rest on the highest region of the wafer and therefore suppress the development of a thickness bulge. Wafers that were melted and recrystallized with this secondary substrate did not demonstrate the substantial amount of mass flow that was characteristic of the wafer in Figure 6. However, the 200 μm wafers that were melted and recrystallized with this top substrate still consistently demonstrated 50-100 μm thickness gradients along the length of the wafer.

![Top Substrate Diagram](Image)

**Figure 7: Top backing plate counters the development of a convex bulge by always making contact with the highest point of the silicon melt**

Furthermore, a technique to coat the substrates with a thin quartz powder release layer was developed to release the recrystallized wafer from its containing substrates. This powder ensures that the encapsulating material does not make direct contact with the substrates. Furthermore, this powder layer intercepts any silicon that escapes from the capsule. Figure 8 shows how small silicon 'burst-outs' that escape from the capsule do make contact with the substrate.

![Capillary Diagram](Image)

**Figure 8: Burst outs incident on quartz release layer that resulted from two grains overlaying each other and entrapping melt**
The combination of a quartz powder release layer and a top substrate consistently allowed for an encapsulated wafer to be released from the substrates, maintain the edges of the original geometry, and exhibit only a ~100 μm thickness profile.

2.2 Work Continuation

This section will develop a conceptual understanding of the phenomenon that govern the thickness profile of silicon wafer with an oxide capsule. From this understanding, the encapsulation and support of the wafer will be modified to reduce the amount of mass flow that occurs when the wafer is molten.

Because the thickness profile of the wafer is created when liquid silicon flows from one region of the wafer to another, the phenomena that govern this gradient must be associated with the liquid phase of the wafer. Two mechanisms that could create mass flow were identified. The first involves the volume contraction and expansion that silicon undergoes when it is respectively melted and solidified. The second is associated with surface tension forces acting to minimize the surface area of the wafer.

2.2.1 Thickness Profile Created by Volumetric Expansion

Melting and directionally recrystallizing silicon can result in a thickness gradient along the length of a wafer. In contrast to all metals silicon undergoes a volume expansion of approximately 7% during freezing. Therefore, when an increment of liquid silicon solidifies at the existing height of the melt, it expels the excess mass that is not needed to fill this volume into the remaining melt. This additional quantity increases the height of the melt, resulting in the next increment of liquid solidifying at a larger thickness. This phenomena continues as the wafer incrementally crystallizes.

A MATLAB script was written to show how significantly this dynamic can affect the thickness profile of a wafer. Figure 9 shows how a wafer that is originally 190 μm thick would span a ~30 μm gradient for 80% of the wafer length. This is an acceptable thickness profile for a silicon wafer. When this solidification model is compared to the thickness profile observed in Figure 6 that spanned over 100 μm, it is apparent that there are other phenomena that govern the thickness profile of the wafer.

![Figure 9: Simulated solidification profile that results from the incremental solidification of a silicon wafer](image-url)
2.2.2 Thickness Profile Created by Pressure Imbalance

A force imbalance can cause liquid silicon to flow from one region of the capsule to another. This section will identify potential sources for pressure differences and analyze their respective capabilities to affect the wafer’s final thickness profile.

Tilting the wafer with respect to the horizontal axis will result in a pressure gradient in the liquid silicon. The magnitude of the pressure at the lowest region of the wafer will be

\[ \Delta P_{\text{gravity}} = \rho g L \sin \theta \]  

where \( \rho \) is the density of silicon, \( g \) is the gravitational acceleration constant, \( L \) is the length of the wafer, and \( \theta \) is the angle between the wafer and the horizontal axis.

Another force imbalance can be imposed on a region of the wafer by the substrate that rests on the top surface of the wafer. The pressure that a 2 mm silicon carbide (SiC) plate can exert on a region of the wafer is

\[ \Delta P_{\text{bp}} = \frac{m_{bp} g}{A_{\text{contact}}} \]  

where \( m_{bp} \) is the mass of the backing plate and \( A_{\text{contact}} \) is the contact area on which the SiC rests.

Finally, surface tension forces can give rise to a pressure differential called a Laplace pressure that can move mass from region of the wafer to another. Silicon’s high surface tension of \(~700\) mN/m provides a substantial driving force for the encapsulated liquid to minimize its interfacial energy. The magnitude of this pressure is determined by the curvature of each respective region and is equal to:

\[ \Delta P_{\text{st}} = \gamma \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \]  

Where \( \Delta P \) is the pressure difference, \( \gamma \) is the surface tension, and \( R_1 \) and \( R_2 \) are the respective curvatures of an enclosed area. As described in Equation 3, a flat surface, or infinite radius, will not give rise to any pressure. However, a positive or negative pressure can be created in a region of the wafer that develops a curvature. Because the magnitude of a Laplace Pressure scales with curvature, the region with the largest respective curvature will drain into a neighboring region. As shown in Figure 10, a concave region will therefore drain into a convex region.

![Figure 10: Two potential geometries of the encapsulated silicon melt](image)

Furthermore, the evolution of a curved region can give rise to a reinforcing dynamic that can completely drain an entire region of the wafer if left undisturbed. This phenomenon, commonly
referred to as Ostwald Ripening, occurs because as one region of the wafer drains into another, it obtains a more pronounced curvature. This curvature yields a larger driving force to drain another region, as illustrated in Figure 11.

![Figure 11: Adaptation of traditional concept of Ostwald ripening for the dynamic of the wafer](image)

To determine how significantly each source could affect the thickness profile of the wafer, each pressure source was evaluated for feasible parameters that could occur in the RX process. The potential force imbalance that could arise from surface tension was evaluated assuming that one side of the wafer was flat and the other side exhibits a radius that is a multiplier of the wafer thickness. Possible hydrostatic pressure values were evaluated for different height differences between the top and bottom of the wafer. Finally, the potential values for the pressure gradient created by the normal force of the top substrate were evaluated assuming that the backing plate was in contact with only a percentage of the wafer.

![Figure 12: Potential pressure gradients created in wafer from multiple sources. R is the radius of curvature, t is the wafer thickness, h is the height difference between sections of the wafer, A% is percentage of the wafer in contact with the top substrate](image)

Figure 12 shows that the surface tension forces can yield the largest pressure imbalances inside the capsule. Therefore, the wafer that is shown in Figure 6 was most likely drained by the surface tension forces. Because surface tension forces can result in significantly larger pressure
differences than other the sources, it is critical to prevent curvatures from developing along the length of the wafer.

A curvature along the length of the wafer can only occur if the capsule deforms. An oxide capsule softens at temperatures above $1250^\circ$ C, and therefore allows for plastic deformation. Alternatively, SiN does not soften and adds more structural stability to the capsule, as shown in Figure 5.

A wafer with a 1 μm oxide capsule was coated in 160 nm PE-CVD coating of silicon nitride (SiN) and then melted and recrystallized. Compared to wafers recrystallized with only oxide capsules, these wafers exhibited substantially reduced thickness profiles. A thickness profile measured along the center of the wafer matched well with the solidification model previously developed, as shown in Figure 13.

![Figure 13: Thickness line profile of the center of a RX wafer with a 160 nm PE-CVD layer of SiN](image)

However, a white light optical profilometer topography map of the surface revealed that this shallow profile did not result because the capsule remained rigid throughout the process. Rather, a more homogenous thickness profile in the center of the wafer occurred because the surface of the capsule bowed inward in response to the volume contraction of the melt, as shown in Figure 14.
The volumetric contraction inherent to melting put the capsule in tension with this concave geometry which prevented mass flow along the wafer. Surface tension forces could not give rise to mass flow because the negative pressure created by surface tension was less what is required to yield the capsule further.

Unfortunately, the regions of the capsule near the center of the wafer are not supported by the edges. Therefore, a capsule that spans 6” will be less constrained than the 1” sample that is shown in Figure 14. To observe the mass flow of a melt without the negative pressure maintained by the edges of the capsule, the edges of a wafer with a SiN/oxide capsule were scribed off prior to melting and resolidification. The topography map in Figure 15 shows that the 160 nm SiN layer was not enough to prevent the surface tension forces from substantially deforming the wafer without the edges maintaining a negative pressure inside the capsule.

Therefore, a thick layer (~80 micon) of quartz release powder was used to stabilize the thin oxide capsule and ensure good contact between the capsule and the top substrate. The powder allows for the top substrate to make many conformative point contacts with the oxide capsule. Furthermore, the point contacts of the powder pressing into the oxide capsule create a local tension in the capsule that prevents the wrinkling of the surface, as shown in Figure 16.
Because surface tension forces become increasingly strong as a curvature develops, the evolution of a curvature must be prevented. The top substrate can suppress the development of a curvature in the capsule only when it makes contact with the region that is developing a convex bulge. As shown in Figure 16, the rigid walls of the SiN/oxide prevent the substrate from making contact with the melt until a convex region develops that is taller than the height of the walls. But once a region this large evolves, the substrate may not have enough weight to counteract the full development of the bulge.

An oxide only capsule, however, is not rigid at the melting temperature of silicon and the edges of the wafer will yield under the combined effects of the melt contraction and the top substrate pressure. An oxide capsule will therefore ensure the substrate stays in contact with the melt, as shown in Figure 17.

The quartz powder layer structurally stabilizes the capsule without creating a thickness profile along the perimeter of the wafer. Figure 18 shows a planar cross-section of a wafer that was reinforced with a quartz powder layer. The combination of a thermally grown oxide capsule (~300 nm) and a thick layer of quartz powder repeatably yields wafers that have less than ±15% thickness gradients for over 85% of the wafer.

In summary, the phenomena that govern the thickness gradients of the wafer were identified, and an understanding of how they effect the RX process was developed. Furthermore, techniques to suppress thickness gradients along the length of the wafer were progressed. Specifically, a thick layer of quartz powder on the top surface of the wafer was used to locally stabilize the capsule.
and inhibit the evolution of thickness gradients caused by Ostwald Ripening. The present RX process can robustly release wafers with ± 15% thickness gradients for over 85% of the wafer.

Figure 18: Typical thickness profile for a 200 μm wafer. This image sandwiches the profile between an image of both the top and the bottom wafer.
3. Nucleation and Grain Growth

3.1 Impact of Grain Size

It is important to understand how the grain size of the wafer can influence the performance of a solar cell. Grain boundaries affect the diffusion of the p-n junction, the location of impurities in the wafer, and the recombination activity both at the grain boundary and within the bulk of the crystal. The following mechanisms are the ways in which grain boundaries are problematic for the post-processing of the wafer.

Grain boundaries act as short circuits for the diffusion of the p-n junction.\(^4\) Therefore, the position of the depletion region is not consistent at grain boundaries, potentially reducing the \(V_{oc}\) of the cell. Furthermore, grain boundaries act as recombination sites for excited carriers. Therefore, to minimize the overall recombination activity of the wafer, grains must be significantly larger than the diffusion length of an excited carrier. For a given multi-crystalline cell, a good base minimum grain size of 1 mm\(^2\) can be assumed to minimize this phenomenon.

The recombination activity of a grain boundary is determined by the impurities that decorate it. Grain boundaries obtain impurities at two different stages of processing. The first stage where grain boundaries obtain impurities is during solidification. Because grain boundaries are the last regions to solidify, they contain a relatively large amount of impurities that were segregated from the rest of the wafer material. The second stage at which grain boundaries obtain impurities is during the POCL diffusion process step when impurities that are still distributed in the crystal bulk are gettered to the grain boundaries. Grain boundaries effectively ‘clean’ the bulk of the lattice during this stage at the cost of higher recombination activity at the grain boundaries.\(^8\) Although gettering may increase the average lifetime in the bulk of the lattice, the overall efficiency of the wafer may diminish because of the heightened recombination activity at the depletion zone will lower the open circuit voltage of the cell. Furthermore, thermal stress at the grain boundaries can create areas with larger concentrations of dislocations. Therefore, the recombination activity of the area around grain boundaries is generally increased as well. Also, colliding grains often result in melt entrapment that can potentially crack the wafer. Finally, grain boundaries act as sites for light impurities to precipitate. Common precipitates like SiO\(_2\), SiC, and SiN stress the lattice locally and have been shown to form complexes with metallic impurities, thereby further increasing the electrical activity of the region.

3.2 Large Grain Growth at Accelerated Process Rates

It is highly desired to grow large grains at accelerated process speeds. As shown in Figure 19, an existing grain can grow without the nucleation of new grain if heat is extracted through the solidification interface. This is challenging at accelerated process rates because both solidification and nucleation are thermally driven. Therefore, increasing the process speed also increases the driving force for heterogeneous nucleation.
Figure 19: Conceptual illustration of the goal of the RX process where the interface is grown faster than other grains can nucleate

How readily a ribbon process can grow large grains at accelerated process rates is indicated by the angle of its solidification profile, as shown in Figure 20. If the angle is too small, as is the case with RGS, there is no driving force to directionally propagate existing grains and island growth occurs. If the angle is too large, as is the case with String-Ribbon processes, then the process rate is limited by the amount of heat extracted through the interface, as shown in Figure 21.

Figure 20: Schematic of Solidification Interface of RX Wafer

This chapter focuses on identifying the conditions needed to grow existing grains at accelerated process rates. The following section, Heat Extraction through Existing Grains, will first derive a basic heat transfer expression that relates the interfacial velocity ($V_{\text{INT}}$) to the heat flow ($q_y$) from the surface of the wafer. This theory will be used to design a recrystallization furnace for high process speeds. Section 3.4 will then develop a relationship between the heat flow of the furnace and the average expected grain size for a wafer. This theory will be used to identify the process rate limitations of the existing RX furnace and potential paths for improvement. Finally, this chapter will end with experimentally reducing the number of preferential nucleation sites on the oxide capsule to reduce nucleation ahead of the growth front.
3.3 Heat Extraction through Existing Grains

The relationship between the solidification angle and the rate of heat transferred from the surface of the wafer is critical for the design of the RX furnace. The diagram provided in Figure 20 shows that the interfacial velocity can be geometrically related to the process rate and the angle.

\[ V_{\text{int}} = V_h \sin \theta \]  

(4)

where \( V_{\text{int}} \) is the velocity of the interface, \( V_h \) is the process rate, and \( \theta \) is the solidification angle. Furthermore, the rate of solidification can be directly related to the amount of heat removed from the surface by

\[ \dot{m}h_{fs} = q_y x = h_{fs} \rho L V_{\text{int}} \]  

(5)

where \( q_y \) is the incremental heat flow from the surface of the wafer, \( x \) is the horizontal length of the solidification profile, \( h_{fs} \) is the latent heat of silicon, \( \rho \) is the density of silicon, and \( L \) is the length of the solidification interface. Combining Equation 4 and Equation 5 yields the relationship between the solidification angle and the heat flow from the surface of the wafer for a given process rate, as given by

\[ q_y = h_{fs} V_h \rho \tan \theta \]  

(6)

Chalmers claims that a solidification angle of only 1° is necessary to directionally propagate an existing grain.\(^9\) Figure 22 shows that as the speed of the process increases, the amount of heat that must be extracted to maintain a given small solidification angle scales linearly. For accelerated process speeds, the RX furnace will have to be designed to remove a substantial amount of heat from the surface of the wafer. Existing String-Ribbon processes are presently limited to \( \sim 40 \) mm/min, whereas RGS processes have yielded material at over 200 mm/min.
3.3.1 RX Furnace Design

Heat extraction from the surface of the wafer must be sufficient to maintain a solidification angle that will not result in island growth. The RX furnace must be designed to remove heat quickly from the wafer as it solidifies, as shown in Figure 23. This section focuses on how the radiation profile of the solidification zone was tailored to rapidly remove heat from surface of the wafer as it crystallizes.

\[ \dot{q}_y = \dot{q}_{\text{element}} + \dot{q}_{\text{insulation}} = F_e \sigma (\varepsilon_e T_e^4 - \varepsilon_{bp} T_{bp}^4) + (1 - F_e) \sigma (\varepsilon_{bp} T_{bp}^4 - \varepsilon_{ins} T_{ins}^4) \]  

where \( \dot{q}_{\text{element}} \) is the heat flow from the element to the wafer, \( \dot{q}_{\text{insulation}} \) is the heat flow from the insulation to the wafer, \( F_e \) is the radiation view factor from the element to the backing plate, \( \varepsilon_e \) is the effective emissivity of the element, \( \varepsilon_{bp} \) is the effective emissivity of the backing plate, \( \varepsilon_{ins} \) is the effective emissivity of the insulation, \( T_e \) is the temperature of the element, \( T_{bp} \) is the temperature of the backing plate, and \( T_{ins} \) is the temperature of the insulation. The two alterable
parameters in Equation 7 are the view factor from the element to the backing plate ($F_e$) and the emissivity of the insulation ($\epsilon_{ins}$).

The radiation view factor ($F_e$) is the element's radiation profile on the horizontal axis of the wafer. The radiation profile from the element to the wafer becomes more concentrated as the distance between the element and the backing plate diminishes, as shown in Figure 24. Concentrating the view factor between the substrate and the heating element reduces the radiation transfer from the element to the wafer as it travels further into the solidification zone. Reducing the amount of heat flow from the elements to the substrate stack in the solidification zone allows the wafer to cool and solidify more quickly. Therefore, to minimize the heat flow from the heating elements to the backing plates in the solidification zone, the spacing between the heating elements and the wafer must be minimized.

![Figure 24: View factor from the element to the backing plate as function of the elements distance from the substrate](image)

The surface roughness and emissivity of the insulation govern how fast heat is removed from the wafer in the solidification zone. If the surface of the insulation material is rough, it will scatter incident radiation from the backing plate to a cooler region of the furnace. If the insulation material has a low emissivity, then it will reflect the majority of the radiation incident on its surface. Low emissivity insulation therefore has a lower temperature than high emissivity insulation.

An insulation material that has both a low emissivity and a high surface roughness removes will remove heat from the wafer faster than other insulation choices. As shown in the qualitative ray
tracings in Figure 25, this insulation type scatters incident radiation from the wafer away from the solidification zone to regions of the furnace with a lower temperature.

Figure 25: Ray tracing illustration of the radiation profile at the solidification zone. The low emissivity insulation reflects incident radiation at the same wavelength. High emissivity insulation emits the radiation spectrum of its temperature profile. High surface roughness results scatters heat from the backing plate to cooler regions of the furnace.

A zone-melting furnace was constructed to remove heat quickly from the wafer at the solidification zone. The hot zone consisted of four sets of closely spaced silicon carbide (SuperSiC©) heating elements that exhibited working temperatures up to 1690°C in ambient atmosphere. The low emissivity, high surface roughness insulation material used was mullite, and the interior of the furnace is lined with a rectangular quartz tube to limit contamination. The temperatures of the elements are monitored by three independent dual colored pyrometers that are positioned over the elements. These pyrometers feed directly into a LabView program which controls three phase-angle fired SCRs. Typical operating conditions for running samples at 100 mm/min require the elements to be at ~1680°C, which requires each set of two elements provide ~200 W at 240 V.

3.3.2 RX Furnace Characterization

As described by Equation 6, the heat flow from the substrate stack in the solidification zone dictates the solidification profile of the wafer. This section determines the magnitude of heat flow from substrate stack in the RX furnace.
To measure the amount of heat leaving the stack as the wafer solidifies ($q_y$), a thermocouple was sandwiched between two silicon carbide backing plates and shuttled through the furnace. For different process rates, the measured temperature profile of the RX furnace is plotted as a function of position in Figure 26.

![Measured Zone Melting Furnace Temperature Profile](image)

**Figure 26**: Thermocouple measurements of the zone-melting furnace at different process rates and temperature set points

Because silicon carbide does not undergo any phase transformation at the melting temperature of silicon, its temperature simply depends on the amount of heat leaving the substrate. The rate at which the silicon carbide stack cools is

$$q_y = \rho_{SiC} c_{SiC} t_{SiC} \dot{T}$$

where $\rho_{SiC}$ is the density of the SiC substrates, $t_{SiC}$ is the thickness of one silicon carbide substrate, $c_{SiC}$ is the specific heat of the SiC substrates, $\dot{T}$ is the rate of temperature change of a region of the backing plate.

The combination of Equation 8 and Equation 7 can predict the amount of heat flow from the silicon carbide substrate stack as it enters the solidification zone. Assuming that the temperature of the insulation is $1280^\circ$ C and that the elements are 3 mm from each side of the substrate stack, Figure 27 shows the expected respective heat contributions from the element and the insulation as a function of the backing plate’s position in the solidification zone.
Figure 27: Model of Heat Flow to Backing Plate as a Function of Position

Given the expected heat flow profile in Figure 27, the expected temperature of the silicon carbide substrate can be found by incrementally by

\[ T_{i+1} = T_i + \frac{q_y(T_{i+1}, x)}{\rho_{SiC} c_{SiC} t_{SiC}} \frac{V_H}{x} \]  \hspace{1cm} (9)

where \( T_i \) is the old temperature of the backing plate, \( T_{i+1} \) is the new temperature of the backing plate, and \( q_y(T_{i+1}, x) \) is the heat flow from the wafer as a function of position and the temperature of the backing plate. Equation 9 and Equation 7 can be used jointly to model the temperature profile of the silicon carbide backing plate as it enters the solidification zone. Figure 28 plots the model’s predicted temperature profile of the backing plate alongside the measured thermocouple data for a process rate of 40 mm/min.

Figure 28: Predicted and Measured Temperature of the Backing Plate as it Enters the Solidification Zone
Since the simulated temperature profile matches well with the measured data, the model seems to accurately simulate the radiation profile of the furnace. Therefore, this radiation model can now be tailored to simulate the heat flow from a substrate stack with the silicon wafer. The heat flow from the silicon carbide substrate stack that contains the silicon wafer will differ from the thermocouple measurement because the substrate stack will remain at the melting temperature of silicon as the wafer solidifies. Therefore, the heat flow from the stack with the wafer will be respectively greater because the temperature difference between the substrate stack and the furnace will not decrease as the latent heat from the wafer is removed. Figure 29 simulates the heat flow from the substrate stack with the wafer as it enters the solidification zone of the RX furnace. Figure 29 assumes that wafer emits radiation through only one side.

![Single-Sided Heat Flow from Substrate Stack with Silicon Wafer Simulation](image)

**Figure 29:** Simulated heat flow from substrate stack with silicon wafer. Single-sided heat removal assumed.

Given the simulated heat flow from the substrate stack, the solidification profile of the wafer can be found by

\[
t_{i+1} = t_i + \frac{\dot{q}_x(1414, x) \cdot v_H}{\rho_s l_h f_s x}
\]

where \( t_i \) is the incremental thickness of the solidified wafer. Figure 30 shows the simulated solidification profile of the wafer in the RX furnace.
If it is assumed that the solidification profile in Figure 30 is linear, then the solidification angle of the wafer can be simply found by

$$\theta_{\text{solidification}} = \tan^{-1} \frac{t_{\text{wafer}}}{L_{\text{solidify}}}$$

(11)

where $L_{\text{solidify}}$ is the length of the solidification profile and $t_{\text{wafer}}$ is the thickness of the wafer.

Figure 31 shows the simulated solidification angle as a function of the process rate for the RX furnace. The desired 1° solidification angle occurs at process rate of approximately 60 mm/min. Furthermore, the solidification angle can be used with Equation 4 to find the interfacial velocity of the wafer at a given process rate, as shown in Figure 31.
In summary, this section develops a radiation model of the RX furnace that predicts the temperature profile of a silicon carbide substrate stack that was shuttled through the RX furnace. This radiation model was used to characterize the incremental heat loss from the substrate stack as the wafer solidifies in the RX furnace. This heat flow was related to the solidification angle of the wafer at different process rates in the RX furnace. Given the solidification profile of the wafer, the following sections will focus on limiting nucleation ahead of the growth interface.

3.4 Nucleation Suppression Ahead of Solidification Interface

Because the rate of solidification and the rate of nucleation are both dependent on the level of undercooling sustained in the melt, the probability of heterogeneous nucleation occurring on the surface of the capsule increases as the driving force of solidification increases. This section focuses on minimizing the nucleation rate ahead of the solidification interface.

This section will first relate the interfacial velocity of the wafer to the amount of undercooling sustained in the melt in front of the interface. Next, this undercooling will be related to the nucleation rate ahead of the interface. For a given process rate, capsule material, and heat flow from the wafer to the RX furnace, the nucleation rate will then be used to predict the relative number of grains on the wafer per unit area. This section will then identify and reduce the number of preferential nucleation sites so as to further reduce the number of grains on the wafer per unit area.

3.4.1 Relationship between Interfacial Velocity and Melt Undercooling

This section will develop a conceptual understanding of how the interfacial velocity of the wafer is related to the undercooling of the melt ahead of the solidification interface. The driving force of crystallization is proportional to the undercooling at the solidification interface and is given by:

\[-\Delta F_v = \frac{h_{fs} \Delta T}{V_m T_m}\]  \hspace{1cm} (12)

Where \(h_{fs}\) is the latent heat of fusion in J/mol, \(\Delta T\) is the undercooling, \(T_m\) is the melting temperature, and \(V_m\) is the molecular volume of the solid. Based on the driving force of solidification, an interface can advance by either discontinuous, screw dislocation growth or by continuous growth. Discontinuous growth occurs at low undercoolings where the interface advances via discrete steps. Continuous growth occurs when the critical radius of nucleation is comparable to the size of the advancing steps. This rapid growth mechanism is characterized by grain refinement and cellular growth and is not preferred. The critical driving force that distinguishes the boundary between the two growth mechanisms is

\[-\Delta F_v^* = \frac{\pi \sigma g}{a}\]  \hspace{1cm} (13)

where \(a\) is the lateral spacing of growth, \(\sigma\) is the interfacial energy between solid and liquid silicon, and \(g\) is the ordering parameter. The critical undercooling for silicon above which continuous growth would occur is
The lateral spacing of growth is approximately the distance between neighboring silicon atoms in the crystal lattice. Furthermore, Jackson et al. claim that high entropy of fusion materials, like silicon, have sharp interfaces. Hillig and Turnbull assert that for sharp interfaces, \( g \sim 1.1 \). For the parameters given in the Table 2, the critical undercooling for silicon is calculated to be 223° K.

\[
\Delta T^* = \frac{g \sigma V_m T_m}{a h_{fs}} \tag{14}
\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( g )</td>
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</tr>
<tr>
<td>( \sigma )</td>
<td>0.438 J/m²</td>
</tr>
<tr>
<td>( V_m )</td>
<td>3.34 \times 10^6 m^3/mol</td>
</tr>
<tr>
<td>( h_{fs} )</td>
<td>50.2 kJ/mol</td>
</tr>
<tr>
<td>( a )</td>
<td>2.2 \times 10^{-10} m</td>
</tr>
<tr>
<td>( T_m )</td>
<td>1683 K</td>
</tr>
<tr>
<td>( D )</td>
<td>4 \times 10^{8} m^2/s</td>
</tr>
</tbody>
</table>

Table 2: Parameters used to determine the growth mechanism for silicon

This calculation is consistent with undercooling studies performed by Li et al., as shown in Figure 32. Because experiments performed by Appapallia show that encapsulated silicon wafers typically nucleate well below this level of undercooling, the solidification interface is likely to advance in the RX process by screw dislocation growth.

**Figure 32:** Undercooling studies reveal that silicon does not exhibit the grain refinement typical to continuous growth until the melt is undercooled beyond 220° K. Hillig and Turnbull relate the velocity of screw dislocation growth in high entropy material to the undercooling of the interfacial melt by

\[
V_\infty = \frac{3D h_{fs} \Delta T}{a R T^2} \tag{15}
\]

where \( D \) is the self-diffusion coefficient of liquid silicon given in Table 2. The screw dislocation velocity is related to the interfacial velocity by

\[
V_{int} = \frac{V_\infty a}{4 \pi r_c} \tag{16}
\]
where \( r_c \) is the critical radius of nucleation on the interface, given by

\[
r_c = \frac{\sigma}{\Delta F_p}
\]  

(17)

The relation between the melt undercooling and the interfacial velocity is

\[
V_{int} = \frac{3D_h f_s^2 \Delta T^2}{RT^2(4\pi)\sigma T_m V_m}
\]  

(18)

How the interface growth rate relates to the undercooling of the silicon melt is shown in Figure 33. This figure shows that only a small level of undercooling is needed to quickly propagate the interface. This will be important when discussing preferential nucleation sites in the next section.

![Figure 33: Interface Growth Rate as a function of the undercooling of silicon](image)

This section has related the level of undercooling in the silicon melt to the growth rate of the solidification interface. The next section will now relate the level of undercooling in the melt to the nucleation rate ahead of the interface.

### 3.4.2 Relationship between Melt Undercooling and Nucleation Rate

The probability of a nucleation of a new grain occurring ahead or on the surface of the solidification interface is dependent on the level of undercooling exhibited by the melt. The expression for a heterogeneous nucleation rate on the capsule wall is

\[
J = J_0 e^{-\frac{\Delta G_{het}}{kT}} * SA
\]  

(19)

where \( J_0 \) is a constant that scales linearly with the number of nucleation sites for heterogeneous nucleation available per unit area, \( k \) is the Boltzmann constant, \( \Delta G_{het} \) is the heterogeneous nucleation driving force for the critical radius of nucleation, \( SA \) is the surface area of the interface on which nucleation occurs, and \( T \) is the temperature at which nucleation occurs. \( \Delta G_{het}^* \) is the free energy of the critical radius of nucleation given by the expression
\[ \Delta G_{\text{het}} = \Delta G_v V_{\text{silicon}} + A_{l/s} \sigma_{l/s} = f \left( \frac{h_{fs} \Delta T}{V_m T_m} V_{\text{silicon}} + A_{l/s} \sigma_{l/s} \right) \]  

where \( \Delta G_{\text{nuc}} \) is the energy of reduction achieved by the nucleation of a particle, \( \Delta G_v \) is the is the volumetric-free energy difference between the solid and liquid phases, \( V_{\text{silicon}} \) is the volume of solidifying silicon, \( A_{l/s} \) is the interfacial area between the solid and liquid/substrate interface respectively, \( \sigma_{l/s} \) is the interfacial energy of the solid and the melt/substrate, \( h_{fs} \) is the latent heat of fusion, \( \Delta T \) is the amount of undercooling experienced by the melt, and \( T_m \) is the melting temperature. The critical radius of nucleation is associated with the apex of the free energy curve and can therefore be found by differentiating Equation 12 and setting it equal to zero

\[ \frac{\partial \Delta G_{\text{nuc}}}{\partial r} = 0 \]  

\[ r^* = \frac{2 \sigma}{G_v} = \frac{2 \sigma V_m T_m}{h_{fs} \Delta T} \]  

\[ \Delta G_{\text{het}}^* = f \left( \frac{16 \pi a^3 V_m^2 T_m^2}{3 h_{fs} \Delta T^2} \right) \]  

where \( \Delta T \) is the level of undercooling that can be sustained by the given capsule material, \( h_{fs} \) is the latent heat of silicon, \( T_m \) is the melting temperature of silicon, \( f \) is the heterogeneous compensation factor specific to the capsule material given by

\[ f = \frac{1}{2} - \frac{3}{4} \cos \theta_{SI} + \frac{1}{4} (\cos \theta_{SI})^3 \]  

where \( \theta_{SI} \) is the contact angle between the silicon and the capsule material. In a levitation suspension setup, Li et al. measured the interfacial energy between liquid and solid silicon to be .438 J/m\(^2\).[12] Quartz and liquid silicon have been documented to have a wetting angle of \( \sim 85^\circ \)[13] and SiN has been documented to have a wetting angle of \( \sim 42^\circ \) with liquid silicon.[14]

Figure 34 relates the relative nucleation rate of a given capsule material to the level of undercooling in the melt. The nucleation rates for each respective capsule material are normalized to a given number of nucleation sites so that the material properties can be respectively compared. A ‘rough’ surface is modeled to have three times the surface area of a ‘smooth’ surface, and therefore three times the nucleation rate.
Figure 34 shows that a SiN capsule would consistently have a significantly higher nucleation rate than a quartz capsule. Furthermore, the difference between SiN and quartz capsule’s respective nucleation rate grows with the level of undercooling of the silicon melt. Alternatively said, a SiN capsule that experiences a low level of undercooling would have comparable nucleation behavior to a quartz capsule at a high level of undercooling.

3.4.3 Grain Size in Wafer Related to Process Rate and Heat Extraction from the Solidification Interface

Up to this point, the following relationships have been forged. The heat flow from the substrate stack to the RX furnace and the process rate has been related to the interfacial velocity by Equation 5. The interfacial velocity of the wafer has been related to the undercooling of the melt by Equation 18, and the undercooling of the melt has been related to a material’s nucleation rate by Equation 19. Using these relationships, the number of grains that occur per unit area of the wafer can be found by dividing the rate of nucleation (particles/time) by the respective process rate (Area/time). For a given amount of heat flow from the wafer to the furnace in the solidification zone, the average number of grains in a wafer is

\[ \frac{N}{A} = \frac{J}{v_H} \]  

(25)

where J is the normalized rate of nucleation, N/A is the relative number of nucleation for a given surface area. Equation 25 can be used to determine the process rate for a given RX furnace to minimize the number of grains in a recrystallized wafer. As shown in Figure 35, an RX furnace should be designed to maintain a shallow solidification angle for a desired process rate to have the fewest total number of grains per unit area. This result is intuitive because a smaller solidification angle will result in a lower interfacial velocity for a given process rate. And a
lower interfacial velocity requires less undercooling of the melt, which results in a lower nucleation rate.

![Normalized Nucleations per Area for Different Solidification Angles with Smooth Capsules](image)

**Figure 35: Normalized number of nucleations per unit area for different solidification angles for different capsule materials**

Figure 35 shows that the number of grains per area initially has a proportional relationship with the process rate, but then declines after a critical point. This suggests that the process rate of the RX concept is limited by the amount of heat that can be extracted from the interface. Therefore, future RX furnaces can be designed using Figure 35 in combination with Figure 22.

The normalized number of grains per unit area of a wafer with a given capsule material is shown in Figure 35. The relative number of grains per unit area decreases significantly for the SiN capsule as the process rate rises.

However, for the existing RX furnace, the present theory can predict the number of grains per unit area for a given process rate and sample preparation. Figure 36 shows that for a process rate of 60 mm/min, a wafer recrystallized with a SiN capsule should exhibit ~10X the number of grains exhibited by a wafer recrystallized with a thermally grown oxide capsule.
Figure 36: Normalized number of grains formed per unit area of wafer for a given process rate for the measured heat flow from the RX furnace

The two wafers in Figure 37 qualitatively demonstrate this relationship.

Figure 37: SiN and Oxide encapsulated wafers recrystallized at 60 mm/min in the RX furnace

This section has developed a conceptual understanding of how the number of grains in a wafer relates to the capsule material, process rate, and radiation profile of the RX furnace. However, the nucleation rates found in this section scale with the number of preferential nucleation sites on the capsule, as described by Equation 19. Therefore, the next section will focus on the identifying and reducing the number of preferential nucleation sites on the oxide capsule ($J_0$) and the amount of surface area on which nucleation can occur ($SA$). The following sections will develop a conceptual understanding how these two parameters can be tailored to suppress heterogeneous nucleation.

3.4.4 Experimentally Observed Relationship between the Preferential Nucleation Sites on a Thin Oxide Capsule and the Nucleation Rate ($J_0$)
The heterogeneous nucleation rate on the capsule surface scales with the number of preferential nucleation sites per unit area. This section identifies the type of defect that typically triggers nucleation and experimentally develops methods to reduce this defect's occurrence.

For a given material, a preferential nucleation site is a defect that locally lowers the energy barrier to nucleation. A structural defect on the capsule can be a preferential nucleation site if its size is comparable to that of a nucleating particle. If a defect on the capsule is smaller than this dimension, it will congregate too few atoms to overcome the interfacial energy of a new phase and will therefore not trigger a nucleation. Defects that are significantly larger than this dimension will energetically resemble a flat surface and will therefore not preferentially trigger a nucleation. Varanasi claims that the size of a structural defect must be between one and fifty times the critical radius of nucleation for it to be a preferential nucleation site.

The critical radius, or minimum size of a stable nucleating particle, can be found by setting the differential of the free energy curve for nucleation to zero, as described by Equation 22. For a given solidification angle, the relationship between the critical radius of nucleation and the process feed rate is given in Figure 38. As shown, a structural feature that is between ~200 nm and 10 μm can therefore act as a preferential nucleation site for process rates of ~60 mm/min. Reducing the number of structures that are comparable in size to the critical radius of nucleation will reduce the overall nucleation rate.

![Critical Radius of Nucleation for a Given Process Speed, θ = 1°](image)

**Figure 38: Critical radius of a nucleating silicon grain for a given solidification angle**

Two types of structural features are typical on the capsule of the wafer. The first one occurs when the wafer melts and locally pulls the oxide capsule inward, as shown in Figure 39. However, the size of this deformation is typically on the order of 10s of microns and generally very smooth, making this site less likely to act as a preferential nucleation site.
Figure 39: Partially melted silicon RX wafer with texture etching. The encircled ‘speckles’ are small melt pools that thin down and deform the capsule locally.

The quartz powder release layer is a more likely source for preferential nucleation sites. Structures that are on the order of 10 microns can be created by the multiple point contacts made between quartz powder release layer and the capsule. Furthermore, an irregular layer of quartz powder can increase the amount of interfacial area between the melt and the oxide capsule, making nucleation more likely.

A set of experiments were conducted to isolate the mechanism by which the quartz powder release layer influences the nucleation rate. The first experiment involved recrystallizing two samples with and without a thermally grown oxide capsule. Both samples were confined by a quartz powder release layer of the same thickness. As shown in Figure 40, the wafer without an oxide capsule conformed more readily to the geometry of the quartz powder release layer, resulting in more interfacial area between the melt and quartz. The wafer encapsulated in a thin oxide, on the other hand, did not conform as readily to the release layer, but instead made small point contacts with the powder.

Figure 40: Conformation of the wafers to the topology of the quartz powder
Of the two recrystallized wafers, the sample with the oxide capsule exhibits much larger grains than that of the wafer without the capsule, as shown in Figure 41.

![Image of wafers with oxide capsule versus without]

**Figure 41: Wafers that were recrystallized with and without an oxide capsule**

The difference of grain structure in the two samples of Figure 41 could be attributed to the way the liquid silicon conformed to the silica powder. However, bare wafer samples with thicker quartz powder release layers demonstrated larger grains for the same furnace conditions, as shown in Figure 42. Because different powder thicknesses will not yield different surface roughness, these results suggest that another factor other than the interfacial area between the melt and the capsule is affecting the nucleation rate of these bare wafers.

As shown in Equation 19, the heterogeneous nucleation rate is determined by the temperature of the silicon melt. If there were a mechanism by which a region of the wafer ahead of the solidification interface could preferentially develop a local undercooling, the chance of that site nucleating before an existing grain propagated to that area would increase.
3.4.5 Experimentally Observed Relationship between the Number of Local Undercooling Sites and the Nucleation Rate

Figure 42 showed that another phenomenon other than the increased surface area of the quartz powder release layer results in the surface nucleation. This section will focus on identifying the thermal mechanism inherent to the quartz powder release layer that increases the nucleation rate.

When the liquid wafer is cooling and solidifying, the latent heat released from the wafer travels through the quartz powder layer to the substrate and then radiates to the furnace. An irregular thermal resistance between the wafer and the substrate may result in the melt locally undercooling ahead of the solidification interface, making that region more likely to nucleate a new grain.

A discontinuity in the dominant mode of heat transfer through the quartz release layer could result in a local undercooling. To determine the dominant mode of heat transfer from the wafer to the backing plate during solidification, the heat transfer coefficients for radiation and conduction were calculated using Equation 26 and Equation 27:

\[ h_{\text{conduction}} = \frac{K_c A_{\text{contact}}}{L_c A_{\text{surf}}} = \frac{K_c P}{L_c} \]  
\[ h_{\text{radiation}} = 4\sigma e_{\text{effective}} T_m^3 \]
where \( p \) is the porosity of the powder, \( K_c \) is the thermal conductivity of quartz, \( L_e \) is the thickness of the powder layer, \( \sigma \) is the Stefan-Boltzmann constant, \( \epsilon_{\text{effective}} \) is the effective emissivity between the wafer and the backing plate, and \( T_m \) is the average of the backing plate and wafer’s temperature. For a given set of assumptions about the thermal properties of the quartz release layer, Figure 44 shows that thermal conduction is the dominant mode of heat transfer.

![Heat Transfer Coefficient](image)

Figure 43: Heat transfer coefficients for radiation and conduction from the wafer to the backing plate during solidification.

Therefore, a conduction thermal resistance irregularity in the quartz powder release layer can result in a local undercooling ahead of the solidification interface. Specifically, a region of the liquid that has a significantly lower thermal contact resistance with the backing plate than the bulk of the melt will develop a local undercooling. How readily regions of the wafer locally undercool ahead of the solidification interface depends on both how readily the liquid makes contact with the most conductive regions. As shown in Figure 44, a region of the wafer is more likely to make contact with a thermally conductive region of the quartz release layer when it is not encapsulated in a thin oxide capsule. Because the oxide capsule spans highest, most thermally resistive points of the quartz powder, there are fewer resulting undercoolings than the bare silicon wafer.
Furthermore, the magnitude of the undercooling, and thus the rate of nucleation associated with a contact depends on the relative thermal resistance associated with that contact. A thinner quartz release layer will result in larger heat flow from the substrate to the region, resulting in a larger local undercooling. Therefore, sample in Figure 42 with the thick powder capsule may have larger grains because the magnitudes of local undercoolings in that wafer were less significant than those inherent to the thinner quartz powder capsule.

To isolate a section of the wafer from the surface roughness of the quartz powder release layer, an experiment was performed where sections of a bare wafer were not coated with quartz powder. As shown in Figure 45, the regions of the wafer that were not coated developed a natural oxide (~100 nm) as the wafer was heated up in the open air RX furnace. Once the wafer was melted, the unsupported oxide sagged down and made contact with the backing plate. This formed a small, uniform thermal resistance between that region of the wafer and the backing plate. The rest of the wafer was still susceptible to the non-uniform topography of the quartz powder.

Figure 44: Conformation of the wafers to the topology of the quartz powder and the corresponding thermal gradients

Figure 45: Illustration thermal shunt experiment
A single dendrite propagated the length of the channel where the wafer made contact with the backing plate. The region surrounding the channel, however, contains multiple small grains. Figure 46 shows that the imprint of the quartz release layer is absent from the region that made contact with the backing plate. And although it cannot be seen at this resolution, the texture of the backing plate is imprinted in this grain, defining the edges of the channel with an even thermal resistance. The results of this experiment support the theory that an even thermal resistance between the wafer and the backing plate will yield less thermal gradients, and thus cause fewer grains to nucleate.

![Figure 46: RX wafer that was re-solidified with a 'slit' release layer](image)

The channel that was created in Figure 47 had both an even thermal resistance between the wafer and the backing plate as well as a smoother surface than the surrounding regions of the wafer that were supported by the quartz powder.

This section developed a conceptual understanding of how the quartz powder release layer can thermally influence the nucleation rate of an RX wafer. Experimental evidence suggests that a non-uniform quartz powder can introduce localized undercoolings that can instigate the nucleation of new grains. It was shown that a thin oxide capsule can reduce the probability of the wafer coming in contact with high thermal conductivity areas.

### 3.4.6 Reducing the Nucleation Rate in Front of the Solidification Interface

The experimental evidence and conceptual understanding developed in the previous section suggests two process modifications to reduce the number of preferential nucleation sites. First, a more homogenous quartz powder release layer would provide fewer sites that would give rise to local undercoolings. Furthermore, the smooth topography would have less interfacial area on
which nucleation could occur. Figure 47 shows that the use of a finer quartz release layer in combination with a thin oxide capsule results in fewer grains in RX wafers.

Figure 47: 6” RX wafers with different release layer uniformities

The second process modification performed to reduce the number of nucleation sites was to thermally bias one side of the wafer to cool faster than the other. When heat flows through only one side of the wafer, the number of sites available for nucleation is reduced by a factor of two. The following analysis was used to determine the most effective method to thermally bias one side of the wafer to cool faster than the other.

A section of the wafer begins to cool down and solidify once the amount of heat it receives from the heating element is less than that which it radiates to the surrounding insulation. Therefore, the parameter that can best limit the amount of radiation transfer between the heating element and the wafer will be tailored to constrain the thermal profile in the surface direction.

To identify the most sensitive parameter for heat transfer from the heating element to the backing plate, a radiation circuit of the solidification zone was constructed. The radiation circuit in Figure
48 models the heating element as a thermal radiation source and the surface of the backing plate stack as a radiation sink. There are two radiation paths by which heat is transferred to the backing plate stack. The first is direct radiation from the heating element to the backing plate. The amount of heat transferred by this mechanism is a function of the view factor of the element and the emissivity of the backing plate. The second mechanism is via power reradiating and reflecting from the insulation to the backing plate stack. This mechanism is dependent on the emissivity of the backing plate and the insulation.

\[ Q = \frac{(e_2 - e_1)}{\left( A_1 F_{12} + \frac{1}{F_{13} A_1} + \frac{2(1 - \epsilon_{\text{insulation}})}{\epsilon_{\text{insulation}} A_3} + \frac{1}{F_{32} A_3} \right)^{-1} + \frac{1 - \epsilon_{\text{element}}}{\epsilon_{\text{element}} A_1} + \frac{1 - \epsilon_{\text{bp}}}{\epsilon_{\text{bp}} A_2} } \]

where \( e_2 \) is the radiation source from the element, \( e_1 \) is the radiation source from the backing plate, \( F_{12} \) is the view factor from the element to the backing plate, \( F_{13} \) is the view factor from the element to the insulation, \( F_{32} \) is the view factor from the insulation to the backing plate, \( \epsilon_{\text{element}} \) is the thermal emissivity of the heating element, \( \epsilon_{\text{insulation}} \) is the thermal emissivity of the insulation, \( \epsilon_{\text{bp}} \) is the thermal emissivity of the backing plate, \( A_{\text{element}} \) is the surface area of the element, \( A_{\text{insulation}} \) is the surface area of the insulation, and \( A_{\text{bp}} \) is the surface area of a region of the backing plate.

By manipulating the variables in Equation 8, the emissivity of the backing plate was identified as the parameter that most significantly affects heat flow from the element to the backing plate. As shown in the Figure 50, the rate of heat removal from a substrate with an emissivity of .2 was almost a factor of two lower than that of a substrate with an emissivity of .8.
Figure 49: Normalized power from element to the backing plate with varying design parameters

Liquid and solid silicon exhibit emissivity values of .18 [16] and .8 [17] respectively. Therefore, a partially solidified silicon wafer naturally creates an emissivity bias on the surface. The emissivity profile shown in Figure 50 could be created if one surface of the wafer could be exposed directly to the furnace while the other was coupled to a high emissivity refractive substrate.

Figure 50: Substrate mismatch results in an effective emissivity difference between the top and bottom of the wafer, creating an asymmetric thermal profile for crystallization

As discussed in Chapter 2, a top substrate is necessary to yield a planar wafer. Therefore, a top substrate that could optically expose the wafer to the furnace had to be used to contain the wafer. Because quartz is optically transparent for the relevant wavelengths as shown in Figure 51, a quartz substrate was chosen as the top substrate. A SiC substrate was used for the refractive substrate.
Figure 51: Radiation from black body curves for temperatures varying from 1200° to 1650° C separated by the transmission limitation of quartz.

The emissivity profile created by the mismatched substrates biases one side of the wafer to cool faster than the other. Figure 52 qualitatively illustrates the magnitude and direction of the heat flow that will result from the substrate combination. The indigo arrows illustrate the incremental radiation contributions from each surface to the furnace. The single amber arrow shows the resulting heat profile vector.

Figure 52: Relative heat flow magnitudes are qualitatively illustrated by the purple arrows. The orange arrow illustrates the resulting, combined heat flow vector.

To experimentally demonstrate that the mismatched substrate combination constrains biases the thermal profile, a gallium doped wafer was melted and re-solidified with mismatching substrates. Gallium has a high segregation coefficient with silicon and therefore readily segregates into the melt as the wafer solidifies. As the concentration of gallium increasingly accumulates in the melt, the incremental concentration of gallium that is solidified into the wafer increases as well. Therefore, the sheet resistance at different depths of the wafer will vary based on their local respective gallium concentrations.

A spreading resistance measurement of the recrystallized gallium wafer was performed by Solecon Laboratory. This measurement found the local sheet resistance of the wafer, which scales with the concentration profile of the gallium, as a function of depth. As shown in Figure 53, the concentration of gallium was significantly higher on one side of the wafer than the other. This implies that the wafer preferentially solidified from the side with the refractive substrate.
Figure 53: Spreading Resistance Measurements performed by Solecon Laboratory to determine the solidification profile of the wafer

Wafers that were recrystallized with the mismatched substrates demonstrated much larger grains than wafers with matching refractive substrates, as shown in Figure 54 below. These results support the concept that biasing the wafer to preferentially cool on side minimizes the nucleation rate.

Figure 54: RX wafers crystallize at 60 mm/min in zone melting furnace with (a) matching SiC/graphite plates and (b) mismatched substrate quartz/silicon carbide
4. Minimizing Dislocation Counts

Stressing the wafer as it cools from the melting temperature of silicon to the brittle-to-ductile transition (BDT) temperature (~900° for silicon) will generate dislocations in the silicon lattice. Dislocations trap impurities in energy wells and prevent their removal during post-process POCLing. Wafers with large numbers of dislocations typically have low internal quantum efficiencies (IQE) because the impurities trapped in the bulk of the lattice promote the recombination of excited carriers. Figure 55 shows how the impurity concentration in the wafer, reflected by the recombination factor $\Gamma$, becomes less detrimental to the IQE as the dislocation density is decreased to $\sim 10^4$ dislocations/cm$^2$. Therefore, to minimize the recombination activity in the bulk of the wafer, it is aspired for RX wafers to exhibit an average dislocation density of $10^4$ dislocations/cm$^2$.

![Figure 55: Measured and experimental relationship between the IQE and dislocation density of a silicon wafer. The gamma denotes the recombination factor which includes the effects for different levels of impurities.][18]

Dislocations are created when a stress field is imposed on a discontinuity in the crystal lattice like a grain boundary or another existing dislocation. Stress fields are typically created by thermal gradients along the length of the wafer. The most problematic discontinuity in an RX wafer is associated with a region stressed with a burst-out. The following sections discuss the measures taken to reduce the number of discontinuities in the wafer and the magnitude of thermally induced stress gradients in the wafer.

4.1 Reducing the Number of Structural Defects in the Wafer

Structural features on the surface locally amplify stress fields and thus lower the energy required to generate a dislocation. The two types of structural features on RX wafers that have been observed to generate dislocations are grain boundaries and areas through which burst outs ruptured, as shown in the dislocation etches in Figure 56.
Figure 56 a) dislocation etch of three colliding grains. The black speckles are etched out dislocations. b) Cross-section of an RX wafer with the top and bottom side of the wafer shown above and below. The black speckling on the ‘Dislocation Zipper’ show how grain boundaries. c) Dislocations around a burst out feature that was created by entrapped melt.

Because impurities migrate to areas with high dislocation counts during the diffusion of the pn-junction, burst out regions typically exhibit heightened recombination activity. The LBIC image in Figure 57 shows that burst-outs between colliding grains are electronically more problematic than the surrounding grain boundaries. This figure contains an RX wafer that has been fully processed into a cell where the red and blue regions respectively indicate low and high recombination activity. Furthermore, burst out regions may have a number of shunts across the depletion region of the cell, which reduces the open circuit voltage of the cell. This particular cell had a fairly low open circuit voltage of only .574 V which may be attributed to the combined effects of impurities and dislocations at these burst-out regions. Other reasons for the low open circuit voltage may be that the wafer contains saturated levels of oxygen.
As shown in Figure 58, burst-outs are created when two grains with a concave solidification profile collide. As the contained melt solidifies and expands, the surrounding wafer is either significantly stressed or a portion of the melt 'bursts out' from the wafer. Burst-outs between colliding grains can be avoided by having a single-sided solidification profile.

Both the frequency of burst-out regions and number of grain boundaries are reduced by the single-sided thermal bias imposed on the wafer and nucleation suppression process modifications discussed in Chapter 3.

4.2 Mitigating Thermal Gradients

Thermal gradients stress the wafer at temperatures above the BTD temperature of silicon. For each dimension, thermal stress in the wafer can be given by the expression below.

$$\sigma_x = E\epsilon_x = E\alpha\Delta T_x$$  \hspace{1cm} (29)

where \(\sigma_x\) is the stress generated in the wafer, \(E\) is the Young’s modulus for silicon, \(\epsilon_x\) is the thermal strain in the wafer, \(\alpha\) is silicon’s thermal expansion coefficient, and \(\Delta T_x\) is the thermal gradient in the wafer. To minimize the thermal gradient experienced by the wafer as it cools
from the melting temperature to the BTD temperature, two process modifications were made. First, the RX furnace was extended to create a more gradual cooling thermal profile. Second, the thermal resistance between the wafer and the refractive substrate was minimized to increase the heat flow along a thermal gradient.

4.2.1 Furnace Modifications

Thermal gradients along the length of the wafer that can generate dislocations develop in the furnace after the solidification zone. Thermal gradients arise because more heat is removed from one region of the wafer than another. Figure 59 illustrates that insulation reduces the thermal profile along the length of the wafer because radiation emitted from one area of the substrate is reflected back to another region of the substrate. Because the insulation of the furnace has a low emissivity and high surface roughness, the amount of heat that leaves a region of the wafer is not significantly affected by temperature profile of the insulation. Instead, the temperature profile of the refractive substrate is determined by how readily radiation reflected from the insulation can escape to the environment. Therefore, the length of the insulation tube determines how significant the thermal profile of the furnace is.

![Figure 59: Ray tracing of heat from refractive substrate to environment](image)

The cooling zone of the furnace was therefore extended, as shown in Figure 60. This extension would provide an additional thermal buffer between the backing plate stack and the ambient temperature, thereby reducing the thermal gradient upon cool down.
Lifetime measurements and dislocation counts of samples that were crystallized in the furnace with the new cooling extension showed mild improvement, as shown in Table 3. Lifetime measurements were performed on samples after a phosphorous gettering step (no surface passivation).

<table>
<thead>
<tr>
<th>Sample</th>
<th>Cooling Tube?</th>
<th>Heater?</th>
<th>Lifetime Range (μs)</th>
<th>Best Average Dislocation Density (#/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>No</td>
<td>No</td>
<td>1.4-5.3</td>
<td>1.32 e5</td>
</tr>
<tr>
<td>53</td>
<td>Yes</td>
<td>No</td>
<td>2.9-6.4</td>
<td>1.1 e5</td>
</tr>
<tr>
<td>52</td>
<td>Yes</td>
<td>Yes</td>
<td>3.8-8.1</td>
<td>9 e4</td>
</tr>
</tbody>
</table>

Table 3: Lifetime measurements and dislocation counts of samples with different furnace modifications

4.2.2 Minimizing Thermal Contact Resistance

The low emissivity insulation reflects the radiation emitted from the substrate stack to other regions of the furnace and eventually to the environment, as shown in Figure 60. The primary contribution of the cooling tube extension is reducing the temperature gradient of the insulation and not the amount of heat that is reflected away from the substrate stack. Therefore, the temperature of an incremental region of the wafer temperature is primarily dependent on the amount of time that it spends outside the solidification zone, as shown in Figure 61.
If it is assumed that the incremental radiation heat flow from a region of the wafer is constant, then the temperature gradient that develops along the length of the wafer can be approximated by:

$$\Delta T_{\text{transverse}} = \frac{(t_i - t_{i-1})}{m_{\text{Stack}} c_{\text{Stack}}} \left[ q_{\text{rad}}^{\text{surface}} + q_{\text{cond}}^{\text{transverse}} \right]$$

where $\Delta T_{\text{transverse}}$ is the thermal gradient in the transverse direction of the wafer, $q_{\text{rad}}^{\text{surface}}$ is the incremental radiation heat flow from a region of the wafer, $q_{\text{cond}}^{\text{transverse}}$ is the conductive heat flow in the transverse direction of the wafer, $(t_i - t_{i-1})$ is the difference in time that neighboring regions have spent outside the solidification zone, $m_{\text{Stack}}$ is the incremental mass of the substrate stack, and $c_{\text{Stack}}$ is the specific heat of the substrate stack. Equation 30 and Figure 61 suggest that the thermal gradient in the wafer could be countered by increasing the conduction in the transverse direction of the wafer.

Heat flow in the transverse direction of the silicon wafer scales with the cross-sectional area normal to the transverse direction of the wafer. Because the cross-sectional area of the refractive substrate is ten times that of the silicon wafer, heat flow could be substantially increased if good thermal contact could be forged between the wafer and the substrate. As shown in Figure 63, the quartz powder release layer acts as a thermal resistor between the wafer and the backing plate.
Figure 62: Thermal circuit for silicon wafer demonstrating two parallel paths for heat flow. The first path is through the silicon wafer; the second is through a much thicker SiC/graphite substrate.

To counteract a thermal gradient in the wafer, the thickness of the quartz powder release layer must be minimized. To determine how sensitive heat flow through the substrate is to the thickness of the quartz powder release layer, the following assumptions were made. Neglecting the dimension coming out of the page, the amount of heat transferred through the wafer is given by the equation below.

\[ Q_{\text{wafer}} = \frac{\Delta T k_w t_w}{L} \]  

(31)

where \( k_w \) is the thermal conductivity of silicon at 1200° C, \( t_w \) is the thickness of the wafer (200 \( \mu \text{m} \)), and \( L \) the characteristic length of the thermal gradient. This length can be approximated to be the thermal diffusive length of silicon, which can be found by

\[ L = 2\sqrt{\alpha t} \]  

(32)

where \( \alpha \) is the thermal diffusivity of silicon and \( t \) is the characteristic time, assumed to be .1 seconds. Assuming that the cross-sectional area of the quartz release layer through which heat is conducted is half of the thermal diffusive length, the amount of heat transferred through the substrate backing plate is

\[ Q_{\text{graphite}} = \frac{\Delta T L}{\frac{t_{\text{powder}}}{k_{\text{powder}}} + \frac{t_{\text{graph}}}{k_{\text{graph}}}} \]  

(33)

where \( t_{\text{powder}} \) is the thickness of the powder, \( k_{\text{powder}} \) is the thermal conductivity of the powder (assumed to be .6 W/m²K), \( t_{\text{graph}} \) is the thickness of the graphite, and \( k_{\text{graph}} \) is the thermal conductivity of the graphite at 1200° C. The ratio ‘R’ compares the magnitude of heat flow through the substrate to the heat flow through the wafer. A large value of R results when heat flow through the substrate is significantly larger than that through the wafer.

\[ R = \frac{Q_{\text{graphite}}}{Q_{\text{wafer}}} \]  

(34)

Figure 64 shows how R becomes significantly larger as the thickness of the quartz powder release layer decreases. This figure shows that the two paths of heat flow are equivalent at release layer thickness of ~60 microns and that heat flow through the substrate becomes asymptotically more dominant as this layer is reduced.
Figure 63: Ratio of Heat Transfer through the Substrate vs. Through the Wafer for Different Quartz Release Layer Thicknesses

Figure 64 suggests that a 10 μm quartz release layer would result in significantly more heat flow along a thermal gradient than that of a 70 μm layer. Therefore, samples with varying quartz powder release layer thicknesses were recrystallized at 100 mm/min. It was found that the samples recrystallized with the thinner release layer had over an order of magnitude fewer dislocations than that of the samples with thicker release layers. Dislocation etches of the respective samples are shown in Figure 65.

![Dislocation Etch of Typical RX Samples Processed at 100 mm/min with Different Powder Thicknesses](image)

Figure 64: Dislocation etch of typical RX samples processed at 100 mm/min with different powder thicknesses.

The role of the backing plate in mitigating thermal gradients in the wafer was further investigated with another experiment where the wafer was spanned between two SiC/graphite backing plates that were separated by a small gap. Because the region of the wafer that spanned this millimeter size gap would not be capable of transmitting heat through the backing plate, this setup would prevent a specific portion of the wafer from using the SiC/Graphite plate to reduce thermal gradients. The μ-PCD lifetime map of the RX sample in Figure 66 shows that the region above the gap has distinctively poor electronic quality. Furthermore, even though the size of the gap was only a millimeter in distance, the electronic quality of the wafer was affected even .5”
away from the gap. This drastic difference in electronic quality supports the idea that the thermally shorting the wafer to the substrate can substantially mitigate out thermal gradients in the wafer as cools.

![Image of Si Wafer and SiC/Graphite substrate](image)

**Figure 65:** Semilab µ-PCD lifetime map of an RX sample where an interrupt in the SiC/graphite substrate resulted in localized poor electronic quality.

A thinned quartz powder release layer reduced the number of dislocations in the bulk of the wafer to be on the order of \( \sim 10^4 \) dislocations/cm\(^2\). Furthermore, samples recrystallized with thinned quartz powder release layers did not exhibit heightened levels of dislocations around grain boundaries, as shown in Figure 67.

![Image of Dislocation etch](image)

**Figure 66:** Dislocation etch of RX sample recrystallized at 60 mm/min with a thin quartz release layer. The etch shows an example of there not being any increase in dislocation numbers around grain boundaries or twin structures.
5. Conclusions and Future Work

The proposed Direct Wafer/RX technology is a two step process for making high quality, inexpensive kerfless silicon wafers for photovoltaic cells. The purpose of the RX process step is to create a thermal profile that can melt and directionally solidify wafers with large grains and few dislocation densities. A novel furnace design and a novel substrate combination created a unique thermal profile that consistently yielded wafers that achieved this process goal.

A zone-melting furnace was designed to create a sharp, constrained radiation profile in the pull direction of the wafer to preferentially grow existing grains faster than a new grain can nucleate. This radiation furnace is unique in the following ways. First, it is made of only semi-conductor clean components. Second, it operates in air at temperatures up to 1650°C. Third, and most importantly, this furnace imposes a 30°C/cm gradient on the wafer (10X the gradient of conventional radiation tube furnaces) as it exits the hot-zone and begins solidifying.

To create a sharp directional thermal profile in the thickness of the wafer, the wafer was constrained with mismatched substrates (SiC and quartz) to create a biased emissivity profile on the wafer. The side of the wafer that interfaces with the refractive SiC substrate preferentially cools much faster than the opposing side. The sharp thermal gradient that is created by the zone-melting furnace and the mismatched substrate combination is critical to directionally growing large grains.

To minimize the number of stress induced dislocations and maintain the planarity of the wafer, the wafer was contained by an oxide capsule, a quartz release agent, and two substrates. The thickness of the quartz release layer was minimized to reduce the thermal contact of the wafer.
References


