Single-crystal Germanium Growth on Amorphous Silicon
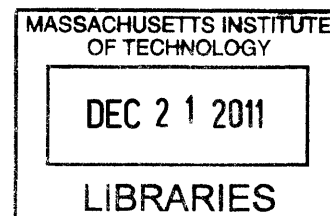
By

Kevin A. McComber

B.S. Materials Science and Engineering
B.S. Physics
Massachusetts Institute of Technology, 2005

Submitted to the Department of Materials Science and Engineering in Partial Fulfillment
of the Requirements for the Degree of

Doctor of Philosophy in Materials Science and Engineering
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Chair, Departmental Committee on Graduate Students

Single-crystal germanium growth on amorphous silicon

By

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ABSTRACT

The integration of photonics with electronics has emerged as a leading platform for microprocessor technology and the continuation of Moore's Law. As electronic device dimensions shrink, electronic signals encounter crippling delays and heating issues such that signal transduction across large on-chip distances becomes increasingly more difficult. However, these issues may be mitigated by the use of photonic interconnects combined with electronic devices in electronic-photonic integrated circuits (EPICs).

The electronics in proposed EPIC designs perform the logic operations and short-distance signal transmission, while photonic devices serve to transmit signals over longer lengths. However, the photonic devices are large compared to electronic devices, and thus the two types of devices would ideally exist on separate levels of the microprocessor stack in order to maximize the amount of silicon substrate available for electronic device fabrication.

A CMOS-compatible back-end process for the fabrication of photonic devices is necessary to realize such a three-dimensional EPIC. Back-end processing is limited in thermal budget and does not present a single-crystal substrate for epitaxial growth, however, so high-quality crystal fabrication methods currently used for photonic device fabrication are not possible in back-end processing.

This thesis presents a method for the fabrication of high-quality germanium single crystals using CMOS-compatible back-end processing. Initial work on the ultra-high vacuum chemical vapor deposition of polycrystalline germanium on amorphous silicon is presented. The deposition can be successfully performed by using a pre-growth hydrofluoric acid dip and by limiting the thickness of the amorphous silicon layer to less than 120 nm. Films deposited at temperatures of 350° C, 450° C, and 550° C show (110) texture, though the texture is most prevalent in growths at 450° C. Poly-Ge grown at 450° C is successfully doped n-type *in situ*, and the grain size of as-grown material is enhanced by lateral growth over a barrier.

Structures are fabricated for the growth of Ge confined in one dimension. The growths show faceting across large areas, in contrast to as-deposited poly-Ge, corresponding to enhanced grain sizes. Growth confinement is shown to reduce the defect density as the poly-Ge grows. When coalesced into a continuous film, the material grown from 1D confinement exhibits a lower carrier density and lower trap density than as-

deposited poly-Ge, indicating improved material quality. We measure an increased grain size from as-deposited poly-Ge to Ge grown from 1D confinement.

Single-crystal germanium is grown at 450° C from confinement in two dimensions. Such growths exhibit faceting across the entire crystal as well as the presence of $\Sigma3$ boundaries ({111} twins), with many growths showing no other boundaries. These twins mediate the growth of the crystal, as they serve as the points for heterogeneous surface nucleation of adatom clusters. The twins can form after the crystal nucleates and are strongly preferred in order to obtain appreciable crystal growth rates. We model the growths from the confining channels in order to find the optimum channel geometry for large, uniform, single-crystal growths that consistently emerge from the channel. The growths from 2D confinement show lower trap density than those from 1D confinement, indicating a further enhancement of the crystal quality due to the increased confinement.

This method of single-crystal growth from an amorphous substrate is extensible to any materials system in which selective non-epitaxial deposition is possible.

Thesis Supervisor: Lionel C. Kimerling
Title: Thomas Lord Professor of Materials Science and Engineering

Acknowledgments

To try to thank everyone who helped make this thesis a reality is nearly an impossible task, but if there's one thing to be learned from getting a PhD, it's that you should attempt the impossible.

To say that the epitome of graduate school is the obtaining of a degree is, however, to miss much of the point. I would like to take this space to thank the people who were not only instrumental in helping me obtain the degree itself, but also in ensuring that my graduate school experience was one of personal growth and enrichment.

In the summer of 2005, when I was searching for a research group to join, Professor "Kim" Kimerling stuck out as the clear choice for an advisor. I remember my first meeting with him: he asked me what I wanted to do for research and I said I'd like to make things and do hands-on work. With a faint but warming southern drawl, he said he had a CVD reactor I could tinker with, and I was sold. Kim is an inspiration for anyone pursuing materials science and engineering, and I deeply appreciate his mentorship. He has also been extremely supportive of my ventures in extracurricular student activities while in grad school, as he realizes the importance of non-scientific pursuits for one's personal development.

Playing Robin to Kim's Batman is Dr. Jurgen Michel, the resin that holds many students' and projects' fibers together. There have been numerous instances in which Jurgen has rescued me from the depths of confusion and/or despair, providing an island of calm in the storm of grad school. Always willing to chat about scientific, social, and even personal issues, Jurgen is akin to the uncle whom you're always happy to see and whom you're glad to have in your family so you can say you have some normal relatives.

Three more gentlemen – Prof. Chris Schuh, Prof. Carl Thompson, and Prof. Harry Tuller – also deserve recognition as willingly submitting to be on my thesis committee. As a first-year assistant professor in 2002, Chris Schuh was my undergraduate advisor when I started in MIT's Department of Materials Science and Engineering as a sophomore. Having him on my panel helps bring the MIT academic experience full-circle. Prof. Tuller is one of only a few senior tenured professors whom I've seen at the department socials, and he's always a pleasure to speak with, unless he's criticizing my work. Prof. Thompson is a deity in the world of semiconductor processing; I couldn't read more than two papers without seeing his work referenced. I have benefited greatly from his wisdom in pointing me to many useful resources and concepts, and I appreciate his insightful and timely help with all my questions.

The grease that helped keep our research group's gears turning for many years was Dr. Jifeng Liu, now an assistant professor at Dartmouth University. Jifeng was my graduate student mentor when I started in the Kimerling group in 2005, showing me how to operate all the necessary processing tools and indulging me as I tried to learn the Chinese language and stumbled through many mispronounced words with him. Jifeng is the quintessential mentor: extremely bright, patient, understanding, funny, and generous. It was a pleasure getting to know him and his wife, Xiaoxin, and I look forward to seeing their son as an MIT student when he's 12 years old or so.

While I realize a mentor is generally older than the pupil, I feel that is not the case in my relationship with Rodolfo Camacho. Rodolfo is a few years behind me in age but a few decades ahead in ability. While not mastering another foreign language or doing

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capoeira, Rodolfo has his nose to the grindstone in the lab and is cranking out results. On many occasions, those results were to help me with my work, though I was never in the position to return the favor. He has been extremely helpful in setting up lab equipment and helping to run the UHVCVD reactor, and our shared interest in fine distilled spirits comes as a bonus.

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Dr. Anat Eshed has been enormously helpful in maintaining our labs, and especially the UHVCVD reactor. She successfully calmed me down after my processing mistakes and cheered with me as we restored functionality after a reactor malfunction. She does a fantastic job keeping both the machines and the machine operators happy.

Mark Beals has been tireless in keeping our labs functioning properly and always looking for ways to improve our facilities. He's also not afraid to show his face at our social events and is perennially personable and encouraging.

Joining our group recently but nonetheless providing a lot of final-year help to me is Dr. Jonathan Bessette, a postdoc we exchanged with Dartmouth for Jifeng Liu. Jon has been more than helpful in the lab and has provided good conversation and perspective in the office.

There are many other members of our group I'd like to thank. Dr. Anu Agarwal has a notable sense of humor and often keeps the boys of the group in check. Xing Sheng has been a great officemate in the "Emat oasis" that is 13-4025. Jing Cheng and I leaned on each other for support through our classes, and she helped guide me through many parts of the final stretch of my thesis. I met Jianfei Wang in the Muddy Charles Pub on campus during grad student orientation and he's been fun to practice Chinese with, in exchange for some English lessons. Sarah Bernardis provided some pep during our core classes and was always good for an entertaining chat. Yan Cai performed many hours of manual labor polishing my samples in my final dash for crucial EBSD data. Daisuke Okamoto from NEC in Japan came to work with our group in 2009 and, though our reactor broke that summer, he made some useful measurements on our material. And there are many more past and present group members who deserve recognition, including Rong Sun, Xiaochen Sun, Dave Danielson, Dan Sparacin, Donghwan Ahn, Michiel Vanhoutte, Timothy W.C. Zens, Ching-yin Hong, Mindy Baughman, Juejun Hu, Winnie Ye, Lirong Zeng, Piotr Becla, Clara Dimas, and Samerkhae Jongthammanurak. It has been a pleasure working with them all.

The final member of our group whom I'd like to acknowledge does not have a graduate degree and isn't pursuing one, but she needs no such certification to leave an indelible mark on the lives of many in our group. Lisa Page is our group's administrator, consoler, cheerleader, heartwarmer, baker, truth-teller, and overall control center who gave me what was probably the best advice I received in grad school: "Everyone moves at their own pace." I doubt she knows how many times I've reminded myself of that simple but powerful sentence. A few days after Lisa started with our group, we had a group outing to go candlepin bowling. I think she was in a bit of shock when she found out what a bunch of PhD students are like in a social setting, and I wondered if she would want to keep her position. I can't really put in writing how glad I am that she did.

The staff members of the Center for Materials Science and Engineering Shared Experimental Facilities have been extremely supportive and helpful. Scott Speakman at the x-ray diffraction facility doesn't seem to mind that he has to explain the same thing to me multiple times, and he's always a good guy to chat with while taking a scan. I really appreciate his patience and instruction. Shiahn Chen and Yong Zhang in the electron microscopy facility helped produce a lot of great data, and Shiahn has been a good companion while spending time trying to figure out the new Helios system.

The staff at the MIT Microsystems Technology Laboratories have been nothing short of phenomenal. Paul Tierney's patience knows no bounds, but I'm pretty sure he's glad I won't be around the photo tools anymore. Eric Lim, Kris Payer, Bob Bicchieri, Vicky Diadiuk, Kurt Broderick, Pat Varley, Bernard Alamariu, Paudely Zamora, and Dennis Ward have all been helpful in getting some new processes to work, and they're fun to boot. Keep those MTL socials coming!

It is to the MIT Graduate Student Council (GSC) that I owe a vast number of my positive MIT experiences. I started my work with the GSC as a first-year grad student when I attended a meeting because I heard there would be free pizza. I ended five years later as the vice president, serving alongside Alex Hamilton Chan, Nan Gu, and Chuck Gammal as my fellow officers. They are some of my closest friends. I am honored to have been part of such a great tradition as the GSC, and to have come to understand what professionalism means alongside leaders like Leeland Ekstrom, Shan Wu, Shahriar Khushrushahi, Mireille Akilian, David Opolon, Oaz Nir, Johnna Powell, Paul Monasterio, Ulric Ferner, and Vivek Sakhrani. I could not have asked for more benefits from a meeting with free pizza...except maybe more pizza.

The GSC provided a springboard into another organization that greatly shaped my grad school experience: the National Association of Graduate-Professional Students (NAGPS). Through NAGPS I had the pleasure of working with Alex Evans, Jason Heustis, Jon Kowalski, Donna Dueker, and Paul Monasterio on rebuilding a national organization from the ground up.

The MIT Club of Boston has also been a great source of support for my event-planning tendencies, and I am indebted to the leadership there: Rich Moy, Mireille Akilian, David Provost, Mike Owu, Lina Morales, Jennifer Wong, and Michael Goldberger. They run a fine group.

I also worked with many MIT administrators who helped me develop my leadership capacity, including Heather Fry, Barrie Gleason, Jed Wartman, Paul Spangle, Alicia Erwin, Ike Colbert, Steve Lerman, and Steve Immerman. Thanks to them all for their service to students.

Many more friends have been instrumental in the whole process. I'd like to recognize Yoda Patta and Megan Brewster, my DMSE ladies who were always up for lunch and some good venting. Ivan Nausieda and Steve Boles were the first guys I really made friends with in grad school and they both beat me to the finish line, but I won't hold that against them. Thanks to Matt Smith for the very stylish SCBA demonstrations and the early-morning TEM sample prep help. Emily Peterson, Josh Krueger, Dave Russo, Melissa Webster, Jeff Povelaites, Joseph Kovac, Arlene and Roland Sargeant, and Maria Aglietti have all made the journey much more lively and enjoyable.

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My family deserves no small amount of praise. My "doting aunts" Lisa and Mary, my aunt Janie and her husband Rudy, and my uncle Larry and his wife Diane have been very supportive of all my endeavors.

My brother Scott has been a source of stability and inspiration as well. We've been great friends since high school and I'm always happy to reconnect with him when I'm home.

My mom and dad have encouraged my nerdy ways since the beginning, buying me math practice books in elementary school and supporting me when I told them in seventh grade that I wanted to go to MIT. Clarinet lessons, soccer practice, marching band performances, track meets, math competitions, Future Problem Solving trips, New Year's vacations, our wedding and reception, my past and upcoming commencements...it's hard to say how one's parents make a difference, because it's impossible to know where to start.

The person deserving the most credit is my wife, Eileen Peng. Eileen and I met at MIT in the summer of 2002 and she has since been my principal source of peace, inspiration, and joy. We were married on Killian Court, and I consider *that* my greatest achievement at MIT.

This thesis is for Eileen.

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Chapter 1: Introduction

1.1 Overview and Motivation

In April of 1965, Gordon Moore, an executive at Fairchild Semiconductor and a future co-founder of Intel Corporation, said of microprocessors that "[t]he complexity for minimum component costs has increased at a rate of roughly a factor of two per year" and that this rate could be expected to be nearly constant "for at least 10 years" [1]. Today, more than 45 years later, the semiconductor industry is still working furiously to stay on track with "Moore's Law," or the doubling of the component density on a chip every ~2 years. This thesis details a method that will help enable the integration of photonics with electronics for the continuation of Moore's Law into the foreseeable future.

With the on-chip dimensional shrink predicted by Moore's Law comes a host of challenges. As shown in Figure 1.1, the shrinking device size engenders significant penalties in the circuit delay. Though most metal interconnects in today's 45 nm and 32 nm nodes have shifted to the use of Cu/low-k technology, the advantage provided by optical interconnection is plainly seen. As light traveling through a waveguide (a "wire" that carries light) does not encounter the resistance-capacitance (RC) delays or heating seen in electronic interconnects, the use of optical interconnects integrated with electronic components, or electronic-photonic integrated circuits (EPICs), presents a viable method for the continuation of the device shrink necessary to hold true to Moore's Law.
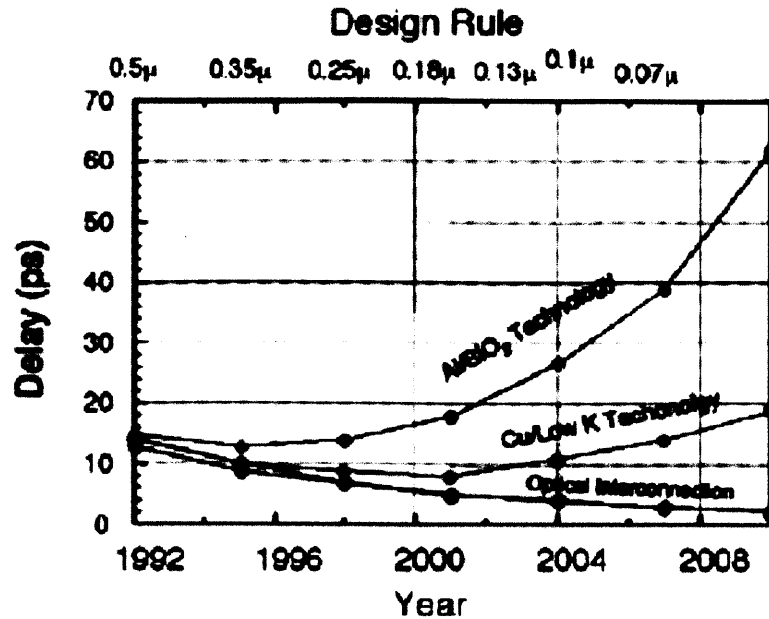
Figure 1.1. Signal transmission delay (over 1 cm) versus technology line width and time for three distinct interconnect technologies: aluminum metal and SiO_2 insulator, copper and low-k dielectric, and optical interconnects. From [2].

In the envisioned EPIC, electronic components (transistors, resistors, etc.) still perform the processing functions, as they do today. However, long-haul signal transmission among groups of electronic components will be done over optical interconnects instead of electrical interconnects, thus using the computing power of electrical devices while leveraging the superior transmission properties of optical interconnects. Figure 1.2 depicts the "H-tree" configuration of an EPIC using an optical clocking source and local electrical distribution of the clock signal.

Optical Clocking Source

Optical receiver (photodetector/TIA)

Local Electrical H-tree distribution
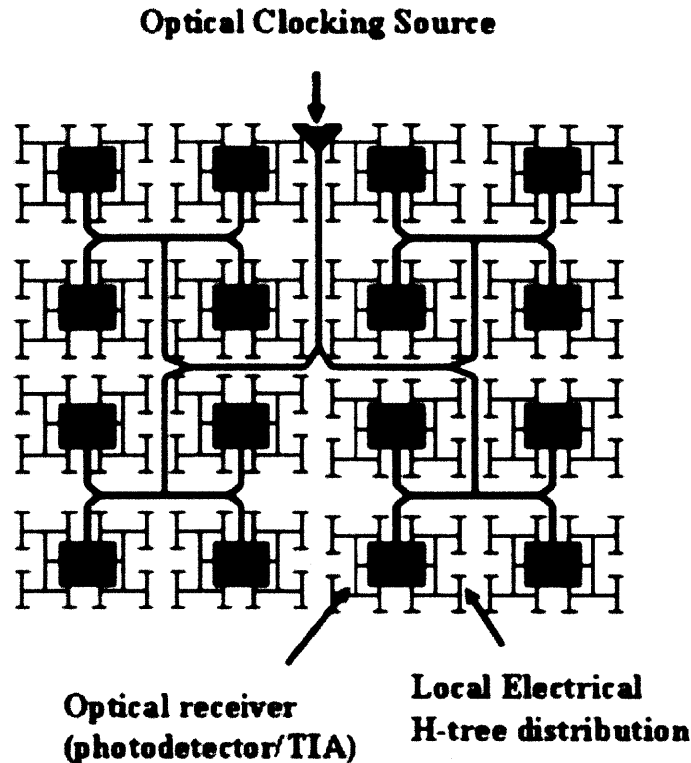
Figure 1.2. Schematic diagram of the H-tree architecture of an EPIC, showing the optical clocking structure monolithically integrated with electronics in a Si microprocessor. From [3].

As shown in Figure 1.3, an optical data bus comprises five basic units: the transmitter (modulator), the laser (light source), the waveguide, the photodetector, and the receiver. In this system, the transmitter encodes the laser light with the digital signal it receives from electronic components; this is done either by modulating the laser's drive current, or by shuttering the laser light with the laser in continuous and constant operation. This data-encoded laser light is transmitted over some distance by the waveguide and the light is detected by the photodetector. The photodetector converts the photonic signal to an electronic one; this electronic signal is conditioned by the receiver and sent on to further electronic devices [3].
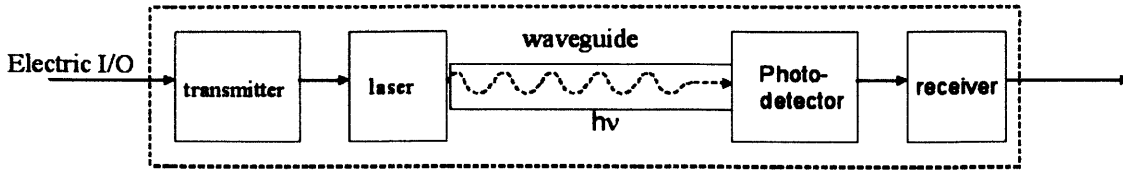
Figure 1.3. Schematic of the optical data bus. From [3].

The advantages of this system over an all-electrical bus are multifold: first, the transmission of light does not encounter the transmission delays seen by shrinking electronics, as depicted in Figure 1.1. Additionally, as in current fiber optic technology, multiple optical signals may be transmitted on a single optical interconnect, in a manner called wavelength division multiplexing (WDM). This is not possible with electronic interconnects, which may only carry one signal at any given time. Figure 1.4 shows the bandwidth gained by utilizing optical interconnects over electronic interconnects.
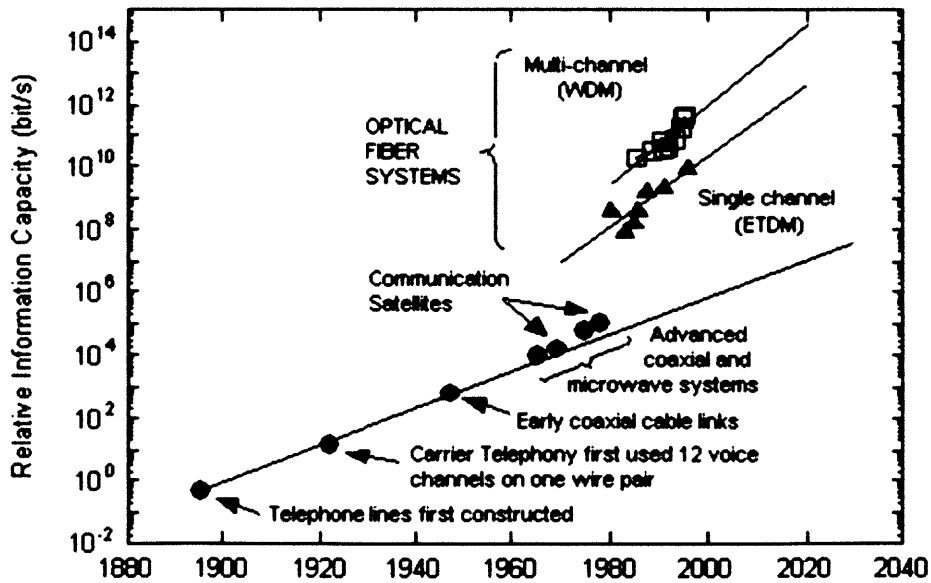
Figure 1.4. The improvement in information-carrying capacity of a single communications line with time. The paradigm shift from electronic lines to optical lines around 1980 enabled much higher data bandwidths. From [3].

To enable optical communications on a chip, the five principal devices used in an optical data bus must be developed to a point at which losses associated with the devices

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are low enough to justify the use of photonics. Research is ongoing in order to improve photonic devices' efficiencies.

Researchers have demonstrated [4-9] Si complementary metal-oxide-semiconductor (CMOS)-compatible lasers, photodetectors, and modulators; these devices are strong candidates for use in EPICs. The devices have all been made from germanium (Ge) or GeSi, as germanium has a number of attractive qualities. First, Ge has a lower processing temperature than Si, meaning that it can be deposited and annealed at temperatures that do not significantly affect Si devices. Second, Ge has a high absorption coefficient for wavelengths around 1550 nm, the wavelength used by fiber-to-the-home (FTTH) technology, due to Ge's direct band gap at 0.8 eV (corresponding to 1550 nm light). Finally, Ge has a higher hole and electron mobility than does Si, meaning it can serve as a relatively fast device in signal transduction applications.

Currently, photonic devices are fabricated at the chip's substrate level, where processing temperatures can exceed 900° C and the single crystal Si substrate is available to serve as the template for epitaxial deposition. Accordingly, the fabrication of photonic devices currently requires the high-temperature processing and single-crystal growth template afforded by the Si substrate.

The Si substrate level is becoming increasingly densely packed as electronic devices continue their dimension shrink, and the addition of photonic devices will only exacerbate the competition for substrate real estate. Compared to electronic devices, which have typical lateral dimensions on the order of tens of nanometers, photonic devices, with typical lateral dimensions on the order of micrometers to tens of micrometers, are extremely large. Thus, the photonic devices would ideally not reside on

the same chip level as the electronic devices, but would instead be fabricated on the

chip's interconnect (metal) levels, thus freeing up substrate space for further utilization

by electronic devices.

Figure 1.5 shows a schematic cross-section of a microprocessor chip stack,

illustrating the current state of electronic-photonic integration and the proposed method

of integration, with photonic devices fabricated at the chip's interconnect levels.
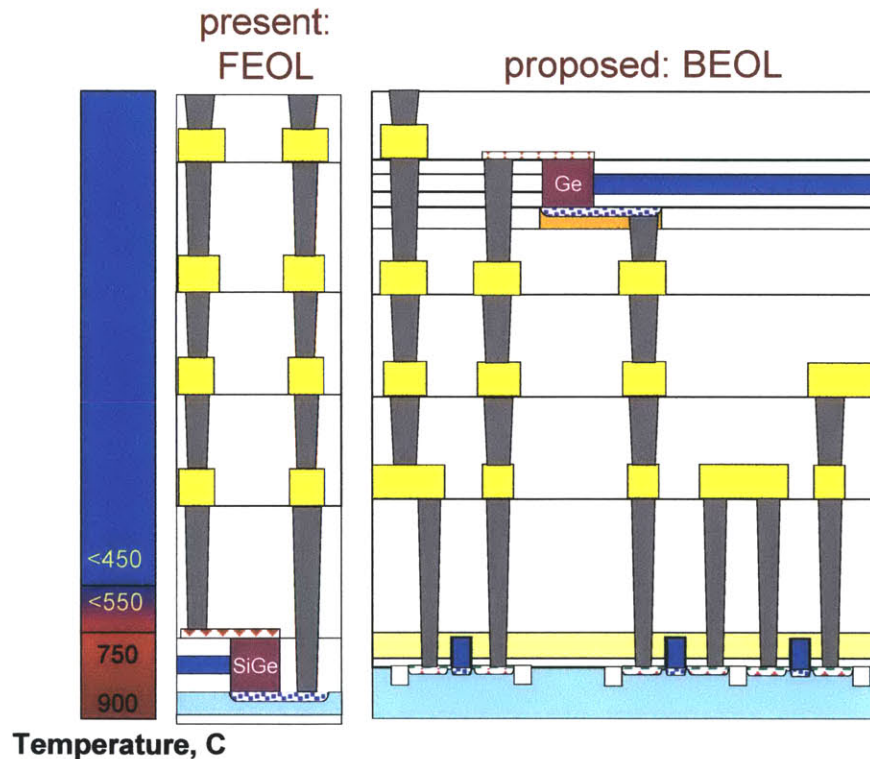
Figure 1.5. Schematic cross-section of a microprocessor chip stack, showing the typical maximum processing temperature with stack height, the present front-end-of-line (FEOL) photonic device integration, and the proposed back-end-of-line (BEOL) photonic device integration. Devices are in purple. From [10].

The back-end-of-line (BEOL) integration of photonic devices at the interconnect

levels of a microprocessor chip stack encounters two significant challenges. The first

main challenge is the lack of a single crystal template off which to perform epitaxial

materials deposition. The Si substrate level is the only level at which a single-crystal

substrate exists in monolithic processing (i.e. without the use of any bonding techniques), as single-crystal layer formation at higher levels would require the use of extremely high temperatures that are forbidden in the process flow. Thus, devices fabricated at the interconnect levels must be formed in a non-epitaxial manner. Devices deposited non-epitaxially typically have very high defect densities and these defects degrade device performance by inducing large leakage currents and significant carrier scattering.

The second principal challenge in BEOL photonic device fabrication is the low thermal processing budget. Processing temperatures must be kept to a minimum when working at the interconnect levels so as not to deteriorate the integrity of the metal interconnects; typically, interconnect-level processing is performed at temperatures under 450° C. Due to the low-temperature constraint, materials defects in devices cannot be easily annealed out or passivated, meaning that the defects are essentially "locked in" once the material is deposited.

Thus, the combination of a lack of epitaxy and a very low thermal budget means defects are readily formed in materials deposited at interconnect levels and these defects are very difficult to remove. This thesis will present a method of removing defects in non-epitaxially-deposited material (germanium) at low temperatures in a manner that is compatible with CMOS technology.

1.2   Outline of the Thesis

Chapter 2 will discuss the non-epitaxial deposition of Ge on Si; specifically, the process of Ge deposition on amorphous Si (a-Si) will be considered. The processes of nucleation and growth are discussed, as well as twinning and film texture development. The advantages and disadvantages of using polycrystalline materials for devices are

elucidated, and previous researchers' attempts to mitigate the deleterious effects of polycrystalline defects are highlighted.

Chapter 3 will cover initial work performed on the selective deposition of Ge on a-Si by ultra-high vacuum chemical vapor deposition (UHVCVD). Deposition and other processing parameters will be discussed, and films deposited between 350° C and 550° C will be examined. We demonstrate n-type *in situ* doping of poly-Ge and present results from samples of laterally-overgrown Ge on a-Si.

In Chapter 4, the phenomenon of 1D-confined growth of Ge will be introduced, and challenges associated with the fabrication of such a structure will be discussed. We observe an enhanced grain size and significant faceting of Ge grown from such structures, and material grown from 1D confinement exhibits a lower carrier density and higher photoluminescence intensity than does as-deposited poly-Ge.

Chapter 5 reports on the deposition of Ge in 2D confinement structures. The growth structure and its fabrication will be detailed, as will the results of growths from the structure. We find that the 2D-confined growths are mediated by atom adsorption at twin boundaries, and we present a model to predict the most desirable confinement structure geometries. Crystals grown from 2D confinement have an even lower defect density than do those grown from 1D confinement.

Chapter 6 gives a summary of the significant results of the thesis work, as well as suggestions for future research.

Chapter 2: Polycrystalline Ge Deposition

2.1   Motivation for polycrystalline material deposition

Polycrystalline semiconductors have long been used in many applications, most famously as highly-doped polycrystalline Si (poly-Si) serving as the "metal" gate in a metal-oxide-semiconductor field-effect transistor (MOSFET). They also find uses in applications such as solar panels and thin film transistors (TFTs), among others [11].

Polycrystalline (poly) materials are typically used when processing conditions are such that single-crystal material is either not attainable or not desirable. Unlike single-crystal materials, poly materials may be deposited directly on amorphous and poly substrates, and may be deposited in a wider range of temperatures than single-crystal materials; this means that poly materials may be deposited on a wider variety of potential substrates (such as glass [12-14] and plastic [15-17]) and it also means that processing costs can be lower. Additional steps used in many systems for the deposition of high-quality single-crystal material are often not required with polycrystalline material deposition, meaning that processing costs can be further reduced.

As discussed in Chapter 1, the fabrication of three-dimensional EPICs will require back-end-of-line (BEOL) processing of photonic devices at the interconnect levels, and this processing dictates low-temperature (<450° C) processing combined with the lack of a single-crystal substrate. The use of polycrystalline germanium suits this application well – it can be deposited at temperatures below 450° C on non-single-crystal templates, and is compatible with fiber-to-the-home telecommunications, as previously discussed.

This chapter will focus on the process of polycrystalline material deposition with an emphasis on polycrystalline germanium (poly-Ge) deposition, and relevant work on this material.

2.2   Fundamentals of polycrystalline germanium deposition

Polycrystalline material may be formed in a number of ways; the two most common methods in device fabrication are to deposit the material in a polycrystalline form or to crystallize an amorphous film into a polycrystalline film. The work performed for this thesis deals only with the former manner. The latter often requires the application of post-deposition annealing or another method of energetic excitation, and is generally difficult to perform in practice when attempting to achieve high-throughput manufacturing of semiconductor devices, and is also typically incompatible with CMOS-compatible BEOL processing constraints. This section will therefore focus solely on material deposited in polycrystalline form.

At the beginning of the polycrystalline material deposition, the depositing material's atoms adhere to the surface of the substrate and are then called "adatoms." The adatoms may subsequently desorb from the substrate surface, or they may remain attached if they group together in islands called nuclei such that their free energy is lowered by the satisfaction of some of their dangling bonds. The minimum size of a stable nucleus is called the critical nucleus size, and nuclei with sizes greater than this can grow with further material deposition.

The growth of stable nuclei leads to the formation of individual crystals, or grains, on the substrate. Adatoms may either continue to nucleate new layers on the growing grains in a manner similar to the formation of the initial nucleus, or they may attach at

points on the growing grain surface that present a non-uniformity compared to the rest of the surface; this can be compared to homogeneous nucleation versus heterogeneous nucleation, respectively, in a fluid system, for example. Such surface non-uniformities include ledges and kinks; a ledge is essentially the edge of a growing layer, and a kink is an atomic-level bend in that edge. A great deal of literature (see, for example, Ref. 18 and Ref. 19) has been published on the adsorption of atoms at ledges and kinks, and the sources of such features, and will not be covered here.

As multiple grains on a given surface grow larger, they eventually impinge on each other and form a continuous film. However, as they grow, each grain will develop a crystallographic orientation relative to the substrate surface plane, depending on the orientation of the grain's nucleus. Due to the underlying anisotropic nature of the material's crystallographic structure, grains with certain orientations grow more quickly in the direction normal to the substrate plane than do others. These fast-growing grains eventually overgrow the other, more slowly-growing grains, and come to give the overall film a dominant global orientation, or texture, which is that of the fast-growing grains [20]. For example, a film with the majority of its grains having their (100) planes parallel to the surface of the substrate is said to have (100) texture.

Because our process operates at a relatively low temperature (<70% of the melting point of Ge), this work does not need to consider grain growth after coalescence [21]. Growth from the vapor is taken to be the single source of grain growth.

The texture and morphology of a diamond cubic film (such as germanium, silicon, and diamond) that has not undergone twinning is determined by the α factor [22], or the ratio of the rate of growth on {100} and {111} faces, given by

$$\alpha = \sqrt{3}\,\frac{V_{100}}{V_{111}} \qquad\qquad (2.1)$$

where V_{100} and V_{111} are the normal growth rates of the {100} and {111} faces, respectively. The α value (and thus the specific preferred texture) for a given polycrystalline film is a function of the growth parameters, such as source gas, growth pressure, and substrate temperature used during the film's fabrication [22, 23]. Figure 2.1 shows the effect of varying α on the crystal's ideal shape (idiomorph). Growths with $\alpha \leq$ 1 will have a (111) texture, those with α = 1.5 a (110) texture, and those with $\alpha \geq 3$ will have a (100) texture. The orientation of the arrow in Figure 2.1 shows the direction of fastest growth for a given value of α; that direction is the normal of the plane that defines the resulting film's texture. The flat faces in the figure are the crystal's facets, which form in order to lower the crystal's surface free energy for a given value of α.

α **1**   **1.5**   **2**   **2.5**   **3**
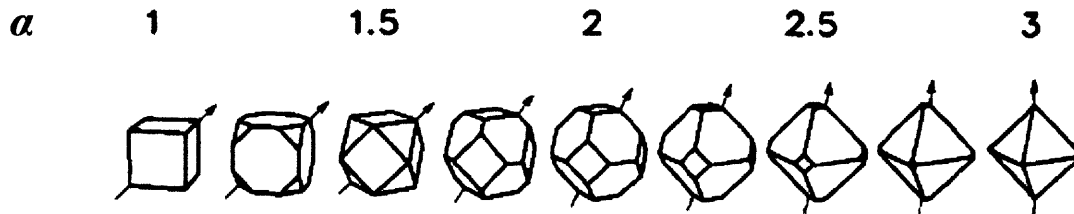
Figure 2.1. Idiomorphs of the diamond cubic structure for various values of α, ranging from cubic for $\alpha \leq 1$ to octahedral for $\alpha \geq 3$. The arrows indicate the directions of fastest growth. From [22].

Researchers have used analytical methods as well as computer models to predict the evolution of film properties with film thickness during the deposition process. Perhaps the most pertinent finding is that the average grain size evolves with film thickness according to

$$d \sim h^{b} \qquad\qquad (2.2)$$

where d is the average grain size, h is the average film thickness, and b is a value in the range of 0.4-0.5 [24]. Other predictions about grain size distribution, film surface roughness, and grain orientation distribution have also been made in the literature for various values of α [24].

For the purposes of simple illustration, Figure 2.2 shows the results of 2D simulations of grain growth, using $\alpha = \sqrt{2}\dfrac{V_{10}}{V_{11}} = \sqrt{2}$ as the two-dimensional version of α and V_{10} and V_{11} as the two-dimensional facet growth velocities. The figure clearly shows that nuclei oriented with their corners pointed in the direction of the substrate surface plane's normal tend to dominate the growth, due to the faster rate of growth from the corner than from any single facet (faster by a factor of $\sqrt{2}$).
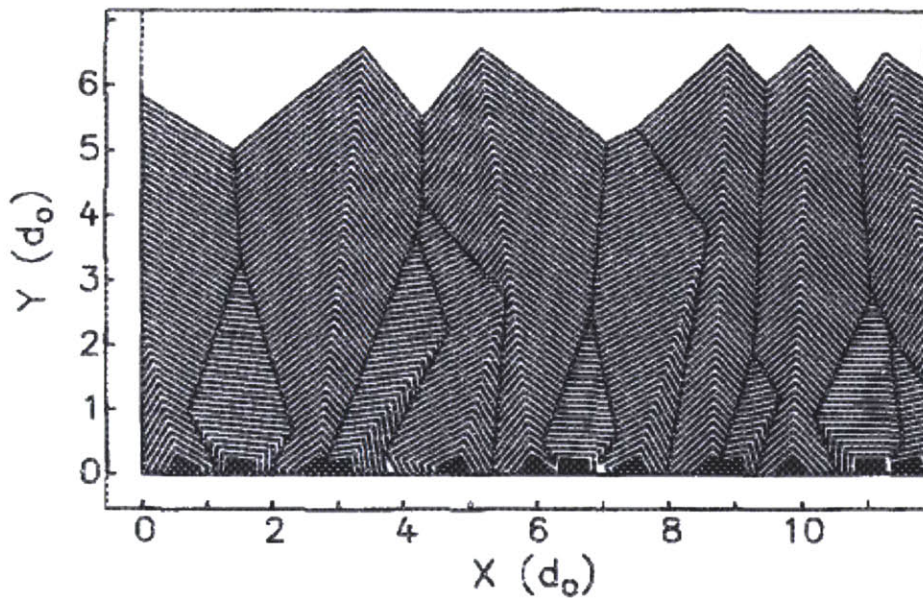
Figure 2.2. Computer simulation of the 2D growth of a polycrystalline film, with $\alpha = \sqrt{2}$, seen in cross-section. Both axes have been normalized to d_0, the average nuclei separation distance. From [25].

More complex 3D simulations were also performed [26] and the results are shown in the cross-section model of a film in Figure 2.3. In the figure, the apparent

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disappearance of certain grains is due to two factors. The first factor is the grain growth velocity anisotropy leading to grain selection, as previously described. The second factor is solely due to the method of display, in that we are looking at a three-dimensional phenomenon in two dimensions: some grains' growth directions have components normal to the plane of observation, and thus grow through the plane of the cross-section. This also accounts for the apparent "nucleation" of grains at various points in the through-thickness dimension of the film. This type of grain evolution during growth is indeed seen in reality, as depicted in Figure 2.4.
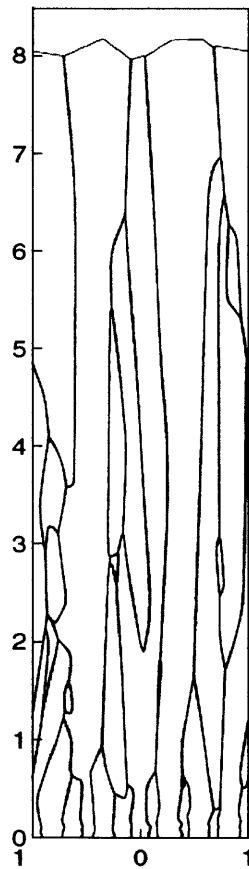
Figure 2.3. Computer simulation of the 3D growth of a polycrystalline film, with $\alpha = 2$, seen in cross-section. Axes' labels are arbitrary units. From [26].
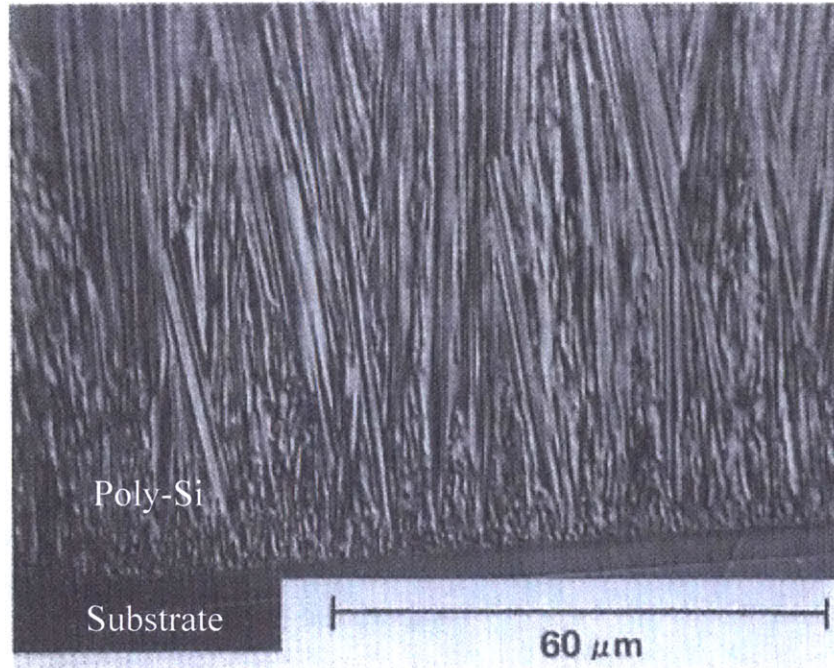
Figure 2.4. Polycrystalline Si cross-section SEM, showing the evolution of grains into a columnar structure. From [11].

Experiments with polycrystalline materials growth, however, have sometimes not conformed to the simulation results outlined above. One case is that of (110)-textured polycrystalline diamond showing only {111} facets, where the α factor modeling for this particular film would predict the presence of both {111} and {100} facets; a film with (110) texture has $\alpha = 1.5$, and from Figure 2.1 it is apparent that both {111} and {100} facets bound the idiomorph.

To understand the discrepancy, we must first understand some basics of crystallography. The {111} planes in a diamond cubic crystal are of principal importance because they have the highest planar atomic packing density, and thus the lowest surface free energy, of all planes in the crystal [27]. When the {111} planes form the boundaries of a growing crystal (its facets), the growth velocity in the directions of their normals is slow. Two grain orientations are theoretically possible within the confines of the {111}

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surface boundaries – these are growth with a <110> orientation and growth with a <100> orientation [25]. The <110> directions lie along the edges of the octahedron bounded by {111} facets, and the <100> directions span the octahedron between two opposite tips. Assuming equal normal growth velocities of the {111} bounding planes, the <100> directions should grow faster than the <110> because the enhanced growth rate seen at the octahedron's tips due to normal {111} growth is greater than that seen at its edges (Figure 2.5).

This purely geometrical argument, however, does not produce the correct result: polycrystalline diamond films were deposited with (110) texture and exhibited only {111} facets. Thus, another explanation for the growth mechanism of this crystal must be made.
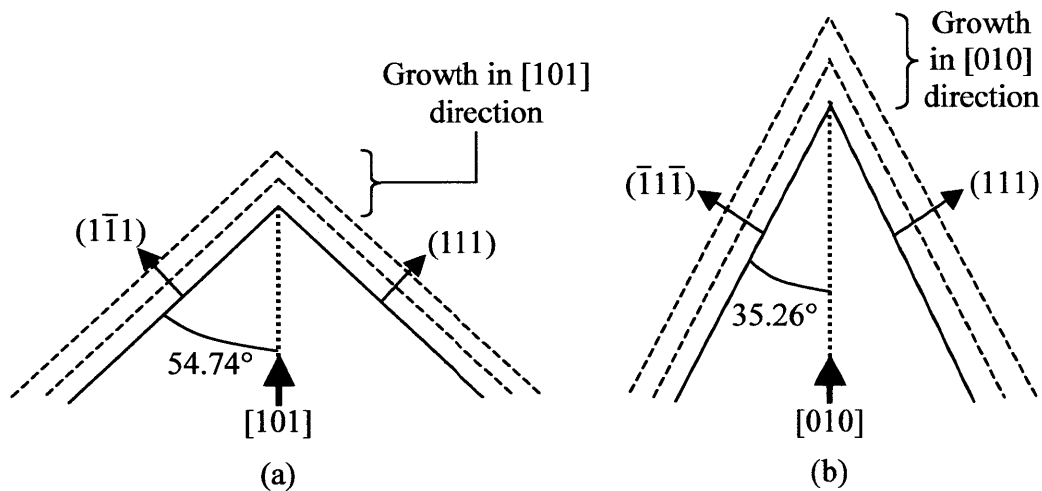
Figure 2.5. Growth of a crystal bound by {111} facets in the direction of (a) [101] and (b) [010]. In (b), the {111} planes are at a smaller incline to the growth direction than in (a) and thus the geometric growth rate enhancement in the direction indicated is greater in (b) than in (a) for a uniform normal growth rate on the {111} facets.

The concept needed to correct this apparent incongruence is that of twinning. In the case of growth twinning (twinning during crystal growth), the stacking sequence of

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atoms in the crystal is disrupted and the stacking continues to follow this stacking fault such that the resulting post-twin crystal lattice has an angular shift from that of the pre-twin lattice. The energy required to create a twin in a face-centered cubic (FCC) material is nearly zero [28] because twinning occurs on {111} faces where the post-twin lattice grows at an angle of 60° to the pre-twin lattice and requires no dislocations to form a coherent boundary.

In the case of FCC materials, if a grain is growing with <100> orientation and it twins, its orientation will no longer be <100>, as the <100> only form 90° angles with each other. However, if a grain is growing with <110> orientation and twins, it can still grow in a <110> orientation as some of the <110> form 60° angles with each other. Thus, twinned <100> orientations will no longer be favored for growth, but some twinned <110> orientations may continue to grow after twinning [25]. Twinning thus changes the preferred crystal growth orientation for {111}-bound FCC crystals from <100> to <110>.

As previously mentioned, the {111} planes bounding polycrystalline Ge grains have very slow normal growth, due to their low out-of-plane bond density and thus the dearth of sites on which adatoms may adhere. This slow growth normal to the bounding {111} planes will cause the grain growth to stagnate, as the slow normal growth of these planes impedes the growth of the crystal. However, as a twin on {111} in Ge requires essentially no energy, the material may form a series of twins that enhance the growth rate with negligible energetic penalty. From work on the growth of Ge crystals from the melt, it was suggested [29] that <211> crystals require the presence of multiple twin planes for perpetual growth, with growth occurring by the addition of Ge atoms at grooves caused by the intersections of {111} twin planes with the crystal surface. The

twins essentially provide heterogeneous surface nucleation sites on the Ge crystal at which another layer may start to form; multiple twins are required for long-range growth, as the growth on one twin eventually self-terminates. This idea was expanded [30, 31] to include <110> crystals grown from the melt, which exhibit only {111} faces and thus cannot be explained by the α parameter. It is believed that the <110>-oriented growth is actually the result of simultaneous growth in two <211> directions, mediated by adatom cluster nucleation at twin boundaries intersecting the crystal surface.

As growth from the melt and growth from the vapor phase both require crystal surface nucleation to continue the crystal growth, this twin-mediated growth phenomenon is expected to hold true for vapor-phase crystal deposition as well. This will be explored further in the experimental discussion in Chapter 5.

2.3   Grain engineering

While the flexibility of polycrystalline film deposition is an advantage for the use of such films, poly films do have drawbacks. The most serious disadvantage in the use of poly films in microelectronics and photonics is the films' defect densities; the defective regions between the individual grains are grain boundaries, commonly modeled as a series of dislocation cores [32]. The manipulation of grain boundaries has allowed materials engineers to control many materials' properties, but in the case of electronic and photonic materials, grain boundaries are generally seen as deleterious to device performance. Grain boundaries can lead to unwanted electronic carrier generation and recombination, unintentional dopant migration and aggregation, and carrier scattering [33]. They can also change the electronic character of the material; in the case of undoped

germanium, grain boundaries introduce acceptor levels in the band structure and cause otherwise-undoped material to become p-type [34-36].

Researchers have attempted to fabricate devices from as-deposited polycrystalline materials, and those most relevant to this thesis are made from polycrystalline germanium. Colace, Masini, and colleagues have been the most prolific in their publications about their attempts to fabricate poly-Ge photodetectors [37-40]. However, they found that their detectors suffered from extremely low responsivity, attributed to the high defect density in their active poly-Ge material. They suggested that grain boundary passivation may help alleviate device performance issues.

Other researchers have focused on methods of ameliorating the defects (primarily grain boundaries) in poly-Ge so as to improve device performance; these methods can be separated into high-T (non-BEOL-compatible) and low-T (BEOL-compatible) categories. The primary objective in both categories is the same: increase the overall grain size so that the grain boundary density (and thus the defect density) is decreased. (The grain boundary density has units of $\frac{area}{volume}$, or $\frac{1}{length}$.)

2.3.1 High-T grain engineering

The primary method of high-T polycrystalline grain size enhancement (other than just annealing) is that of graphoepitaxy, in which an artificial surface relief pattern in the substrate increases the surface energy of the film under consideration. This increased surface energy causes surface-energy-driven grain growth (SEDGG) of a crystalline film on an amorphous substrate that energetically favors a large-grained, consistently-textured film [41-43].

A secondary advantage of graphoepitaxy is that it results in films with consistent and controllable texture. This is due to the fact that the film's surface and interface energies drive the grain growth and these energies are also anisotropic, so that they favor certain crystallographic planes at the surface/interface and can even favor specific in-plane directions with respect to the surface patterning [41]. This degree of control over the crystallographic orientations of the grains gives added uniformity to the film.

While graphoepitaxy of Ge was able to achieve grain sizes of one to many microns, the processing was performed at 900° C for one hour [41]. Given the exponential dependence of atomic mobility on temperature, it is extremely unlikely that graphoepitaxy could have the same effect at temperatures below 450° C within a reasonable amount of time. Of course, some improvements to the graphoepitaxy process could be made, such as a finer periodicity of the substrate surface pattern, but this encounters significant processing challenges as the substrates become exceedingly difficult to fabricate for use in device manufacturing.

2.3.2 Low-T grain engineering

The work performed for this thesis focuses only on low-T (<450° C) processing, and the literature is bountiful in its recorded attempts to enhance the average grain size of a poly-Ge film at low temperatures.

A common method to enhance grain sizes while keeping the substrate at a low temperature is that of laser annealing [44-48]. The concept is fairly simple: instead of using thermal energy to produce larger grains, optical excitation from a laser light source provides the necessary energy to grow the grains. The light may even be intense enough to melt the material and allow it to re-crystallize. This method has a few significant

drawbacks, however. First, in actual device fabrication, the laser must only irradiate the areas of the wafer surface that are to form the devices; any radiation that strays from the devices can damage other parts of the substrate. Thus, to irradiate micron-sized photonic devices, fairly precise optics and controls would be needed. Couple this challenge with the need to scan the laser over possibly millions of devices on a single wafer and it becomes obvious that the non-batch processing nature of this method seriously limits its throughput and thus its validity for real-world manufacturing applications.

Another method of grain size enhancement uses an ion beam to impart added energy to the film and enhance its average grain size [49-53]. There exist two general methods of enhancing a film's grain size using ion beams. The first method is to bombard the film with the beam and, in combination with thermal annealing, use the ion beam's imparted energy to enhance the grains' sizes. It is believed that the energy is mostly absorbed in the form of greater defect densities, which allow grain boundaries to move and reduce their free energy, thus enhancing grain sizes. The second method is to use the ion beam to amorphize a large part of the film (i.e. turn the material from a crystalline to an amorphous structure) and then recrystallize the film by annealing. Due to ion channeling during the implant process (in which ions travel easily down certain crystallographic orientations and thus do not extensively damage the sample), the part of the film that is not amorphized is typically left with a consistent texture. Annealing the sample causes recrystallization of the amorphous part of the film, using the textured grains as seeds for recrystallization, leading to an overall film texture with enhanced grain sizes. This process also suffers from the fact that ion implantation must only be done in the areas of the devices, meaning the rest of the wafer must be masked, thus

reducing throughput. Furthermore, though the ion implantation can be performed at low temperatures, the process ultimately requires the application of an annealing step to mobilize defects and/or induce the recrystallization, which is incompatible with low-T processing.

A third and very well-documented method of enhancing grain sizes at low temperatures is that of metal-induced crystallization (MIC) and metal-induced lateral crystallization (MILC) [54-64]. In both MIC and MILC, a metal (typically nickel) is brought into contact with Ge or Si and annealed at a low temperature (typically up to 550° C for Ge). The metal induces crystallization of the semiconductor at these low temperatures, and the area of the semiconductor immediately beneath/above the metal is considered MIC material, while that not directly beneath/above the metal is considered MILC material. This distinction is depicted in Figure 2.6. In both processes, it is generally agreed that the metal atoms move through the semiconductor material and cause the formation of a crystalline phase. As the metal moves through the material, it leaves a crystalline wake that is large-grained compared to as-grown material (typically more so for MILC than for MIC). MILC fronts have been observed to have a dendritic nature, with a high concentration of metal in the dendrites.

MIC/MILC suffers from several setbacks as well. Generally, many of the metals used for the process are not CMOS-compatible and the resulting crystalline material is rich in metal. This metal is often detrimental to device operation, so a gettering step (in which the metal atoms are collected in some non-critical location) would be required to potentially bring the material into specifications for device fabrication. These two drawbacks, in addition to the extra processing steps required for metal patterning and the

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slow nature of the crystallization process, make MIC and MILC unfavorable for use in a manufacturing process.
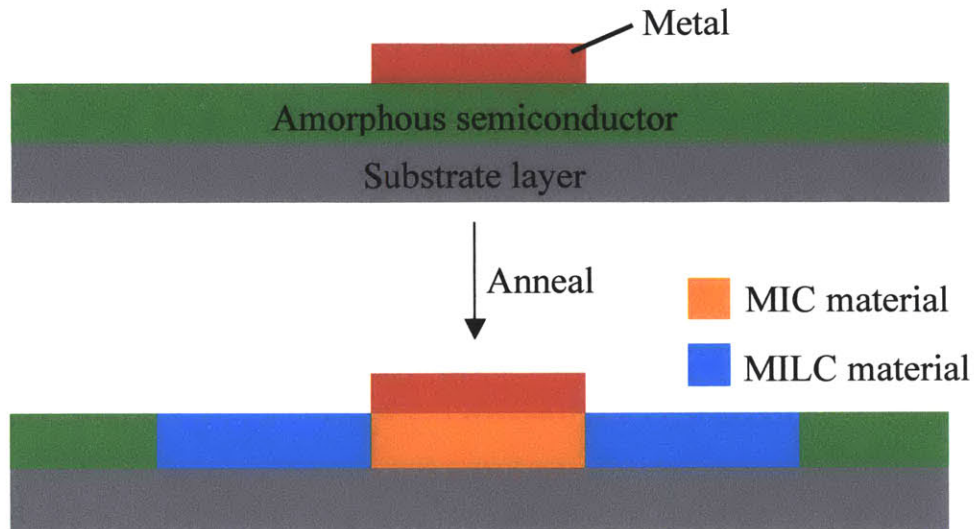
Figure 2.6. Schematic of the MIC/MILC process.

2.4 Chapter summary

The growth of polycrystalline material is an interaction among many factors, from nucleation through growth and texture formation. As-deposited polycrystalline germanium is typically unsuitable for device fabrication, due to the high defect density of the material that degrades device performance. While several possible methods exist for the enhancement of the grain size (and thus the reduction of the grain boundary density) in germanium, including a number of methods at low temperatures, all suffer from serious drawbacks that prevent them from being implemented in a high-throughput silicon CMOS manufacturing capacity.

This thesis will demonstrate a novel, CMOS-compatible method for grain size enhancement that is suitable for high-throughput BEOL manufacturing.

Chapter 3: Selective ultra-high vacuum chemical vapor deposition of germanium on amorphous silicon

3.1 The ultra-high vacuum chemical vapor deposition system

3.1.1 Motivation for using ultra-high vacuum chemical vapor deposition

Polycrystalline semiconductor materials may be fabricated using a variety of methods. The most common methods include chemical vapor deposition (CVD), evaporation, and sputtering; in the latter two cases, the film is often deposited as an amorphous film and annealed to give a polycrystalline film (see, for example, Ref. 50). Because this thesis concerns processes with thermal budgets not exceeding 450° C, such that annealing at high temperatures is not a possibility, focus has been placed solely on depositing Ge as a polycrystalline material and not attempting to anneal it from an amorphous state.

As the long-term goal of this work is to engineer material that is suitable for the fabrication of photonic devices (including photodetectors and modulators), the reduction of device performance-degrading defects in the germanium is the main objective. While Chapter 2 discussed the effects of grain boundaries on device performance, other defects may also play a role in determining the viability of device fabrication. We strive to reduce these defects as much as possible while still maintaining a process that has a reasonably high throughput, in order that the work may be applicable to manufacturing.

For this work, we chose to use ultra-high vacuum chemical vapor deposition (UHVCVD) to deposit ("grow") poly-Ge. The UHVCVD system idles at a very high vacuum (low pressure), on the order of 10^{-8} to 10^{-10} Torr, while not depositing material. This low base pressure reduces potential contamination of the material by maintaining an environment in which very few atoms of any type exist. In germanium, oxygen is of

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primary concern, as it introduces a donor state that can affect device performance [65]. The low pressure of the UHVCVD system thus reduces the potential for any oxygen contamination of the material and should give better device performance than another otherwise-identical CVD system with a higher base pressure.

CVD also affords another necessary feature: the selective deposition of Ge on Si. A common material used in CMOS processing is silicon dioxide, SiO_2, the natural oxide of Si that gives Si its competitive advantage over all other semiconductors for wide-scale applications. In a UHVCVD reactor, normal pressures, temperatures, and deposition rates give deposition of Ge on Si but not on SiO_2, as Ge forms GeO and other compounds with SiO_2 that are too volatile to remain adhered to the substrate [66]; this means SiO_2 can be used as a patterning template on the Si to define Ge features. An image of Ge selectively deposited on Si is given in Figure 3.1. To obtain patterned Ge features selectively deposited on Si, SiO_2 is first deposited on Si and subsequently photolithographically patterned such that predetermined areas of the Si substrate are exposed to the UHVCVD atmosphere. As the Ge precursor gas (germane, GeH_4) flows through the UHVCVD reactor, Ge deposits only on the Si and not on the SiO_2 – this is selective deposition, and has been used for decades to define Ge growth on Si.
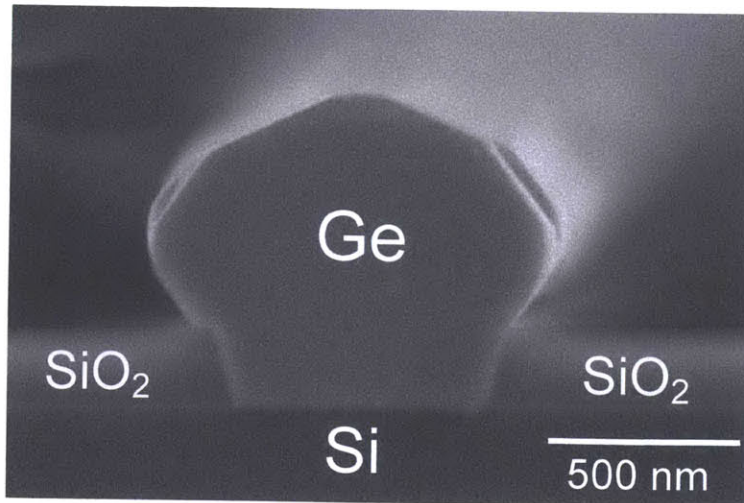
Figure 3.1. Cross-section scanning electron microscope image of selective Ge growth on Si by UHVCVD. Ge has been selectively and epitaxially deposited on the single-crystal Si, but not on the SiO$_2$.

3.1.2 Details of the UHVCVD system

Figure 3.2 gives a schematic representation of the main components of a functioning UHVCVD reactor chamber. The chamber is kept at a low pressure by the concerted effort of a number of pumps, typically including a dry pump (e.g. Roots pump) and multiple turbomolecular pumps. Heat can be applied in one of two manners: it can either be applied to the tube itself, such that the walls of the tube are heated and radiate heat into the deposition chamber (called a hot-walled CVD reactor), or the heat can be applied directly to the substrate through a device called a susceptor such that the walls are unheated (called a cold-walled CVD reactor). The hot-walled reactor can be used for batch processing (tens of wafers processed simultaneously), while the cold-walled reactor typically only processes one or a few wafers at a time.

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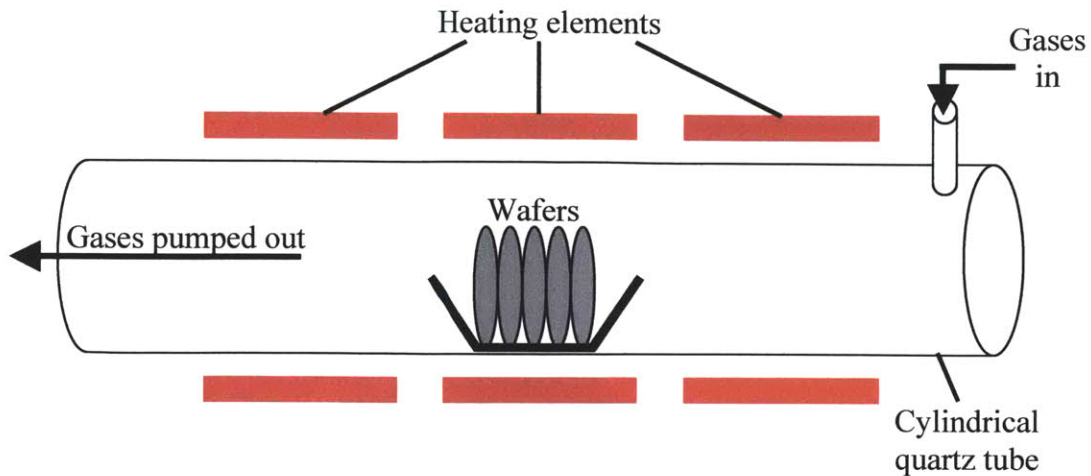
Figure 3.2. Schematic of the UHVCVD reactor chamber used in this work.

The deposition chamber can be maintained under constant vacuum by use of an adjacent load lock chamber. The load lock chamber is a small-volume enclosure that can be sealed off from the larger deposition chamber and vented to atmospheric pressure. While at atmospheric pressure, the sample can be placed in the load lock, and the load lock can then be pumped down to ultra-high-vacuum (or near-UHV). The seal between the load lock and the deposition chamber can then be released, and the sample can be transferred into the deposition chamber for processing. Once processing is finished, the sample is passed back to the load lock and the load lock is sealed off from the deposition chamber. The load lock is then again brought to atmospheric pressure and the sample is removed.

During the deposition process, gases are introduced into the reaction chamber from an inlet port near the load lock. For the deposition of Ge, germane (GeH_4) is commonly used and has been used in the present work.

The wafers in our UHVCVD reactor are placed such that their surfaces on which Ge is to be deposited are facing away from the inlet port, as this had been observed to

give more uniform and specular growth in work on epitaxial Ge on Si. As the chamber

pressure during deposition is around $4\text{x}10^{-4}$ mbar, the mean free path of a typical GeH_4

molecule is on the order of 10-100 cm at 450° C while the characteristic dimension of the

system (the tube length) is on the order of a few hundred cm, so the gas within the tube

cannot be reliably treated as a continuous medium (as the Knudsen number Kn is near 1),

but should be considered more as individual molecules in the chamber. After spending

time in the chamber, the gas molecules are evacuated from the tube by the pumps and

exhausted from the system.

3.1.3 Deposition parameters and considerations

Using UHVCVD as the deposition method and considering the utility of selective

Ge deposition on Si for the definition of devices in a CMOS-compatible process, we

employed amorphous silicon (a-Si) as the seed material for our work with poly-Ge. A-Si

is not only CMOS-compatible and works as a seed for UHVCVD Ge deposition, but it

also can be deposited by plasma-enhanced CVD (PECVD) at 350° C; this is within the

thermal budget of 450° C and is thus compatible with the BEOL work in this thesis.

The process flow for deposition of blanket (across-the-wafer, i.e. non-patterned)

deposition of Ge on a-Si is shown in Figure 3.3. In this process, we begin with a 6" Si

wafer (typically p-type, but doping type is not relevant) and use thermal oxidation of the

Si wafer to provide an insulating substrate on which to deposit the a-Si. It is accepted that

this step could easily be exchanged with a low-temperature oxide deposition (such as

PECVD SiO_2 at 400° C) without negative effects on the process. We then deposit a thin

layer of a-Si on the thermal oxide by PECVD at 350° C, and finally deposit poly-Ge on

the a-Si by UHVCVD with a 7.5 standard cubic centimeter per minute (sccm) GeH$_4$ flow. The poly-Ge growth rate is approximately 150 nm/min.

1. Start with 6" Si wafer.

2. Grow 500 nm SiO$_2$ by thermal oxidation.

3. Deposit thin (40-150 nm) a-Si layer by PECVD.

4. Deposit blanket poly-Ge layer.
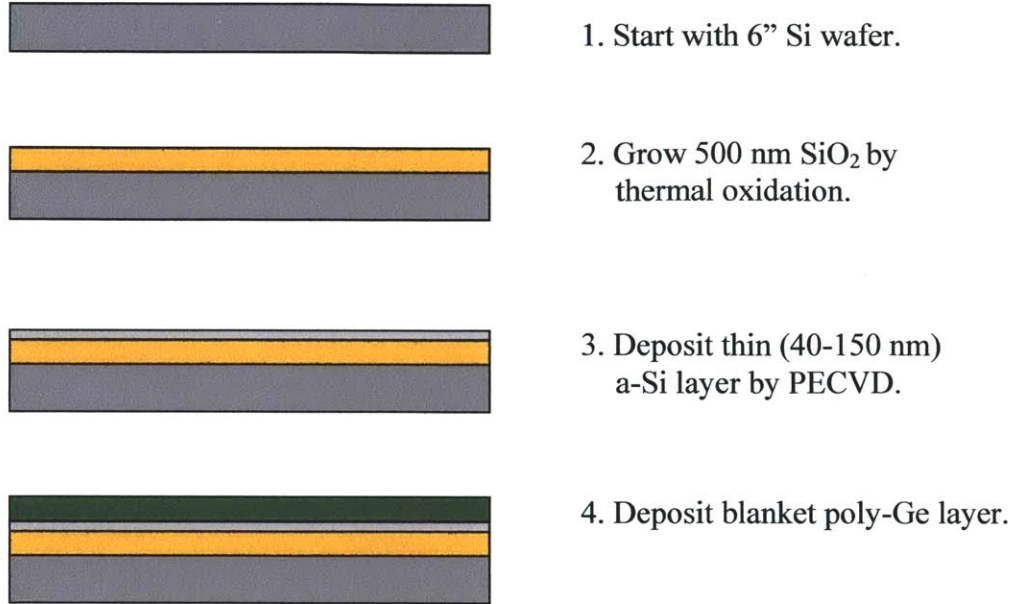
Figure 3.3. Process flow for the blanket deposition of Ge on a-Si, with the sample shown in cross-section. The figure is not to scale.

We had to investigate the capabilities of our UHVCVD reactor and the materials system to understand the limitations and possibilities of our poly-Ge deposition on a-Si. Previous researchers [4, 6-9] have done extensive work with Ge deposited epitaxially on single-crystal Si (c-Si), so this was taken as the starting base of our knowledge.

In the epitaxial deposition of Ge on c-Si, a buffer layer is grown first on Si at 360° C to a thickness of approximately 50-100 nm, and the temperature of the reactor is then ramped up to 650-750° C for subsequent deposition of a thicker Ge film. We began by utilizing this same process (low-T buffer and high-T growth), but on a-Si instead of c-Si, in order to understand how this process would be affected by the exchange of substrates. As shown in Figure 3.4, the buffer layer dewetted from the a-Si during the ramp to high temperatures. This occurs because the buffer is deposited as a polycrystalline material

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with significant free energy at the grain boundaries and surface. It is able to reduce this free energy by dewetting into islands (presumably of larger grain sizes or single-crystalline) as the surface atomic mobility increases with increasing temperature. The a-Si substrate may also crystallize into poly-Si, further enabling the breakup of the poly-Ge film. Since this method of processing exceeded the 450° C thermal processing budget and did not provide a material that was viable for measurement, further work using poly-Ge buffers at high temperatures, and buffers in general, was not pursued.
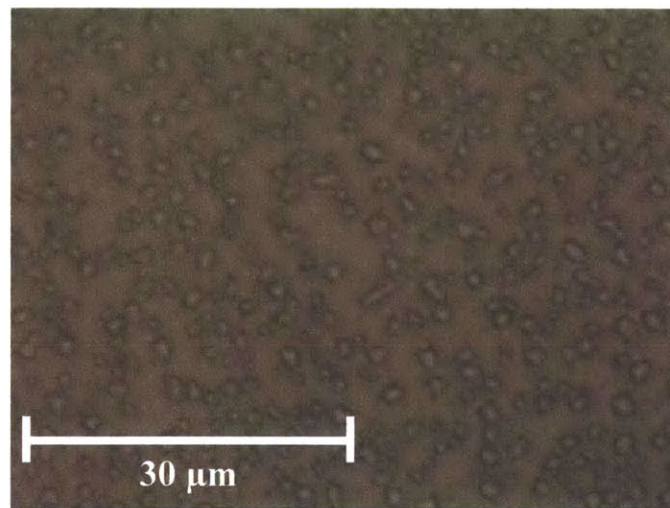
Figure 3.4. Plan-view optical micrograph of a representative poly-Ge buffer layer (~120 nm nominal thickness) on a-Si that has been annealed at 750° C for one hour. The film dewetted and formed islands as the substrate temperature increased.

Also employed in the epitaxial deposition of Ge on c-Si is a pre-growth RCA wafer clean which ends with a short wafer dip in a diluted bath of hydrofluoric acid (HF), 1:50 HF:deionized (DI) water. This dip has been shown [65] to increase the material quality of the deposited Ge by terminating dangling Si bonds with monatomic H and preventing the formation of native oxide on the Si surface; this process is called surface passivation. While epitaxial deposition of Ge on Si is extremely sensitive to the surface

state of the substrate, it was unclear whether deposition of Ge on a-Si would exhibit the same sensitivity.

Wafers with a thin (50 nm) layer of a-Si on top of oxide (as prepared in Figure 3.3, Steps 1-3) were passivated using HF dips of 0, 5, 10, 20, and 30 seconds; the time used for epitaxial Ge depositions is 30 seconds. Results are shown in the scanning electron microscope (SEM) cross-sectional micrographs of Figure 3.5. It is clearly evident that an HF passivation dip of some duration is necessary to preclude the formation of voids at the poly-Ge/a-Si interface. More discussion of the HF dip optimization will be given in Chapter 4.

Another issue encountered in selective epitaxial Ge deposition is that of fluoropolymer formation on the Si surface during the dry etch step used to define features in the SiO_2. A dry etch step (using reactive ion etching, RIE) is employed to remove oxide from the Si surface to allow for the selective deposition of Ge on the Si in specific locations. Previous research [67] found that a fluorocarbon polymer from the etch step remains on the Si surface when the dry etch is allowed to reach the Si surface; in our work with epi-Ge, this was mitigated by using an underetch such that a very thin (tens of nanometers thick) oxide was left on the Si, with a wet etch (buffered oxide etch or 1:50 HF:DI water) used to remove the remaining oxide. This method produces excellent (continuous and smooth) epitaxial films without any added thermal budget or complicated cleaning techniques.
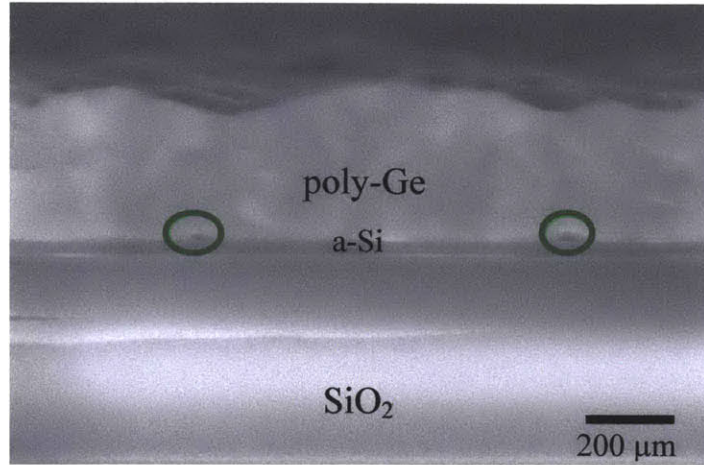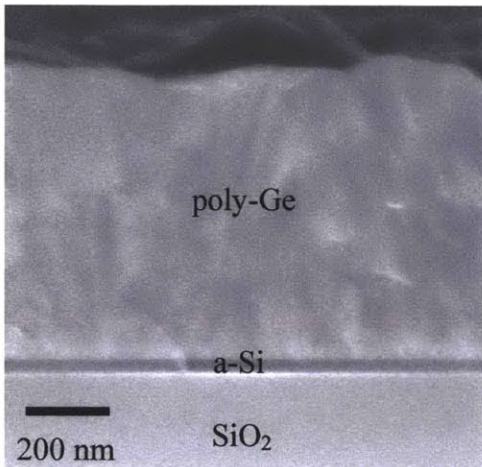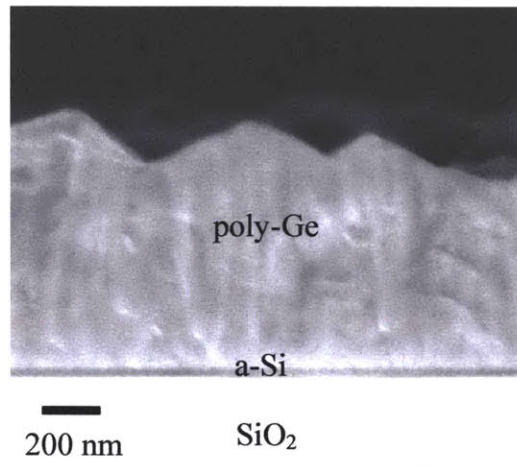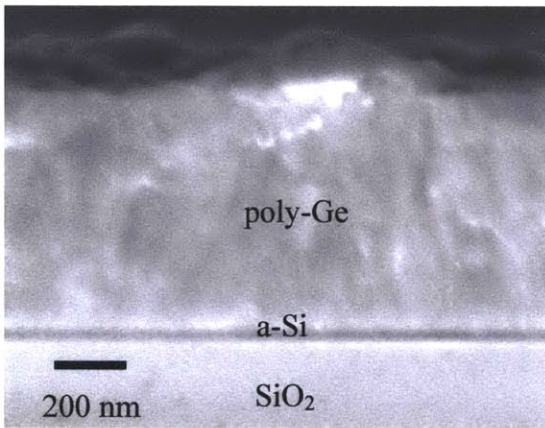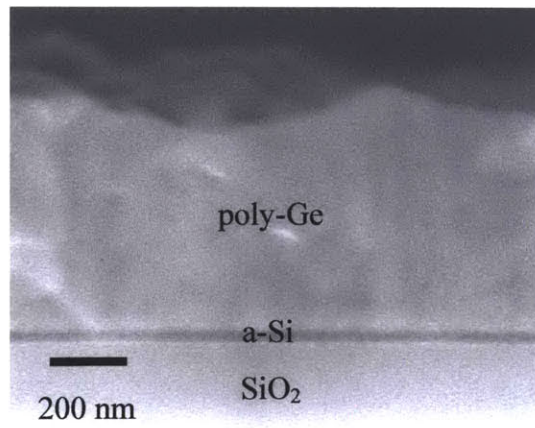
Figure 3.5. Cross-section SEM micrographs of poly-Ge films after deposition on an a-Si surface that was passivated with HF for (a) 0 sec; (b) 5 sec; (c) 10 sec; (d) 20 sec; and (e) 30 sec. The voids in (a), the sample which received no HF passivation, are encircled.

However, in the case of poly-Ge deposition, there seems to be no noticeable effect of an overetch in RIE on the resulting film morphology, so we are thus able to skip the wet chemical etch of the oxide in the sample preparation process, simplifying the process. It is likely that the poly-Ge growth is not as sensitive to surface contamination as is the epi-Ge growth, so there is no need to remove the residual fluoropolymer layer when performing poly-Ge deposition.

One concern that arose in the deposition of poly-Ge which was not a factor in epi-Ge growth was that of hydrogen (H) outgassing from the PECVD-deposited materials (a-Si and SiO_2). It has been documented [65] that PECVD-deposited materials, due to their low deposition temperatures and fast rates of deposition, retain a significant amount of H from the precursor gases (such as SiH_4 in the case of Si and SiO_2 deposition). This H is mobile at elevated temperatures and will diffuse out of the material into the material's surroundings, assuming its surroundings are comparatively depleted in H. In UHVCVD, the sample is introduced into a heated environment with a high vacuum, and the H will therefore diffuse out from the hydrogenated materials. This has been observed to cause film bubbling and cracking, as the H attempts to move to the sample surface but is impeded as it must diffuse through various layers; a plan-view optical micrograph of such bubbling is shown in Figure 3.6 and a cross-section SEM micrograph of a bubble may be seen in Ref. 65.
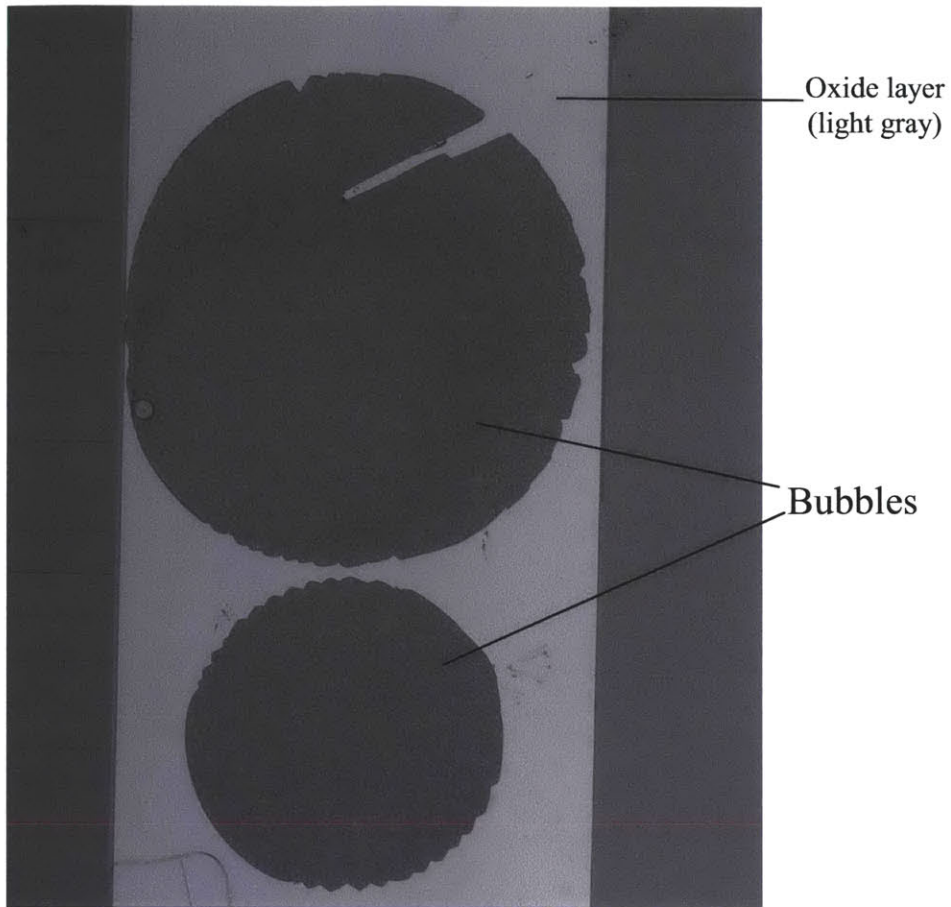
Figure 3.6. Plan-view optical micrograph of bubbles that have formed and subsequently delaminated in an oxide layer on a sample wafer.

As the samples used in our studies most commonly employ PECVD SiO_2 and PECVD a-Si, care was taken to ensure that neither material was subject to bubbling during poly-Ge deposition. As the total H content of the film increases with film volume, the film thicknesses were kept as minimal as possible. It was observed that, for PECVD a-Si films greater than approximately 120 nm in thickness, bubbling was evident across the wafer, and the bubbling severity increased with an increase in the film's thickness; films with a-Si thicknesses of approximately 500 nm were completely destroyed when heated to 450° C. Thus, a-Si films with thicknesses under 120 nm were used in this study.

Due to the outgassing of H and the fact that H_2 is a byproduct of the $GeH_4(g)$

decomposition into $Ge(s)$ on the a-Si surface (Eqn. 3.1), the presence of additional H in

the reactor may cause a decreased rate of Ge deposition; the added pressure may also

introduce flow effects in the tube. For these reasons, the samples were annealed *in situ*

before growth (at the growth temperature) for 1 to 2 hours in order to outgas H from the

PECVD films. H partial pressure in the reactor was monitored with a residual gas

analyzer (RGA) and the film growth was started when the H pressure had dropped to a

constant value.

3.2 Texture

3.2.1 Nucleation

X-ray diffraction (XRD) was performed using a Rigaku copper source

diffractometer with 185 mm detector length on blanket samples deposited at 450° C for

growth times varying from 45 minutes to 16 hours. The resulting peak heights of the

(111), (220), and (311) planes were observed. (Note that the (220) peak corresponds to

(110) planes in XRD of face-centered cubic materials.) The orientation preference, P,

was calculated for the (220) peak to the (111) and the (220) to the (311), where the factor

is given as

$$P_{220/111} = \frac{I_{220}}{I_{111}} * \frac{100}{57} * \frac{L_{111}}{L_{220}}$$ (3.2)

for the preference of the (220) peak to the (111) peak, and as

$$P_{220/311} = \frac{I_{220}}{I_{311}} * \frac{39}{57} * \frac{L_{311}}{L_{220}}$$ (3.3)

where the L_{hkl} are the lengths of the incident x-ray beam on the sample, as given by

$$L_{hkl} = \frac{2R \tan \dfrac{\delta}{2}}{\sin \theta} \qquad (3.4)$$

where R is the length of the detector (185 mm in our case), θ is the incident angle

between the x-ray source and the sample plane of interest $(= \frac{1}{2} * 2\theta)$, and δ is the

divergence slit angle ($0.5°$ in our setup). A value of $P = 1$ means there is no preference

between the two orientations under study.

The results of the $P_{220/111}$ and $P_{220/311}$ versus film thickness are plotted in Figure

3.7 and an exponential curve is found to best fit the data in each case. The curve can be

used to extrapolate the preference factor for a film of zero thickness, giving the expected

nucleation preference. We find that, for $P_{220/111}$, the curve's equation is given by

$P_{220/111} = 1.62e^{0.0015t}$, where t is the film thickness, and we find that the best fit for $P_{220/311}$

$= 2.45e^{0.0013t}$. Thus, for zero thickness, the preference factors are

$P_{220/111, t=0} = 1.62$ and $P_{220/311, t=0} = 2.45$. It should be noted that these preferences are

relatively miniscule compared to the preferences seen for thicker films. It is thus evident

that film growth, not nucleation, is the principal driver of texture development, as

expected.

(a)

(b)
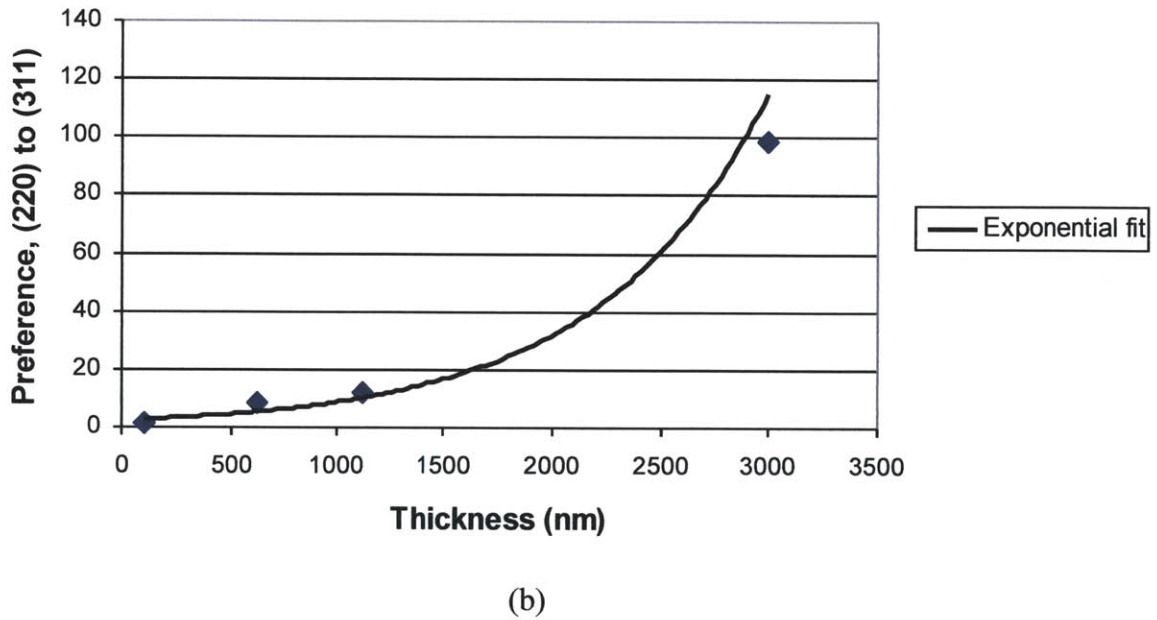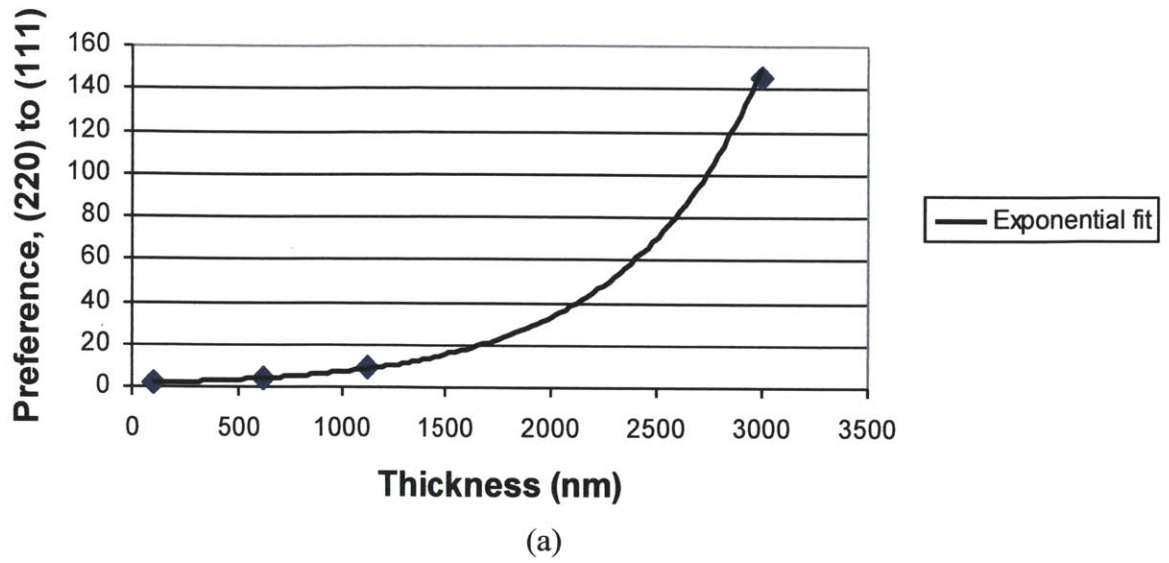
Figure 3.7. Orientation preference versus blanket film thickness for (a) (220) to (111), and (b) (220) to (311).

3.2.2 Temperature effects

The imposed thermal budget ceiling for this work was 450° C, in order to maintain compatibility with BEOL CMOS processing. As it is the case that atomic surface mobilities increase with increasing temperature, it was assumed that the highest temperature possible (i.e. 450° C) should always be used for Ge deposition in order to

obtain the largest grains. However, as this is the first work (to our knowledge) to investigate Ge deposited by UHVCVD on a-Si, we felt it prudent to explore the temperature space of the deposition in order to better understand the effects of temperature on the resulting film.

First, growths at temperatures lower than 450° C were attempted. A growth at 300° C for 4 hours produced no growth detectable by SEM or XRD. We can thus conclude that, for our system, GeH_4 does not decompose on the substrate surface and/or nuclei of critical size are not able to form at 300° C. Previous work [68] used 360° C as the buffer layer growth temperature for epi-Ge on Si, so a poly-Ge growth at 350° C for 8 hours was attempted. This temperature did lead to deposition of a poly-Ge film, and XRD confirmed that the film was polycrystalline (not amorphous). This demonstrates that the temperature for GeH_4 decomposition on a-Si in UHVCVD is between 300° C and 350° C and, at 350° C, Ge adatoms on the a-Si surface have sufficient surface mobility to form polycrystals.

Next, blanket poly-Ge growths on a-Si were performed at 450° C and 550° C for 8 hours each. While the maximum processing temperature allowed in this thesis is 450° C, some applications (such as the deposition of thin film transistors on low-cost glass) can endure processing temperatures up to 550° C. Thus, a growth at 550° C may have applications in areas outside microphotonics, in addition to illuminating the effects of temperature on the films' properties.

Results from these growths and the growth at 350° C are shown in Table 3.1, which gives the films' thicknesses, carrier concentrations from Hall effect measurements, and preference of the (220) to the (111) peak as given by XRD. The preference from the

XRD powder diffraction file is also shown, as this value represents a completely random texture. We examine the preference of (220) to (111) peak as a proxy for the texture; the preference of the (220) to the (311) follows the same trend. As can be seen in the table, the films deposited at 350° C and 450° C appear to follow the trend that would be expected – the film growth rate (thickness) increases with temperature, the carrier concentration decreases with temperature, and the (110) texture (given by the (220) peak) increases with temperature. These can be explained by noting that the deposition process is thermally activated; thus, the growth rate increases with an increase in temperature, the average grain size increases (so the carrier concentration due to grain boundaries decreases), and the texture also increases as the properly-oriented grains come to dominate the film with increasing thickness (cf. Figures 2.2, 2.3, and 2.4).

Table 3.1. Sample thicknesses, carrier concentrations, and XRD peak intensity ratios for three blanket poly-Ge samples deposited on a-Si for 8 hours at different temperatures. The XRD orientation preference from a Ge powder diffraction file is included for comparison.

Sample	Thickness (nm)	Carrier concentration (p, cm^{-3})	Preference of (220) to (111)
Deposited at 350° C	220	2.7×10^{18}	4.41
Deposited at 450° C	1150	9.3×10^{17}	6.22
Deposited at 550° C	770	7.4×10^{17}	2.14
Powder Diffraction File	N/A	N/A	1

However, the sample deposited at 550° C is an anomaly in this trend. Not only is the film thinner than the 450° C film, but it is also not as strongly textured as the other two films. In their work on the LPCVD deposition of poly-Si, Joubert et al. [69] found that their poly-Si film's as-deposited texture changed with deposition temperature and silane partial pressure. It is possible that the 550° C-grown film is in a state of transition

between (110) texture and another higher-temperature texture. As this transition would also mean a change of the film's a value, it is also very likely that this corresponds to a change in the growth rate, as observed in the case of simulations of polycrystalline diamond CVD [70] and demonstrated here by the 550° C-grown film's reduced thickness compared to that of the 450° C-grown film.

The sample deposited at 550° C does appear to have larger grains (fewer grain boundaries) than the other two samples, though, as given by its low p-type character. This would be expected for a film deposited at higher temperatures, as the greater adatom mobility would allow the film to form larger grains.

3.3   Doping of poly-Ge

In order to fabricate a p-i-n device, we must be able to dope the active material both p-type and n-type. In high-T-compatible processing, this can be done in one of two ways: in the first method, the active material may be co-deposited with the dopants by flowing both the active material's precursor as well as the dopant's precursor during the time of deposition (*in situ* doping). For epi-Ge, a typical chemistry would be GeH_4 + PH_3 (germane and phosphine) for n-type doping with phosphorus (P) and GeH_4 + B_2H_6 (germane and diborane) for p-type doping with boron (B). The other method of doping the active layer in high-T processing is to use ion implantation of the desired dopant with a subsequent anneal to activate the dopant (i.e. to break the electron or hole free from the dopant atom).

In the case of low-T poly-Ge deposition, however, the implant-and-anneal method is not viable due to the high-T nature of the process. It was unknown prior to this work whether it would be possible to dope poly-Ge *in situ* at 450° C and activate the dopant.

Two experiments were performed with PH_3 doping of poly-Ge on a-Si in 4-hour growths at 450° C. In the first experiment, PH_3 was flowed at 1 standard cubic centimeter per minute (sccm) flow rate, while GeH_4 was flowed at the typical value of 7.5 sccm. No resulting growth was observed, as the GeH_4 has to compete with phosphorus-containing species for a-Si surface adsorption sites. In the second experiment, PH_3 was flowed at 0.5 sccm while GeH_4 was flowed at 7.5 sccm. This produced a blanket film of 175 nm thickness and $2.6 \times 10^{18}/cm^3$ n-type doping. Due to complications with our B_2H_6 source gas, experiments with p-type doping could not be performed. However, we believe that the demonstrated successful n-type doping and activation should also be possible with p-type doping, as both dopants have similar activation requirements.

3.4   Lateral overgrowth

A wide body of work (for example, Ref. 67 and Refs. 71-73) has been amassed concerning the epitaxial lateral overgrowth (ELO) of semiconductor materials. In ELO, a material is selectively and epitaxially deposited on a substrate and is grown to such an extent that it grows over the barriers that define the growth region (e.g. SiO_2 barriers); see Figure 3.8 for a depiction of the process. In the case of epi-Ge growth from Si over SiO_2, in the overgrown region, threading dislocations from the Ge/Si interface are eliminated due to shadowing by the sidewalls at points sufficiently far over the SiO_2. This leads to a higher-quality film in the overgrown region and has been suggested as a route to fabricate high-performance devices as well as thin films on oxide.
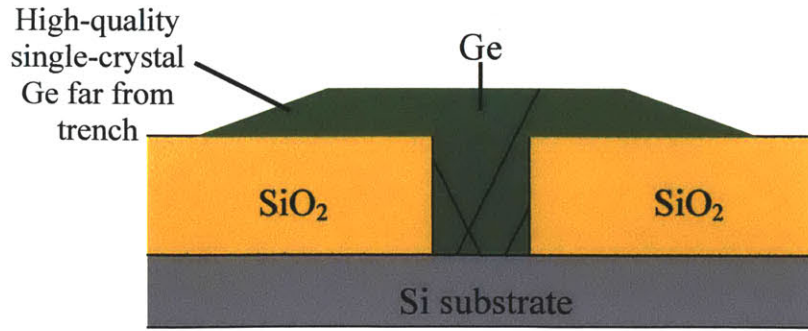
Figure 3.8. Schematic of the ELO process of Ge on Si. Lines within the Ge trench represent threading dislocations.

A similar concept may be applied in the case of selective growth of polycrystalline materials. However, in the case of poly materials, it is grain boundaries that extend from the film/substrate interface, not threading dislocations as in the case of ELO. As a poly film grows to a height greater than that of the barrier that defines the growth region, growth will continue vertically and will also proceed laterally, as depicted in Figure 3.9a. In Figure 3.9b is shown the plan view schematic of the LO (lateral overgrowth) phenomenon. As only the grains nearest the barrier serve as sites from which to grow laterally, the number of grains that can grow laterally is reduced from the total number of grains in the selectively-grown region. These grains may also grow unimpeded across the barrier, such that a relatively small number of grains can take up a large volume and thus reduce the grain boundary density from that of the as-deposited poly-Ge. This phenomenon of "turning a corner" eliminates defects that follow line-of-sight propagation, such as threading dislocations; in the case of poly-Ge LO, it eliminates many grain boundaries that propagate vertically from the poly-Ge/a-Si interface.
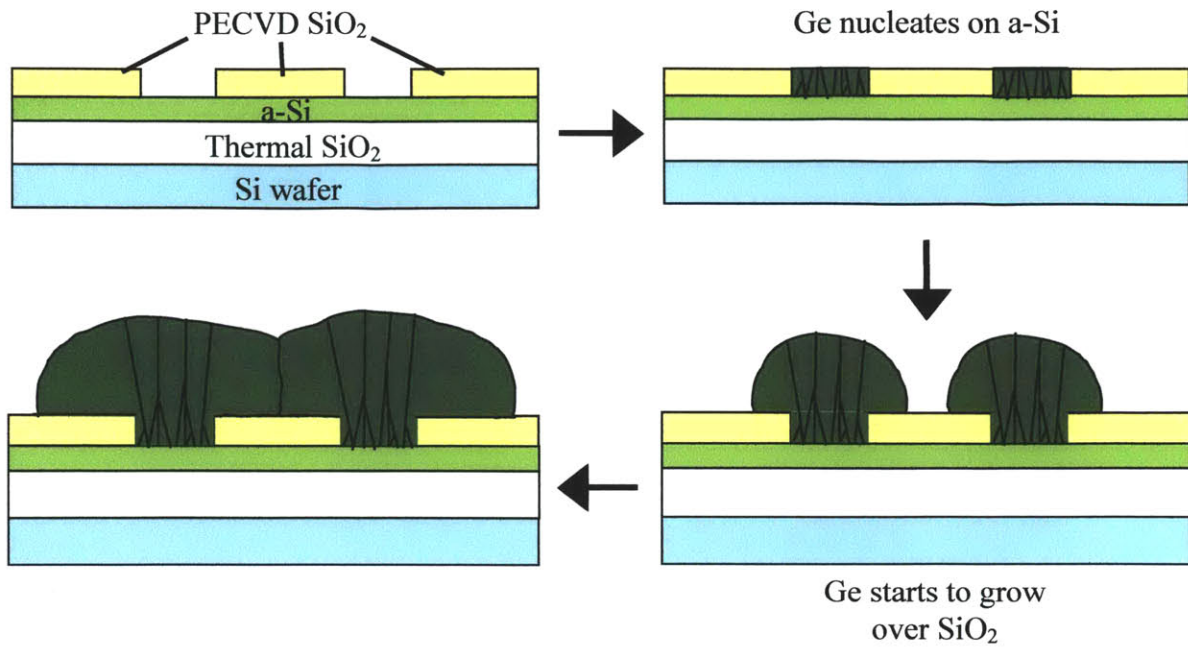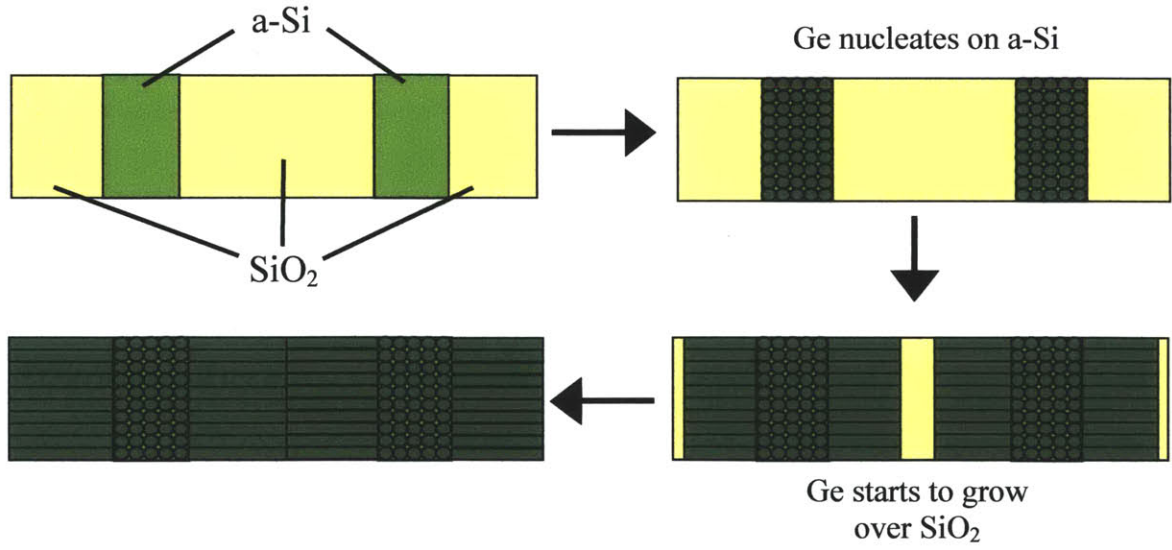
Figure 3.9. The poly-Ge LO process depicted schematically in (a) cross-section, and (b) plan view.

Figure 3.10 shows a cross-section SEM (XSEM) and a cross-section transmission electron microscope (XTEM) image of the poly-Ge LO. The XSEM image shows the poly-Ge LO from two adjacent regions of grain growth, where the growth fronts have

grown together in the LO region. In the XTEM image, striations that indicate defects are seen to decrease in density in the laterally-overgrown region.

While it does appear that poly-Ge LO alone enhances the grain size of poly-Ge as expected, this enhancement can only go so far: there are still numerous grains in the LO region. In Figure 3.10, although the grain sizes are enhanced in the plane of the images, it is not expected that poly-Ge LO gives any grain size enhancement in the direction perpendicular to the plane of the images over that seen in as-deposited film growth.

The lateral overgrowth of poly-Ge over oxide barriers represents our initial foray into the enhancement of poly-Ge grain sizes at low temperatures using selective deposition by UHVCVD. A further application of this process will be detailed in Chapter 5.

3.5   Chapter summary

This chapter presented the method of poly-Ge deposition on a-Si in our UHVCVD reactor. A dip in HF solution after the RCA clean's SC2 bath was required for high-quality poly-Ge film growth, and the a-Si layer thickness has to be limited to a maximum of 120 nm in order to avoid film bubbling due to H outgassing. Characterization of poly-Ge films deposited at 350° C, 450° C, and 550° C showed (110) texture in all films, with the strongest such texture at 450° C. We gave results from the successful *in situ* n-type doping of poly-Ge with phosphorus, and showed that the growth of poly-Ge over oxide barriers enhances the material's grain size.
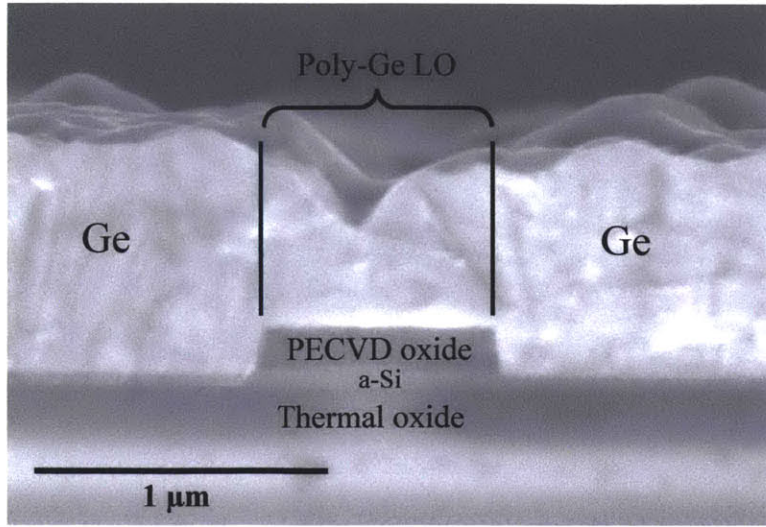
(a)
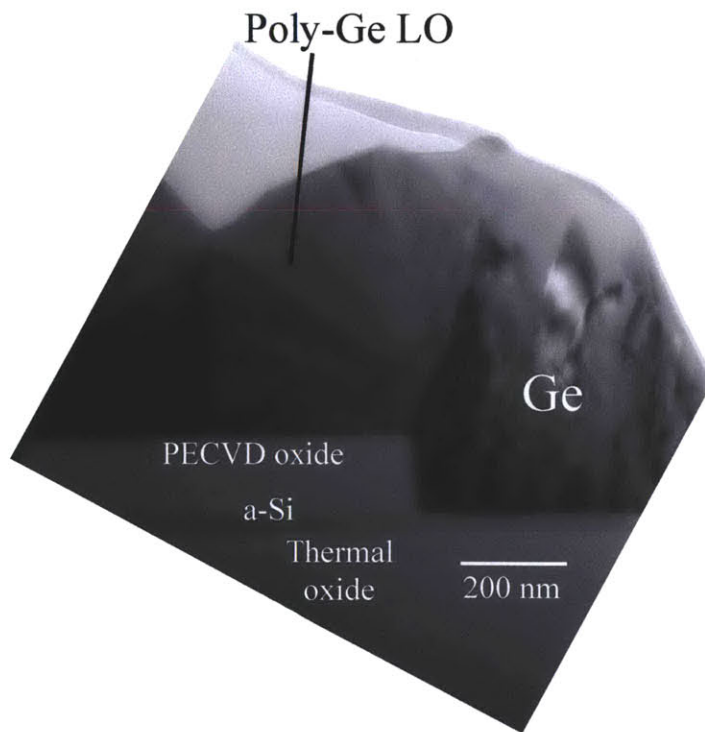
(b)

Figure 3.10. Micrographs of the LO region in poly-Ge on a-Si, from (a) XSEM and (b) XTEM.

Chapter 4: Geometrically-confined lateral growth of germanium on amorphous silicon: one-dimensional confinement

4.1 Background and motivation

The main thrust of this thesis is to demonstrate grain size enhancement, and thus a decrease in the grain boundary density, in poly-Ge using temperatures that do not exceed 450° C. As was elucidated in Chapter 2, several attempts have been made to achieve this result, but none have been truly satisfactory in producing large-grained Ge on reasonable timescales using CMOS-compatible processing. It is from this starting point that we introduce our novel method for low-T Ge grain size engineering.

Inspiration for this method was partly drawn from previous work (see Ref. 67), which has investigated the effect of high-aspect-ratio structures on semiconductor growth in a phenomenon called epitaxial necking. In epitaxial necking, a threading dislocation generated at the heteroepitaxial Ge/Si interface propagates in a non-vertical direction to the surface of the wafer (45° to the surface in the case of a (100) Si substrate); if the Ge is confined in trenches with wall heights greater than the trench widths, the threading dislocations terminate at the Ge/sidewall interface and the Ge continues to grow vertically without any threading dislocations. In our system, the Ge growth is not epitaxial so there are not lattice mismatch-induced dislocations to concern us, but there are instead grain boundaries that nucleate at the Ge/Si interface and propagate to the Ge surface. However, these grain boundaries, like the threading dislocations in epi-Ge growth, also do not propagate perfectly normal to the plane of the interface. Thus, we can also use high-aspect-ratio structures to terminate grain boundaries at sidewalls and grow reduced-defect-density material after this termination.

This process of using necking to reduce defect density is not, in general, novel. The process is used in the Czochralski crystal growth method, in which the growing crystal is seeded and then necked to eliminate dislocations [74]. A structure called a "pigtail" is used in the fabrication of single-crystal turbine blades; the pigtail selects single, consistently-oriented grains for extended solidification [75]. A team from MIT in the 1980s also did experiments in which they used zone melting to solidify silicon through a series of SiO_2 barriers that selected certain grains for further growth, resulting in a narrow, predetermined distribution of in-plane grain orientations [76].

Thus, we started our series of experiments with the belief that, if we could selectively grow poly-Ge on a-Si in a high-aspect-ratio structure as shown in Figure 4.1, we could eventually select certain grains for extended growth and thus increase the average overall grain size of our material. In the example shown in Figure 4.1, two Ge grains nucleate at the a-Si layer, and one (on the right) grows faster than the other, due to grain growth velocity anisotropy (see Chapter 2) and eventually fills the entire channel. This grain serves as the seed for further large-grained or single-crystalline growth outside the channel.
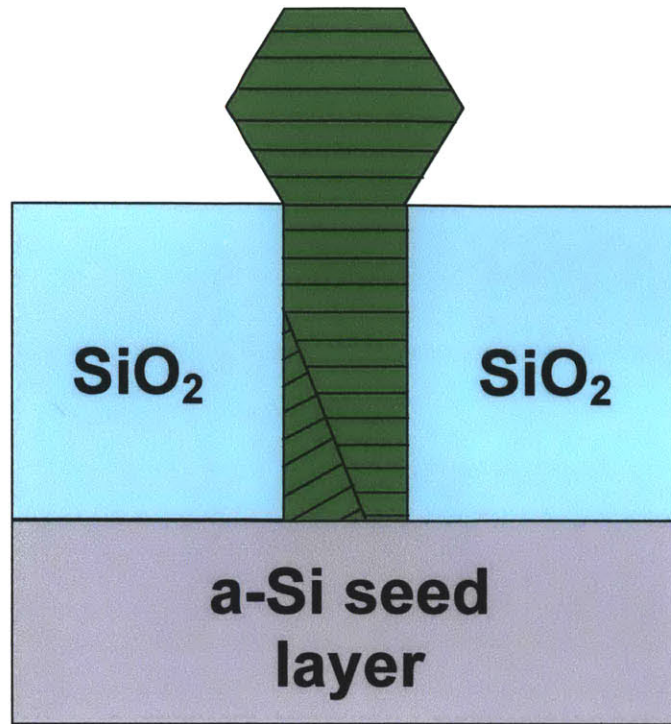
Figure 4.1. Schematic of the envisioned effect of geometric confinement on poly-Ge growth from an a-Si seed; the Ge is confined by the SiO_2 walls on either side.

4.2   Fabrication challenges and approaches

We will now consider the application of this idea of necking, or "geometric confinement," to micron-sized features of poly-Ge on a-Si, suiting our application.

The fabrication of a structure such as that shown in Figure 4.1 is difficult to perform using standard planar photolithographic processes. To obtain high-aspect-ratio structures, special lithographic techniques are needed, as the high aspect ratios cause numerous problems with conventional lithography. In work on epitaxial necking, interference lithography was employed in order to pattern high-aspect-ratio structures. Interference lithography, however, is not a common lithographic process, and is limited to producing arrays of features. It is our desire to fabricate high-aspect-ratio structures using common lithographic processes that are not limited to producing any certain subset of feature types (such as only arrays of features).

The concept enabling our work is the fabrication of a high-aspect-ratio structure using the vertical dimension of thin films deposited by planar processing to define the structure's thinnest dimension. This stands in contrast to the use of lithography to define the thinnest dimension, as is traditionally done. Films can be fabricated with thicknesses on the order of a few tens of nanometers, so we are able to obtain one very small dimension that is not defined lithographically. It follows that the high-aspect-ratio structure should have its long dimension(s) oriented laterally in the plane of the wafer, using the thickness of a deposited layer as the smallest dimension in the high-aspect-ratio structure.

Using processing to be described, we can fabricate a structure as depicted in Figure 4.2(a), where the thickness of the a-Si layer defines the smallest dimension of the confinement structure. This is a one-dimensional (1D) confinement structure, as it is a structure that provides confinement in the vertical dimension, with the confinement aspect ratio defined as d/h (length of the confining region divided by its height). Using SiO_2 as the confining layers below and on top of the a-Si allows for the selective deposition of poly-Ge on the sides of the a-Si and subsequent lateral growth between the confining SiO_2 layers, as shown in Figure 4.2(b). We call this type of growth geometrically-confined lateral growth (GCLG), and this specific 1D-confined growth is 1D GCLG.
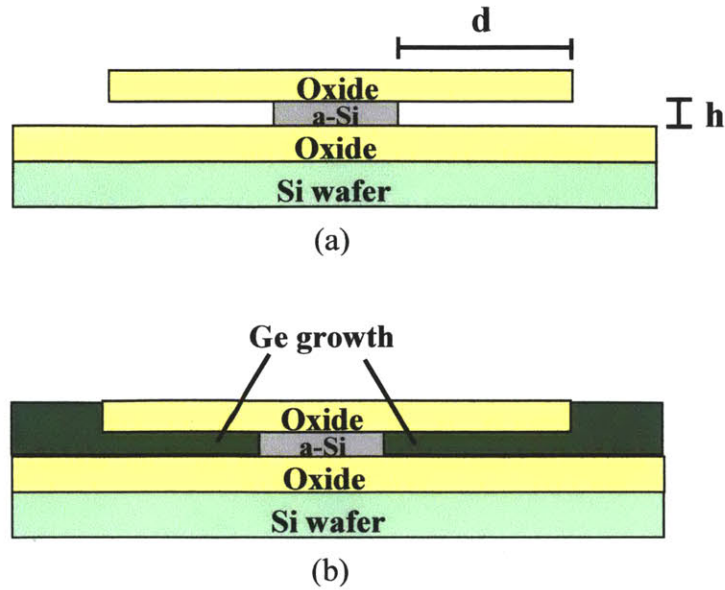
Figure 4.2. (a) Cross-section schematic (not to scale) of the high-aspect-ratio structure, with 1D confinement in the vertical dimension. The value h is the channel height and d is its length. (b) Cross-section schematic (not to scale) of poly-Ge deposition on the sides of the a-Si and subsequent growth between the confining SiO_2 layers.

Performing 1D GCLG for our experiments was fairly straightforward, and the process flow is illustrated in Figure 4.3. First, a layer of SiO_2 (in the case of our experiments, we used thermal SiO_2 for simplicity) was deposited on a 6" Si wafer (the doping and orientation of the wafer is not important, as the wafer does not interact with the growth). Next, a layer of a-Si was deposited by plasma-enhanced CVD (PECVD) at 350° C, followed by deposition of a layer of SiO_2 at 400° C by PECVD. The wafer was coated with photoresist and patterned with rectangles; the top oxide and the underlying a-Si were then etched in a reactive ion etch (RIE) down to the bottom layer of SiO_2. Next, the wafers were immersed in a bath of 20% tetramethylammonium hydroxide (TMAH) in deionized (DI) water at 80° C for varying amounts of time, on the order of a few minutes. TMAH etches Si preferentially to SiO_2 and thus etched the a-Si between the two SiO_2 layers. The wafers were then cleaned in a double piranha clean (3:1 H_2SO_4:H_2O_2) with a hydrofluoric acid (50:1 DI:acid) dip step in between the piranha cleans, and further

65

cleaned in an RCA clean plus post-clean HF dip to passivate the Si surface. The wafers were then loaded into our hot-walled UHVCVD reactor idling at 450° C and $<1 \times 10^{-9}$ Torr and allowed to anneal for approximately 1-2 hours to allow the PECVD-deposited layers to degas H. Ge was then grown on the structure by flowing 7.5 sccm GeH_4 in the UHVCVD reactor at 450° C.

XSEM images of the pre-growth and post-growth 1D GCLG structures are shown in Figure 4.4(a) and (b), respectively. Upon examination of Figure 4.4(b), it is clear that the PECVD SiO_2 layer has been severely etched, as evidenced by the curved nature of the layer near the a-Si and the fact that the confinement region – hereafter called the "channel" – is much wider in Figure 4.4(b) than in 4.4(a), where Figure 4.4(a) was taken immediately after the TMAH etch of the a-Si layer. It was believed that the SiO_2 was being etched by the two wet chemical cleans, or by the Ge growth process itself. As previous growths with other structures had not shown significant SiO_2 etching during the Ge deposition process, it seemed the SiO_2 etching was likely due to the wet chemical cleans.

Cross-section   **Plan view**

Start with Si wafer
substrate

Growth thermal
SiO$_2$

Deposit a-Si
seed layer

Deposit PECVD
SiO$_2$

Pattern PECVD
SiO$_2$ using dry etch

Pattern a-Si layer in
same pattern as
PECVD SiO$_2$ layer

Undercut etch a-Si
layer using TMAH

Deposit Ge by
UHVCVD
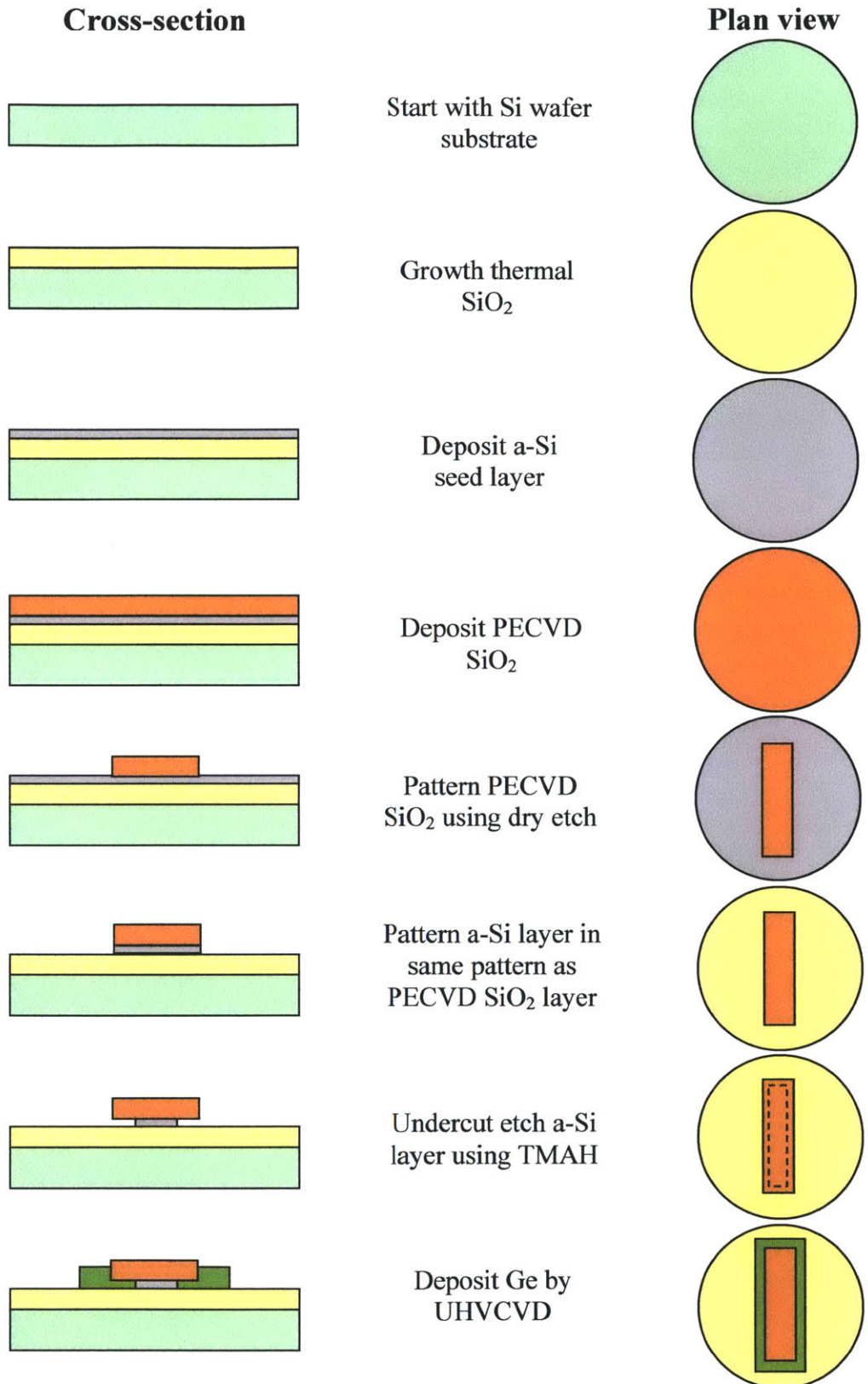
Figure 4.3. The process flow for the fabrication of geometrically-confined lateral growth structures with 1D confinement (not to scale).

PECVD SiO$_2$

a-Si

Thermal SiO$_2$

200 nm

(a)

Ge growths

PECVD SiO$_2$
a-Si

Thermal SiO$_2$

200 nm

(b)
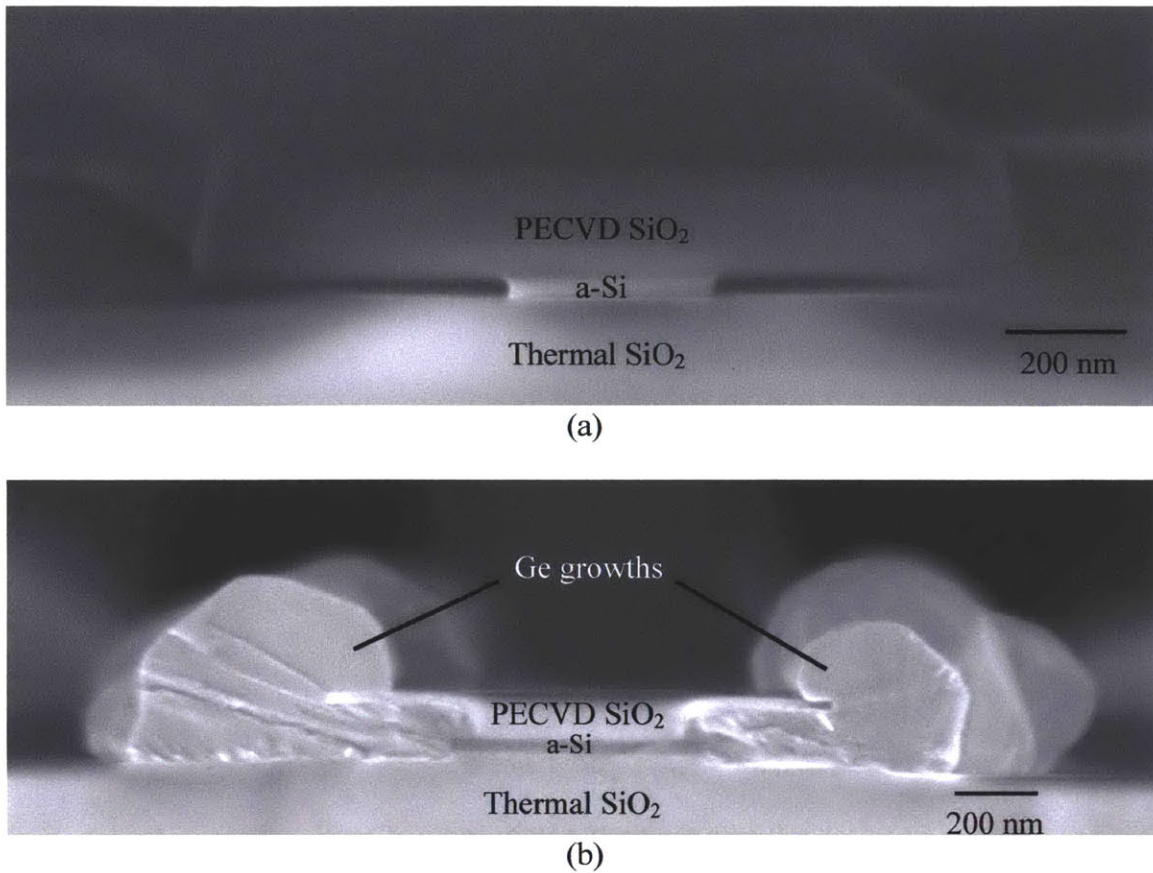
Figure 4.4. (a) XSEM image of the 1D GCLG growth structure before Ge deposition, and (b) after Ge deposition.

We reduced the HF dip times during all parts of the wet chemical cleans in an attempt to alleviate the SiO$_2$ etching issue. However, the HF dip after the RCA SC2 clean is known to be a crucial step, as explained in Chapter 3, as it prevents the formation of native oxide on the Si prior to Ge deposition. For this reason, we examined the effect of the post-SC2 HF dip time on the quality of the poly-Ge growth on a-Si, and the results have been shown in Figure 3.5(a)-(e). Based on these results, we were able to reduce the post-SC2 HF dip from the previously-used 30 seconds to 5 seconds. Additionally, the HF dip time between the piranha cleans was reduced from 15 seconds to 3 seconds, and the HF dip time between the SC1 and SC2 cleans in the RCA clean was reduced from 60

seconds to 10 seconds. This total HF dip time reduction of nearly 90 seconds (a reduction of more than 80% from the original total 105 seconds of HF dip time) resulted in the PECVD SiO$_2$ only being etched approximately 35 nm in our samples, as shown in the XSEM micrograph of Figure 4.5, as compared to the roughly 160 nm that was etched using the original HF dip durations.
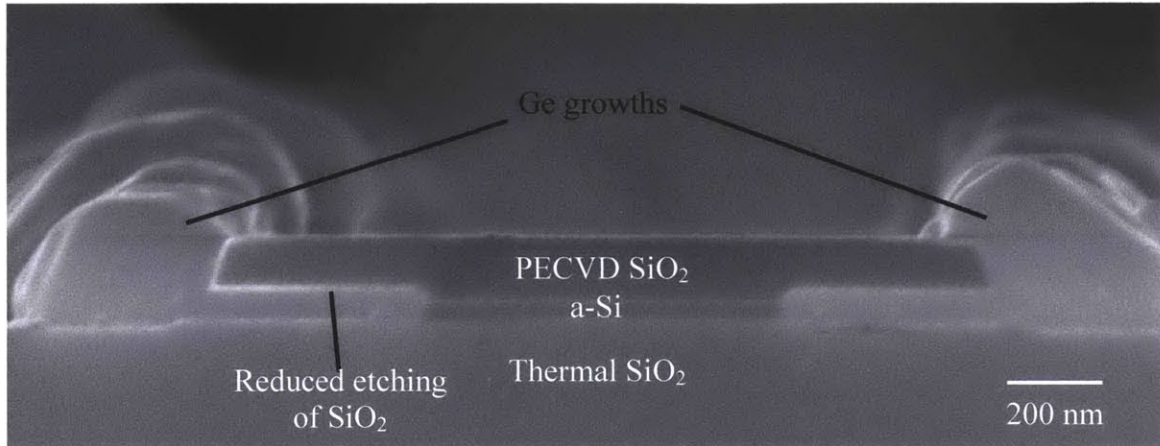
Figure 4.5. XSEM image of the 1D GCLG structure after Ge growth; this structure has undergone pre-growth wet chemical cleans with the total HF dip time reduced by approximately 90 seconds (85%) from the standard HF dip time.

The use of silicon nitride, Si$_3$N$_4$, deposited by PECVD as the top confining layer (instead of SiO$_2$) was also attempted in order to reduce the wet chemical cleans' etching effect on this layer. However, the Ge did not deposit selectively to the Si$_3$N$_4$, and the Si$_3$N$_4$ delaminated from the a-Si in some cases. Since it was demonstrated that we could successfully mitigate the SiO$_2$ top confinement layer's etching issues, and since the Ge deposition is very selective to SiO$_2$, we chose SiO$_2$ as our confining material and further work with Si$_3$N$_4$ was not explored.

The rate at which 20% TMAH at 80° C etches a-Si in confinement was unknown before our experiments. Using XSEM micrographs to observe the etch distance for various etch times with various channel heights (i.e. the vertical channel dimension), we

calculated that the etch rate was approximately 2-5 nm/sec. A large amount of variance in this rate was even observed among locations on the same wafer, as can be seen in Figure 4.6. The exact cause of this variation is unclear, but we can rule out some possibilities. The TMAH bath was immersed in a heated water bath for at least 20 minutes before performing the etch, so thermal variations should be minimal. The channels were of the same dimensions, so mass transport variations can be ruled out. However, the RIE of the top SiO_2 is known to leave a fluoropolymer residue on Si, as discussed in Chapter 3, when the SiO_2 is overetched. During our fabrication process, the top SiO_2 was indeed overetched in the RIE in order to ensure that the a-Si layer was reached, as the SiO_2 etch and a-Si etch were done sequentially in the same RIE machine. Thus, it is possible that local variations in fluoropolymer formation on the a-Si from the SiO_2 dry etch influenced the TMAH's ability to etch the a-Si. It is also possible that local variations during the a-Si dry etch could cause these results, though this has not been explored.
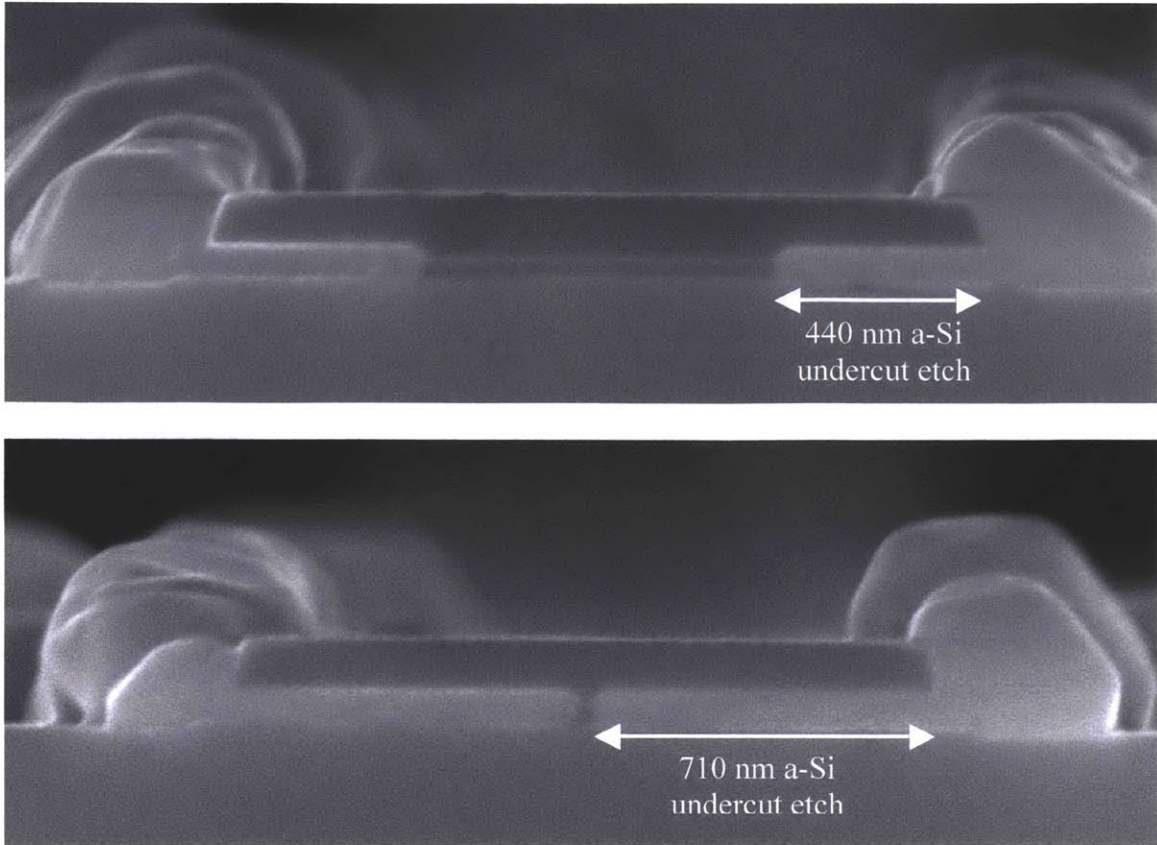
Figure 4.6. XSEM micrographs of two identical structures on the same wafer, subjected to the same TMAH etch, with differing a-Si undercut etch distances.

Additional work further verified that the top SiO_2 etch could be causing issues with the a-Si wet etch. In a deviation from the process flow, the a-Si dry etch step was skipped and the a-Si was etched purely by TMAH; as the thickness of the a-Si layer was small compared to the undercut etch distance, it was believed the TMAH should remove all a-Si in the open SiO_2 window. However, as can be observed in Figure 4.7, it appears that some a-Si remained in the window. The TMAH has etched the channel a-Si to the same extent that it has etched the residual a-Si in the open window; this would make sense if the TMAH is able to access the a-Si only at the a-Si/PECVD SiO_2 interface. This could result if the a-Si is completely covered by a fluoropolymer, such that the TMAH is only able to access the a-Si by penetrating at the SiO_2/a-Si interface where there may be

some voids, and proceeds to etch the a-Si under the fluoropolymer such that the fluoropolymer is effectively lifted off as the etch proceeds.
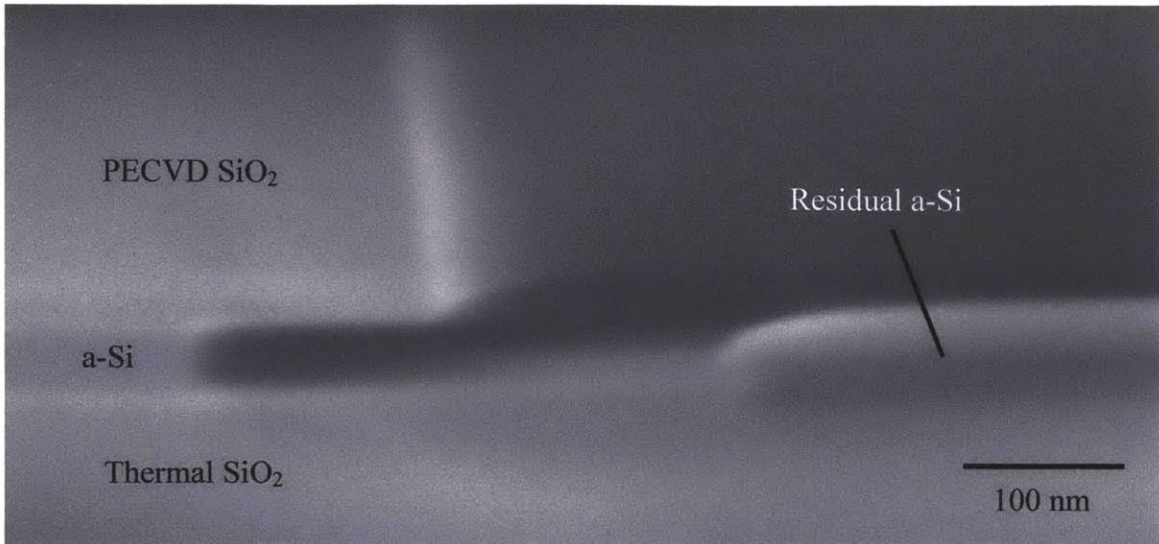
Figure 4.7. XSEM micrograph showing the 1D GCLG structure fabricated using a wet (TMAH) etch of the a-Si in the open window in place of the dry a-Si etch. a-Si appears to remain in the center of the window.

A final consideration is that of H outgassing from the PECVD-deposited materials after being loaded in the UHVCVD reactor, idling at 450° C, as discussed in Chapter 3. It was observed early in our experiments that the PECVD-deposited films could bubble and crack due to H outgassing. Our initial work used a-Si and SiO_2 films that were each 500 nm thick, and these films readily disintegrated in our UHVCVD reactor. The film thicknesses were subsequently reduced to a range of 40-150 nm for a-Si and 200-300 nm for SiO_2. We observed little effect of the oxide thickness on the post-UHVCVD film quality, but noted that, for a-Si thicknesses greater than approximately 120 nm, large bubbles were readily visible in the deposited films (Figure 3.6); this is due to the fact that the thicker a-Si layer contains a higher absolute amount of H than a thin layer, and this causes the encapsulating SiO_2 film to bubble when the H degasses from the a-Si film. Thus, we limited our a-Si film thicknesses to 120 nm at most.

After the wafers were loaded into the UHVCVD reactor, the H outgassing was monitored using a residual gas analyzer (RGA) attached to the vacuum chamber. The wafers were allowed to degas at 450° C until the H pressure as measured by the RGA had settled to a constant value. The RGA was then turned off and the growth was started.

4.3   Results and discussion

Figure 4.4(b) showed that the Ge growth from the a-Si in the 1D GCLG structure proceeds as expected, but the primary question regarding this and other 1D-confined growths is how a confined growth is different from an as-grown (unconfined) poly-Ge film. This section will show results from many growths and discuss the differences between those results and the results from as-deposited poly-Ge films.

4.3.1   Microscopy and diffraction results and discussion

Figure 4.8(a) and (b) show plan-view SEM (PVSEM) images of growths from two 1D GCLG structures. The Ge in Figure 4.8(a) has been grown from a channel with an aspect ratio of 0.25 (weak confinement); that in Figure 4.8(b) has been grown from a channel with an aspect ratio of 3.0 (stronger confinement). It is readily apparent that the surface morphologies of the two growths are very different, with the sample in Figure 4.8(b) showing obvious faceting, while little is observed in the sample in Figure 4.8(a).
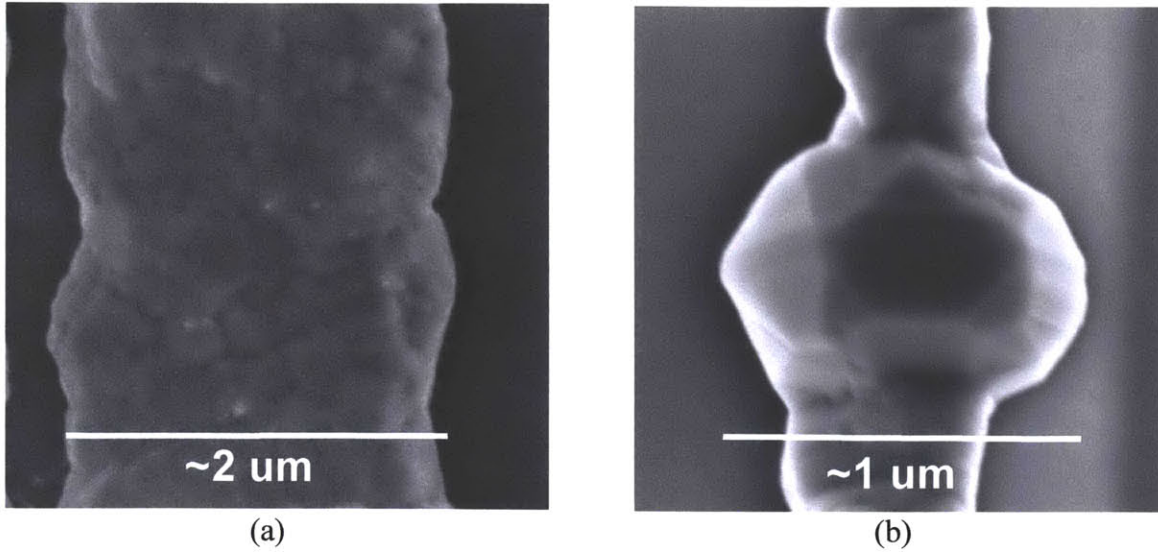
Figure 4.8. Ge growth from 1D confinement structures with aspect ratios of (a) 0.25, and (b) 3.0.

In order to explain the results shown in Figure 4.8(a) and (b), Figure 4.9(a) depicts what is seen at the microscopic level when a poly-Ge film grows from an a-Si seed. As discussed in Chapter 2, some grains, due to their crystallographic orientation with respect to the substrate surface, grow more quickly in the substrate normal direction than do others. Such a fast-growing grain is depicted in Figure 4.9(a), where a schematic snapshot of the a-Si seed and the Ge growing from it are shown (the growth front of the Ge is not shown, for ease of instruction). In Figure 4.9(b), the poly-Ge growth is put into perspective in a 1D GCLG structure to illustrate how the growth proceeds in this structure (with the growth outside the channel removed for ease of viewing). The large grain is the fastest-growing grain among all of those in the figure, and because it is the fastest-growing, it overcomes the other grains nearby and dominates the growth locally. Also, since it is the fastest-growing grain, it will emerge from the channel before any other grains and will grow to be the largest grain for a given amount of growth time. The other grains will emerge from the channel after the fast-growth grain and will not grow to

as large an extent as this grain. The fast-growing grain will also show faceting as it minimizes its surface free energy, as discussed in Chapter 2. This reasoning explains both of the phenomena – the selected, fast-growing grain being largest as well as being faceted – that appear in Figure 4.8(b). In the case of the Ge in Figure 4.8(a), the confinement was not enough (i.e. the aspect ratio was not sufficiently high) to select a fast-growing grain within the distance of the confinement (the channel length). Thus, no certain grains were locally selected, and the growth's surface morphology did not show any dominating grain growths or strong faceting.

To confirm that the channel is indeed selecting certain grains for extended growth, selected area diffraction (SAD) in a transmission electron microscope (TEM) was performed on a 1D GCLG sample, the results of which are shown in Figure 4.10. As the growth proceeds from the a-Si on the right to the open end of the channel on the left, the SAD images show that the material becomes more single-crystalline as the poly-crystalline rings transform into well-defined dots. Moiré patterns observed near the a-Si also indicate defects such as stacking faults and low-angle boundaries, but these did not propagate out of the channel.

This grain is growing fastest

a-Si seed

(a)

Oxide overlay

a-Si seed

This grain is growing fastest

Thermal oxide pseudosubstrate

(b)
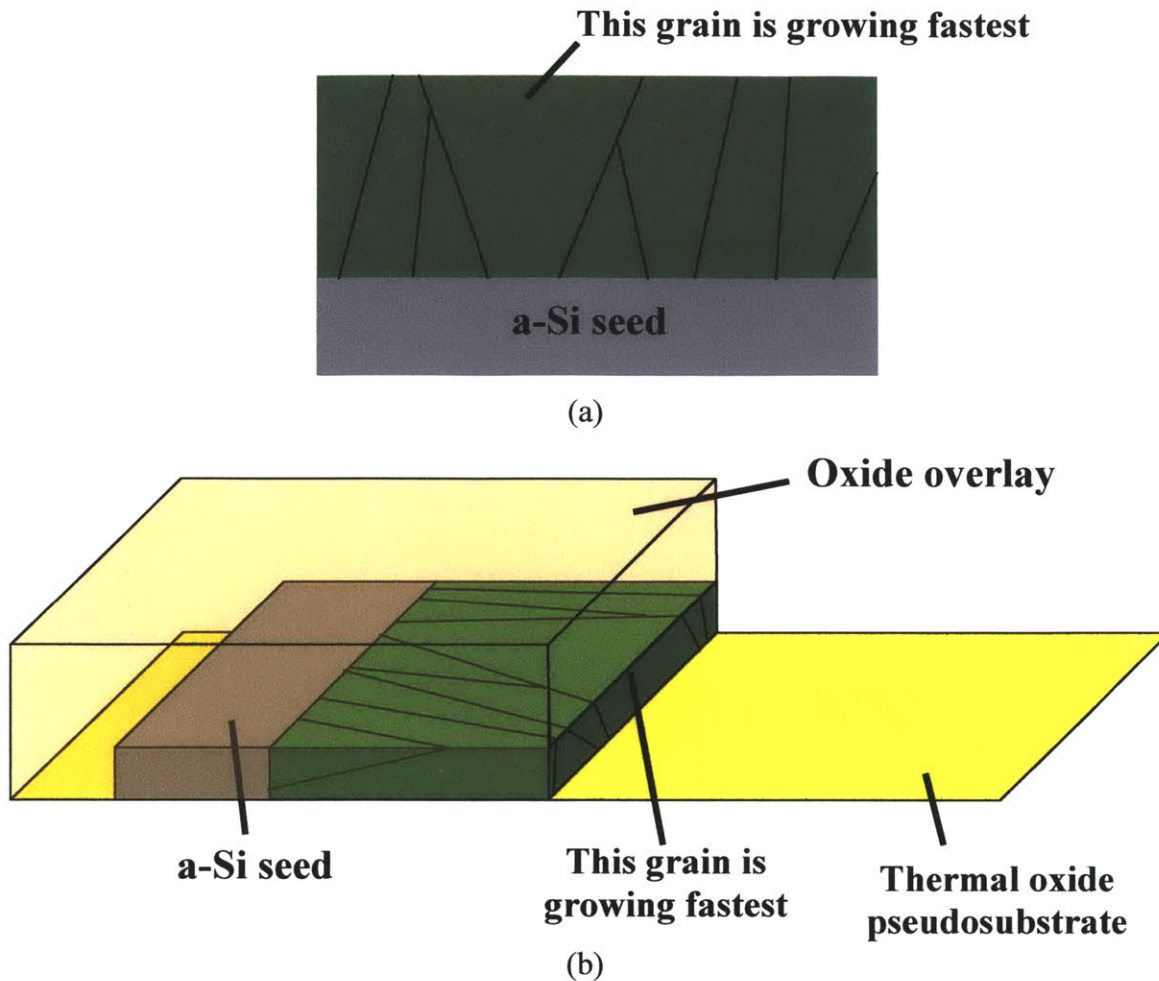
Figure 4.9. Schematic of the 1D GCLG Ge grain growth from an a-Si seed layer (a) in plan view (without showing any of the confining SiO_2), and (b) in perspective, showing the SiO_2/Ge/SiO_2 structure. In both cases, the schematic has been truncated so it does not show the growth outside the channel, in order to ease viewing.

As was discussed in Chapter 3, poly-Ge films deposited for sufficient times (several hours) at 450° C on a-Si in UHVCVD develop a strong (110) texture. In the case of the 1D GCLG samples, all growths were performed at 450° C, so a (110) texture in the direction of growth is expected. The grain orientation in the plane of the seed plane (the side of the a-Si layer) is, however, expected to be random or nearly random (as the oxide sidewalls may have a slight influence on the grain orientation). Figure 4.11 depicts this schematically.

X-ray diffraction (XRD) was performed on two similar 1D GCLG samples that had been grown for 16 hours. The partial (220) pole figures are shown in Figure 4.12. Figure 4.12a shows the pole figure for a sample in which the 1D GCLG top oxide "lines" (the long rectangles in Figure 4.3) run parallel to one of the <110> directions in the underlying silicon wafer, and we see the diffraction spots from the underlying silicon overlapping the pattern of the diffraction spots of the Ge film. Thus, it is difficult to determine if the symmetry seen in the diffraction is due to the Si or due to the Ge. However, in Figure 4.12b, the 1D GCLG oxide lines have been rotated with respect to the underlying silicon wafer by 45°, and we see that part of the diffraction pattern has also been rotated by 45°. This proves that the growth structure influences the crystallographic orientation of the 1D GCLG. As will be discussed in Chapter 5, channels with 2D confinement were shown to produce growths with (110) texture in the channel, so it is very likely the 1D GCLG films also generally have (110) textures in the channel and we are witnessing a rotation of these directions in the plane of the wafer between Figure 4.12a and 4.12b. Further x-ray and/or electron diffraction and analysis would be necessary to fully understand the effects of the 1D GCLG structure on the Ge orientation, but such inspection was not carried out in the current work as it is time-intensive and was not believed to be critical to the process; it could be pursued in the future if 1D GCLG material is deemed to be fit for use in device fabrication.
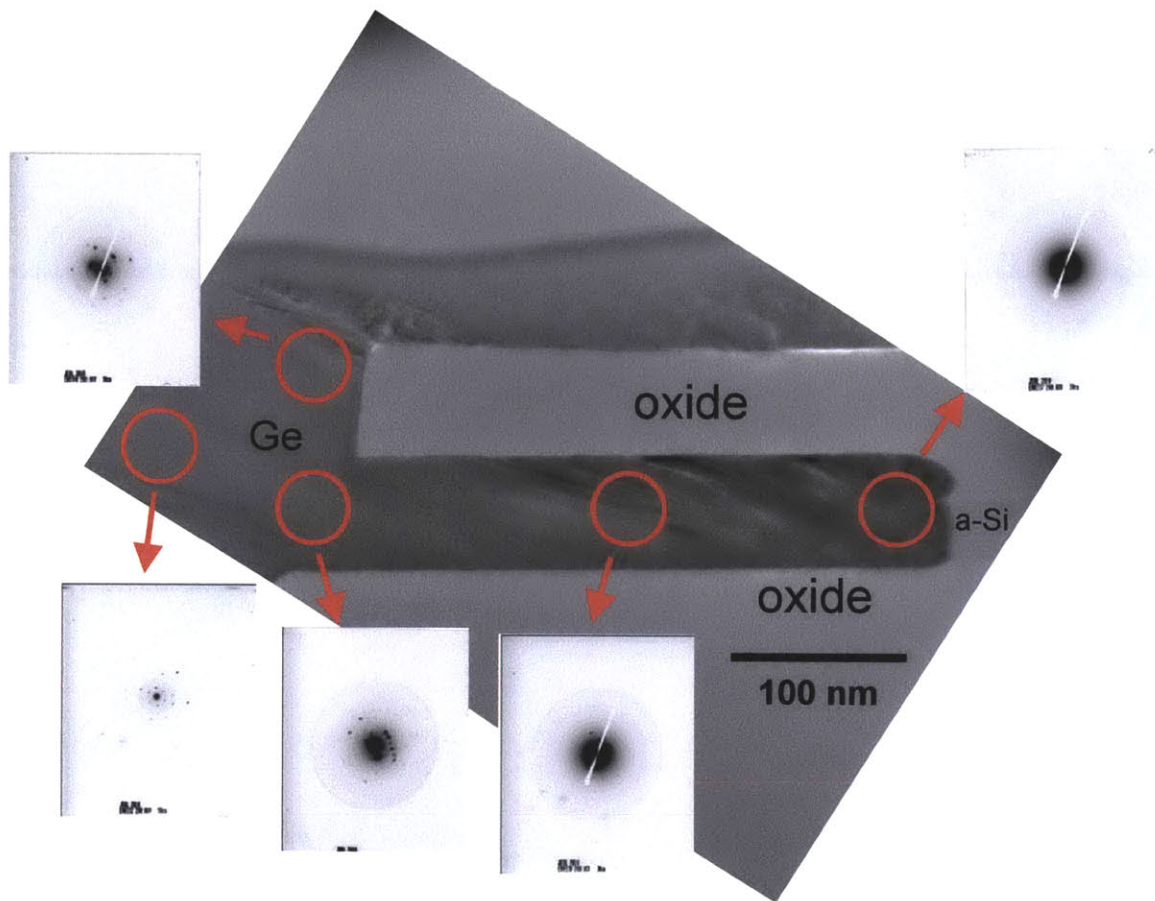
Figure 4.10. Cross-section TEM micrograph (200 kV, bright field) of a 1D GCLG channel with superposed SAD patterns, showing the transition from polycrystalline Ge near the a-Si seed to large-grained or single-crystalline Ge at the channel exit.
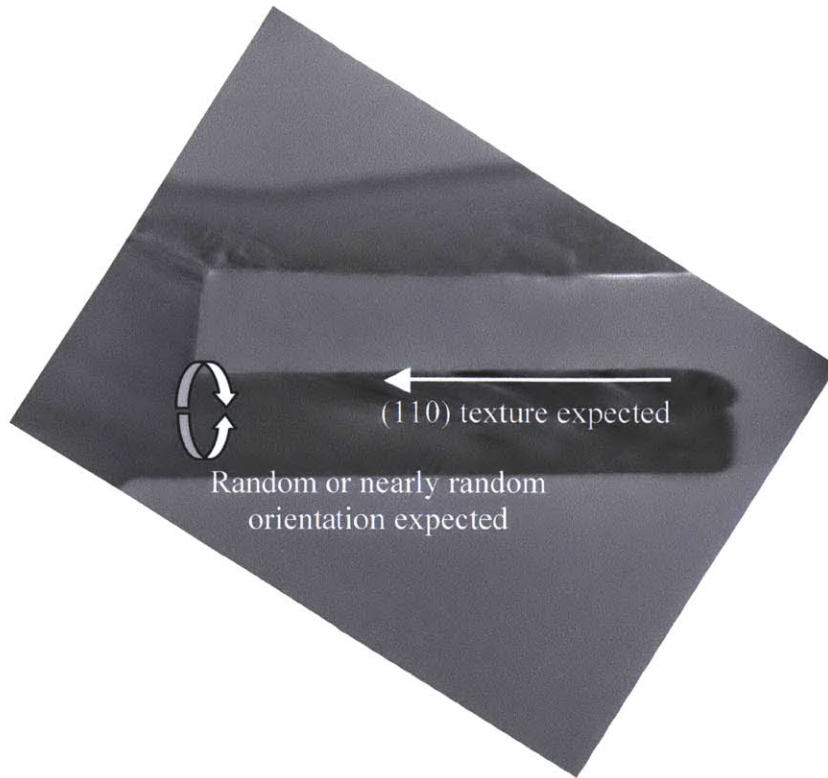
Figure 4.11. Illustration of the expected texture in the 1D GCLG channel: the in-channel direction should have (110) texture while the grain orientation in the plane of the nucleating a-Si plane should not show strong directionality.

(a)

(b)
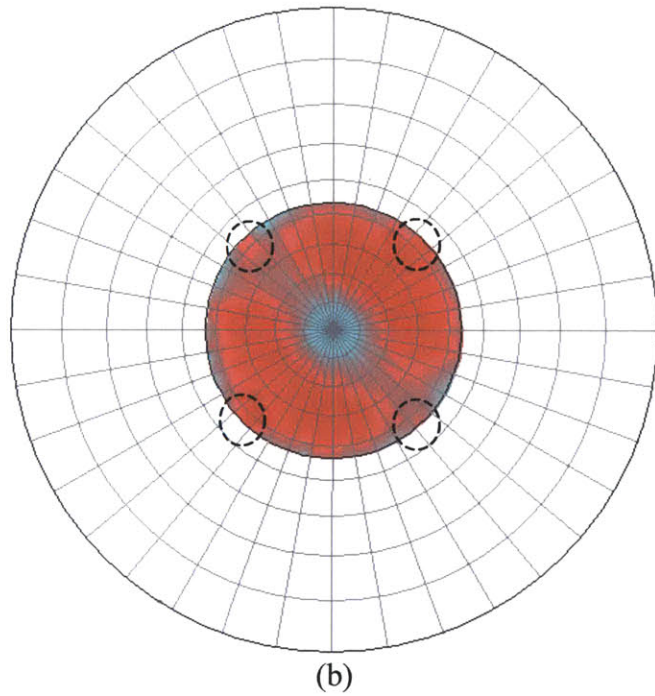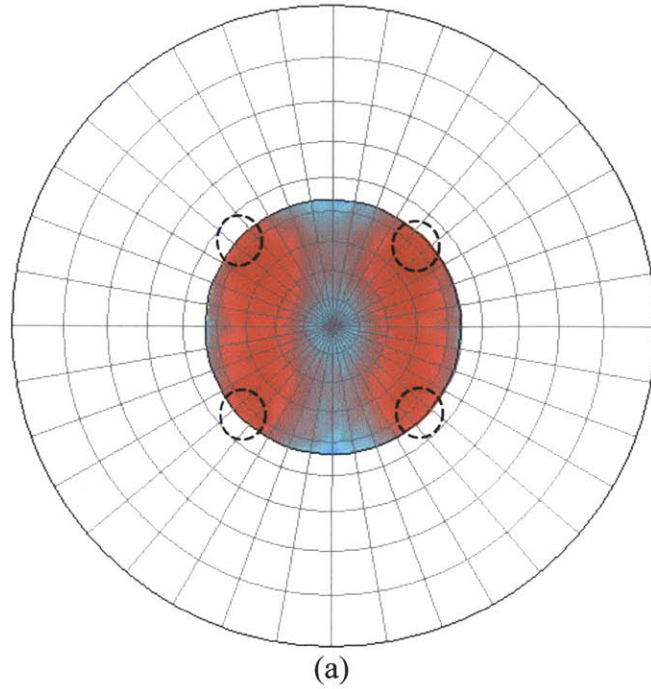
Figure 4.12. Partial (220) pole figures for 1D GCLG films, where redder hues indicate greater intensity. The Si peaks are encircled. The radial distance from the center corresponds to Ψ, the sample tilt angle. (a) A sample with the top oxide lines parallel to one of the underlying Si wafer's <110> directions, and (b) a sample with the top oxide lines at 45° to the Si <110>.

We performed cross-section TEM and electron backscatter diffraction (EBSD) studies to determine the grain sizes in the blanket (unconfined) films and the films grown from 1D confinement structures. TEM samples were prepared by focused ion beam milling and mounting on a copper grid. EBSD samples were polished using fine-grit paper and alumina particles in an ethylene glycol solution and band contrast was used to determine the grain sizes. TEM showed a blanket film grain size at 1 μm film thickness of approximately 170 nm, while EBSD showed a grain size of about 215 nm. TEM gave a 1D GCLG grain size at 1 μm film thickness around 520 nm, and EBSD showed a grain size of approximately 630 nm. It should be noted that EBSD likely overestimates the grain size, as the technique did not resolve small grains due to contrast issues, possibly due to surface roughness or instrumentation. Both methods, however, show that the 1D GCLG structure causes approximately a three-fold increase in the grain size for a 1 μm-thick film.

4.3.2 Electrical characterization results and discussion

The application of poly-Ge to use in active photonic devices will likely require the fabrication of a p-i-n structure, as discussed in Chapter 3. We have demonstrated our ability to dope poly-Ge n-type and predicted the ability to dope p-type as well, but the fabrication of an intrinsic layer is also necessary. We explore here our ability to deposit intrinsic germanium on a-Si.

The Hall effect measurement is a common method for determining the carrier concentration within a semiconductor material. As discussed in Chapter 2, undoped poly-Ge is found to be p-type due to defect states in the grain boundaries; the boundaries also decrease the carrier mobility due to scattering. However, the presence of grain boundaries

in the samples under test could potentially lead to erroneous Hall measurements, as the conduction may be preferential along the grain boundaries and thus not give the true character of the material's overall electrical properties. Previous work [77-79] has determined that a number of conduction regimes exist in polycrystalline materials, depending on the grain boundaries' trap densities relative to the doping density of the material. Still, all previous work has been on polycrystalline samples either grown in a blanket fashion or crystallized from amorphous material, and none has been performed on grains from a 1D confinement structure. For that reason, we are unable to assume that the regimes determined in previous work apply to our samples, as the boundaries in our 1D GCLG films may differ in character from those of the films used in previous work.

Thus, while we are unable to definitively say that Hall effect measurements are an accurate absolute measurement of the overall sample carrier concentration, we are confident that the measurement can provide comparative results among samples of similar grain boundary types. We assume that the grain boundaries between our blanket (unconfined) poly-Ge and 1D GCLG material are of sufficient similarity for comparison, and we proceed with Hall effect measurements on our samples as a relative indicator of material properties.

Performing a Hall effect measurement on a blanket sample of poly-Ge is a straightforward experiment. However, obtaining a film from a 1D GCLG sample is not as simple. In order to be able to perform a Hall effect measurement on a 1D GCLG film, a long (16-hour) Ge growth was executed using a 1D GCLG structure, such that the growth fronts coalesced and also grew over the top of the structure into a continuous film. A cross-section SEM image of such a growth is shown in Figure 4.13. The growth occurs in

the same manner as in the other samples (e.g. that shown in Figure 4.4b), but the growth time is extended (for example, the growth time for the sample in Figure 4.4b was 4 hours).
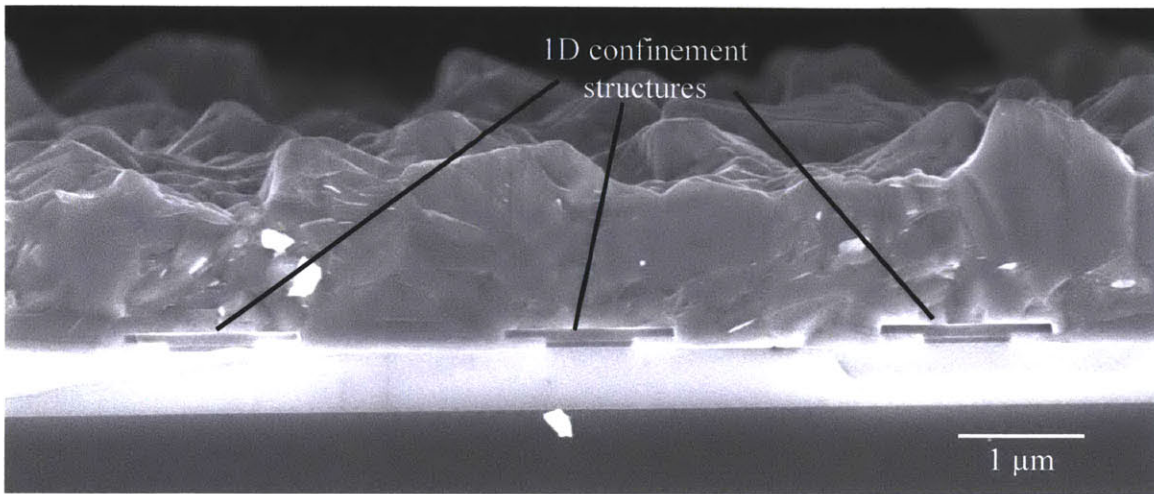
Figure 4.13. Cross-section SEM image of a typical 1D-confined sample used for Hall effect measurement. The Ge has grown over the 1D confinement structures.

Figure 4.14 presents the data from Hall effect measurements on three blanket (as-deposited) poly-Ge films and three Ge films grown from 1D GCLG structures, plotting carrier concentration against inverse film thickness. As was elucidated in Chapter 2, films' grain boundaries grow larger as the films get thicker, meaning their grain boundary densities decrease with increasing thickness. Thus, it follows that the carrier density decreases as the film's thickness increases, as observed in Figure 4.14. However, for a given film thickness, it is observed that the carrier concentration is significantly lower in a film grown from a 1D GCLG structure than in a blanket film. This indicates that the confinement is decreasing the carrier concentration, most likely by increasing the grain size, and is thus making the material more suitable for use in active p-i-n photonic devices.
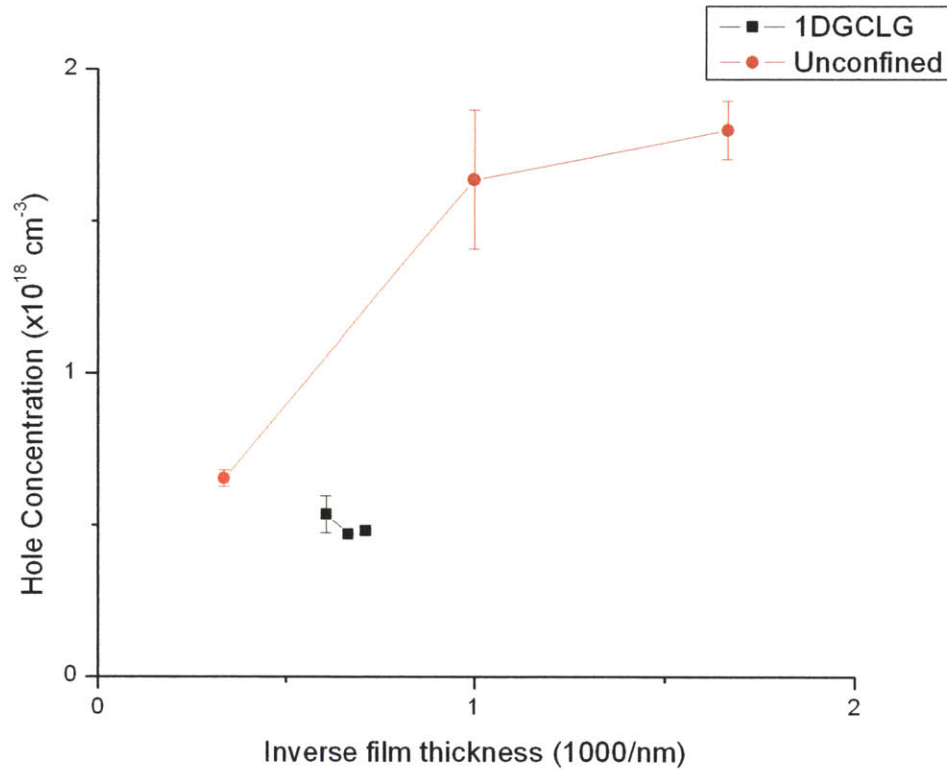
Figure 4.14. Hole concentration versus inverse film thickness for three unconfined poly-Ge films as well as three films grown from 1D confinement. The thinnest film grown from confinement had thickness 1400 nm and aspect ratio 4.5, the second such film had thickness 1500 nm and aspect ratio 1.4, and the thickest film had thickness 1650 nm and aspect ratio 2.5. Lines are added to guide the eye and error bars are ± one standard deviation.

It is to be noted, however, that the increasing 1D GCLG channel's aspect ratio of the films presented in Figure 4.13 does not always correspond to a drop in the carrier concentration. It is expected that a larger aspect ratio would give a lower carrier concentration, due to the enhanced grain selection, though this is not the rule in the three films examined. In the figure, the film with 1400 nm thickness and aspect ratio 4.5 had a higher hole concentration than the film with thickness 1650 nm and aspect ratio 2.5. We should also bear in mind that the concentrations given by the Hall effect measurement for

these two samples were 3.6×10^{17} cm^{-3} and 3.0×10^{17} cm^{-3}, however, so the difference is only 20% and thus is not dramatic.

It is possible that the aspect ratio does not play an extremely significant role in the carrier concentrations of films grown from 1D confinement, as the growth of the film from the 1D confinement structure is such that the film is also growing around one or two corners in order to form the continuous film, as depicted in Figure 4.15. This effect of "turning a corner" was highlighted in Chapter 3, when it had previously been explored for use in laterally-overgrown poly-Ge. From work done on this type of material, it was observed that the corner-turning also increased the grain size. Thus, the data presented in Figure 4.14 are a convolution of the effects of geometric confinement and turning corners, and the effects of the increasing aspect ratio may be partially lost in this corner-turning effect. (Due to the nature of the 1D GCLG structure, obtaining a film for Hall measurement that does not include any turned corners does not seem possible.) Additionally, the aspect ratio difference among the films may not be significant enough to cause an appreciable difference in the carrier concentrations; the aspect ratio must be kept fairly low in order to ensure that a continuous film is obtained within a reasonable growth time, as higher aspect ratios would cause more discrepancies in growth velocities between fast-growing grains and other grains and the growth time would thus have to be increased to minimize film voids in areas of slower-growing grains.
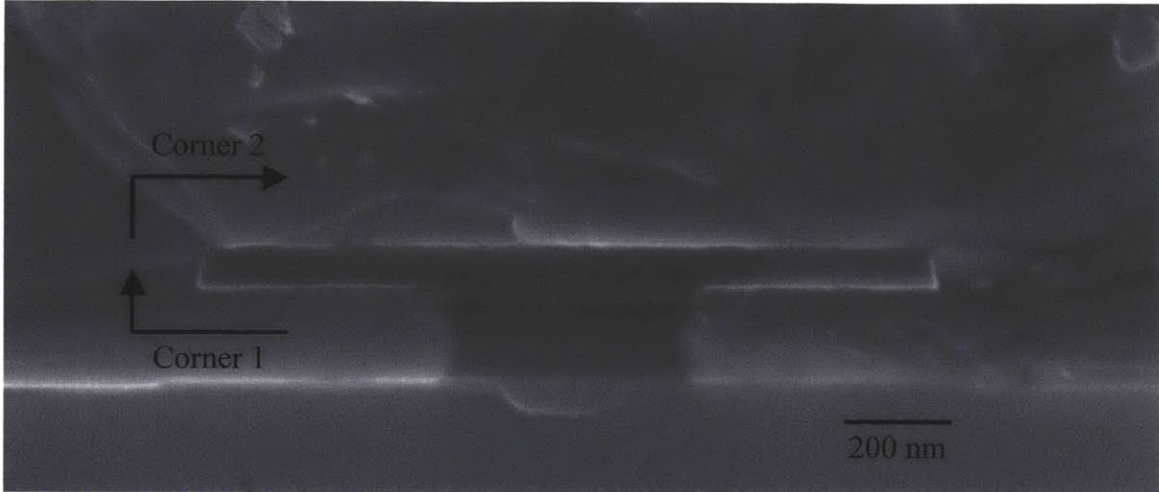
Figure 4.15. Depiction of the concept of "turning a corner" in the case of growth in a 1D GCLG structure.

It should also be mentioned that defects other than grain boundaries may cause p-type carrier generation; for example, dislocations and point defects can serve as carrier generation sites [80-83]. While we believe that the grain boundaries will have the most significant influence on the carrier density, the decrease in carrier concentration as measured by Hall effect may also indicate a decrease in dislocation and/or point defect concentration. In any case, confinement during growth reduces the p-type nature of the material and makes the Ge more likely to serve our purpose in active photonic devices.

Photoluminescence (PL) measurements are another common method of determining the electrical qualities of a material. Unlike Hall effect measurements, PL measurements do not require a continuous film. In a PL setup, laser light of energy greater than that of the material's band gap is focused on the material. The laser excites the material such that electron-hole pairs are generated; these pairs recombine either radiatively (giving off radiation) or non-radiatively (not giving off radiation, but instead releasing energy in another manner, most commonly as phonons). The emissions from the radiative recombinations are collected through a tunable filter and the intensity is

plotted versus wavelength. The non-radiative emissions are not collected and thus do not register in the PL intensity. A PL intensity plot for a semiconducting material will show a peak around the material's band gap, as this is the wavelength at which the majority of the radiative recombination emits. Comparing data from two different materials gives an indication of the efficiency of radiative recombination compared to that of non-radiative recombination, or what fraction of the generated electron-hole pairs recombine radiatively versus non-radiatively. A higher PL signal means the sample in question has a higher radiative recombination efficiency relative to its non-radiative recombination efficiency.

Material defects often serve as sites for non-radiative recombination because they provide an energy level within the band gap that "traps" a carrier and promotes its energy transfer to a phonon instead of a photon. As poly-Ge is highly defective and thus likely contains a large number of traps, it was hypothesized that our poly-Ge would have a very low PL intensity compared to single-crystal Ge; Figure 4.16(a) shows that this is true, where PL from n-type epi-Ge (which has a low defect density and a high amount of radiative recombination at the band gap energy) is plotted against PL from Ge grown from 1D confinement (aspect ratio 4.5) as well as PL from blanket poly-Ge. As 1D confinement increases the grain size and decreases the grain boundary density over blanket poly-Ge, it was believed that 1D GCLG Ge would exhibit a stronger PL intensity than blanket poly-Ge. As shown in Figure 4.16(a) and further elucidated in Figure 4.16(b), this also is indeed the case. The PL data further confirm that the material grown from the 1D confinement structure has a lower defect density than does the blanket poly-Ge. It should also be noted that the laser spot used in the PL measurement is large relative to the

confining structure and penetrates the top oxide, so the poor material in the 1D GCLG channel is also probed, likely giving lower PL than if only the material outside the channel were investigated.
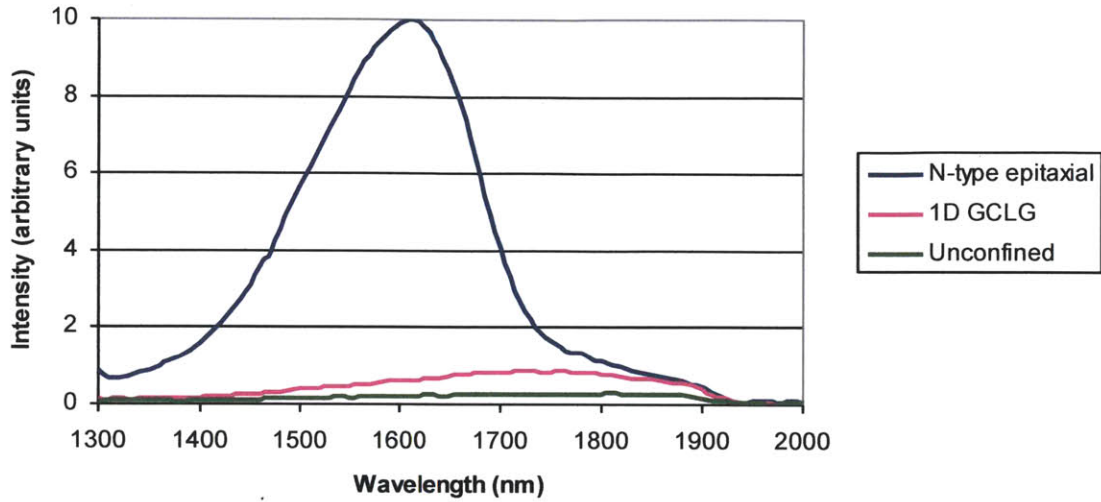
(a)
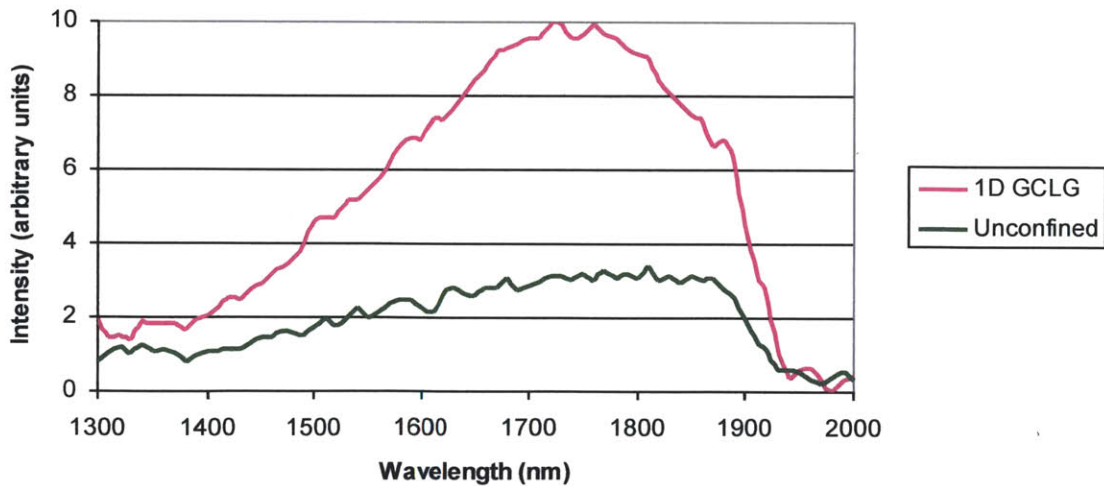
(b)

Figure 4.16. PL spectra for (a) single-crystal n-type epitaxially-grown Ge, 1D GCLG Ge (aspect ratio 4.5), and unconfined (blanket) poly-Ge, and (b) the 1 GCLG Ge and blanket poly-Ge from (a), shown to more accurately demonstrate the enhanced PL intensity of the 1D GCLG Ge compared to the blanket poly-Ge.

PL spectra were also obtained for three 1D GCLG samples of differing aspect ratios, where the samples were the same as those used for the Hall effect measurements shown in Figure 4.14. The PL data for these samples are presented in Figure 4.17. It is expected that a larger aspect ratio would give a stronger PL intensity. It is observed that, while the film grown from the 1D GCLG structure with the greatest aspect ratio (4.5) does exhibit the greatest PL intensity, the difference between the aspect ratio 2.5 and aspect ratio 1.4 films does not appear to be significant, and the difference in PL intensity between these films and that with aspect ratio 4.5 is also not large. The case with PL is similar to that seen in the Hall effect measurements taken to determine the films' carrier concentrations, in which the differences in aspect ratios did not give large differences in the electronic properties of the films. However, in the case of the Hall measurements, the film with aspect ratio 4.5 did not have the lowest carrier concentration, though in PL it shows the highest intensity. We can therefore state that the differences in electrical characteristics among the three films are too miniscule to be reliably tested. We postulate that the same effects that likely caused the minimal variations in Hall effect results also hold true for the PL spectra – namely, that turning corners in the structure may wash out some of the effects of the varying aspect ratios, and that the films' aspect ratios may not be disparate enough to observe significant changes in the films' electrical characteristics.
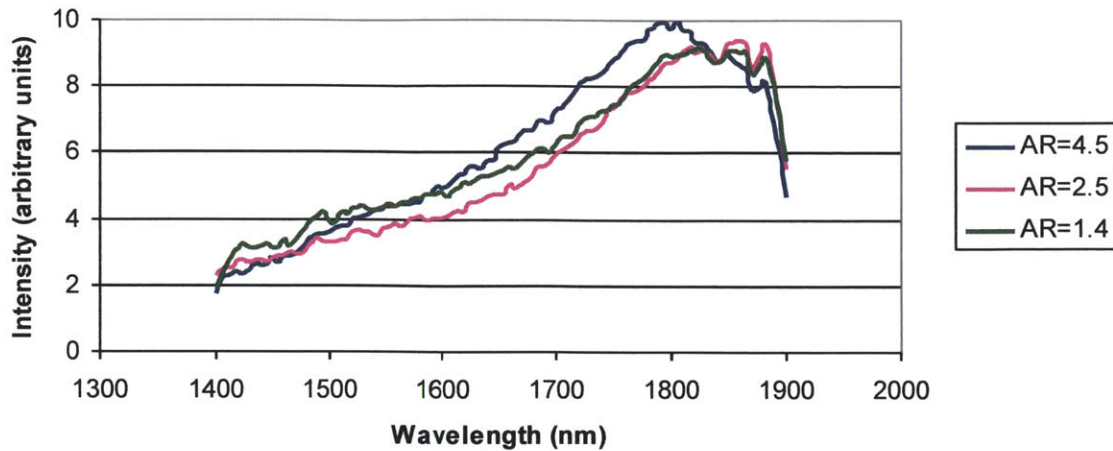
Figure 4.17. PL spectra for three films grown from 1D confinement, with varying aspect ratios of the GCLG channel.

4.4   Chapter summary

In this chapter, the development of the process of one-dimensional confinement of poly-Ge was presented and data from a number of experiments on the resulting material were shown. SEM images indicated that the growth proceeded as anticipated and that it exhibited a faceted nature, similar to that seen in single-crystal Ge grown epitaxially on Si. TEM imaging and diffraction showed the confining channel's ability to decrease the Ge's defect density as deposition within the channel proceeded. XRD showed that the channel has an influence on the material's texture, and we concluded that the material is most likely (110)-textured in the growth direction. Hall effect measurements demonstrated the results of the 1D confinement on the electrical characteristics of the material as observed in the carrier concentrations, and PL measurements further indicated a decreased defect density as the material is confined in one dimension during deposition. Varying the 1D confinement's aspect ratio from 1.5 to 4.5 did not significantly impact the electrical properties of the films grown from 1D confinement, however.

Chapter 5: Geometrically-confined lateral growth of germanium on amorphous silicon: two-dimensional confinement

5.1 Motivation

In Chapter 4, a method for grain size enhancement using geometrically-confined lateral growth (GCLG) of Ge from a-Si, with confinement in one direction (vertically), was discussed. While the 1D GCLG is able to limit the multiplicity of grain orientations in the vertical direction and thus select some grains for extended growth outside the channel, these selected grains occur at random locations along the channel (in the plane of the wafer) and thus two significant challenges arise. The first is that the large, selected grains' locations cannot be precisely controlled. Determination of a large grain's placement on the wafer would be necessary for the definition of devices from these grains. Second, though some grains are selected, many grains that are not fast-growing grains also emerge from the channel. Thus, it is apparent that the growth confinement structure needs improvement before it can legitimately be considered for the low-T non-epitaxial fabrication of BEOL-compatible photonic devices.

5.2 Fabrication

To further enhance the constrictive nature of the channel, it would be advantageous to not only confine the growth vertically, but also laterally. This is called two-dimensional (2D) GCLG. To fabricate 2D GCLG structures, we began with 6" Si wafers (orientation and doping are unimportant) and used thermal oxidation to grow a layer of SiO_2 on the silicon. We then deposited a thin (50-120 nm) layer of a-Si by plasma-enhanced chemical vapor deposition (PECVD) on the SiO_2 and patterned the a-Si using photolithography. The patterned a-Si was then overlaid with SiO_2 deposited by

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PECVD, and the samples were coated with photoresist. The samples were patterned with rectangles and were etched through the PECVD SiO_2 and the a-Si by reactive ion etching, down to the thermal SiO_2. The a-Si was undercut etched using 20% tetramethylammonium hydroxide (TMAH) in DI water at 80° C for varying amounts of time, on the order of a few minutes, to selectively etch the a-Si and not the oxide. The wafers were then cleaned in a double piranha clean (3:1 H_2SO_4:H_2O_2) with a hydrofluoric acid (1:50 acid:DI) dip step in between the piranha cleans, and further cleaned in an RCA clean plus post-clean HF dip to passivate the Si surface. The wafers were then loaded into our hot-walled UHVCVD reactor idling at 450° C and $<1x10^{-9}$ Torr and allowed to anneal for approximately 1-2 hours to allow the PECVD-deposited layers to degas H. Ge was then grown on the structure by flowing 7.5 sccm GeH_4 in the UHVCVD reactor at 450° C.

The steps for growth on 2D GCLG structures are identical to those in the growth from 1D GCLG structures except that the a-Si layer is patterned *before* being overlaid with SiO_2. The patterning defines the a-Si layer into thin features, such as strips, and the processing then follows the same steps as in Figure 4.3. The 2D GCLG structure before and after Ge growth is shown schematically in Figure 5.1.
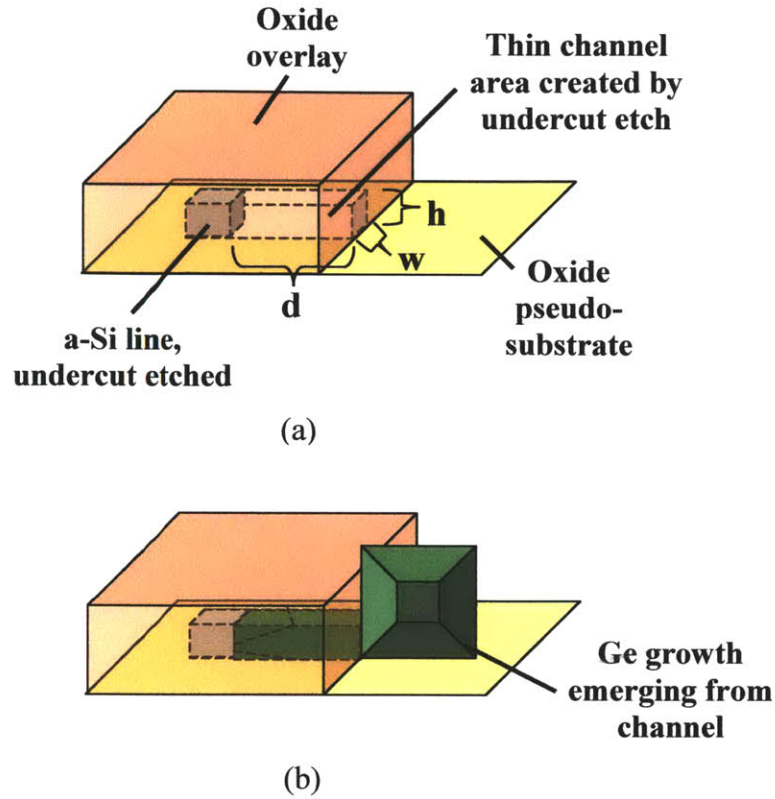
Figure 5.1. Schematic of the 2D GCLG structure (a) before Ge growth, and (b) after Ge growth. The structure is fabricated in the same manner as that in Figure 4.3, but with an additional step in which the a-Si layer is patterned before being overlaid with oxide. Figure is not to scale.

Such a 2D GCLG structure solves both issues mentioned above: it eliminates the emergence of slower-growing grains from the channel and it allows for the precise placement of single-crystal material.

It was hypothesized before beginning our work with 2D GCLG that the confinement dimension in the lateral direction (the plane of the wafer) would have to be on the order of the poly-Ge grain size, like the vertical confinement dimension in 1D GCLG, in order to have an effect on the Ge within a reasonable growth distance (<1 μm). The small dimension ensures that a single grain may occupy the entire channel and serve as the sole seed for single-crystal growth in the space outside the channel.

This requirement of a very small lateral channel dimension initially proved difficult to fabricate. Using the i-line stepper in the Integrated Circuits Laboratory at MIT's Microsystems Technology Laboratories, researchers have been able to define resist lines down to approximately 400 nm in width using conventional step-and-repeat exposures. However, the goal for the fabrication of 2D GCLG structures was to define ~200 nm or narrower line widths, so changes had to be made to the traditional method of exposure in the stepper.

First, we used the stepper's offset feature, in which a mask area can be initially exposed and then exposed again with a translational offset on the wafer surface (of at least 500 nm) without removing the wafer from the stepper. As we use a positive resist, any resist that is exposed is subsequently removed upon development. Any resist that is exposed more than once is also removed, but unexposed resist stays on the wafer.

We first exposed long, thin strips with inter-strip spacing of 1.5 μm. We then used an offset of 0.8 μm to 1.2 μm in the direction perpendicular to that of the strips' long axes to do another exposure of some of the inter-strip resist that was not exposed in the first exposure. This left thin strips of unexposed resist, down to approximately 200-300 nm in width, on the wafer. Figure 5.2 illustrates this double exposure technique.
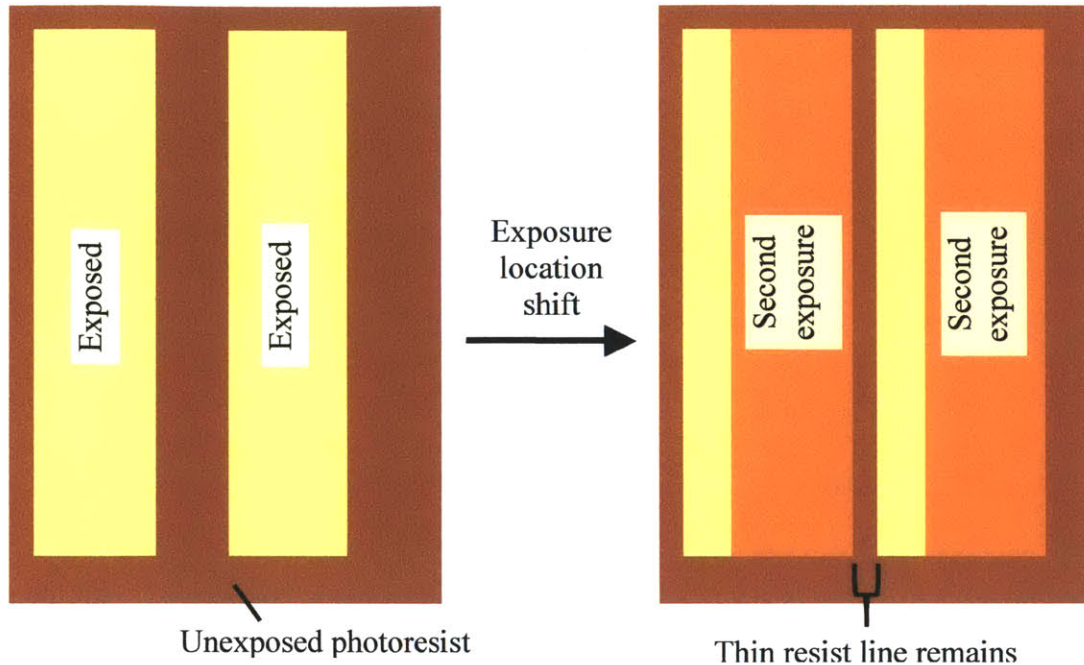
Figure 5.2. Illustration of the double exposure technique employed to define resist line widths down to approximately 200-300 nm in an i-line stepper. A positive photoresist is used.

An offset of more than 1.2 μm did not prove beneficial, although the nominal unexposed resist width was 1.5 um. Offsets between 1.2 μm and 1.3 μm gave the same line widths as offsets of 1.1-1.2 μm, and offsets greater than 1.3 μm caused all resist to be removed. After the double exposure process, the wafers were transferred to a dry etch chamber and were subjected to an oxygen plasma for 30 seconds. The plasma etches resist and further shrinks the lateral dimension of the lines and has been used in other work to obtain thin resist lines (for example, in Ref. 58). However, it was found that resist etch times greater than 30 seconds often gave lines with significant sidewall roughness, as shown in Figure 5.3. It was also found that the etching caused a deterioration of the lines' vertical dimensions, such that the lines lost their height. Such lines are shown in Figure 5.4. SEM images of photoresist lines after the double exposure and 30-second plasma etch sequence are shown in Figure 5.5. As the a-Si to be etched

was generally under 100 nm in thickness and the dry etch has strong selectivity to resist, vertical deterioration of the resist did not cause issues in the a-Si etch,
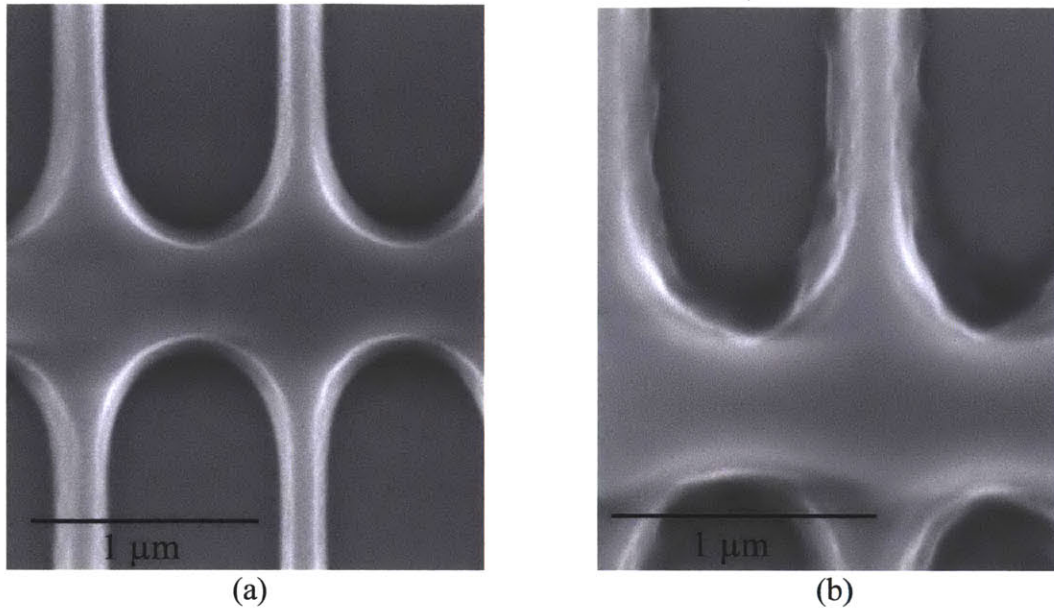
Figure 5.3. PVSEM images of photoresist lines remaining after (a) 30-second oxygen plasma etch, and (b) 50-second oxygen plasma etch. The nominal width of the resist lines before the plasma etch was 0.5 μm.
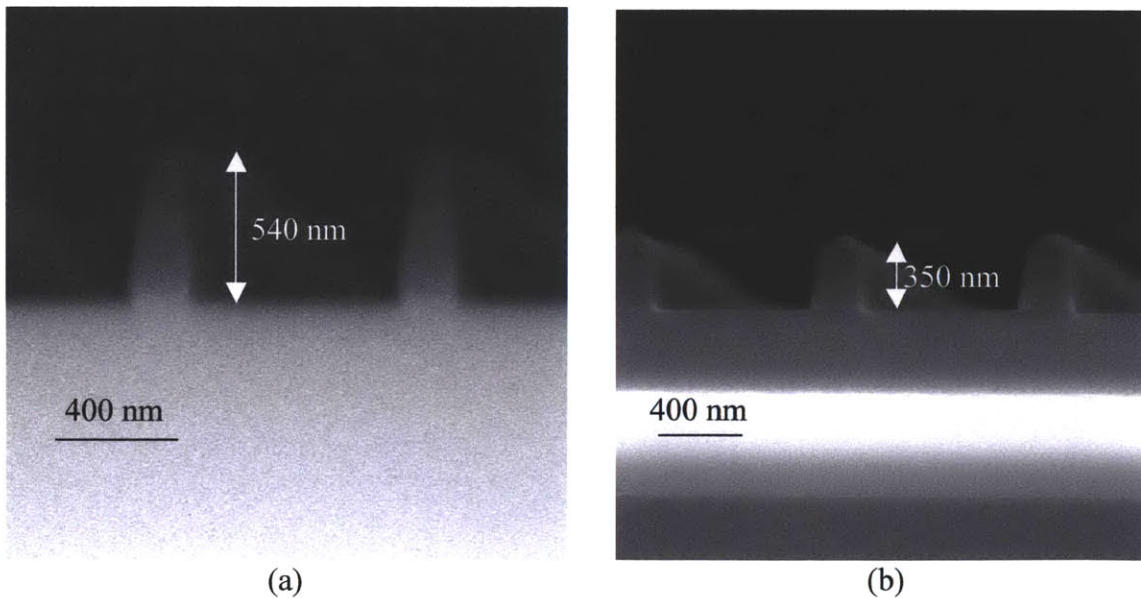
Figure 5.4. XSEM images of photoresist lines after (a) 30-second oxygen plasma etch, and (b) 40-second oxygen plasma etch.
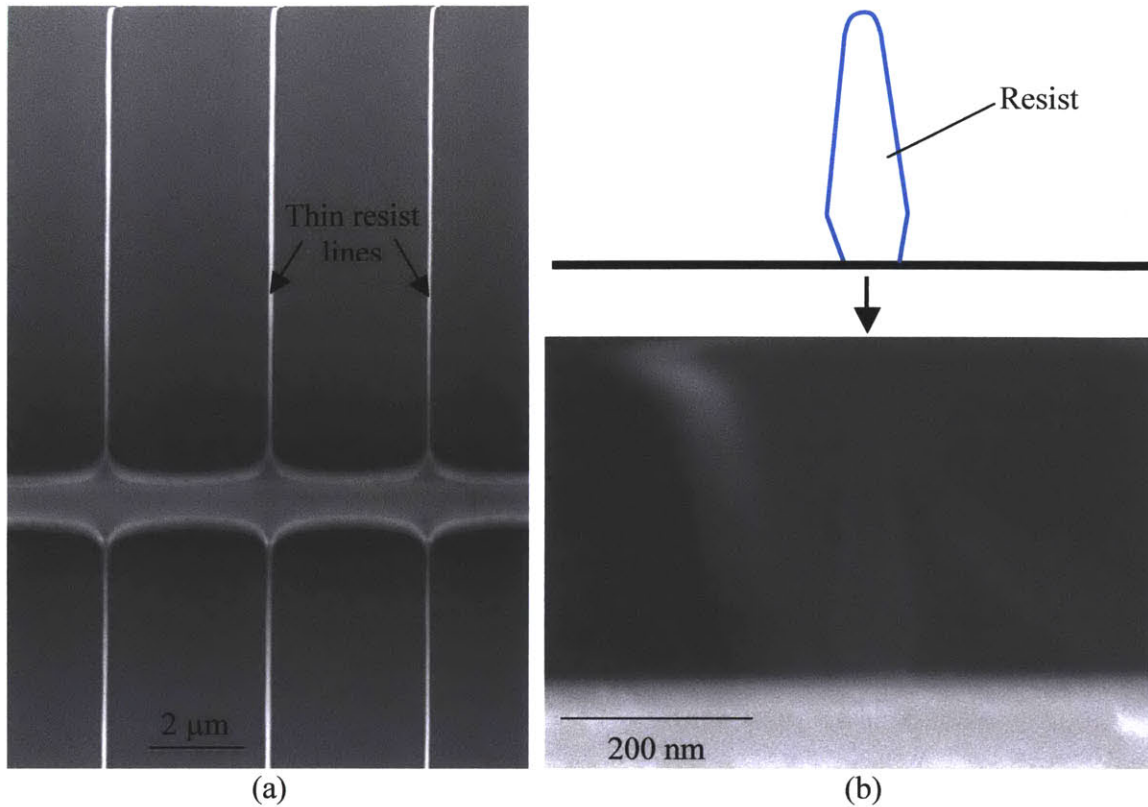
Figure 5.5. (a) PVSEM image and (b) XSEM image of a photoresist line after the double exposure and 30 second oxygen plasma etch, with instructional schematic of the resist. The line width of the resist is in the range of 65-115 nm.

Using the double exposure process to define the very narrow features imposes a lower limit on the spacing of the channels (the a-Si strips). If the minimum feature size of the exposure system is 500 nm, then a 500 nm area must be exposed next to a 500 nm area that is unexposed and subsequently exposed again with an offset of a few hundred nanometers to obtain a thin line width. In the case of the i-line stepper at MIT, however, the minimum offset step size is 500 nm, so the width of the unexposed region must be at least 500 nm plus the desired width of the offset shot's line width. This combination of minimum resolvable feature size plus minimum offset distance imposes a lower limit on the spacing distance between channels. In the case of the MIT i-line

stepper this distance is approximately 1.2 μm (= 0.4 μm minimum feature size + 0.5 μm minimum offset + 0.3 μm minimum residual resist line width).

As in the fabrication of the 1D GCLG structures, a TMAH etch was used to undercut etch the a-Si features. It is desirable to know the etch rate of the a-Si in the 2D GCLG channels, as the restrictive nature of the 2D GCLG channels may cause a variation in the TMAH etch rate from that observed for the 1D GCLG channels (e.g. due to mass transport flow restrictions in the case of the 2D GCLG channels). In the case of the 1D GCLG structures, observing the extent of the TMAH etch was straightforward: a cross-section cut through the structure could be performed by cleaving the wafer in the area with the features. However, in the case of the 2D GCLG structures, such a simple preparation is not possible as the cross-section must be performed in very precise locations (due to the lateral definition of the a-Si features). To circumvent this issue, the top oxide was removed from a few samples after the a-Si etch step so the extent of the etch could be observed from above, as shown in Figure 5.6. These samples were not used for Ge growth. The a-Si etch rate in the case of 2D GCLG structures varied as in the case of the etching of 1D GCLG structures, and was approximately 2-4.5 nm per second. Channels near each other, though, appeared to have identical etch rates, so the etch rate variation may not be due to local fluctuations in fluoropolymer formation from the oxide etch, as hypothesized in Chapter 4.
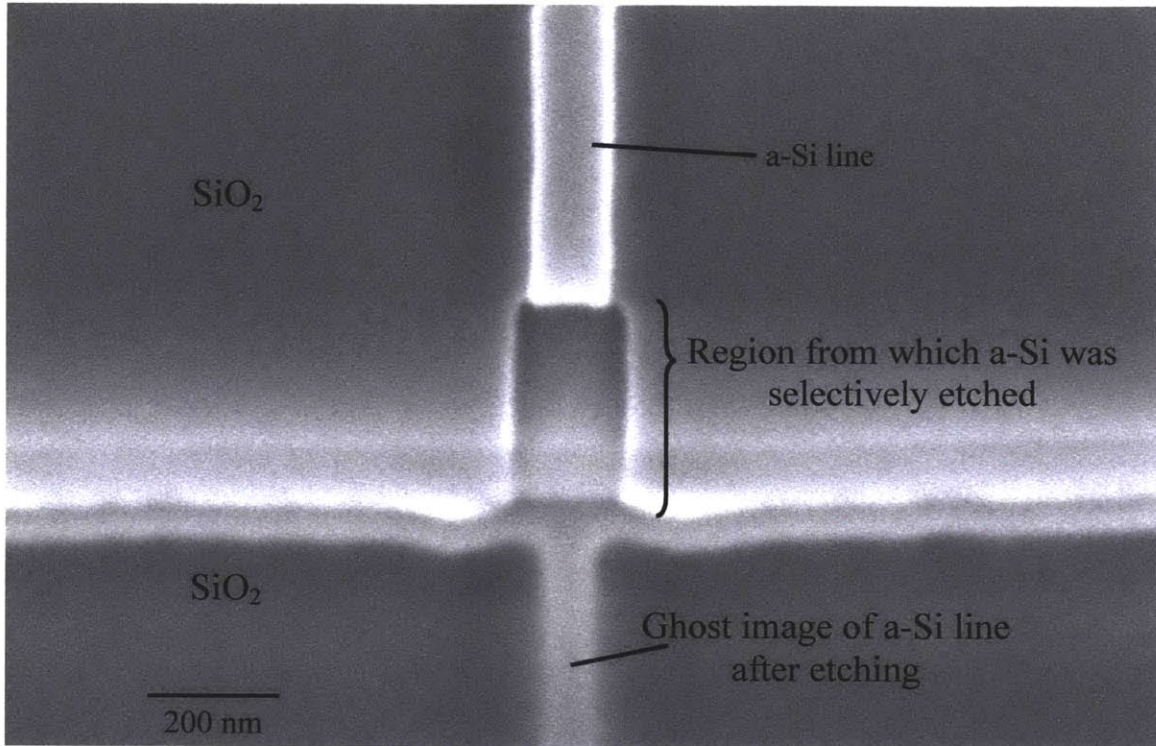
Figure 5.6. PVSEM image showing the 2D GCLG structure with the a-Si etched for 300 seconds.

A final consideration was whether the germane (GeH_4, the germanium precursor gas) would be able to reach the a-Si seed inside the 2D GCLG channel. Since the pressure inside the UHVCVD chamber is low enough that the gas behaves more as individual molecules with a mean free path on the order of 10-100 cm (see Chapter 3), we did not anticipate any mass transport limitation into the channel; the GeH_4 gas inside the chamber can be thought of as a cloud of molecules instead of a flowing medium, so the GeH_4 concentration inside the channels should be similar to that outside the channels. The Knudsen number *Kn* of the GeH_4 inside the channels is on the order of (10 cm / 1 um) = 10^5, meaning the gas in the channel can be considered to be well into the molecular regime. Assuming the interaction of GeH_4 with the channel sidewalls does not diminish

the molecule's ability to deposit Ge on the a-Si seed, there should therefore be no effects of the channel's size on the deposition of Ge on the a-Si seed.

5.3   Results and discussion

5.3.1   SEM results

Selected plan view SEM images of 2D GCLG crystals are shown in Figure 5.7. In the figure, the channel is clearly seen as the bright white columnar area at the bottom of the image; above the Ge growth, there is another region that appears similar to the channel but darker. This area is an artifact of the dry etches of the top oxide and the a-Si strip; only oxide remains in this area.

As is clearly seen in Figure 5.7, the crystal growing from the channel is often faceted across a large part of its visible surface. This implies that it is a large grain or single crystal, where the faceting occurs to reduce the crystal's surface energy; small grains would not exhibit such extended faceting, as each grain would try to minimize its own surface energy and thus would exhibit different facets than those of its neighbors. The images also show that it is possible to place the crystals in specific locations across the wafer, which was previously not possible with the random nature of the 1D GCLG structures.
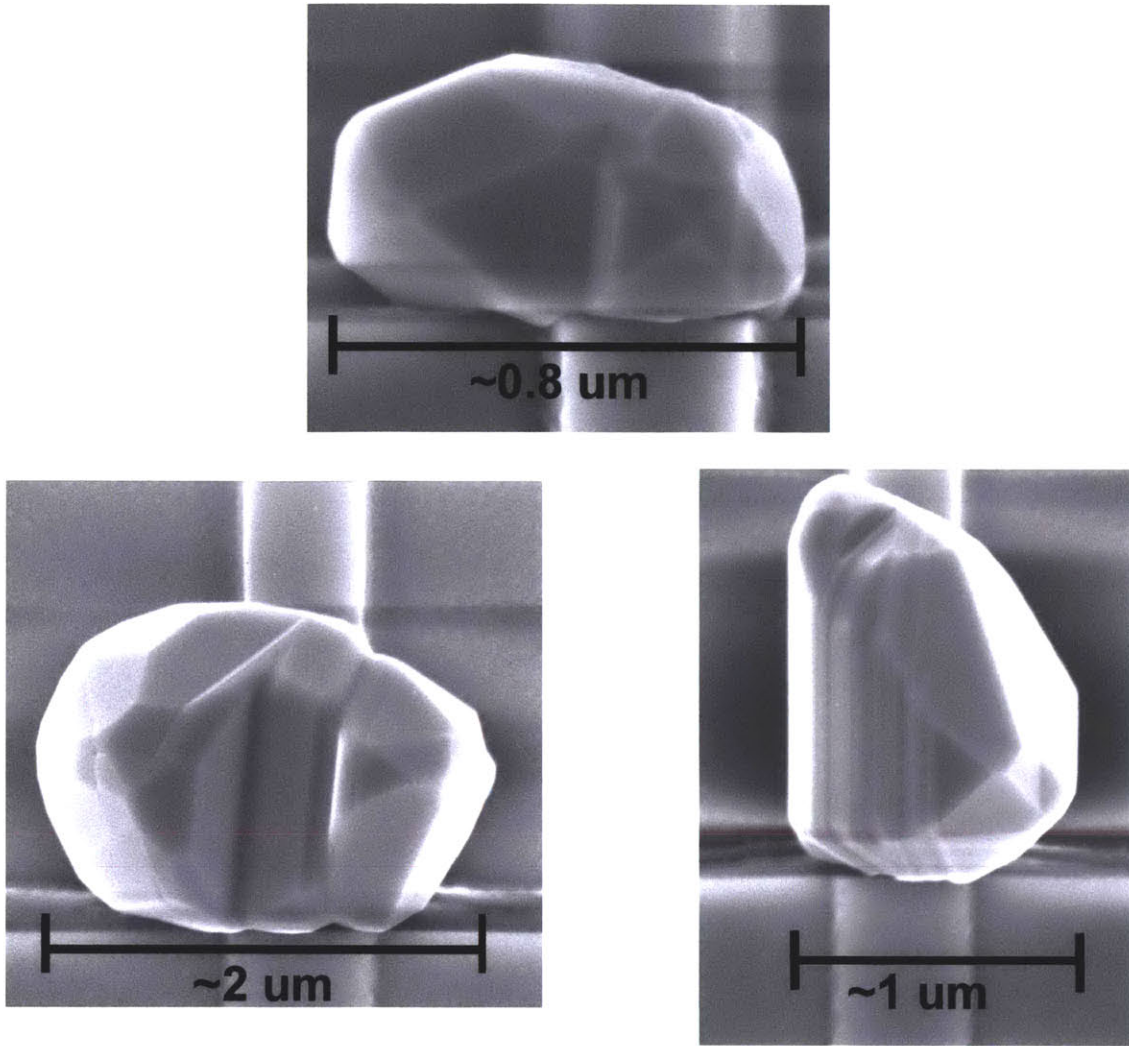
Figure 5.7. SEM micrographs of crystals growing from 2D GCLG structures.

5.3.2 Twin-mediated crystal growth

Also apparent in the images of Figure 5.7 are features that appear to be boundaries. These are highlighted in Figure 5.8. It is well known that germanium easily forms twin boundaries ($\Sigma3$ coincidence site lattice boundaries), as the $\Sigma3$ twin formation requires very little energy [84]. Thus, we hypothesized that these are likely twin boundaries, formed during the early stages of growth in the channels and subsequently propagating out of the channels. Evidence supporting the idea that these features

propagate from the insides of the channels comes from the fact that all such features observed in the SEM appeared to originate within the channel and propagated in a line-of-sight manner to the end of the growth.
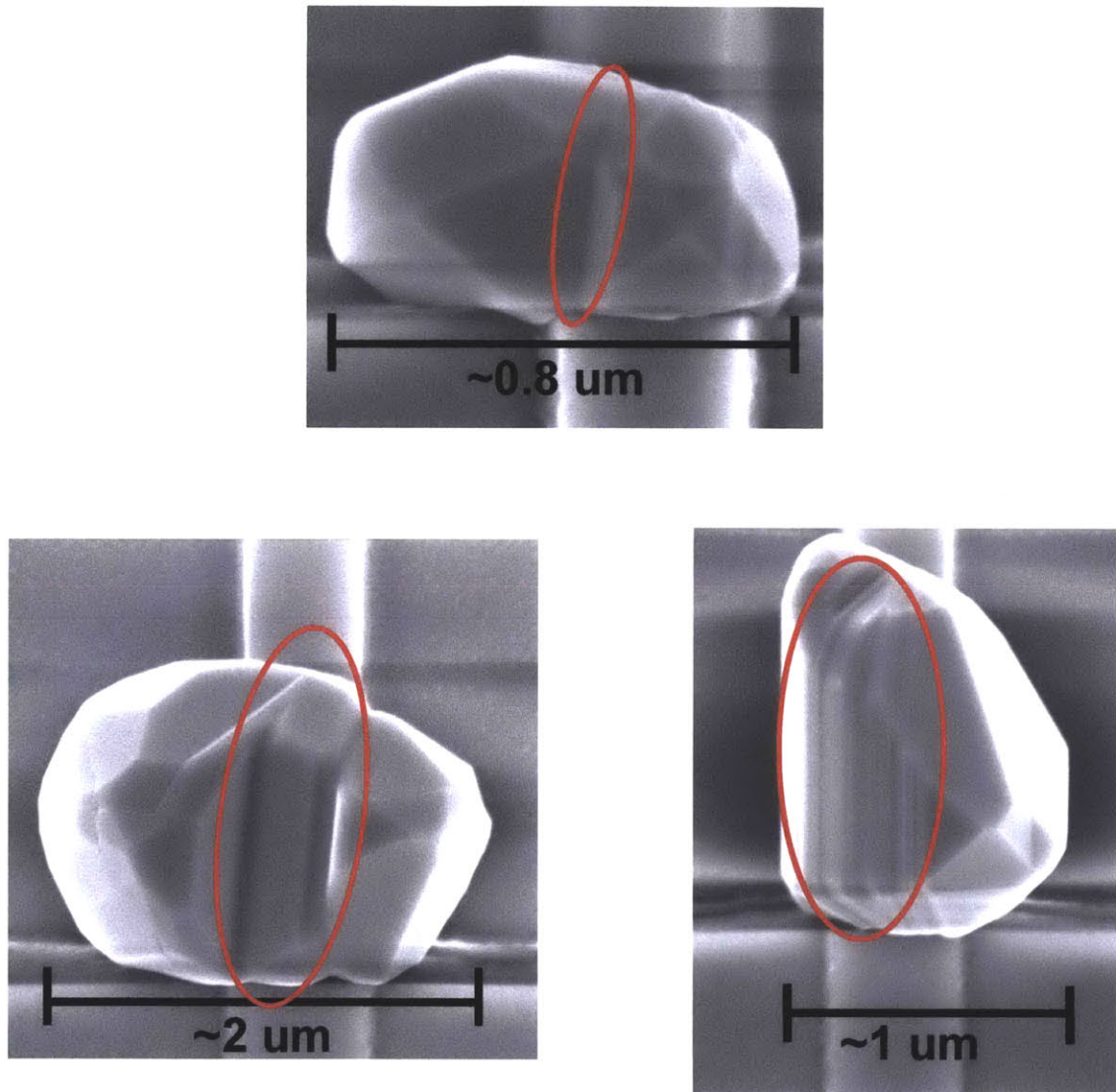
Figure 5.8. The images from Figure 5.7 with the features in question highlighted. We hypothesized that these features are twin boundaries.

To analyze the boundaries observed in the crystals in Figures 5.7 and 5.8, electron backscatter diffraction (EBSD) was performed on many samples. In EBSD, the electron beam of an SEM is diffracted off the atomic planes of the specimen under examination

and the diffracted lines are collected by a detector mounted in the microscope. The electron diffraction from the planes follows Bragg's Law, such that planes more closely spaced show a larger spacing in their diffracted lines. Using this relation and the known angles between planes within the crystal system, the resulting Kikuchi pattern (the set of diffraction lines observed from the sample) can be analyzed to determine the crystal orientations within the sample. These various grain orientations within one crystal can be compared to each other and the types of boundaries between the grains (e.g. twin, higher-Σ coincidence site lattice boundary, general grain boundary, etc.) may be computed.

Crystals grown from 2D GCLG and analyzed with EBSD show $\Sigma 3$ {111} twin boundaries as had been predicted from our discussion in Chapter 2, but some also show $\Sigma 9$ boundaries. $\Sigma 9$ boundaries can result from the intersection of two $\Sigma 3$ boundaries [84], so it is likely that $\Sigma 3$ boundaries intersect, either inside or outside the channel, to form $\Sigma 9$ boundaries. In addition, EBSD shows that the facets of the 2D GCLG crystals are {111}. Thus, growths like those seen in Figure 5.8 can be determined to have a <110> orientation in the direction of the channel, as the <110> directions form the intersections between the {111} twins and the {111} facets. This result – that the crystal is (110)-textured in the channel – is as expected from our observations of (110) texturing of blanket films in Chapter 3.

With regard to the devices for which this material may ultimately be used, $\Sigma 3$ and $\Sigma 9$ boundaries should not negatively impact device performance. Both the $\Sigma 3$ and $\Sigma 9$ boundaries are coherent [84, 85], so there are no dangling bonds across the boundaries. According to simulations, the $\Sigma 9$ boundary does introduce new states in the material's electronic structure, but these states exist within the valence band (primarily centered

around ~5eV below the valence band maximum), the boundary does not introduce states in the band gap [85, 86]. Dangling bonds at the boundaries, as explained in Chapter 2, are the primary cause of device degradation when using polycrystalline materials, so the presence of boundaries with no dangling bonds and only electronic states outside the band gap is not of significant concern.

As shown in Chapter 2, twinning in FCC polycrystalline materials causes (110) texturing, but untwinned films may also grow with a (110) texture if they can sustain both (111) and (100) facets. X-ray diffraction (XRD) studies of our blanket poly-Ge (unconfined) films confirm that our poly-Ge has a (110) texture and SEM and EBSD studies of our 2D GCLG Ge show a (110) texture in the channel, but EBSD studies of our 2D GCLG Ge show that the facets are all {111}. Thus, we conclude that the (110) texture of our poly-Ge is caused by twinning. This is believed to be true not only for our crystals deposited at 450° C as in the case of GCLG, but also those deposited in the range of 350° C – 550° C, as the (110) texture is seen in our poly-Ge deposited throughout this temperature range (Chapter 3).

This finding of twin-mediated vapor phase growth extends previous research performed on twin-mediated crystal growth. As discussed in Chapter 2, it was shown that <110>-oriented Ge crystals grown from the melt at low undercooling grow by the adsorption of Ge atoms at the intersections of twin boundaries with the Ge surface, and we asserted that Ge vapor phase crystal growth should proceed in the same manner. Like previous researchers, we observed {111} planes bounding our crystals as well as twins on the {111} planes. We have also observed striking similarities between our material grown from 2D confinement and the ideal twin-mediated crystal growth morphology; the ideal

morphology for <110>-oriented crystals grown from the melt is shown in Figure 5.9a, while in Figure 5.9b is shown a Ge crystal grown during our work with 2D GCLG Ge, using a 6-hour Ge growth at 450° C and a subsequent 2.5-hour growth at 650° C to accelerate the growth process. (We assume this higher-T step did not significantly alter the crystal morphology, as growth is expected to proceed epitaxially on the seed grown at 450° C.) Based on these parallels, we assert that the theory developed for Ge crystals grown from the melt at low undercooling also holds for Ge crystals deposited from the vapor phase on a-Si by UHVCVD under our growth conditions, and that our crystals grow primarily by twin-mediated surface atom adsorption.

While all crystals observed do exhibit twin boundaries, many of them do not show any other types of boundaries. As twin boundaries are not grain boundaries, we conclude that we have successfully deposited single-crystal germanium on an amorphous substrate.
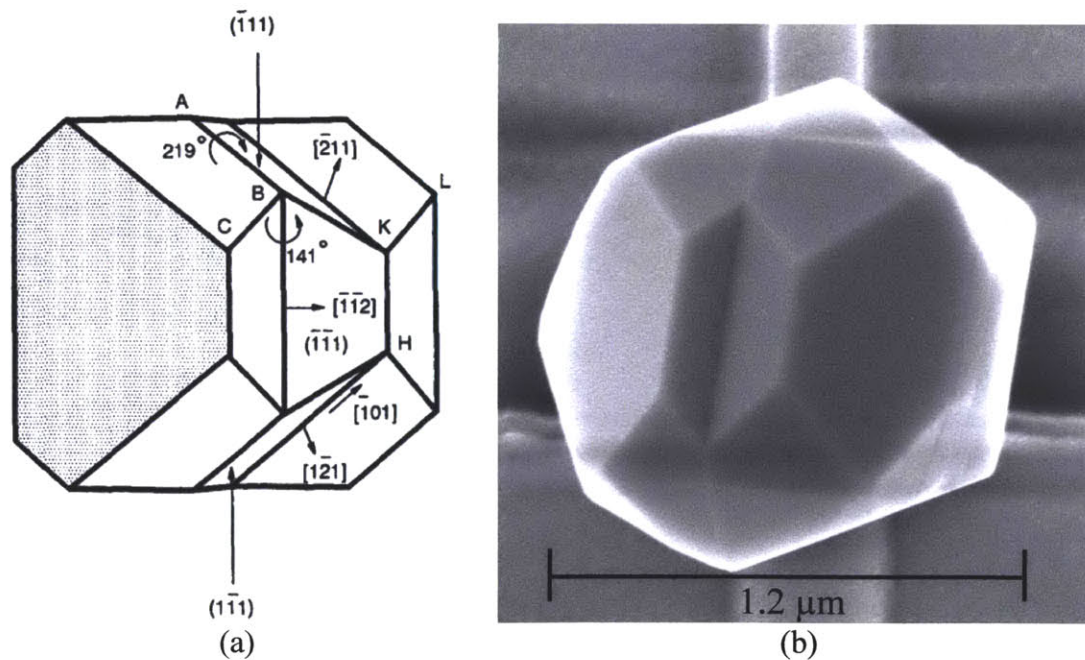
Figure 5.9. (a) Idealized schematic from Ref. 31, showing the various facets and growth directions associated with a <110> Ge dendrite grown from the melt at low undercooling. (b) Ge crystal grown in the current work from 2D confinement.

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5.3.3 Channel geometry optimization

Knowing the ideal channel geometry needed to obtain the best possible material would allow for the design of an optimal channel. We define the best possible growth outcome as one in which growths emerge from every channel, are of uniform size, are as large as possible, and contain as few grains as possible (i.e. are most monocrystalline); the optimum channel geometry would lead to such a growth. Figure 5.10 depicts two growth cases, where one shows consistent emergence and one shows inconsistent emergence.

(a)
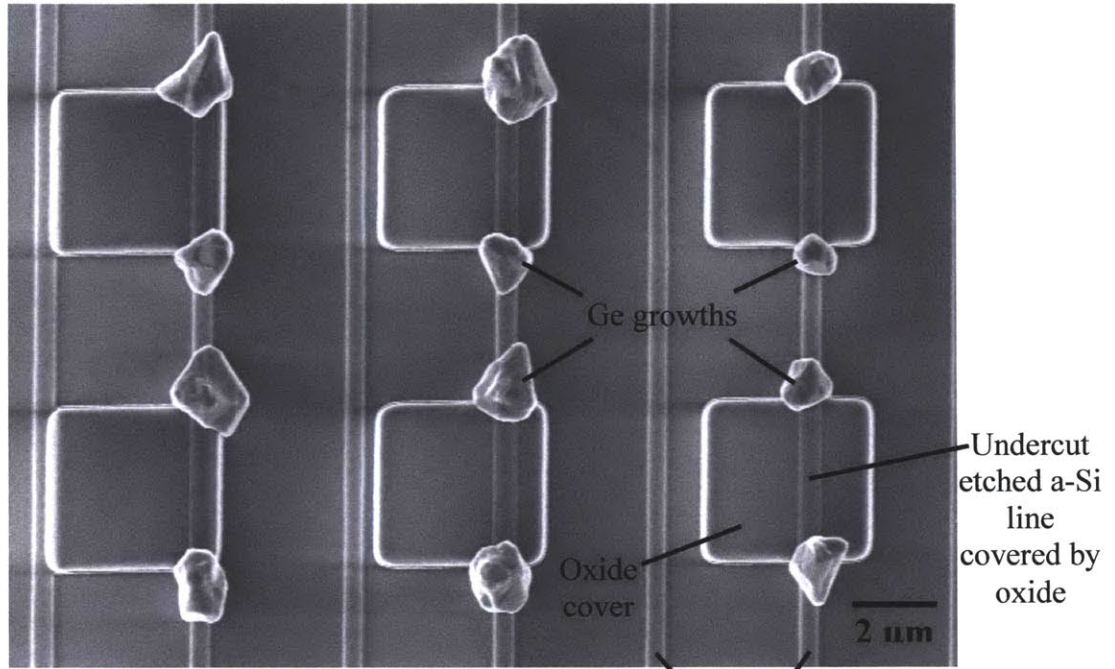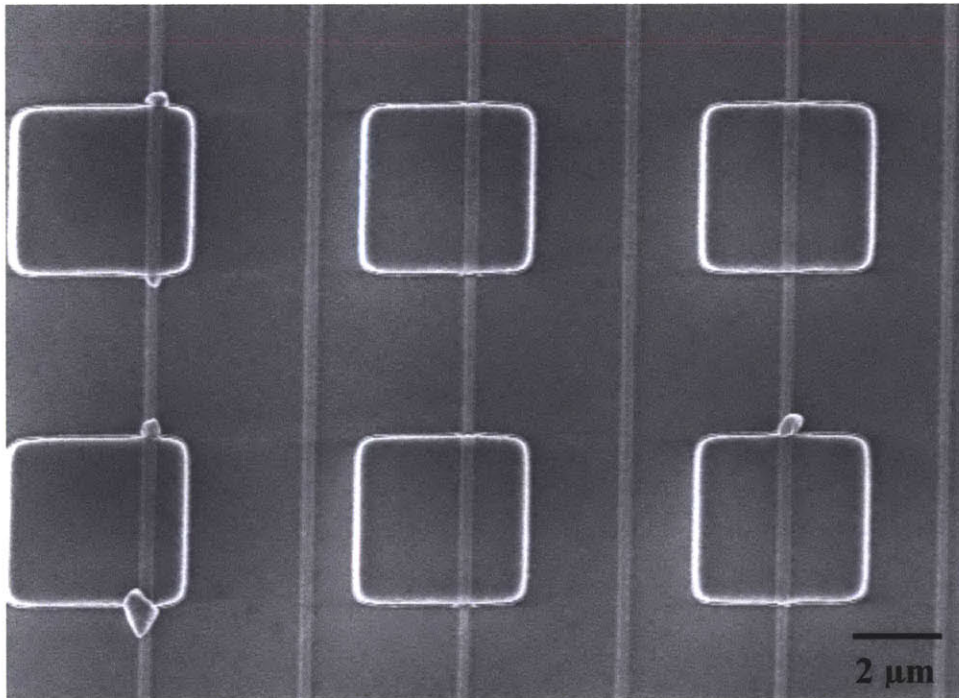
(b)

Figure 5.10. SEM plan-view micrographs showing an array of channels with (a) consistent emergence, and (b) inconsistent emergence. The channels in (b) are approximately half the width of those in (a), 2.5 times the length, and the same height.

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In order to understand the effects of the channel geometry on the Ge GCLG, the channel was modeled as a rectangular prism, with dimensions d, h, and w, as shown in plan view in Figure 5.11. The solid angle ratio $\frac{\Omega_c}{\Omega_n}$ was calculated, where Ω_c is the solid angle of the channel's opening as seen from the center of the a-Si nucleation seed and Ω_n is the solid angle of the four standard stereographic triangles surrounding a single (110) pole; outside the area defined by Ω_n, the crystallographic symmetry dictates that another of the {110} would be closer to the a-Si normal, so Ω_n defines the area swept out by the possible misorientations of one (110) pole with respect to the a-Si normal. The values of Ω_c and Ω_n are given by:

$$\Omega_c = 4\arcsin\frac{hw}{\sqrt{(4d^2+w^2)(4d^2+h^2)}} \tag{5.1a}$$

$$\Omega_n = 2\pi * \frac{4}{24} = \frac{\pi}{3} \tag{5.1b}$$

This ratio ($\frac{\Omega_c}{\Omega_n}$) was multiplied by the approximate number of grains that grow from the channel's a-Si seed, equal to the area of the seed in the channel (hw) in nm^2 divided by the average area of a Ge grain on a-Si, or the "grain base area," at 450° C. The average grain base area on a-Si from UHVCVD Ge deposition at 450° C, based on our TEM observations, is approximately 500 nm^2 (~25 nm in diameter).

The product of the solid angle ratio and the approximate number of grains growing from the a-Si seed gives N_G, the average number of grains expected to emerge from a channel of height h, width w, and length d:

$$N_G = \frac{\Omega_c}{\Omega_n} * \frac{hw}{500} \qquad (5.2)$$

This model assumes that, if a grain does not have a {110} normal oriented such that it would intersect the area defined by the channel exit, it would self-terminate and not emerge from the channel in the time of the growth. Images of growths that have self-terminated in the channels support this assumption. The model also assumes random nuclei orientations, though we calculated in Chapter 3 that the nuclei tend to have a slight preference for the (110) orientation. This preference is figured to be relatively small, however, and can be ignored for the sake of simplicity in modeling. The effect of this nucleation preference on the model will be discussed after the model's conclusions are drawn. Finally, the model assumes that the a-Si seed area in the channel is much larger than the grain base area, such that many grains may grow in a channel and we thus may use probability to determine the likely outcomes.
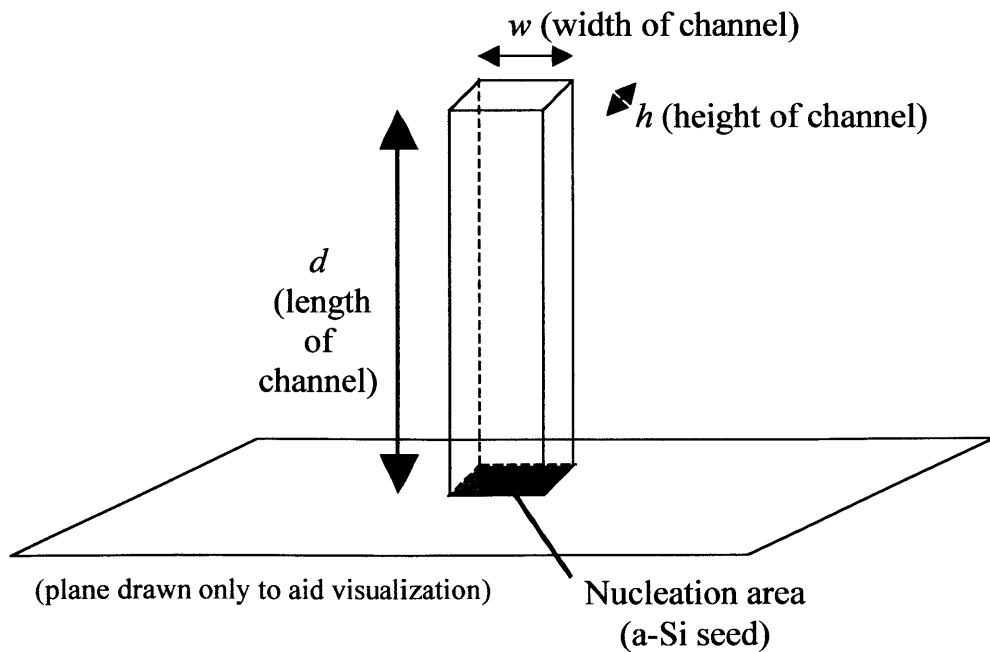
Figure 5.11. Schematic plan view of the channel geometry used in the modeling of 2D GCLG.

Setting $N_G = 1$ defines the channel's geometry at which there is a cutoff point: for geometries giving $N_G < 1$, growth is not expected to consistently emerge from all channels in an array, while for $N_G \geq 1$, growths are expected from every channel in an array. Figure 5.12 shows experimental data for growth emergence vs. N_G, taken from numerous channel arrays with at least 50 channels per array. The fabricated channels have heights between 35 nm and 120 nm, widths between 145 nm and 600 nm, and lengths between 450 nm and 1200 nm; the blanket growth from the same experiment had thickness ~1700 nm, so the growth was definitely of sufficient duration to be able to emerge from all channels. It can be seen in Figure 5.12 that the model predicts nearly the correct relation, as growths with N_G greater than approximately 0.6 show consistent emergence. This discrepancy is easily understood, as the model conservatively assumes that *any* growing grain that does not have a {110} normal that will intersect the area defined by the channel exit will self-terminate, though we know that grains can also grow (albeit more slowly) in non-{110}-normal directions. Thus, we would expect to see growth emergence for even lower values of N_G than predicted, as is indeed the case. Despite the discrepancy, the value of N_G still has strong physical significance and is of paramount importance when determining the ideal channel geometry, as will be seen.
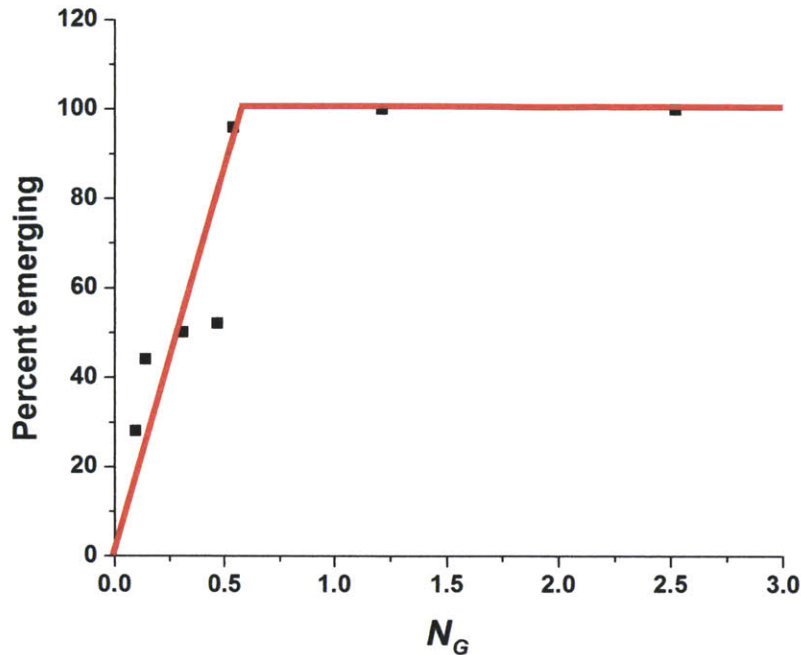
Figure 5.12. Percent of growths that emerge from their channels versus N_G. 100% or nearly 100% of growths emerge for values of N_G higher than those shown here. The red line is added to guide the eye.

We verified that the lack of emergence at low values of N_G is not due to an inability of the precursor GeH_4 molecules to reach the a-Si seed. In two samples with extremely different values of N_G (one with $N_G = 0.08$ and the other with $N_G = 9.6$), the maximum growth extent observed in each sample was approximately 2 μm, indicating that the GeH_4 is indeed able to reach the a-Si seed and the potential for growth is the same in both. The channel with the lower value of N_G does show much more disparity in growth extent among channels, however.

The relation between growth extent and N_G as well as between growth extent variation and N_G for an array of 2D-confined growths is depicted in Figure 5.13a and 5.13b, respectively. The growth size is given as a length and is measured by recording each growth's dimension in the direction of the channel, and the growth size variation is calculated as the coefficient of variation (CV) of the crystals' sizes, measured from at

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least 20 growths per data point. All channels investigated for the generation of the plots in Figure 5.13 had lengths in the range of 500 nm to 700 nm so as to minimize the effect of the channel length on the resulting growth extent. As seen in Figure 5.13a, the average growth extent initially increases with N_G as more fast-growing grains are correctly oriented to emerge from the channel and are also strongly confined. The average growth extent then attains a maximum in the range $2.0 \leq N_G \leq 3.0$ and subsequently decreases as the confinement is further reduced (N_G is increased) and the fast-growing grains are no longer efficiently selected. It levels off when the degree of confinement is low enough that the film is essentially unconfined. In Figure 5.13b, growths' CV values are nearly constant around 0.3, though a minimum is observed in the range $2.0 \leq N_G \leq 3.0$.

Based on the experimental data, the optimal N_G, chosen to maximize growth emergence frequency, growth uniformity, and growth size, lies in the range $2.0 \leq N_G \leq 3.0$. However, in order to ensure that the fewest (110)-oriented grains emerge from any given channel while still maintaining consistent emergence across many channels, a value of N_G in the low end of this range (i.e. nearest 2.0) should be chosen. This finding sets restrictions on the relations among the length, width, and height of a channel to obtain the best material quality (emergence, uniformity, extent, and monocrystallinity) from the confined growths.

This single constraint is not enough to completely define the optimum channel geometry, however; for example, an extremely thin and wide channel with a suitable length could have $N_G = 2.0$, though it is obvious that this case is not ideal because a fast-growing grain could not overcome all other grains in a very wide (albeit thin) channel. Thus, the channel width and height should be chosen to be as equal in size as possible in

order to maximize the symmetry of the channel and thus minimize the distance any grains need to grow in order to overtake all other grains in the channel. Furthermore, the geometry of the channel should also be chosen to obtain the shortest channel length, within the above framework, in order to minimize the growth time needed for growth emergence from the channels.

To summarize, the following geometric property guidelines for obtaining optimized growths with the shortest processing times apply to our 2D GCLG channels. Recall that we define the optimized growth as one in which Ge crystals emerge from every channel, are of uniform size, are as large as possible, and contain as few grains as possible (i.e. are most monocrystalline). The guidelines are listed here, roughly in descending order of importance:

1. $N_G = 2.0$

2. $w = h$

3. d as short as possible

The reasoning for the guidelines' order of importance is as follows: we have shown that the value of N_G has a dramatic effect on many growth properties, and is thus of principal importance. Setting w equal to h provides the highest symmetry and thus the highest probability that a single grain can overcome the others in the channel and lead to single-crystal growth. And minimizing d minimizes the growth (processing) time, but does not affect the material quality as long as the criterion for N_G is met. It is recognized that the order of importance may vary based on the intended application and desired materials properties, however.

Additionally, by setting $h = w$, we see that

$$N_G \sim h^2 * \arcsin \frac{h^2}{4d^2 + h^2} \qquad (5.3)$$

In order to obtain smaller N_G, we can increase d or decrease h. Increasing d slowly asymptotes the arcsin term to 0, while decreasing h quickly decreases the h^2 term and also decreases the arcsin term to 0. This is due to the fact that the value of h affects the number of grains that form on the a-Si as well as the degree of confinement, while the value of d solely affects the degree of confinement. Thus, decreasing h causes the Ω_c term to approach 0 much more quickly than increasing d by an equal amount, so decreasing the channel height and/or width is a more effective method of obtaining small values of N_G for a given dimension change, and it also adheres to the fact that we want to keep d small in order to minimize processing time.

Following some of these guidelines can cause adherence to others to become impossible, however. For example, setting $N_G = 2.0$ and $w = h$ determines d such that property #3 is no longer freely determined. While it is clear that there exist situations in which the above three guidelines may not all be applicable, it is also extremely likely that there exist situations (e.g. lithographic limitations) in which adherence to all three guidelines is not possible, such that a subset of the three must be chosen to optimize the growth under the given constraints.
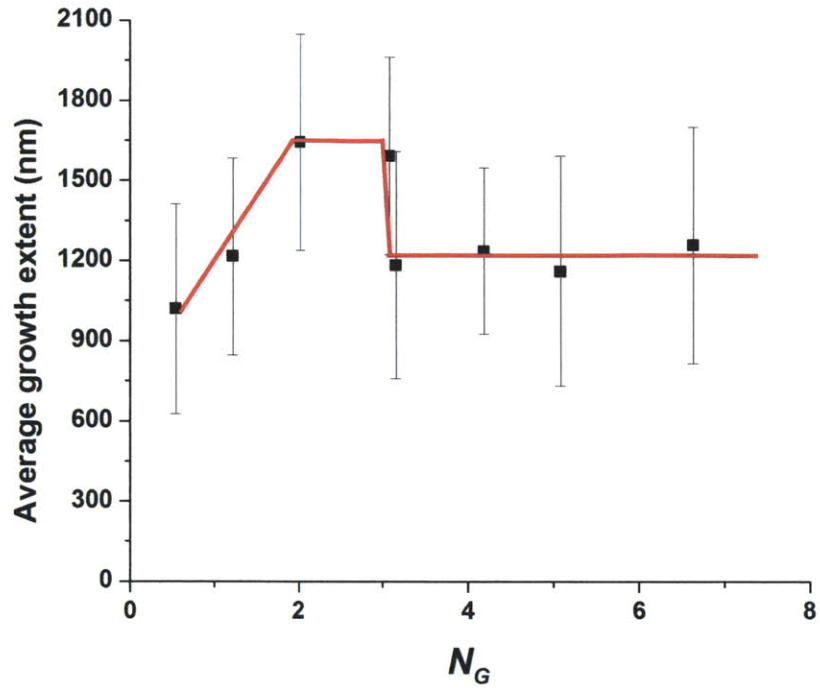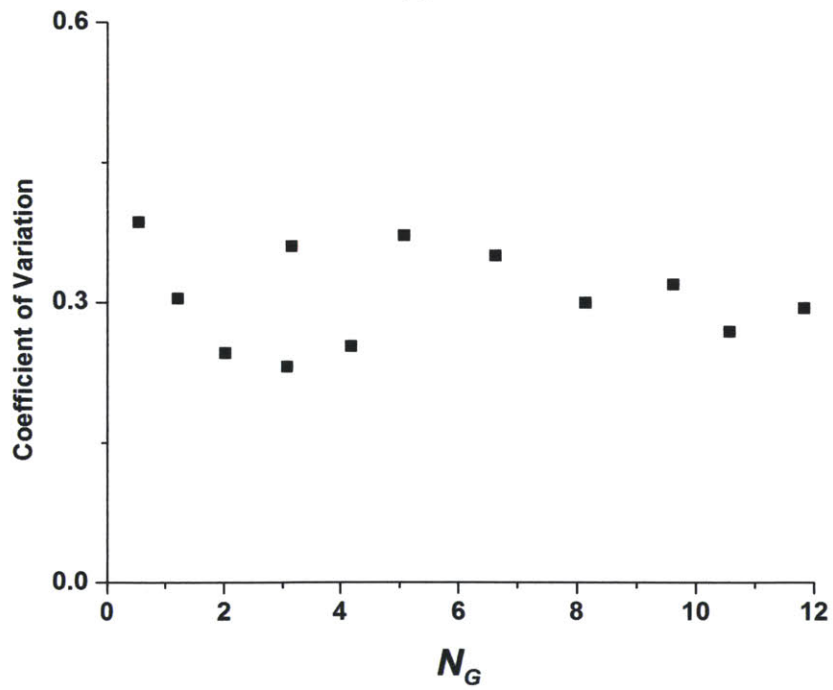
Figure 5.13. (a) Growth extent versus N_G and (b) growth extent coefficient of variation versus N_G (where error bars are ± one standard deviation). Red lines are added to guide the eye.

Recall that the model was derived assuming random nuclei orientations, but that we calculated in Chapter 3 that the nuclei likely have a slight preference for (110) orientations. This finding would modify the model slightly in that the solid angle given by Ω_n would no longer have a uniform probability distribution, but would instead have a distribution weighted toward its center. We would thus expect (110)-oriented grains to emerge from channels with smaller values of N_G than predicted in the current model, and this is indeed the case. If it were possible to calculate this probability distribution, we may be able to adjust the model to even more accurately reflect reality. The current form of the model, however, is simple and accurate and allows us to define design criteria for the optimum channel. Thus, any modification of the model to account for the slight predicted preferential nucleation orientation is unnecessary.

5.3.4 In-channel growth

In order to more accurately observe the final morphologies of the 2D GCLG growths in the channels (before emergence), we used reactive ion etching to remove the top oxide after Ge deposition on a number of samples. We were able to directly observe results like those in Figure 5.14, in which is seen an array of 2D GCLG growths. It is obvious that some growths emerge from the channels and continue growing in free space, while other growths terminate in the channel well before emergence. As discussed in the development of our 2D GCLG growth model, we attribute this self-termination to a misorientation between the channel's lengthwise direction and the <110> principal growth direction of the Ge crystal in the channel. Notice, as well, the highly slanted but very straight nature of the self-terminated growth fronts. This indicates that the growth fronts are faceted, as would be expected, but that the single crystals that were selected in

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the channels did not have their growth directions (the <110>) oriented along the lengths of the channels. Thus, they self-terminated by impinging on the channel sidewalls.
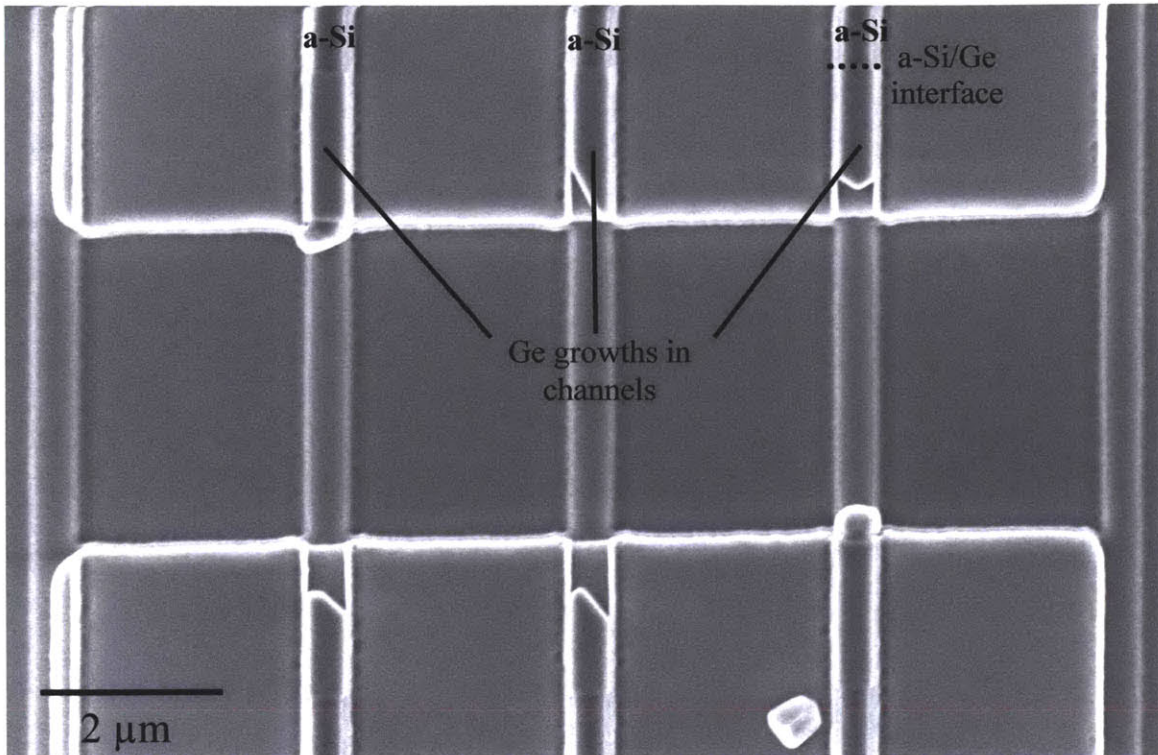
Figure 5.14. Ge growths in 2D GCLG channels, where the top oxide has been removed. The growths that have self-terminated in the channels show faceting, indicating that they are monocrystalline but not of the appropriate orientation for emergence from the channels.

5.3.5   Photoluminescence results

As described in Chapter 4, the photoluminescence (PL) intensity from a material increases as its trap density decreases. This is due to the fact that traps serve as sources for non-radiative recombination, which competes with radiative recombination but is not registered in PL measurements. As material defects are sources of traps, an increase in the PL intensity correlates to a decrease in the material's defect density.

In Figure 5.15 are presented PL spectra for three samples, where one is an as-deposited (unconfined) poly-Ge film, one is a 1D GCLG line of Ge, and one is an array

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of growths from 2D GCLG channels. All samples were deposited at 450° C for 16 hours, and the 1D GCLG sample had an aspect ratio of 6.7 while the 2D GCLG channels had N_G = 3.2. The 1D GCLG sample was not a coalesced film, but was instead two lines of 1D Ge GCLG. Thus, the amount of material subjected to the PL measurement in the cases of the 1D GCLG and 2D GCLG material is much less than that in the as-deposited growth, as neither the 1D GCLG material nor the 2D GCLG material formed a continuous film across the area of observation. Still, the PL spectra from both 1D and 2D GCLG have greater intensity, and thus lower defect density, than the as-deposited film's PL spectrum. Also, the amount of material under observation in the 2D GCLG case was undoubtedly less than that being observed for the 1D GCLG, so any volumetric normalization would further enhance the observation of improvement from 1D to 2D GCLG. Furthermore, as mentioned in Chapter 4, the PL measurement probes the material inside the channel as well as outside, so it is likely the PL intensity of the material grown from confinement would be higher than what is observed if it were possible to probe only the material outside the channel. The 2D GCLG also shows a peak shift to shorter wavelengths, indicating that it is more similar to single-crystal Ge, which shows more PL from its direct band gap at 1550 nm than does poly-Ge.
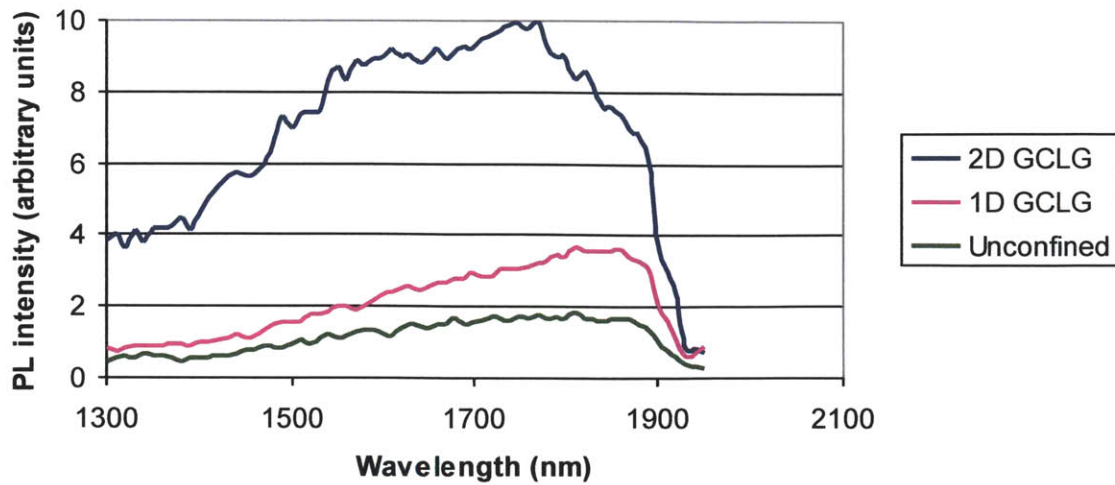
Figure 5.15. PL spectra from unconfined, 1D GCLG, and 2D GCLG of Ge. For the 1D sample, the aspect ratio was 6.7, and for the 2D GCLG sample, $N_G = 3.2$. The spectra have not been normalized for sample thickness because the two confined growths did not form continuous films.

Further growths with coalesced, continuous films consisting of 2D GCLG material would allow intensity normalization to the material thickness and thus a more accurate interpretation of the trap density decrease by 2D confinement.

5.4   Further channel geometry variations

While the 2D GCLG structure does successfully filter out many grain boundaries, some grain boundaries may persist (for example, if multiple (110)-oriented grains emerge from the channel simultaneously). In an attempt to further reduce the boundary density of our 2D GCLG growths, we coupled the concept of grain selection by geometric confinement with that of grain size enhancement by lateral overgrowth (LO, as discussed in Chapter 3). In this scheme, the growing Ge would be confined as in 2D GCLG but would also have to turn a corner or pass an obstacle before emerging from confinement. A schematic of one such growth structure is shown in Figure 5.16.

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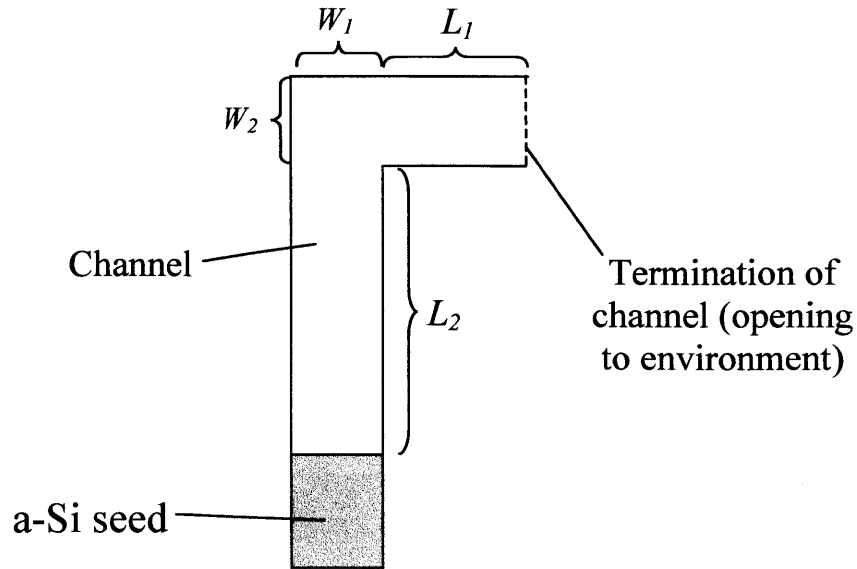
Figure 5.16. Plan view schematic of a revised 2D GCLG structure, which includes the turning of a corner before emerging from confinement.

Recall from Chapter 3 that the turning of a corner can increase the grain size of a polycrystalline material, as only the grains closest to the corner serve as the templates off which the grains may continue to grow around the corner. This reduces the number of potential grains after the corner has been turned. Therefore, if the channel contains multiple grains arranged in such a way that a subset of the channel grains are closer to the corner than the others (as would likely be the case), those closer would serve as the templates for further growth around the corner and the grain size would be further increased.

In order to fabricate such structures, a mask was made with two different types of channels. The first is a pattern like that seen in Figure 5.16, in which the growing Ge has to turn a corner before emerging from confinement. The second is a zigzag pattern like that seen in Figure 5.17, in which the growing Ge has to pass an obstacle introduced in the channel. The reason to use such a zigzag structure lies primarily in the concept that, if the channel is selecting a preferred growth direction, changing the growth direction to

one that is at a 90° angle to the preferred direction by bending the channel (as with the structure in Figure 5.16) may terminate the growth altogether. Thus, allowing the growth to continue in its preferred direction but obstructing it with an obstacle could eliminate all grains that are incapable of bypassing the obstacle, thus further enhancing the overall grain size.

The bent and zigzag channel geometries were fabricated with many variations in the channel width and lengths. For the bent geometry, the L_i were varied between 0 and approximately 2.5 μm across a single wafer. In the zigzag geometry, the H_i varied from 0 to approximately 2.0 μm across a single wafer, and Z was kept at 0.5 μm. However, as the TMAH etch of the a-Si could only be applied once to the entire wafer, all samples had approximately the same overall channel length after the TMAH etch (so the sums $L_1 + L_2$ and $H_1 + H_2 + H_3$ were constant on a given wafer). For this reason, only a few channels of the bent and zigzag geometries had the desired forms after fabrication; others had values of the individual L_i and H_i that were too small or too large to take advantage of the effects of the bend or zigzag.
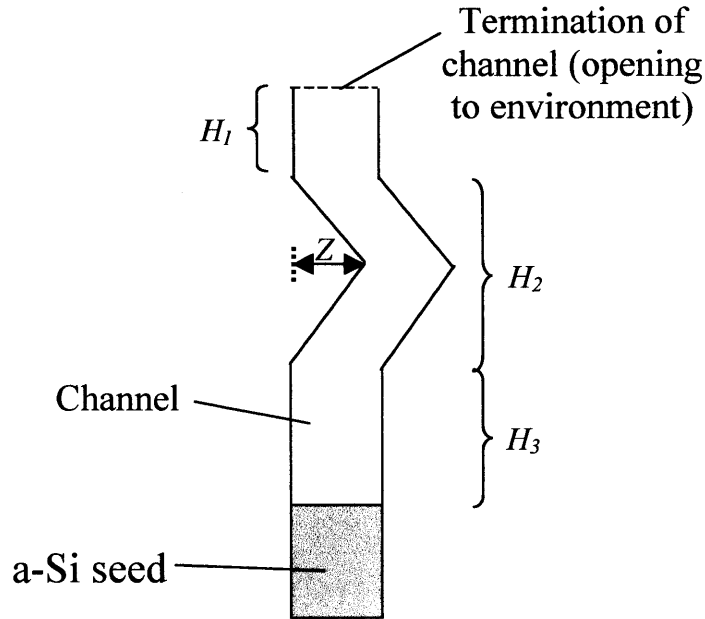
Figure 5.17. Plan view schematic of a channel zigzag pattern used to further select grains for extended growth.

Images of representative growths from the successfully-fabricated bent and zigzag channel geometries can be seen in Figure 5.18. These images have been taken with the SEM's electron beam at a voltage high enough to allow the electrons to penetrate the top oxide, so that the Ge growth in the channel is visible in the image. From the images of growths in the bent channels, we see that the surface at which the Ge nucleates (the a-Si seed surface in the channel) is curved. This is due to the isotropic etching nature of the TMAH. As the TMAH etches the leg of the channel exposed to the environment (defined by length L_1 in Figure 5.16), it etches uniformly across the cross-section of the channel. However, when the channel bends, the TMAH also starts to etch around the corner, such that the a-Si in the second leg (that defined by L_2) closest to the corner begins to etch before the TMAH etches the first leg completely. This phenomenon is depicted in Figure 5.19. It is not expected that the a-Si seed plane's angular offset with respect to the channel axis affects the growth.

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EBSD performed on ten growths from bent channels and ten growths from channels with zigzags showed that all growths contain $\Sigma3$ (twin) boundaries. Based on our previous discussion of twin-mediated growth, it was expected that twinning should be observed in the crystals, as we hypothesized that our confined crystals grow by Ge adatom adsorption at the intersections of twins with the crystal surface. However, this finding adds a new dimension to the situation, as twins we observe in the emerging crystals grown from bent/zigzagged channels could not have propagated from the a-Si seed due to the obstacles at the channel bends and zigzags. This confirms that the twins are indeed strongly preferred for the growth of our crystals; if they were not, the twins would terminate at the corner or zigzag and the growth could continue twin-free. It also shows that the twins will form in the crystals *after* nucleation, and the resulting crystals likely grow at a rate mediated by the adsorption of Ge atoms to the crystal at the twins.
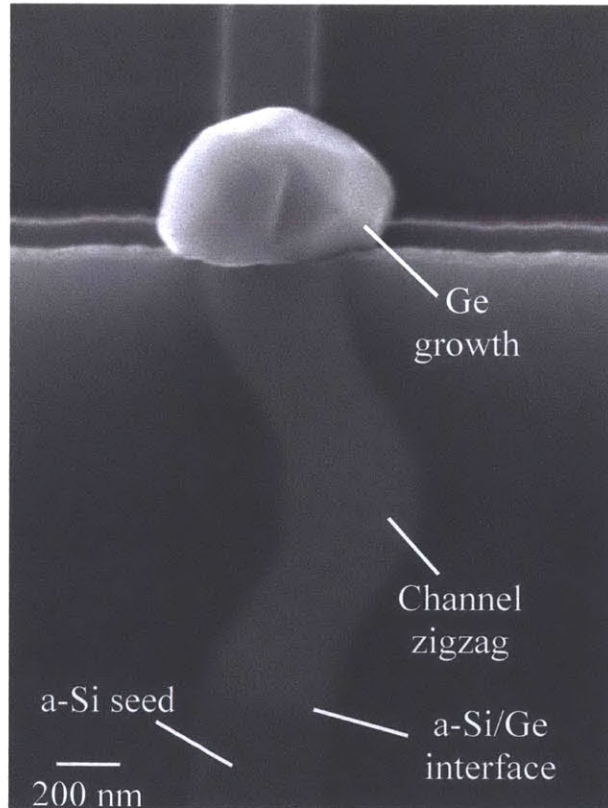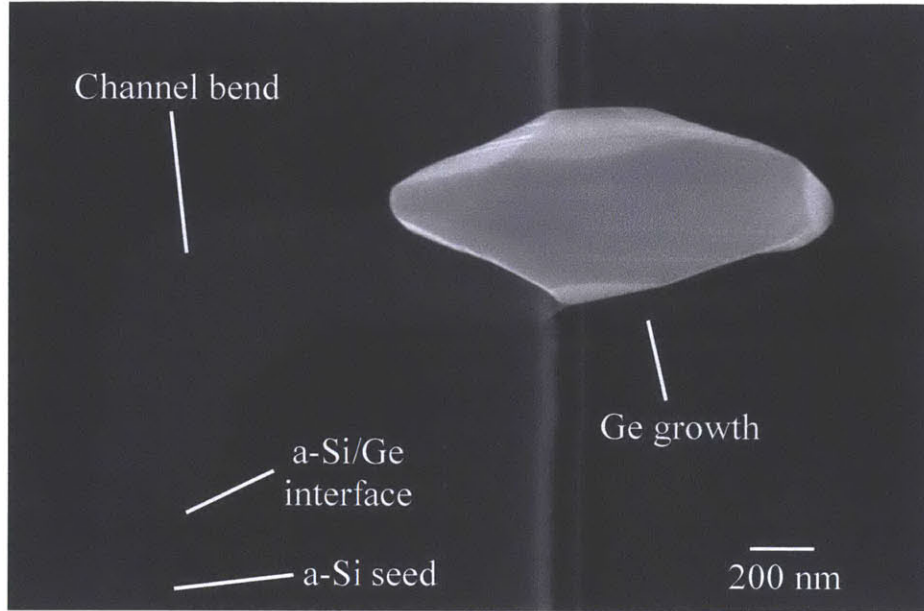
Figure 5.18. Representative crystals grown from 2D GCLG channels with bends or zigzags. The Ge can be seen in the channel, due to the SEM's high operating voltage.
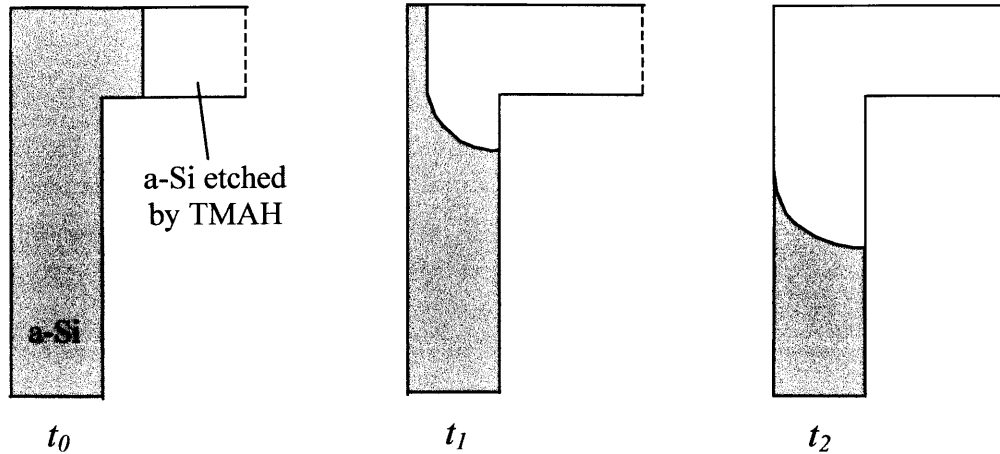
Figure 5.19. Schematics of TMAH isotropic a-Si etch in a bent channel. Schematics shown are for times $t_0 < t_1 < t_2$ after the start of the TMAH etch.

5.5 Chapter summary

This chapter presented the most advanced achievements of Ge crystal growth confinement in the current work, with the observation of single-crystal Ge growths from 2D GCLG channels. Though some crystals had no grain boundaries, all did possess twin boundaries on {111} planes, and these twins serve as attachment sites for Ge atoms on the growing crystal. PL measurements demonstrated that the material grown from 2D GCLG has a lower trap density than that grown from 1D GCLG. A model was constructed to determine the optimal channel geometries for single-crystal, large, uniform, consistently-emerging growths in 2D GCLG. By adding bends and zigzags to the 2D GCLG channel geometry, it was shown that twins are both strongly preferred for growth and capable of being formed after crystal nucleation.

Chapter 6: Summary and future work

6.1 Summary

This thesis details a method for the formation of single-crystal germanium on amorphous silicon, fabricated by ultra-high vacuum chemical vapor deposition utilizing temperatures under 450° C. In Chapter 1 we discussed the motivation for the work, introducing the concept of 3D-integrated electronics and photonics, and the need for a method of monolithically fabricating active photonic devices in the back-end microprocessor planes. In Chapter 2, we discussed the deposition of polycrystalline thin Ge films, the advantages and disadvantages of utilizing these films in practice, and work that has been done to improve such films' performance in device fabrication.

Chapter 3 covered our system for growth of poly-Ge films on a-Si by UHVCVD. We detailed several fabrication challenges in obtaining poly-Ge films, as well as the solutions to those issues. It was found that a dip in RCA post-SC2 $HF:H_2O$ 1:50 solution must be performed to obtain poly-Ge growth on a-Si without voids, though this dip can be as short as 5 seconds. We found that the a-Si film should be no thicker than approximately 120 nm in order to avoid bubbling of the a-Si and SiO_2 layers from H outgassing in the UHVCVD chamber at 450° C. Poly-Ge depositions at 350° C, 450° C, and 550° C were investigated, showing that the growths all have (110) texturing but that the growth at 450° C possesses the strongest such texture. Texturing is formed primarily during growth, though nuclei do show a slight preference toward (110) orientation. We detailed the successful *in situ* n-type low-temperature doping experiments on poly-Ge, as well as the results of lateral overgrowth of poly-Ge.

Chapter 4 introduced the concept of 1D-confined lateral growth of Ge on a-Si. The fabrication of a 1D confinement structure, consisting of two SiO_2 confining layers and one a-Si seed layer forming a confining channel, was described and the results of Ge growth on such a structure were presented. We found that the channel indeed reduced the Ge material's defect density and increased the material's grain size, and the channel was found to have an effect on the texture of the Ge. The material grown from 1D confinement exhibited a lower carrier density than as-deposited poly-Ge, attributed to a lower density of grain boundaries. PL measurements showed an increased intensity for the 1D-confined films compared to as-deposited films, further indicating improved material quality with confinement.

In Chapter 5, we presented the successful fabrication of single crystals of Ge on a-Si. We introduced the concept of 2D confinement and detailed the 2D confining structure's fabrication. We showed that the crystals grown from 2D confinement grew by surface atom adsorption at twin boundaries on the {111} planes of the Ge crystal, and that the presence of twin boundaries was strongly preferred for long-range crystal growth. Twins can be formed during growth and they enhance the growth rate. A model was developed to predict the channel geometry that will give the fewest grain boundaries, largest and most uniform growths, and the greatest probability of emergence from all channels. We also presented PL data showing that the 2D-confined growths had even more efficient radiative recombination than the 1D-confined growths, meaning the 2D-confined growths had better material quality than any other material in this study.

This method of single crystal formation on an amorphous substrate is applicable to any materials system that allows for selective non-epitaxial materials deposition.

6.2   Future work

There remain many items to study in the system used for this work. The most pertinent topic for investigation is the fabrication of devices from the 2D-confined material. While the crystal quality of the growths is high, the small sizes of the growths make fabrication of devices challenging. The unique structure of the confinement channel also presents a hurdle for successfully doping the material to make p-i-n devices. A method of filling a defined volume with single crystals grown from 2D confinement and successfully electrically contacting the material is of paramount importance.

For the successful fabrication of devices from Ge grown from confinement, it would also be useful to understand the strain state of the material and origins of any strain. Strain in Ge has previously been used in work on Ge photoconductors, modulators, and lasers [4, 6-9, 68] to engineer the material's band gap and may prove useful in the design of devices from 2D GCLG material as well. However, the modeling of a strained layer in a BEOL process would need to account for the effects of all the underlying layers, which may prove impossible in reality.

While grain boundaries have been targeted as the principal culprits in the performance deterioration of devices made from poly-Ge, an investigation of the dislocation density in GCLG material and its correlation to materials properties would help complete the picture of the defect evolution in material grown from confinement.

Finally, some parameters and materials used in making the confinement structures should be investigated. For example, the TMAH etch rate variability mentioned in Chapter 4 does not permit the definite specification of channel length; this issue should be resolved. The oxide used as a confining layer could be substituted with a low-k

dielectric to mimic the likely environment in a microprocessor stack. Deposition of Ge on other seed materials (e.g. Si_3N_4) may also be attempted, as the flexibility in seed layer could prove useful in BEOL integration. The growth rate of the germanium crystals in the channels may also be increased by, for example, using digermane (Ge_2H_6) as the precursor gas. Furthermore, additional growths and measurements could be performed in order to determine the exact shapes of the various plots of materials characteristics versus N_G.

While there is still a significant amount of effort required to bring devices made from confined Ge to reality, this thesis lays the groundwork for CMOS-compatible BEOL photonic device fabrication. Such material helps enable the continuation of Moore's Law, with the eventual integration of photonics and electronics on a microprocessor chip.

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