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# High-Performance Integrated Dual-Gate AlGaIn/GaN Enhancement-Mode Transistor

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**Abstract**—In this letter, we present a new AlGaIn/GaN enhancement-mode (E-mode) transistor based on a dual-gate structure. The dual gate allows the transistor to combine an E-mode behavior with low on-resistance and very high breakdown voltage. The device utilizes an integrated gate structure with a short gate controlling the threshold voltage and a long gate supporting the high-voltage drop from the drain. Using this new dual-gate technology, AlGaIn/GaN E-mode transistors grown on a Si substrate have demonstrated a high threshold voltage of 2.9 V with a maximum drain current of 434 mA/mm and a specific on-resistance of  $4.3 \text{ m}\Omega \cdot \text{cm}^2$  at a breakdown voltage of 643 V.

**Index Terms**—AlGaIn/GaN, dual-gate, enhancement-mode (E-mode), high-electron-mobility transistor (HEMT), power electronics.

## I. INTRODUCTION

AlGaIn/GaN high-electron-mobility transistors (HEMTs) have attracted a great interest for power electronics applications. A standard AlGaIn/GaN HEMT is a depletion-mode (D-mode) device due to the large 2-D electron gas induced by the polarization charge at the AlGaIn/GaN interface [1]. However, enhancement-mode (E-mode) AlGaIn/GaN HEMTs are highly desirable for power electronics as they can greatly simplify circuit designs and improve system reliability.

Several approaches have been reported in the past for fabricating normally-off GaN transistors, including gate recess [2], fluorine/hydrogen plasma treatment [3]–[5], p-type gate injection [6], engineering the surface potential with dielectrics [7], [8], dipole engineering [9], [10], and GaN MOSFETs [11]–[14]. However, it is difficult to use these methods to fabricate devices that simultaneously have large threshold voltage, low on-resistance, and high breakdown voltage. In this letter, we report the use of a new integrated dual-gate technology on a standard AlGaIn/GaN D-mode HEMT structure that allows the fabrication of state-of-the-art AlGaIn/GaN E-mode power transistors with high threshold voltage ( $> 2.8 \text{ V}$ ), high drain current ( $> 400 \text{ mA/mm}$ ), and high breakdown voltage (643 V).

The concept of the dual-gate technology is based on the circuit topology shown in Fig. 1(a). High-performance E-mode

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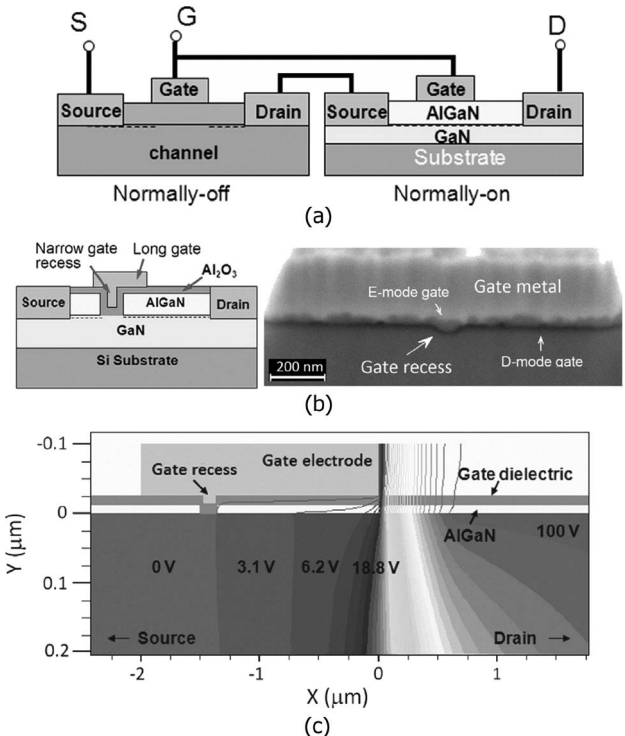


Fig. 1. (a) Normally-off operation by connecting an AlGaIn/GaN D-mode transistor with a normally-off transistor. (b) Schematic of the proposed integrated dual-gate E-mode device and its SEM cross-sectional image. (c) ATLAS simulation of the potential distribution in the integrated dual-gate normally-off transistor with  $V_{gs} = 0 \text{ V}$  and  $V_{ds} = 100 \text{ V}$ .

operation can be achieved by connecting a high-voltage D-mode AlGaIn/GaN HEMT with a low-voltage short-gate E-mode device, which can be a Si MOSFET or an E-mode GaN-based transistor. This circuit topology can be integrated into a single device on an AlGaIn/GaN structure—the integrated dual-gate transistor—as shown in the device schematic in Fig. 1(b), where the E-mode gate is implemented by gate recess. Although two separated gate fingers can be used, the integrated dual-gate structure gives the smallest form factor when the two gates are biased at the same voltage.

When the device is in the pinchoff, the channel underneath the D-mode gate will be depleted, and the short E-mode gate will be shielded from the large drain voltage. Only a voltage that is equal to the threshold voltage of the D-mode gate ( $|V_{th}|$ ) is dropped across the E-mode short gate, as shown by the simulation of the potential distribution in the device performed with the device simulator Silvaco ATLAS [Fig. 1(c)]. Different from the conventional gate-recessed E-mode AlGaIn/GaN transistors in [12]–[14], the integrated dual-gate structure needs to

be carefully designed so that the following will be achieved: 1) the gate length of the E-mode gate [shown in the SEM image in Fig. 1(b)] should be as short as possible to reduce its impact on the device total on-resistance; 2) the D-mode gate needs to be long enough ( $\sim 1 \mu\text{m}$  in our devices) to support the high drain voltage; and 3) the pinchoff voltage of the D-mode gate should not exceed the drain punchthrough voltage of the E-mode gate, which requires the D-mode gate to be as close to the channel as possible.

## II. DEVICE FABRICATION

The devices used in this letter were fabricated on an Al-GaN/GaN heterostructure grown on a 4-in Si (111) substrate by Nitronex Corporation. The structure has an  $\sim 1.8\text{-}\mu\text{m}$  undoped GaN/AlGaN buffer and a 17-nm  $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$  barrier. Ti/Al/Ni/Au alloyed source and drain ohmic contacts were formed by rapid thermal annealing (RTA). Mesa isolation was achieved by  $\text{BCl}_3/\text{Cl}_2$  plasma etching. Then, the short E-mode gate ( $L_g = 95 \pm 10 \text{ nm}$ ) was patterned with electron beam lithography, and the AlGaN barrier was fully recessed with low-damage  $\text{BCl}_3/\text{Cl}_2$  plasma etching. A 14-nm  $\text{Al}_2\text{O}_3$  gate dielectric was then deposited by atomic layer deposition, followed by 90-s RTA at  $700^\circ\text{C}$ . Finally, a  $2\text{-}\mu\text{m}$ -long Ni/Au/Ni gate electrode was deposited, overlapping with the first gate-recess region. The  $2\text{-}\mu\text{m}$  gate was shifted  $\sim 1 \mu\text{m}$  toward the drain side forming the D-mode gate in the integrated dual-gate structure, as shown in the SEM image in Fig. 1(b). The gate was annealed at  $500^\circ\text{C}$  for 3 min. Standard D-mode transistors were also fabricated at the same time as a reference on the same sample without the gate recess. The breakdown voltage was measured using a Tektronix curve tracer connected to Agilent 34401A multimeters. The breakdown voltage is defined as the voltage when the leakage current reaches  $1 \text{ mA/mm}$ .

## III. EXPERIMENTAL RESULTS

The dc characteristics of a normally-off integrated dual-gate device with  $L_{\text{gd}} = 5 \mu\text{m}$  are shown in Fig. 2. The maximum forward gate bias voltage ( $V_{\text{gs}}$ ) of the fabricated devices is  $7 \text{ V}$ , beyond which the gate dielectric breaks. The maximum drain current at  $V_{\text{gs}} = 7 \text{ V}$  of the E-mode dual-gate device is  $434 \text{ mA/mm}$  [Fig. 2(a)]. The transfer characteristics of the E- and D-mode devices are shown in Fig. 2(b). The E-mode device has a threshold voltage of  $2.9 \text{ V}$ , while the D-mode device has a threshold voltage of  $-3.5 \text{ V}$ , which is also the pinchoff voltage of the D-mode gate in the integrated dual-gate device. Measurements from five E-mode devices on the sample give an average threshold voltage of  $2.9 \text{ V}$  with a standard deviation  $\sigma$  of  $0.10 \text{ V}$ , which is comparable to the one in D-mode devices ( $\sigma = 0.13 \text{ V}$ ). The integrated dual-gate E-mode and standard D-mode transistors reach maximum transconductances ( $g_m$ 's) of  $143$  and  $134 \text{ mS/mm}$ , respectively, which are limited by the access resistance.

The  $I_d$ - $V_{\text{ds}}$  curves in Fig. 2(a) show two knee voltages that are a unique characteristic of the dual-gate devices. The first knee voltage is at  $V_{\text{ds}} = V_{\text{gs}} - V_{\text{th,E-mode}}$ , where  $V_{\text{th,E-mode}} = 2.9 \text{ V}$ , the E-mode gate threshold voltage. The second knee voltage is at  $V_{\text{ds}} = V_{\text{gs}} - V_{\text{th,D-mode}}$ , where

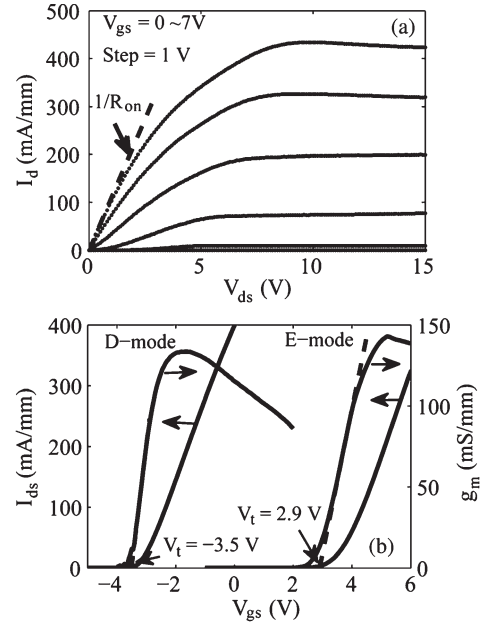


Fig. 2. (a)  $I_d$ - $V_{\text{ds}}$  characteristics of an integrated dual-gate E-mode device with  $L_{\text{gd}} = 5 \mu\text{m}$ . (b) Transfer characteristics of the E-mode device compared to a D-mode device of the same structure without gate recess. The E-mode device is biased at  $V_{\text{ds}} = 12 \text{ V}$ , while the D-mode device is biased at  $V_{\text{ds}} = 10 \text{ V}$ .

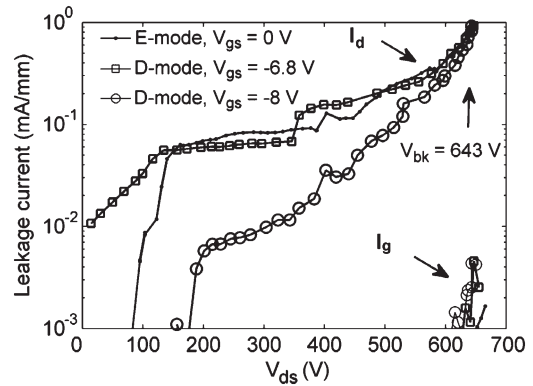


Fig. 3. Three-terminal breakdown measurement of an E-mode device at  $V_{\text{gs}} = 0 \text{ V}$  and a D-mode device at  $V_{\text{gs}} = -8$  and  $-6.8 \text{ V}$ . Both devices have  $L_{\text{gd}} = 18 \mu\text{m}$ . The resolution in the measurement setup is  $1 \mu\text{A/mm}$ .

$V_{\text{th,D-mode}} = -3.5 \text{ V}$ , the D-mode gate threshold voltage. The output conductance between the two knee voltages is due to the short-channel effect of the  $95\text{-nm}$  E-mode gate.

A maximum  $643\text{-V}$  three-terminal breakdown voltage is achieved on a dual-gate E-mode device at  $V_{\text{gs}} = 0 \text{ V}$  with  $L_{\text{gd}} = 18 \mu\text{m}$  (shown in Fig. 3). Its specific on-resistance ( $R_{\text{sp,on}}$ ) is extracted to be  $4.3 \text{ m}\Omega \cdot \text{cm}^2$ , with  $L_{\text{sd}} = 24 \mu\text{m}$  (including a  $2\text{-}\mu\text{m}$  transfer length from the source and drain contacts). A device with  $L_{\text{gd}} = 15 \mu\text{m}$  has a breakdown of  $567 \text{ V}$  and a  $R_{\text{sp,on}}$  of  $3.4 \text{ m}\Omega \cdot \text{cm}^2$ . The breakdown curves of a standard D-mode device with the same  $L_{\text{gd}}$  biased at  $V_{\text{gs}} = -8 \text{ V}$  and  $-6.8 \text{ V}$  are compared with that of the E-mode device in Fig. 3. Both E- and D-mode devices reach the same breakdown voltage at  $I_d = 1 \text{ mA/mm}$ , which is limited by the Si substrate. However, the E-mode device has higher drain leakage than the D-mode device biased at  $V_{\text{gs}} = -8 \text{ V}$ . A

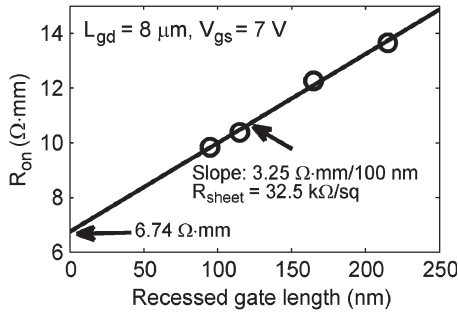


Fig. 4.  $R_{on}$  versus recessed gate lengths. The extrapolation to zero recessed gate length gives a resistance of  $6.74 \Omega \cdot \text{mm}$ , which is the  $R_{on}$  ( $6.76 \Omega \cdot \text{mm}$  at  $V_{gs} = 7 \text{ V}$ ) of a standard D-mode device of the same dimensions.

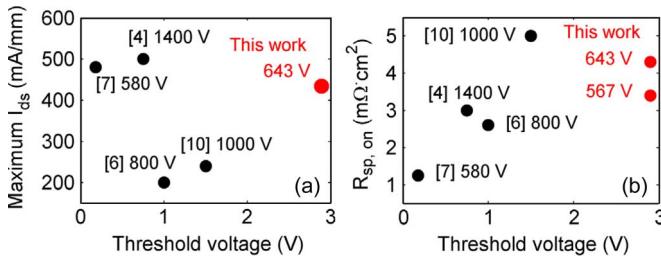


Fig. 5. Benchmark plot of (a) the maximum  $I_{ds}$  vs threshold voltages and (b)  $R_{sp,on}$  versus threshold voltages for published E-mode GaN transistors with a breakdown voltage over 500 V.

similar trend is also reported in [14]. The higher drain leakage associated with the E-mode device is due to its insufficient electron blocking barrier in the channel at the  $V_{gs} = 0\text{-V}$  pinchoff condition. Similarly, lowering the electron blocking barrier in the D-mode device by increasing the gate bias from  $-8$  to  $-6.8 \text{ V}$  increases its drain leakage as well (as shown in Fig. 3). Improving the electron confinement by using a back barrier in the AlGaIn/GaN structures would reduce the drain leakage of the E-mode transistor.

By varying the recessed gate lengths in the integrated dual-gate structure, the resistance from the gate-recessed region can be extracted from the on-resistance ( $R_{on}$ ) versus recessed-gate-length curve in Fig. 4, where the  $R_{on}$  of these devices is calculated from the  $I$ - $V$  characteristics at a gate bias of  $7 \text{ V}$ . The slope of the curve gives a sheet resistance of  $32.5 \text{ k}\Omega/\square$  in the recessed region. Therefore, the  $95\text{-nm}$  recessed gate region contributes only 17% of the total device resistance of the  $643\text{-V}$  E-mode device with  $L_{gd} = 18 \mu\text{m}$ . The dual-gate design allows the decoupling of the E-mode recessed region from the D-mode high-voltage region, which significantly improves the on-resistance and the maximum current of the devices, as shown in Fig. 5, where the combination of the maximum drain current,  $R_{sp,on}$ , and threshold voltage for several published E-mode GaN transistors with a breakdown voltage of over  $500 \text{ V}$  is benchmarked.

The relatively high sheet resistance of the recess region is due to the low electron mobility in that region. The electron mobility at the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface in the recessed region of the dual-gate E-mode transistors is  $16 \pm 2 \text{ cm}^2/\text{V} \cdot \text{s}$  (extracted from the  $g_m - V_g$  characteristics), while the extracted mobility for the D-mode device is  $1045 \pm 79 \text{ cm}^2/\text{V} \cdot \text{s}$ . The

device performance can be further improved by increasing the  $\text{Al}_2\text{O}_3/\text{GaN}$  interface mobility.

#### IV. SUMMARY

This letter has demonstrated the concept of an integrated dual-gate structure for E-mode GaN transistors where a short gate controls the threshold voltage and a longer gate supports the drain voltage drops. Using gate recess and  $\text{Al}_2\text{O}_3$  gate dielectric, the fabricated dual-gate E-mode AlGaIn/GaN on Si transistors show a threshold voltage of  $2.9 \text{ V}$ , a maximum drain current of  $434 \text{ mA/mm}$ , and a  $R_{sp,on}$  of  $4.3 \text{ m}\Omega \cdot \text{cm}^2$  with a breakdown voltage of  $643 \text{ V}$ . The proposed integrated dual-gate transistor is therefore a very promising approach to achieving high breakdown and threshold voltage with minimum impact on on-resistance. These three properties are important requirements for the use of GaN transistors in high-performance power electronics.

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