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A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS

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***Abstract*—Implementing efficient and cost-effective power regulation schemes for battery-powered mixed-signal SoCs is a key focus in integrated circuit design. This paper presents a fully-integrated switched-capacitor DC-DC converter in 45 nm digital CMOS technology. The proposed implementation uses digital capacitance modulation instead of traditional PFM and PWM control methods to maintain regulation against load current changes. This technique preserves constant frequency switching while also scaling switching and bottom-plate losses with changes in load current. Therefore, high efficiency can be achieved across different load current levels while maintaining a predictable switching noise behavior. The converter occupies only 0.16 mm², and operates from 1.8 V input. It delivers a programmable sub-1 V power supply with efficiency as high as 69% and load current between 100 μA and 8 mA. Measurement results confirm the theoretical basis of the proposed design.**

***Index Terms*—CMOS digital power supply, DC-DC conversion, digital capacitance modulation, LDO replacement, switched capacitor.**

I. Introduction

THE recent expansion in the use of electronic devices in every aspect of human life has fueled the demand for wider functional capabilities, multiple wireless/wire-line connectivity options, several digital/analog interface mechanisms, significantly higher digital processing horsepower, and larger than ever data storage capacities. Expanding digital processing functionality has driven the IC industry towards drastically scaling-down silicon fabrication technology to the nanometer levels along with reducing power supplies to sub-1 V. This scaling allows very dense digital implementations at minimum power consumption. On the other hand, in systems that require analog/RF capabilities in addition to extensive digital processing, expanding functionality has led to the evolution of mixed-signal Systems-on-Chip (SoCs). In these SoCs, analog, RF, and digital processing circuitries are all integrated into a single chip to form the full system in an attempt to maximize functionality at minimum power, cost, and footprint. However, the demand for diverse functionalities to be integrated in a single SoC creates a serious power management bottleneck. Particularly, the large number of independent, well-isolated, and uniquely-defined power supplies required by these diverse circuits is making the process of converting, regulating, and efficiently delivering power to the SoC from a single energy source (the battery) extremely challenging. In fact, in a typical mixed-signal SoC there could be as many as 30 isolated power supply domains for the analog/RF portions only.

There are fundamentally two methods for generating these independent power supply domains from the battery: switching regulators and linear regulators [1], [2]. Switching regulators are definitely superior for implementing highly-efficient power supplies, but in a SoC context, there are several factors that limit their use. Firstly, the large external passive components (inductors and capacitor) required by these types of regulators make using several of them in the SoC a cost/size prohibitive strategy. Secondly, these external passive components require multiple package pins to connect to the regulator's control circuitry, and hence using more than a few switching regulators is virtually impossible. Linear regulators on the other hand, while power-inefficient, are becoming very cost/size effective. First, they require only a single capacitor. This capacitor has traditionally been implemented using an external component, which is still much cheaper and smaller than an inductor. Second, research work both in academia and industry has demonstrated that even those capacitors can be minimized to levels that can be integrated on-chip [3]–[5]. Therefore, in addition to eliminating the cost/size of the external capacitor itself, as many linear regulators as needed in the SoC can be implemented without any package/PCB overhead.

In this paper, the advantages of both these regulation techniques are combined in a capacitor-based fully-integrated switching regulator in 45 nm standard CMOS technology. The proposed architecture uses 30 MHz switching frequency with on-chip poly-Nwell capacitors for both the charge-transfer and the load capacitors. The design uses a digital capacitance modulation control mechanism rather than traditional PFM and PWM control methods to maintain regulation against load current changes. This technique preserves constant frequency switching while also scaling switching and bottom-plate losses with changes in load current. Therefore, high efficiency is

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achieved across different load current levels while maintaining a predictable switching noise behavior. The proposed switching regulator was specifically designed to replace linear regulators used to power the mixed-signal modules inside a fully-integrated FM transceiver. However, it can also be used as a realistic cost-effective replacement for linear regulators in many other applications.

II. Power Domains in Wireless Systems

Fig. 1 shows a widely adopted power regulation scheme in modern mixed-signal SoCs. As shown, the scheme is based on using only two efficient high-current switching regulators operating directly from the Li-Ion battery to generate a single 1.8 V "analog" supply shared by all the mixed-signal modules in the SoC, and a single 1.2 V "digital" supply used by the digital processing unit of the SoC. These two regulators are the only switching regulators in the system interfacing with the battery, and are typically implemented in a separate chip using high-voltage technologies. This eliminates reliability issues associated with interfacing the low-voltage SoC directly with Li-Ion voltage levels. The SoC is then left with the task of generating all the necessary local power supplies needed by its mixed-signal modules (which can be as low as 0.9 V–1 V) out of the shared 1.8 V "analog" supply using an array of fully-integrated low-current linear regulators (loads typically between 5 mA–10 mA). With this strategy, the number of switching regulators and their associated external passives is minimized. It is worth mentioning that the choice of operating the array of linear regulators in Fig. 1 from the 1.8 V supply rather than the 1.2 V supply is driven by two main factors. The first factor is that the digital 1.2 V typically employs dynamic voltage scaling which is a function of the performance requirements of the DSP, as well as the process technology and temperature corners, in order to control both yield and power consumption. This dynamic voltage scaling result in a large variability in the digital supply that is not correlated to the performance requirements of the mixed signal modules. In fact, in 45 nm, the 1.2 V digital supply can be as low as 0.75 V in some conditions. At these same conditions many mixed signal modules could still require a 0.9 V–1 V supply levels, and thus the choice of the 1.8 V analog supply instead of the 1.2 V digital supply. The second factor is the fact that the digital supply contains a lot of unpredictable noise that is not easily suppressed using linear regulators with on-chip capacitors. This unpredictable noise is very difficult to account for in the design of the mixed-signal modules and can result in significant performance degradation.

The scheme in Fig. 1, while cost-effective, constitutes a major efficiency loss. This is due to the fact that many of the power supplies needed by the mixed-signal modules can be as low as 0.9 V. At this large difference between the input voltage (1.8 V) and the output voltage, linear regulators become very inefficient. Moreover, with each mixed-signal module consuming between 5 mA to 10 mA, and with the large number of linear regulators needed, the collective impact of this efficiency loss on the overall power consumption of the SoC becomes quite significant.

Additionally, the array of linear regulators used in Fig. 1 render any efforts spent in designing low-voltage analog circuits

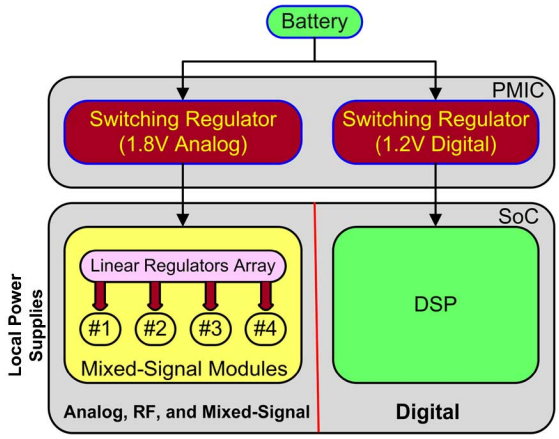

Fig. 1. Most commonly-used power regulation scheme in modern mixed-signal SoCs.

to enable lower power consumption through supply scaling practically ineffective. This is simply due to the fact that the total current consumption in analog circuits does not generally scale with power supply reduction, and therefore any power savings through power supply scaling gets wasted across the linear regulator. In digital loads, power savings are still achievable through power supply scaling even if linear regulators are used to generate the scaled power supply. Nevertheless, the savings achieved are significantly reduced.

For the previous reasons, the trend in industry is to attempt to replace the linear regulators in Fig. 1 by a more efficient switching alternative to fully leverage the power savings benefits of power supply scaling. However, any switching alternative must fulfill three requirements in order to make sense from a cost point of view. First, the regulator should not rely on any external passive components, i.e., must be fully integrated on the chip. Second, it must consume a silicon area that is as close as possible to an equivalent linear regulator. Third, the noise associated with the switching operation of the regulator must be fully predictable and invariant with load current in order to accurately account for it in the design of any noise-sensitive analog or digital circuits in the system. This applies to circuits powered by the regulator itself, or any other circuits powered by the global input power supply which can be contaminated by the switching behavior of the regulator. It is worth noting that due to the low-current nature of the load circuits this converter in targeting, changes in load current is limited to only few milliamps. Thus, the inherent switching noise of the converter itself dominates the overall switching noise at both the input and output sides of the converter rather than any load current steps caused by the action of the load circuits.

The first requirement can be fulfilled by implementing switching regulators with relatively high switching frequency. Higher switching frequency can linearly scale the size of the necessary passive components to very small levels. It was generally avoided due to high switching losses associated with older CMOS technologies, which significantly degraded the efficiency of the regulator. However, with advanced nanometer technologies, switching at very high frequencies with very little power overhead is becoming attainable. For example, previous

work in 90 nm has been reported where the passive components were reduced to small enough levels to be integrated on-package [6]. Further reduction in the passives for on-chip integration was also explored in 0.13 μm [7]. With CMOS technologies reaching the 45 nm level and beyond, further reduction in passive components through switching at higher frequencies without compromising efficiency is a very realistic goal.

The second requirement can be fulfilled by making the right choice between inductor and capacitor based switching regulators. Recent work has demonstrated fully-integrated inductor-based switching regulators [7]. However, the large area overhead of integrated inductors makes inductor-based solutions unattractive for linear regulators replacement. This area overhead can be reduced by allowing the inductor to operate in Discontinuous-Conduction-Mode. Nevertheless, achieving high efficiency would be extremely difficult. On the other hand, on-chip well-based capacitors enjoy much higher density than metal-based on-chip inductors. In fact, capacitor-based fully-integrated switching regulators have been introduced in older technologies (0.35 μm) with low switching frequency (1 MHz) [8]. However, the area occupied is prohibitively large. Nevertheless, in 45 nm technology, the switching frequency can be significantly increased to reduce the total area of capacitor-based solutions without compromising efficiency. Moreover, this area can be reduced even further if the load-current is low. Since each linear regulator in Fig. 1 has relatively low load-current demand (5 mA–10 mA), capacitor-based switching regulators offer an attractive and viable replacement to these linear regulators in SoC applications.

III. Switched Capacitor Charge Transfer

The sub-10 mA current requirements of many of the power domains lend themselves to the possibility of using switched capacitor DC-DC converters for replacing the linear regulators. By switching these converters at high frequencies, it is possible to reduce the area overhead over a linear regulator. To cater to load voltages between 0.8 V–1 V, the current implementation uses a 2BY3 gain setting [9] switched capacitor DC-DC converter which when switching at no-load provides a 1.2 V output from an input voltage of 1.8 V. Fig. 2 shows the 2BY3 gain setting implemented as a 2-way interleaved structure to reduce the input current and output voltage ripple. The converter employs a total charge-transfer capacitance of $64\mathrm{C_B}$ and the load capacitance is $\mathrm{C_L}$. The input voltage (V_{BAT}) to the system is 1.8 V.

A. Loss Mechanisms

Fig. 3 shows the charging and discharging of the charge-transfer capacitors during the two phases of the clock for one-bank of the interleaved structure. Assuming that this block is delivering charge to the load capacitor at a voltage V_L, the charge extracted from the battery during phase φ_1 can be given by

$$Q_{BAT} \approx 48C_B(1.2 - V_L). \tag{1}$$

This charge also flows into the load capacitor. Here, the switches are sized just enough to allow the capacitor voltage to settle close to its final value. During φ_2, the excess charge gained by the charge-transfer capacitors is transferred to the load by splitting the charge-transfer capacitor into two and connecting in series with the load. The total charge transferred to the load can be given by

$$Q_L = Q_{BAT} + Q_{\varphi 2} \approx 72C_B(1.2 - V_L). \tag{2}$$

It can be seen from (1) and (2) that for the G2BY3 gain setting, for every quantum of charge extracted from the battery during a cycle, $1.5\times$ that charge is delivered to the load. This puts a fundamental efficiency limitation of $V_L/1.2$ for this gain setting. The excess energy is lost as ohmic losses along the switches.

On top of this fundamental conduction loss, another significant loss factor is due to the bottom-plate parasitic capacitor shown in Fig. 3. The bottom-plate parasitic can be 5–10% of the actual capacitance for the poly-Nwell capacitors used in this implementation. This parasitic capacitor gets charged during φ_1 to the load voltage and a part of it gets discharged to ground while the other gets discharged to close to $0.5V_L$ during φ_2. As a result, the energy lost every cycle due to this bottom-plate parasitic can be given by

$$E_{BP} \approx 24\alpha_B V_L^2. \tag{3}$$

This combined with the energy lost in switching the charge-transfer switches every cycle and control losses associated with maintaining the output voltage at a regulated value bring the efficiency further down. For a more detailed explanation of these loss mechanisms and the equations associated with them, please refer to [10].

B. Regulation Techniques

The amount of charge delivered to the load every cycle by a single bank of the interleaved structure in Fig. 1 was given by (2). From this, the load current handling capability [9] of the

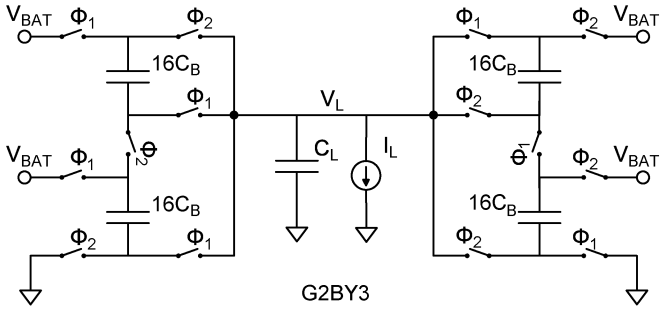

Fig. 2. A two-way interleaved G2BY3 gain setting to provide voltages below 2/3rd the input voltage (1.8 V).

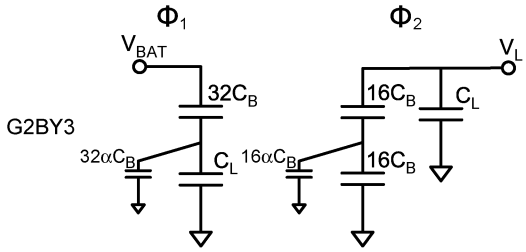

Fig. 3. Arrangement of the charge-transfer capacitors during phases φ_1 and φ_2 in the G2BY3 gain setting.

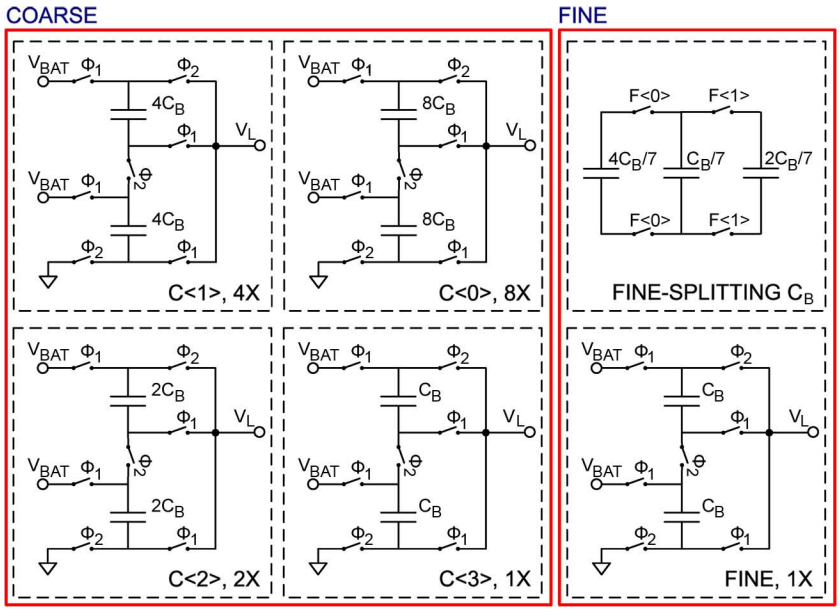

Fig. 4. Binary-weighted partitioning of the charge transfer capacitors and switches for digital capacitance modulation. $C\langle 0:3\rangle$ turns ON or OFF the coarse blocks. $F\langle 0:1\rangle$ controls the finer splitting of the $1C_B$ capacitor.

G2BY3 gain setting when switching at a frequency f_s can be given by

$$I_L = 2Q_L f_s \approx 144C_B(1.2 - V_L)f_s \tag{4}$$

where $64C_B$ is the total on-chip charge transfer capacitance used, Q_L is the charge delivered to the load every switching cycle by one bank of the interleaved structure and I_L is the current delivered at a load voltage of V_L. The goal of the DC-DC converter is to provide a regulated voltage supply at V_L when the output current changes. It can be observed from (4) that in order to regulate the output to a specified voltage V_L while delivering a load current I_L, the only available knobs are f_s or Q_L.

One popular technique for regulation is to change the switching frequency (f_s) of the converter with change in load current. Here, charge is delivered to the load only when needed depending on the load current. This is the traditional pulse frequency modulation (PFM) [9] based variable frequency control. While this is an inherently stable mode of control with low losses, the frequency of operation of the converter changes with the load current being delivered. Hence, the characteristics of the switching noise it introduces in the input and output vary with the current and cannot be controlled. While this method of control is useful in certain digital systems, wireless applications where the digital load being supplied co-exists with critical analog/RF blocks cannot handle uncontrolled tones that cover a wide frequency range. Hence, a fixed frequency control methodology is required.

For fixed frequency control, it can be seen from (4) that the charge delivered to the load every cycle has to be changed to maintain regulation. One of the popular constant frequency control methods is to use duty cycle control [8] to regulate the output voltage. In this scheme, the ON time of the switches of the switched capacitor DC-DC converter is varied as the load current changes. Another technique is to use segmented switch width [11] control to change the size of switches, as the load current varies. Both these methods effectively change the series resistance of the charge-transfer switches thereby changing the amount of charge delivered to the load every cycle (Q_L). However, since they switch at all cycles with the same amount of charge-transfer capacitance, the bottom-plate losses do not scale with change in load current. In the case of duty-cycle control, since the switch sizes do not change either, the switching losses also remain fixed with change in load current delivered. Both of these effects lead to a drop in efficiency at low loads. Also, since the switch resistance is the control parameter, effective regulation with a wide change in load current is difficult to achieve especially when taking process variations in nanometer CMOS processes into account.

IV. Digital Capacitance Modulation

To overcome the above-mentioned problems, a digital-capacitance-modulation (DCpM) mode of control [13] is introduced, where regulation is maintained by controlling the amount of capacitance that takes part in the charge transfer process. Since the amount of charge delivered per cycle is proportional to the charge-transfer capacitance engaged, Q_L can be changed with change in load current by varying the amount of capacitance being switched. The advantage with this scheme is that the width of the charge-transfer switches can be made to scale in size as the capacitance scales. This helps in scaling both the bottom-plate and switching losses with change in load current.

In the actual implementation of the switched capacitor converter with DCpM mode of control, the total charge-transfer capacitance is broken into binary weighted banks. Fig. 4 shows how the capacitors are partitioned for one tile of the interleaved structure. The charge transfer capacitance is broken into 5 different banks of sizes 8X, 4X, 2X, 1X and 1X,FINE. Of these banks the first 4 are coarse controlled and the final 1X bank is fine controlled.

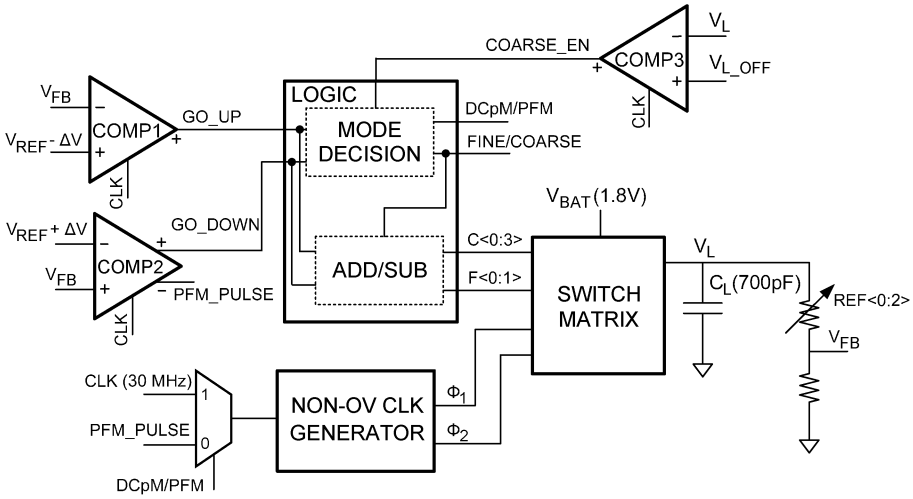

Fig. 5. Architecture of the switched capacitor DC-DC converter system.

The coarse split banks are controlled by the coarse mode signals $C\langle 0:3\rangle$. Each bank is enabled only when the corresponding coarse mode signal is high. As the size of the charge transfer capacitors change in each bank, so do the width of the switches, such that every bank has similar charge/discharge times. This way the switching and bottom-plate losses are incurred only when the respective bank is enabled, and their magnitude changes with the size of the bank. With coarse control, the charge transfer capacitance can be increased in steps of $1\mathrm{C_B}$.

The 1X,FINE bank remains always on. The charge-transfer capacitance in this bank is further subdivided into three capacitances of value $\mathrm{C_B}/7$, $2\mathrm{C_B}/7$ and $4\mathrm{C_B}/7$. While the $\mathrm{C_B}/7$ capacitance is always engaged, the other capacitances are engaged only when the fine mode signals $F\langle 0\rangle$ and $F\langle 1\rangle$ are high. By controlling the 4-bit COARSE signal and the 2-bit FINE signal, the converter adjusts the amount of capacitance taking part in the charge transfer process. The next section discusses how the COARSE and FINE signals are enabled to maintain regulation of the output voltage with change in load current.

V. Architecture

Fig. 5 shows the architecture of the switched capacitor DC-DC converter. The switch matrix contains the capacitor banks and the switches as shown in Fig. 4. The amount of capacitance involved in the charge transfer process is controlled using a 6-bit digital signal of which 4 bits (C<0:3>) are used for coarse control and the remaining 2 bits (F<0:1>) are used for fine control. The converter uses hysteretic mode of control and tries to maintain the feedback voltage V_{FB} within the hysteretic band $[V_{\mathrm{REF}} - \Delta V, V_{\mathrm{REF}} + \Delta V]$, where V_{REF} is a fixed reference voltage (0.53 V) and ΔV is set to 20 mV. The feedback voltage V_{FB} is obtained from the load voltage V_L using a resistive divider network which is digitally controlled by a 3-bit reference signal REF<0:2>. Using these 3 bits, the load voltage can be set to be between 0.8 V–1 V. This 3-bit signal controls the resistive ladder division ratio such that the load voltage that is desired is divided down to the reference voltage of 0.53 V.

The operation of the converter is controlled by the digital capacitance modulator which determines the mode of operation of the converter. The 2 clocked comparators COMP1 and COMP2 help maintain regulation of V_L by generating the *GO_DOWN* or *GO_UP* signals. COMP1 sends the *GO_UP* pulse when V_{FB} falls below the lower end of the hysteretic band. Similarly, COMP2 sends the *GO_DOWN* pulse when V_{FB} goes above the hysteretic band. These signals feed into the logic block where the MODE DECISION unit generates the *FINE/COARSE* and *DCpM/PFM* signals which determine the operating mode of the converter. Following this, the ADD/SUB block suitably modifies the C<0:3>, F<0:1> signal which controls the amount of charge-transfer capacitance engaged. Depending on whether the *GO_UP* or *GO_DOWN* signal goes high, the ADD/SUB block either increments or decrements the amount of capacitance engaged in charge transfer by enabling or disabling the capacitor banks. A third comparator COMP3 is used to detect sudden changes in load voltage. When the load voltage falls 100 mV below the reference voltage, this comparator triggers the *COARSE_EN* signal. This signal feeds into the logic block to transition the converter into coarse mode. The converter normally operates in the DCpM mode of operation but at very low output currents, it automatically transitions into a pulse frequency modulation (PFM) mode of control to maintain efficiency. The next section explains how the converter transitions between the different modes of operation.

VI. Control Modes

A. COARSE/FINE Mode of Control

For fast transient response, the converter employs COARSE regulation during startup and load transients. In this mode only the 4 coarse bits C<0:3> are changed, the 2 fine bits F<0:1> are set to '11', and the capacitor step size for regulation is $1C_B$. Once the transients have settled, to prevent limit cycling with COARSE regulation, the converter enters FINE regulation where the capacitor step-size is reduced to $2C_B/7$, as shown in

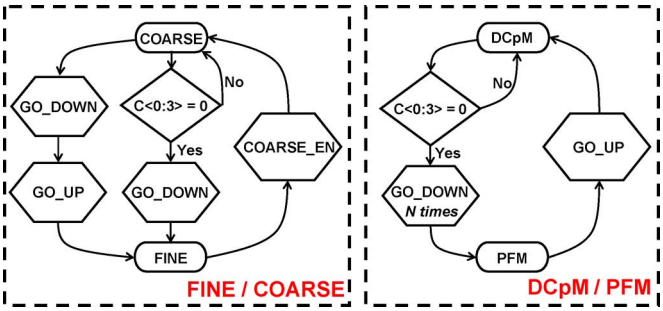

Fig. 6. Flowchart showing the events leading to transition between FINE/COARSE modes of regulation and DCpM/PFM modes of control. 'N' can be set to 4 or 8.

Fig. 4. This enables the converter to settle within narrow hysteretic bands without any unwanted low-frequency oscillations. Fig. 6 shows the events leading to the transition between the FINE and COARSE modes of control. The transition from the COARSE to FINE mode occurs when the output voltage transitions from falling to rising and this is detected by observing a *GO_DOWN* signal followed by a *GO_UP* signal. This can be seen in Fig. 7(a). The COARSE to FINE transition can also occur when all 4-coarse mode bits $C\langle 0:3\rangle$ are zero and a *GO_DOWN* signal occurs. This happens when the load current is too small as can be seen in Fig. 7(b). The transition from the FINE to COARSE mode occurs when the *COARSE_EN* signal output by COMP3 goes high. This happens during sudden load increases and helps the converter to settle fast while minimizing the droop in V_L. COMP3 compares V_L with a reference voltage V_{L_OFF} which is generated on-chip and is designed to be 100 mV lesser than the required V_L. The rising edge of the *COARSE_EN* signal also causes $C\langle 0\rangle$ to go high further reducing the settling time. During step-down transients in load current, since the converter uses a G2BY3 gain setting, the load voltage does not rise above 1.2 V, even in the worst case transition of maximum to zero load current. During such extreme step-down transients, the converter effectively shuts down letting the load current bring the load voltage down to within the hysteretic band. This happens as the converter transitions into PFM mode of operation as described in the next section.

B. DCpM/PFM Mode of Control

Constant frequency control through digital capacitance modulation (DCpM) effectively regulates the output voltage to within the specified hysteretic band. The FINE/COARSE modes of control help in achieving a fast transient response while at the same time maintaining a tight hysteretic band. However, since the switches corresponding to the capacitor banks which are enabled, are constantly being turned ON/OFF, the switching losses cannot be brought down below a certain point. The minimum amount of power lost due to switching depends on the switching frequency that the converter operates in, C_B and the lowest capacitance bank that the converter is allowed to operate in. If the load power becomes low enough, this constant switching power being lost begins to significantly affect the efficiency of the converter. Pulse Frequency Modulation (PFM) mode is used in this converter to prevent this big drop in efficiency. This is justified from a supply noise point of view because very low loads typically occur only in standby type of conditions where the load circuits are not required to operate with full performance. Thus, the unpredictable switching noise associated with PFM control can be tolerated.

In this implementation, at very light load conditions of less than 500 μA, the converter automatically switches to PFM mode control to maintain efficiency by making the *DCpM/PFM* signal go low. As shown by the flowchart in Fig. 6, the transition from DCpM to PFM occurs when the logic block encounters multiple *GO_DOWN* signals when the coarse bits are all zero. If the load current is too small, then the converter operating in constant frequency control with only the lowest allowed capacitor bank turned ON, will not be able to regulate the output voltage to within the hysteretic band. This can be seen from (4) where fixing the capacitance and frequency means V_L needs to increase as I_L decreases. This observation is utilized to switch to the PFM mode of operation. When a set of *GO_DOWN* signals occur with the capacitor bank at its lowest allowed state, the converter determines that the load power is too low for normal operation and switches to PFM mode. The logic block in Fig. 5 counts the number of *GO_DOWN* signals that occur when all 4 bits of $C\langle 0:3\rangle$ are zero. If this number exceeds a certain threshold, the logic block switches the converter mode to PFM.

In the PFM mode, the negative output signal of COMP2, *PFM_PULSE* is multiplexed in to act as the clock to the switch matrix. This helps to maintain the output close to the upper threshold of the hysteretic bank as shown in Fig. 7(b). With the above mentioned method, it is possible to implicitly detect the load current instead of actually measuring it as happens in many approaches to switch to PFM mode. Also, the threshold of the load current at which to switch to PFM mode can be easily set by changing the lowest allowed state of the capacitor bank. When the load current increases above the PFM threshold, the PFM mode is no longer capable of supplying the current and the voltage droops below the lower threshold of the hysteretic bank. This makes the *GO_UP* signal go high which is then used to return to the DCpM mode.

VII. Measurement Results

The switched capacitor DC-DC converter was implemented in a 45 nm digital CMOS process. Fig. 8 shows the die photo of the test chip. The total active area consumed by the switched capacitor DC-DC converter is only 0.16 mm^2. The bulk of this area is occupied by the charge-transfer and load capacitors. The total charge-transfer capacitance employed is 534 pF while the load capacitance was 700 pF. All the capacitors used are obtained using poly-Nwell capacitors, which had the highest density in the process used.

Fig. 9 shows measured waveforms of the load transient response. For these measurements, the converter was input a reference signal of '000' which corresponds to a load voltage of 1 V. The load current was transitioned from 270 μA to 7.6 mA. Fig. 9(a) shows the transient response when the COARSE_EN comparator COMP3 is enabled. When the load current is 270 μA, owing to its low value, the converter automatically operates in the FINE mode of control with PFM modulation and the output voltage is regulated to 1 V. When the load transition

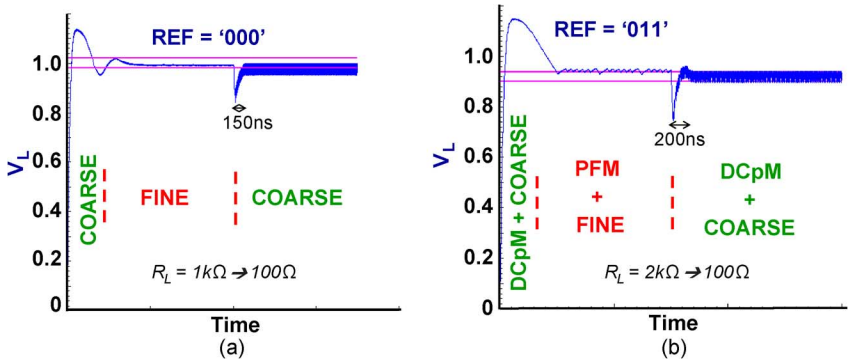

Fig. 7. Simulated load transient performance of the SC converter with (a) the reference voltage set to '000' (1 V) and (b) the reference voltage set to '011'.

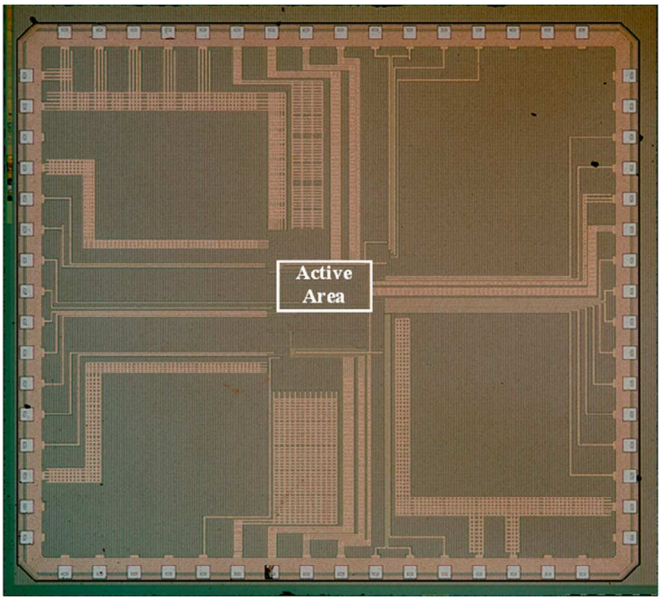

Fig. 8. Die photo of the switched capacitor DC-DC converter identifying the area consumed by the active blocks.

occurs, comparator COMP3 catches the droop in load voltage and makes the *COARSE_EN* signal go high. This feeds into the MODE DECISION unit which transitions the converter into COARSE mode of control with DCpM modulation. This enables the converter to settle within 120 ns when the converter is switching at a clock frequency of 30 MHz. The *COARSE_EN* signal also makes the MSB of the COARSE block $C\langle 0\rangle$ to go high immediately. This engages the largest capacitance available instantly thereby preventing the load voltage from drooping too low. The transient response shown in Fig. 9(b) is with the COARSE_EN comparator disabled. In this case, the transition to COARSE mode does not occur and it takes 1.2 μs for the converter to settle, with a more pronounced droop in V_L. The converter keeps the ripple voltage on the output to less than 50 mV in both DCpM and PFM modes of operation.

Fig. 10 shows measured waveforms of the transient response of the converter when the reference voltage is varied. For this measurement, the load resistance was fixed at 130 Ω ohms and the reference voltage ($REF\langle 0:2\rangle$) was changed from '100' to '000' and back. The converter operates in the DCpM mode throughout as the load current is higher than the PFM threshold. When the reference voltage is '100' the converter operates in FINE mode of control and delivers a load voltage of 0.8 V. When the reference voltage is transitioned to '000', the comparator COMP3 makes the *COARSE_EN* signal go high and the converter immediately switches to COARSE mode as can be seen by the transition of the *FINE/COARSE* signal. This helps the converter to settle to the new load voltage of 1 V within 2 μs. At 1 V, the converter continues to operate in the COARSE mode. When the reference voltage is brought back to '100', the converter takes 4 μs to settle back to 0.8 V output. As V_L is falling, it undershoots first before recovering. When the voltage begins to rise again after undershooting, the converter automatically transitions to FINE mode of control.

Fig. 11(a) shows the measured efficiency of the converter with change in V_L while delivering a load current of 5 mA. The converter provides above 60% efficiency over the load voltage range from 0.8 V to 1 V, which is much higher than LDO's and other completely on-chip switched capacitor DC-DC converters [12]. Table I shows a breakdown of the losses in the switched capacitor DC-DC converter. While delivering a voltage close to 1 V, the converter provides an overall efficiency of 68.5%. At this voltage, 14.8% is lost due to conduction losses, with 8.8% lost due to bottom-plate parasitics and 7.2% lost due to switching losses. At a V_L of close to 0.9 V, the contribution due to conduction losses increases to 23%. This is consistent with the explanation provided in Section III-A, wherein the farther away V_L is from the no-load voltage of 1.2 V, the larger the contribution of the conduction losses. Also, the drop in contribution of bottom-plate losses is consistent with (3). The contribution of switching losses decreases as the amount of capacitance engaged in the charge-transfer process for a given load current decreases as V_L decreases. As a result of this, the number of banks that are turned ON decreases thereby bringing down the switching losses.

Fig. 11(b) shows the efficiency with change in I_L while delivering a 0.9 V output. The DCpM mode of control helps to keep the efficiency constant over a wide range of load current. At light loads below 500 μA, the PFM mode control sets in to reduce switching losses and improve efficiency. The efficiency continues to fall at very low load currents due to the constant control losses which do not scale in this implementation. Table II shows the overall performance summary of the switched capacitor DC-DC converter.

TABLE I
BREAKDOWN OF CONTRIBUTION OF THE DIFFERENT LOSS MECHANISMS IN BRINGING DOWN THE OVERALL MEASURED EFFICIENCY OF THE SWITCHED CAPACITOR DC-DC CONVERTER. THE LOAD CURRENT DELIVERED IS 5 mA FOR THIS MEASUREMENT

V_L	Conduction Loss	Bottom-plate Loss	Switching Loss	Control + Other Loss	Final Efficiency
0.987	14.8%	8.8%	7.2%	0.7%	68.5%
0.889	23%	5.4%	4.8%	0.9%	65.9%

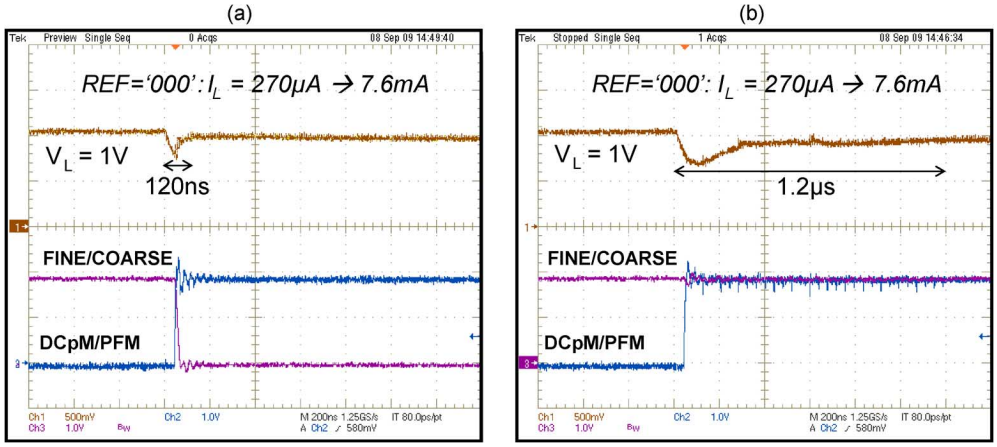

Fig. 9. Measured load transient performance of the SC converter with COMP3 (a) enabled and (b) disabled for a load current change from 270 μA to 7.6 mA.

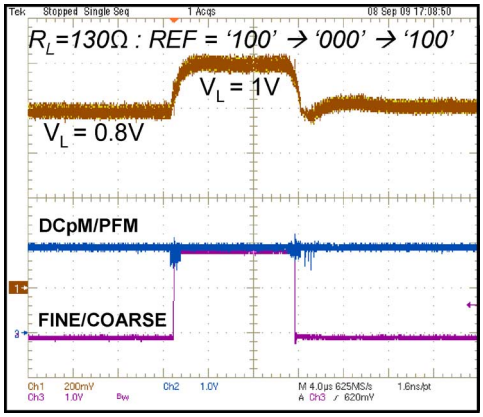

Fig. 10. Measured load transient performance of the SC converter with change in the reference voltage.

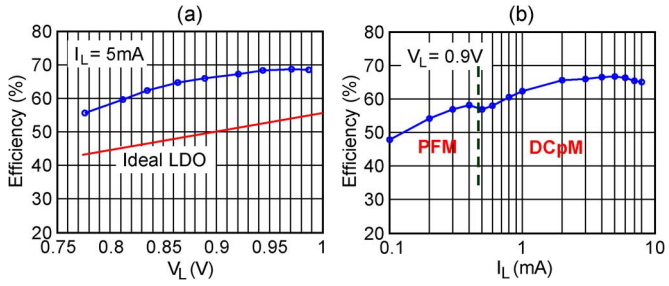

Fig. 11. Efficiency of the switched capacitor DC-DC converter with (a) change in load voltage while delivering a load current of 5 mA (b) Change in load current while delivering a load voltage of 0.9 V from a 1.8 V input supply.

VIII. CONCLUSION

This paper presented a fully-integrated switched-capacitor DC-DC converter as an alternative to on-chip linear regulators in 45 nm digital CMOS technology. The proposed implementation used digital capacitance modulation instead of traditional PFM and PWM control methods to maintain regulation against load current changes. This technique preserves constant frequency switching while also scaling switching and bottom-plate losses with changes in load current. Thereby, high efficiency was achieved across different load current levels while maintaining a predictable switching noise behavior. The converter occupied only 0.16 mm^2 in total on-chip area and delivered a programmable sub-1 V power supply with efficiency as high as 69% for load currents between 100 μA and 8 mA. Multiple modes of operation were used within the converter to enable fast transient response while keeping the ability to settle within narrow hysteretic bands.

TABLE II
SUMMARY OF THE KEY FEATURES OF THE CONVERTER

Technology	45nm CMOS
Active Area	0.16mm^2
Switching Frequency	30MHz
Input Voltage	1.8V
Output Voltage	0.8V – 1V
Maximum Load Current	8mA
Peak Efficiency	69%
Power Density (with load cap)	50mW/mm^2
Charge Transfer Capacitance	534pF
Load Capacitance	700pF
Capacitor Type	Gate-oxide

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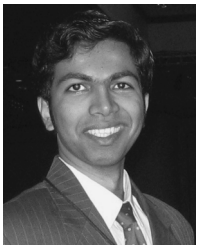

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