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Lifetime Estimation of Intrinsic Silicon Nitride MIM Capacitors in a GaN MMIC Process

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Abstract

We have studied the reliability of intrinsic SiN MIM capacitors designed for 48 V and 125 ^{0}C operation and manufactured in a GaN process flow. It is shown that very small area capacitors (10um x 10um) with a dielectric thickness of 400nm exhibit lifetimes as long as 1.48E10 hours under such conditions.

INTRODUCTION

In estimating Monolithic Microwave Integrated Circuit (MMIC) lifetimes, it is just as important to correctly evaluate the lifetime of the passive elements as that of the transistors. This becomes particularly crucial when the MMIC circuits are designed to operate at harsh conditions such as high voltages or high temperatures. GaN MMIC technology is one such example where the operation voltage can be as high as 48V and the application temperature can reach 125^{0}C. The lifetimes of passive elements in this technology should be assessed at these same conditions to make sure they are not the limiting agents for reliable operation of the whole structure.

There have been many studies to estimate the lifetimes of intrinsic MIM capacitors by different authors. In a GaAs process at 20 V of application voltage, lifetimes on the order of 1E9, 1E7 and 1E2 hours were reported for SiN thicknesses of 250 nm, 200 nm and 50 nm, respectively [1]. For a 160 nm thickness at 50 V operation, [2] reported lifetimes on the order of 3E9 hours. In this work, we evaluate the reliability of SiN MIM capacitors in a 48 V GaN HEMT process. The SiN thickness is 400 nm. This value is suitable for high voltage applications as the stressing electric field across the device stays at moderate values. The use of a relatively thick SiN dielectric improves the lifetime by decreasing the leakage current that is responsible for "charge to breakdown" [3]. This comes at the expense of decreasing capacitor density. Additionally, the dimensions of the capacitors were as small as 10um x 10um to assume a nominal thickness throughout the structure. Using small area capacitors helps eliminate weak spots and defects that could distort the intrinsic assumption through effective thinning model described in [4]. Weak spots and defects are responsible for increasing the stressing electric field locally which in turn decreases the lifetime.

FABRICATION

The capacitors in this work were realized as part of a full-flow wafer process using Nitronex NRF1 MMIC technology platform that is based on a 0.5um gate-length GaN-on-Si HEMT technology. In this technology platform, the AlGaN/GaN epitaxial layers were deposited by metalorganic chemical vapor deposition (MOCVD) on high-resistivity silicon substrates (>10 kΩ•cm). Wafers were processed through the entire process flow, including final thinning. Further details of the epitaxial growth, processing and reliability for this technology platform have been published in [5, 6].

The lower MIM electrode consists of a 500nm stack of Ni/Au which is also used to form the gate electrode. This was deposited directly on the GaN surface which had previously been implanted with nitrogen to assure device isolation. A 400 nm dielectric layer of silicon nitride was deposited by plasma-enhanced chemical vapor deposition (PECVD) at a temperature of 300^{0}C. This SiN thickness yields MIM capacitors with a capacitance of 150fF/um^2. The top electrode consisted of a Ti/Pt/Au metallization with a total thickness of 1000 nm. Interconnection to the top electrode is realized by means of a 4.5um gold plated air bridge process with 3um of nominal underpass clearance.

METHODOLOGY

The time it takes a capacitor to fail depends on the electric field and thus the voltage, and the temperature. Two major models for the dependence of capacitor lifetime on the applied electric field are widely used in the literature. These are the *linear field model* where $t \sim \exp(-\gamma E)$ and the *reciprocal field model* where $t \sim \exp(G/E)$ [1, 2, 4, 7, 8, 9]. Although the linear field model predicts a finite lifetime for no applied electric field, it estimates

reasonable median time to failure (MTTF) at high voltages. This is the model that is adopted in this work. On the other hand, reciprocal field model reveals suspiciously long lifetimes [1, 7]. The temperature dependence is characterized by t ~ exp(E_a/k_BT), however dependence on temperature is generally much weaker than field dependence as indicated by typical activation energies of around 0.1 eV [7]. Determination of lifetimes requires an estimation of the field acceleration parameter (γ), the activation energy (E_a) and the proportionality constant for the exponential expression for lifetime specified by the form:

$$t_{APP} = A \cdot \exp\left(-\gamma E + \frac{E_a}{k_B T} \right) \qquad (1)$$

In the linear field model, charge to breakdown model allows E_a and γ to project the associated stress time at one stress condition to another through the relationship [7]:

$$\Delta t_2(V_2, T_2) = \Delta t_1(V_1, T_1) \cdot \exp\left[-\gamma\left(\frac{V_2}{h} - \frac{V_1}{h} \right) + \frac{E_a}{k_B}\left(\frac{1}{T_2} - \frac{1}{T_1} \right) \right] \qquad (2)$$

where h is the dielectric thickness. In other words, the time spent under one stress condition (V_1, T_1) can be related to an "equivalent" stress time under a different condition (V_2, T_2) through the field acceleration parameter and the activation energy. This property is widely utilized in a quite useful way. Using a constant high voltage stress to estimate lifetimes will reveal possibly shorter lifetimes than measurement tools can accurately measure. On the other hand, a constant low voltage stress may not cause the device to fail in a reasonably short time to monitor. The voltage that will fail the device in a desirable time window is not known before the experiment.

As an alternative to constant voltage stressing schemes, a ramped voltage stress test method with constant step size in time and voltage has been proposed as a fast and reliable way to estimate lifetimes [8]. As described in Figure 1, this involves projecting the time spent at each step of the staircase voltage to the final value (V_{BD}) at which the device eventually breaks down and taking the sum of the equivalent times. This gives an estimate of the lifetime of the capacitor if it were to be stressed at a constant voltage of V_{BD} as [8]:

$$t_0 \approx \frac{\Delta\tau}{1 - \exp\left(-\gamma \frac{\Delta V}{h} \right)} \approx \frac{h}{\gamma R} \qquad (3)$$

where ΔV and $\Delta\tau$ are the incremental voltage and time step of the staircase voltage, respectively. R is the ramp rate calculated as $\Delta V/\Delta\tau$. Once t_0 is calculated, it can easily be related to the equivalent lifetime (t_{APP}) at any desired application voltage (V_{APP}) and temperature (T_{APP}) through equation (2):

$$t_{APP} = t_0 \cdot \exp\left[-\gamma\left(\frac{V_{APP} - V_{BD}}{h} \right) + \frac{E_a}{k_B}\left(\frac{1}{T_{APP}} - \frac{1}{T_{TEST}} \right) \right] \qquad (4)$$

V_{BD} and T_{TEST} are, respectively, the breakdown voltage value obtained during that specific ramp test and the temperature during that test. This formula does not neglect the effect of temperature unlike the majority of previously cited work.

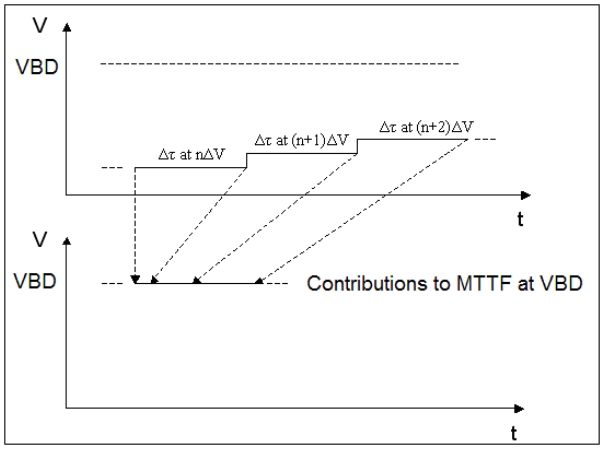

Fig. 1: Projection of stress times at different voltage levels to V_{BD} level (not to scale). Note that the contributions increase as the stepped voltage level gets closer to V_{BD}.

This analysis so far has assumed that γ and E_a are both known. Fortunately they can be calculated from similar ramped voltage stress tests. Combining and rewriting equations (3) and (4) in a more useful way after a few lines of algebra yield [7]:

$$\frac{V_{BD}}{h} = C_0 + C_1 \cdot \left(\frac{1}{k_B T} \right) + C_2 \cdot \ln R \qquad (5)$$

where C_0, C_1 and C_2 are constants. It can be easily shown that $\gamma = 1/C_2$ and $E_a = C_1/C_2$. This equation with three unknowns could be solved for the constants C_0, C_1 and C_2 by using V_{BD} values from three ramped stress experiments with at least two different ramp rates and two different temperatures.

RESULTS

In the approach followed in this paper, the same set of experimental data was used to estimate the field acceleration parameter, the activation energy and finally the lifetimes of capacitors. Two different voltage ramp rates, namely R_1=1V/s and R_2=0.1V/s at T_1=25^{0}C, were used to extract γ. Two different temperatures, namely T_1=25^{0}C and T_2=150^{0}C at a voltage ramp of R_1=1V/s, were used to extract E_a. This required three different stress conditions. Three groups of capacitors each consisting of

118 devices from 3 different lots and 4 different wafers were stressed at (R_1, T_1), (R_1, T_2) and (R_2, T_1). This is summarized in Table 1.

Table 1
Ramp rates and the temperatures used to stress three test groups of capacitors

Group 1	Group 2	Group 3
R_1 = 1 V/s T_1 = 25 ^{0}C	R_1 = 1 V/s T_2 = 150 ^{0}C	R_2 = 0.1 V/s T_1 = 25 ^{0}C

The ramps were approximated by a staircase voltage where the step voltage was ΔV=0.25V. $\Delta\tau$, the step time was 0.25s and 2.5s to obtain the desired ramp rates of 1V/s and 0.1V/s, respectively. The measurements were taken by means of a Keithley 4200 Semiconductor Characterization System where each device was stressed until catastrophic failure [7] as shown in Figure 2. The wafers were placed on a metal chuck where the temperature was maintained by a temperature controller.

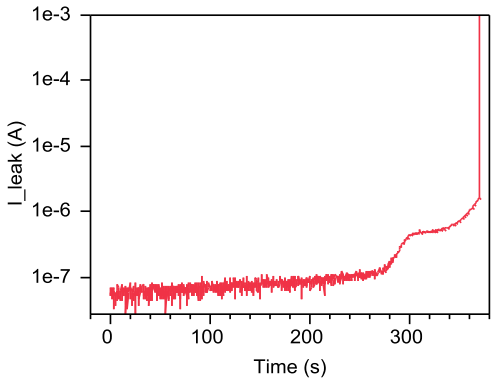

Fig. 2: Typical leakage current change over time in a voltage ramp test on capacitors. This specific capacitor was stressed at R_1=1V/s at T_1=25^{0}C.

Histograms for the breakdown voltages obtained for each of the groups are shown in Figure 3. A total of 28 devices from the whole set of capacitors were excluded from the analysis as they either did not fail until the measurement setup limit of 400V or did fail below 200V indicating infant mortality. For each group, the breakdown voltage distribution (V_{BD}) is well described by a narrow normal distribution, which indicates an intrinsic breakdown process rather than a defect driven process. The mean values for V_{BD} for each test condition is used to solve equation (5) to yield γ=37.5 nm/V and E_a=0.094 eV. These results are in close agreement with previously reported values [1, 2, 7, 9] for smaller SiN thicknesses. These parameters were also calculated for each wafer for comparison and close values were obtained as in Table 2.

DISCUSSION

Once γ and E_a were extracted, the lifetimes of each capacitor were evaluated using equation (4) for different

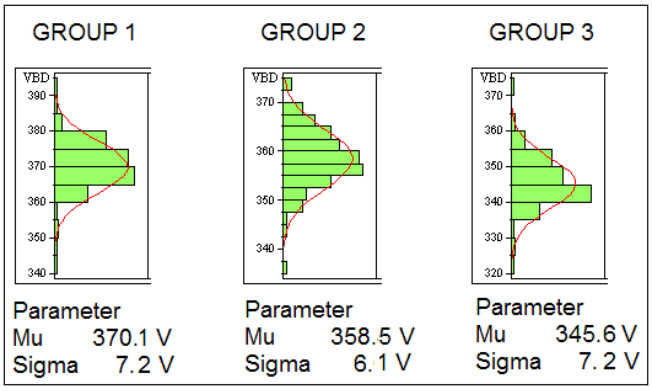

Fig. 3: Histograms of breakdown voltages during ramped voltage tests and the fit normal distributions. Groups include capacitors from all wafers and lots.

Table 2
γ and E_a by wafer

	Lot 1		Lot 2	Lot 3
	Wafer 1	Wafer 2	Wafer 3	Wafer 4
γ (nm/V)	34.8	36.9	40.6	39.8
E_a (eV)	0.084	0.091	0.104	0.114

V_{APP} and T_{APP}. The cumulative failure, the corresponding lognormal and Weibull probability plots of the lifetimes estimated for 28V and 25^{0}C for all the capacitors are illustrated in Figure 4. A good fit to the lognormal distribution indicates that this is a better model than Weibull for this intrinsic set of lifetimes with a normally distributed set of V_{BD} [9]. Thus this distribution is used to evaluate times to 0.1% failure and 50% failure (MTTF) with a 95% lower confidence bound using JMP for statistical calculations. Results are summarized for different voltages and temperatures of interest in Table 3.

An encouraging MTTF of 1.48E10 hours is obtained at 48V and 125^{0}C even with the 95% confidence bound. When the results are extrapolated for different voltages as in Figure 5, they are seen to be more than 1E9 hours up to 70V of application voltages. However, it should be kept in mind that these are intrinsic lifetimes obtained from small area capacitors of 10um x 10um. For extrinsic capacitors with larger areas, weak spots inside the dielectric will come into play through the "effective thinning model" and further analysis should be carried out to estimate lifetimes as described in [4, 10]. However, an intrinsic lifetime study is the first step to carry out such an analysis as it reveals the field acceleration parameter, activation energy and provides an upper bound for the extrinsic lifetime.

CONCLUSION

We have studied the reliability of 10um x 10um SiN dielectric MIM capacitors in a GaN process at high voltage and high temperature. From ramped voltage tests we have extracted a field acceleration parameter (γ) of 37.5nm/V

and activation energy (E_a) of 0.094eV. An encouraging intrinsic MTTF without neglecting the effect of temperature was calculated as 1.48E10 hours at 48V and 125^{0}C. This work is the first step for an extrinsic lifetime analysis as it provides the required parameters and the upper bound for extrinsic lifetimes.

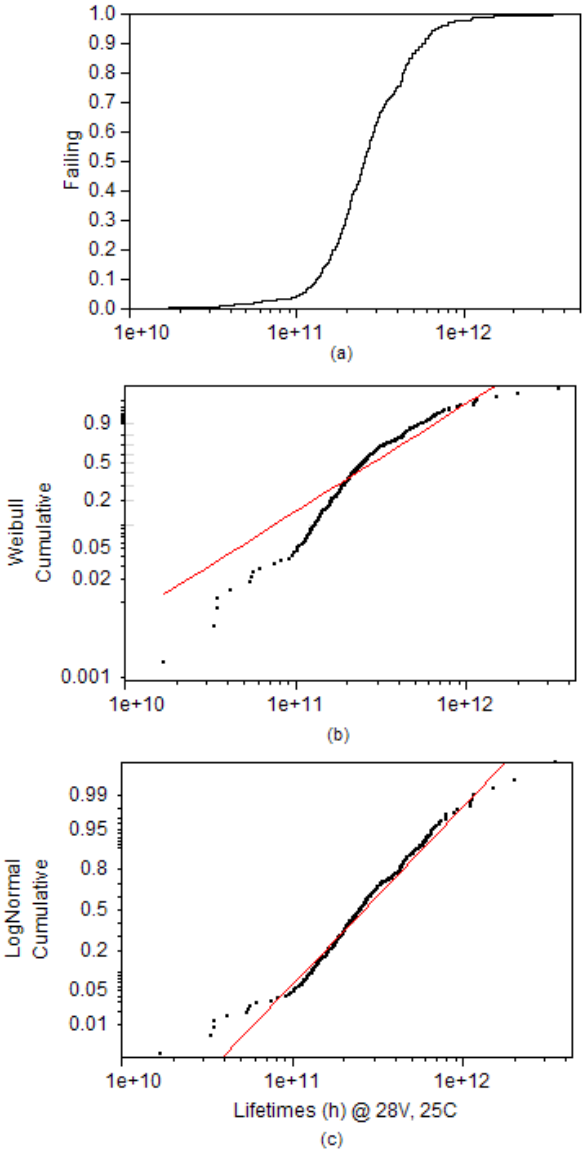

Fig. 4: Cumulative failure of caps (a) at 28V and 25C along with probability plots of lifetimes for Weibull (b) and lognormal (c) distributions

Table 3
Time (h) to percent failure evaluated by lognormal distribution with a 95% lower confidence bound

	28 V, 25 ^{0}C	28 V, 125 ^{0}C	48 V, 25 ^{0}C	48 V, 125 ^{0}C
0.1%	3.09E10	1.22E10	4.73E9	1.87E9
50% (MTTF)	2.44E11	9.66E10	3.74E10	1.48E10

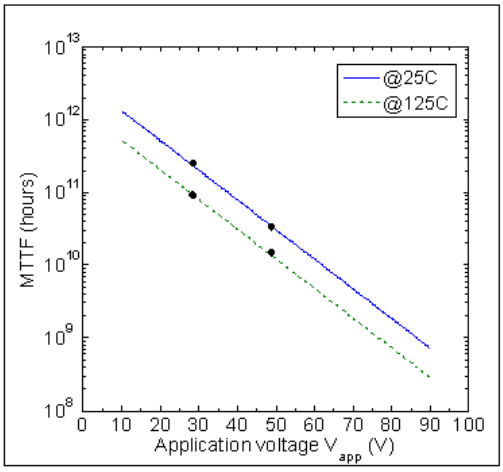

Fig. 5: Estimated MTTF with 95% lower confidence bounds versus application voltage at 25^{0}C and 125^{0}C. Dots represent data for time to 50% failure when operated at 28V and 48V as shown in Table 3.

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ACRONYMS

MIM: Metal Insulator Metal
MMIC: Monolithic Microwave Integrated Circuit
MTTF: Median Time to Failure