Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed Cmos Electronics

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***Abstract*—Carbon-based nanomaterials such as metallic single-walled carbon nanotubes, multiwalled carbon nanotubes (MWCNTs), and graphene have been considered as some of the most promising candidates for future interconnect technology because of their high current-carrying capacity and conductivity in the nanoscale, and immunity to electromigration, which has been a great challenge for scaling down the traditional copper interconnects. Therefore, studies on the performance and optimization of carbon-based interconnects working in a realistic operational environment are needed in order to advance the technology beyond the exploratory discovery phase. In this paper, we present the first demonstration of graphene interconnects monolithically integrated with industry-standard complementary metal–oxide–semiconductor technology, as well as the first experimental results that compare the performance of high-speed on-chip graphene and MWCNT interconnects. The graphene interconnects operate up to 1.3-GHz frequency, which is a speed that is commensurate with the fastest high-speed processor chips today. A low-swing signaling technique has been applied to improve the speed of carbon interconnects up to 30%.**

***Index Terms*—Carbon nanotubes, graphene, high speed, interconnect, on-chip.**

I. Introduction

INTERCONNECT wires have always been one of the major technology components of modern high-speed integrated circuits (ICs). In the most advanced IC technology, the capacitance associated with interconnects typically accounts for about 50% of the active processor power consumption [1], and the associated signal delay along interconnects is one of the main bottlenecks for the routing of high-speed signals. With the progressive miniaturization of semiconductor devices, the need for longer, thinner, and faster interconnects with lower power consumption is becoming more pronounced. Conventional interconnect materials such as copper are facing great challenges to satisfy requirements when physical dimensions are scaled down to the nanoscale range. First, the conductance of copper significantly decreases when the lateral dimension is scaled down: the resistivity of local interconnects is increased by about 50% when wire pitch decreased from 100 to 50 nm due to increased electron scattering at the grain boundaries and wire surfaces [2], which increases the circuit signal delay; equally important is that the reliability of copper wires suffers when the current density increases due to the miniaturization. Increased wire resistivity leads to increased Joule heating and degraded electromigration lifetime, which result in decreased maximum allowed current density in copper wires [2]–[4]. Therefore, alternative interconnect materials are being actively researched to improve on-chip interconnect performance [5].

In recent years, graphene has gained a lot of attention for being a promising new material for high-speed electronics [6]–[9], since it not only shares the same outstanding transport properties as carbon nanotubes [10]–[13], such as high mean free path and high current-carrying capacity but also offers potential advantages such as simpler fabrication process, better material control, and better reproducibility [14]. Researchers have demonstrated graphene transistors with intrinsic cutoff frequency as high as 100 GHz [7], graphene nanomechanical resonators operating at 50–80 MHz [8], and microwave switches operating at gigahertz (GHz) range [9]. When used as interconnects, graphene also showed a great potential: previous theoretical calculations have shown that the conductivity of metallic graphene nanoribbons (GNR) would outperform copper wires with unity aspect ratio when interconnect width is scaled down below 8 nm [15]. The theory also predicts that high-quality doped GNRs offer smaller signal delay than copper at the 11-nm technology node when used as global wires [16]. DC experimental characterizations showed that the resistivity of good-quality GNRs in the width range from 18

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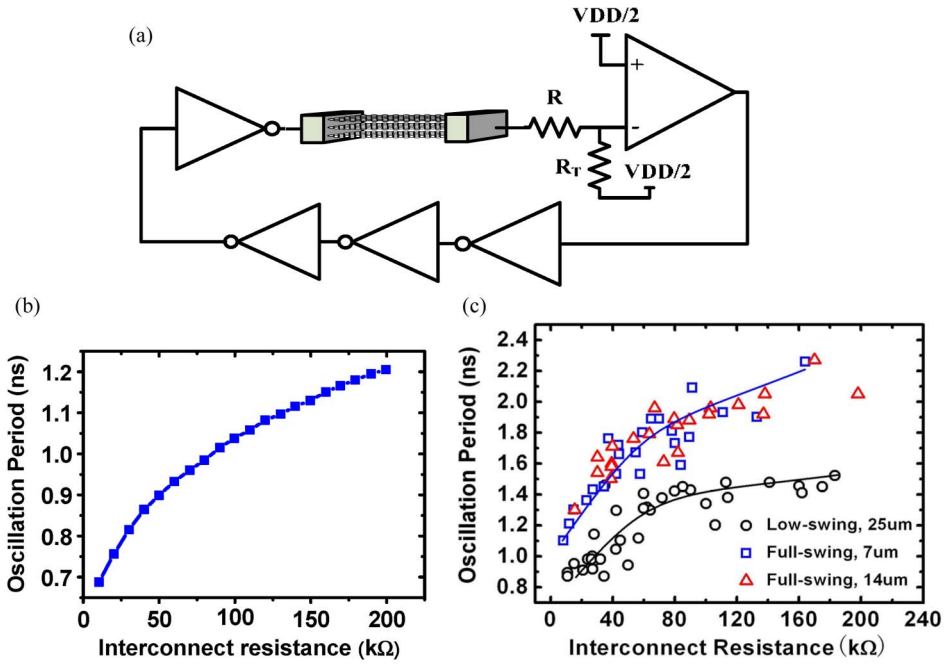

Fig. 1. Application of low-swing oscillator circuitry for interconnect performance improvement. (a) Circuit diagram of a five-stage low-swing ring oscillator with a differential amplifier at the receiver end of the inverter chain. The line is terminated by a termination resistor ($R_T = 20$ kΩ, $R \sim 0.5R_T$ is a value determined by the tradeoff between speed improvement brought by low-swing signaling and the sensitivity of the differential amplifier at the receiving end) to a midsupply voltage; hence, the signal swing at the receiver end is reduced to $V_{DD} \times R/R_T$, whereas the speed is increased by a factor R/R_T. (b) Modeling results of signal delay along 30-μm-long MWCNT interconnects integrated with a low-swing oscillator circuit. The signal delay increases with increasing MWCNT resistance, as expected. For a good-quality MWCNT (lower resistivity), signal delay as low as 0.7 ns can be expected. (c) Experimental performance comparison of MWCNT interconnects integrated on both full- and low-swing circuits. We can see that, even with an increased length, the MWCNT interconnect integrated with a low-swing circuit still shows a significant signal delay improvement of about 30% at the same resistance value. (Symbols) Experimental data. (Solid lines) Visual guides.

to 50 nm is smaller than 10 $\mu\Omega \cdot$ cm, which is comparable with copper wires with the same physical dimensions [17]. Furthermore, GNRs have breakdown current density on the order of 10^8 A/cm^2, which is ten times higher than the maximum permissible current density of copper [18]. However, despite the favorable theoretical and dc characterization results of graphene interconnects, experimental demonstration of high-speed signaling using graphene interconnects has not yet been made, and there is no report of integration of graphene with standard CMOS technology, which is a key requirement for future integrated graphene electronics. We address these topics by presenting the first experimental demonstration of high-speed graphene interconnects integrated with a five-stage standard CMOS low-swing ring oscillator circuit operating above 1 GHz, which is a major milestone for graphene electronics.

II. Low-Swing Circuitry

The CMOS five-stage ring oscillator circuit is fabricated using standard 0.25-μm CMOS technology.[1] Each ring oscillator is designed with a missing interconnect wire onto which a graphene interconnect wire was subsequently integrated. Only one graphene interconnect is integrated with each ring oscillator, so that we can characterize each graphene interconnect individually while maintaining the high oscillation speed. A low-swing signaling technique is implemented for the ring oscillator circuit to serve as a method to investigate the high-frequency performance of interconnects. A lower input-signal swing shortens the time needed to charge up the load capacitance, thereby improving the ring oscillator speed substantially. Since the main focus of this paper is interconnect performance, the possible extra chip area and power cost of introduction of a low-swing receiver is not discussed here but has been previously studied elsewhere [19]. Fig. 1(a) shows the ring oscillator circuit diagram. The differential amplifier at the receiving end provides higher signal sensitivity than a simple inverter stage. Simulation shows that the signal delay of 30-μm-long multiwalled carbon nanotube (MWCNT) interconnects (diameter $\sim$ 30 nm and resistivity $\sim$ 650 $\mu\Omega \cdot$ cm) in this low-swing ring oscillator loop can be on the order of 100 ps [see Fig. 1(b)].

To demonstrate the speed improvement brought by the improved ring oscillator circuit design, we integrated, using dielectrophoresis, the same kind of MWCNT interconnects onto both the low-swing CMOS ring oscillators and the standard full-swing CMOS oscillators. The fabrication process was detailed in [20]. The experimental characterization result shows a significant 30% average speed improvement for the same wire resistance [see Fig. 1(c)].

III. Graphene Interconnect Device Fabrication

The process flows of graphene growth/transfer and post-CMOS fabrication are shown in Fig. 2. First, large-area multilayered graphene (average thickness of about 15–20 nm,

[1]The 0.25-μm ring oscillator CMOS platforms were fabricated by Taiwan Semiconductor Manufacturing Company.

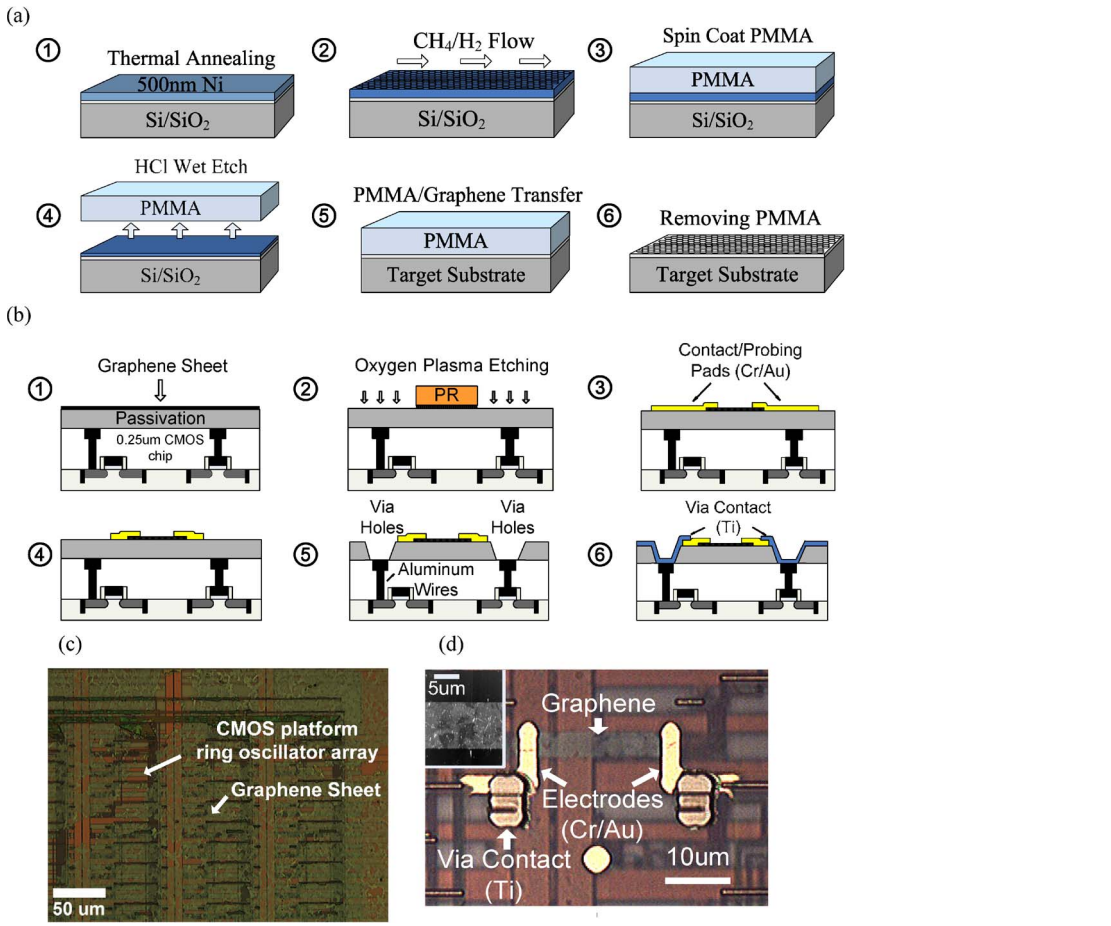

Fig. 2. Device fabrication process flows and images of as-fabricated on-chip graphene interconnects. (a) Process flow of CVD graphene growth and PMMA-assisted transferring. (b) Process flow of the posttransfer fabrication process for integrating graphene with underneath CMOS circuitry. (c) Optical image of graphene after being transferred on top of the CMOS ring oscillator array. (d) Optical image of one fabricated graphene interconnect on top of the CMOS ring oscillator array. The lines that appear black in the middle of Ti via contacts are M3 Al lines. (Inset) AFM image of graphene stripes on the SiO_2/Si test substrate.

which is measured using atomic force microscopy) is grown using chemical vapor deposition (CVD) on a 500-nm electron-beam-evaporated nickel layer and then transferred to a 5 mm $\times$ 5 mm CMOS chip with the low-swing circuitry as previously described. The CVD growth is carried out for 5 min at 1000 °C, with 5 sccm of methane and 1300 sccm of hydrogen [21]. After the growth is completed, a thin layer of polymethyl methacrylate (PMMA) is spin coated on top of the graphene/nickel substrate, and a 10% HCl aqueous solution is used to lift off the PMMA–graphene layer from the underneath nickel layer. Then, the PMMA–graphene film is placed on the target substrate, and the PMMA is subsequently washed off using acetone. An average sheet resistance of about 700 $\Omega/$sq is extracted for graphene before post-CMOS processing by transferring graphene on top of the Si/SiO_2 substrate. In principle, this method is scalable to transferring arbitrary large areas of graphene from arbitrary substrates to CMOS substrates. For this reason, it is an attractive option for integrating wafer-scale graphene with wafer-scale CMOS substrates to facilitate very large scale integrated (VLSI) graphene/Si electronics.

After the graphene transfer, all processing steps are done using standard CMOS-compatible fabrication techniques. First, graphene is patterned into stripes of different widths/lengths using optical lithography and oxygen plasma etching. The interconnect width ranges from 3 to 5 μm, whereas the length ranges from 5 to 145 μm. Cr/Au electrodes are deposited as contacts to graphene. Then, via holes are formed by etching through the passivation layer, reaching down to the topmost metal layer of the CMOS chip. Finally, the via contacts between graphene interconnects and underlying CMOS circuitry are made by filling the via holes with Ti.

IV. Characterization Results

To see whether the quality of this novel nanomaterial is significantly degraded by going through the standard CMOS fabrication process, we measured the sheet resistance of graphene before and after the standard CMOS fabrication process, Fig. 3(a) shows that the average sheet resistance of graphene remains to be 700 $\Omega/$sq on average, which indicates that the quality of graphene is generally preserved during device fabrication. The I–V characteristics of the fabricated graphene interconnect in Fig. 3(a) indicate that we have achieved an ohmic contact between graphene and metal. At the same time, the linear I–V curves show that the contact between graphene and metal is ohmic. Contact resistance is negligible compared with

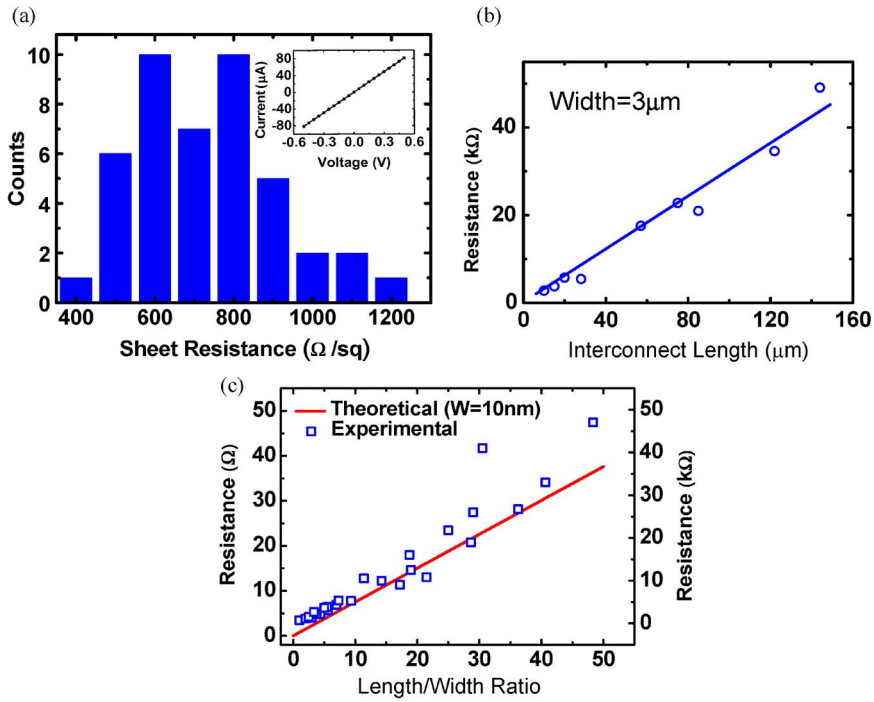

Fig. 3. DC characterization results for graphene interconnects. (a) Sheet resistance distribution. The average sheet resistance is Rs $\sim$ 711 Ω/sq. The wide distribution was due to variation in the number of layers and surface defects. (Inset) I–V curve of a graphene interconnect showing an ohmic contact (L/W = 28 μm/3 μm, $R = 6.15$ kΩ). (b) Interconnect resistance as a function of length, indicating diffusive transport. The intercept on the y-axis gives the contact resistance between graphene and metal. It is negligible compared with the interconnect resistance. (c) Comparison between theoretical and experimental results for interconnect conductance for the same length/width ratio. (Experimental results are obtained using interconnects with varied widths.) Theoretical results are derived using the model proposed in [16].

interconnect resistance [see Fig. 3(b)]. Theoretical conductance calculation is done based on the multilayer graphene conductivity model proposed in [16] using the material mean free path derived from our sheet resistivity data. Comparison with experimental measurement is shown in Fig. 3(c). To demonstrate the high-speed signal routing capability of graphene interconnects, we characterized the ring oscillator frequencies and amplitudes by wire bonding the postprocessed CMOS chip to a pin grid array package and mounting the package into a printed circuit board for high-frequency electrical testing [see Fig. 4(a)]. Gigahertz oscillation frequency is observed for ring oscillators with graphene interconnects as long as 80 μm, which confirms the great potential of graphene for future VLSI interconnects. The oscillation frequency of the ring oscillator circuit is determined by the total circuit RC delay as in (1) (f is the circuit oscillation frequency, R is the total resistance of the circuit dominated by graphene interconnect resistance, $C_{\rm tot}$ is the total capacitance of the circuit, ρ_s is the sheet resistivity of graphene, L is the interconnect length, and W is the interconnect width), which agrees with our experimental characterization results shown in Fig. 4(b) and (c): the circuit oscillation frequency is directly correlated with the interconnect width and inversely correlated with the length/width ratio. Thus

$$f \propto \frac{1}{RC_{\rm tot}} \propto \frac{1}{\rho_s\left(\frac{L}{W}\right)\cdot C_{\rm tot}}. \quad (1)$$

By integrating graphene and the MWCNT with the same type of low-swing CMOS ring oscillator, we directly compared the RF performances of the two materials. Fig. 4(d) shows that graphene offers a higher oscillation frequency because of its lower resistivity, and the ring oscillator with best performance graphene wire has an oscillation frequency that is comparable with the reference oscillators with aluminum wire. However, at the same resistance value, the MWCNT has better signal delay performance. This may be due to the larger total capacitance associated with our wide graphene stripes: using the Predicative Technology Model [22], the wire-to-ground electrostatic capacitance for a 1-μm-wide graphene wire is around 0.118 fF/μm (dielectric thickness = 500 nm), whereas a 30-nm-wide MWCNT wire has capacitance around 0.0345 fF/μm. When graphene is scaled down to similar physical dimensions as the MWCNTs (width $\sim$ 30 nm), the estimated single graphene wire electrostatic capacitance is about 0.01 fF/μm, similar to that of the MWCNT wire estimated using the 1-D transmission line model [23]. However, while scaling down the width of graphene decreases the interconnect capacitance, it brings other issues like increased contact resistance and increased wire resistivity due to limited material quality and edge roughness. Although study has shown that it is possible to fabricate chirality-controlled graphitic nanoribbons [24] and that optimizing contact figuration can help achieve an ohmic contact between GNRs and metal, more research needs to be done to make high-frequency operation of GNR interconnects practical.

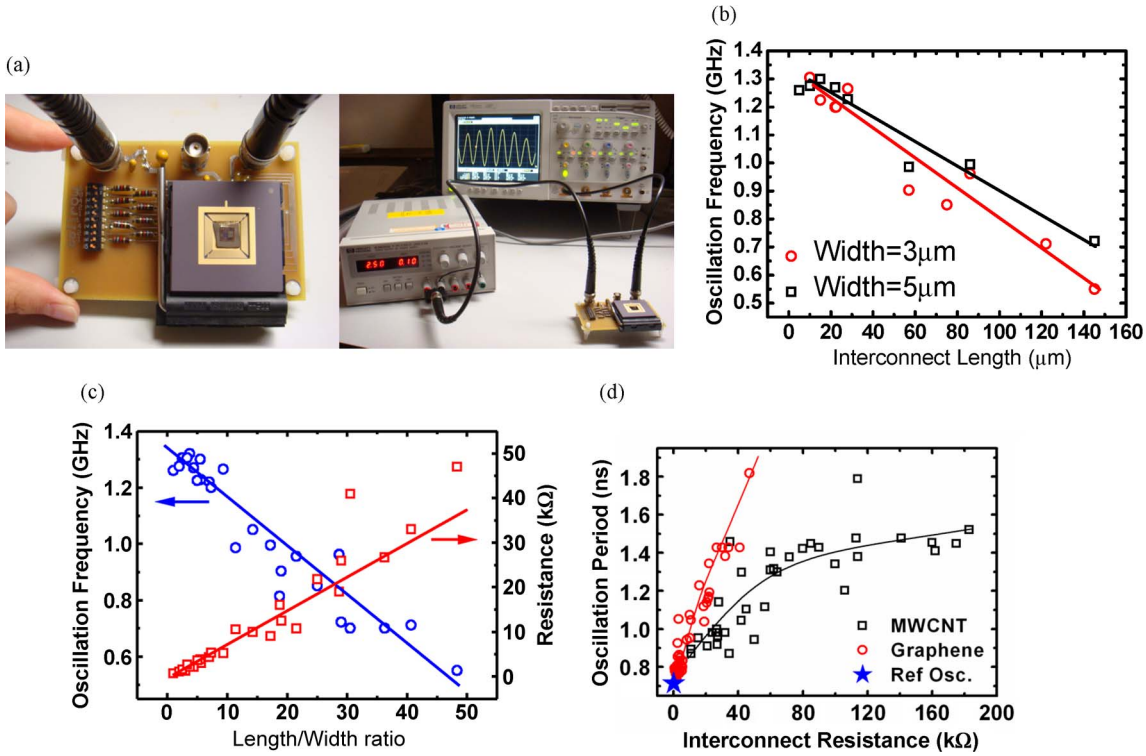

Fig. 4. RF characterization of graphene on-chip interconnects. (a) Printed circuit board and setup for RF measurements. (b) Oscillation frequency for various interconnect lengths and widths. Gigahertz range operation frequency is observed for interconnects up to ~ 80 μm long. (c) Oscillation frequency and resistance as functions of L/W ratio indicative of the number of squares. (Symbols) Experimental data. (Bold lines) Visual guides. (d) Oscillation period as a function of interconnect resistance for the CMOS reference interconnects (aluminum), MWCNTs, and graphene. For the same ring oscillator circuit, graphene offers higher speed operation compared with MWCNTs. However, at the same resistance values, MWCNT interconnects are faster most likely due to their smaller capacitance. (Symbols) Experimental data. (Bold lines) Visual guides.

V. Conclusion

In summary, we have successfully demonstrated the first integration of graphene interconnects with standard CMOS technology. Gigahertz operation frequency is observed for graphene interconnects as long as 80 μm. By using the low-swing signaling technique, wire signal delay performance is further improved by about 30%. Along with recent reports on large-scale [25] transfer-free [26] low-temperature [27] graphene synthesis techniques, the future of graphene interconnects in VLSI technology appears increasingly promising, although advances in the controlled synthesis of continuous sheets of graphene and understanding of graphene interconnect performance limits require further research.

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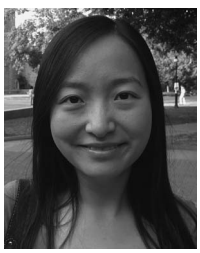

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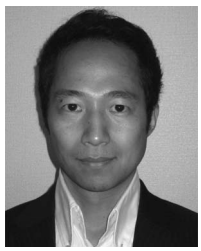

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Shinobu Fujita, photograph and biography not available at the time of publication.

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