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GaN-on-Si Technology, A New Approach for Advanced Devices in Energy and Communications

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***Abstract*—The Si substrate of GaN-on-Si wafers offers new opportunities to increase the functionality and performance of nitride-based devices. This paper will review three examples of these new devices/systems. First, GaN-on-Si substrates allow the on-chip heterogeneous integration of GaN and Si electronics. Second, the easy removal of the Si substrate through dry or wet etching gives access to the N-face of the GaN layer, and all the new device structures that this orientation enables. Finally, the use of Si substrates for the growth of GaN high voltage switches makes the cost of these devices competitive with Si devices, and the total or partial etch of Si brings a new degree of freedom to increase the breakdown and performance of GaN transistors.**

I. INTRODUCTION

Nitride semiconductors are quickly transforming our world by enabling new solid-state lighting, highly efficient amplifiers for wireless communications, advanced power electronics with unprecedentedly low losses, and a large array of new high performance devices. Out of the different substrates available for the growth of nitride-based semiconductors (i.e. bulk GaN, Si, sapphire and SiC), the Si substrate has traditionally been considered a low-cost, lower-performance option. In this paper we will show that the use of a Si substrate, far from hindering the performance of nitride semiconductors, is a powerful tool that gives unprecedented flexibility for the fabrication of advanced new nitride-based devices.

Three different examples will be discussed. First, the wafer bonding of a GaN-on-Si sample to a Si (100) wafer has been used to demonstrate the first on-wafer integration of GaN electronics and Si (100) CMOS circuits [1]. This integration allows the combination of the high complexity and flexibility of Si circuits with the vast array of new devices enabled by GaN: transistors, LEDs, energy harvesting devices, and filters. A second example involves the fabrication of N-face GaN transistors by removing the Si substrate of a Ga-face-grown sample [2]. These new devices offer new opportunities for improved heat dissipation and high frequency electronics. Finally, the large wafer diameters available for GaN-on-Si samples provide an important competitive advantage for the development of GaN-based high performance power electronics [3]. These devices, with an estimated potential market above $10 billion dollar, could be key to energy savings equivalent to 10% of the global electricity consumption.

II. ON-WAFER INTEGRATION OF GAN TRANSISTORS AND SI (100) CMOS ELECTRONICS

The unique properties of AlGaN/GaN High Electron Mobility Transistors (HEMTs) have made them the best option for many RF amplifiers. The unsurpassed high current levels possible in these devices, in combination with their very high breakdown voltage allow almost 10 times higher maximum power density than GaAs amplifiers [4]. In

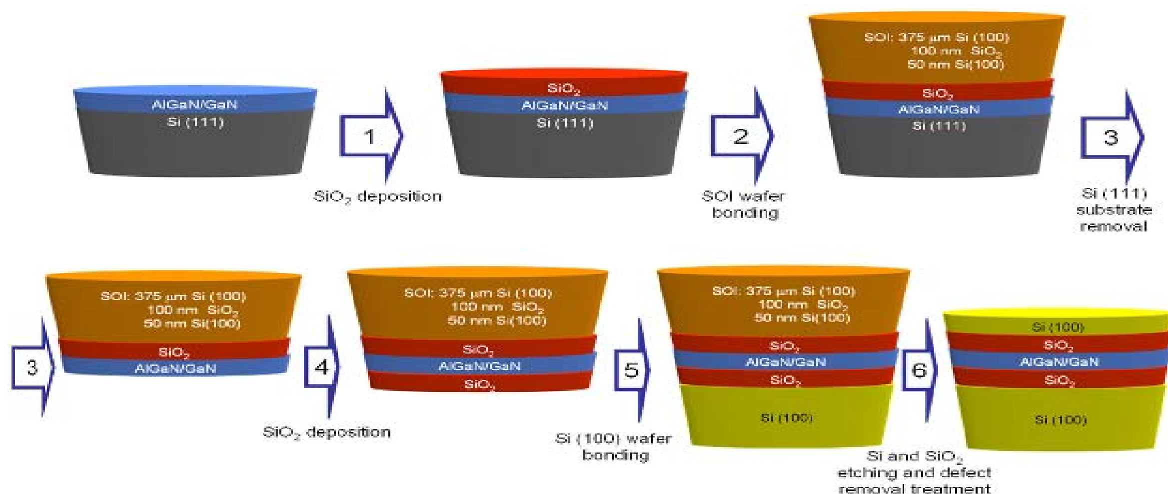


Figure 1. Main steps in the fabrication of a Si/GaN/Si hybrid wafer.

addition, their high frequency performance enables extremely high power added efficiencies by maximizing the available power gain, and their high output resistance significantly simplifies the design of the matching networks in RF amplifiers. Finally, the recent demonstration of device lifetimes in excess of 10^6 hours at a channel temperature of 175ºC make this technology one of the most reliable semiconductor technologies.

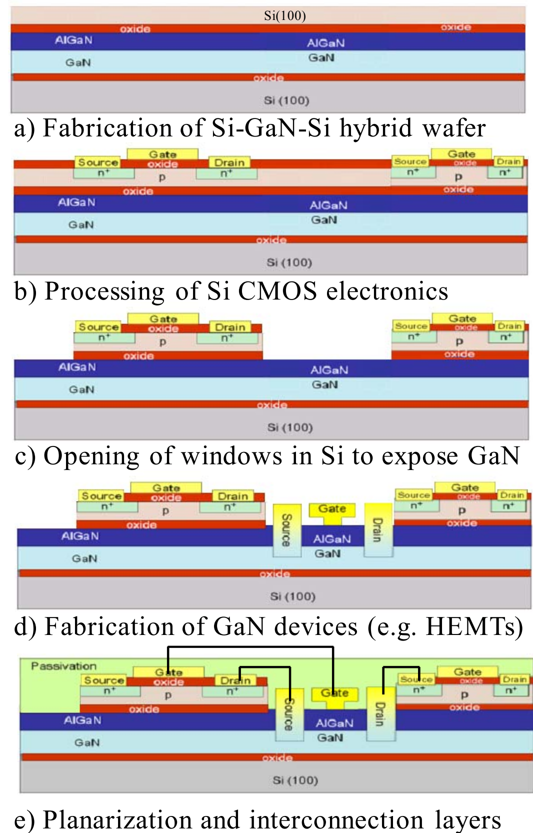
In spite of the excellent performance demonstrated by nitride transistors, these devices cannot compete with Si MOSFETs in terms of scalability and level of integration. On the other hand, traditional Si electronics is facing tremendous challenges to continue its scaling and performance improvement. The on-chip heterogeneous integration of GaN power devices and Si (100) CMOS electronics would enable unprecedented flexibility for advanced circuits, from highly linear power amplifiers, to new power distribution networks in Si microsystems.

The high thermal stability of GaN-based semiconductors makes them ideal for their integration with Si, as the GaN material can survive the very demanding thermal budget of Si processing. We have recently demonstrated a technology to integrate, for the first time, these two devices. This technology is based on the fabrication of a hybrid Si (001) / GaN / Si (001) substrate by wafer bonding (Figures 1 and 2). Due to the high thermal stability of GaN, Si CMOS electronics can then be processed in this new substrate without affecting the nitride layers underneath the surface (Figure 3). After the Si devices are fabricated, the Si material is removed from the regions where nitride devices are needed. Then, the nitride devices (transistors, LEDs, lasers or sensors) are processed and, finally, an interconnection layer forms the final hybrid circuits.

Figure 2. Scanning electron micrograph of the cross-section of a Si/nitride/Si wafer.

Figure 4 shows the scanning electron micrograph of a finished sample where AlGaN/GaN HEMTs were fabricated in very close proximity to Si (100) pMOSFETs following the process flow outlined in Figure 3. These devices show excellent DC performance and we are currently developing new circuits to take advantage of the flexibility enabled by this integration. Some of these circuits include:

- Integrated GaN power switches and Si control electronics
- High power digital-to-analog converters (DACs)
- On-wafer wireless transmitters
- Driver stages for on-wafer optoelectronics
- Power amplifiers coupled to Si linearizer circuits
- High speed (high power) differential amplifiers
- Normally-off power transistors based on the cascaded connection on a Si normally-off transistor and a normally-on GaN HEMT.



a) Fabrication of Si-GaN-Si hybrid wafer

b) Processing of Si CMOS electronics

c) Opening of windows in Si to expose GaN

d) Fabrication of GaN devices (e.g. HEMTs)

e) Planarization and interconnection layers

Figure 3. Main processing steps for the fabrication of GaN-Si hybrid

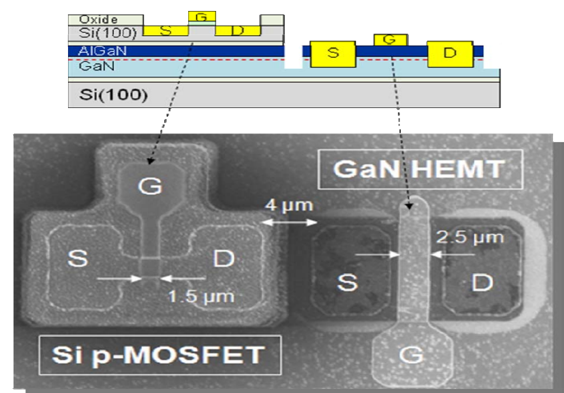


Figure 4. Scanning electron micrograph of the heterogeneous integration of GaN and Si electronics.

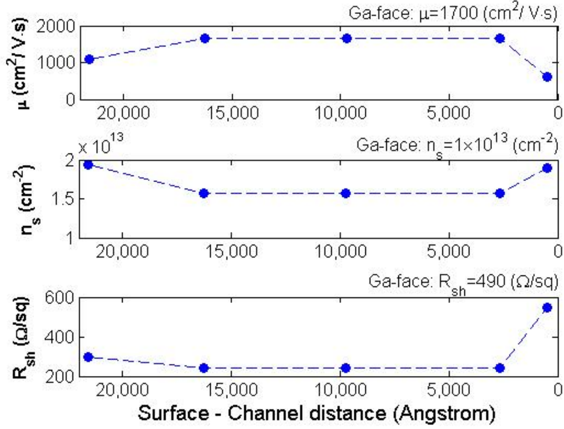


Figure 5. Electron mobility (μ), 2DEG density (n_s), and sheet resistance (R_{sh}) of N-face GaN as a function of the distance between N-face surface and 2DEG channel estimated by room temperature Hall measurement.

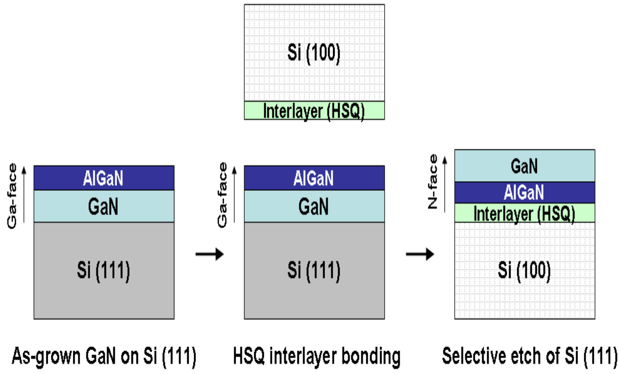


Figure 6. Main processing steps in the fabrication of N-face GaN on Si (100) substrate through substrate removal.

- New enhancement-mode power transistors
- Buffer stages for ultra-low-power electronics

III. N-FACE GAN ELECTRONICS FROM GA-FACE GAN-ON-SI WAFERS

Although most of the reported GaN devices have been fabricated on nitride structures grown along the c-direction (i.e. Ga-face), N-face GaN/AlGaN transistors have the potential of higher electron confinement and lower contact resistances [5]. However, in spite of this promise, the performance of N-face devices is still much lower than in Ga-face devices due to the inferior material quality. Although N-face devices have been grown by molecular beam epitaxy and, recently [6], by metal-organic chemical vapor deposition (MOCVD) [7], the growth of N-face nitrides is much more challenging than the growth of the more stable Ga-face structure. The use of Si substrates provides a new approach for the fabrication of N-face nitride wafers, not through growth but through the substrate removal of a Ga-face-grown GaN samples, as we will demonstrate in this section.

The Ga-face AlGaN/GaN transistor structures used in this work were grown on Si (111) substrates by MOCVD at Nitronex with a structure similar to the one described in Reference [8]. To have access to the N-face of these samples, we have developed the substrate transfer technology shown in Figure 6. First, the Ga-face surface was bonded to a Si (100) carrier wafer by using a hydrogen silsesquioxane (HSQ) interlayer. HSQ is a flowable oxide with excellent thermal stability, which stands the high thermal budget required during the processing of GaN devices. The HSQ film is spin-coated on Si (100) to a thickness of about 1000 Å and baked sequentially on hot plates at 150 ºC and 200 ºC for 1 minute each. Then, the HSQ-coated Si (100) substrate is attached to the as-grown AlGaN/GaN layer and thermally compressed at 400 ºC for an hour. The elevated temperature hardens the HSQ layer and forms an extremely stable bond between the GaN wafer and the Si carrier wafer. After the wafer bonding, the original Si (111) substrate is completely removed by dry etching using an SF_6-based dry etch. The GaN buffer is an effective etch-stop layer for the SF_6 plasma etch and a smooth N-face GaN surface is obtained at the end of the etch. After the substrate transfer, the N-face GaN buffer is etched by electron cyclotron resonance reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture until the desired distance between

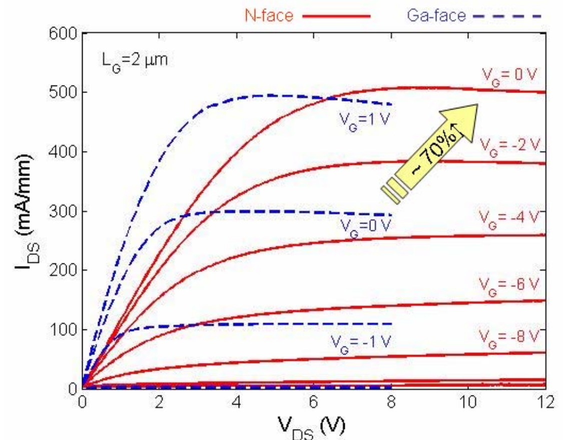


Figure 7. DC current-voltage characteristics of N-face (solid line) and Ga-face (dashed line) HEMTs with a gate length (L_G) of 2 μm. Almost 70% higher maximum current at V_G=0 V is achieved in N-face HEMTs. Higher on-resistance (R_{on}) in N-face HEMTs is due to non-optimized ohmic contacts.

the N-face GaN surface and the AlGaN/GaN interface is achieved.

The effect of the GaN buffer thickness on the electron transport was evaluated by four-point van der Pauw Hall measurements. The GaN buffer was etched as described in the previous paragraph and the remaining GaN thickness was measured with an interferometer (NanoSpec). The main transport properties are almost constant with buffer thickness (μ=1670 $cm^2/V \cdot s$, n_s=1.6×10^3 cm^{-2}, R_{sh}=240 Ω/sq). The sheet resistance is 50% lower than the sheet resistance measured in the Ga-face of the sample. This important reduction in the sheet resistance is due to an increase in the mobility and electron density during the substrate removal process. The change in the Fermi level pinning when the N-face surface is

exposed after the substrate removal is believed to be partly responsible for this improvement although other causes are still under investigation.

N-face GaN/AlGaN structures fabricated through the substrate removal process described previously have been used in the fabrication of N-face high electron mobility transistors (HEMTs). In this samples, the distance between the N-face surface and the 2DEG was reduced to 1000 Å by a Cl_2-based dry etching process. A Ti/Al/Ni/Au multilayer was deposited for the ohmic contacts and annealed at 870ºC for 30 s in a N_2 atmosphere. Then Cl_2/BCl_3 plasma was used for the mesa isolation. Finally, a 2 µm-length gate is defined by photolithography and a Ni/Au/Ni metallization was deposited for the Schottky contact. The drain current versus drain voltage characteristic of the N-face device is shown in Figure 7 and it is compared to a Ga-face HEMT used as a reference. For a gate voltage of 0 V, the maximum current in the N-face device is almost 70% higher than in the Ga-face device. This difference is mainly due to the higher charge density in the N-face device. The transconductance in this initial N-face deviced is low due to the large gate-to-channel distance.

To improve the performance and yield of this technology, we are currently focused on increasing the wafer diameter and in developing a selective etch technique to reproducibly thin down these N-face wafers and improve, in that way, the device transconductance.

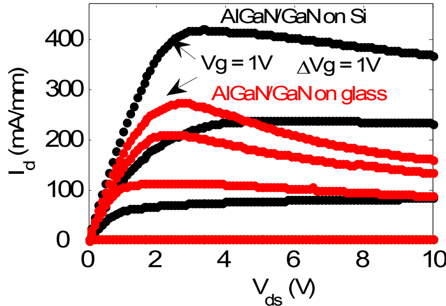


Figure 8. I-V characteristics of an AlGaN/GaN HEMT before and after transferring it to a glass substrate.

IV. GaN-on-Si Power Electronics

AlGaN/GaN HEMTs grown on Si substrates have also attracted a great interest for power electronics applications. However, despite the low cost of the Si substrate, the breakdown voltage (V_{bk}) of AlGaN/GaN HEMTs grown on Si (less than 600 V for 2 µm total nitride epilayer) is much lower than that grown on SiC (1.9 kV for 2 µm total epi-layer), which severely reduces device performance. In this section we propose the total or partial removal of the Si substrate to increase the breakdown voltage of GaN power switches grown on Si substrates [3].

For the device demonstration, we used the same standard epitaxial structure described in Section III. In this case, the devices have a gate width of 100 µm, a 2 µm gate length, and varying gate-to-drain distances. To eliminate the vertical breakdown of the AlGaN/GaN HEMTs on Si, we removed the Si substrate and transferred the AlGaN/GaN HEMTs to a glass wafer through wafer bonding.

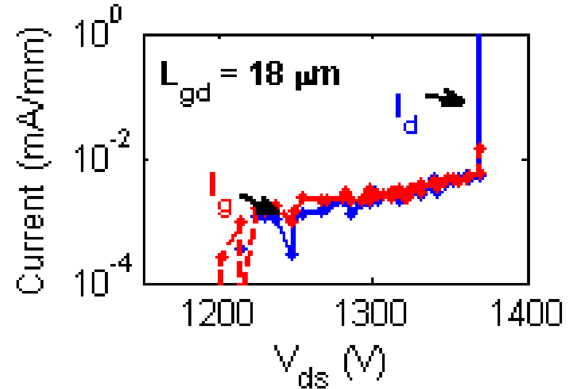


Figure 9. Three terminal breakdown of an AlGaN/GaN device on glass with L_{gd} = 18 µm and V_{gs} = - 8 V.

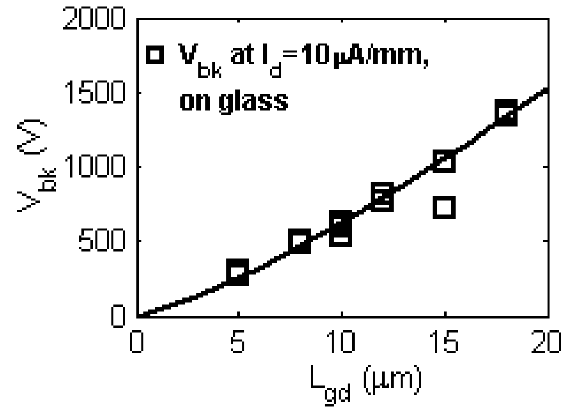


Figure 10. Three terminal breakdown of AlGaN/GaN HEMTs with different L_{gd} transferred to a glass substrate.

The device maximum current (Figure 8) is lower after bonding to the glass substrate due to increased self-heating, however the breakdown voltage increases significantly. A device with L_{gd} = 18 µm shows breakdown of 1370 V and on-resistance of 4.3 mΩ•cm^2 with very low leakage current (< 10 µA/mm) (Figure 9). Three terminal breakdown voltage as a function of gate-to-drain spacing (L_{gd}) is shown in Figure 10. More than 1450 V breakdown and an on-resistance of 5.3 mΩ•cm^2 is achieved on devices with L_{gd} = 20 µm, which is beyond our power supply maximum output voltage. The breakdown voltage of these devices before the Si removal was below 600 V. These results show the tremendous potential of GaN heterostructures grown on Si for very high voltage applications, once that the Si substrate has been removed. It should be noted that the removal of the Si substrate can be integrated with the packaging of the device, which will reduce cost and increase performance.

V. Conclusions

In summary, the micromachining and processing of the Si substrate in GaN-on-Si wafers is a new tool that device engineers can use to improve the performance and increase

the flexibility of GaN electronics. This paper has described three different devices where the partial or total removal of the Si substrate is beneficial: heterogeneous on-chip integration of GaN and Si transistors, N-face GaN devices, and ultra high voltage GaN power switches. The substrate should, therefore, no longer be considered a secondary part of modern devices GaN-on-Si devices, but an integral part of the device with which achieve higher device performance in applications such as power electronics and high speed communications.

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