Stacked Switched Capacitor Energy Buffer Architecture

by

Minjie Chen

B.S., Tsinghua University (2009)

Submitted to the Department of Electrical Engineering and Computer Science,
Massachusetts Institute of Technology
in partial fulfillment of the requirements for the degree of

Master of Science in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2012

Author .....
Department of Electrical Engineering and Computer Science
December 29, 2011

Certified by .....
David J. Perreault
Professor
Thesis Supervisor

Certified by .....
Khurram K. Afridi
Visiting Associate Professor
Thesis Supervisor

Accepted by .....
Professor Leslie A. Kolodziejski
Chairman, Department Committee on Graduate Students
Department of Electrical Engineering and Computer Science

Stacked Switched Capacitor Energy Buffer Architecture

by

Minjie Chen

Submitted to the Department of Electrical Engineering and Computer Science,
Massachusetts Institute of Technology
on December 29, 2011, in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Engineering

Abstract

Electrolytic capacitors are often used for energy buffering applications, including buffering between single-phase ac and dc. While these capacitors have high energy density compared to film and ceramic capacitors, their life is limited and their reliability is a major concern. This thesis presents a series of stacked switched capacitor (SSC) energy buffer architectures which overcome this limitation while achieving comparable effective energy density without electrolytic capacitors. The architectural approach is introduced along with design and control techniques which enable this energy buffer to interface with other circuits. A prototype SSC energy buffer using film capacitors, designed for a 320 V dc bus and able to support a 135 W load has been built and tested with a power factor correction circuit.

This thesis starts with a detailed comparative study of electrolytic, film, and ceramic capacitors, then introduces the principles of SSC energy buffer architectures, and finally designs and explains the design methodologies of a prototype circuit. The experimental results successfully demonstrate the effectiveness of the approach.

Thesis Supervisor: David J. Perreault
Title: Professor

Thesis Supervisor: Khurram K. Afridi
Title: Visiting Associate Professor

Acknowledgments

I would like to gratefully acknowledge all people who contributed to this thesis.

First and foremost, I would like to express my deep and sincere gratitude to my advisors, Professor David J. Perreault and Prof. Khurram K. Afridi, for their patient guidance, and effective advices over the past two years. From them, I have gained invaluable understanding and insights of my research and my life, which has made the journey of exploring new technologies exciting and rewarding for me. Professor Perreault and Professor Afridi have both been wonderful mentors and friends of mine. They not only teach me the techniques of how to do research, but also pass me the philosophy of how to become a good person. I cannot overstate my gratitude for their support. At the same time, I hope to acknowledge and thank James Page, summer intern at MIT, for his help with collecting and analyzing film and ceramic capacitor data.

I am greatly indebted to Wei Li for his inspiration and help. Without his generous help for experimental work, the prototype of this thesis would never work. I especially want to thank Yehui Han for sharing his broad knowledge and experience on topics ranging from courses to daily life, since the very first day I arrived at MIT until now. I am also hoping to thank David Guliano, Samuel Chang and Brandon Pierquet for their insightful suggestions.

I am grateful to all the members of the group, Anthony Sagneri, Jackie Hu, Robert Pilawa, Samantha Gunter, Seungbum Lim, Wardah Inam, John Ranson, and Alex Jurkow for their friendship and support. Thank you for sharing your knowledge, and for making the entire group a sweet and productive family.

To all my friends, old and new, thank you for sharing both the ups and the downs of this process with empathy and laughter. Thanks Yao Shen for her warm support during the finalization process of this thesis.

Finally, I cannot express the full extent of my gratitude to my remote parents, Jinyu and Sulan, for their love, persistent confidence, and unwavering support in everything I do. Thank you, father and mother.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

A key consideration in any power conversion system that interfaces between dc and single-phase ac is the need for energy storage to provide buffering between the constant power desired for a dc source or load and the continuously-varying power desired for a single-phase ac system. Applications for such buffering include high-power factor rectifiers (e.g. for power supplies), solar-to-grid power conversion, and grid-connected LED lighting. Due to the requirement of maintaining good power quality, nearly sinusoidal grid current waveforms (in phase with grid voltage) are desired if a constant power is required at the load side. The single phase ac system delivers varying power at twice line frequency (i.e., 120 Hz in the US) in addition to the desired dc average power. As a result, a high-power factor converter interfacing with the single-phase grid is required to have certain amount of energy buffering capability.

This problem is illustrated in Fig. 1-1. Assuming unity power factor, the power from or to the single-phase ac system, $P_{\rm ac}(t)$, varies sinusoidally at twice-line frequency (120 Hz in the US) between zero and twice its average value, $P_{\rm avg}$, with average ac system power equaling the dc system power, $P_{\rm dc}$:

$$P_{\rm ac}(t) = P_{\rm dc}(1 - \cos(2\omega_{\rm line}t)). \tag{1.1}$$

Here $\omega_{\rm line}$ is the line's angular frequency ($2\pi \times 60$ rad/s for the US). The difference in instantaneous power between source and load must be absorbed or delivered by the

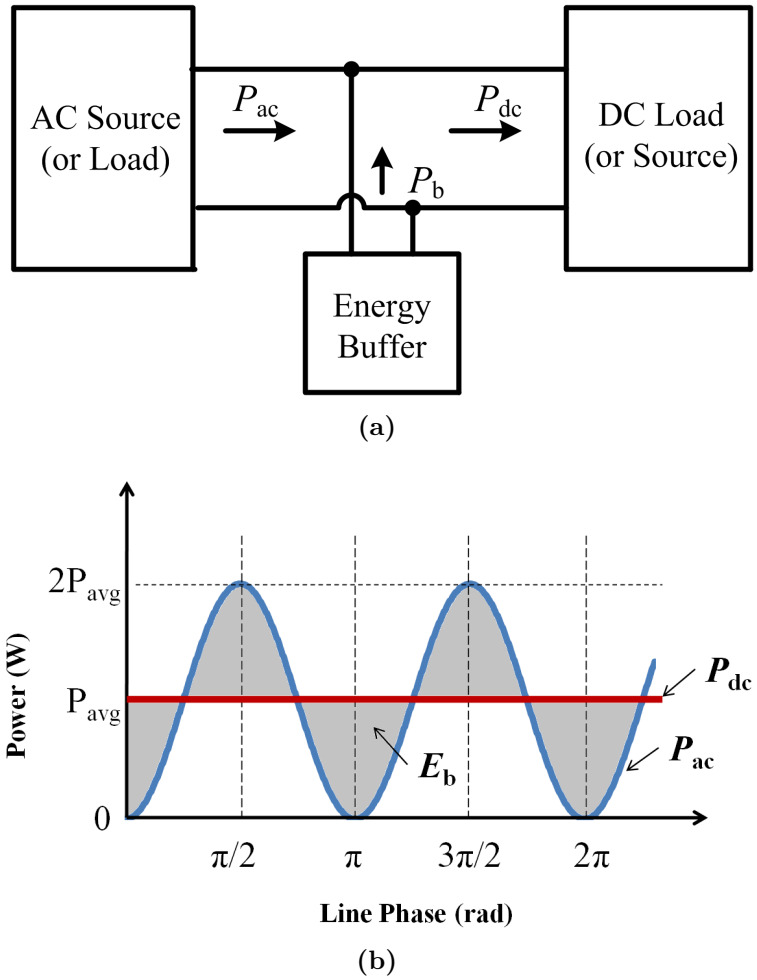


Figure 1-1: Mismatch in instantaneous power between single-phase ac, P_{ac}, and constant power dc, P_{dc}, results in the need for an energy buffer, as shown in (a), to absorb and supply the energy, E_b, indicated by the shaded area in (b).

energy buffer ($P_b(t)$):

$$P_b(t) = P_{dc} - P_{ac}(t) = P_{dc}\cos(2\omega_{line}t). \tag{1.2}$$

The peak energy that needs to be buffered, E_b, is the total energy delivered to (or extracted from) the buffer during a half-line cycle and given by:

$$E_b = \frac{P_{dc}}{\omega_{line}}. \tag{1.3}$$

Since the peak buffered energy depends only on the dc system power and the line

frequency, the volume of the energy buffer cannot be reduced simply by increasing the switching frequency of a power electronic converter interfacing the single-phase ac and dc systems.

Today, electrolytic capacitors are generally used to provide high-density energy storage for buffering. However, it is widely appreciated that despite providing the best available energy density, electrolytic capacitors represent a significant source of system lifetime and reliability problems. On the other hand, film capacitors have much higher reliability and lifetime, but considerably lower peak energy density. Hence, the development of energy buffering architectures that eliminate electrolytic capacitors while maintaining high energy storage density and high efficiency is important for future grid interface systems that have small size and high reliability.

While electrolytic capacitors provide much higher peak energy density than film capacitors (by an order of magnitude), electrolytic capacitors can only be operated over a narrow charge/discharge range (corresponding to a small voltage ripple) at 120 Hz for thermal and efficiency reasons. These considerations directly limit the energy buffering capability of electrolytic capacitors at 120 Hz. Thus, while peak energy densities of up to 0.8 J/cm^3 can typically be achieved with commercially available electrolytic capacitors at the voltage and power levels we consider, the allowable energy swing at 120 Hz yields practical energy densities that are significantly lower [1]. Film capacitors typically have peak energy densities of only about 0.1 J/cm^3. Therefore, if electrolytic capacitors are simply replaced by film capacitors (with similar voltage swing constraints), the passive volume would roughly increase by an order of magnitude, which is usually unacceptable. However, film capacitors have considerably lower series resistance compared to electrolytic capacitors which allows them to be efficiently charged and discharged over a much wider energy range. Using a large fraction of the capacitor's stored energy results in large voltage swings, which is also unacceptable in most applications. Therefore, if electrolytic capacitors are to be replaced by film capacitors while maintaining high energy density, this wide variation in capacitor voltage must somehow be curtailed.

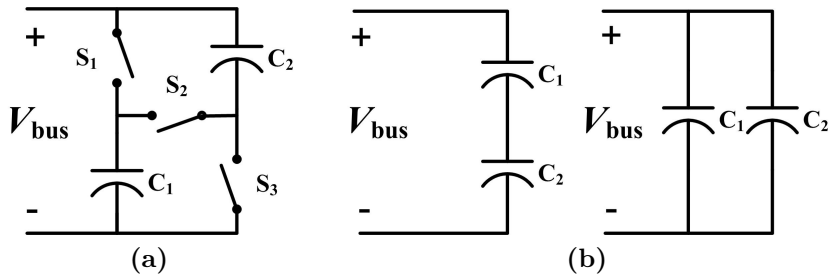


Figure 1-2: (a) A simple parallel-series switched capacitor circuit, and (b) its two configurations under alternate switch states. This circuit can constrain bus voltage to within 33.3% of nominal value while providing energy buffering capability of 93.75% of total peak energy-storage capability of the capacitors.

1.1 Past Work

In past efforts, bidirectional dc-dc converters have been employed to effectively utilize film capacitors while maintaining a desired narrow-range bus voltage [2, 3]. While this approach is flexible in terms of it use, it unfortunately leads to low buffering efficiency if high power density is to be maintained, due to losses in the dc-dc converter. Other systems have incorporated the required energy buffering as part of the operation of the grid interface power stage [4, 5, 6, 7]. This can offset a portion of the buffering loss associated with introduction of a complete additional power conversion stage, but still introduces high-frequency loss and is quite restrictive in terms of operation and application.

An alternative approach relies on switched capacitor circuits. Switched capacitor circuits that reconfigure capacitors between parallel and series combinations have been used to improve the energy utilization of ultra-capacitors [8, 9, 10]. A simple version of this parallel-series switched capacitor circuit is shown in Fig. 1-2. While this circuit has a high energy buffering ratio[1] of 93.75%, it suffers from a large voltage ripple ratio[2] of 33.3%. More complex parallel-series switched capacitor circuits which

[1]**Energy buffering ratio (Γ_b)** is defined as the ratio of the energy that can be injected and extracted from an energy buffer in one cycle to the total energy capacity of the buffer, i.e., $\Gamma_\mathrm{b} = \frac{E_\mathrm{max}-E_\mathrm{min}}{E_\mathrm{rated}}$, where E_max and E_min are the maximum and minimum values of energy stored in the energy buffer during normal operation, and E_{rated} is the total energy capacity of the energy buffer.

[2]**Voltage ripple ratio (R_v)** is defined as the ratio of the peak voltage ripple amplitude to the nominal (or average) value of the voltage, i.e., $R_v = \frac{V_\mathrm{max}-V_\mathrm{min}}{2V_\mathrm{nom}}$, where V_max, V_min and V_nom are the maximum, minimum and nominal values of the voltage, respectively [15].

achieve better voltage ripple ratio have also been developed [10]. However, they suffer from high circuit complexity when high energy utilization and small voltage ripple are required. For example, the circuit with the best performance in [10] (the 8-6-5-4-3 parallel-series switched capacitor circuit) has energy utilization of 92.09% and a voltage ripple ratio of 14.3%. However, it needs 41 switches and 120 capacitors. This makes it overly complicated for practical use.

1.2 Organization of Thesis

To overcome these weaknesses, we propose, design and prototype new switched capacitor structures Stacked switched capacitor energy buffer architecture. It has the following merits:

1. Realizing small bus voltage variation.
2. Providing high utilization of available peak energy storage capacity.
3. Achieving high efficiency.
4. Comparative simple circuits and small volume.

The remainder of this thesis is organized as follows: Chapter 2 describes the fundamentals of capacitor characteristics, including electrolytic, film and ceramic capacitors. Chapter 3 details the fundamental principles, topological implementations of this architecture and the extensions of the proposed stacked switched capacitor (SSC) energy buffer architecture. This chapter also provides design guidelines of selecting an appropriate topology for a particular application. Chapter 4 describes the design and implementation of a prototype SSC energy buffer. The experimental results from this prototype are discussed and compared with simulation in Chapter 5. Finally, Chapter 6 summarizes this thesis and identifies directions for future work. At the end of this thesis, Appendix A provides the implementation details of the prototyped 2-6 bipolar SSC energy buffer, and Appendix B provides the corresponding control codes.

Chapter 2

Capacitor Study

2.1 Introduction

Power electronic research is pushing towards higher frequency, higher efficiency and smaller volume. Passive components, like capacitors and inductors, function as energy storage device in power electronic circuits. Optimization of the passive devices is an important consideration in these systems.

Achieving better energy buffering capability of capacitors is the main focus of this thesis. There are two ways of doing this. One way is to strengthen their energy storage capability, such as developing advanced dielectric materials to make capacitors perform better. The other way is to improve the ancillary power electronics circuits, making energy storage block of the energy storage systems perform better. Explorations in this direction, such as switching converters and switched capacitor topologies, can be found in the existing literature [6, 8, 9, 10].

Developing advanced circuit topologies for energy buffering is the main goal of this thesis. A systematic comparison of the electrical properties of different kinds of capacitors is a necessary basis for achieving this. In this chapter, we study electrolytic capacitors, film capacitors, and ceramic capacitors based on datasheets of commercial capacitor products. The study verifies the motivations of replacing electrolytic capacitors with film capacitors, and provides guidance for the choice of topologies and components in the circuit implementations we explore.

2.2 Capacitor Basics

Electrolytic capacitors are the most popular type of large value capacitors, e.g. for use in line frequency energy buffering. Electrolytic capacitors are usually polarized, and it is necessary to ensure they are placed in the correct direction. They offer far greater peak energy storage density than do film capacitors. The tradeoff is much higher series resistance, resulting in a limit on rms current for thermal reasons, and an inability to withstand a reverse voltage of significant value. As a result, electrolytic capacitors are most often used as dc-link capacitors, in applications where a large capacitance is needed to reduce the ripple, but the rms current is comparatively small.

Compared to electrolytic capacitors, film capacitors have lower peak energy storage densities, but their rated rms currents are much higher than that of electrolytic capacitors. As a result, film capacitors are common choices for applications that require large currents but relatively little capacitance, such as in snubbers or resonant tanks. Film capacitors are very stable and this enables high tolerance capacitors to be made which maintains stable performance over time. In addition, they have a low dissipation factor, and their capacitance remain stable over a wide temperature range. As a result, film capacitors have earned a place as a reliable form of capacitor for use when stability is critical.

Ceramic capacitors based on different classes of dielectrics are available. Some types provide high precision and stability at low energy densities (e.g., NPO ceramics) and other classes providing high peak energy densities but with wide tolerances (e.g., X7R capacitors based on high-k dielectrics). High-k dielectric ceramic capacitors have a comparable or even higher peak energy storage density than electrolytic capacitors, and are normally used for decoupling and filtering applications where precision is not required. Their stability and tolerance are not nearly as good as those of film capacitors, and their electrical performances (capacitance and equivalent series resistance) are strongly correlated with the dc voltage applied to them.

2.3 Capacitor as an Energy Buffer

Capacitors are used for different purposes in electronic circuits, e.g. voltage stabilization, energy buffering and filtering. The focus of this thesis is on energy buffering applications. In an energy buffer, such as for interfacing a single-phase ac supply to a dc load, the power sourced/sinked from the ac side is usually sinusoidal with a dc average, to maintain a high power factor. And the power sinked/sourced at the dc side is typically constant, to maintain a small dc voltage ripple.

A capacitor is normally connected to the dc bus, whose voltage ripple is usually required to be small. Energy is periodically injected and extracted from the energy buffering capacitor. An example of this is the dc-link capacitor at the output port of the power factor correction (PFC) circuit. The peak amount of energy that a unipolar capacitor can buffer is $\frac{1}{2}CV_{\text{rated}}^2$ (assuming that the capacitance doesn't change with the applied voltage), where C is the capacitance and V_{rated} is the rated voltage of the capacitor. This energy represents the amount stored when this capacitor is charged from 0 V to V_{rated}. However, since the bus voltage usually cannot swing over a wide range, the total energy that can be injected and extracted from a capacitor cannot reach the total amount of energy that a capacitor can store. Suppose the bus voltage is V_{bus}, the capacitance is C, and the allowed voltage ripple ratio is R_v (defined in [15] as the ratio of the peak voltage ripple amplitude to the nominal (or average) value of the voltage), the total amount of energy that a capacitor can store is:

$$E_{\text{store}} = \frac{1}{2}CV_{\text{rated}}^2 \tag{2.1}$$

The energy which is buffered in this capacitor is the difference between the energy which the capacitor stores when it is fully charged and the energy which the capacitor stores when it is discharged to the lowest level, such that:

$$E_{\text{buf}} = \frac{1}{2}C(((1+\frac{1}{2}R_v)V_{\text{bus}})^2 - ((1-\frac{1}{2}R_v)V_{\text{bus}})^2) \tag{2.2}$$

For most cases, E_{buf} is only a small portion of E_{store}. For example[1], if $V_{\text{bus}} = 320$ V, $C = 26.4$ μF and $R_v = 10\%$, V_{rated} should be larger than 352 V, and the total amount of energy that this capacitor can store, E_{store}, equals to 1.64 J. And the energy that has be buffered in this capacitor, E_{buf} is 0.55 J. In this case, only 33.5% of the energy storage capability has been used for energy buffering purpose. Moreover, rms current limits for a capacitor can also constrain how much energy can be buffered over one period, with the energy buffering capability decreasing for shorter buffering periods.

When designing a circuit, the size of this energy buffering capacitor is jointly determined by the energy buffering requirements, the maximum bus voltage ripple ratio, together with the rate at which energy can be charged or extracted from the capacitor. If the energy buffering requirement is E_{buf}, and the allowed bus voltage ripple ratio is R_v (peak-to-peak), assuming that the energy charging/extracting rate meets the requirement, the buffering capacitance C, satisfies:

$$\frac{1}{2}C(((1+\frac{1}{2}R_v)V_{\text{bus}})^2 - ((1-\frac{1}{2}R_v)V_{\text{bus}})^2) \geq E_{\text{buf}} \tag{2.3}$$

Equation 2.3 can be rewritten as:

$$C \geq \frac{E_{\text{bus}}}{\frac{1}{2}(((1+\frac{1}{2}R_v)V_{\text{bus}})^2 - ((1-\frac{1}{2}R_v)V_{\text{bus}})^2)} \tag{2.4}$$

Usually on capacitor datasheets, the energy charging/extracting speed is denoted by either one or both of the following parameters: the maximum rate of change of voltage, $\mathrm{d}V/\mathrm{d}t$, and the maximum rms current, I_{rms}. It is necessary to make sure that these two parameters are larger than the actual current which will be injected into the capacitor.

2.3.1 Definitions

In this section we present four definitions to study the energy storage capability and energy buffering capability of electrolytic, film and ceramic capacitors.

[1]See Chapter 4 for the origin of this example.

Definition 1 :Energy Storage Capacity (E_{s})*:* the total amount of energy that can be stored by an energy storage device.

In general for a capacitor, its energy storage capacity is:

$$E_{\mathrm{s}} = \int_0^{V_{\mathrm{rated}}} C(v) v \, dv. \tag{2.5}$$

Here $C(v)$ is the capacitance which may be a function of capacitor voltage, V. For electrolytic and film capacitors, C, capacitance, is normally a constant, and Eq. 2.5 simplifies to $E_{\mathrm{s}} = \frac{1}{2} C V_{\mathrm{rated}}^2$. For ceramic capacitors, C varies with the voltage applied on the capacitor.

Definition 2 :Energy Storage Density (D_{s})*:* the total amount of energy that can be stored per unit volume by an energy storage device.

Suppose the volume of an energy storage device is U, and its energy storage capacity is E_{s}, then

$$D_s = \frac{E_s}{U} = \frac{\int_0^{V_{\mathrm{rated}}} C(v) v \, dv}{U}. \tag{2.6}$$

Definition 3 :Energy Buffering Capacity (E_{b})*:* the amount of effective energy that can be discharged or charged into an energy storage device at a specific charging/discharging frequency.

For a capacitor, the total energy that needs to be charged and discharged in one cycle, E_c, is determined by the total charge that has been injected, Q, which is the time integration of the current over half of the cycle, $Q = \int_0^{\frac{T}{2}} i(t) \, \mathrm{d}t$, as well as the initial voltage of the capacitor. Suppose that the capacitor needs to be discharged by $i(t)$ during half of the cycle period. Ideally, the changing of the voltage ΔV between time instance of $t = 0$ and $t = \frac{T}{2}$, satisfies:

$$\Delta V = \frac{\int_0^{\frac{T}{2}} i(t) \, \mathrm{d}t}{C}. \tag{2.7}$$

The changing of the energy stored in the capacitor is:

$$E_{\mathrm{c}} = \frac{1}{2}CV_{\mathrm{rated}}^2 - \frac{1}{2}C(V_{\mathrm{rated}} - \Delta V)^2. \tag{2.8}$$

The energy which will be consumed by the ESR in one cycle is:

$$E_{\mathrm{r}} = \int_0^T R_r i^2(t)\,\mathrm{d}t. \tag{2.9}$$

The energy that can be effectively buffered by this capacitor is:

$$E_{\mathrm{b}} = E_{\mathrm{c}} - E_{\mathrm{r}} = \frac{1}{2}CV_{\mathrm{rated}}^2 - \frac{1}{2}C(V_{\mathrm{rated}} - \Delta V)^2 - \int_0^T R_r i^2(t)\,\mathrm{d}t. \tag{2.10}$$

Definition 4 :Energy Buffering Density (D_{b})*:* Energy Buffering Density is defined as the total amount of energy that can be buffered per unit volume by an energy storage device at a specific charging/discharging frequency.

Suppose the volume of an energy storage device is U, and its Energy Buffering Capacity is E_{b}, then:

$$D_{\mathrm{b}} = \frac{E_b}{U} = \frac{\frac{1}{2}CV_{\mathrm{rated}}^2 - \frac{1}{2}C(V_{\mathrm{rated}} - \Delta V)^2 - \int_0^T R_r i^2(t)\,\mathrm{d}t}{U}. \tag{2.11}$$

Note that the **Energy Buffering Capacity**, as well as the **Energy Buffering Density** of capacitors are closely correlated with line frequency. Ideally, they should be written as $E_{\mathrm{b}}(f)$, and $D_{\mathrm{b}}(f)$. For the reason that we are mostly dealing with line frequency in this thesis, we omit the frequency part and simplify them as E_{b}, and D_{b}. In the future discussion, the default line frequency is 60 Hz, and the frequency of interest is twice the line frequency (120 Hz).

2.3.2 Analysis and Commercially Available Capacitors

Tables 2.1, 2.2 and 2.3 list the capacitors which we have selected for analysis in this study. We chose these based on appropriate considerations of the application

Table 2.1: Datasheets of sampled electrolytic capacitors.

Electrolytic Capacitor	
Part Names	**Datasheet links**
Illinois Capacitor, INC. BPS Non-Polar Radial Lead Aluminum Electrolytic Capacitors	http://www.illinoiscapacitor.com/pdf/BPS.pdf
Illinois Capacitor, INC. AXZ Low Impedance Surface Mount Aluminum Electrolytic Capacitors	http://www.illinoiscapacitor.com/pdf/AXZ.pdf
Illinois Capacitor, INC. CKE/CKH Extended Life Radial Lead Aluminum Electrolytic Capacitors	http://www.illinoiscapacitor.com/pdf/ckh_cke.pdf
Illinois Capacitor, INC. CKR/CKS General Purpose Radial Lead Aluminum Electrolytic Capacitors	http://www.illinoiscapacitor.com/pdf/catalog-index.pdf
Illinois Capacitor, INC. KXM High Frequency/High Temperature Radial Lead Aluminum Electrolytic Capacitors	http://www.illinoiscapacitor.com/pdf/catalog-index.pdf
KEMET ALS30 Series Long Life High Ripple Current Aluminum Electrolytic Capacitors	http://www.kemet.com/kemet/web/homepage/kechome.nsf/file/ALS30-31%20Series
Vishay Sprague TVA ATOM Miniature, Axial Lead Aluminum Capacitors	http://www.vishay.com/docs/42038/42038.pdf
Panasonic Radial Lead Type Series EE	http://www.panasonic.com/industrial/components/pdf/ABA0000CE113.pdf
Vishay BCcomponents Aluminum Capacitors Axial High Temperature	http://www.vishay.com/docs/28334/118aht.pdf
RLNA MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS	http://www.elna.co.jp/en/capacitor/alumi/catalog/pdf/rfs_e.pdf

of interest and commercial availability of the capacitors. From datasheets of these capacitors, we can get the rated voltage, capacitance, life time, temperature range, size, ripple current at different frequency (rms current), equivalent series resistance (ESR), equivalent series inductance (ESL) and many other parameters. This data serves as the basis of our analysis.[2]

We search for capacitors with best energy buffering capability from the above datasets. In this thesis, film capacitors with rated voltage between 600 V to 800 V, and capacitance of around 2 μF are of the main interest in the prototyped 2-6 bipolar

[2]We sincerely acknowledge Mr. James Page for his contribution of collecting and analyzing the data of ceramic capacitors.

Table 2.2: Datasheets of sampled ceramic capacitors.

Ceramic Capacitor	
Part Names	**Datasheet links**
Cornell Types GE, GH, GM, GP General Purpose Capacitors	http://www.cde.com/catalogs/G.pdf
Cornell EIA Class 2 Temperature/Frequency Stable Capacitors	http://www.cde.com/catalogs/SP.pdf
Cornell Types CE, CM, CP Disc Ceramic Capacitors	http://www.cde.com/catalogs/C.pdf
Dipped Radial Lead Mulitilayer Ceramic Capacitors	http://www.chemi-con.co.jp/e/catalog/pdf/ce-e/ce-sepa-e/ce-thd-e-110701.pdf
KEMET Surface Mount Multilayer Ceramic Chip Capacitors, KPS Series, X7R Dielectric, 10VDC-250VDC	http://www.kemet.com/kemet/web/homepage/kechome.nsf/file/KPS%20Series%20Automotive%20Grade%20Surface%20Mount%20Stacked%20MLCC%20-%20X7R%20Dielectric/$file/KEM_C1021_X7R_KPS_AUTO_SMD.pdf
United Chemi-Con Metal Cap Type Multiplayer Ceramic Capacitors	http://www.chemi-con.co.jp/e/catalog/pdf/ce-e/ce-sepa-e/ce-ntj-e-110701.pdf

Table 2.3: Datasheets of sampled film capacitors.

Film Capacitor	
Part Names	**Datasheet links**
ITW Paktron Type RA Angstor Metallized Polyester Dielectric Capacitor	http://www.paktron.com/pdf/1RA_Angstor.pdf
ITW Paktron Type CS4/CS6 Capstick Metallized Polyester Dielectric Capacitor	http://www.paktron.com/pdf/Capstick_CS4_CS6.pdf
KEMET C4DE MKP Series Low Inductance Capacitors for DC-DC Applications	http://www.kemet.com/kemet/web/homepage/kechome.nsf/file/C4DE%20Series/$file/F3303_C4DE.pdf
KEMET DC Link Film MKP Seris	http://www.mouser.com/catalog/specsheets/C4EEHNX7100BAUK.pdf
KEMET R60 MKT Series Metalized Polyester Film for Multipurpose Applications	http://www.kemet.com/kemet/web/homepage/kechome.nsf/file/R60%20Series/$file/F3301_R60.pdf
Illinois Capacitors, INC. MAB AC/Motor Run Film Capacitors	http://www.alliedelec.com/Images/Products/DataSheets/BM/ILLINOIS_CAPACITOR/Illinois-Capacitor_Actives-and-Passives_6130627.pdf
EPCOS Metallized Polypropylene Film Capacitor	http://www.epcos.com/inf/20/20/db/fc_2009/MKP_B32674_678.pdf

SSC energy buffer[3]. Based on our study, we find that a Metallized Polypropylene Film Capacitor, B32794, manufactured by EPCOS Inc has the highest energy buffering density of 75.36mJ/ cm^3. The rated voltage of this capacitor is 630 V with capacitance of 2.5 μF, and its volume is 6.583 cm^3. As described in Chapter 4, the topology that will be prototyped in this thesis needs two such capacitors placed in parallel, which makes the total passive volume 13.166 cm^3.

In comparison, as described in Chapter 4, the equivalent capacitance for energy buffering purpose of the proposed Stacked Switched Capacitor Energy Buffer is 12 $\times$ 2.2 μF=26.4 μF. We are interested in addressing how much volume our topology can save as compared with single-cap energy buffer. Thus we also need to find best electrolytic capacitor and film capacitor with capacitance of 30 μF, rated voltage larger than 352 V[4], and maximum rms current larger than 0.67 A. Based on our searching results, we found that Panasonic Radial Lead Type Series EE type A aluminum electrolytic capacitor fits best for this. Its energy buffering density is 656.5 mJ/cm^3, rated voltage is 400 V, capacitance is 33 μF, and rms current is 355 mA, with a volume of 4.021 cm^3. In order to meet the rms current requirement, a pair of such capacitors are needed to be placed in parallel, making the total passive volume becomes 8.042 cm^3.

For film capacitor, we found that a Metallized Polypropylene Film Capacitor, B32796, manufactured by EPCOS fits best. It has the highest energy buffering density of 114.02 mJ/cm^3. The rated voltage of this capacitor is 450 V with capacitance of 25 μF. Its maximum rms current is 17 A, which is larger than the needed 0.67 A, its total volume is 43.512 cm^3.

Table 2.4 shows the comparison of main specifications of these three implementations based on the information provided by the datasheet. Note that this is slightly differnt from the actual volume comparision of these three architectures which will be discussed in Chapter 5.

[3]See Chapter 4 for more details.

[4]This is the maximum voltage that will be applied to the capacitor. In our prototype, the V_{bus} is choosen to be $320V$ and V_{ripple} is choosen to be 32 V, this makes V_{rated} to be 352 V.

Table 2.4: Comparision of different energy buffering architectures in terms of energy buffering density based on the information provided by the datasheet.

	Backbone capacitor of the 2-6 bipolar SSC energy buffer	Single electrolytic capacitor	Single film capacitor
Manufacturer	EPCOS	Panasonic	EPCOS
Series Number	MKP B32794	Series EE type A	MKP B32796
Number of Cap	2	2	1
Rated Voltage (V)	630	400	450
Capacitance (μF)	2×2.5	30	25
Dielectric materials	Film	Electrolytic	Film
ESR	14.1 mΩ @ 10 kHz	4.5 Ω @120 Hz	2.9 mΩ @10 kHz
ESL (nH)	24	N/A	30
rms Current	4 A@10 kHz	710 mA@120 Hz	17 A@10 kHz
Volume (cm^3)	13.166	8.043	43.512
Energy Storage Density (mJ/cm^3)	75.36	656.5	114.02
Energy Buffering Density (mJ/cm^3)	72.91	119.48	22

2.3.3 Highest Energy Storage Density Regions

According to the definitions in Section 2.3.1, and using the `curvefit` toolbox of MATLAB, we plot the contour map of capacitance (C), rated voltage (V_{rated}) and energy storage density (E_s) of electrolytic capacitors, film capacitors, and ceramic capacitors, respectively as shown in Fig. 2-1, Fig. 2-2, Fig. 2-3 (at the end of this Chapter). Based on these figures, we have the following three findings:

1. For electrolytic capacitors (Fig. 2-1), the highest energy storage density capacitors among the dataset are found in the 400 V to 500 V, 0 μF to 0.2 μF region. The energy buffering density can reach as high as 0.8 J/cm^3. And the highest rated voltage of electrolytic capacitors surveyed is constrained at around 500 V. This indicates that electrolytic capacitors are best fit for mid voltage high capacitance applications.

2. For film capacitors (Fig. 2-2), the highest energy storage density capacitors

among those surveyed are found in the vicinity of 400 V to 800 V, 600uF to 1200uF region. However, the highest energy storage density is only around 0.1 J/cm^3. This indicates that film capacitor is best fit for high voltage decoupling applications, but it is not suited for direct use in high capacitance applications.

3. For ceramic capacitors (Fig. 2-3), the highest energy storage density capacitors surveyed are located in the 1000 V to 2000 V, 10 μF to 30 μF region. Theoretically, ceramic capacitors can reach an extremely high energy storage density. Recognizing that ceramic capacitor capacitance decays with the voltage it supports, ceramic capacitors don't fit best in energy buffering applications but can be used to provide a high-voltage support and high-frequency filtering and decoupling.

2.3.4 Comparisons among Different Types of Capacitors

Here we compare electrolytic, film and ceramic capacitors. By plotting the energy storage density and energy buffering density of different categories of capacitors as shown in Fig. 2-4, Fig. 2-5, Fig. 2-6 and Fig. 2-7 (at the end of this Chapter), we find:

1. Electrolytic capacitors generally have high energy storage density; the energy storage density of ceramic capacitors varies with voltage; and the energy storage density of film capacitor energy storage density is comparatively low.

2. The rated voltage of readily-available electrolytic capacitors only reaches as high as 500 V. This limits the utilization of electrolytic capacitors for higher voltage applications. Film and ceramic capacitors with rated voltage over 1000 V are readily available.

3. Readily available ceramic capacitors have low capacitance; readily available film capacitors cover a wide range capacitance, while electrolytic capacitors usually have large capacitance.

2.4 Summary

Characteristics of three different kinds of capacitors are studied and compared in this chapter. Electrolytic capacitors have energy storage density roughly ten times higher than that of film capacitors. On the other hand, film capacitors are distinguished by their higher rated voltage, higher rms current and lower resistance compared to that of electrolytic capacitors. This gives us the incentive to develop circuit topologies that vary the capacitor voltage across wider range, inject larger current, and make use of the bipolar charging characteristic of film capacitors to compensate for their low energy storage density. The main goal of this thesis is to develop an energy buffer using film capacitors that achieves energy buffering density comparable to that of electrolytic capacitors. The properties of ceramic capacitors were also studied in this Chapter. However, ceramic capacitors are not utilized in circuits developed in this thesis. This can be an area for the future work.

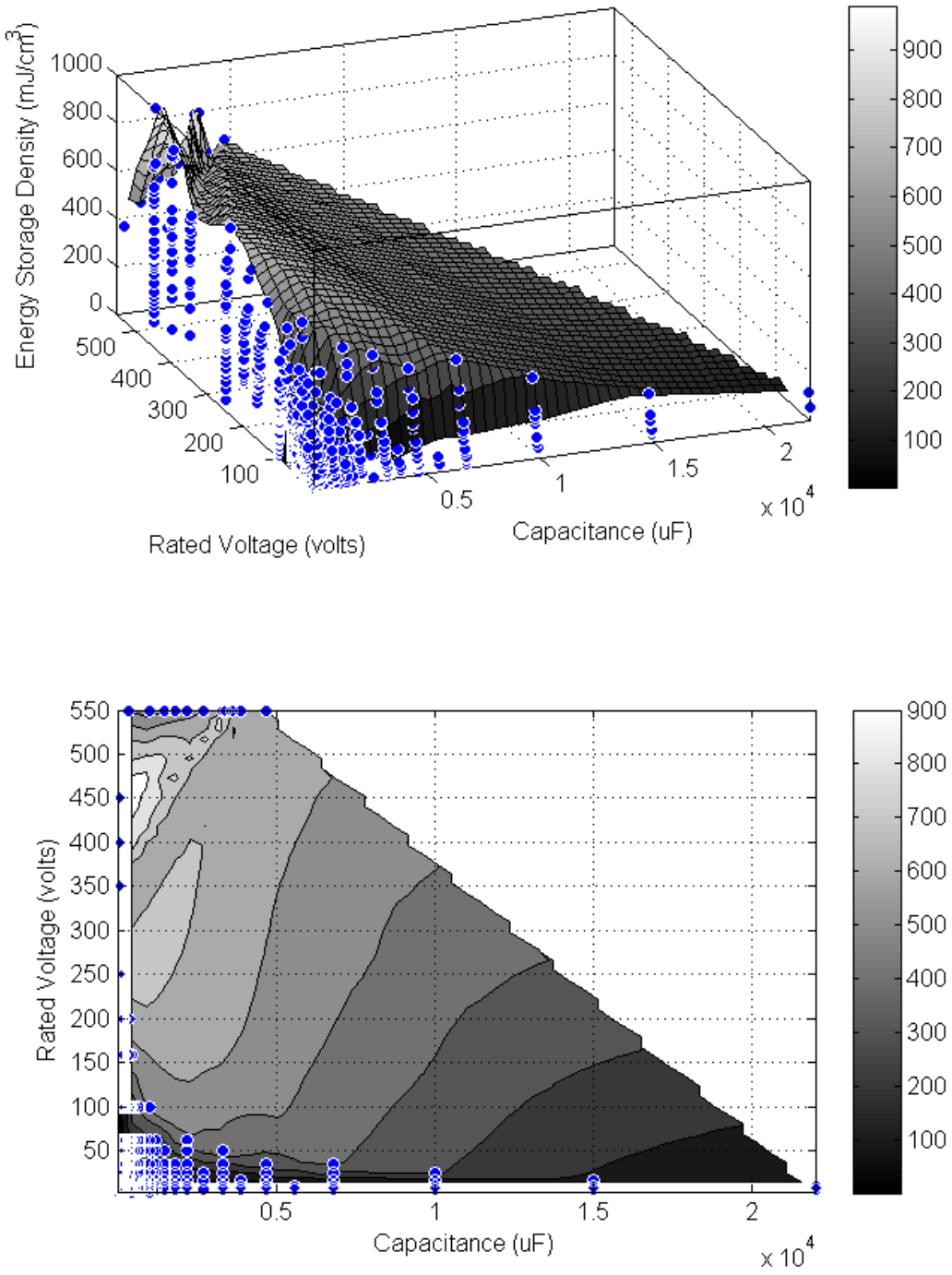


Figure 2-1: Energy storage density of electrolytic capacitors as a function of rated voltage and capacitance.

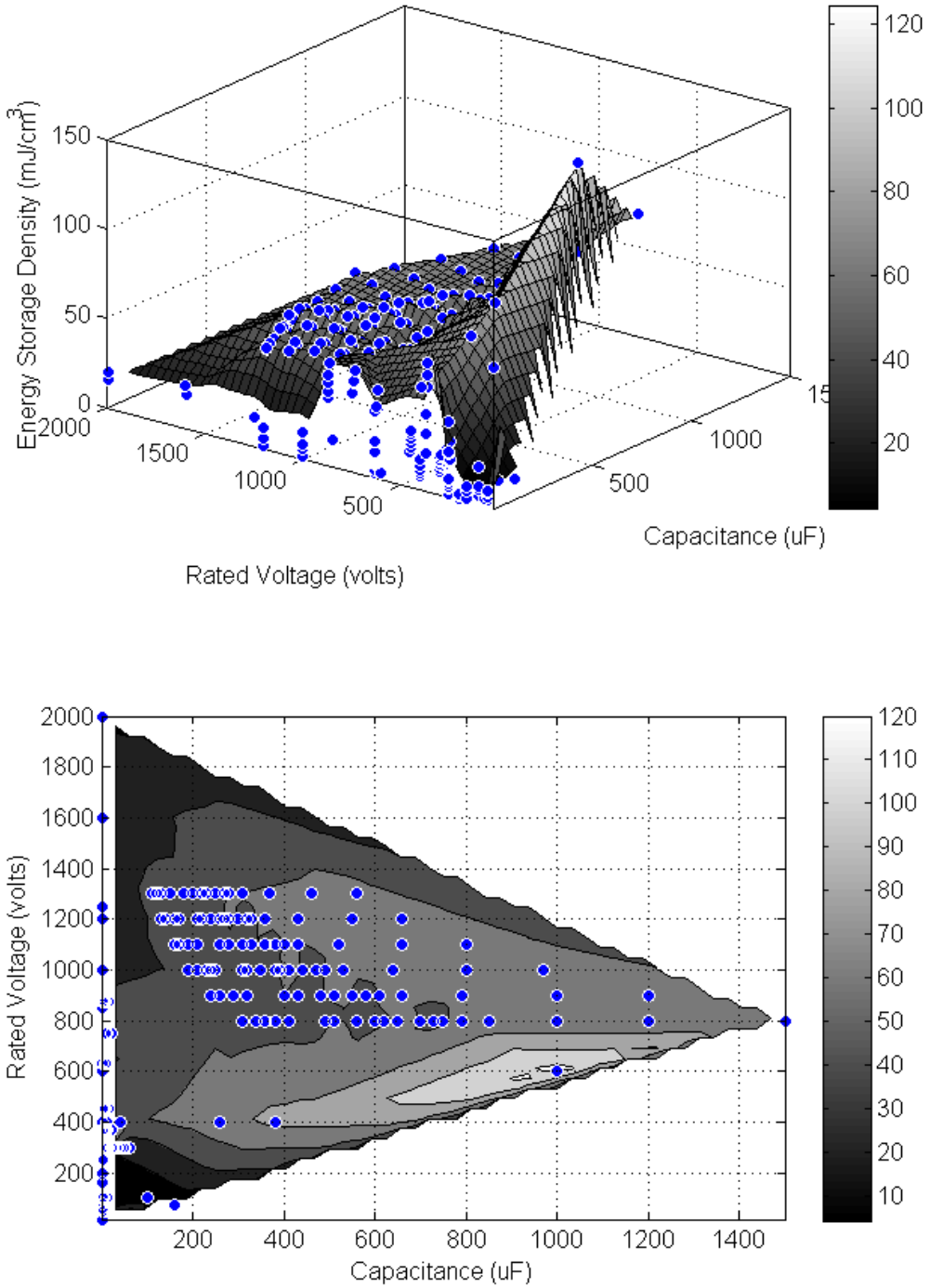


Figure 2-2: Energy storage density of film capacitors as a function of rated voltage and capacitance.

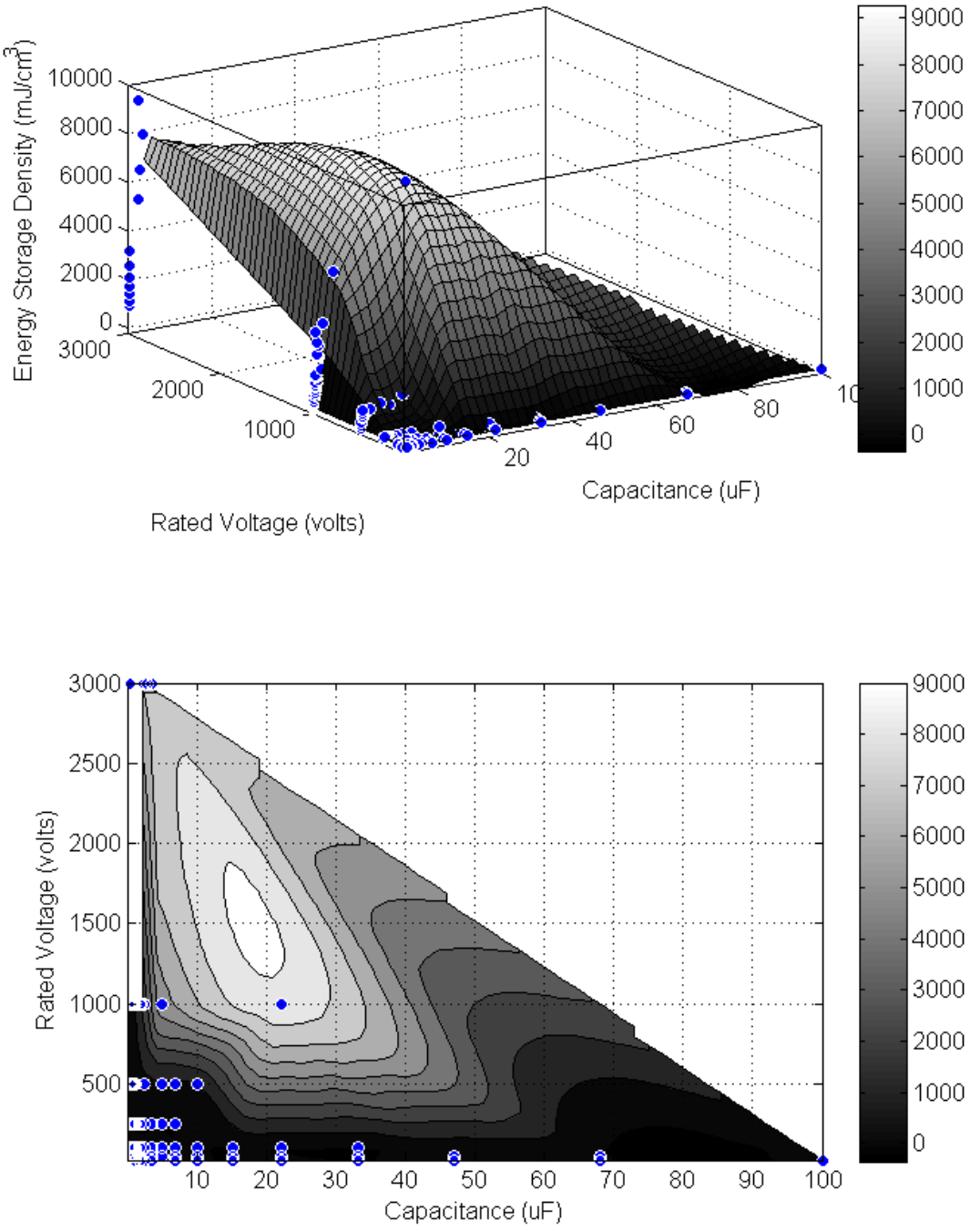


Figure 2-3: Energy storage density of ceramic capacitors as a function of rated voltage and capacitance.

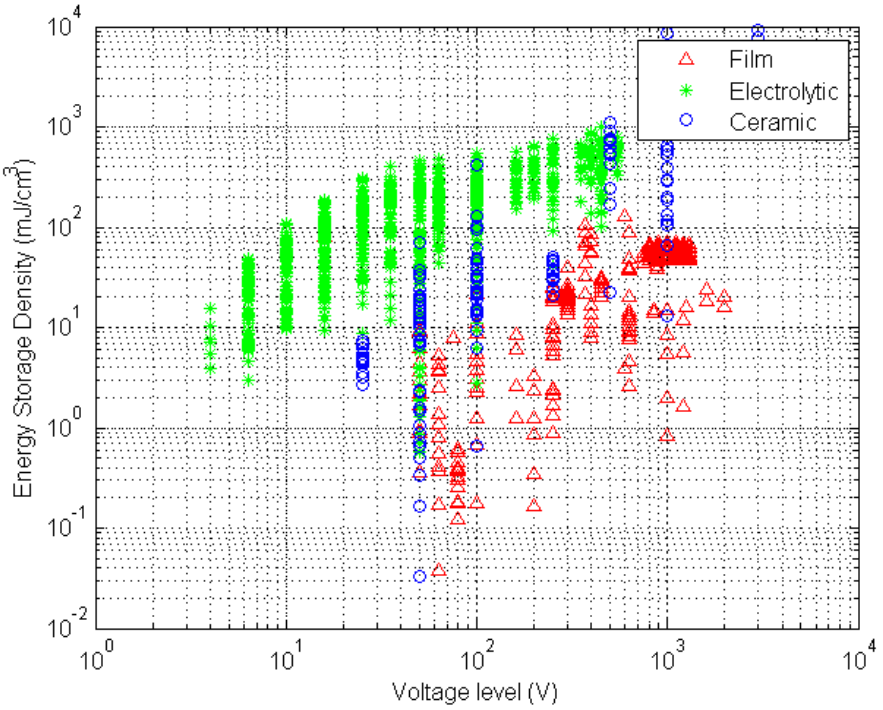


Figure 2-4: Energy storage density as a function of rated voltage.

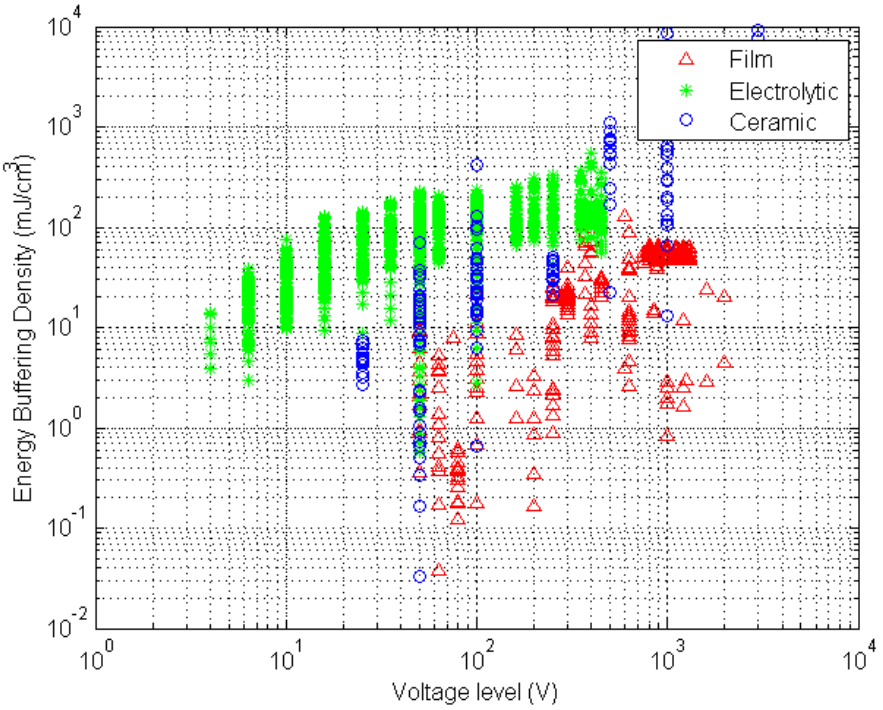


Figure 2-5: Energy buffering density as a function of rated voltage.

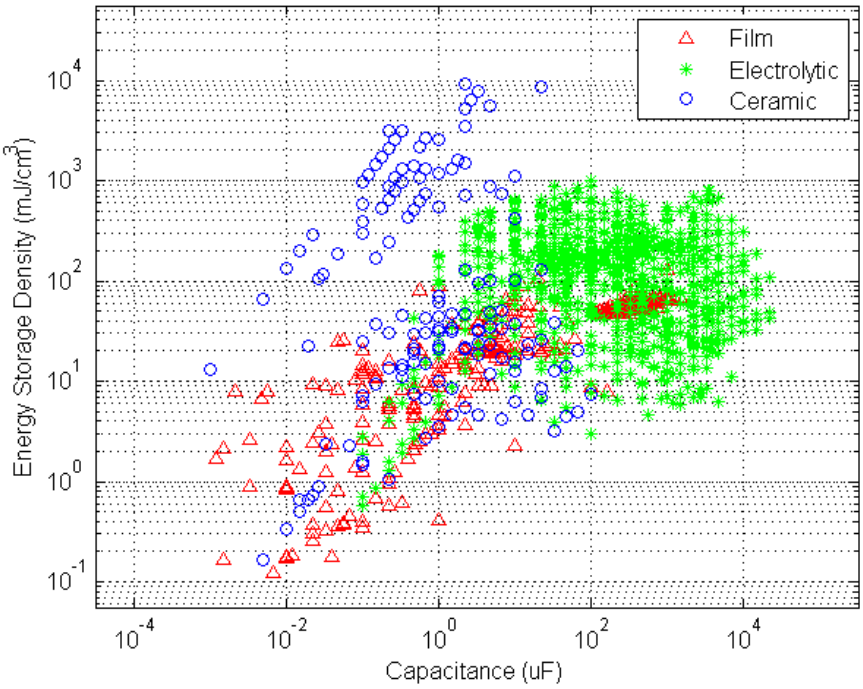


Figure 2-6: Energy storage density as a function of capacitances.

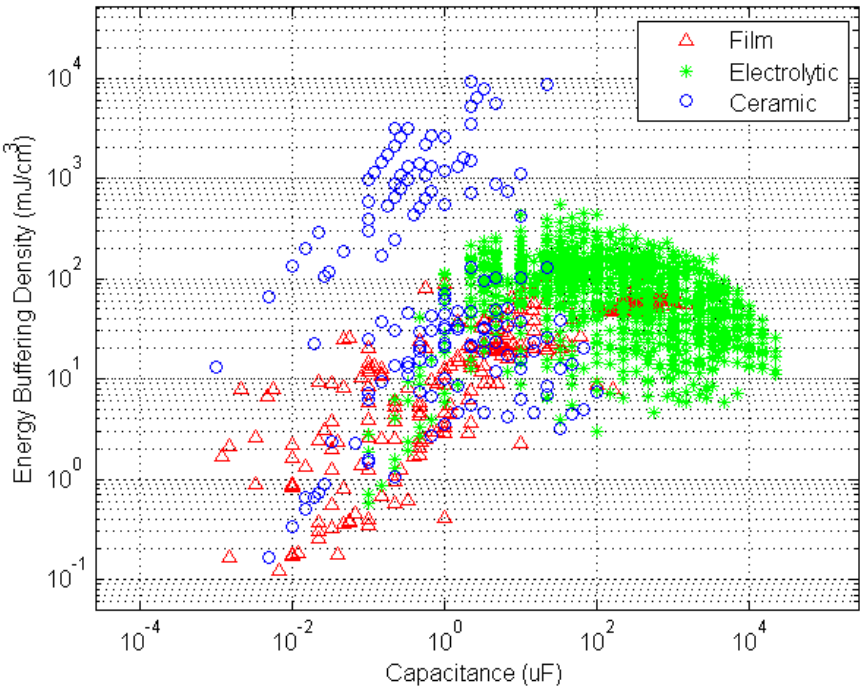


Figure 2-7: Energy buffering density as a function of capacitance.

Chapter 3

Stacked Switched Capacitor Energy Buffer Architecture

This chapter presents the general architecture and a number of embodiments of the stacked switched capacitor (SSC) energy buffer. The proposed stacked switched capacitor (SSC) energy buffer works on the principle that its individual buffer capacitors absorb and deliver energy without tightly constraining their individual terminal voltages, but maintaining a narrow range voltage at the buffer port. This enables maximum utilization of its energy storage capability.

Figure 3-1 shows the general architecture of the SSC energy buffer. It is composed of two series-connected blocks of switches and capacitors. The capacitors are of a type that can be efficiently charged and discharged over a wide voltage range (e.g., film capacitors). The switches enable dynamic reconfiguration of both the interconnection among the capacitors and their connection to the buffer port (V_{bus}). The switching network is operated such that the voltage seen at the buffer port varies only over a small range as the capacitors charge and discharge over a wide range to buffer energy. This enables high effective energy density through maximum utilization of the capacitor energy storage capability.

Efficiency of the SSC energy buffer can be extremely high because the switching network need operate at only very low (line-scale) switching frequencies, and the system can take advantage of soft charging of the energy storage capacitors to reduce

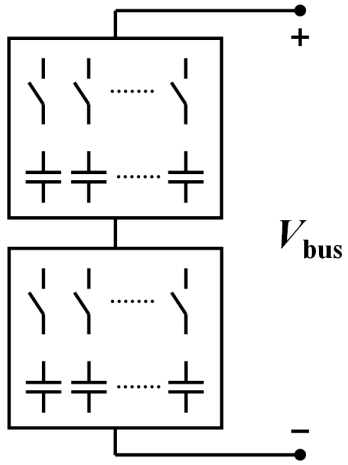


Figure 3-1: General architecture of the stacked switched capacitor (SSC) energy buffer.

loss [14]. Moreover, the proposed buffer architecture exhibits losses that scale with the amount of energy that must be buffered, such that high efficiency can be achieved across the full operating range.

3.1 Specific Embodiments

There are multiple embodiments of the proposed SSC energy buffer. We discuss some of these in the following sections. We start from simple embodiments and modify them to achieve improved performance. This also gives a sense of how these topologies were developed.

3.1.1 1-3 Unipolar Stacked Switched Capacitor (SSC) Energy Buffer

A simple embodiment of the stacked switched capacitor (SSC) energy buffer is shown in Fig. 3-2. This version constrains the bus voltage to within $\pm 1/8$ of its nominal value, while providing an energy buffering capability of more than 72% of the total peak energy-storage rating of the capacitors ($\Gamma_{\mathrm{b}} = 72\%$). Pre-charge and control circuitry is not shown. This energy buffer has one backbone capacitor (C_{11}) and three supporting capacitors (C_{21}, C_{22} and C_{23}) interconnected via four switches. The

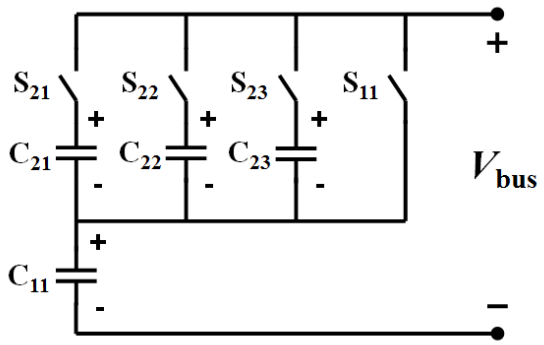


Figure 3-2: The 1-3 unipolar stacked switched capacitor (SSC) energy buffer.

four capacitors have identical capacitance, but different voltage ratings: 9/8 V_{nom} for C_{11}, 4/8 V_{nom} for C_{21}, 3/8 V_{nom} for C_{22} and 2/8 V_{nom} for C_{23}, where V_{nom} is the nominal value of the bus voltage (V_{bus}). Most of the energy is buffered by the backbone capacitor, which supports most of the voltage. And the supporting capacitors play a supporting function, by buffering small amounts of energy and provides some voltage support. A major function of the supporting capacitors is to keep the total bus voltage in the desired range as the buffer circuit charges and discharges.

Figure 3-3 shows the voltage waveforms of the four capacitors during the charging period of this energy buffer. Pre-charging circuitry (not shown in Fig. 3-2) ensures that the following initial voltages are placed on the four capacitors: 4/8 V_{nom} on C_{11}, 3/8 V_{nom} on C_{21}, 2/8 V_{nom} on C_{22} and 1/8 V_{nom} on C_{23}). Once the buffer starts to charge, S_{21} is turned on with other switches turned off. In this case, C_{11} and C_{21} are placed in series with each other and charged until the bus voltage reaches 9/8 V_{nom}, when the voltage of C_{21} reaches 4/8 V_{nom}, and the voltage of C_{11} reaches 5/8 V_{nom}. Then S_{21} is turned off, and S_{22} is turned on. After a similar period of time (assuming a constant charging current), the voltage of C_{22} reaches 3/8 V_{nom} and the voltage of C_{11} reaches 6/8 V_{nom}. Then S_{23} is turned on and C_{23} is charged. In this way, S_{21}, S_{22}, S_{23}, and S_{21} are turned on and off one after another and the voltage of C_{11}, C_{21}, C_{22}, and C_{23} finally reach 9/8 V_{nom}, 4/8 V_{nom}, 3/8 V_{nom} and 2/8 V_{nom}. Then the circuit enters the discharging period. The switches are turned on and off in reverse order during the discharging cycle. Hence, the voltage waveforms during the discharging

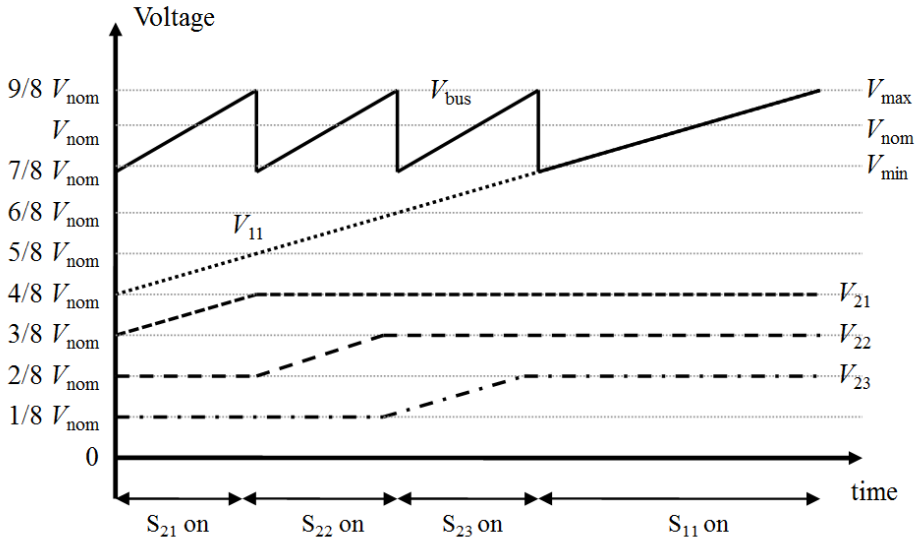


Figure 3-3: Switch states, individual capacitor voltages and resulting bus voltage for the 1-3 unipolar stacked switched capacitor energy buffer of Fig. 3-2.

period are the time reverse of those in the charging period. Note that Fig. 3-3 only shows the waveforms during the charging period.

Hence, by changing the switch configurations appropriately as energy is delivered to and from the buffer port, individual capacitors can be charged/discharged over a wide range (from their initial voltages to rated voltages), while the voltage at the buffer port is maintained within a narrow range (within $\pm 1/8$ of V_{nom}) as shown in Fig. 3-3. This structure provides energy buffering of up to 8/11 (72.7%) of the peak energy storage rating of the capacitors, while providing a buffer port voltage that remains within $\pm 1/8$ of a nominal bus voltage.

The 1-3 Unipolar SSC energy buffer can also be operated in slightly different manner as shown in Fig. 3-4. Unlike the control strategy of Fig. 3-3, this strategy gives equal time to all four switch states due to their equal capacitance. The required voltage rating of the supporting capacitors is lower than in the original design. However, with this modification the energy buffering ratio of the buffer reduces to 68.4% compared to 72.7% of the original design.

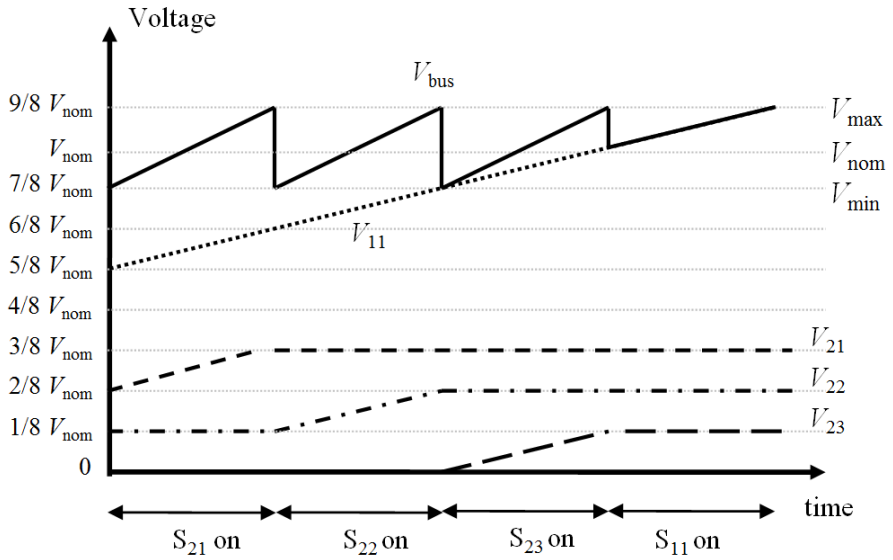


Figure 3-4: Switch states, individual capacitor voltages and resulting bus voltage for the 1-3 unipolar stacked switched capacitor energy buffer of Fig. 3-2 with a modified control.

3.1.2 1-m Unipolar Stacked Switched Capacitor (SSC) Energy Buffer

The 1-3 unipolar SSC energy buffer can be extended to achieve a smaller bus voltage variation or a higher energy buffering ratio by adding more supporting capacitors (in parallel to the three upper capacitors in Fig. 3-2) as shown in Fig. 3-5. Reducing the voltage variation of each capacitor will enable a smaller bus voltage variation, while putting more capacitors in parallel will achieve a high energy buffering ratio. The energy buffering ratio for a 1-m unipolar SSC energy buffer (i.e., one with 1 backbone capacitor of value C_1 and m supportive capacitors of equal value C_2) for R_v of voltage ripple ratio is given by:

$$\Gamma_{\mathrm{b}} = \frac{C_1((1+R_v)^2 - (1-mR_v)^2) + (mR_v)^2}{C_1(1+R_v)^2 + C_2(1+2^2+3^2+\ldots+m^2)R_v^2}. \tag{3.1}$$

Here R_v follows the definition in Chapter 1 and [15].

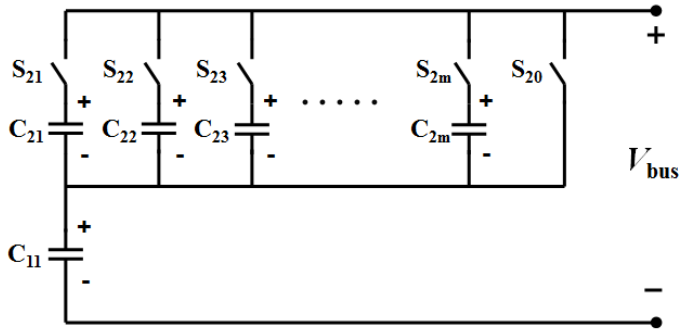


Figure 3-5: The 1-m unipolar switched stacked capacitor (SSC) energy buffer.

3.1.3 1-3 Bipolar Stacked Switched Capacitor (SSC) Energy Buffer

Film capacitors are bipolar and can be charged in either direction. We can take advantage of this fact and improve our topology and operating strategy to push the energy buffering ratio even higher. We call the improved design that takes advantage of the bipolar charging capability of film capacitors the bipolar stacked switched capacitor SSC energy buffer.

Figure 3-6 shows an example of this bipolar topology: the 1-3 bipolar SSC energy buffer. This circuit can constrain bus voltage to within $\pm 1/8$ of a nominal value, while providing an energy buffering capability of 71.1% of the total peak energy-storage rating of the capacitors. Three supporting capacitors (C_{21}, C_{22} and C_{23}) and one backbone capacitor (C_{11}) having identical capacitance values but different voltage ratings (3/8 V_{nom}, 2/8 V_{nom}, 1/8 V_{nom}, and 11/8 V_{nom} respectively) are interconnected via switches. The main difference of this topology compared to the unipolar one is that the four supporting capacitors are now put into an h-bridge to enable bi-directional charging. For operating strategy, pre-charging circuitry (not shown) ensures that specified initial voltages are placed on the capacitors (2/8 V_{nom}, 1/8 V_{nom}, 0 and 5/8 V_{nom}, respectively). At first, S_{h1} and S_{h4} are turned on and S_{h2} and S_{h3} are turned off. Then this topology operates as the unipolar buffer as described above until the voltage

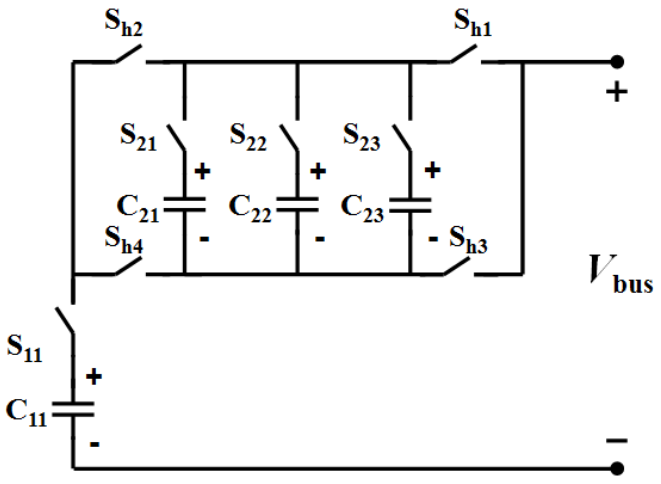


Figure 3-6: The 1-3 bipolar stacked switched capacitor (SSC) energy buffer.

of the four capacitors reaches 3/8 V_{nom}, 2/8 V_{nom}, 1/8 V_{nom}, and V_{nom}, respectively. At this time, S_{h1} and S_{h4} are turned off and S_{h2} and S_{h3} are turned on, thus the voltages that can be applied by the three supporting capacitors to the V_{bus} "stack" voltage are reversed to -3/8 V_{nom}, -2/8 V_{nom} and -1/8 V_{nom}, while the voltage applied by the backbone capacitor, C_{11}, stays the same. After a similar charging process, the three supporting capacitors are charged back to -2/8 V_{nom}, -1/8 V_{nom} and 0, with the voltage of C_{11} charged up to 11/8 V_{nom}.

When the maximum buffered energy is reached, the energy is discharged from the buffer in the time-reverse manner: the three capacitors are charged back in the other direction until 3/8 V_{nom}, 2/8 V_{nom} and 1/8 V_{nom}, the bridge switches are flipped to apply the supporting capacitor voltages to the external circuit in the positive direction, and then the supporting capacitors are sequentially discharged down to 2/8 V_{nom}, 1/8 V_{nom} and 0 again, while C_{11} is discharged all the way discharged back to 5/8 V_{nom}. The waveforms of the voltage of capacitors during a charging period are shown in Fig. 3-7.

As described above, by changing the switch configurations appropriately as energy is delivered to and from the buffer port, the individual capacitors can charge over a

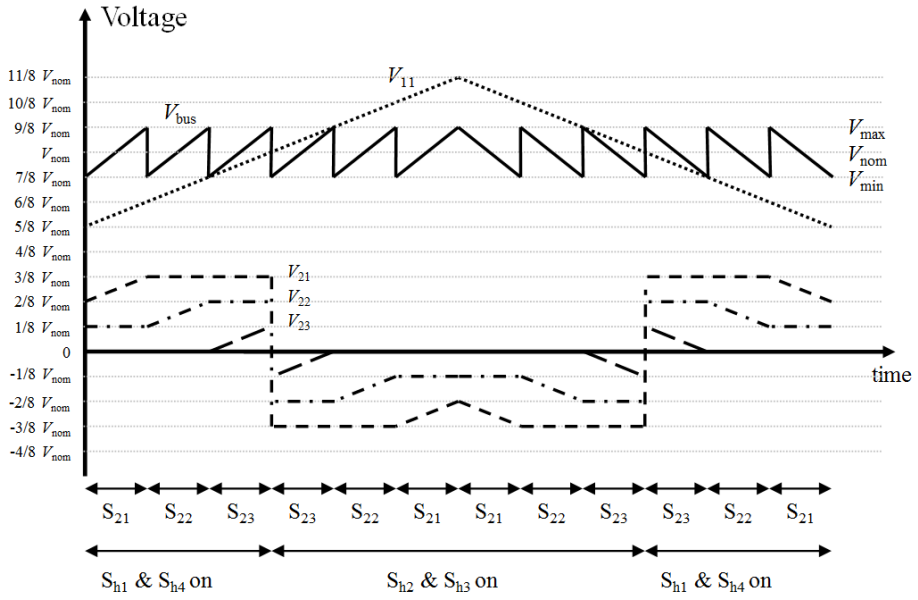


Figure 3-7: Switch states, individual capacitor voltages and resulting bus voltage for the 1-3 bipolar stacked switched capacitor energy buffer of Fig. 3-6.

wide range (from their initial voltages to rated voltages), while the voltage at the buffer port is maintained within a narrow range (within $\pm 1/8$ of V_{nom}) as shown in Fig. 3-7. This structure provides energy buffering of 65.6% of the peak energy storage rating of the capacitors, while providing a buffer port voltage that remains within $\pm 1/8$ of a nominal bus voltage. While this energy buffering ratio is lower than that of the 1-3 unipolar design, the bipolar SSC energy buffer with a slightly modified control and design methodology (as described later in this document) increases its energy buffering ratio to 71.1%.

3.1.4 2-4 Bipolar Stacked Switched Capacitor (SSC) Energy Buffer

Figure 3-8 shows the embodiment of the 2-4 bipolar SSC energy buffer, by adding one backbone capacitor and one supporting capacitor into the 1-3 bipolar SSC energy buffer. It has two backbone capacitors and six supporting capacitors. The supporting capacitors can be connected in reverse direction by reconfiguring the h-bridge. This

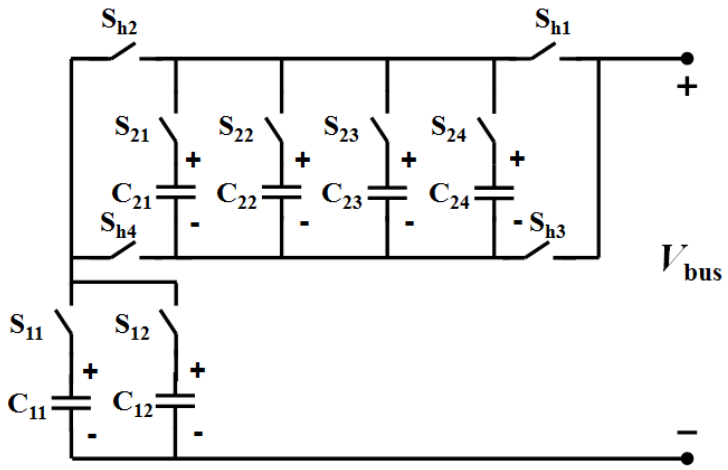


Figure 3-8: An example embodiment of the stacked switched capacitor (SSC) energy buffer architecture: the 2-4 Bipolar SSC energy buffer.

circuit can constrain bus voage to within $\pm$ 1/8 of a nominal value, while providing an energy buffering capability of 75.8% of the total peak energy storage rating of the capacitors. Pre-charge and control circuitry are not shown. The six capacitors have identical capacitance, but different voltage ratings. The two backbone capacitors, C_{11} and C_{12} have voltage ratings of 13/8 V_{nom}, where V_{nom} is the nominal value of the bus voltage (V_{bus}). The voltage rating of the four supporting capacitors is as follows: 5/8 V_{nom} for C_{21}, 4/8 V_{nom} for C_{22}, 3/8 V_{nom} for C_{23}, and 2/8 V_{nom} for C_{24}. Pre-charging circuitry (not shown in Fig. 3-8) ensures that the following initial voltages are placed on the six capacitors: 3/8 V_{nom} on C_{11}, 3/8 V_{nom} on C_{12}, 4/8 V_{nom} on C_{21}, 3/8 V_{nom} on C_{22}, 2/8 V_{nom} on C_{23}, and 1/8 V_{nom} on C_{24}.

When the energy buffer starts charging up from its minimum state of charge (as shown in Fig. 3-9), S_{h1}, S_{h4}, S_{21} and S_{11} are turned on with all the other switches turned off. In this state, C_{11} and C_{21} are connected in series and charged until the bus voltage rises from 7/8 V_{nom} to 9/8 V_{nom}. At this instant the voltage of C_{21} (V_{21}) reaches 5/8 V_{nom} and the voltage of C_{11} (V_{11}) reaches 4/8 V_{nom}. Then S_{21} is turned off and S_{22} is turned on; and the bus voltage drops back down to 7/8 V_{nom}. After a similar period of time (assuming a constant charging current) the voltage of C_{22} reaches 4/8 V_{nom} and the voltage of C_{11} reaches 5/8 V_{nom} and the bus voltage again

reaches 9/8 V_{nom}. Next S_{22} is turned off, S_{23} is turned on and C_{23} is charged. This process is repeated until C_{24} is charged. At this point the capacitor voltages are: 7/8 V_{nom} on C_{11}, 3/8 V_{nom} on C_{12}, 5/8 V_{nom} on C_{21}, 4/8 V_{nom} on C_{22}, 3/8 V_{nom} on C_{23} and 2/8 V_{nom} on C_{24}; and the bus voltage is 9/8 V_{nom}. Next S_{h4} is turned off, and S_{h2} is turned on along with S_{h3}. Hence, the bus voltage again drops to 7/8 V_{nom}. Now C_{11} can continue to charge up through the supporting capacitors (with their application voltage reversed) through a process similar to the one described above, except that the supporting capacitors are discharged in reverse order, i.e., first through C_{24}, then through C_{23}, and so on until finally through C_{21}. At this instant C_{11} is fully charged to 13/8 V_{nom} and charging of C_{12} must begin. For this the h-bridge switches are toggled (i.e., S_{h2} and S_{h3} are turned off, and S_{h1} and S_{h4} are turned on), S_{11} is turned off and S_{12} is turned on. The charging process for C_{12} is identical to the charging process for C_{11}. The switch states, the capacitor voltages (as seen from a port outside the h-bridge) and the resulting bus voltages over a complete charge and discharge cycle are shown in Fig. 3-9. The voltage waveforms are shown assuming a constant charging current.

During the discharge period, the capacitors C_{11} and C_{12} are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge period are a mirror of those in the charging period. Throughout the charging and discharging period of this energy buffer the bus voltage stays within the 7/8 V_{nom} to 9/8 V_{nom} range. Hence, the 2-4 Bipolar SSC energy buffer has a (nominal to peak) voltage ripple ratio of 12.5% of V_{nom}.

The 2-4 bipolar SSC energy buffer with voltage ripple ratio of 12.5% of nominal achieves an energy buffering ratio of 75.8%.

3.1.5 n-m Bipolar Stacked Switched Capacitor (SSC) Energy Buffer

The topology in Fig. 3-8 can be extended by adding more backbone and supporting capacitors, as shown in Fig. 3-10. Note that the capacitor that does the majority of the

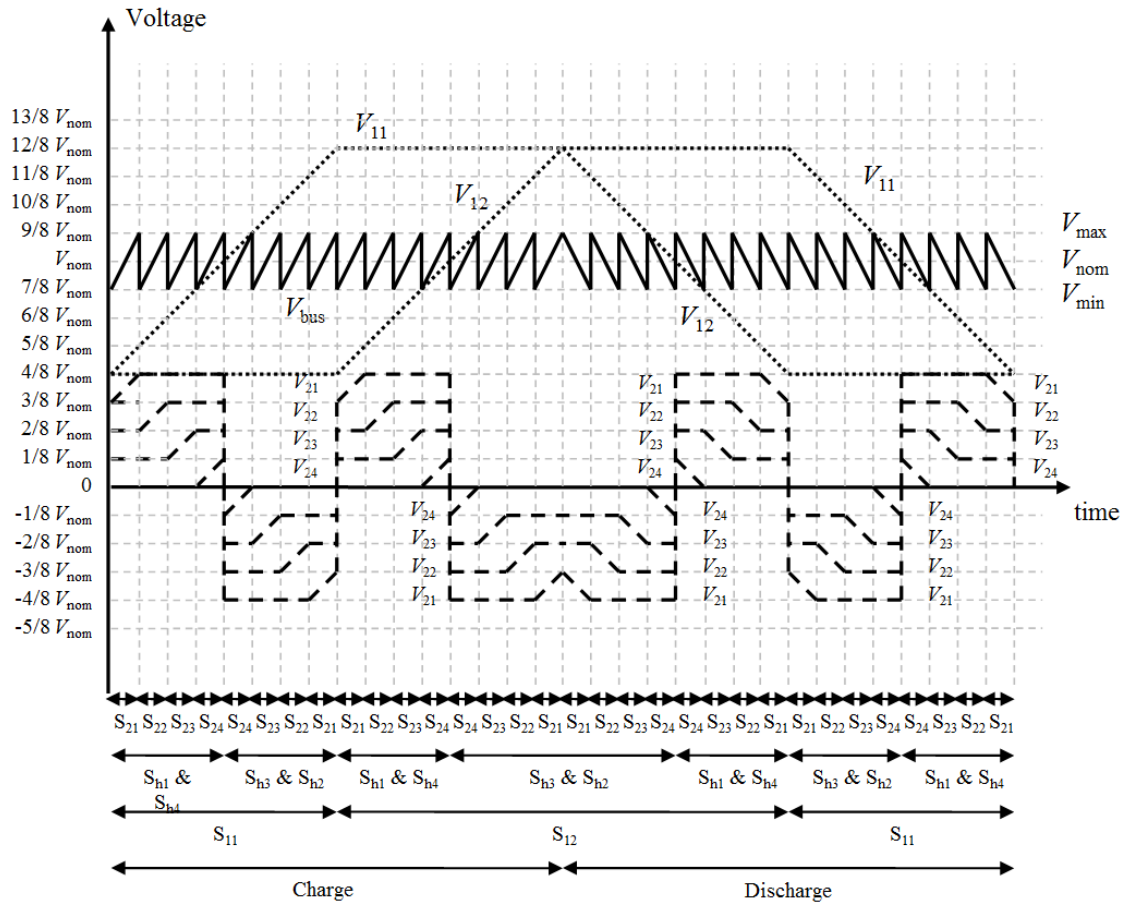


Figure 3-9: Switch states, individual capacitor voltages (as seen from a port outside of the h-bridge), and resulting bus voltage over one charging and discharging cycle of the stacked switched capacitor energy buffer of Fig. 3-8.

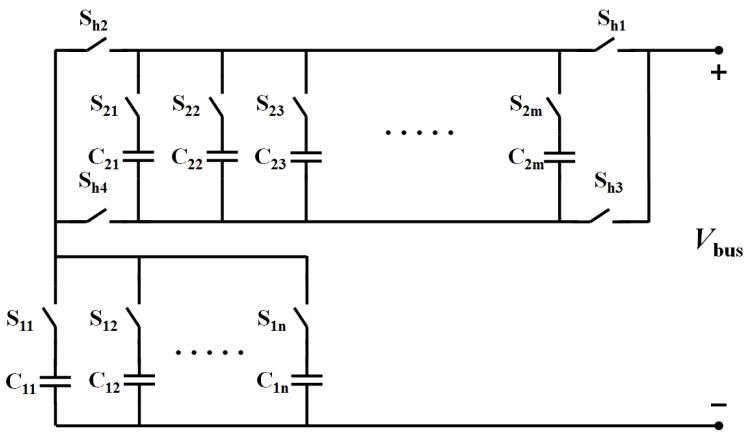


Figure 3-10: The n-m bipolar stacked switched capacitor (SSC) energy buffer. The circuit has n backbone and m supporting capacitors.

energy buffering in the circuit of Fig. 3-8 is the backbone capacitor C_{11}. Therefore, by replacing C_{11} with a parallel bank of capacitors plus selector switches, we can achieve better buffering performance. The supporting capacitors in this case have to switch at a higher switching frequency. The energy buffering ratio for this n-m bipolar SSC energy buffer (with n backbone capacitors of equal value C_1 and m supporting capacitors with equal value C_2) is given by:

$$\Gamma_{\mathrm{b}} = \frac{nC_1((1+2mR_v\frac{C_2}{C_1+C_2})^2 - (1-2mR_v\frac{C_2}{C_1+C_2})^2)}{nC_1(1+2mR_v\frac{C_2}{C_1+C_2})^2 + C_2(1+2^2+3^2+...+m^2)R_v^2}. \tag{3.2}$$

Figure 3-11 shows the variation in energy buffering ratio, Γ_{b}, (with C_1 equal to C_2) as a function of the number of backbone capacitors n and the number of supporting capacitors m for three different values of voltage ripple ratio R_v. These plots indicate that there is an optimal number of supporting capacitors that should be used for a given number of backbone capacitors in order to maximize the energy buffering ratio. Note that this optimal number of supporting capacitors depends on the value of allowed voltage ripple ratio.

These plots can be used to select the optimal number of backbone and supporting capacitors to maximize the energy buffering ratio for a given bus voltage ripple ratio. If a larger voltage ripple ratio is allowed, a high energy buffering ratio can be achieved

with fewer backbone and supporting capacitors. For a fixed number of backbone capacitors, a lower voltage ripple ratio requires a larger number of supporting capacitors if maximum energy buffering is to be achieved. However, increasing the number of supporting capacitors also increases the complexity of the circuit and the switching frequency of the switches associated with the supporting capacitors (S_{21}-S_{2m}).

3.1.6 Bipolar Stacked Switched Capacitor (SSC) Energy Buffer with Modified Control

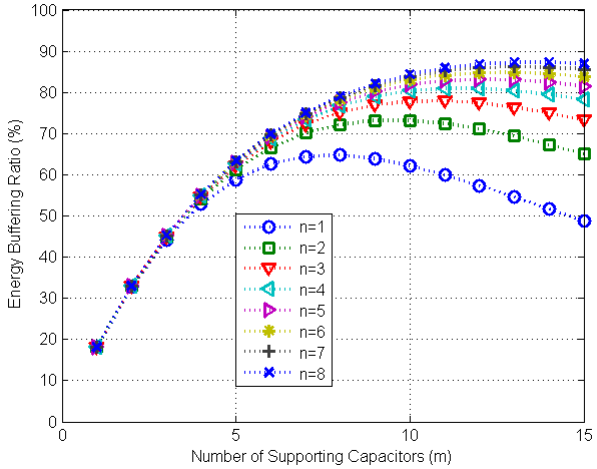
Similar to the unipolar stached switched capacitor (SSC) energy buffer, the bipolar SSC energy buffer can also be controlled in a slightly different manner. Instead of charging the backbone capacitors only in series with the supporting capacitors, a state can be introduced by turning S_{h3} and S_{h4} (or S_{h1} and S_{h2}) on at the same time in which the backbone capacitor is charged directly. An example of this control is shown in Fig. 3-12 for the 2-4 bipolar SSC energy buffer of Fig. 3-8. With this modified control, and assuming that all capacitors have the same capacitance, the expression for energy buffering ratio becomes:

$$\Gamma_b = \frac{nC_1((1+(m+1)R_v)^2 - (1-(m+1)R_v)^2)}{nC_1(1+(m+1)R_v)^2 + C_2(2^2+3^2+\ldots\ldots\ldots+(m+1)^2)R_v^2}. \tag{3.3}$$

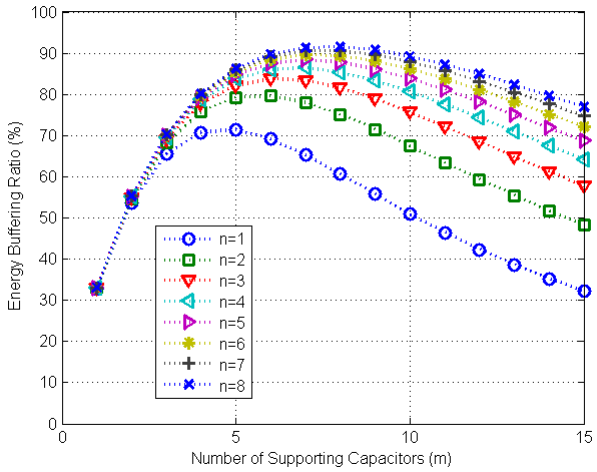
The energy buffering ratio of this 2-4 bipolar SSC energy buffer increases from 75.8% to 79.4% with this modified control methodology.

3.2 Summary

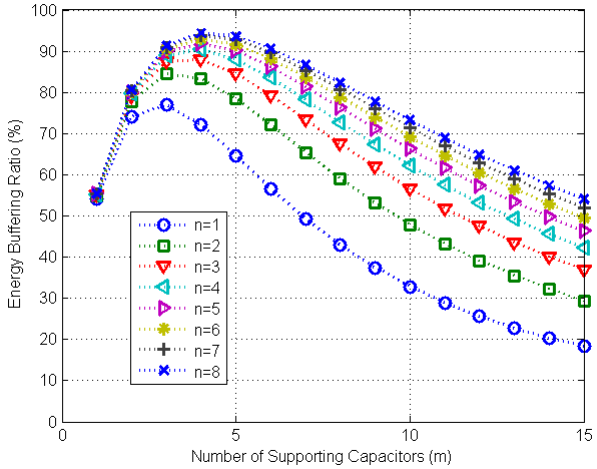
This Chapter introduces the basic structure of the stacked switched capacitor energy buffer. A series of embodiments of stacked switched capacitor energy buffer are explained in details. Table 3.1 summarizes the energy buffering ratio of different implementations operating within $\pm 1/8$ of V_{bus}. Table 3.2 is placed here as a reference for the technology described in [10]. The 8-7 Bipolar SSC energy buffer reaches an



(a) 5% of voltage ripple ratio



(b) 10% of voltage ripple ratio



(c) 20% of voltage ripple ratio

Figure 3-11: Energy buffering ratio (Γ_b) as a function of the number of backbone capacitors n and number of supporting capacitors m, with 5%, 10% and 20% of voltage ripple ratio (R_v).

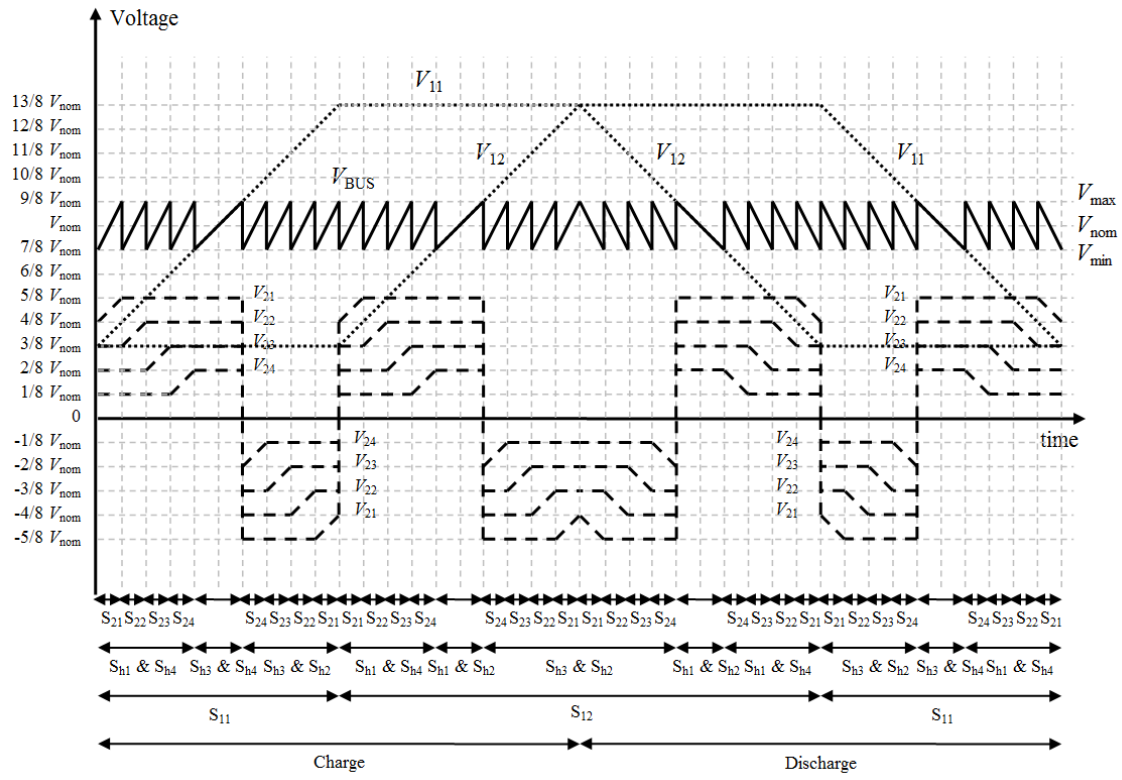


Figure 3-12: Switch states, individual capacitor voltages (as seen from a port outside of the h-bridge), and resulting bus voltage over one charging and discharging cycle of the 2-4 stacked switched capacitor energy buffer with modified control of Fig. 3-8.

Table 3.1: Comparisons of different SSC energy buffer embodiments.

SSC energy buffer	Num. of Swi.	Num.of Cap.	Γ_b	R_v
1-3 unipolar SSC	3	4	72.70%	12.5%
1-3 unipolar SSC (m)	4	4	68.40%	12.5%
1-3 bipolar SSC	7	4	65.57%	12.5%
1-3 bipolar SSC (m)	7	4	71.11%	12.5%
2-4 bipolar SSC	10	6	75.83%	12.5%
2-4 bipolar SSC (m)	10	6	79.37%	12.5%
4-6 bipolar SSC (m)	14	10	86.49%	12.5%
8-7 bipolar SSC (m)	19	15	91.59%	12.5%
16-8 bipolar SSC (m)	28	24	95.05%	12.5%
32-8 bipolar SSC (m)	44	40	97.33%	12.5%
64-9 bipolar SSC (m)	77	73	98.52%	12.5%

Table 3.2: Comparisons of other energy buffer technologies [10].

Circuit of [10]	Num. of Swi.	Num.of Cap.	Γ_b	R_v
One single capacitor	1	1	33.06%	12.5%
2-1 parallel-seris	3	3	93.75%	33.5%
4-2-1 parallel-seris	9	9	98.44%	33.5%
8-4-2-1 parallel-seris	21	8	99.61%	33.5%
6-4-3-2 parallel-series	22	12	95.06%	20%
4-3 parallel-seris	7	12	68.36%	14.3%
5-4-3 parallel-series	16	60	79.75%	14.3%
6-5-4-3 parallel-series	27	60	85.94%	14.3%
8-6-5-4-3 parallel-series	41	120	92.09%	14.3%

energy buffering ratio of 91.59% with only 19 switches and 15 capacitors for 12.5% of R_v, which is significantly simpler than the 8-6-5-4-3 parallel-series implementation introduced in [10].

In general, energy buffering ratio approaches one as the circuit complexity increases. However, increasing circuit complexity increases cost, risk of failure, and brings higher switching losses. Circuit designers should choose appropriate topologies to reach a balance between circuit complexity and energy buffering ratio. This chapter provides theoretical basis for the implementation of this SSC energy buffer in Chapter 4.

Chapter 4

Prototype Design

This chapter focuses on the design and simulation considerations of this stacked switched capacitor (SSC) energy buffer prototype, and leave the simulation and experimental results of this prototype described in Chapter 5.

The prototype is designed as the energy buffer for a power factor correction (PFC) front-end of a two-stage single-phase ac to dc power converter as shown in Fig. 4-1. The SSC energy buffer replaces the electrolytic capacitor normally connected at the output of the PFC. To simplify our implementation, a load resistor is used in place of the second-stage dc-dc converter. The SSC energy buffer is designed to meet a 10% bus voltage ripple ratio requirement on a 320 V dc bus with a maximum load of 135 W, as listed in Table 4.1.

The PFC used for this prototype is a 400 W evaluation board from STMicroelectronics that uses their transition-mode PFC controller (L6562A). This controller operates the boost PFC at the boundary between continuous and discontinuous conduction mode by adjusting the switching frequency. The evaluation board has a

Table 4.1: Design specifications for the 2-6 bipolar SSC energy buffer prototype.

Design Specification	**Value**
Maximum load power ($P_{\text{load(max)}}$)	135 W
Bus voltage (V_{bus})	320 V
Voltage ripple ratio (R_v)	10%

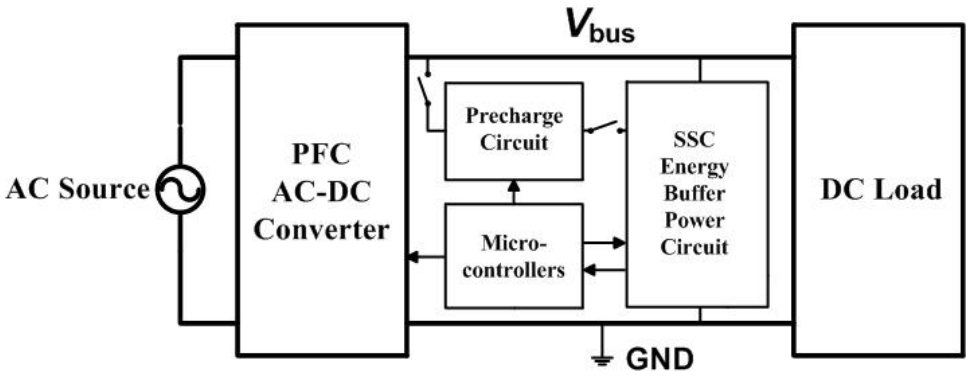


Figure 4-1: Block diagram of the prototype setup consisting of a power factor correction (PFC) ac-dc converter, a dc load and the prototyped SSC energy buffer. The prototyped SSC energy buffer consists of: the SSC energy buffer power circuit, the precharge circuit, and the control unit.

330 μF, 450 V electrolytic capacitor at the output of the PFC, and according to the PFC datasheet can maintain a voltage ripple ratio of 2.5%, while supplying a 400 W load at a bus voltage of 400 V. We have experimentally verified that a 40 μF electrolytic capacitor is sufficient to support 135 W of output power with 10% voltage ripple ratio. The total volume of the 40 μF, 450 V electrolytic capacitor used for this verification is approximately 9 cm^3.

The energy buffer that replaces this electrolytic capacitor consists of three functional blocks: the energy buffer power circuit, the precharge circuit and the control unit, as shown in Fig. 4-1. In addition, the energy buffer needs to provide a feedback signal to the PFC for its proper operation. The design of each of these four elements is discussed below.

4.1 Energy Buffer Power Circuit

As shown in Fig. 3-11(b), to achieve a voltage ripple ratio of 10% with a two-backbone-capacitor (n=2) bipolar SSC energy buffer, the optimal number of supporting capacitors is six, (i.e., m=6). Hence in the prototype, the electrolytic capacitor is replaced by a 2-6 bipolar SSC energy buffer. Note that for an R_v of 10%, with 8 backbone and 8 supporting capacitors, an energy buffering ratio of 91.6% can be achieved. Hence, the SSE energy buffer achieves performance similar to the 8-6-5-4-3 parallel-series

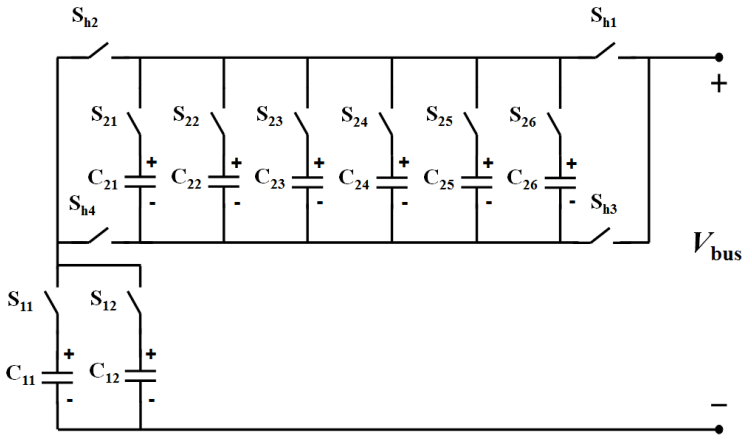


Figure 4-2: The prototyped 2-6 bipolar SSC energy buffer.

switched capacitor circuit of [10] with only 16 capacitors and 20 switches instead of 120 capacitors and 41 switches.

To meet the 10% voltage ripple requirement at the 320 V bus voltage and the 135 W output power level, the eight capacitors of the SSC energy buffer have to be 2.2 μF each. The required voltage rating of these film capacitors is different and ranges from 32 V to 512 V as discussed in Chapter 3. However, for simplicity and to provide adequate safety margin, 700 V film capacitors are used as the two backbone capacitors and 250 V capacitors are used as the six supporting capacitors. All the switches are implemented using silicon power MOSFETs. Switches S_{11} S_{12}, S_{21}, S_{22}, S_{23}, S_{24}, S_{25} and S_{26} are implemented with reverse voltage blocking capability. The schematic of this 2-6 bipolar SSC energy buffer is shown in Fig. 4-3.

This topology has two backbone capacitors, C_{11} and C_{12}; six supporting capacitors, C_{21}, C_{22}, C_{23}, C_{24}, C_{25}, and C_{26}; and twelve switches, S_{11}, S_{12}, S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{26}, S_{h1}, S_{h2}, S_{h3}, and S_{h4}. This circuit can keep the bus voltage ripple within 10% of nominal value when designed and operated in the manner described below.

The eight capacitors are chosen to have identical capacitance, but different voltage ratings. The two backbone capacitors, C_{11} and C_{12}, have voltage rating of $1.6V_{\mathrm{nom}}$, where V_{nom} is the nominal value of the bus voltage (V_{bus}). The voltage rating of the six supporting capacitors is as follows: $0.6V_{\mathrm{nom}}$ for C_{21}, $0.5V_{\mathrm{nom}}$ for C_{22}, $0.4V_{\mathrm{nom}}$

for C_{23}, $0.3V_{\text{nom}}$ for C_{24}, $0.2V_{\text{nom}}$ for C_{25} and $0.1V_{\text{nom}}$ for C_{26}. A precharge circuit (not shown in Fig. 4-3, but discussed in section 4.2) ensures that the following initial voltages are placed on the eight capacitors: $0.4V_{\text{nom}}$ on C_{11}, $0.4V_{\text{nom}}$ on C_{12}, $0.5V_{\text{nom}}$ on C_{21}, $0.4V_{\text{nom}}$ on C_{22}, $0.3V_{\text{nom}}$ on C_{23}, $0.2V_{\text{nom}}$ on C_{24}, $0.1V_{\text{nom}}$ on C_{25}, and 0 V on C_{26}.

Figure 4-4 shows the switch states, the capacitor voltages and the resulting bus voltage for the 2-6 bipolar SSC energy buffer over a complete charge and discharge cycle. When the energy buffer starts charging up from its minimum state of charge, S_{h1}, S_{h4}, S_{21} and S_{11} are turned on with all the other switches turned off. In this state, C_{11} and C_{21} are connected in series and charged until the bus voltage rises from $0.9V_{\text{nom}}$ to $1.1V_{\text{nom}}$. At this instant the voltage of C_{21} (V_{21}) reaches $0.6V_{\text{nom}}$ and the voltage of C_{11} (V_{11}) reaches $0.5V_{\text{nom}}$. Then S_{21} is turned off and S_{22} is turned on; and the bus voltage drops back down to $0.9V_{\text{nom}}$. Then as the charging continues, the voltage of C_{22} rises to $0.5V_{\text{nom}}$ and the voltage of C_{11} reaches $0.6V_{\text{nom}}$ and the bus voltage again reaches $1.1V_{\text{nom}}$. Next S_{22} is turned off, S_{23} is turned on and C_{23} is charged. This process is repeated until C_{26} is charged. At this stage all the supporting capacitors are at their maximum voltage; the voltage of the backbone capacitors is: V_{nom} on C_{11} and $0.4V_{\text{nom}}$ on C_{12}; and the bus voltage is $1.1V_{\text{nom}}$. Next S_{h1} and S_{h4} are turned off, and S_{h3} and S_{h2} are turned on. This connects C_{26}, and the other supporting capacitors, in reverse orientation with C_{11} and the bus voltage again drops to $0.9V_{\text{nom}}$. Now C_{11} can continue to charge up through the now reverse-connected supporting capacitors through a process similar to the one described above, except that the supporting capacitors are discharged in reverse order, i.e., first through C_{26}, then through C_{25}, and so on until finally through C_{21}. At this stage C_{11} is fully charged to $1.6V_{\text{nom}}$ and charging of C_{12} must begin. For this the h-bridge switches are again toggled (i.e., S_{h3} and S_{h2} are turned off, and S_{h1} and S_{h4} are turned on), S_{11} is turned off and S_{12} is turned on. The charging process for C_{12} is identical to the charging process for C_{11}, as shown in Fig. 4-4. During the discharge period, the capacitors C_{11} and C_{12} are discharged one at a time through a process that is the reverse of the charging process. Hence, the voltage waveforms during the discharge

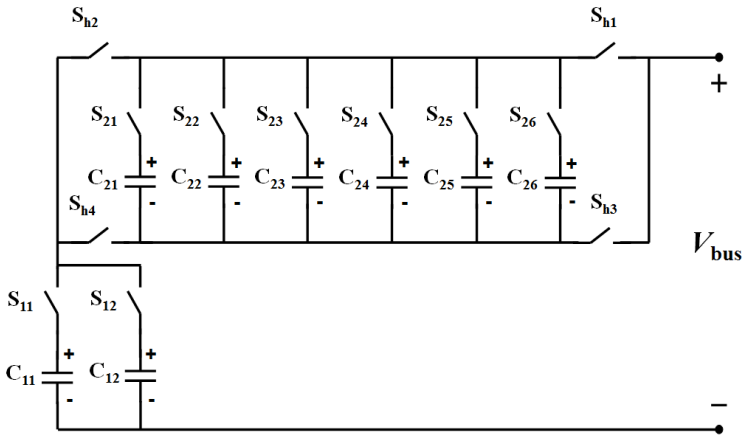


Figure 4-3: An example embodiment of the SSC energy buffer architecture: the 2-6 bipolar SSC energy buffer. This circuit has two backbone capacitors C_{11} and C_{12} and six supporting capacitors C_{21} to C_{26} and twelve switches. Precharge and control circuits are not shown.

period are a mirror of those in the charging period.

Throughout the charging and discharging period of this energy buffer, the bus voltage stays within the range $0.9V_{\text{nom}}$-$1.1V_{\text{nom}}$. Hence, the 2-6 bipolar SSC energy buffer operating in this manner has a bus voltage ripple ratio (R_v) of 10%. Furthermore, it has an energy buffering ratio (Γ_{b}) of 79.6%.

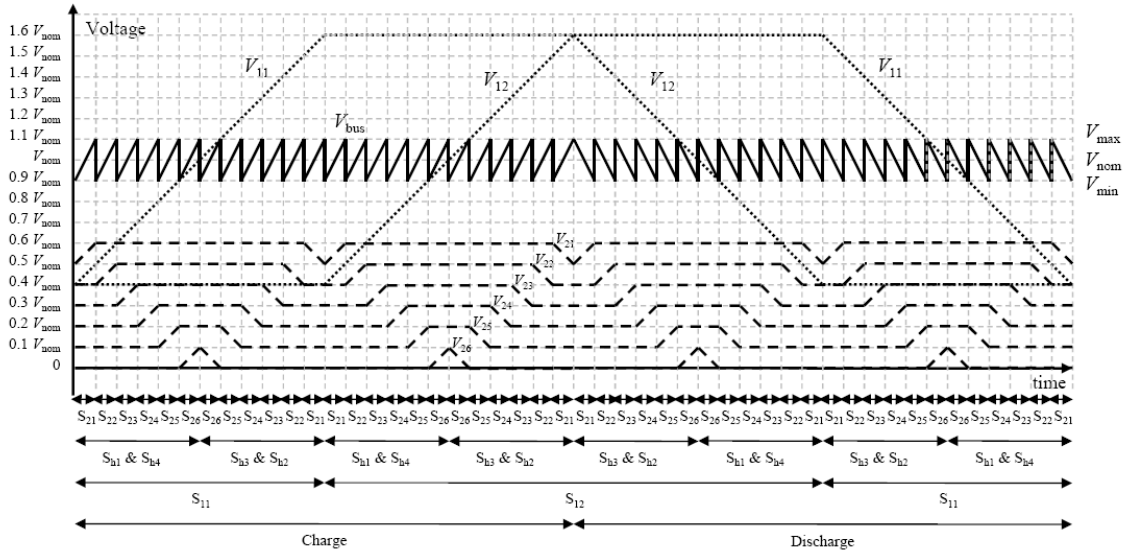


Figure 4-4: Switch states, individual capacitor voltages, and resulting bus voltage over a charge and discharge cycle of the 2-6 bipolar SSC energy buffer of Fig. 4-3.

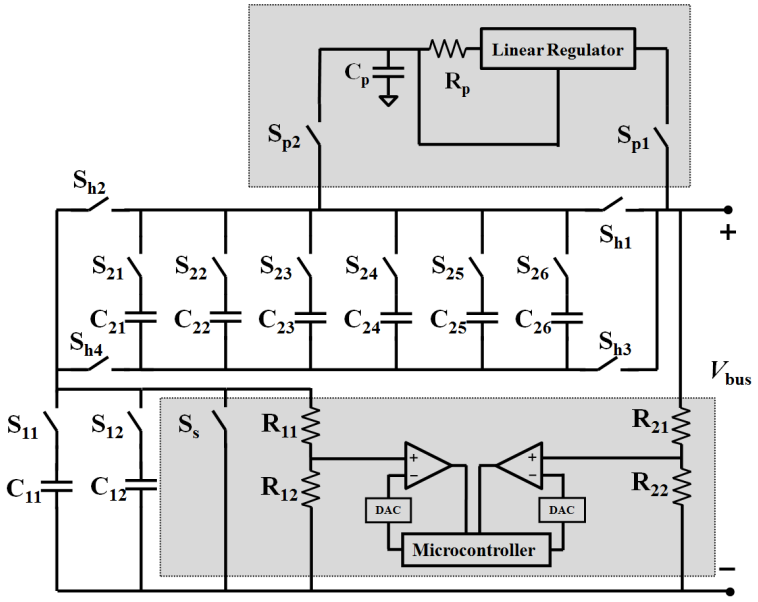


Figure 4-5: Precharge circuit (shaded regions) for the 2-6 bipolar SSC energy buffer.

4.2 Precharge Circuit

An important part of the SSC energy buffer is the precharge circuit. When the system starts, the precharge circuit draws power from the PFC to charge the individual capacitors of the energy buffer to the desired initial voltage levels. The precharge circuit designed here uses a linear regulator operated as a current source as shown in Fig. 4-5. The linear regulator used is Supertex LR8 with a maximum output current of 20 mA. The linear regulator can be disconnected from the energy buffer power circuit by two isolating switches S_{p1} and S_{p2}.

The precharge circuit is controlled by an ATMEL ATmega2560 microcontroller. The flow chart of the precharge control is shown in Fig. 4-6. A scaled down version of the voltage across each capacitor is compared with a specified reference provided by the microcontroller through a digital to analog converter (DAC). The results of the comparison are fed back to the microcontroller to trigger an interrupt.

During precharge, the microcontroller turns the switches on or off appropriately to connect the current source to the capacitor that needs to be charged. The states (on or off) of the switches for charging a particular capacitor during the precharge period

Table 4.2: State of the switches during precharge of each of the eight capacitors of the 2-6 bipolar SSC energy buffer. Blank cell indicates the switch is off.

	$\mathbf{C_{11}}$	$\mathbf{C_{12}}$	$\mathbf{C_{21}}$	$\mathbf{C_{22}}$	$\mathbf{C_{23}}$	$\mathbf{C_{24}}$	$\mathbf{C_{25}}$	$\mathbf{C_{26}}$
$\mathbf{S_{11}}$	on							
$\mathbf{S_{12}}$		on						
$\mathbf{S_{21}}$			on					
$\mathbf{S_{22}}$				on				
$\mathbf{S_{23}}$					on			
$\mathbf{S_{24}}$						on		
$\mathbf{S_{25}}$							on	
$\mathbf{S_{26}}$								on
$\mathbf{S_{h1}}$								
$\mathbf{S_{h2}}$	on	on						
$\mathbf{S_{h3}}$								
$\mathbf{S_{h4}}$			on	on	on	on	on	on
$\mathbf{S_{p1}}$	on	on	on	on	on	on	on	on
$\mathbf{S_{p2}}$	on	on	on	on	on	on	on	on
$\mathbf{S_s}$			on	on	on	on	on	on

are shown in Table 4.2. First S_{p1}, S_{p2}, S_{21}, S_{h4} and S_{s} are turned on, and all the other switches are turned off to charge C_{21}. The microcontroller senses the voltage of C_{21} (through the voltage divider formed by R_{21} and R_{22}) and compares it with the specified precharge voltage ($0.5V_{\mathrm{nom}}$=160 V). Once the voltage of C_{21} reaches 160V, S_{21} is turned off and S_{22} is turned on to charge C_{22} to its specified precharge level. Similarly, C_{23}, C_{24}, C_{25} and C_{26} are charged one at a time to their designed initial level. Once C_{26} is charged, S_{26}, S_{h4} and S_{s} are turned off, and S_{h2} and S_{11} are turned on to charge C_{11}. Now the microcontroller senses the voltage of C_{11} (through the voltage divider formed by R_{11} and R_{12}) and compares it with the specified precharge voltage ($0.4V_{\mathrm{nom}}$=128 V). Once the voltage of C_{11} is larger than 128 V, S_{11} is turned off and S_{12} is turned on to charge C_{12}. Once all the capacitors are precharged, the precharge circuit is disconnected from the SSC energy buffer by switches S_{p1} and S_{p2}, and the energy buffer enters normal operation.

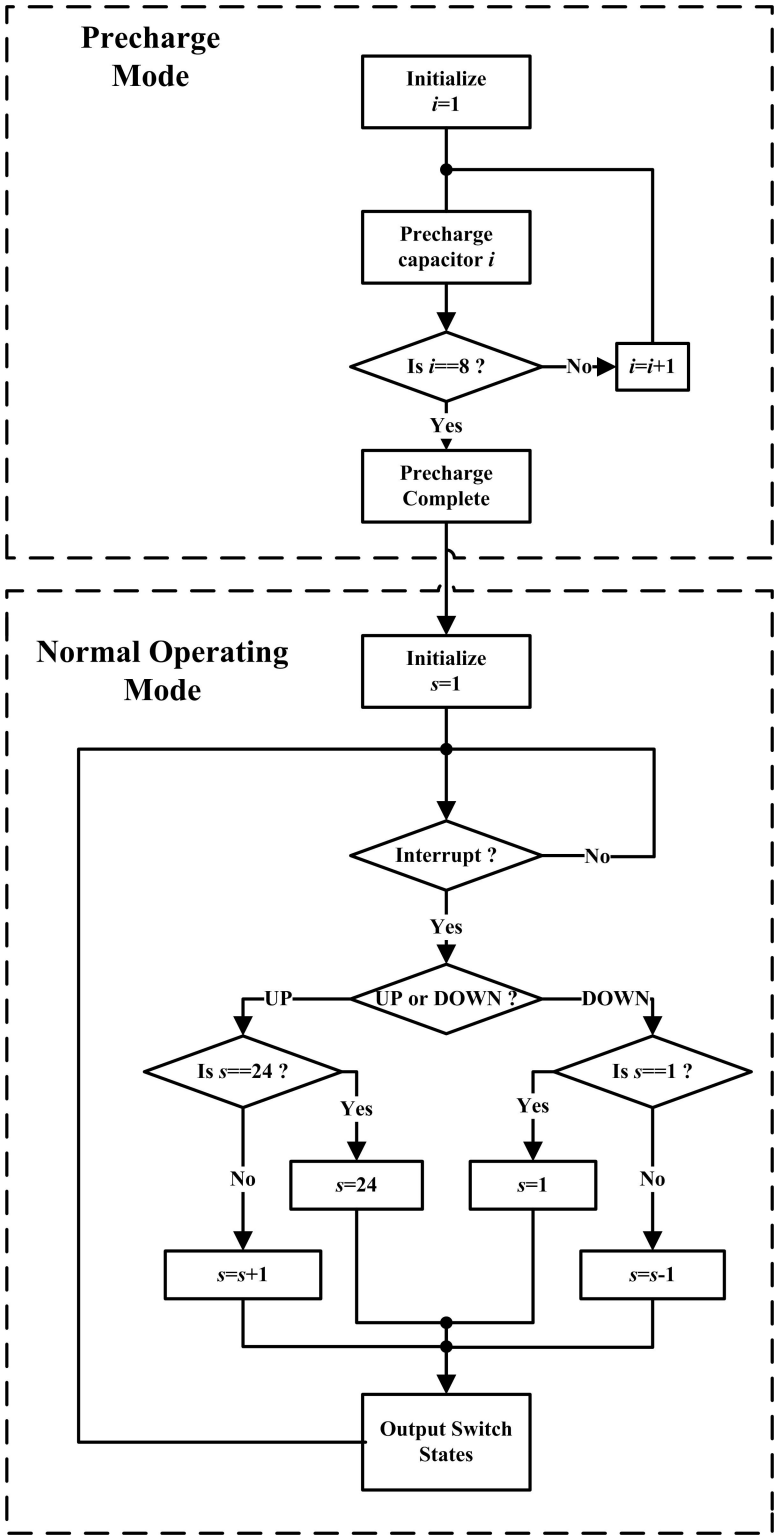


Figure 4-6: Flow chart showing the control logic during precharge and normal operation of the 2-6 bipolar SSC energy buffer.

4.3 Control

The normal operation of the energy buffer is also controlled by a state machine implemented in the ATMEL ATmega2560 microcontroller. The state machine controls the state (on or off) of the twelve switches in the SSC energy buffer power circuit. The state machine has a total of 24 states, with each state corresponding to a unique and valid combination of the states of the twelve switches, as shown in Table 4.3.

The flow chart of the normal operation mode control logic of the energy buffer is shown in Fig. 4-6. In this flow chart, s denotes the current state of the state machine. The energy buffer starts normal operation in state 1 (i.e., s=1), which corresponds to minimum energy stored in the buffer, and starts to charge up. Once the bus voltage reaches the maximum allowed voltage, $1.1V_{\text{nom}}$ (352 V), the $\widehat{\text{UP}}$ interrupt is triggered and the state is incremented by one (i.e., s=s+1). The microcontroller turns the appropriate power switches on or off to match the configuration for the new state. This drops the bus voltage back to $0.9V_{\text{nom}}$ (288 V), and the charging of the energy buffer continues until it again reaches the upper voltage limit. This process is repeated as long as the energy buffer is being charged and it has not reached state 24. Once the energy buffer has reached state 24, the state machine stays in state 24 even if it receives additional $\widehat{\text{UP}}$ interrupts. This helps protect the energy buffer to a certain extent in case load power exceeds its design specifications. During this overload condition the energy buffer looks like a 1.1 μF capacitor to the external system. The energy buffer will return to normal operation once the load power returns to the design range.

During discharge of the energy buffer, the $\widehat{\text{DOWN}}$ interrupt is triggered when the bus voltage reaches the minimum allowed voltage, $0.9V_{\text{nom}}$ (288 V). This decrements the state by one (i.e., s=s-1). The microcontroller turns the appropriate power switches on and off to match the configuration for the new state and the bus voltage increases to $1.1V_{\text{nom}}$ (352 V). This process is repeated each time the bus voltage reaches the lower voltage limit until it has reached state 1. As in the case of charging, to protect the energy buffer, the state machine stays in state 1 even if it receives

additional $\widehat{\text{DOWN}}$ interrupts.

Hence during normal operation at maximum power, the state machine will iterate through states 1 through 24 in a sequential manner, first going from 1 to 24 as it charges, and then returning from 24 to 1 as it discharges, and this process is repeated as long as the energy buffer is in normal operation.

4.4 Artificial Voltage Feedback

In a conventional system with an energy buffering electrolytic capacitor at the output of the PFC, the PFC uses the bus voltage (i.e., the voltage across the buffering capacitor) to control its output current. The bus voltage is scaled down by a resistive divider and fed back to the PFC control chip. Since the bus voltage is a good measure of the energy stored in the capacitor, this feedback mechanism ensures that the average output power from the PFC matches the power drawn by the dc load and the system stays stable. However, when the electrolytic capacitor is replaced with the SSC energy buffer, the bus voltage is no longer a true representation of the energy stored in the energy buffer. Hence, an artificial signal must be generated (and fed back to the PFC control chip) that represents the energy stored in the energy buffer and mimics the bus voltage of the electrolytic capacitor. In our prototype this function is performed by a second ATMEL ATmega2560 microcontroller.

In the precharge mode, the SSC energy buffer behaves simply like two capacitors connected in series. Hence, during this period, the bus voltage reflects the energy stored inside the two capacitors and so the voltage that needs to be fed back is simply a scaled version of the bus voltage.

Once the energy buffer enters normal operating mode, its stored energy increases monotonically as it goes from state 1 to state 24 and then decreases monotonically as it returns to state 1. The energy that gets stored in the energy buffer as it goes from state 1 to state 24 is given by:

$$\Delta E(t) = \sum_{i=1}^{N} \frac{1}{2} C_i (V_i(t)^2 - V_{i0}^2), \tag{4.1}$$

Table 4.3: States of the twelve switches in the 2-6 bipolar SSC energy buffer corresponding to each of the 24 states of the state machine. Blank cell indicates the switch is off.

States	$\mathbf{S_{21}}$	$\mathbf{S_{22}}$	$\mathbf{S_{23}}$	$\mathbf{S_{24}}$	$\mathbf{S_{25}}$	$\mathbf{S_{26}}$	$\mathbf{S_{11}}$	$\mathbf{S_{12}}$	$\mathbf{S_{h1}}$	$\mathbf{S_{h2}}$	$\mathbf{S_{h3}}$	$\mathbf{S_{h4}}$
1	on						on		on		on	
2		on					on		on		on	
3			on				on		on		on	
4				on			on		on		on	
5					on		on		on		on	
6						on	on		on		on	
7						on	on			on		on
8					on		on			on		on
9				on			on			on		on
10			on				on			on		on
11		on					on			on		on
12	on						on			on		on
13	on							on	on		on	
14		on						on	on		on	
15			on					on	on		on	
16				on				on	on		on	
17					on			on	on		on	
18						on		on	on		on	
19						on		on		on		on
20					on			on		on		on
21				on				on		on		on
22			on					on		on		on
23		on						on		on		on
24	on							on		on		on

where N is the total number of capacitors in the energy buffer (eight in the 2-6 bipolar SSC case), C_i is the capacitance of capacitor i, $V_i(t)$ is the voltage of capacitor i at time t, and V_{i0} is the initial voltage of capacitor i after it is precharged. In our prototype all eight capacitors have the same capacitance C_b (equal to 2.2 μF). The effective energy in the energy buffer as a function of time is given by[1]:

$$E_{\mathrm{b(eq)}}(t) = \frac{1}{2} C_\mathrm{eq} V_\mathrm{min}^2 + \Delta E(t), \tag{4.2}$$

where C_eq is an equivalent capacitance for this energy buffer valid while it is operating in normal operating mode, and is given by:

$$C_\mathrm{eq} = \frac{2 \int_{\mathrm{t}_1}^{\mathrm{t}_2} p(t)\,\mathrm{d}t}{V_{\mathrm{t}_2}^2 - V_{\mathrm{t}_1}^2}. \tag{4.3}$$

Here $p(t)$ is the power flowing into the energy buffer, and V_{t_1} and V_{t_2} are the voltages at beginning (time t_1) and the end (time t_2) of the charging period, respectively. For our prototype, C_eq is equal to 26.4 μF.

Hence, the voltage that needs to be fed back in normal operating mode is given by:

$$V_\mathrm{fb}(t) = \sqrt{\frac{C_\mathrm{eq} V_\mathrm{min}^2 + 2\Delta E(t)}{C_\mathrm{eq}}}. \tag{4.4}$$

This feedback signal reflects the apparent energy stored in the energy buffer.

While the expression given by Eq. 4.4 for the normal operating mode feedback signal can be implemented, it is simpler to implement an approximation to this expression which works just as well within the resolution of our 8-bit digital to analog converter (DAC). The approximate feedback signal is derived assuming that the feedback voltage signal is linear between two switching instances and the current flowing into or out of the energy buffer is constant (i.e., current has a square profile). This

[1]Note that $E_{\mathrm{b(eq)}}$ as given by Eq. 4.2 is not the actual energy in the energy buffer but rather the apparent energy.

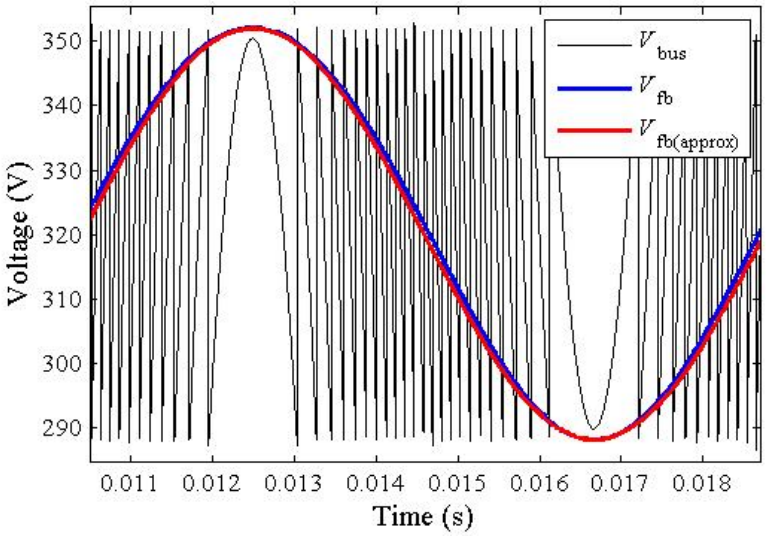


Figure 4-7: Comparisons between the accurate (V_{fb}) and approximate ($V_{\text{fb(approx)}}$) artificial feedback voltages for a sinusoidal energy buffer terminal current.

approximate feedback voltage is given by:

$$V_{\text{fb(approx)}}(t) = V_{\min} + (V_{\max} - V_{\min})\frac{i}{24} + (V_{\text{bus}}(t) - V_{\min})\frac{C_{\text{b}}}{2C_{\text{eq}}}. \tag{4.5}$$

Figure 4-7 shows that this approximate feedback signal matches the more accurate one quite well even when the terminal current of the energy buffer is sinusoidal. It has been experimentally demonstrated that the slower outer control loop of the PFC works well with this approximate feedback signal.

4.5 Summary

This chapter describes the prototype design of the SSC energy buffer. We selected the energy buffer required at the output port of a PFC circuit as our targeted application. Then we picked the 2-6 bipolar SSC energy buffer as our prototype topology, which best fits this application. The designs of the control strategy, precharge circuit and artificial feedback methodology are then introduced in detail. The simulation and experimental results of this 2-6 bipolar SSC energy buffer will be discussed in Chapter 5. Hardware implementation details of this prototype is provided in Appendix A.

Chapter 5

Simulation and Experimental Results

5.1 Simulation

A PLECS[1] model for this energy buffer has been built to simulate this prototype. Fig. 5-1 shows the schematics of this PLECS simulation model. A sinusoidal current source ("I_ac") is applied at the two terminals of the 2-6 bipolar stacked switched capacitor energy buffer. The eight capacitors' initial voltages are set to be the precharge voltages as described in Chapter 4. After the simulation starts, the "Cap-Voltage Probe" observes the voltages of each of capacitors and passes the information to the "C-Script" block, which simulates the microcontroller. Finally, the "C-Script" block processes the information and outputs the switching commands.

Figure 5-2 shows the voltage waveforms of the bus voltage and the capacitor voltages. Figure 5-3 and Fig. 5-4 show the drain-to-source voltage ($V_{\rm ds}$) and current ($I_{\rm ds}$) of each switch during one operating cycle, respectively. These figures will be refered in Appendix A when sizing the switches of the prototype.

[1]PLECS is a simulation tool for power electronic circuits.

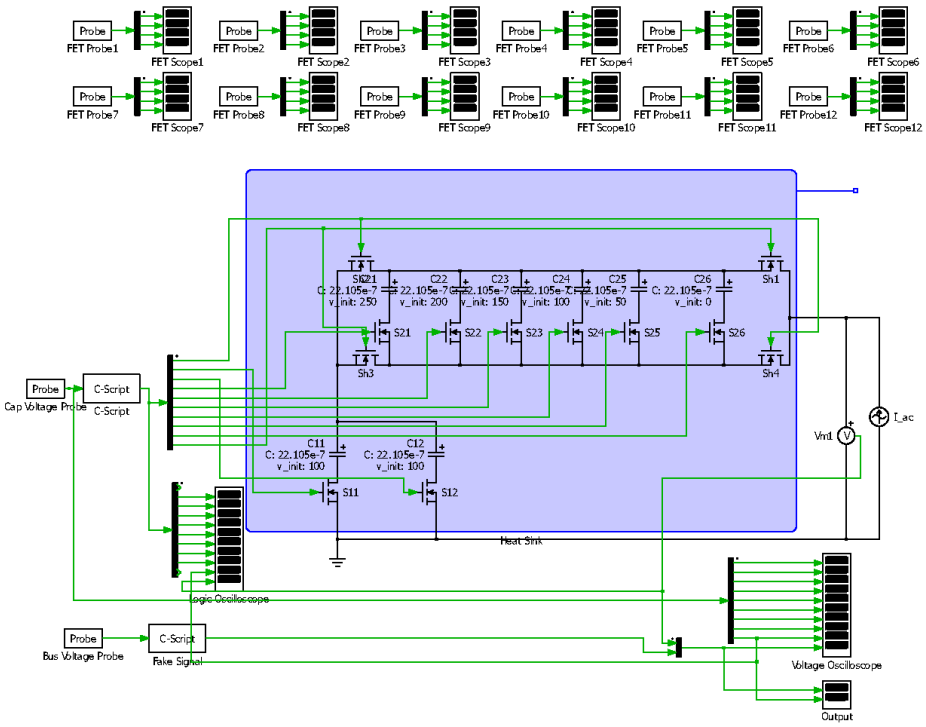


Figure 5-1: Simulated waveforms of (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time ($V_{2\text{x}}$), and (b) corresponding state (1-24) of the state machine.

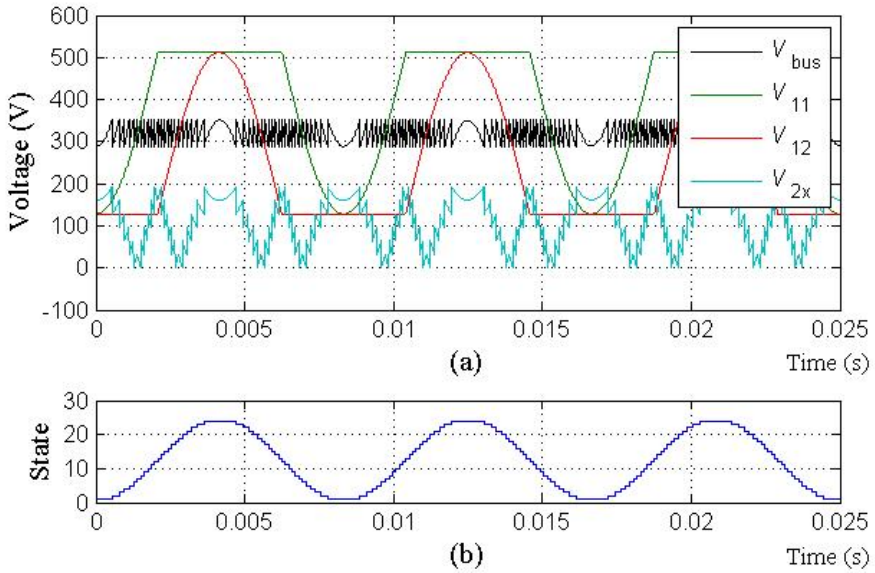


Figure 5-2: Simulated waveforms of (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time ($V_{2\text{x}}$), and (b) corresponding state (1-24) of the state machine.

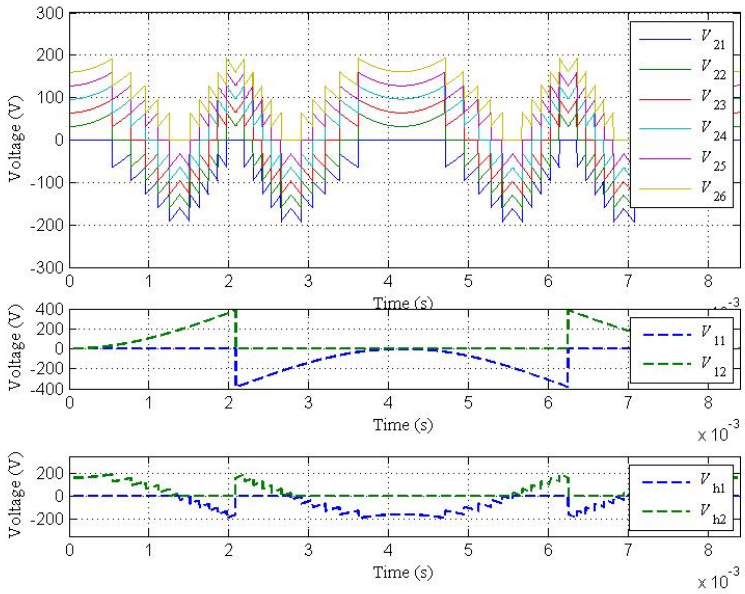


Figure 5-3: The drain-to-source voltage (V_{ds}) of each switch. The maximum V_{ds} for S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{26}, S_{11}, S_{12}, S_{h1} and S_{h2}, are 192 V, 160 V, 128 V, 128 V, 160 V, 192 V, 512 V, 512 V, 192 V, and 192 V, respectively (The voltages of S_{h3} and S_{h4} are identical to that of S_{h1} and S_{h2}). S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, and S_{26} need to block bidirectional voltages.

5.2 Experimental Results

5.2.1 Functionalities

The prototype 2-6 bipolar SSC energy buffer has been successfully tested with the PFC and a load resistor up to power levels of 135 W. Details of the prototype, including hardware implementation process and component list are provided in Appendix A. A photo of the set-ups are shown in Fig. 5-6. The measured waveforms from the energy buffer operated at 100 W are shown in Fig. 5-5. As the energy flows into and out of the energy buffer at 120 Hz, the backbone capacitors are charged and discharged over a wide voltage range. However, this voltage variation is compensated for by the supporting capacitors and the bus voltage remains within the 300 V and 370 V range. Hence, it meets the voltage ripple ratio design requirement of 10%.

Comparing Fig. 5-5 and Fig. 5-2, there is a reasonably close match between the experimental and simulated waveforms. The main difference is due to the fact that

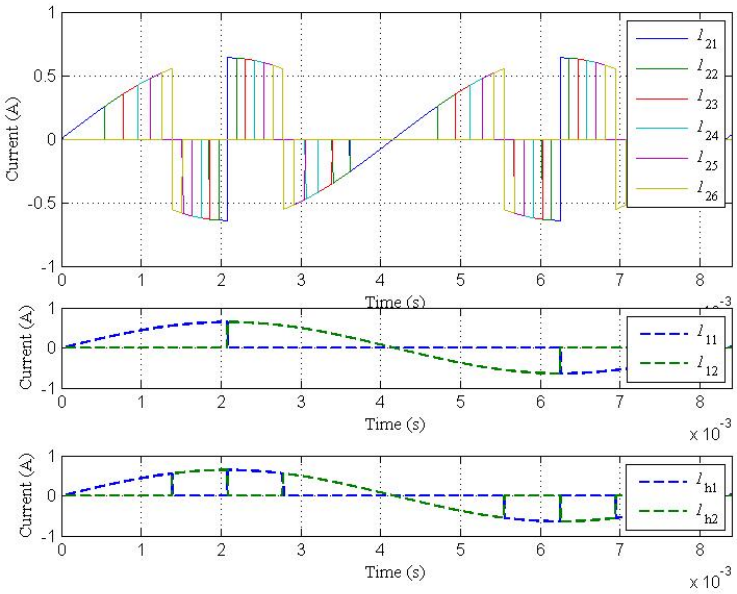


Figure 5-4: The drain-to-source current (I_{ds}) of each switch. The maximum I_{ds} for S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{26}, S_{11}, S_{12}, S_{h1} and S_{h2}, are 0.6400 A, 0.6377 A, 0.6310 A, 0.6196 A, 0.6032 A, 0.5816 A, 0.6400 A, 0.6400 A, 0.6400 A, and 0.6400 A, respectively(The voltages of S_{h3} and S_{h4} are identical to that of S_{h1} and S_{h2}).

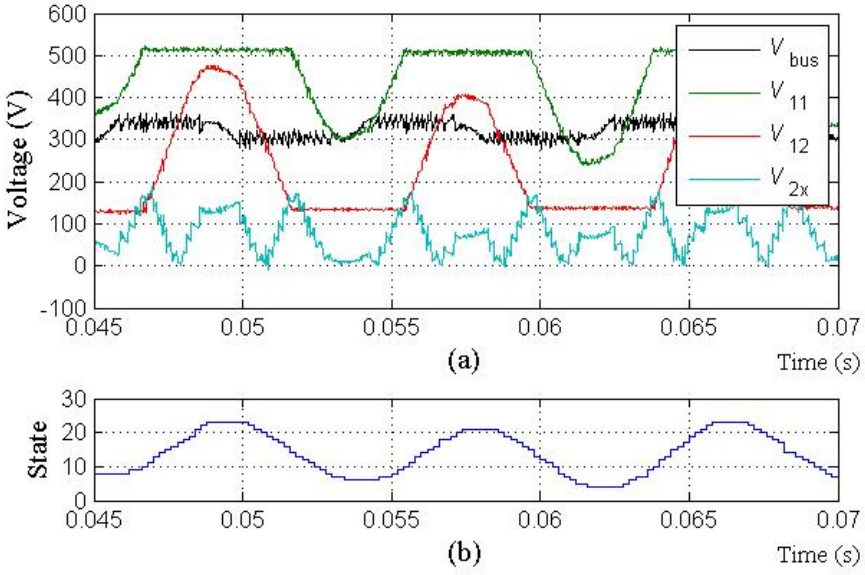


Figure 5-5: Measured waveforms of (a) bus voltage (V_{bus}), backbone capacitor voltages (V_{11} and V_{12}) and voltage across the supporting capacitor that is charging or discharging at the time ($V_{2\mathrm{x}}$), and (b) corresponding state (1-24) of the state machine.

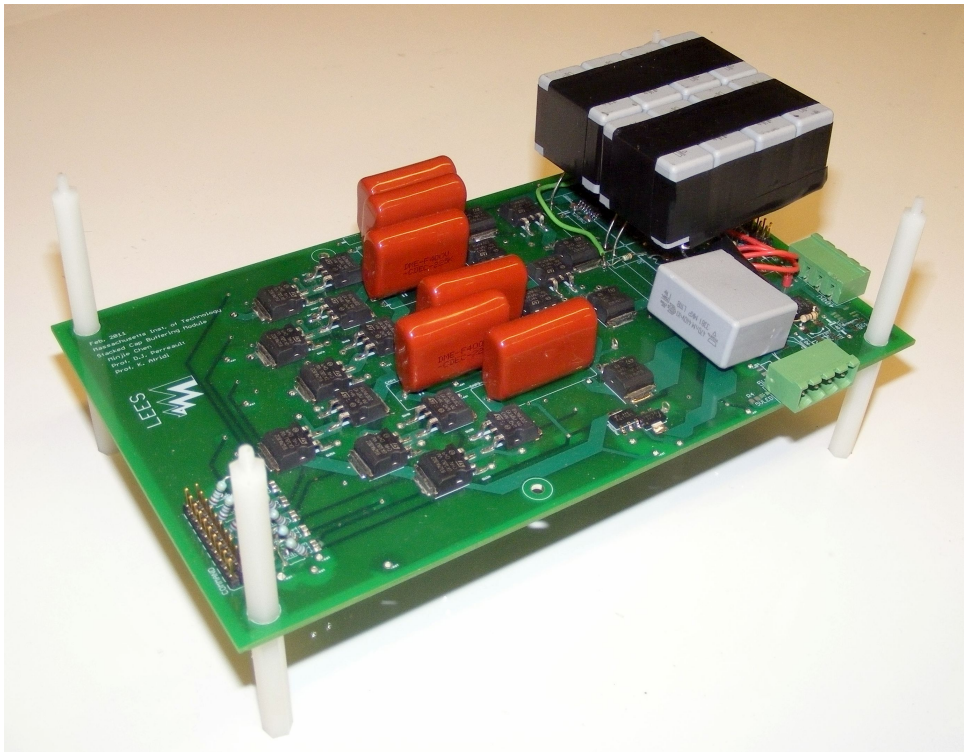


Figure 5-6: Prototyped bipolar 2-6 bipolar SSC energy buffer.

in the simulation the terminal current of the energy buffer is assumed to be perfectly sinusoidal, while in the case of the experimental setup that is not exactly the case. Figure 5-5(b) shows the state of the state machine. As can be seen, the state machine goes down to state 4 and up to state 24. The state machine does not go into states 1, 2 and 3 in its normal operating mode as the load power is not large enough to discharge it down to its minimum stored energy level. The circuit behaves as designed, and validates the concept of the stacked switched capacitor energy buffer.

5.2.2 Performances

A summary of the specifications of this prototype is shown in Table. 5.1. The highest load it can support is 127.6 W, with a highest operating efficiency of 97.0% (without loss in the control circuits) and 10% of voltage ripple ratio. The round-trip efficiency of the prototype 2-6 bipolar SSC energy buffer was measured for the 18.9 W to 127.6 W load power range as shown in Fig. 5-7. The efficiency stays above 95.3%

Table 5.1: Summary specifications of the prototyped 2-6 bipolar stacked switched capacitor energy buffer.

Name	Value
Maximum Load	127.6 W
Voltage Ripple Ratio	10%
Maximum Efficiency	97.0% at 127.6 W

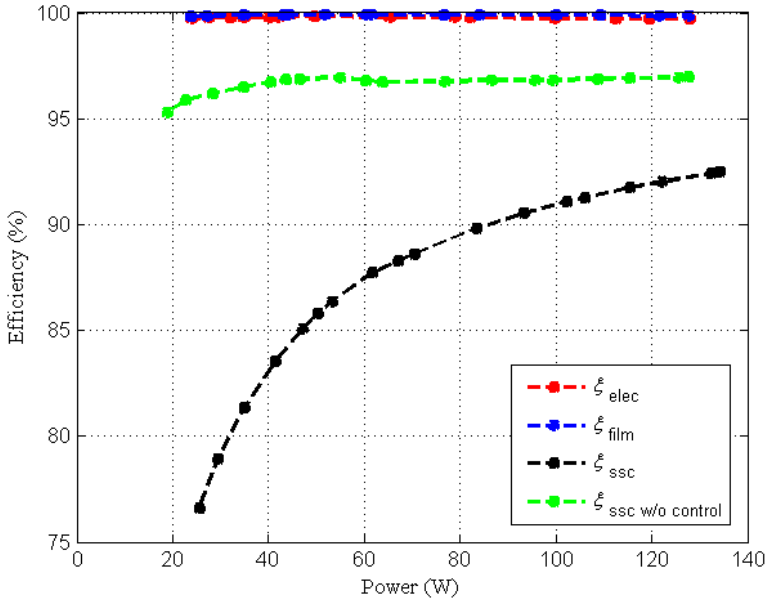


Figure 5-7: Round-trip efficiency (ξ) of the prototype 2-6 bipolar SSC energy buffer with and without the control circuit as a function of power drawn by the load. It is compared to the round trip efficiency of the electrolytic-capacitor-only and film-capacitor-only energy buffer.

throughout this power range. We noticed an efficiency drop of around 0.2% at the power range of around 65 W, which indicates a 0.13 W power lose by flipping of the H-bridge.

The control and gate drive circuit were not designed for high efficiency in our prototype. From the measurement, losses consumed by the gate drivers and the Digital to Analog Converters are roughly staying at 6.67 W over the entire operating range, which significantly diminished the efficiency of the SSC energy when it is supplying light load (e.g. the efficiency drops from 92.79% to 78.97% for 30 W of load).

Table 5.2: The losses composition of the prototyped 2-6 bipolar SSC energy buffer.

Components	Loss	Percentage
Gate Drivers (Adum5230)	3.0 W	44.77%
Conduction and Parasitic Loss	2.5 W	37.32%
Voltage Dividers, Comparators, D/A and A/D Converters	1.0 W	14.93%
Microcontrollers (ATMEL ATmega2560)	0.2 W	2.98%

The losing mechanism of this prototype can be evaluated combining the information we get from the experimental results and the datasheets of each components. The result shown in Table 5.2 indicates that the gate drivers are the main loss mechanism for this prototype. More efficient gate driving techniques can significantly improve the overall efficiency of the system. Parasitic and conducting losses take the other large proportion, which can be reduced by better layout of the components.

The prototype energy buffer successfully replaces the function of the electrolytic capacitor at the output of the PFC. Its passive volume of 20 cm^3, which is much smaller than the 65 cm^3 needed for a film-capacitor-only solution, is only about twice the size of the 9 cm^3 electrolytic capacitor it replaces, as shown in Fig. 5-8. Hence, the SSC energy buffer achieves energy buffering density comparable to an electrolytic capacitor while providing much longer life.

5.3 Summary

This chapter presents the experimental results of the prototyped 2-6 bipolar SSC energy buffer. The efficiency is measured over a wide load range, with a highest measured efficiency of 97.0% (not considering the loss of the control circuits). The total passive volume of the prototype is 13 cm^3, which is comparable to the 9 cm^3 of the electrolytic-capacitor-only energy buffer, and much smaller than the 65 cm^3 of the film-capacitor-only energy buffer. It is verified that the 2-6 bipolar SSC energy buffer with film capacitors can successfully replace the function of the electrolytic capacitor as energy buffers, and potentially achieve much higher reliability and longer life time.

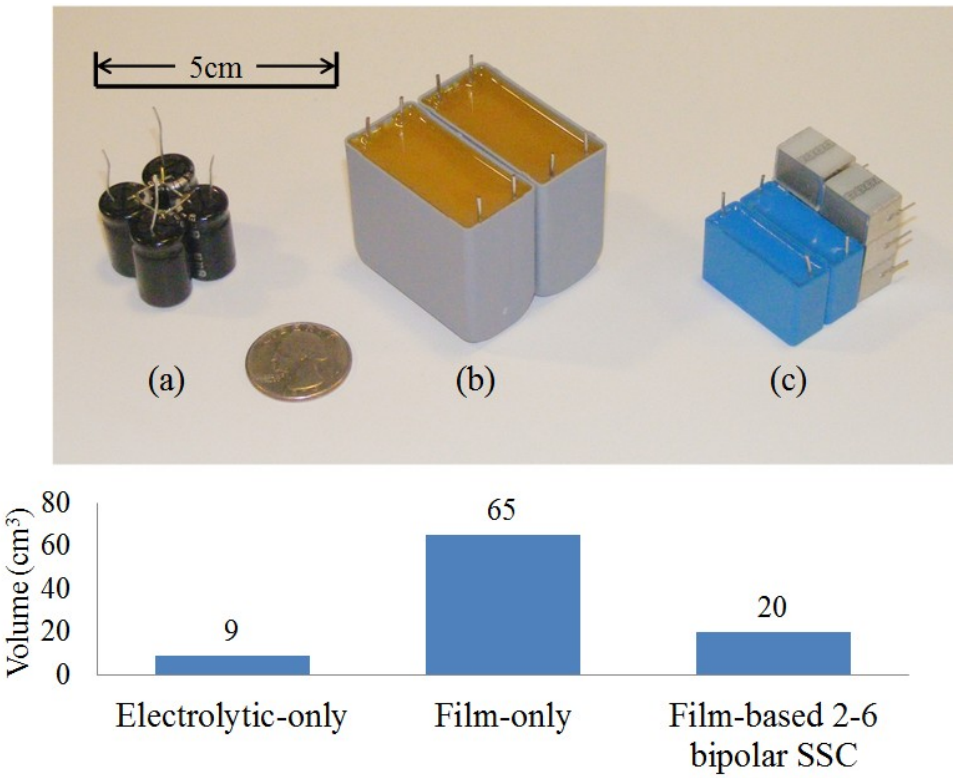


Figure 5-8: Relative size of passive energy storage components in different energy buffer architectures: (a) electrolytic-capacitor-only (9 cm^3) (b) film-capacitor-only (65 cm^3) and (c) film-capacitor-based SSC (20 cm^3) energy buffer.

Chapter 6

Summary, Conclusions and Future Work

6.1 Summary

This thesis introduces and studies stacked switched capacitor (SSC) architecture for dc-link energy buffering applications, including buffering between single-phase ac and dc. Traditionally, electrolytic capacitors are used as energy buffers as they have high energy density. However, they fail to fully use their energy storage capacity due to constrain of maintaining small bus voltage ripples. And their limited life is an issue. Film capacitors have much longer life but a roughly order of magnitude lower energy density.

By appropriately reconfiguring the connections of capacitors in two stacked layers, the SSC architecture is capable of utilizing the energy storage capability of capacitors more effectively than previous switched capacitor designs, while still maintaining the bus voltage ripple within a narrow range. This allows the energy buffer to achieve higher effective energy buffering density, and reduce the volume of passive components in power electronic circuits. In the proposed stacked switched capacitor energy buffer, with two-layer architecture, energy is mainly stored in one layer of capacitors (backbone capacitors), with the other layer of capacitors works as a voltage ripple compensator. In this case, although the capacitors which store energy have wide

voltage swing, the bus voltage will only have a comparative small voltage ripple.

A prototype of this architecture has been built. Considering the application requirements to keep the circuit complexity at a minimum, we picked the 2-6 SSC energy buffer topology for prototype. The SSC energy buffer is connected at the output port of a 400 W power factor correction (PFC) circuit to replace the use of a 40 μF electrolytic capacitor and required to supply 135 W of output power while maintaining a voltage ripple ratio of 10%. A linear regulator working as a current source is used to perform the function of a precharge circuit that charges all the capacitors of the SSC energy buffer to their initial start-up voltage. A microcontroller controls the switching of the SSC energy buffer by operating a 24-state state-machine. It makes decisions by observing the variations in the bus voltage. Another microcontroller, alone with analog/digital converters, generates an artificial feedback signal which reflects the actual amount of energy stored in the energy buffer. This signal is fed back to the PFC to generate the PWM signal which controls the duty ratio of the PFC.

6.2 Conclusions

The prototype proves the fundamental principles of this architecture. The PFC functions as a current source with rms current equal to the required load current. And the prototype functions identical to a 26.4 μF 450 V electrolytic capacitor, using only 17.8 μF of film capacitor (of different rated voltages). It is able to supply 127.6 W of power at 320 V with 10% of voltage ripple ratio. It is shown that the SSC energy buffer can successfully replace the limited-life electrolytic capacitors with much longer life film capacitors, while maintaining volume and efficiency at a comparable level. The volume of the passive device is comparable with the original electrolytic capacitor. The prototyped 2-6 bipolar SSC energy buffer has a peak round trip efficiency of 97.00%.

This thesis proves that the SSC architecture is an effective way of enhancing the effective energy density of film capacitors while maintaining a narrow bus voltage vari-

ation in an energy buffering application. The SSC energy buffer architecture enables the use of film capacitors in replace of electrolytic capacitors and hence overcomes capacitor life-limitation without an order of magnitude increase in passive volume. For different application requirements, different embodiments of the SSC energy buffer architecture should be selected. A detailed selecting methodology has been introduced in Chapter 3.

6.3 Future Work

The stacked switched capacitor energy buffer architectures demonstrated in this thesis is the first attempt of applying this architecture for energy buffering applications. It would be valuable to evaluate the use of ceramic capacitors, in place of film capacitors, as the supporting capacitors in the SSC architecture. Also there are other implementations of the stacked switched capacitor energy buffer architecture. They should also be explored in the future.

Appendix A

Hardware Implementation

This appendix lists some useful detals of the hardware implementation of the prototyped 2-6 bipolar switched stacked capacitor (SSC) energy buffer. The detailed explanations and design considerations of the topology can be found in Chapter 4, and the simulation and experimental results of this prototype can be found in Chapter 5.

A.1 Component Selecting

A.1.1 Capacitors and Switches

As described in Chapter 4, we simulated the circuit with PLECS and plot the drain to source voltage (V_{ds}) and current (I_{ds}) of all switches. The related waveforms are shown in Fig. 5-3 and Fig. 5-4. Based on this, each switch can be sized according to the maximum V_{ds} and I_{ds} applied on it. Similarly, capacitors of this prototype can be sized according to the simulation results shown in Fig. 5-2. The part numbers of selected switches and capacitors are listed in Table A.1.

A.1.2 Gate Drivers

The six high level switches and the four h-bridge switches in the 2-6 bipolar SSC energy buffer architecture are floating switches, as a result, we use AD5301, an isolated

half-bridge gate driver chip with isolated dc-dc power supply, followed by FAN3111, a low side gate driver which is able to supply currents as high as 1.0 A to drive these floating switches. As described in Chapter 5, this gate driver has a high quiscent energy consumption (around 200mW each). To design a customized gate driver for the SSC energy buffer is an interesting and valuable topic for the further investigation of this technology.

A.1.3 Precharge Circuits

We connect Supertex LR8 linear regulator as a current source to conduct the function of precharge circuit. The precharge circuit is isolated from the power circuit when the periodic operating period begins. The circuit which connects Supertex LR8 as a current source can be found from its application notes.

A.1.4 Microcontrollers

Two ATMEL ATmega2560 8 bit 16 MHz microcontrollers are used in this prototype. One is used for controlling the switching states, provideing the appropriate threshold voltages, V_{up}, V_{down} through DACs, and communicating with the other microcontroller to feed the actual amount of energy that is stored by the SSC energy buffer back to the power factor correction (PFC) circuit. We call this controller as Microcontroller#1. The other microcontroller, called Microcontroller#2, senses the bus voltage through a voltage divider and an ADC, communicates with Microcontroller#1 and generates the feedback signal through another DAC.

A.1.5 Data Conversion Circuits

The data conversion circuits include four low speed Digital to Analog Converters (DACs), four comparators, one high speed Analog to DIgital Converter (ADC), one high speed DAC and several active signal buffers. The four AD5301 serial 8-bit voltage output DACs with 8 μs of output settling time is used for generating the four threshold voltage during the precharge and periodic operating mode. These

DACs's transition frequency is far below the line frequency so that it can use serial communication ($I2C$). One AD7822 parallel 8 bit ADC with 420 ns of conversion time, and one AD558 parallel 8 bit DAC with 3 μs of conversion time is used for sensing the bus voltage and generating the feedback signals. Their short conversion time minimizes the loop delay of the voltage feedback and maintains the stability of the system.

A.1.6 Other Ancillary Circuits

There are several ancillary circuits which are implemented in a standard way without specifically selecting the components, including voltage dividers, testing points, connection jacks, decoupling capacitors and isolating transformers. We also use two CLARE CPC1779J DC power relays to provide a garenteed isolation between the precharge circuit and power circuit for debugging purpose.

A.2 PCB Layouts

We draw the SSC architecture of this 2-6 bipolar SSC energy buffer on a 4 layer 1oz PCB board with EAGLE[1]. The PCB layout of the four layers as well as necessary drills and pads are shown in Fig. A-1, Fig. A-2, Fig. A-3, and Fig. A-4. They satisfy the commonly used layout electronic rule check (ERC) and design rule check (DRC) criteria.

[1]EAGLE: A printed circuit boards (PCB) designing tool.

Table A.1: Part number of critical components. All these components have been sized with debugging margins.

Part Number	Value	Function
C_{11}	2.2 μF KEMET MKPB32794	Backbone Capacitor
C_{12}	2.2 μF KEMET MKPB32794	Backbone Capacitor
C_{21}	2.2 μF CORNELL DME4W22K-F	Supporting Capacitor
C_{22}	2.2 μF CORNELL DME4W22K-F	Supporting Capacitor
C_{23}	2.2 μF CORNELL DME2W22K-F	Supporting Capacitor
C_{24}	2.2 μF CORNELL DME2W22K-F	Supporting Capacitor
C_{25}	2.2 μF CORNELL DME1W22K-F	Supporting Capacitor
C_{26}	2.2 μF CORNELL DME1W22K-F	Supporting Capacitor
S_{11}	STMicroelectronics STP12NK80Z	Blocking 382 V voltage (bipolar)
S_{12}	STMicroelectronics STP12NK80Z	Blocking 382 V voltage (bipolar)
S_{21}	STMicroelectronics STP12NK40Z	Blocking 192 V voltage (bipolar)
S_{22}	STMicroelectronics STP12NK40Z	Blocking 160 V voltage (bipolar)
S_{23}	STMicroelectronics STP12NK40Z	Blocking 128 V voltage (bipolar)
S_{24}	STMicroelectronics STP12NK40Z	Blocking 128 V voltage (bipolar)
S_{25}	STMicroelectronics STP12NK40Z	Blocking 160 V voltage (bipolar)
S_{26}	STMicroelectronics STP12NK40Z	Blocking 192 V voltage (bipolar)
S_{s}	Fairchild FQT1N80TF	Blocking 700V voltage
S_{iso1}	Fairchild FQT1N80TF	Blocking 700V voltage
S_{iso2}	Fairchild FQT1N80TF	Blocking 700V voltage
R_{11}	100 kΩ	Voltage divider
R_{12}	1 kΩ	Voltage divider
R_{21}	100 kΩ	Voltage divider
R_{22}	1 kΩ	Voltage divider
R_{load}	1000 kΩ 250 W	Power resistor
IC	Maxim FAN3111	Gate driver
IC	Analog Device ADUM5230	Gate driver
IC	Analog Device AD5301	DAC
IC	Maxim MAX9031	Comparator
IC	Analog Device AD7822	ADC for dummying the feedback
IC	Analog Device AD820	Op-Amp signal buffer
IC	Analog Device AD558	DAC
IC	ATMEL ATmega2680	Microcontroller
IC	Supertex LR8	Linear regulator
IC	STMicroelectronics L6562A	PFC demonstration board
DC Relay	CLARE CPC1779J	DC power relay

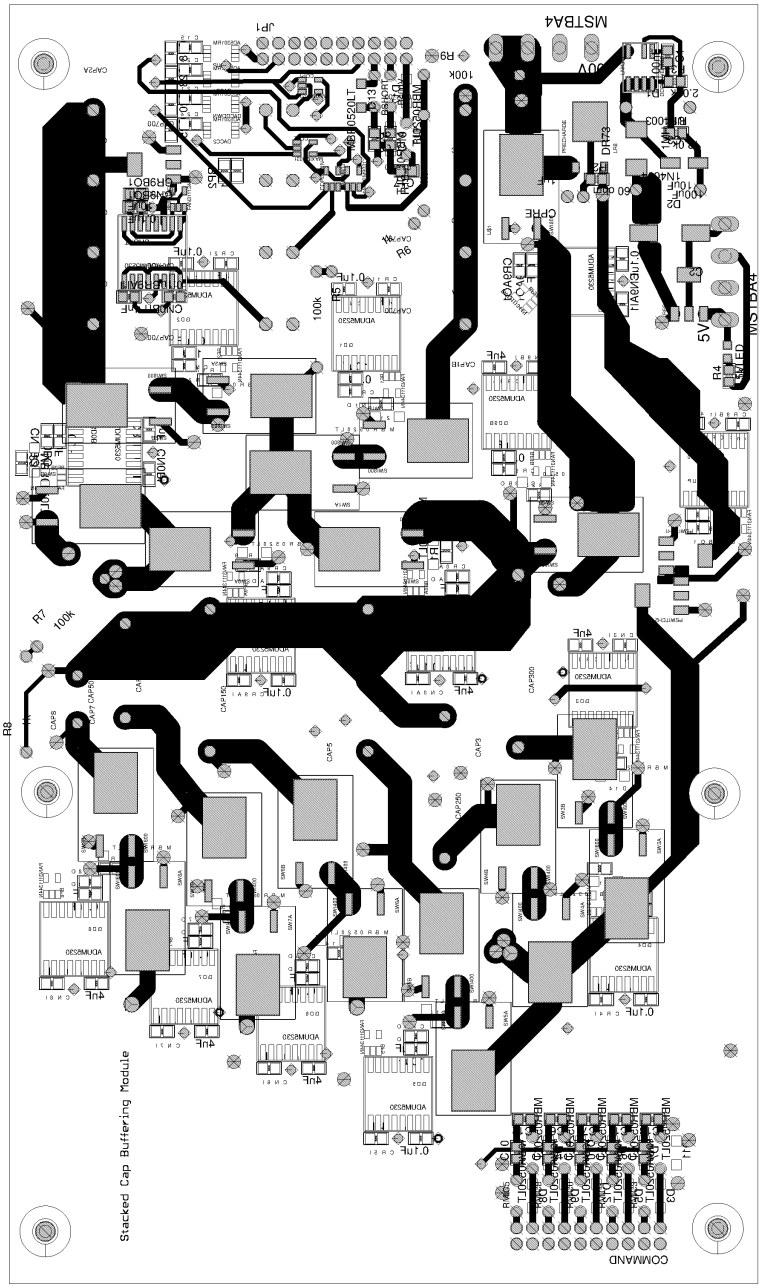


Figure A-1: The top layer of the board.

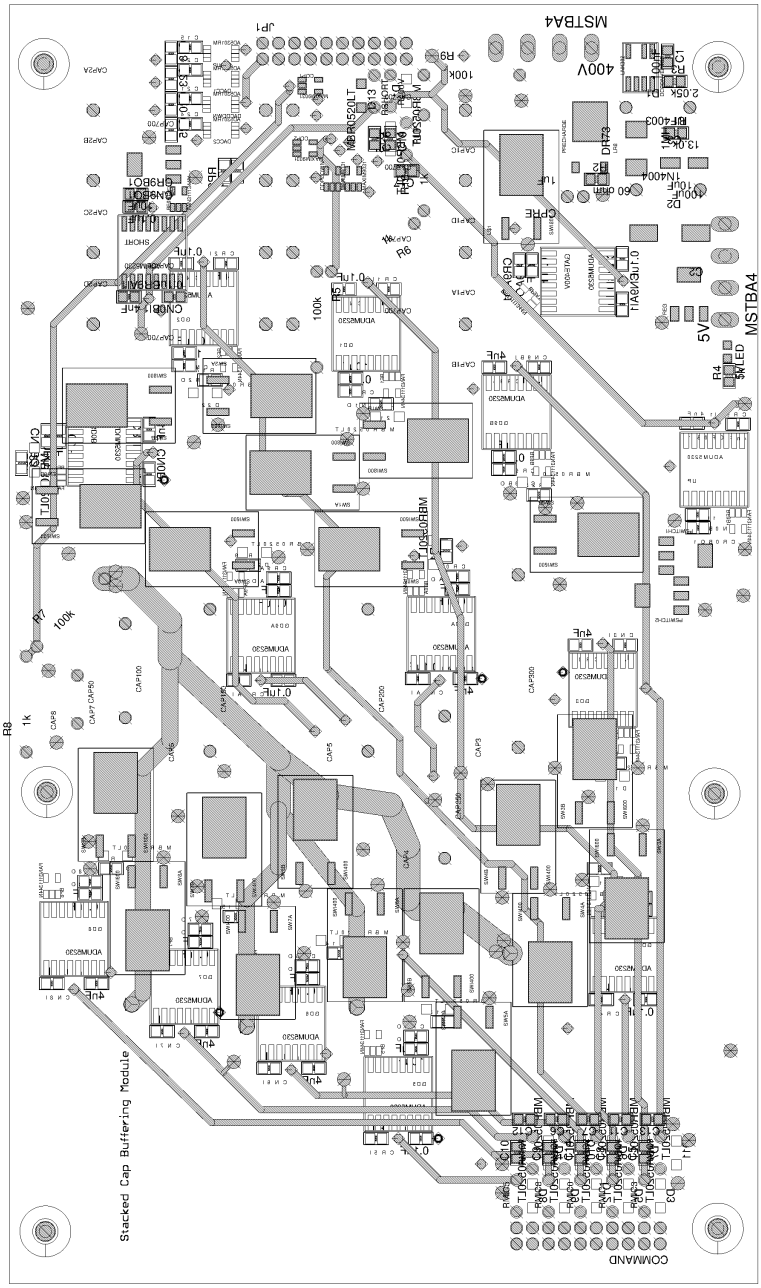


Figure A-2: The 2nd layer of the board.

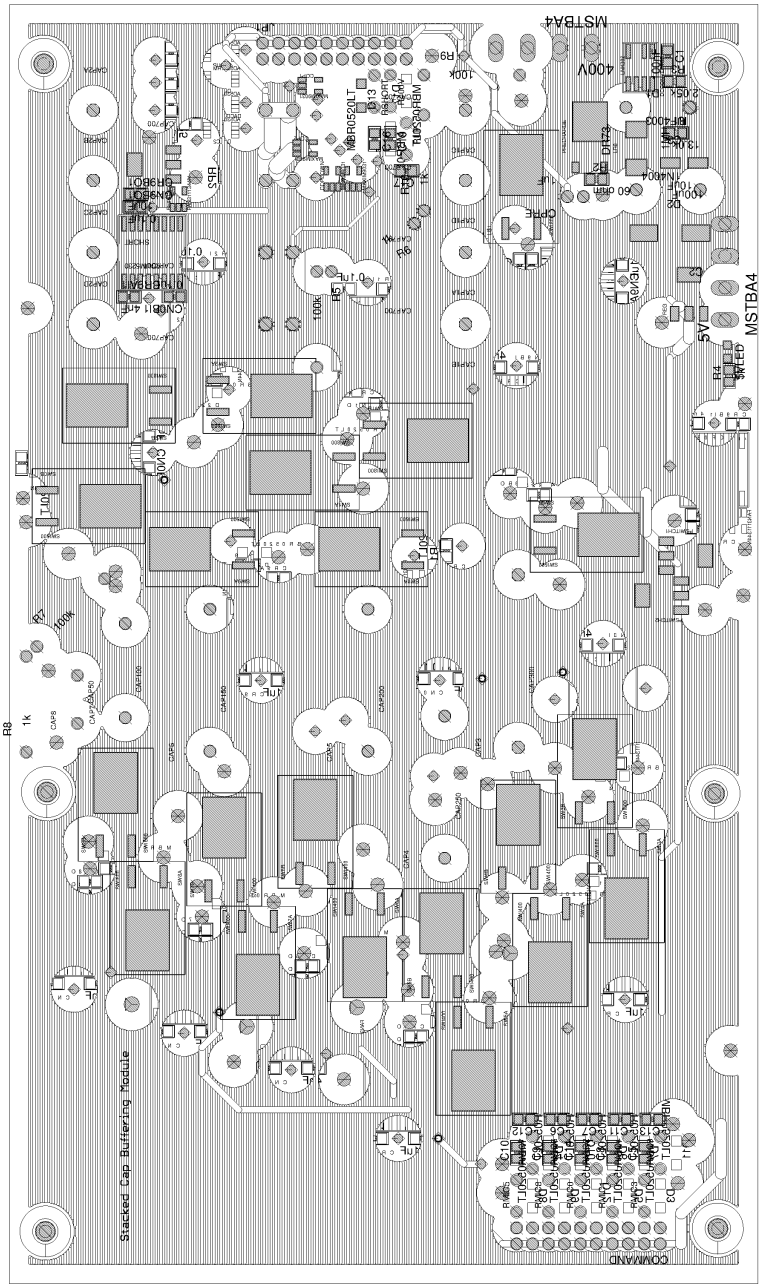


Figure A-3: The 3rd layer of the board.

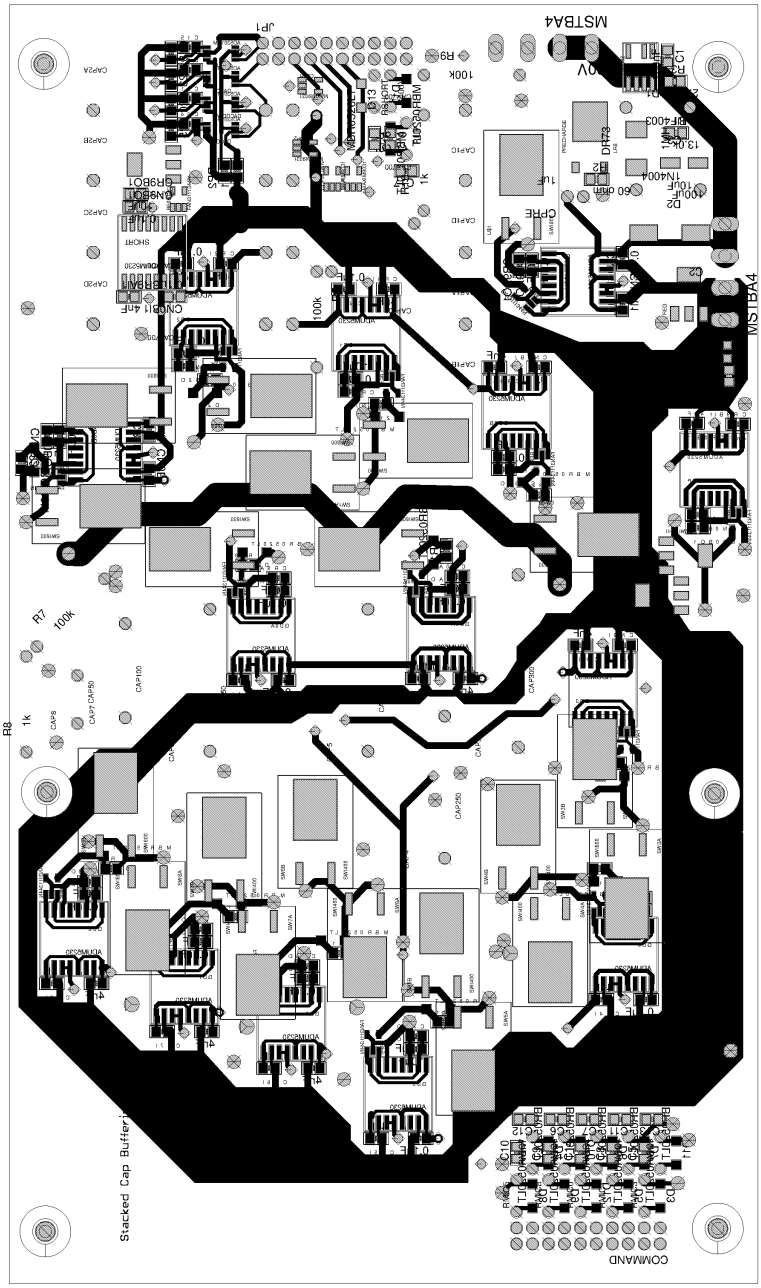


Figure A-4: The bottom layer of the board.

Appendix B

Codes

B.1 Microcontroller #1

```
1  //This is the operating code of the Microcontroller \#1. It is a ...
       ATMEL Mega2560 Microcontroller running on Arduino programming ...
       platform. The code is writting in C.
2  //by Minjie Chen 12/06/2011.
3
4  //including necessary communication packages
5  #include <Wire.h>
6
7  //assigning addresses for the ADCs
8  #define DAC0 (B0001100)//350V
9  #define DAC1 (B0001101)//Smallcapvoltage
10 #define DAC2 (B0001110)//450V
11 #define DAC3 (B0001111)//Bigcapvoltage,interrupt 4
12
13 //define the Port name for the eight main switch, giving to PORTL
14 #define S1 (B10000000)
15 #define S2 (B01000000)
16 #define S3 (B00100000)
17 #define S4 (B00010000)
18 #define S5 (B00001000)
```

```
#define S6 (B00000100)
#define S7 (B00000010)
#define S8 (B00000001)
#define S9 (B00001010)
#define S0 (B00000101)
#define SUP (B00010000)
#define S400V (B00100000)
#define SSHORT (B01000000)
#define SUPSHORT (B01010000)
#define PRECHARGE (B00000001)
#define PERIODIC (B00000010)

//defining the setting functions of DACs
void dacwrite(int address, int voltage) {
  int value = (voltage)/1.5;
  int Highvalue = value/16;
  int Lowvalue = (value-Highvalue*16)*16;
  byte HighBit = B00001111 & (byte(Highvalue));
  byte LowBit = B11110000 & (byte (Lowvalue));
  Wire.beginTransmission(address);
  Wire.send(HighBit);  //  send data
  Wire.send(LowBit);
  Wire.endTransmission();
}

//initializing the register values
int RegUL=0;
int RegUC=0;
int RegDL=0;
int RegDC=0;
int PORTLC=0;
int PORTLD=0;
int PORTFC=0;
int PORTFD=0;
int OutputL=0;
int OutputC=0;
```

```
55 int Busstate = 1;
56 int C1Ready=0;
57 int C2Ready=0;
58 int C3Ready=0;
59 int C4Ready=0;
60 int C5Ready=0;
61 int C6Ready=0;
62 int C7Ready=0;
63 int C8Ready=0;
64 int Run=0;
65 int sum=0;
66 int count =0;
67 int state=0;
68 int switchstate=0;
69 int ∆=32;
70 int vbus=320;
71
72 //setting up and intiatling the system
73 void setup(){
74
75     //turning on communication packages
76     Wire.begin();
77
78     //enabling output ports
79     DDRL=B11111111;
80     DDRF=B11111111;
81     DDRG=B11111111;
82     DDRA=B11111111;
83
84     //indicating precharge signals
85     pinMode(50,OUTPUT);
86     digitalWrite(50,LOW);
87     pinMode(51,OUTPUT);
88     digitalWrite(51,LOW);
89
90     //initialing output ports
```

```
91      PORTG=B00000000;
92      state=0;
93      RegUL=0;
94      RegUC=0;
95      RegDL=0;
96      RegDC=0;
97      PORTLC=0;
98      PORTLD=0;
99      PORTFC=0;
100     PORTFD=0;
101     OutputL=0;
102     OutputC=0;
103     Busstate =1;
104     C1Ready=0;
105     C2Ready=0;
106     C3Ready=0;
107     C4Ready=0;
108     C5Ready=0;
109     C6Ready=0;
110     C7Ready=0;
111     C8Ready=0;
112     Run=0;
113     sum=0;
114     count =0;
115
116     //discharging capacitors and initialing switch states
117     PORTL = B10000000;
118     PORTL = B01000000;
119     PORTL = B00100000;
120     PORTL = B00010000;
121     PORTL = B00001000;
122     PORTL = B00000100;
123     PORTL = B00000010;
124     PORTL = B00000001;
125     PORTL = B00000000;
126     PORTF = B10000000;
```

```
127     PORTF = B01000000;
128     PORTF = B00100000;
129     PORTF = B00010000;
130     PORTF = B00001000;
131     PORTF = B00000100;
132     PORTF = B00000010;
133     PORTF = B10000001;
134     PORTF = B00000000;
135 }
136
137 //loop functions
138 void loop() {
139
140     //checking the status of precharge
141     sum=C1Ready+C2Ready+C3Ready+C4Ready+C5Ready+C6Ready+C7Ready+C8Ready;
142
143     //precharging the circuit if not all the capacitors have been ...
            precharged
144     if ((sum<8) && (Run==0))
145     {
146         //initialing
147         PORTA = Busstate;
148         PORTL = B00000000;
149         PORTF = B00000000;
150         PORTG = PRECHARGE;
151         digitalWrite(50,LOW);
152         digitalWrite(51,LOW);
153         PORTL = B00000000;
154         delayMicroseconds(10);
155
156         //precharging C11
157         dacwrite(DAC3,75);//rewriting the DACs
158         PORTL = S1;//setting up PORTL
159         PORTF = S9;//setting up PORTF
160         state = 1;//reset the signal variable which indicates the ...
                situation of each capacitors
```

```
161         state = digitalRead(19);//read-in new signal variable
162         delayMicroseconds(10);//read-in delay
163         //if the capacitor is not fully charged
164         while (state==0)
165         {
166         //charging
167         PORTF = S9 | SUP;
168         delayMicroseconds(1);
169         //refreshing the signal variable again
170         state = digitalRead(19);
171         }
172         PORTF = S9;
173         //indicating that C1 is fully charged
174         C1Ready = 1;
175         //switching off all switches
176         PORTL = B00000000;
177         delayMicroseconds(10);
178
179         //precharging C12
180         dacwrite(DAC3,4*Δ);
181         PORTL = S2;
182         PORTF = S9;
183         state = 1;
184         state = digitalRead(19);
185         delayMicroseconds(10);
186         while (state==0)
187         {
188         PORTF = S9 | SUP;
189         delayMicroseconds(1);
190         state = digitalRead(19);
191         }
192         PORTF = S9;
193         C2Ready = 1;
194         PORTL = B00000000;
195         delayMicroseconds(10);
196
```

```
197         //precharging C21
198         dacwrite(DAC0,95);
199         PORTL = S3;
200         PORTF = S0 | SSHORT;
201         state = 1;
202         state = digitalRead(2);
203         delayMicroseconds(10);
204         while (state==0)
205         {
206         PORTF = S0 | SUPSHORT;
207         delayMicroseconds(1);
208         state = digitalRead(2);
209         }
210         PORTF = S0 | SSHORT;
211         C3Ready = 1;
212         PORTL = B00000000;
213         delayMicroseconds(10);
214
215         //precharging C22
216         dacwrite(DAC0,4*Δ);
217         PORTL = S4;
218         PORTF = S0 | SSHORT;
219         state = 1;
220         state = digitalRead(2);
221         delayMicroseconds(10);
222         while (state==0)
223         {
224         PORTF = S0 | SUPSHORT;
225         delayMicroseconds(1);
226         state = digitalRead(2);
227         }
228         PORTF = S0 | SSHORT;
229         C4Ready =1;
230         PORTL = B00000000;
231         delayMicroseconds(10);
232
```

```
233         //precharging C23
234         dacwrite(DAC0,3*Δ);
235         PORTL = S5;
236         PORTF = S0 | SSHORT;
237         state = 1;
238         state = digitalRead(2);
239         delayMicroseconds(10);
240         while (state==0)
241         {
242           PORTF = S0 | SUPSHORT;
243           delayMicroseconds(1);
244           state = digitalRead(2);
245         }
246         PORTF = S0 | SSHORT;
247         C5Ready =1;
248         PORTL = B00000000;
249         delayMicroseconds(10);
250
251         //precharging C24
252         dacwrite(DAC0,2*Δ);
253         PORTL = S6;
254         PORTF = S0 | SSHORT;
255         state = 1;
256         state = digitalRead(2);
257         delayMicroseconds(10);
258         while (state==0)
259         {
260           PORTF = S0 | SUPSHORT;
261           delayMicroseconds(1);
262           state = digitalRead(2);
263         }
264         PORTF = S0 | SSHORT;
265         C6Ready = 1;
266         PORTL = B00000000;
267         delayMicroseconds(10);
268
```

```
269         //precharging C25
270         dacwrite(DAC0,Δ);
271         PORTL = S7;
272         PORTF = S0 | SSHORT;
273         state = 1;
274         state = digitalRead(2);
275         delayMicroseconds(10);
276         while (state==0)
277         {
278           PORTF = S0 | SUPSHORT;
279           delayMicroseconds(1);
280           state = digitalRead(2);
281         }
282         PORTF = S0 | SSHORT;
283         C7Ready = 1;
284         PORTL = B00000000;
285         delayMicroseconds(10);
286
287         //precharging C26
288         dacwrite(DAC0,0);
289         PORTL = S8;
290         PORTF = S0 | SSHORT;
291         state = 1;
292         state = digitalRead(2);
293         delayMicroseconds(10);
294         while (state==0)
295         {
296           PORTF = S0 | SUPSHORT;
297           delayMicroseconds(1);
298           state = digitalRead(2);
299         }
300         PORTF = S0 | SSHORT;
301         C8Ready = 0;
302         PORTL = B00000000;
303         delayMicroseconds(10);
304     }
```

```
305
306     //finishing the precharge and set-up for the periodic ...
            operating mode
307     if ((sum==8)&&(Run==0))
308     {
309         //turning on the LED to show that the precharge is finished
310         digitalWrite(51,HIGH);
311         PORTG = B00000000;
312         PORTF = B00000000;
313         PORTL = B00000000;
314
315         //setting up up-threshold
316         dacwrite(DAC0,vbus+Δ);
317
318         //setting up down-threshold
319         dacwrite(DAC2,vbus-Δ);
320
321         //setting up initial states of the state machine registers
322         RegUL=S1 | S4;
323         RegUC=S400V | S0;
324         RegDL=S1 | S3;
325         RegDC=S400V | S0;
326         delay(3);
327
328         //setting up initial states of the ourput ports
329         PORTL=S1 | S3;
330         PORTF=S400V | S0;
331         delayMicroseconds(10);
332
333         //finishing setting ups
334         Run=1;
335     }
336
337     //entering periodic operating mode
338     if (Run==1)
339     {
```

```
340         //keeping the LED on
341         digitalWrite(50,HIGH);
342 
343         //setting up the external switches
344         PORTG= PERIODIC;
345         PORTA= Busstate;
346 
347         //state machine up-trigger
348         if (digitalRead(2)==1)
349         {
350             UP();
351         }
352 
353         //state machine down-trigger
354         if (digitalRead(3)==1)
355         {
356             DOWN();
357         }
358     }
359 }
360 
361 //State machine operating function
362 void DOWN()
363     {
364     //outputing the control signal
365     RegUL=PORTL;
366     RegUC=PORTF;
367     PORTL=RegDL;
368     PORTF=RegDC;
369 
370     //decreasing the Busstate
371     Busstate=Busstate--;
372 
373     //protective action if exceeding the operating range
374     if (Busstate<1)
375     {
```

```
376         Busstate=1;
377       }
378
379       //updating the down register according to the current Busstate
380       switch (Busstate)
381       {
382        case 1:
383           RegDL=S1 | S3;
384           RegDC=S400V | S0;
385           break;
386        case 2:
387           RegDL=S1 | S3;
388           RegDC=S400V | S0;
389           break;
390        case 3:
391           RegDL=S1 | S4;
392           RegDC=S400V | S0;;
393           break;
394        case 4:
395           RegDL=S1 | S5;
396           RegDC=S400V | S0;
397           break;
398        case 5:
399           RegDL=S1 | S6;
400           RegDC=S400V | S0;
401           break;
402        case 6:
403           RegDL=S1 | S7;
404           RegDC=S400V | S0;
405           break;
406        case 7:
407           RegDL=S1 | S8;
408           RegDC=S400V | S0;
409           break;
410        case 8:
411           RegDL=S1 | S8;
```

```
412             RegDC=S400V | S9;
413             break;
414         case 9:
415             RegDL=S1 | S7;
416             RegDC=S400V | S9;
417             break;
418         case 10:
419             RegDL=S1 | S6;
420             RegDC=S400V | S9;
421             break;
422         case 11:
423             RegDL=S1 | S5;
424             RegDC=S400V | S9;
425             break;
426         case 12:
427             RegDL=S1 | S4;
428             RegDC=S400V | S9;
429             break;
430         case 13:
431             RegDL=S1 | S3;
432             RegDC=S400V | S9;
433             break;
434         case 14:
435             RegDL=S2 | S3;
436             RegDC=S400V | S0;
437             break;
438         case 15:
439             RegDL=S2 | S4;
440             RegDC=S400V | S0;
441             break;
442         case 16:
443             RegDL=S2 | S5;
444             RegDC=S400V | S0;
445             break;
446         case 17:
447             RegDL=S2 | S6;
```

```
448             RegDC=S400V | S0;
449             break;
450         case 18:
451             RegDL=S2 | S7;
452             RegDC=S400V | S0;
453             break;
454         case 19:
455             RegDL=S2 | S8;
456             RegDC=S400V | S0;
457             break;
458         case 20:
459             RegDL=S2 | S8;
460             RegDC=S400V | S9;
461             break;
462         case 21:
463             RegDL=S2 | S7;
464             RegDC=S400V | S9;
465             break;
466         case 22:
467             RegDL=S2 | S6;
468             RegDC=S400V | S9;
469             break;
470         case 23:
471             RegDL=S2 | S5;
472             RegDC=S400V | S9;
473             break;
474         case 24:
475             RegDL=S2 | S4;
476             RegDC=S400V | S9;
477     }
478 }
479
480 //State machine operating function
481 void UP()
482 {
483     //outputing the control signal
```

```
484     RegDL=PORTL;
485     RegDC=PORTF;
486     PORTL=RegUL;
487     PORTF=RegUC;
488
489     //increasing Busstate
490     Busstate=Busstate++;
491
492     //protective action if exceeding the operating range
493     if (Busstate>24)
494     {
495       Busstate=24;
496     }
497
498     //updating the up register according to the current Busstate
499     switch (Busstate)
500     {
501      case 1:
502         RegUL=S1 | S4;
503         RegUC=S400V | S0;
504         break;
505      case 2:
506         RegUL=S1 | S5;
507         RegUC=S400V | S0;
508         break;
509      case 3:
510         RegUL=S1 | S6;
511         RegUC=S400V | S0;
512         break;
513      case 4:
514         RegUL=S1 | S7;
515         RegUC=S400V | S0;
516         break;
517      case 5:
518         RegUL=S1 | S8;
519         RegUC=S400V | S0;
```

```
520             break;
521         case 6:
522             RegUL=S1 | S8;
523             RegUC=S400V | S9;
524             break;
525         case 7:
526             RegUL=S1 | S7;
527             RegUC=S400V | S9;
528             break;
529         case 8:
530             RegUL=S1 | S6;
531             RegUC=S400V | S9;
532             break;
533         case 9:
534             RegUL=S1 | S5;
535             RegUC=S400V | S9;
536             break;
537         case 10:
538             RegUL=S1 | S4;
539             RegUC=S400V | S9;
540             break;
541         case 11:
542             RegUL=S1 | S3;
543             RegUC=S400V | S9;
544             break;
545         case 12:
546             RegUL=S2 | S3;
547             RegUC=S400V | S0;
548             break;
549         case 13:
550             RegUL=S2 | S4;
551             RegUC=S400V | S0;
552             break;
553         case 14:
554             RegUL=S2 | S5;
555             RegUC=S400V | S0;
```

```
556             break;
557         case 15:
558             RegUL=S2 | S6;
559             RegUC=S400V | S0;
560             break;
561         case 16:
562             RegUL=S2 | S7;
563             RegUC=S400V | S0;
564             break;
565         case 17:
566             RegUL=S2 | S8;
567             RegUC=S400V | S0;
568             break;
569         case 18:
570             RegUL=S2 | S8;
571             RegUC=S400V | S9;
572             break;
573         case 19:
574             RegUL=S2 | S7;
575             RegUC=S400V | S9;
576             break;
577         case 20:
578             RegUL=S2 | S6;
579             RegUC=S400V | S9;
580             break;
581         case 21:
582             RegUL=S2 | S5;
583             RegUC=S400V | S9;
584             break;
585         case 22:
586             RegUL=S2 | S4;
587             RegUC=S400V | S9;
588             break;
589         case 23:
590             RegUL=S2 | S3;
591             RegUC=S400V | S9;
```

```
592          break;
593       case 24:
594          RegUL=S2 | S3;
595          RegUC=S400V | S9;
596          break;
597      }
598 }
599 \\The end.
```

B.2 Microcontroller #2

```
1  //This is the operating code of the Microcontroller \#2. It is a ...
       ATMEL Mega2560 Microcontroller running on Arduino programming ...
       platform. The code is writting in C.
2  //by Minjie Chen 12/06/2011.
3
4  //including necessary communication packages
5  #include <Wire.h>
6
7      //setting up the registers
8      void setup(){
9      Wire.begin();
10     DDRC=B11111111;
11     DDRL=B00000000;
12     DDRA=B00000000;
13     DDRF=B11111111;
14     pinMode(52,OUTPUT);
15     pinMode(50,INPUT);
16     PORTC=0;
17 }
18
19 //initialing the state variables
20     int Busstate=0;
```

```
21      int realvol=0;
22      int readvol=0;
23      int ready=0;
24      int value=0;
25      int count=0;
26      float a=1.22;
27      float b=0.94;
28      int downthres=200;
29      int upthres=249;
30      float c=(upthres-downthres)/24;
31
32  //beginning the loop
33  void loop() {
34
35      //enabling the DAC, providing a falling edge
36      digitalWrite(52,LOW);
37
38      //reading in DAC values
39      readvol=PINL;
40
41      ready=digitalRead(50);
42      digitalWrite(52,HIGH);
43
44      realvol=readvol*a;
45
46      //reading in the Busstate from Microcontroller \#1.
47      Busstate=PINA;
48
49      //outputing Busstates to the oscilliscope for monitoring
50      PORTF=Busstate;
51
52      //if the periodic operating mode has not start, no feedback
53      if (ready == 0)
54      {
55          PORTC=0;
56      }
```

```
57
58      //beginning the feedback
59      else
60      {
61          //if the bus voltage has not entered the region fixed by ...
                the down threshold and up threshold
62          if (realvol<downthres)
63          {
64              //outputing the original value
65              value=realvol*b;
66          }
67          else
68          {
69              //outputing the artificial value
70              value=downthres+1.4*Busstate+(realvol-downthres)/24;
71              value=value*b;
72          }
73
74          //output-protective action
75          if (value>255)
76          {
77              value=255;
78          }
79
80          //output-protective action
81          if (value<0)
82          {
83            value=0;
84          }
85
86          //experimentally offsetting the output values
87          PORTC=value+7;
88      }
89  }
```

B.3 PLECS C-script Code

```
1  //This is the operating code of the PLECS simulation of the 2-6 ...
       SSC energy buffer. It is a ATMEL Mega2560 Microcontroller ...
       running on Arduino programming platform. The code is writting ...
       in C.
2  //by Minjie Chen 12/06/2011.
3  //including necessary packages
4  #include <math.h>
5
6  //defining input/output ports
7  #define V1 Input(0)
8  #define V2 Input(1)
9  #define V3 Input(2)
10 #define V4 Input(3)
11 #define V5 Input(4)
12 #define V6 Input(5)
13 #define V7 Input(6)
14 #define V8 Input(7)
15 #define I Input(8)
16
17 //main control functions
18 if (I≥0)
19 {
20     //outputing the control signal according to the bus voltage
21     //exceeding the operating range
22     if (V1 ≤ 100)
23     {
24         Output(0)=0;//FET10
25         Output(1)=1;//FET1
26         Output(2)=0;//FET2
27         Output(3)=1;//FET3
28         Output(4)=0;//FET4
29         Output(5)=0;//FET5
30         Output(6)=0;//FET6
```

```
31          Output(7)=0;//FET7
32          Output(8)=0;//FET8
33          Output(9)=1;//FET11
34      }
35      //state=0-1
36      if ((V1>100)&&(V1 ≤ 150))
37      {
38          Output(0)=0;//FET10
39          Output(1)=1;//FET1
40          Output(2)=0;//FET2
41          Output(3)=1;//FET3
42          Output(4)=0;//FET4
43          Output(5)=0;//FET5
44          Output(6)=0;//FET6
45          Output(7)=0;//FET7
46          Output(8)=0;//FET8
47          Output(9)=1;//FET11
48      }
49      //state=1-2
50      if ((V1>150)&&(V1 ≤ 200))
51      {
52          Output(0)=0;//FET10
53          Output(1)=1;//FET1
54          Output(2)=0;//FET2
55          Output(3)=0;//FET3
56          Output(4)=1;//FET4
57          Output(5)=0;//FET5
58          Output(6)=0;//FET6
59          Output(7)=0;//FET7
60          Output(8)=0;//FET8
61          Output(9)=1;//FET11
62      }
63      //state=2-3
64      if ((V1>200)&&(V1 ≤ 250))
65      {
66          Output(0)=0;//FET10
```

```
67          Output(1)=1;//FET1
68          Output(2)=0;//FET2
69          Output(3)=0;//FET3
70          Output(4)=0;//FET4
71          Output(5)=1;//FET5
72          Output(6)=0;//FET6
73          Output(7)=0;//FET7
74          Output(8)=0;//FET8
75          Output(9)=1;//FET11
76      }
77      //state=3-4
78      if ((V1>250)&&(V1 ≤ 300))
79      {
80          Output(0)=0;//FET10
81          Output(1)=1;//FET1
82          Output(2)=0;//FET2
83          Output(3)=0;//FET3
84          Output(4)=0;//FET4
85          Output(5)=0;//FET5
86          Output(6)=1;//FET6
87          Output(7)=0;//FET7
88          Output(8)=0;//FET8
89          Output(9)=1;//FET11
90      }
91      //state=4-5
92      if ((V1>300)&&(V1 ≤ 350))
93      {
94          Output(0)=0;//FET10
95          Output(1)=1;//FET1
96          Output(2)=0;//FET2
97          Output(3)=0;//FET3
98          Output(4)=0;//FET4
99          Output(5)=0;//FET5
100         Output(6)=0;//FET6
101         Output(7)=1;//FET7
102         Output(8)=0;//FET8
```

```
103             Output(9)=1;//FET11
104         }
105         //state=5-6
106         if ((V1>350)&&(V1 ≤ 400))
107         {
108             Output(0)=0;//FET10
109             Output(1)=1;//FET1
110             Output(2)=0;//FET2
111             Output(3)=0;//FET3
112             Output(4)=0;//FET4
113             Output(5)=0;//FET5
114             Output(6)=0;//FET6
115             Output(7)=0;//FET7
116             Output(8)=1;//FET8
117             Output(9)=1;//FET11
118         }
119         //state=6-7
120         if ((V1>400)&&(V1 ≤ 450))
121         {
122             Output(0)=1;//FET10
123             Output(1)=1;//FET1
124             Output(2)=0;//FET2
125             Output(3)=0;//FET3
126             Output(4)=0;//FET4
127             Output(5)=0;//FET5
128             Output(6)=0;//FET6
129             Output(7)=0;//FET7
130             Output(8)=1;//FET8
131             Output(9)=0;//FET11
132         }
133         //state=7-8
134         if ((V1>450)&&(V1 ≤ 500))
135         {
136             Output(0)=1;//FET10
137             Output(1)=1;//FET1
138             Output(2)=0;//FET2
```

```
139          Output(3)=0;//FET3
140          Output(4)=0;//FET4
141          Output(5)=0;//FET5
142          Output(6)=0;//FET6
143          Output(7)=1;//FET7
144          Output(8)=0;//FET8
145          Output(9)=0;//FET11
146      }
147      //state=8-9
148      if ((V1>500)&&(V1 ≤ 550))
149      {
150          Output(0)=1;//FET10
151          Output(1)=1;//FET1
152          Output(2)=0;//FET2
153          Output(3)=0;//FET3
154          Output(4)=0;//FET4
155          Output(5)=0;//FET5
156          Output(6)=1;//FET6
157          Output(7)=0;//FET7
158          Output(8)=0;//FET8
159          Output(9)=0;//FET11
160      }
161      //state=9-10
162      if ((V1>550)&&(V1 ≤ 600))
163      {
164          Output(0)=1;//FET10
165          Output(1)=1;//FET1
166          Output(2)=0;//FET2
167          Output(3)=0;//FET3
168          Output(4)=0;//FET4
169          Output(5)=1;//FET5
170          Output(6)=0;//FET6
171          Output(7)=0;//FET7
172          Output(8)=0;//FET8
173          Output(9)=0;//FET11
174      }
```

```
175     //state=10-11
176     if ((V1>600)&&(V1 ≤ 650))
177     {
178         Output(0)=1;//FET10
179         Output(1)=1;//FET1
180         Output(2)=0;//FET2
181         Output(3)=0;//FET3
182         Output(4)=1;//FET4
183         Output(5)=0;//FET5
184         Output(6)=0;//FET6
185         Output(7)=0;//FET7
186         Output(8)=0;//FET8
187         Output(9)=0;//FET11
188     }
189     //state=11-12
190     if ((V1>650)&&(V1<700))
191     {
192         Output(0)=1;//FET10
193         Output(1)=1;//FET1
194         Output(2)=0;//FET2
195         Output(3)=1;//FET3
196         Output(4)=0;//FET4
197         Output(5)=0;//FET5
198         Output(6)=0;//FET6
199         Output(7)=0;//FET7
200         Output(8)=0;//FET8
201         Output(9)=0;//FET11
202     }
203     if ((V1≥700))
204     {
205         Output(0)=0;//FET10
206         Output(1)=0;//FET1
207         Output(2)=1;//FET2
208         Output(3)=1;//FET3
209         Output(4)=0;//FET4
210         Output(5)=0;//FET5
```

```
211          Output(6)=0;//FET6
212          Output(7)=0;//FET7
213          Output(8)=0;//FET8
214          Output(9)=1;//FET11
215      }
216      //state=12-13
217      if ((V2>100)&&(V2 ≤ 150))
218      {
219          Output(0)=0;//FET10
220          Output(1)=0;//FET1
221          Output(2)=1;//FET2
222          Output(3)=1;//FET3
223          Output(4)=0;//FET4
224          Output(5)=0;//FET5
225          Output(6)=0;//FET6
226          Output(7)=0;//FET7
227          Output(8)=0;//FET8
228          Output(9)=1;//FET11
229      }
230      //state=13-14
231      if ((V2>150)&&(V2 ≤ 200))
232      {
233          Output(0)=0;//FET10
234          Output(1)=0;//FET1
235          Output(2)=1;//FET2
236          Output(3)=0;//FET3
237          Output(4)=1;//FET4
238          Output(5)=0;//FET5
239          Output(6)=0;//FET6
240          Output(7)=0;//FET7
241          Output(8)=0;//FET8
242          Output(9)=1;//FET11
243      }
244      //state=14-15
245      if ((V2>200)&&(V2 ≤ 250))
246      {
```

```
247             Output(0)=0;//FET10
248             Output(1)=0;//FET1
249             Output(2)=1;//FET2
250             Output(3)=0;//FET3
251             Output(4)=0;//FET4
252             Output(5)=1;//FET5
253             Output(6)=0;//FET6
254             Output(7)=0;//FET7
255             Output(8)=0;//FET8
256             Output(9)=1;//FET11
257         }
258         //state=15-16
259         if ((V2>250)&&(V2 ≤ 300))
260         {
261             Output(0)=0;//FET10
262             Output(1)=0;//FET1
263             Output(2)=1;//FET2
264             Output(3)=0;//FET3
265             Output(4)=0;//FET4
266             Output(5)=0;//FET5
267             Output(6)=1;//FET6
268             Output(7)=0;//FET7
269             Output(8)=0;//FET8
270             Output(9)=1;//FET11
271         }
272         //state=16-17
273         if ((V2>300)&&(V2 ≤ 350))
274         {
275             Output(0)=0;//FET10
276             Output(1)=0;//FET1
277             Output(2)=1;//FET2
278             Output(3)=0;//FET3
279             Output(4)=0;//FET4
280             Output(5)=0;//FET5
281             Output(6)=0;//FET6
282             Output(7)=1;//FET7
```

```
283             Output(8)=0;//FET8
284             Output(9)=1;//FET11
285         }
286         //state=17-18
287         if ((V2>350)&&(V2 ≤ 400))
288         {
289             Output(0)=0;//FET10
290             Output(1)=0;//FET1
291             Output(2)=1;//FET2
292             Output(3)=0;//FET3
293             Output(4)=0;//FET4
294             Output(5)=0;//FET5
295             Output(6)=0;//FET6
296             Output(7)=0;//FET7
297             Output(8)=1;//FET8
298             Output(9)=1;//FET11
299         }
300         //state=18-19
301         if ((V2>400)&&(V2 ≤ 450))
302         {
303             Output(0)=1;//FET10
304             Output(1)=0;//FET1
305             Output(2)=1;//FET2
306             Output(3)=0;//FET3
307             Output(4)=0;//FET4
308             Output(5)=0;//FET5
309             Output(6)=0;//FET6
310             Output(7)=0;//FET7
311             Output(8)=1;//FET8
312             Output(9)=0;//FET11
313         }
314         //state=19-20
315         if ((V2>450)&&(V2 ≤ 500))
316         {
317             Output(0)=1;//FET10
318             Output(1)=0;//FET1
```

```
319             Output(2)=1;//FET2
320             Output(3)=0;//FET3
321             Output(4)=0;//FET4
322             Output(5)=0;//FET5
323             Output(6)=0;//FET6
324             Output(7)=1;//FET7
325             Output(8)=0;//FET8
326             Output(9)=0;//FET11
327         }
328         //state=20-21
329         if ((V2>500)&&(V2 ≤ 550))
330         {
331             Output(0)=1;//FET10
332             Output(1)=0;//FET1
333             Output(2)=1;//FET2
334             Output(3)=0;//FET3
335             Output(4)=0;//FET4
336             Output(5)=0;//FET5
337             Output(6)=1;//FET6
338             Output(7)=0;//FET7
339             Output(8)=0;//FET8
340             Output(9)=0;//FET11
341         }
342         //state=21-22
343         if ((V2>550)&&(V2 ≤ 600))
344         {
345             Output(0)=1;//FET10
346             Output(1)=0;//FET1
347             Output(2)=1;//FET2
348             Output(3)=0;//FET3
349             Output(4)=0;//FET4
350             Output(5)=1;//FET5
351             Output(6)=0;//FET6
352             Output(7)=0;//FET7
353             Output(8)=0;//FET8
354             Output(9)=0;//FET11
```

```
355      }
356      //state=22-23
357      if ((V2>600)&&(V2 ≤ 650))
358      {
359          Output(0)=1;//FET10
360          Output(1)=0;//FET1
361          Output(2)=1;//FET2
362          Output(3)=0;//FET3
363          Output(4)=1;//FET4
364          Output(5)=0;//FET5
365          Output(6)=0;//FET6
366          Output(7)=0;//FET7
367          Output(8)=0;//FET8
368          Output(9)=0;//FET11
369      }
370      //state=23-24
371      if ((V2>650)&&(V2 ≤ 700))
372      {
373          Output(0)=1;//FET10
374          Output(1)=0;//FET1
375          Output(2)=1;//FET2
376          Output(3)=1;//FET3
377          Output(4)=0;//FET4
378          Output(5)=0;//FET5
379          Output(6)=0;//FET6
380          Output(7)=0;//FET7
381          Output(8)=0;//FET8
382          Output(9)=0;//FET11
383      }
384  }
385  ////////////////////DISCHARGE PERIOD//////////////////
386  if (I<0)
387  {
388      if (V2≥700)
389      {
390          Output(0)=0;//FET10
```

```
391             Output(1)=0;//FET1
392             Output(2)=1;//FET2
393             Output(3)=1;//FET3
394             Output(4)=0;//FET4
395             Output(5)=0;//FET5
396             Output(6)=0;//FET6
397             Output(7)=0;//FET7
398             Output(8)=0;//FET8
399             Output(9)=1;//FET11
400         }
401         //state=23-24
402         if ((V2>650)&&(V2 ≤ 700))
403         {
404             Output(0)=1;//FET10
405             Output(1)=0;//FET1
406             Output(2)=1;//FET2
407             Output(3)=1;//FET3
408             Output(4)=0;//FET4
409             Output(5)=0;//FET5
410             Output(6)=0;//FET6
411             Output(7)=0;//FET7
412             Output(8)=0;//FET8
413             Output(9)=0;//FET11
414         }
415         //state=22-23
416         if ((V2>600)&&(V2 ≤ 650))
417         {
418             Output(0)=1;//FET10
419             Output(1)=0;//FET1
420             Output(2)=1;//FET2
421             Output(3)=0;//FET3
422             Output(4)=1;//FET4
423             Output(5)=0;//FET5
424             Output(6)=0;//FET6
425             Output(7)=0;//FET7
426             Output(8)=0;//FET8
```

```
427             Output(9)=0;//FET11
428         }
429         //state=21-22
430         if ((V2>550)&&(V2 ≤ 600))
431         {
432             Output(0)=1;//FET10
433             Output(1)=0;//FET1
434             Output(2)=1;//FET2
435             Output(3)=0;//FET3
436             Output(4)=0;//FET4
437             Output(5)=1;//FET5
438             Output(6)=0;//FET6
439             Output(7)=0;//FET7
440             Output(8)=0;//FET8
441             Output(9)=0;//FET11
442         }
443         //state=20-21
444         if ((V2>500)&&(V2 ≤ 550))
445         {
446             Output(0)=1;//FET10
447             Output(1)=0;//FET1
448             Output(2)=1;//FET2
449             Output(3)=0;//FET3
450             Output(4)=0;//FET4
451             Output(5)=0;//FET5
452             Output(6)=1;//FET6
453             Output(7)=0;//FET7
454             Output(8)=0;//FET8
455             Output(9)=0;//FET11
456         }
457         //state=19-20
458         if ((V2>450)&&(V2 ≤ 500))
459         {
460             Output(0)=1;//FET10
461             Output(1)=0;//FET1
462             Output(2)=1;//FET2
```

```
463             Output(3)=0;//FET3
464             Output(4)=0;//FET4
465             Output(5)=0;//FET5
466             Output(6)=0;//FET6
467             Output(7)=1;//FET7
468             Output(8)=0;//FET8
469             Output(9)=0;//FET11
470         }
471         //state=18-19
472         if ((V2>400)&&(V2 ≤ 450))
473         {
474             Output(0)=1;//FET10
475             Output(1)=0;//FET1
476             Output(2)=1;//FET2
477             Output(3)=0;//FET3
478             Output(4)=0;//FET4
479             Output(5)=0;//FET5
480             Output(6)=0;//FET6
481             Output(7)=0;//FET7
482             Output(8)=1;//FET8
483             Output(9)=0;//FET11
484         }
485         //state=17-18
486         if ((V2>350)&&(V2 ≤ 400))
487         {
488             Output(0)=0;//FET10
489             Output(1)=0;//FET1
490             Output(2)=1;//FET2
491             Output(3)=0;//FET3
492             Output(4)=0;//FET4
493             Output(5)=0;//FET5
494             Output(6)=0;//FET6
495             Output(7)=0;//FET7
496             Output(8)=1;//FET8
497             Output(9)=1;//FET11
498         }
```

```
499     //state=16-17
500     if ((V2>300)&&(V2 ≤ 350))
501     {
502         Output(0)=0;//FET10
503         Output(1)=0;//FET1
504         Output(2)=1;//FET2
505         Output(3)=0;//FET3
506         Output(4)=0;//FET4
507         Output(5)=0;//FET5
508         Output(6)=0;//FET6
509         Output(7)=1;//FET7
510         Output(8)=0;//FET8
511         Output(9)=1;//FET11
512     }
513     //state=15-16
514     if ((V2>250)&&(V2 ≤ 300))
515     {
516         Output(0)=0;//FET10
517         Output(1)=0;//FET1
518         Output(2)=1;//FET2
519         Output(3)=0;//FET3
520         Output(4)=0;//FET4
521         Output(5)=0;//FET5
522         Output(6)=1;//FET6
523         Output(7)=0;//FET7
524         Output(8)=0;//FET8
525         Output(9)=1;//FET11
526     }
527     //state=14-15
528     if ((V2>200)&&(V2 ≤ 250))
529     {
530         Output(0)=0;//FET10
531         Output(1)=0;//FET1
532         Output(2)=1;//FET2
533         Output(3)=0;//FET3
534         Output(4)=0;//FET4
```

```
535          Output(5)=1;//FET5
536          Output(6)=0;//FET6
537          Output(7)=0;//FET7
538          Output(8)=0;//FET8
539          Output(9)=1;//FET11
540      }
541      //state=13-14
542      if ((V2>150)&&(V2 ≤ 200))
543      {
544          Output(0)=0;//FET10
545          Output(1)=0;//FET1
546          Output(2)=1;//FET2
547          Output(3)=0;//FET3
548          Output(4)=1;//FET4
549          Output(5)=0;//FET5
550          Output(6)=0;//FET6
551          Output(7)=0;//FET7
552          Output(8)=0;//FET8
553          Output(9)=1;//FET11
554      }
555      //state=12-13
556      if ((V2>100)&&(V2 ≤ 150))
557      {
558          Output(0)=0;//FET10
559          Output(1)=0;//FET1
560          Output(2)=1;//FET2
561          Output(3)=1;//FET3
562          Output(4)=0;//FET4
563          Output(5)=0;//FET5
564          Output(6)=0;//FET6
565          Output(7)=0;//FET7
566          Output(8)=0;//FET8
567          Output(9)=1;//FET11
568      }
569      if ((V2 ≤ 100))
570      {
```

```
571             Output(0)=1;//FET10
572             Output(1)=1;//FET1
573             Output(2)=0;//FET2
574             Output(3)=1;//FET3
575             Output(4)=0;//FET4
576             Output(5)=0;//FET5
577             Output(6)=0;//FET6
578             Output(7)=0;//FET7
579             Output(8)=0;//FET8
580             Output(9)=0;//FET11
581         }
582         //state=11-12
583         if ((V1>650)&&(V1<700))
584         {
585             Output(0)=1;//FET10
586             Output(1)=1;//FET1
587             Output(2)=0;//FET2
588             Output(3)=1;//FET3
589             Output(4)=0;//FET4
590             Output(5)=0;//FET5
591             Output(6)=0;//FET6
592             Output(7)=0;//FET7
593             Output(8)=0;//FET8
594             Output(9)=0;//FET11
595         }
596         //state=10-11
597         if ((V1>600)&&(V1 ≤ 650))
598         {
599             Output(0)=1;//FET10
600             Output(1)=1;//FET1
601             Output(2)=0;//FET2
602             Output(3)=0;//FET3
603             Output(4)=1;//FET4
604             Output(5)=0;//FET5
605             Output(6)=0;//FET6
606             Output(7)=0;//FET7
```

```
607             Output(8)=0;//FET8
608             Output(9)=0;//FET11
609         }
610         //state=9-10
611         if ((V1>550)&&(V1 ≤ 600))
612         {
613             Output(0)=1;//FET10
614             Output(1)=1;//FET1
615             Output(2)=0;//FET2
616             Output(3)=0;//FET3
617             Output(4)=0;//FET4
618             Output(5)=1;//FET5
619             Output(6)=0;//FET6
620             Output(7)=0;//FET7
621             Output(8)=0;//FET8
622             Output(9)=0;//FET11
623         }
624         //state=8-9
625         if ((V1>500)&&(V1 ≤ 550))
626         {
627             Output(0)=1;//FET10
628             Output(1)=1;//FET1
629             Output(2)=0;//FET2
630             Output(3)=0;//FET3
631             Output(4)=0;//FET4
632             Output(5)=0;//FET5
633             Output(6)=1;//FET6
634             Output(7)=0;//FET7
635             Output(8)=0;//FET8
636             Output(9)=0;//FET11
637         }
638         //state=7-8
639         if ((V1>450)&&(V1 ≤ 500))
640         {
641             Output(0)=1;//FET10
642             Output(1)=1;//FET1
```

```
643             Output(2)=0;//FET2
644             Output(3)=0;//FET3
645             Output(4)=0;//FET4
646             Output(5)=0;//FET5
647             Output(6)=0;//FET6
648             Output(7)=1;//FET7
649             Output(8)=0;//FET8
650             Output(9)=0;//FET11
651         }
652         //state=6-7
653         if ((V1>400)&&(V1 ≤ 450))
654         {
655             Output(0)=1;//FET10
656             Output(1)=1;//FET1
657             Output(2)=0;//FET2
658             Output(3)=0;//FET3
659             Output(4)=0;//FET4
660             Output(5)=0;//FET5
661             Output(6)=0;//FET6
662             Output(7)=0;//FET7
663             Output(8)=1;//FET8
664             Output(9)=0;//FET11
665         }
666         //state=5-6
667         if ((V1>350)&&(V1 ≤ 400))
668         {
669             Output(0)=0;//FET10
670             Output(1)=1;//FET1
671             Output(2)=0;//FET2
672             Output(3)=0;//FET3
673             Output(4)=0;//FET4
674             Output(5)=0;//FET5
675             Output(6)=0;//FET6
676             Output(7)=0;//FET7
677             Output(8)=1;//FET8
678             Output(9)=1;//FET11
```

```
679     }
680     //state=4-5
681     if ((V1>300)&&(V1 ≤ 350))
682     {
683         Output(0)=0;//FET10
684         Output(1)=1;//FET1
685         Output(2)=0;//FET2
686         Output(3)=0;//FET3
687         Output(4)=0;//FET4
688         Output(5)=0;//FET5
689         Output(6)=0;//FET6
690         Output(7)=1;//FET7
691         Output(8)=0;//FET8
692         Output(9)=1;//FET11
693     }
694     //state=3-4
695     if ((V1>250)&&(V1 ≤ 300))
696     {
697         Output(0)=0;//FET10
698         Output(1)=1;//FET1
699         Output(2)=0;//FET2
700         Output(3)=0;//FET3
701         Output(4)=0;//FET4
702         Output(5)=0;//FET5
703         Output(6)=1;//FET6
704         Output(7)=0;//FET7
705         Output(8)=0;//FET8
706         Output(9)=1;//FET11
707     }
708     //state=2-3
709     if ((V1>200)&&(V1 ≤ 250))
710     {
711         Output(0)=0;//FET10
712         Output(1)=1;//FET1
713         Output(2)=0;//FET2
714         Output(3)=0;//FET3
```

```
715             Output(4)=0;//FET4
716             Output(5)=1;//FET5
717             Output(6)=0;//FET6
718             Output(7)=0;//FET7
719             Output(8)=0;//FET8
720             Output(9)=1;//FET11
721         }
722         //state=1-2
723         if ((V1>150)&&(V1 ≤ 200))
724         {
725             Output(0)=0;//FET10
726             Output(1)=1;//FET1
727             Output(2)=0;//FET2
728             Output(3)=0;//FET3
729             Output(4)=1;//FET4
730             Output(5)=0;//FET5
731             Output(6)=0;//FET6
732             Output(7)=0;//FET7
733             Output(8)=0;//FET8
734             Output(9)=1;//FET11
735         }
736         //state=0-1
737         if ((V1>100)&&(V1 ≤ 150))
738         {
739             Output(0)=0;//FET10
740             Output(1)=1;//FET1
741             Output(2)=0;//FET2
742             Output(3)=1;//FET3
743             Output(4)=0;//FET4
744             Output(5)=0;//FET5
745             Output(6)=0;//FET6
746             Output(7)=0;//FET7
747             Output(8)=0;//FET8
748             Output(9)=1;//FET11
749         }
750     }
```

Bibliography

[1] S. G. Parler, Jr., *Selecting and Applying Aluminum Electrolytic Capacitors for Inverter Applications*, www.cornell-dubilier.com.

[2] A.C. Kyritsis, E.C. Tatakis, *A Novel Parallel Active Filter for Current Pulsation Smoothing on Single Stage Grid-Connected AC-PV Modules*, 11th European Conference on Power Electronics and Applications (EPE), Aalborg, Denmark, Sep. 2007.

[3] A.C. Kyritsis, N.P. Papanikolaou, and E.C. Tatakis, *Enhanced Current Pulsation Smoothing Parallel Active Filter for Single Stage Grid Connected AC-PV Modules*, Proceedings of the International Power Electronics and Motion Control Conference (EPE-PEMC), pp. 1287-1292, Poznan, Poland, Sep. 2008.

[4] T. Shimizu, K. Wada, and N. Nakamura, *Flyback-Type Single-Phase Utility-Interactive Inverter With Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System*, IEEE Transactions on Power Electronics, vol. 21, no. 5, pp. 1264-1272, Sep. 2006.

[5] S.B. Kjaer and F. Blaabjerg, *Design Optimization of a Single-Phase Inverter for Photovoltaic Applications*, Proceedings of the IEEE Power Electronics Specialists Conference (PESC), pp. 1183-1190, Acapulco, Mexico, Jun. 2003.

[6] P.T. Krein and R.S. Balog, *Cost-Effective Hundred-Year Life for Single-Phase Inverters and Rectifiers in Solar and LED Lighting Applications Based on Minimum Capacitance Requirements and a Ripple Power Port*, Proceedings of the IEEE Applied Power Electronics Conference (APEC), pp. 620-625, Washington, DC, Feb, 2009.

[7] B.J. Pierquet and D.J. Perreault, *Single-Phase Photovoltaic Inverter Topology with Series-Connected Power Buffer*, IEEE Energy Conversion Congress and Exposition (ECCE), Sept. 2010.

[8] A. Rufer and P. Barrade, *A Supercapacitor-Based Energy Storage System for Elevators with Soft Commutated Interface*, IEEE Transactions on Industry Applications, vol. 38, issue 5, pp. 1151-1159, Sept-Oct, 2002.

[9] S. Sugimoto, S. Ogawa, H. Katsukawa, H. Mizutani and M. Okamura, *A Study of Series-Parallel Changeover Circuit of a Capacitor Bank for an Energy Storage System Utilizing Electric Double-layer Capacitors*, Electrical Engineering in Japan, vol. 145, pp. 33-42, 2003.

[10] X. Fang, N. Kutkut, J. Shen and I. Batarseh, *Ultracapacitor Shift Topologies with High Energy Utilization and Low Voltage Ripple*, International Telecommunications Energy Conference (INTELEC), Orlando, FL, June 2010.

[11] D.J. Perreault, Unpublished Research Notes, Massachusetts Institute of Technology, 2010.

[12] M. Chen, Unpublished Research Notes, Massachusetts Institute of Technology, 2010.

[13] K.K. Afridi, Unpublished Research Notes, Massachusetts Institute of Technology, 2011.

[14] R.C.N. Pilawa-Podgurski, D. Giuliano, and D.J. Perreault, *Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer*, Proceedings of the IEEE Power Electronics Specialists Conference, pp. 4008 4015, Rhodes, Greece, Jun. 2008.

[15] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*, New York: Addison-Wesley, 1991, ch. 3