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# III-V CMOS: What have we learned from HEMTs?

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## Abstract

The ability of Si CMOS to continue to scale down transistor size while delivering enhanced logic performance has recently come into question. An end to Moore’s Law threatens to bring to a halt the microelectronics revolution: a historical 50 year run of exponential progress in the power of electronics that has profoundly transformed human society. The outstanding transport properties of certain III-V compound semiconductors make these materials attractive to address this problem. This paper outlines the case for III-V CMOS, harvests lessons from recent research on III-V High Electron Mobility Transistors (HEMTs) and summarizes some of the key challenges in front of a future III-V logic technology.

## 1. Introduction

For nearly 50 years, the microelectronics revolution has been characterized by “smaller is better,” the amazing realization that scaling down transistor size leads to increased transistor density, faster switching speed and enhanced power efficiency. A significant turn in this exhilarating ride took place in the last few years. Si CMOS scaling is now in a new phase of “power constrained scaling” in which the power density dissipated by logic CMOS chips has all but hit a limit of about 100 W/cm<sup>2</sup> [1]. Power density cannot increase much more without incurring in very substantial packaging and cooling costs that are impractical for most applications. Under power constrained scaling, continued transistor size scaling demands a reduction in operating voltage [2]. Trying to accomplish this while enhancing transistor performance has become increasingly difficult. Partly because of this, the operating voltage for CMOS has bottomed at around 1 V for the last few generations of technology. This hard limit poses a serious threat to further progress.

One way out of this is by introducing a new channel material with a much higher carrier velocity. This would allow further voltage scaling while continuing to enhance performance. A promising family of materials is III-V compound semiconductors. III-Vs are well known for their unique suitability for high frequency electronics. III-V-based integrated circuits are now widely used in communications and defense applications. Some of these are mission critical, such as space systems where exceedingly high reliability is essential. Others are mass-market and very cost-sensitive applications such as low-noise amplifiers and switches for smart phones. Of all alternatives that are being considered to extend the life of CMOS, III-Vs are the only materials with an established manufacturing and reliability record.

The barrier for insertion of a new channel material into the CMOS roadmap is huge. At the earliest insertion point that seems plausible today, the transistor gate length will be at most in the 10-15 nm range and its entire footprint will be less than 100 nm [2]. Tens of billions of transistors will be integrated together. To compound the mag-

nitude of the challenge, a disruptive technology such as one incorporating III-Vs, will need to deliver a substantial performance premium with respect to the best available scaled Si option (30-50% seems the minimum). It must also offer the promise of more than one scaled generation beyond the insertion node. All this has to be possible under cost-effective manufacturing and with unprecedented levels of reliability.

This paper reviews the case for III-V CMOS, summarizes the lessons learned from recent research on HEMTs, and outlines the challenges ahead.

## 2. The case for III-Vs: what have we learned from HEMTs?

The case for III-V CMOS is often made by bringing attention to the extraordinary electron mobility of certain III-Vs. For InGaAs or InAs,  $\mu_e$  can easily be 50 times higher than in Si at comparable sheet carrier density. Sometimes, the outstanding frequency response of III-V HEMTs is invoked. For example, we have reported a record  $f_T$  value of 644 GHz in InAs HEMTs [3].  $f_{max}$  values in excess of 1 THz have also been reported in these kinds of devices [4]. Arguments like this are very indirect because they do not consider what really matters for logic in a transistor.

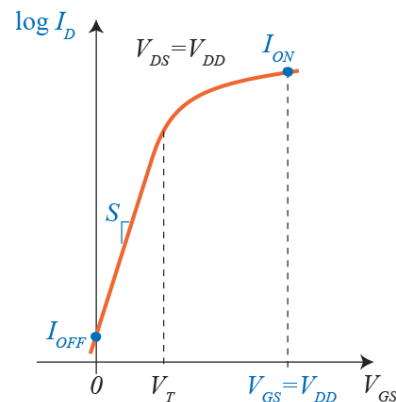


Fig. 1 - Sketch of subthreshold characteristics of a logic transistor defining  $I_{ON}$  and  $I_{OFF}$ .

In a logic gate, a transistor is operating as a switch that toggles between an ON state and an OFF state (Fig. 1). The current that flows in the ON state,  $I_{ON}$ , is desired to be high to allow fast switching. In the OFF state, the transistor should ideally be a perfect open but, inevitably, some residual current,  $I_{OFF}$ , flows.  $I_{OFF}$  matters because it contributes to the standby power consumption.

In a FET in saturation,  $I_{ON}$  is given by the product of the sheet carrier concentration at the virtual source times the injection velocity of electrons at the same point [5]. The virtual source is the bottleneck to carrier flow at the source-end of the channel and it is the electron velocity at this location,  $v_{inj}$ , the transport parameter that matters for logic applications. Recent measurements of  $v_{inj}$  in InGaAs and InAs HEMTs have revealed outstanding values [6]. A summary of the results is given in Fig. 2 that graphs  $v_{inj}$  for different channel compositions as a function of gate length. For reference, measurements of  $v_{inj}$  for Si MOSFETs are also shown (at 1.1-1.3 V).

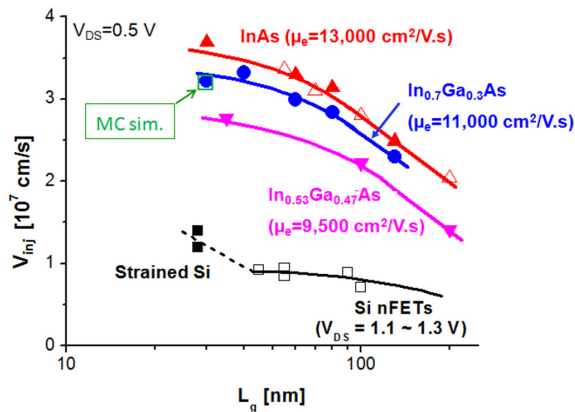


Fig. 2 - Injection velocity at the virtual source in InGaAs and InAs HEMTs as a function of gate length at  $V_{DD}=0.5$  V [6]. Measurements in bulk and strained Si CMOS are also included ( $V_{DD}=1.1-1.3$  V) [6]. The green square is the result of purely ballistic Monte Carlo simulations on an  $In_{0.7}Ga_{0.3}As$  HEMT [7].

Several conclusions can be extracted from this graph. First,  $v_{inj}$  values approaching  $4 \times 10^7$  cm/s are obtained for 30-40 nm gate length devices operating at only 0.5 V. This is more than twice as high as  $v_{inj}$  in Si at half the voltage. Second, for the materials that are shown,  $v_{inj}$  increases with the InAs composition in the channel. This is because of a reduction in electron effective mass. The third observation is that for  $L_g > 40$  nm,  $v_{inj}$  decreases as  $L_g$  increases while for shorter transistors,  $v_{inj}$  tends to saturate. This suggests that at around this gate length, the devices approach purely ballistic transport. This is further confirmed through ballistic Monte Carlo simulations of an  $L_g=30$  nm  $In_{0.7}Ga_{0.3}As$  channel HEMT which yield a value for  $v_{inj}$  virtually identical to the experimental measurement [7].

Sheet carrier concentration also enters in  $I_{ON}$ . A concern has been expressed about the low effective mass of the InAs-rich InGaAs family of compounds that might

make it difficult to obtain a high sheet carrier concentration in the channel at low voltages. Recent measurements of charge control in HEMTs suggest this to be less of a problem than originally believed. This is because the electron effective mass in the quantum-well of an InAs-rich InGaAs HEMT is substantially heavier than the bulk value [8]. This is due to quantization, non-parabolicity in the conduction band and biaxial compressive stress due to lattice mismatch.

The combination of a very high value of  $v_{inj}$  and reasonable channel effective mass confers InGaAs and InAs QW-FETs with the potential of delivering outstanding  $I_{ON}$  at reduced  $V_{DD}$ , something essential in future CMOS.

$I_{OFF}$  is just as important as  $I_{ON}$ . In quantum-well devices without source and drain junctions such as HEMTs,  $I_{OFF}$  is set by the subthreshold swing  $S$ , as shown in Fig. 1.  $S$  quantifies the sharpness of the drop of the drain current for  $V_{GS}$  values below  $V_T$  (the units are mV/dec so a small subthreshold swing is desired). In InAs and InGaAs HEMTs, the quantum nature of the channel has been shown to effectively confine electrons and yield outstanding subthreshold characteristics [9]. This is illustrated in Fig. 3 where  $S$  for InAs and InGaAs HEMTs with different channel thickness is plotted [9]. InAs HEMTs with a 5 nm thick channel exhibit subthreshold swings that barely increase as  $L_g$  is shunk to 40 nm and are significantly better than in Si MOSFETs (shaded region) [9].

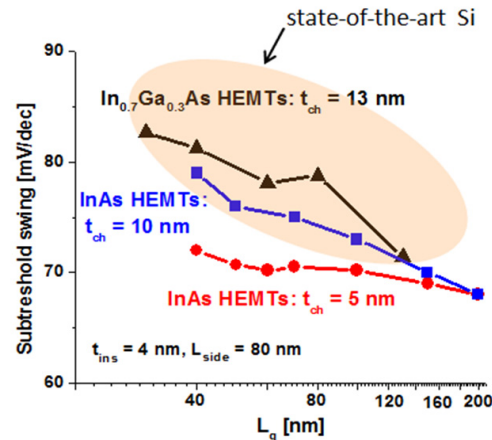


Fig. 3 - Subthreshold swing of InGaAs and InAs HEMTs with different channel thickness as a function of gate length. The shaded area represents values obtained in state-of-the-art Si MOSFETs.

Thinning down the channel does not come for free as scattering tends to increase which negatively affects transport. For example, for the data in Fig. 3, the InAs HEMTs with a 10 nm thick channel are characterized by  $\mu_e=13,000$   $cm^2/V.s$  at room temperature while the 5 nm thick InAs channel devices only yield  $9,950$   $cm^2/V.s$ . However, as argued above, what matters for a nm scale transistor is the injection velocity. As it turns out, the degradation in  $v_{inj}$  is much less severe. Recent measurements of  $v_{inj}$  in InAs HEMTs with a 5 nm thick channel yield values around

$3.3 \times 10^7$  cm/s at  $L_g=40$  nm [10], almost as high as those in much thicker channel devices (Fig. 2). It seems clear that a quantum-well based device architecture has potential to scale to very small dimensions.

A key goal of scaling is to maximize  $I_{ON}$  while moderating the increase in  $I_{OFF}$ . A suitable figure of merit that packages together these two important properties and allows the comparison of different transistor technologies is the  $I_{ON}$  that can be obtained for a given value of  $I_{OFF}$  at a certain  $V_{DD}$ . This figure of merit can be unambiguously defined even if the transistor does not have the “correct”  $V_T$ , as is commonly the case in experimental devices.

Fig. 4 shows this figure of merit for a standard  $I_{OFF}$  of 100 nA/ $\mu$ m and  $V_{DD}=0.5$  V for different transistors. Shown are some of our InAs HEMTs [11] as well as commercial Si CMOS scaled to 0.5 V [12]. In addition, projections for future Si CMOS based on the International Technology Roadmap for Semiconductors are also shown. This graph clearly shows that, according to this figure of merit, InAs FETs substantially outperform Si MOSFETs of similar gate length. The gap is more startling considering that the Si MOSFETs have a source resistance of about 80  $\Omega \cdot \mu$ m, while in the InAs HEMTs,  $R_s=230 \Omega \cdot \mu$ m. If this shortcoming can be addressed, substantially more performance is to be expected from a future InAs FET technology.

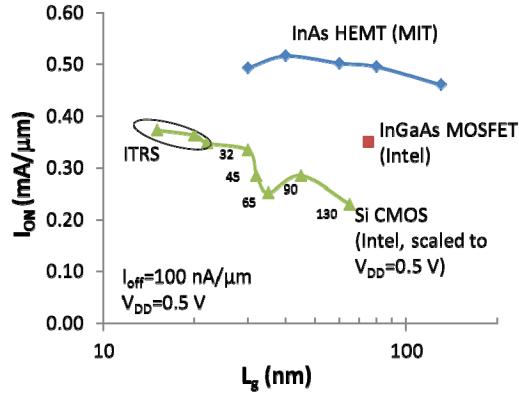


Fig. 4 –  $I_{ON}$  for an  $I_{OFF}$  of 100 nA/ $\mu$ m at  $V_{DD}=0.5$  V for InAs HEMTs and Si CMOS as a function of gate length. The Si CMOS data are based on Intel’s High Performance technologies scaled to 0.5 V operation. Also added are projections from the International Technology Roadmap for Semiconductors.

### 3. III-V CMOS device design and challenges

In spite of their impressive attributes, HEMTs are not suitable logic devices. The fundamental problem is gate leakage current which contributes to static power dissipation. At  $L_g=30$  nm, modern devices are already at the limit of what is tolerable. Further scaling will require proportional reductions in InAlAs barrier thickness that will make  $I_G$  increase exponentially. This is illustrated in Fig. 5 which shows a dramatic dependence of  $I_G$  with barrier thickness in  $L_g=30$  nm InAs HEMTs.

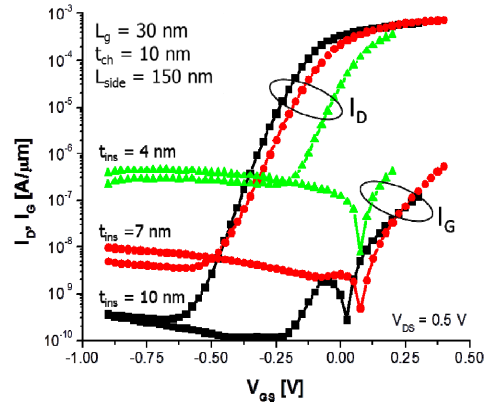


Fig. 5 –  $I_D$  and  $I_G$  in  $L_g=30$  nm InAs HEMTs with different InAlAs barrier thickness.

The only way forward is to insert a dielectric barrier in the gate stack that offers substantially higher conduction band discontinuity with the channel. Just like in Si CMOS, to meet the electrostatic integrity goals, a relatively high dielectric constant (“high K”) will be required.

This brings us to discuss likely architectures for future III-V CMOS transistors. From HEMTs we have learned that at their heart these devices should have a very thin quantum well channel. To preserve electrostatic integrity at the required dimensions, the source and drains must also be raised. Two broadly different designs emerge. They are both illustrated in Fig. 6.

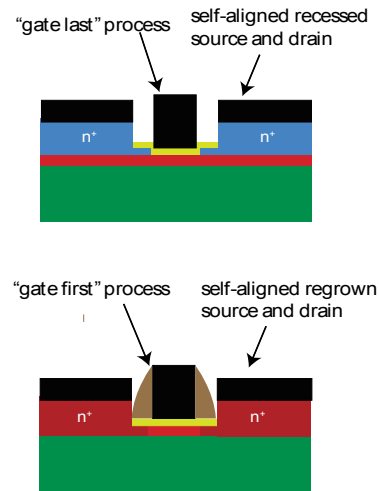


Fig. 6 – Conceptual schematic of two possible types of planar III-V QW-FETs for III-V CMOS.

The top design features source and drain regions that are grown with the original heterostructure and are then recessed to make space for a self-aligned gate. An advantage of this design is that the quantum well extends all the way underneath the source and drain and high mobility transport is preserved in the extrinsic device. A second advantage is that the gate/dielectric interface is formed relatively late in the process providing substantial process flexibility. A recent  $L_g=75$  nm InGaAs MOSFET with

this broad design has yielded outstanding electrical characteristics [13]. At an  $I_{\text{OFF}}=100$  nA/mm and  $V_{\text{DD}}=0.5$  V, the  $I_{\text{ON}}$  of this device already outperforms Si MOSFETs, as shown in Fig. 4 (red square).

A second possible device design is shown at the bottom of Fig. 6. In this device architecture, the gate stack is formed early in the process. Using the gate as a mask, the channel is etched away from the extrinsic portion of the heterostructure and then the source and drain regions are epitaxially grown in a self-aligned way. A potential advantage of this approach is the ability to introduce uniaxial strain in the channel. Prototype devices of this kind have been fabricated exhibiting promising electrical characteristics [14].

Regardless of device design, the introduction of a III-V channel into CMOS will represent the greatest disruption in the 50 year history of this technology. The challenges are enormous. The development of a reliable and manufacturable gate stack that includes a high-K dielectric and yields a high-quality interface is perhaps the greatest one. Recent research has shown the great promise of *ex-situ* Atomic Layer Deposition (ALD) as a deposition technique for high-K dielectrics on suitably treated InGaAs surfaces [13]. Through ALD, the bonding structure at the III-V interface can be appropriately engineered and a low density of interface states can be obtained [15].

Transistor size scalability is also a major worry. It is not obvious that future III-V transistors will be able to scale to the required dimensions while preventing excessive short-channel effects and attaining the demanding parasitic resistance objective. If we were to scale the extrinsic region of today's record HEMTs to the dimensions required in a future 10 nm III-V MOSFET, its external resistance would be about two orders of magnitude too high [16]. The problem does not seem fundamental as the conductivity of heavily doped InGaAs and the contact resistance to InGaAs are both as good as in Si [16].

If planar devices do not yield the required short-channel effects at the desired dimensions, 3D designs might offer a viable approach. In Si, FinFETs and nanowire transistors are serious contenders for the 22 nm CMOS node and perhaps beyond. Recent 3D device demonstrations in III-Vs give hope also to this avenue. GaAs FinFETs and InAs nanowire transistors with impressive characteristics have been demonstrated recently [18,19]. This bodes well to the potential of III-V FETs with 3D device designs.

CMOS requires n-channel as well as p-channel devices. In most III-Vs, the hole mobility is rather small, in fact, for many arsenides it is actually lower than in Si. This is a serious problem. A path to enhancing the hole transport characteristics is to introduce strain. This has been done very successfully in Si where thanks to strain, the p-channel device now exhibits a performance that approaches that of the n-MOSFET [20]. The gains that can be expected from strain using the arsenides are unclear at this point. An alternative approach is to use the antimonides in which mobilities in the  $1500$  cm<sup>2</sup>/V.s range have been measured [21]. Yet a third path is to rely on Ge transistors where the hole mobility is quite high and it can also be enhanced through strain [22]. This suggests a possi-

ble CMOS platform with Ge and a III-V transistors integrated side by side [23].

To complete the list of major challenges, a future III-V CMOS technology will also have to “look and feel” as much as Si as possible. This will insure that it can take advantage of the economy of scale of the Si industry. The proper view for III-V CMOS seems closer to the introduction of an enhancement to Si CMOS through the insertion of a III-V channel than a disruptive new technology. In this view, it is imperative to create thin high-quality III-V layers on top of large Si wafers. The challenge is compounded if two dissimilar materials are required to separately optimize the n- and p-channel devices.

## Conclusions

The introduction of III-Vs into Si CMOS offers the potential for reinvigorating Moore's law. III-Vs have already shown their worth at the front end of many communications systems. In the not too distant future, III-Vs could well be at the heart of mainstream electronics.

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