THE DESIGN AND REALIZATION OF HIGHER ORDER VARACTOR FREQUENCY MULTIPLIERS

by

JOSEPH FRANCIS BALCEWICZ

S. B., Massachusetts Institute of Technology
1966

SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
MASTER OF SCIENCE
at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
June, 1967

Signature of Author _____
Department of Electrical Engineering, May 25, 1967

Certified by _____
Thesis Supervisor

Accepted by _____
chairman, Departmental Committee on Graduate Students

THE DESIGN AND REALIZATION OF HIGHER ORDER VARACTOR FREQUENCY MULTIPLIERS

by

JOSEPH FRANCIS BALCEWICZ

Submitted to the Department of Electrical Engineering on May 25, 1967 in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

A solid-state UHF signal source is quite desirable from the point of view of low power consumption and noise. It has been proposed to frequency multiply an existing VHF source into the UHF range by using a high order varactor multiplier. A 249.1 Mhz source is available and realizable varactor sextupler will be designed to provide a low S-band source at 1494.6 Mhz.

The varactor diode, under the condition of reverse bias, exhibits a non-linear junction capacitance. This effect generates a series of harmonics of the drive frequency. Thus, the problem in designing a frequency multiplier is to find some sort of imbedding network that will match the diode's impedance values at the harmonics we wish to be present. The impedance specifications for this network have been previously determined so this thesis is involved in discovering a method of physically realizing the imbedding network.

The impedance specifications depend strongly on the maximum value of the junction elastance. A procedure for measuring this value as well as such diode parameters as the series resistance and reverse breakdown voltage has been described and the results presented for a sample of Motorola varactor diodes.

A low-pass input filter was designed for the multiplier to prevent any unwanted excitations of the diode. A band-pass output filter, centered about the sixth harmonic, was also designed to prevent any spurious responses in the output of the multiplier.

Two possible realizations of the imbedding network are derived. One, the shorted stub structure, is analogous to the low frequency realizations of varactor multipliers. The other, a transformer structure, is a single unit which matches the proper impedance levels.

A major feature of this research is in the use of a computer for much of the analysis and design. The diode junction elastance

versus space charge layer stored charge characteristics were derived by computer analysis of capacitance versus reverse voltage data.

In addition, the design of the low-pass input filter and the transformer imbedding network was done on a computer. The input filter was constructed and a comparison is made between the predicted and actual characteristics of this filter.

Thesis Supervisor: Robert P. Rafuse

Title: Associate Professor of Electrical Engineering

ACKNOWLEDGEMENTS

I would like to express my deep appreciation to Doctor Robert P. Rafuse for agreeing to supervise this thesis and for his constant interest in the results determined. I would also like to thank Donald H. Steinbrecher for the many ideas and contributions he has made to this research.

TABLE OF CONTENTS

LIST OF FIGURE CAPTIONS

LIST OF TABLE TITLES

CHAPTER 0

A PRELIMINARY DISCUSSION

Section 0.1 - Introduction

There has been much controversy lately about the use of varactor, step-recovery, diodes for frequency multiplication in the UHF and microwave ranges. It would be very useful to be able to develope a highly efficient microwave frequency multiplier, for this step would ultimately yield a high power microwave signal source. Multiplying an existing solid-state VHF source into the microwave spectrum by an efficient method such as the varactor multiplier would produce a completely solid-state (and thus efficient) source of microwave energy.

In the present case, a crystal controlled, phase-locked source at a frequency of 249.1 Mhz is available and a realizable varactor sextupler will be designed to multiply this input frequency up to 1494.6 Mhz (low S-band).

Section 0.2 - The Step-Recovery Diode

A step-recovery diode is one in which the junction capacitance as a function of the reverse bias voltage has a well defined minimum value (or the elastance has a maximum value). Figure 0.1 shows a typical graph of a step-recovery diode's elastance under reverse bias. The details of how these measurements were carried out are given in Chapter I.

The model that will be used for the diode under the reverse bias condition is given in Figure 0.2. $C(V)$ is the junction capacitance and R_S is the bulk series resistance of the diode. It is assumed to be constant for all values of reverse bias. The details of how the measurement of R_S was carried out is also given in Chapter I.

The theory of varactor frequency multiplication was presented in a book by Paul Penfield, Jr. and Robert P. Rafuse entitled Varactor Applications, (M. I. T. Press - 1962). In it, the efficiency of a 1-2-3-6 and a 1-2-4-6 varactor sextupler was derived.

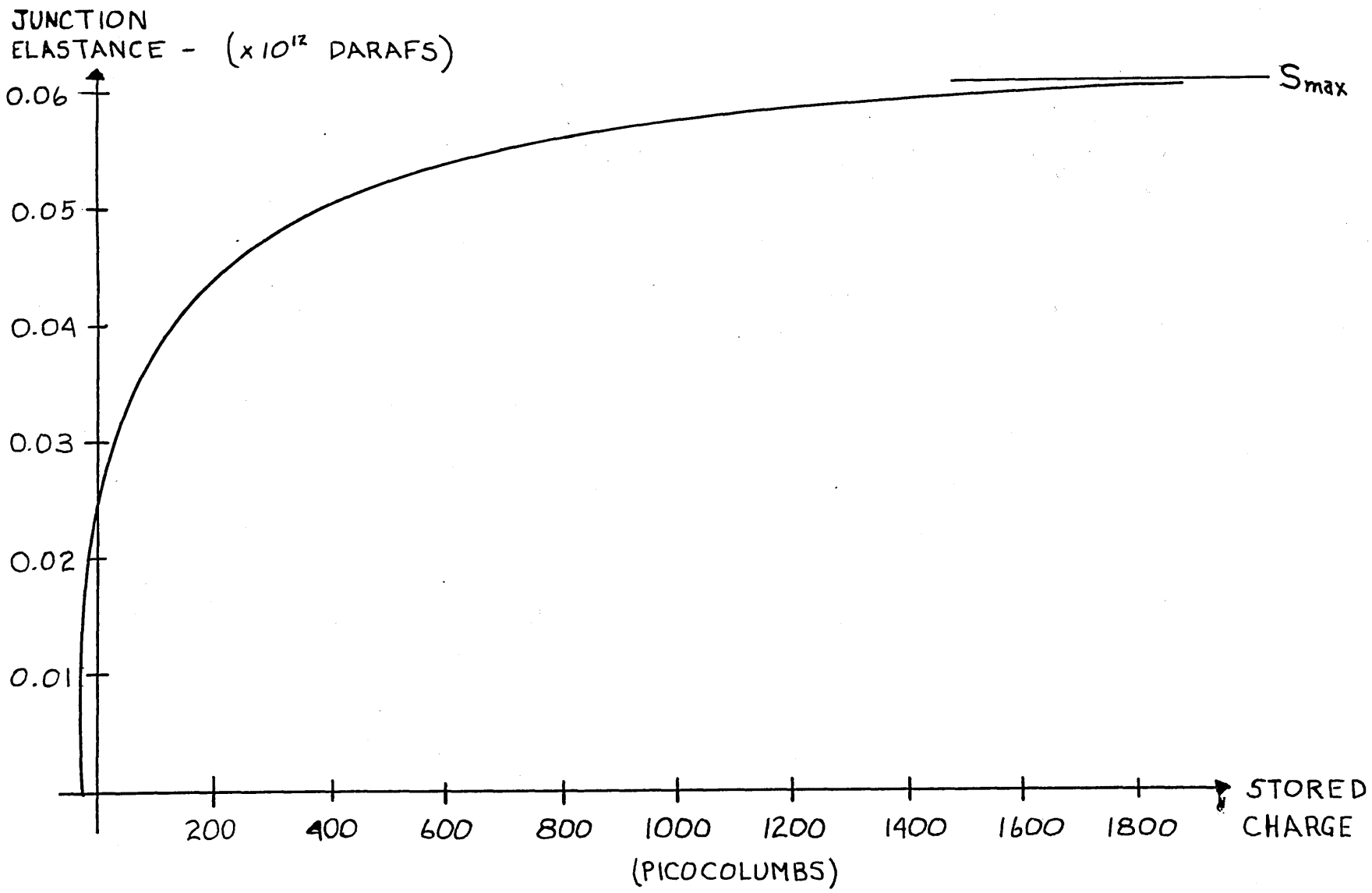

FIGURE 0.1 - JUNCTION ELASTANCE VERSUS STORED CHARGE — MOTOROLA TYPE MV 1805-C DIODE

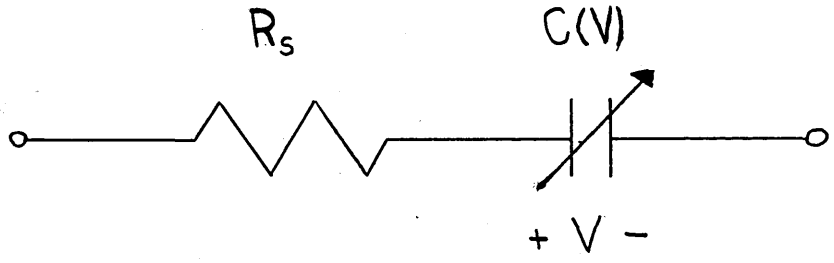

FIGURE 0.2

MODEL FOR A REVERSE BIASED STEP-RECOVERY VARACTOR DIODE. JUNCTION CAPACITANCE IS A NON-LINEAR FUNCTION OF THE REVERSE BIAS VOLTAGE.

(The former configuration implies idlers at the second and third harmonics and the latter implies idlers at the second and fourth harmonics). The efficiency is given in terms of the diode's cut-off frequency, f_c, which is given below in eq. 0.1,

$$f_c = \frac{S_{max} - S_{min}}{2\pi R_s} \quad , \qquad (0.1)$$

where S_{max} and S_{min} are the maximum and minimum values of junction elastance respectively.

For a typical diode measured (see Fig. 0.1) S_{max} is approximately 6×10^{10} darafs and S_{min} is approximately 0. R_s for a typical diode is around .15 ohms so we can calculate a cut-off frequency of about $f_c = 63.6$ Ghz. Thus, an input frequency of 249.1 Mhz is $3.9 \times 10^{-3} \times f_c$. Using Figures 8.46 and 8.50 given in Varactor Applications, the maximum predicted efficiency for a 1-2-3-6 sextupler is 62% and for the 1-2-4-6 sextupler is 69%.

Futhermore, it is felt that if idlers are included at each intermediate frequency, then a still greater efficiency will be possible. So, with this assumption, a 1-2-3-4-5-6 sextupler will be designed.

An interesting side note is some results published in July 1965 in -hp associates- Application Note #8, entitled, "Frequency Multiplication with the Step Recovery Diode". In it is presented a graph of the predicted efficiency of a frequency multiplier operated at an input frequency of 100 Mhz and using the rectification characteristics of a forward biased diode instead of the non-linear capacitance characteristic of the reverse biased varactor. The diode used in their multiplier was an -hpa- 0241 step-recovery diode with a $C_{min} = 3.3$ pf, an $R_s = .3$ ohms and a cut-off frequency of 160 Ghz.

Their expected efficiency for a sextupler is approximately 59% while the same diode, operated under reverse bias in a 1-2-4-6 configuration would yield (according to Penfield and Rafuse) a 94% efficiency. This extra efficiency, amounting to an extra 2db saving in output power, is the motivation for attempting to design

a realizable reverse biased, varactor sextupler.

Section 0.3 - The Synthesis of a Realizable Multiplier

Figure 0.3 is a shematic representation of the frequency multiplier. In this case, if ω_o is the input frequency then a frequency of $6\omega_o$ is delivered to the load. The imbedding network consists of the idler structure, bias network and any filters it may be necessary to use.

Regardless of the composition of the imbedding network, it has been determined that the impedance as seen by the diode, $Z(\omega)$, must be given by the following equations - (see "Efficiency Limits for Tuned Harmonic Multipliers with Punch-Through Varactors", by Donald H. Steinbrecher - M. I. T. - Research Laboratory of Electronics):

$$
\begin{aligned}
Z(\omega_o) &= A\frac{S_{max}}{\omega_o} + j\frac{S_{max}}{2\omega_o} \\
Z(2\omega_o) &= j\frac{S_{max}}{4\omega_o} \\
Z(3\omega_o) &= j\frac{S_{max}}{6\omega_o} \\
Z(4\omega_o) &= j\frac{S_{max}}{8\omega_o} \\
Z(5\omega_o) &= j\frac{S_{max}}{10\omega_o} \\
Z(6\omega_o) &= j\frac{S_{max}}{12\omega_o} \\
|Z(7\omega_o)| &>> \frac{S_{max}}{12\omega_o}
\end{aligned}
\qquad (0.2)
$$

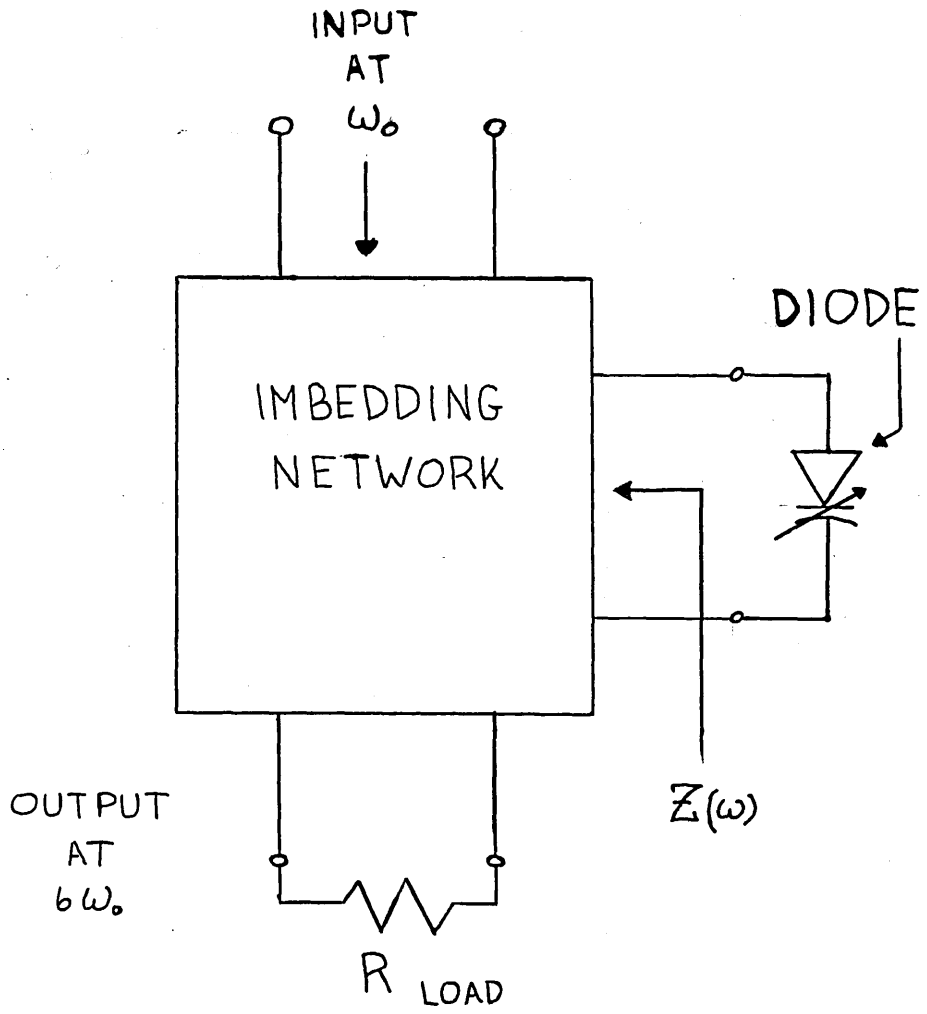

FIGURE 0.3

SCHEMATIC DIAGRAM OF A VARACTOR FREQUENCY SEXTUPLER. $Z(\omega)$ IS SPECIFIED IN EQUATIONS 0.2.

$$|Z(8\omega_o)| >> \frac{S_{max}}{12\omega_o}$$

$$|Z(9\omega_o)| >> \frac{S_{max}}{12\omega_o} \quad , \tag{0.2}$$

where A = 0.337 and B = 0.083. Using a value of $S_{max} = 6 \times 10^{10}$ darafs and $\omega_o = 2\pi \times 249.1 \times 10^6/\text{sec} = 1.57 \times 10^9/\text{sec}$ we have the following impedance values (in ohms).

$$Z(\omega_o) = 12.87 + j(19.1)$$

$$Z(2\omega_o) = j(9.55)$$

$$Z(3\omega_o) = j(6.37)$$

$$Z(4\omega_o) = j(4.78)$$

$$Z(5\omega_o) = j(3.82) \tag{0.3}$$

$$Z(6\omega_o) = 3.18 + j(3.18)$$

$$\left.\begin{matrix} |Z(7\omega_o)| \\ |Z(8\omega_o)| \\ |Z(9\omega_o)| \end{matrix}\right\} >> 3.18 \quad .$$

The values given in equations 0.3 are to be synthesized by two different means. The first method bears a close resemblance to the low frequency synthesis of varactor multipliers. Essentially the diode is connected to a circuit which resonates at a specific intermediate idler frequency and thus eliminates this frequency from the output of the multiplier. In the low frequency design, these idlers take the form of either series or parallel L-C circuits. In the UHF design, these idlers may be realized by the use of shorted lenghts of coax with a suitable tuning capacitor. This method of realizing the idler network is discussed in Chapter III.

Another and more aesthetically pleasing method of realizing the required impedance values is to use some sort of transformer structure (shown in Figure 3.2). The analysis of this type of structure is carried out on a computer and a suitable design can be found.

The compactness of this latter structure is its major feature as far as constructing a working model goes.

In addition, the method of computer-aided-design for microwave circuits that was used for determining the parameters of this structure and also the parameters for the low-pass input filter may prove to be a valuable method of designing microwave circuits. It is very difficult to "breadboard" a microwave circuit as one would a lumped element circuit and so the use of a computer may prove quite useful for the design and optimization of UHF and microwave circuitry.

CHAPTER I
DETERMINING THE DIODE PARAMETERS

Section 1.1 - Introduction

It is important to be able to measure the diode parameters. Both R_S and C(V), the circuit elements comprising the reverse bias model for the diode (Fig. 0.2), must be determined as well as such parameters as the breakdown voltage, V_B, and the contact potential, ϕ. V_B and ϕ are defined here in the same way as in the literature concerning low frequency P-N junction devices. V_B is the reverse voltage at which avalanche multiplication occurs and thus the reverse voltage cannot exceed this value. ϕ is the voltage that exists across the P-N junction when the diode has no applied voltage across it.

The necessity for knowing C(V) lies in the fact that the minimum value of C(V) appears in eqs. 0.2, the required impedance of the imbedding network, ($S_{max} = \frac{1}{C_{min}}$). Thus, the imbedding structure that is designed must be designed for a specific diode with a specific S_{max}.

R_s, V_B and ϕ are necessary because these values, in some sense, determine the maximum power handling capability of a diode and therefore, of a frequency multiplier. The "normalization power", P_{norm}, for a diode is given in equation 1.1 below,

$$P_{norm} = \frac{(V_B + \phi)^2}{R_S} \quad . \tag{1.1}$$

The greater P_{norm}, the greater is the power that a varactor multiplier can inherently handle.

For a typical case, let V_B = 100 volts, ϕ = .4 volts and R_s = 1 ohms. This yields a P_{norm} of about 10^4 watts demonstrating that we may expect large power outputs (around 10^{-3} X P_{norm}) from these varactor frequency multipliers. It can also be seen from this example that the contact potential is always much less than break-

down voltage so ϕ will be ignored in the following discussions.

This chapter will be involved with describing the methods used to measure the remaining parameters and with presenting the results of these measurements.

Section 1.2 - The Measurement of R_S

The series resistance in the reverse bias diode model (Fig.0.2) is assumed to be constant for all frequencies and all power levels. In the actual diode, R_S results from the bulk resistance of the semiconductor material used to make diode. The measurements will be made on eight Motorola MV 1805 - C varactor diodes at a frequency of 500 Mhz.

Figure 1.1 is a schematic diagram of the test jig used in the R_S measurement. It essentially consists of a half-wavelength long, (11.8 inches), section of 15 ohm, rigid, coaxial transmission line. At the quater-wavelength point, there is a perpendicular tuning stub with the diode imbedded in the inner conductor of the stub. Tuning of the stub, is accomplished by inserting a certain amount of dielectric material in the space between the stub's inner and outer conductors. This varies the characteristic impedance of a part of the stub and allows the stub to be tuned.

The bias scheme for the diode consists of a hole with a spring in it. The spring, which is self-resonant at 500 Mhz, makes electrical contact with the diode and thus provides a certain amount of reverse bias.

The half-wavelength long line is driven at one end by a 500 Mhz source and the power transmitted through the line is read at the other end on a power meter. First the transmitted power with no tuning stub is read and then the transmitted power with the diode and tuning stub in place is read. The difference between these two values for transmitted power is a measure of R_S plus any other losses in the tuning stub. These additional tuning stub looses may be determined by using a solid brass "diode" ($R_S = 0$) and measuring the change in transmitted power. In this case, since there is no diode resistance, the difference in transmitted power is due to the stub's losses.

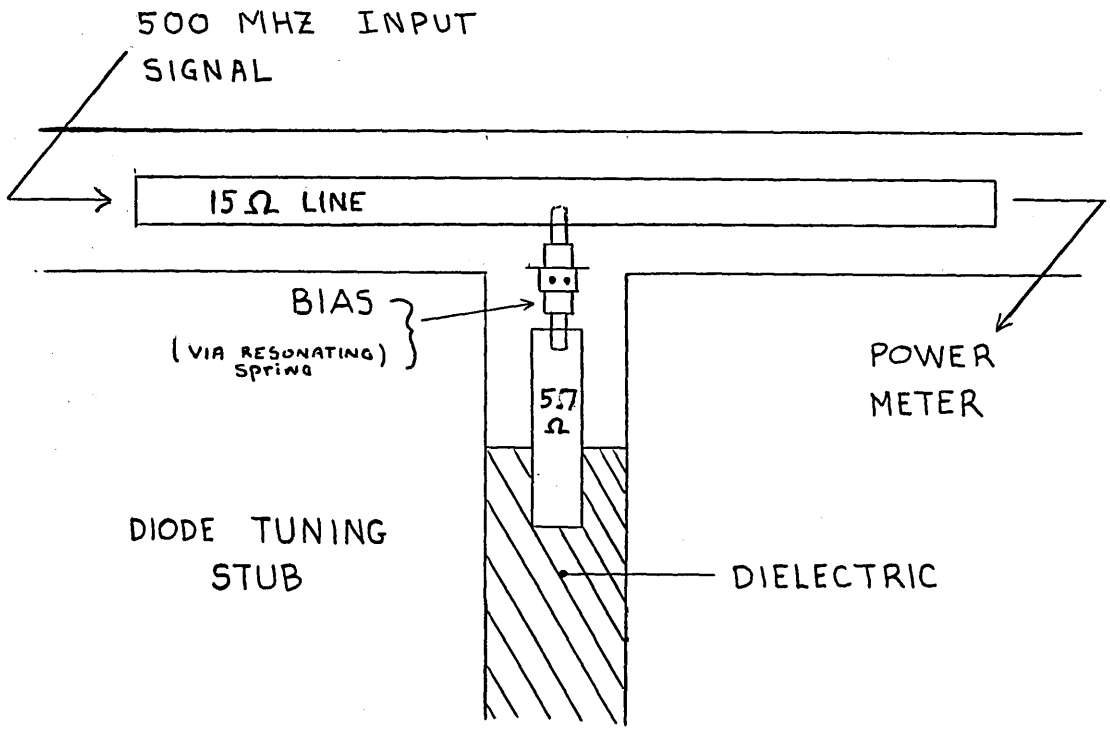

FIGURE 1.1

SCHEMATIC DIAGRAM OF R_s MEASUREMENT TEST JIG.

If the ratio of power transmitted without the stub to power transmitted with the diode and the stub (in db) is G, then

$$G = 10 \log_{10} \left(\frac{P_{\tau,\text{WITHOUT}}}{P_{\tau,\text{WITH}}} \right) \quad . \tag{1.2}$$

In a low frequency model of this situation,

$$P_{\tau,\text{WITHOUT}} = \frac{V^2_{\text{WITHOUT}}}{R_{\text{load}}} \quad ,$$

and

$$P_{\tau,\text{WITH}} = \frac{V^2_{\text{WITH}}}{R_{\text{load}}} \quad . \tag{1.3}$$

Where R_{load} is the load resistance seen at the quarter-wave point, $V_{without}$ is the voltage across the load without the diode and stub and V_{with} is the voltage across the load with the diode and stub.

Let

$$L = \frac{V_{\text{WITHOUT}}}{V_{\text{WITH}}} \quad , \tag{1.4}$$

then, by substituting this back into equation 1.2 we have:

$$G = 10 \log_{10}(L) \quad . \tag{1.5}$$

Furthermore, in the low frequency analogy, R_{load} is the power meter's input impedance transformed back a quater-wavelength. So, if a 100 ohm thermistor mount is used, then

$$R_{load} = \frac{(15)^2}{100} = 2.25\ \Omega. \tag{1.6}$$

Also, the maximum value of impedance for the diode-tuning stub combination, when the imaginary part of the impedance is tuned out, is just $\frac{Z_{os}^2}{R_s + R_t}$, where R_t is the losses due to the tuning stub, ($R_s + R_t < Z_{os}$, the characteristic impedance of the stub, equal to 5.7 ohms).

Now, using a voltage divider relationship, we have for L:

$$L = \frac{1}{\frac{R_{load}}{R_{load} + \frac{Z_{os}^2}{R_s + R_t}}}$$

or

$$L = \frac{32.5}{2.25(R_s + R_t)} + 1 \quad . \tag{1.7}$$

Solving now for R_s:

$$R_s = \frac{14.4}{L-1} - R_t \quad . \tag{1.8}$$

If the brass "diode" is used to find R_t, then:

$$\begin{aligned} G &= 29 \text{ db}, \\ L &= 28.1, \text{ (from eq. 1.5)} \\ \text{and } R_t &= .533 \text{ ohms, (from eq 1.8 with } R_s = 0). \end{aligned} \tag{1.9}$$

So finally, the equation for R_s is:

$$R_s = \frac{14.4}{L-1} - .533 \text{ ohms} \tag{1.10}$$

This method was then applied to the eight Motorola diodes with the results summarized in Table 1.1.

Table 1.1 - A Summary of R_s values

Diode Number	G	L	R_s (in ohms)
1	18.1 db	8.04	1.517
2	19.5 db	9.44	1.177
3	22.0 db	12.6	.708
4	24.4 db	16.6	.370
5	20.2 db	10.2	1.033
6	21.0 db	11.2	.879
7	19.0 db	8.92	1.285
8	19.2 db	9.12	1.242

It should be noted that the d.c. series resistance is between 11 and 13 ohms for these varactor diodes.

This method then, is a straight-forward way to determine the bulk a.c. series resistance of a varactor diode at a frequency of 500 Mhz.

Section 1.3 - The Measurement of C(V) and V_B

The capacitance that exists across the junction of the varactor diodes is of prime importance since it determines the impedance values that the diode must see if it is to be matched in the sextupler that will be designed.

Basically, the C(V) measurement is done on a Boonton Capacitance Bridge. An external D.C. bias voltage is fed into the Bridge and this produces the required reverse bias condition for the diode.

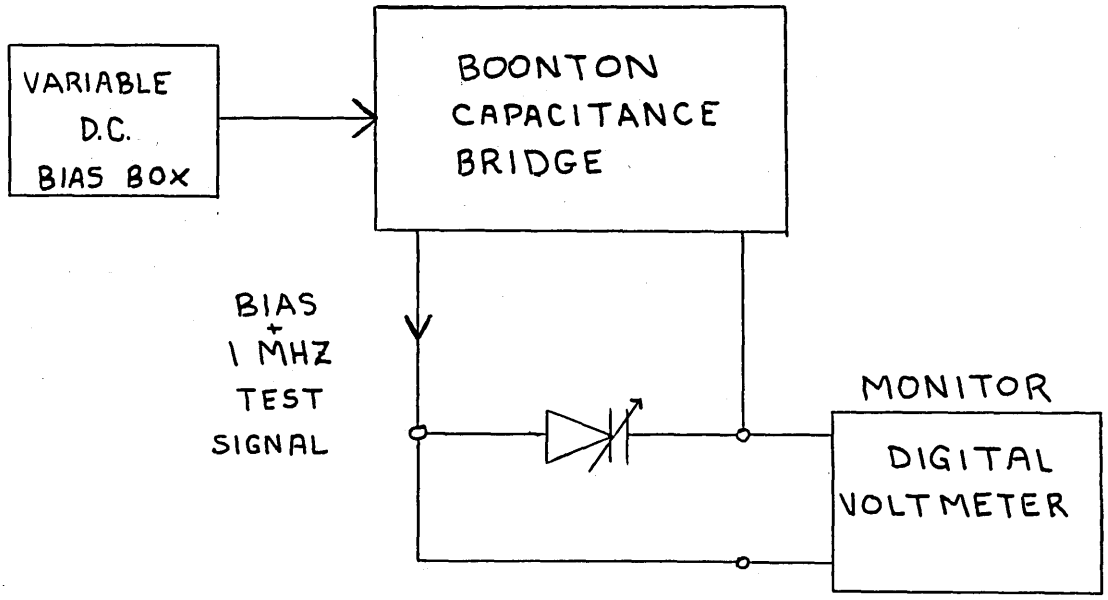

FIGURE 1.2

SCHEMATIC DIAGRAM OF TEST SETUP FOR C(V) MEASUREMENTS.

The value of diode capacitance (which also includes the capacitance of the casing and the leads) is read from the Bridge for various value of reverse bias voltage from 0 to the breakdown voltage. These measurements were made on the eight Motorola diodes at a frequency of 1 Mhz. Figure 1.2 is a block diagram of the test setup.

After the capacitance values were taken for a specific diode, they were fed into the computer and a program known as LØADGØ INTEG would calulate the elastance values (equal to the reciprocal of the capacitance values) and numerically integrate the capacitance-voltage function to obtain a value for the charge stored in the space-charge layer of the diode.

The equation relating a change in stored charge to a change in capacitance and voltage is:

$$dQ = d[VC(V)]; \tag{1.11}$$

remember that C is not constant. So the charge, Q_o, at some value of reverse bias boltage, V_o, is given by:

$$Q_o = \int_0^{V_o} d[VC(V)] \quad) \tag{1.12}$$

and it is this integral that the computer evaluates. The data for the elastance versus stored charge plot (Fig. 0.1) was obtained from the print-out for one of these diodes.

The reverse breakdown voltage may be determined in one of two ways. First, when the values of C(V) are being taken, it can be observed that there is a point where the bias voltage remains relatively constant and that an appreciable amount of reverse current (greater than the saturation current) begins to flow. This value of reverse bias voltage is V_B.

The second method is to observe a V-I plot for the diode on an

oscilloscope. The value of V_B will be clearly visible. This method may be preferable since it shows how steep the breakdown is.

Table 1.2 is a summary of the capacitance and breakdown voltage measurements made.

Table 1.2 - A Summary of C_{min}, S_{max} and V_B Values

Diode Number	C_{min} (pf)	S_{max} (X 10^{10} darafs)	V_B
1	17.4	5.75	93.2 volts
2	19.6	5.10	greater than 105 volts
3	20.6	4.85	89.6 volts
4	22.2	4.51	83.7 volts
5	17.4	5.75	101.6 volts
6	17.5	5.72	93.2 volts
7	17.4	5.75	greater than 110 volts
8	16.9	5.92	greater than 110 volts

By this method, the values of S_{max} were determined for the samples of Motorola diodes. From these values, the specifications for an imbedding network can be determined.

This chapter has described general procedures by which the varactor diode parameters R_s, C(V) and V_B may be measured. With only a few modifications these procedures may be applied to varactors of various shapes and sizes. The use of the computer to numerically integrate the capacitance-voltage function made it quite easy to obtain elastance and voltage versus stored charge data.

CHAPTER II

THE INPUT AND OUTPUT FILTERS

Section 2.1 - Introduction

Referring back to the schematic diagram of the frequency multiplier shown in Figure 0.3, we observed that the imbedding network would contain the impedance matching structure for the diode as well as the bias network and any filters it may be necessary to include. It is these filters toward which we now direct our attention.

The need for filters comes from the fact that it may not be possible to completely eliminate all the other harmonics in the impedance matching network. An output filter is needed to insure that only the desired harmonic frequency is present in the output and an input filter is needed to block any unwanted inputs into the multiplier. Thus, these filters serve to improve the noise figure of the entire multiplier.

The output filter is of the interdigital type. It is a bandpass filter centered around the sixth harmonic (1494.6 Mhz). It was designed for a 17% fractional 3 db band width and passband ripple attenuation of less than .2 db. The attenuation at $5\omega_o$ and $7\omega_o$ was to be at least 60 db with no spurious passbands thru the twelfth harmonic.

The input filter consists of alternate lengths of high and low impedance transmission line. This is a field theory analogy to the low frequency low-pass filters consisting of series inductance and shunt capacitance elements. The 3 db passband edge was set at 300 Mhz and a .2 db ripple was to be allowed in the passband. There would be 60 db of attenuation at the second harmonic, 498.2Mhz. It was hoped that there would be no spurious passbands in the attenuation characteristic.

The remainder of this chapter will present the design of these two filters as well as the predicted and actual responses of these filters.

Section 2.2 - The Output Filter

The design of microwave filters is a fairly routine process since there are many books and articles that detail the design considerations and list the filter parameters and how to choose them. One such book, a very complete treatment, is Microwave Filters, Impedance - Matching Networks, and Coupling Structures by George L. Matthaei, Leo Young and E. M. T. Jones, published by Mc Graw - Hill - 1964.

The band-pass, output filter design was taken from this book. The interdigital configuration was chosen since it theoretically has no spurious passbands until three times the center frequency. Figure 2.1 shows the final design of the output filter. The top coverplate has been removed. The distance between the ground walls (the 1.974 inch dimension of Figure 2.1) is chosen to be a quarter-wavelength at the passband center frequency.

The "fingers" are numbered 0 through 8. Fingers 1 to 7 are resonators and the coupling between the resonators is accomplished via the fringing fields due to the foreshortening of the fingers. Fingers 0 and 8 are impedance matching elements and are intended to match the 50 ohms input line to the resonators.

The proper amount of coupling that is needed to give the desired center frequency is difficult to determine because it is impossible to account for all the fringing capacitance effects. Increasing the amount of foreshortening decreases the fringing capacitance and thus increases the passband center frequency. So it is best to leave the fingers longer than actually needed and shave off the excess in order to "zero in" on the desired center frequency.

For example, the filter was originally built with a spacing of .160 inch. The passband was then centered at 1375 Mhz. When the spacing was increased to .194 inch the passband center shifted up to 1425 Mhz. This attenuation characteristic is shown in Figure 2.2. Measurements of the attenuation were made at 25 Mhz intervals between 1000 and 2000 Mhz. These correspond to the heavy dots of Figure 2.2.

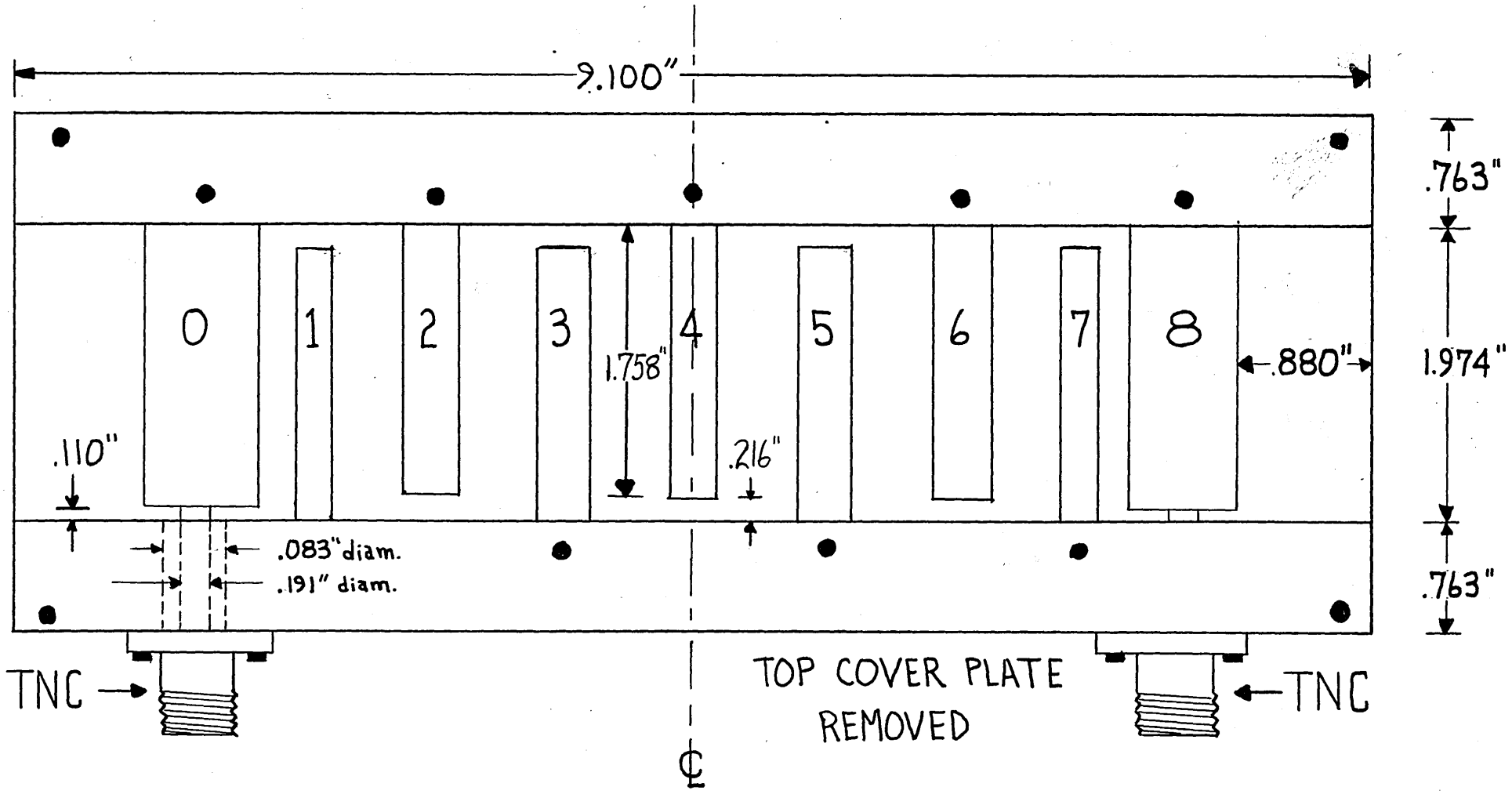

FIGURE-2.1

INTER-DIGITAL BAND-PASS FILTER - CENTER FREQ. 1494.6 MHz;
BANDWITH - 300 MHz; MID-BAND LOSS < 1.0 db.

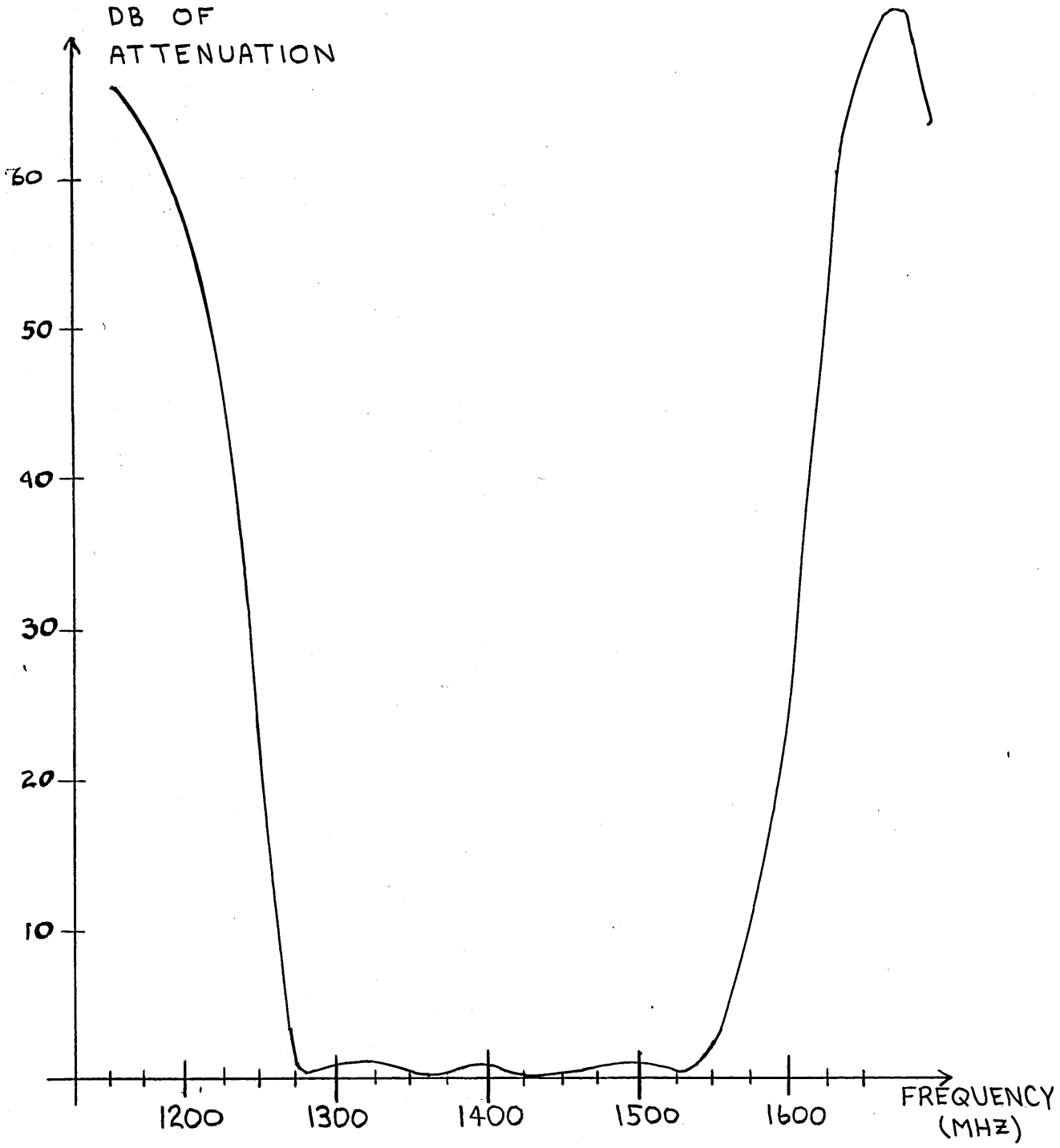

FIGURE 2.2

ATTENUATION CHARACTERISTIC OF THE OUTPUT FILTER. FINGER-TO-GROUND WALL SPACING = .194".

As can be seen from this characteristic, there is more than 60 db of attenuation at the seventh harmonic (as called for in the specifications) but that there is only 35 db of attenuation at the fifth harmonic. This could be increased by shifting the passband closer to the specified center frequency. It is estimated that the spacing would have to be .216 inches to obtain the proper center frequency.

If it should happen that the passband is too high, it can be lowered with the use of tuning screws. By placing $\frac{1}{4}$ inch tuning screws in th top coverplate and locating them over the tips of the first and last two resonators, the passband center frequency can effectively be lowered. Adjusting the screws closer to the tip of the resonator increases the fringing capacitance and thus lowers the center frequency.

In these ways then, by increasing the finger-to-ground wall spacings or by using tuning screws, the passband may be shifted up or down in frequency.

The passband attenuation has a maximum of about 1 db. This is considerably more than the design value. This discrepancy may be due to the fact that there are small spaces between parts of the coverplates and the ground walls. Also, the filter was made out of brass stock. If it were silver or copper plated, this midband loss could be decreased considerably.

Finally, by scanning the response up to 3000 Mhz (the 12th harmonic is at 2989.2 Mhz) it is seen that the out-of-band attenuation remains above 45 db. This fact satisfies the specification that there be no spurious passbands until three times the center frequency.

So, with only a little more work on centering the passband more accurately and by silver plating the structure, we have a fairly good approximation to the required output filter.

Section 2.3 - Computer-Aided-Design of the Input Filter

The design of the input filter was derived from a low-pass filter found in the previously mentioned book by Matthaei, Young and Jones. The parameters were chosen in accordance with the procedure outlined in that book and then the computer was used to analyze and optimize the design.

As was mentioned in the introduction, the input filter is made up of alternate lengths of high and low impedance transmission line; a UHF approximation to a low frequency, low-pass filter. The filter, as initially designed, would have been about three feet in length so it was bent in order to reduce its physical size. It didn't appear that the susceptances due to these bends would affect the filter's performance to any great extent.

The high impedance line was chosen as 114 ohms and the low impedance line as 13 ohms. The reason for these choices is that the brass rods and tubing required to realize these impedance values were readily available. The 114 ohm line has a 1.250 inch outer conductor diameter and a .1875 inch diameter inner conductor. The 13 ohm line has the same outer conductor but it uses a .8750 inch diameter inner conductor with a teflon dielectric filling the space between the outer and inner conductors. The relative dielectric constant of teflon is 2.7. Figure 2.3 is a semi-cutaway view of the final design for this filter.

The computer program that was used to analyze the input filter is known as LØADGØ FILTER ARITH. This program essentially transforms a specified load impedance through the various segments of transmission line, the lengths and characteristic impedance of which are also specified. The impedance seen at the other end of the filter is calculated for various values of frequency. In this case, we are mainly interested in having only a little attenuation at the input frequency and a great amount of attenuation at all harmonics up to the twelfth. What happens in between the harmonies is of little concern.

In order to illustrate the program, look at Figure 2.4. The section at the top of the figure is the input data. ZLR and ZLI specify the real and imaginary parts of the load impedance at each

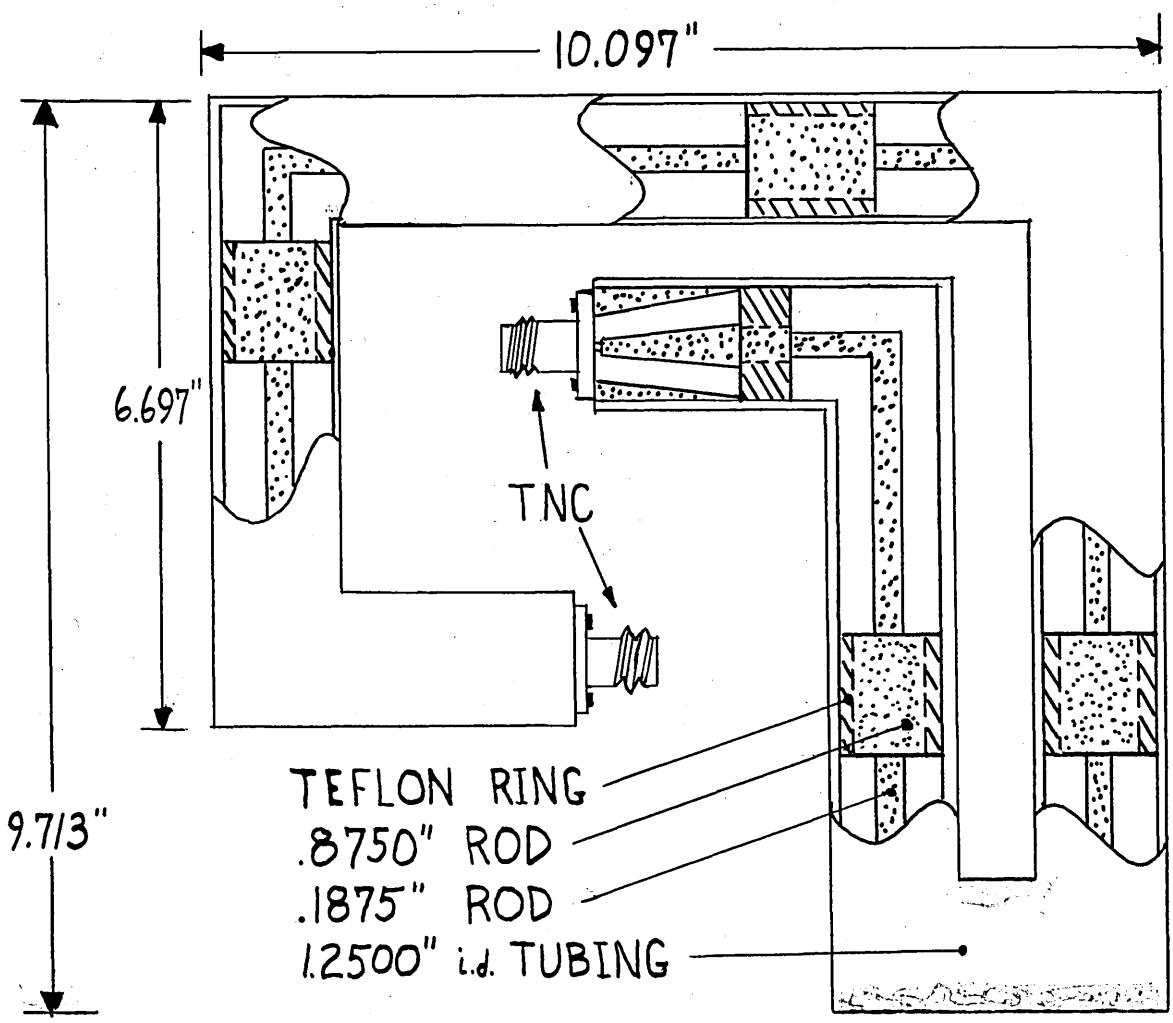

FIGURE - 2.3

LOW-PASS FILTER - CUT-AWAY VIEW OF LOW IMPEDANCE ELEMENTS. PASS BAND EDGE AT 360 MHz. PASS BAND ATTENUATION: LESS THAN .5 db.

```
ZLR(1)=50.,50.,50.,50.,50.,50.,50.,50.,50.,50.,50.,50.,
ZLR(1)=50.,50.,50.,50.,50.,50.,50.,50.,50.,50.,50.,50.,
ZLI(1)=0.,0.,0.,0.,0.,0.,0.,0.,0.,0.,0.,0.,
ZLI(1)=0.,0.,0.,0.,0.,0.,0.,0.,0.,0.,0.,0.,
LAM(1)=12.,6.,4.,3.,2.4,2.,1.7143,1.5,1.3333,1.2,1.0909,1.,
LAM(1)=12.,6.,4.,3.,2.4,2.,1.7143,1.5,1.3333,1.2,1.0909,1.,
N=12,
N=12,
L(1)=1.04,.308,1.54,.339,1.82,.339,1.54,.308,1.04,
L(1)=1.04,.308,1.54,.339,1.82,.339,1.54,.308,1.04,
Z(1)=114.,13.,114.,13.,114.,13.,114.,13.,114.,NN=9*
Z(1)=114.,13.,114.,13.,114.,13.,114.,13.,114.,NN=9*
```

INPUT DATA

K	L(K)	Z(K)
1	.104E 01	.114E 03
2	.308E 00	.130E 02
3	.154E 01	.114E 03
4	.339E 00	.130E 02
5	.182E 01	.114E 03
6	.339E 00	.130E 02
7	.154E 01	.114E 03
8	.308E 00	.130E 02
9	.104E 01	.114E 03

INPUT ARRAY

OUTPUT ARRAY

K	LAM(K)	ZØR(K)	ZØI(K)
1	.12000E 02	.42530E 02	.27452E 02
2	.60000E 01	.29969E-01	.10146E 03
3	.40000E 01	.14370E 00	.10572E 04
4	.30000E 01	.36196E 00	-.16494E 03
5	.24000E 01	.27742E-03	-.70641E 02
6	.20000E 01	.64919E-04	.55756E 01
7	.17143E 01	.37813E-03	.83703E 02
8	.15000E 01	.56881E-01	.20287E 03
9	.13333E 01	.19303E-03	-.67967E 03
10	.12000E 01	.24533E-03	-.12492E 03
11	.10909E 01	.22289E-03	-.28477E 02
12	.10000E 01	.12191E-02	.29893E 02

```
INPUT NUMBER ØF VALUES N ØF
LAM(1) AND NN ØF Z(1),LAM(1),Z(1),L(1)
INPUT ZLR(1),ZLI(1)
```

FIGURE 2.4

COMPUTER ANALYSIS OF INPUT FILTER DESIGN - L(5) = 1.82.

of the 12 frequencies we wish to analyze. Here we have assumed a 50 ohm load (no imaginary part), constant at each harmonic.

The frequencies at which the impedance transformations are to be made are specified by the normalized wavelength, LAM, at these frequencies. In this case, the wavelength at the twelfth harmonic (actually 3.95 inches) is taken as one, an all the other wavelengths are normalized to it. Thus, the wavelength at the input frequency (12 times greater than than the wavelength at the 12th harmonic) is taken to be 12. Even the lengths of the transmission line segments are normalized to this wavelength. Thus, the first section of transmission line, L(1), is given as 1.04 because its real length is 1.04 X 3.95 inches = 4.12 inches.

So, the lengths of the transmission line segments are specified in this way. The impedance of each segment is also specified, Z(1) = ... The first array in Figure 2.4, headed K, L(K), Z(K), merely summarizes the lengths and impedances of the nine transmission line segments comprising the filter.

The last array, headed K, LAM(K), ZØR(K), ZØI(K), specifies the wavelength at the analysis frequency and the computed values of the real and imaginary parts of the transformed impedance in ohms. Looking at ZØR(K), the real part, it can be seen that the value at the input frequency, 42.53 ohms, is greater than any of the other values at the other frequencies. In fact, we would expect the magnitude of the reflection coefficient, $|\Gamma|$, to be close to 1 for these other frequencies and thus provide a great amount of attenuation.

The optimization of this design is accomplished by changing the value of one or more of the parameters at a time and observing how this change affects the ZØR(K) values. Figure 2.4 has L(5), the length of the fifth segment, specified as 1.82. Figure 2.5 has L(5) = 1.85, (note that only a change in the input data needs to be specified). This is a little better design because it makes ZØR(4) smaller (from.36 ohms to .31 ohms).

Now, increase L(5) a little more. Figure 2.6 has L(5) = 1.87. This change has resulted in a further drop in ZØR(4) down to 2.9 ohms, but ZØR(1) is dropping also and it is necessary to keep this as close

```
L(5)=1.85*
L(5)=1.85*
```

K	L(K)	Z(K)
1	.104E 01	.114E 03
2	.308E 00	.130E 02
3	.154E 01	.114E 03
4	.339E 00	.130E 02
5	.185E 01	.114E 03
6	.339E 00	.130E 02
7	.154E 01	.114E 03
8	.308E 00	.130E 02
9	.104E 01	.114E 03

K	LAM(K)	ZØR(K)	ZØI(K)
1	.12000E 02	.42289E 02	.29018E 02
2	.60000E 01	.29399E-01	.10155E 03
3	.40000E 01	.16766E 00	.10623E 04
4	.30000E 01	.31360E 00	-.16367E 03
5	.24000E 01	.27151E-03	-.70625E 02
6	.20000E 01	.83993E-04	.55852E 01
7	.17143E 01	.22269E-03	.83771E 02
8	.15000E 01	.51082E-01	.20382E 03
9	.13333E 01	.26071E-03	-.67937E 03
10	.12000E 01	.63003E-04	-.12477E 03
11	.10909E 01	.20245E-03	-.28456E 02
12	.10000E 01	.15631E-02	.29962E 02

```
INPUT NUMBER ØF VALUES N ØF
LAM(1) AND NN ØF Z(1),LAM(1),Z(1),L(1)
INPUT ZLR(1), ZLI(1)
```

FIGURE 2.5

COMPUTER ANALYSIS OF INPUT FILTER DESIGN - L(5) = 1.85.

```
L(5)=1.87*
L(5)=1.87*
```

K	L(K)	Z(K)
1	.104E 01	.114E 03
2	.308E 00	.130E 02
3	.154E 01	.114E 03
4	.339E 00	.130E 02
5	.187E 01	.114E 03
6	.339E 00	.130E 02
7	.154E 01	.114E 03
8	.308E 00	.130E 02
9	.104E 01	.114E 03

K	LAM(K)	ZØR(K)	ZØI(K)
1	.12000E 02	.42139E 02	.30059E 02
2	.60000E 01	.29058E-01	.10161E 03
3	.40000E 01	.18759E 00	.10662E 04
4	.30000E 01	.28775E 00	-.16292E 03
5	.24000E 01	.27002E-03	-.70615E 02
6	.20000E 01	.10139E-03	.55933E 01
7	.17143E 01	.16878E-03	.83801E 02
8	.15000E 01	.48514E-01	.20441E 03
9	.13333E 01	.31378E-03	-.67911E 03
10	.12000E 01	.36389E-04	-.12473E 03
11	.10909E 01	.19584E-03	-.28443E 02
12	.10000E 01	.19619E-02	.30020E 02

```
INPUT NUMBER ØF VALUES N ØF
LAM(1) AND NN ØF Z(1),LAM(1),Z(1),L(1)
INPUT ZLR(1),ZLI(1)
```

FIGURE 2.6

COMPUTER ANALYSIS OF INPUT FILTER DESIGN - L(5) = 1.87.

to 50 ohms as possible. So, L(5) = 1.85 is chosen as the optimum design for the specified criteria.

This then, is an example of how a computer may be used to optimize the design of a microwave, low-pass filter.

Section 2.4 - The Performance of the Input Filter

Figure 2.5 lists the predicted impedance values of the input filter for values of frequency from the first to the twelfth harmonics. From these values, the predicted attenuation at each of the harmonics will be calculated and compared to the actual values measured on the filter.

The magnitude of the reflection coefficient, $|\Gamma|$, is given by equation 2.1,

$$|\Gamma| = \frac{|Z\emptyset R - 50 + jZ\emptyset I|}{|Z\emptyset R + 50 + jZ\emptyset I|} \quad . \tag{2.1}$$

If 1 watt of power is delivered to the filter, then $|\Gamma|^2$ watts will be reflected and $1 - |\Gamma|^2$ watts will be transmitted through the filter. Thus, the predicted attenuation is db, is given by:

$$A_{db} = -10 \log_{10} (1 - |\Gamma|^2) \quad . \tag{2.2}$$

For small values of ZØR, such as those encountered at the second through twelfth harmonics, A_{db} may be approximated. Let ZØR be much less than 50 ohms. Then, from eq.2.1,

$$|\Gamma| = \sqrt{\frac{(Z\emptyset R - 50)^2 + Z\emptyset I^2}{(Z\emptyset R + 50)^2 + Z\emptyset I^2}} \quad ,$$

or

$$|\Gamma| \cong \sqrt{\frac{Z\phi I^2 + 2500 - 100 Z\phi R}{Z\phi I^2 + 2500 + 100 Z\phi R}} \quad . \tag{2.3}$$

Now, by using the binomial series approximation:

$$\frac{1}{Z\phi I^2 + 2500 + 100 Z\phi R} \cong \frac{1}{Z\phi I^2 + 2500} - \frac{100 Z\phi R}{(Z\phi I^2 + 2500)^2} \quad , \tag{2.4}$$

or, eq.2.3 becomes:

$$|\Gamma| \cong 1 - \frac{100 Z\phi R}{Z\phi I^2 + 2500} \quad . \tag{2.5}$$

Finally, letting $\frac{100 Z\phi R}{Z\phi I^2 + 2500} = \delta$, we have:

$$|\Gamma| \cong 1 - \delta \quad , \tag{2.6}$$

implying that $|\Gamma|^2 \simeq 1 - 2\delta$ or that

$$A_{db} \simeq -10 \log_{10} 2\delta \quad . \tag{2.7}$$

$$(Z\phi R << 50).$$

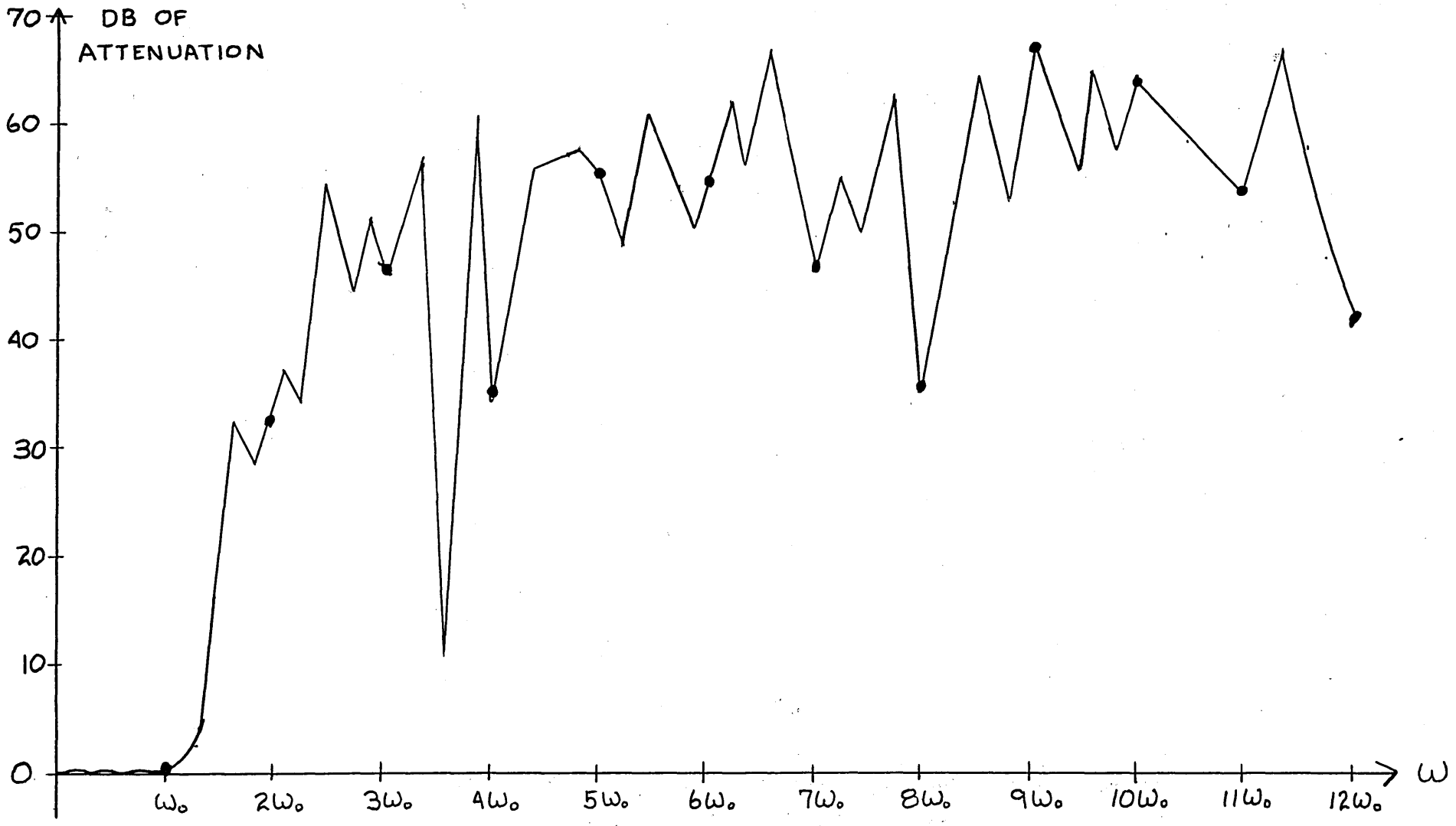

FIGURE 2.7 - ASYMPTOTIC BEHAVIOR OF INPUT FILTER ATTENUATION CHARACTERISTIC.

Figure 2.7 presents an attenuation plot of the actual input filter. The spurious pass bands do not occur at the harmonics and the attenuation at the harmonics is always greater than about 30 db. The pass band losses are less than .5 db and the 3 db band edge is about 360 Mhz.

Table 2.1 is a summary of the predicted and actual attenuation characteristics of this low-pass filter. The predicted values are remarkably accurate especially at the lower harmonics.

Table 2.1 - Comparison of Predicted and Actual Low-Pass Filter Characteristics.

Frequency	Predicted Attenuation (from eq. 2.7)-(in db)	Actual Attenuation (from Fig. 2.7)-(in db)
ω_o	.44	.50
$2\omega_o$	32.5	33.7
$3\omega_o$	45.3	45.0
$4\omega_o$	36.7	32.4
$5\omega_o$	52.0	51.5
$6\omega_o$	52.0	50.8
$7\omega_o$	49.0	50.5
$8\omega_o$	36.4	35.2
$9\omega_o$	68.9	66.3
$10\omega_o$	61.8	61.5
$11\omega_o$	49.2	46.1
$12\omega_o$	40.3	37.9

This chapter has described the input and output filters that are needed to realize the varactor frequency sextupler. The design considerations for each filter were given in detail. And one very important purpose of this chapter has been to demonstrate the use that a computer may be put to in the design and optimization of microwave filters.

CHAPTER III

DESIGN OF THE IMBEDDING NETWORK

Section 3.1 - Introduction

The design of a realizable imbedding structure for the diode that will expose the diode to the proper impedance levels (as given in eqs. 0.2) is the essence of multiplier design. To be realizable, the imbedding network must be of a physical size that would permit its construction. Two solutions to this problem are presented. The first is called the shorted stub approach and the second is the transformer approach.

The shorted stub structure (shown in Figure 3.1) is analogous to the lumped circuit realizations. In a lumped circuit multiplier, the idler network (imbedding network) consists of a resonant L-C circuit that shorts out the diode at each intermediate frequency between the input frequency and the desired output frequency. Thus none of the intermediate harmonics appear in the output waveform. The shorted stub structure does essentially the same thing.

The transformer approach essentially uses a network such as the one in Figure 3.2 and, by choosing the proper lengths and impedances, comes up with a single structure that matches the required impedance function at all frequencies. The analysis of this network is done on a computer and the results are given in Section 3.3.

Section 3.2 - The Shorted Stub Method

In the shorted stub approach a number of stubs, equal to the harmonic number of the multiplier, extend outwardly from the diode. One stub is the input, one the output, and each of the others is designed to "zero out" (match the impedance of the diode) at each intermediate frequency.

This is accomplished in the following manner. The impedance of a length 'l' of transmission line, shorted at one end, is given,

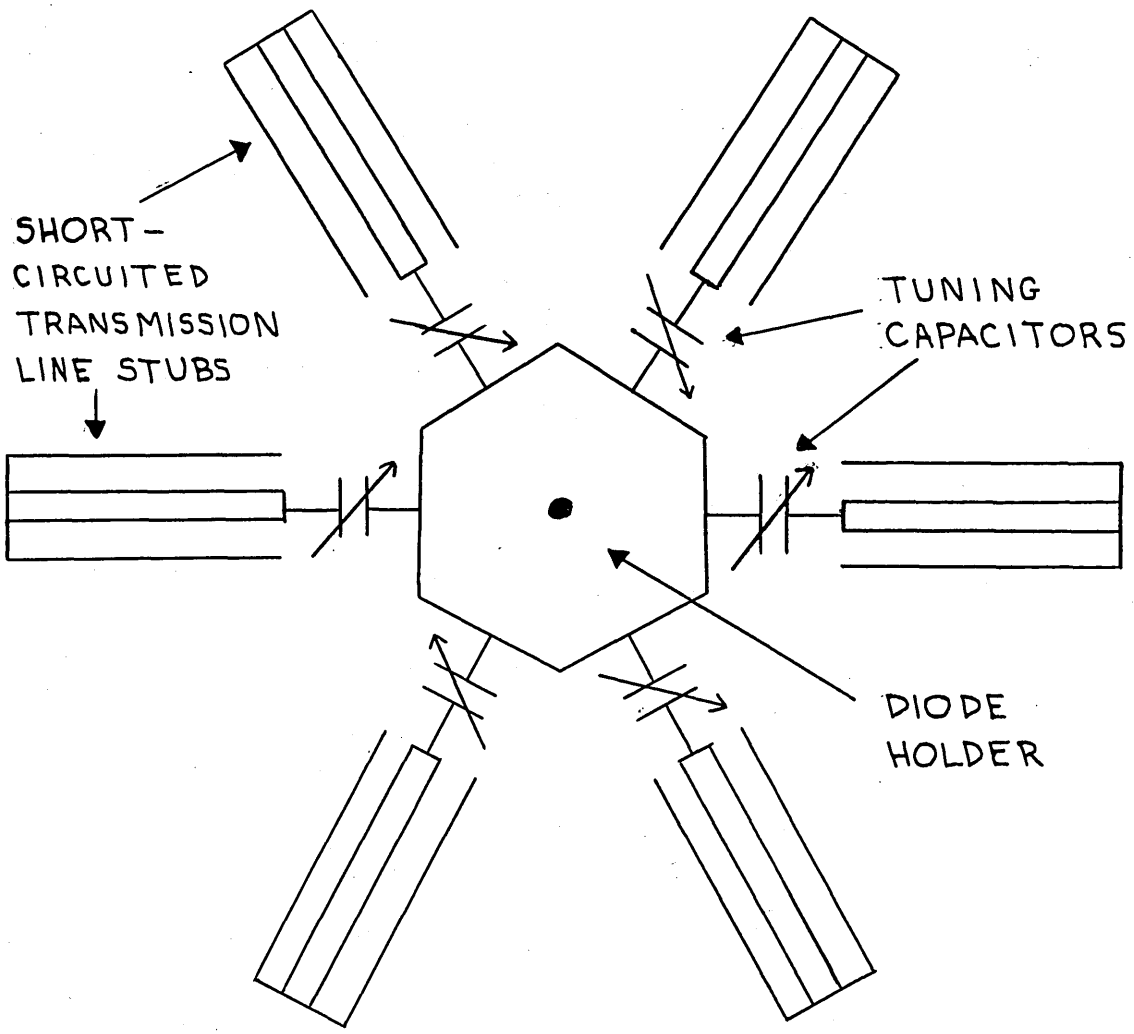

FIGURE 3.1

THE SHORTED-STUB APPROACH TO REALIZING THE REQUIRED IMBEDDING NETWORK. THERE IS A STUB FOR THE INPUT, OUTPUT AND EACH INTERMEDIATE FREQUENCY.

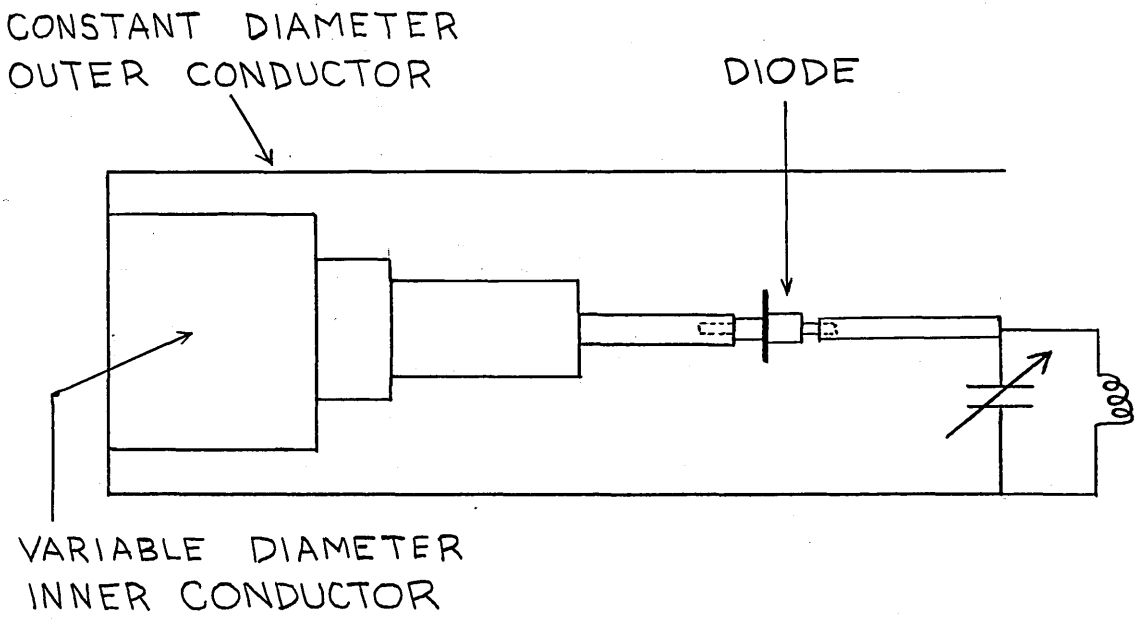

FIGURE 3.2

THE TRANSFORMER APPROACH TO REALIZING THE REQUIRED IMBEDDING NETWORK.

as a function of frequency, by:

$$Z_s(\omega) = j Z_o \tan(\omega \tfrac{\ell}{c}) \quad , \tag{3.1}$$

where 'c' is the velocity of light in the medium filling the line (assume air-filled) and Z_o is the characteristic impedance of line. For an air-filled line, Z_o is given in ohms by:

$$Z_o = 60 \ln(\tfrac{b}{a}) \quad , \tag{3.2}$$

where 'b' is the outer conductor's inner diameter and 'a' is the inner conductor's outer diameter.

Figure 3.3 shows a plot of $Z_s(\omega)$ versus $\omega \frac{\ell}{c}$. Now let us assume we are designing a stub to "zero out" at $2\omega_o$, and futhermore, we have arbitrarily picked 'l', the length of the stub, such that $\ell = \frac{\pi}{5\omega_o c}$. This implies that $\omega = 2\omega_o$ will occur at $\omega \frac{\ell}{c} = \frac{2\pi}{5}$, (as shown in Fig. 3.3).

If we now place a capicitor in series with the stub (the capacitor's impedance characteristic is the dotted line in Fig. 3.3), then, by proper choice of a capacitor we can obtain the specified impedance level. The new configuration is shown in Figure 3.4.

The total impedance of shorted stub and capacitor combination is:

$$Z_t(\omega) = Z_s(\omega) + Z_c(\omega) \quad , \tag{3.3}$$

where $Z_c(\omega) = -j \frac{1}{C\omega}$, the impedance of a capacitor of value C.

At $\omega = 2\omega_o$, this becomes:

$$Z_t(2\omega_o) = j\left(Z_o \tan \tfrac{2\omega_o}{c} \ell - \tfrac{1}{2\omega_o C}\right) . \tag{3.4}$$

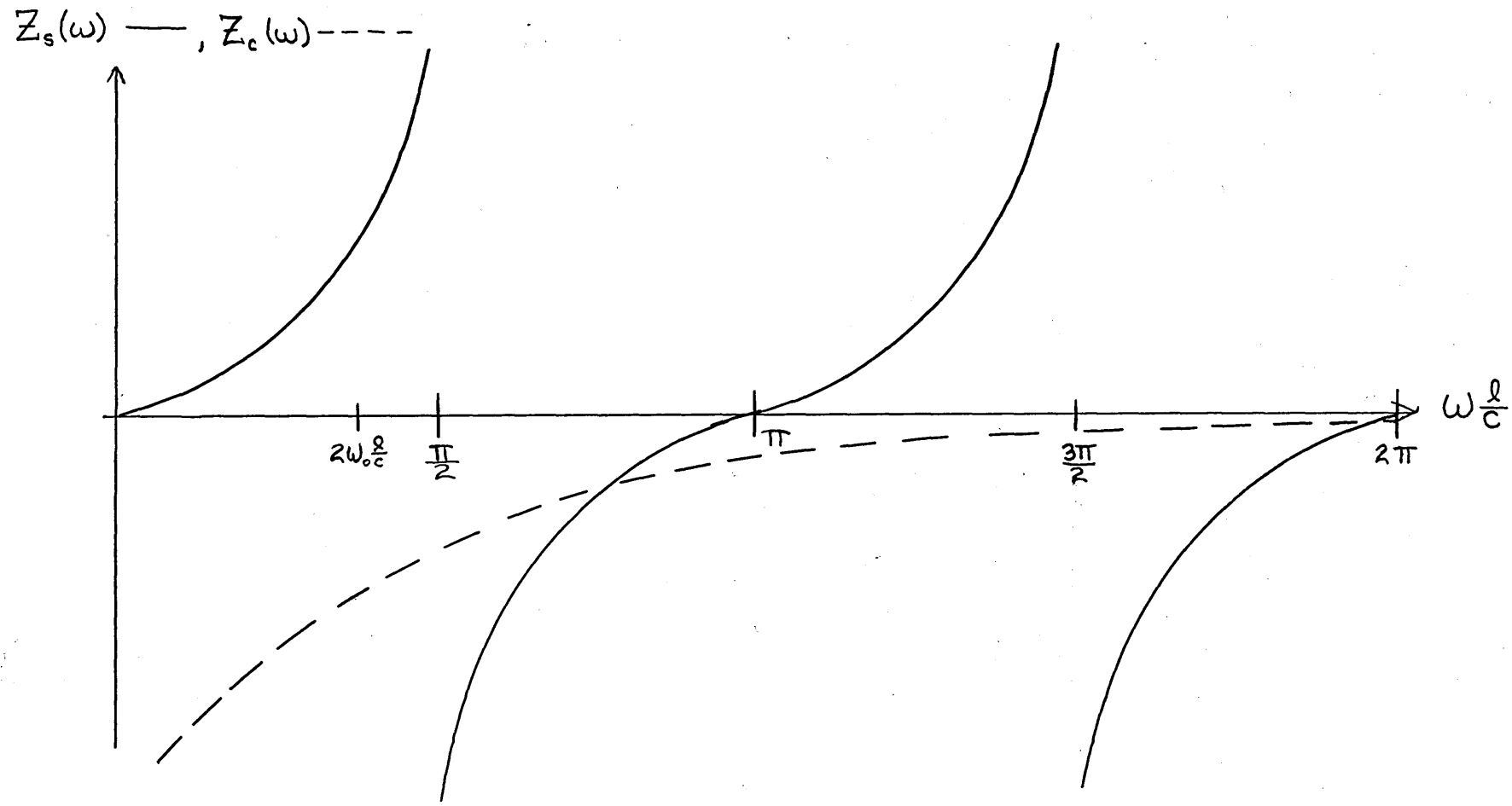

FIGURE 3.3

IMPEDANCE VERSUS FREQUENCY FOR SHORTED STUB, $Z_s(\omega)$, AND TUNING CAPACITOR, $Z_c(\omega)$. $Z_s + Z_c = Z_t$. AT $\omega = 2\omega_o$, $Z_t = j9.55$ ohms.

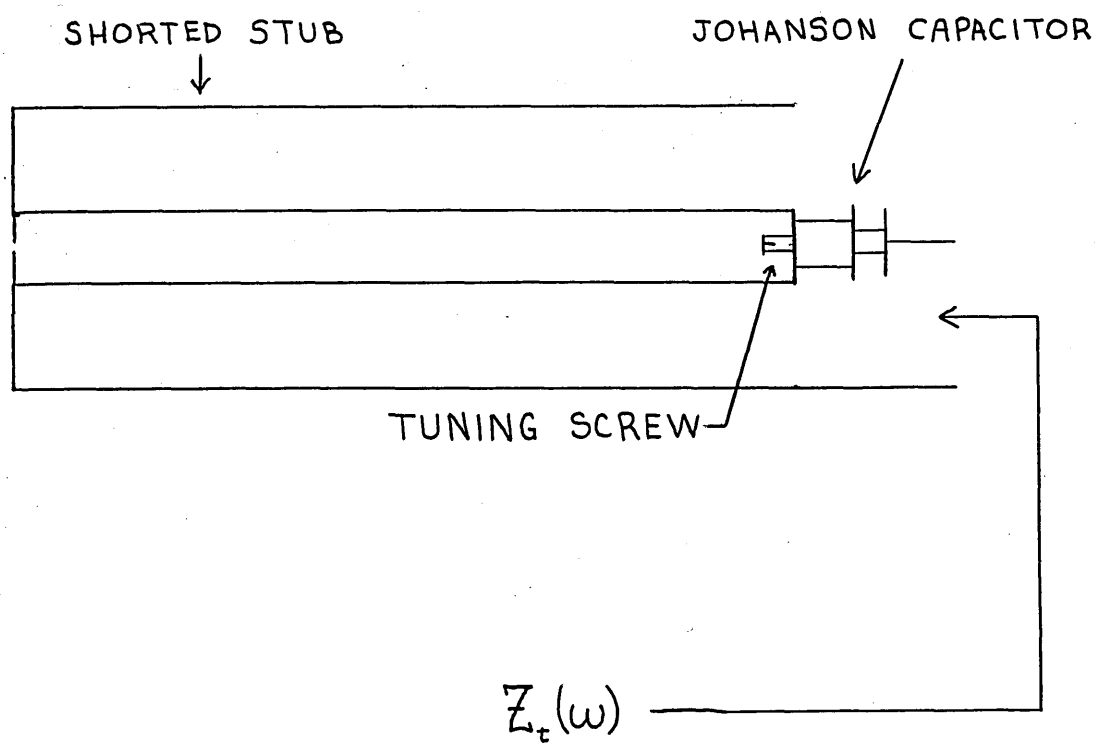

FIGURE 3.4

PHYSICAL REALIZATION OF THE SHORTED STUB - TUNING CAPACITOR CONFIGURATION.
$Z_t(\omega) = Z_s(\omega) + Z_c(\omega)$.

By substituting $\ell = \frac{\pi}{5\omega_o} C$, we have:

$$Z_t(2\omega_o) = j\left[Z_o \tan\left(\frac{2\pi}{5}\right) - \frac{1}{2\omega_o C} \right] . \qquad (3.5)$$

We set this impedance value equal to the value required in eqs. 0.3 for a specific diode and input frequency letting $\tan\left(\frac{2\pi}{5}\right) = 3.08$ we have, approximately:

$$Z_o(3.08) - \frac{1}{C}(2 \times 10^{-9}) = 9.55 \quad , \qquad (3.6)$$

for which we can pick values of Z_0 and C.

For example, if Z_0 = 68 ohms, then C would be about 10pf. And the stub length 'l' previously determined, would be about 30 inches. This length could be cut down considerably by making a better initial choice of the stub length.

But anyway, this example shows that it is certainly possible to realize the imbedding network by this method of shorted stubs.

The capacitors that are required are available from Johanson Manufacturning Corporation, Boonton, New Jersey. They have available, cylindrical, variable capacitors of diameter.140 inches to about .300 inches in various ranges from .35pf to 30pf. They are rated throughout the UHF range and can be readily employed in this design.

Tuning the capacitor to the desired impedance value may be done by using a hollow inner conductor for the stub and tuning through this opening.

So, by carrying out a similar procedure to the one above for the $2\omega_o$ stub, we can design each of the shorted stub resonators. Table 3.1 summarizes the imbedding network that was designed for the sextupler.

Table 3.1 - A Summary of the Shorted Stub Imbedding Network Design Parameters

Stub Number	"Zeros Out" at-	Length of Stub (in inches)	Z_o of Stub (in ohms)	Capacitance Needed (in pf)
1	ω_o	$\frac{\pi}{6\omega_o C} = 3.95$	83.2	23.9
2	$2\omega_o$	$\frac{\pi}{6\omega_o C} = 3.95$	83.2	2.4
3	$3\omega_o$	$\frac{\pi}{8\omega_o C} = 2.96$	48.5	2.0
4	$4\omega_o$	$\frac{\pi}{10\omega_o C} = 2.37$	48.5	1.1
5	$5\omega_o$	$\frac{\pi}{12\omega_o C} = 1.98$	17.1	2.0
6	$6\omega_o$	$\frac{\pi}{14\omega_o C} = 1.69$	17.1	1.5

The capacitors that are required are all JMC - 4700 (.35 to 3.5pf) types except for the one in series with stub #1. It is a JMC - 3908 (1 to 30pf) type. These capacitors will allow the imbedding network to be tuned for any value of C_{min} between 8pf and 25pf. And typical values of C_{min} for the diodes that were measured are between 16pf and 22pf. (See Table 1.2).

The only remaining problem with this design is to determine a way to bias the diode. If we imbed the top of the diode in a block of copper we can feed the bias in through a choke to the block. (See Figure 3.5). The block would also provide a good way to attach the stubs to the diode through the capacitor.

The above design then, shows a straight forward method to realize the imbedding network for the diode. It is a good way to approach the problem and will most likely be the easiest way to obtain a working sextupler.

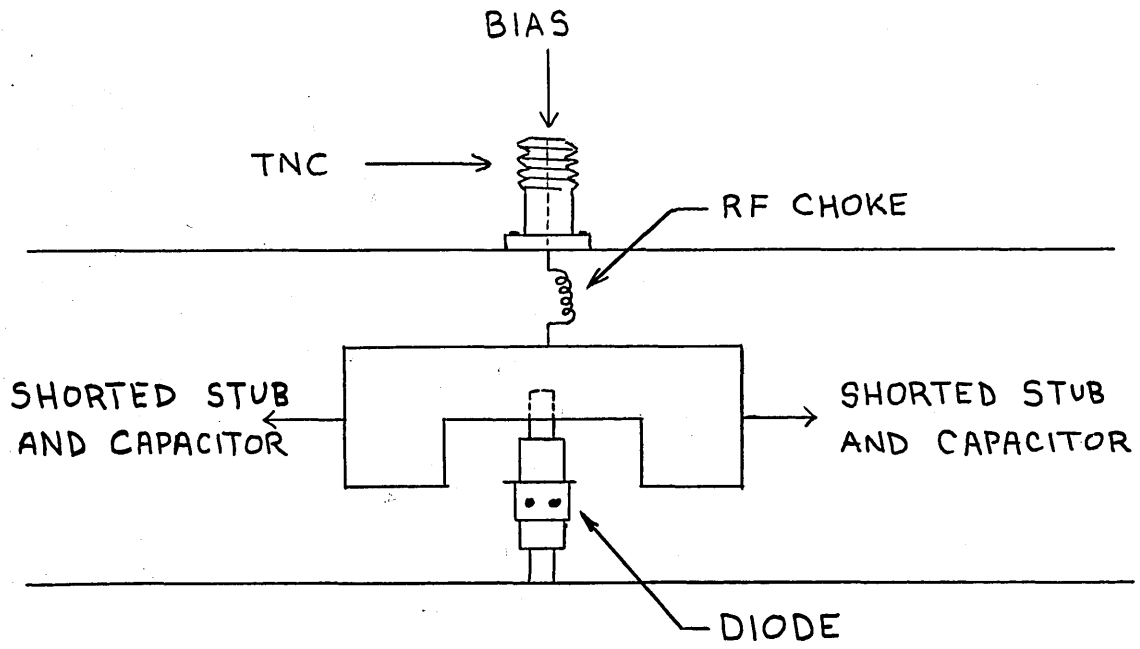

FIGURE 3.5

BIAS SCHEME FOR DIODE IN SHORTED STUB REALIZATION OF IMBEDDING NETWORK.

Section 3.3 - Computer-Aided-Design of the Transformer Imbedding Structure

As a further example of computer-aided-design, another imbedding network will be designed for the diode. This imbedding network will be in the configuration shown in Figure 3.2. The four sections of transmission line will be chosen such that the impedance of the line will be nearly zero at all harmonics from the first through the sixth. The impedance of the parallel L-C combination, when added to the impedance of the transformer structure, will match the diode impedance as specified in eqs. 0.2.

In a manner similar to the design of the low-pass input filter, a design for the transformer structure was chosen and optimized. Figure 3.6 is the computer analysis of the final structure. The short at the end was assumed to have a small resistance (.01 ohms) to keep the functions from increasing without bound. The impedances and lengths of line that were finally chosen are as follows: 11.86 inches of 40 ohm line, 5.56 inches of 45 ohm line, 4.61 inches of 50 ohm line and 1.63 inches of 55 ohm line. The optimization procedure consisted of varying each of the four lengths (keeping the impedance constant) until the best combination was found.

The difference between the impedance of the transformer structure and that required in eqs. 0.3 must be made up by the L-C combination. Table 0.2 gives a summary of these values.

Table 3.2 - A Summary of Impedance Values Pertaining to the Transformer Structure Design

Frequency (IN ω_o)	Impedance of Transformer Structure (in ohms)	Impedance Required by eqs. 0.3 (in ohms)	Needed Impedance in the L-C Combination (in ohms)
1	j3.35	j19.10	j15.75
2	j .66	j 9.55	j 8.89
3	-j1.31	j 6.37	j 7.68
4	j2.09	j 4.78	j 2.69
5	j2.99	j 3.82	j .93
6	-j2.88	j 3.18	j 6.06

```
ZLR(1)=.01,.01,.01,.01,.01,.01,.01,
ZLR(1)=.01,.01,.01,.01,.01,.01,.01,
ZLI(1)=0.,0.,0.,0.,0.,0.,0.,
ZLI(1)=0.,0.,0.,0.,0.,0.,0.,
LAM(1)=7.,3.5,2.3333,1.75,1.4,1.1667,1.,N=7
LAM(1)=7.,3.5,2.3333,1.75,1.4,1.1667,1.,N=7
Z(1)=40.,45.,50.,55.,
Z(1)=40.,45.,50.,55.,
L(1)=1.75,.822,.6802,.24,NN=4*
L(1)=1.75,.822,.6802,.24,NN=4*
```

K	L(K)	Z(K)
1	.175E 01	.400E 02
2	.822E 00	.450E 02
3	.680E 00	.500E 02
4	.240E 00	.550E 02

K	LAM(K)	ZØR(K)	ZØI(K)
1	.70000E 01	.14250E-01	.33475E 01
2	.35000E 01	.12751E-01	.66182E 00
3	.23333E 01	.14693E-01	-.13068E 01
4	.17500E 01	.11226E-01	.20857E 01
5	.14000E 01	.16991E-01	.29909E 01
6	.11667E 01	.14579E-01	-.28826E 01
7	.10000E 01	.16025E-01	-.50571E 01

```
INPUT NUMBER ØF VALUES N ØF
LAM(1) AND NN ØF Z(1),LAM(1),Z(1),L(1)
INPUT ZLR(1), ZLI(1)
```

FIGURE 3.6

COMPUTER ANALYSIS OF TRANSFORMER IMBEDDING NETWORK.

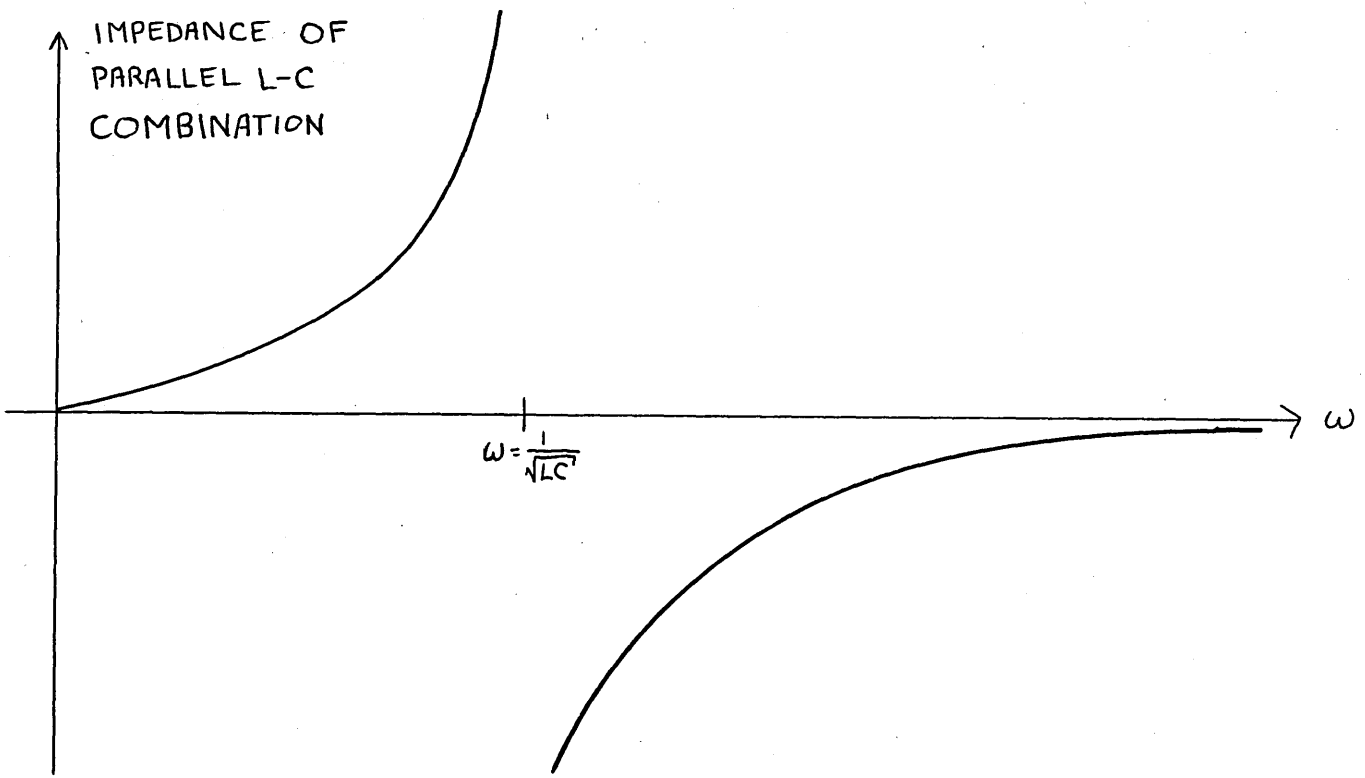

FIGURE 3.7

IMPEDANCE OF AN L-C PARALLEL COMBINATION VERSUS FREQUENCY.

Figure 3.7 shows the impedance of a parallel L-C combination. By choosing the proper values for L and C we may place the positive side of the impedance function at the correct points to realize the required impedance values as specified in Table 3.2. It would be wise to make the capacitance variable so the best match to the impedance function may be obtained. Here, the best match is defined as the point at which the output is maximized.

A good approximation to this parallel L-C combination would be an RF choke with a natural resonant frequency a little more than $6\times \omega_o$, (as shown in Fig. 3.7).

The bias for the diode may be fed in through the outer conductor at any convenient point and the input and output may be taken by H-field loops at the low impedance end of the structure.

Actual values for L and C and details of construction have not been included in this paper because it is felt that this transformer network would be more difficult to realize than the shorted stub approach of the preceding section. The design procedures and consideration would have to be much more carefully worked out in order to make this an efficient multiplier.

The value of this approach lies in the fact that it proves that it is possible to realize the proper impedances with a single structure and that the computer may be used in the design and analysis of such a structure.

CHAPTER IV

A SUMMARY OF IMPORTANT RESULTS AND CONCLUSIONS

Section 4.1 - Summary

Many ideas have been presented in this paper so it would be worthwhile to collate these ideas and summarize the results that have been determined.

The major aim of this investigation was to demonstrate that higher order frequency multipliers in the UHF and microwave ranges could indeed be realizably synthesized. The example of a sextupler was chosen and two possible realizations of this multiplier were presented in Chapter III.

It should be emphasized that these results are not restricted merely to the sextupler but may however, be extended to other higher order multipliers with little or no difficulty. The shorted stub approach may become a little unwieldy when applied to say, a X100 network. The design of such a structure, while not impossible, may warrant an attempt at having a stub "zero-out" on more than one harmonic. With the proper choice of stub length and tuning capacitor value, this is certainly possible.

Perhaps it would be better to approach the X100 problem with a single, transformer structure. It would be considerably more compact than the shorted stub approach but may require many more sections than the sextupler example used. Nevertheless, computer analysis of this network is indeed possible and this alone may preclude that intelligently designed high order frequency multipliers be of this type.

This leads to the other main conclusion that has been reached: that computer-aided-design is a valuable technique when applied to the design and optimization of microwave circuitry. CAD has proven its worth in many other areas of engineering and should be quite useful in microwave design especially since it is almost impossible in most cases to "breadboard" networks as can be done at the lower frequencies.

The computer was used extensively in this research in the

design of the transformer structure imbedding network and in the optimization of the imput filter design. Both of these examples have been thoroughly discussed already. It would be wise to mention, however, that the computer is not the ultimate answer to microwave design. The designer must be aware of the inherent limitations in constructing a specific microwave circuit.

For example, it would be very difficult to manufacture air-filled coax with a characteristic impedance greater than about 120 ohms without using a very large outer conductor or a very small inner conductor. Also, it is unwise to specify dimensions with a tolerance tighter than about .0005 inch since this is the limit of most machine shop equipment. It is limitations like these that must be imposed when using the computer for the analysis of microwave design problems.

Section 4.2 - Suggestions for Additional Investigations

The work undertaken for this thesis, while yielding a number of useful results, is by no means complete. Many doors to interesting and constructive reseach problems have been opened and it is the author's hope that at least some of these may be investigated.

The most exciting problem to be looked into yet is to verify that the multipliers that have been designed will actually work. Verification of this result essentially involves constructing one or both of the imbedding networks and getting it to multiply. Measurements could be made to determine how closely this network conforms to the impedance that the theory requires the diode see (eqs. 0.2). Determination of dynamic range, bandwidth and maximum output power would also prove valuable and instructive.

Another investigation could be made to try to find some sort of parallel circuitry that would permit the simultaneous use of more than one diode. This would increase the maximum power handling capability of the multiplier.

The input filter was optimized on the computer and was assumed to be a continous series of unbent transmission line sections. Therefore, the discontinuity susceptances due to variations in the

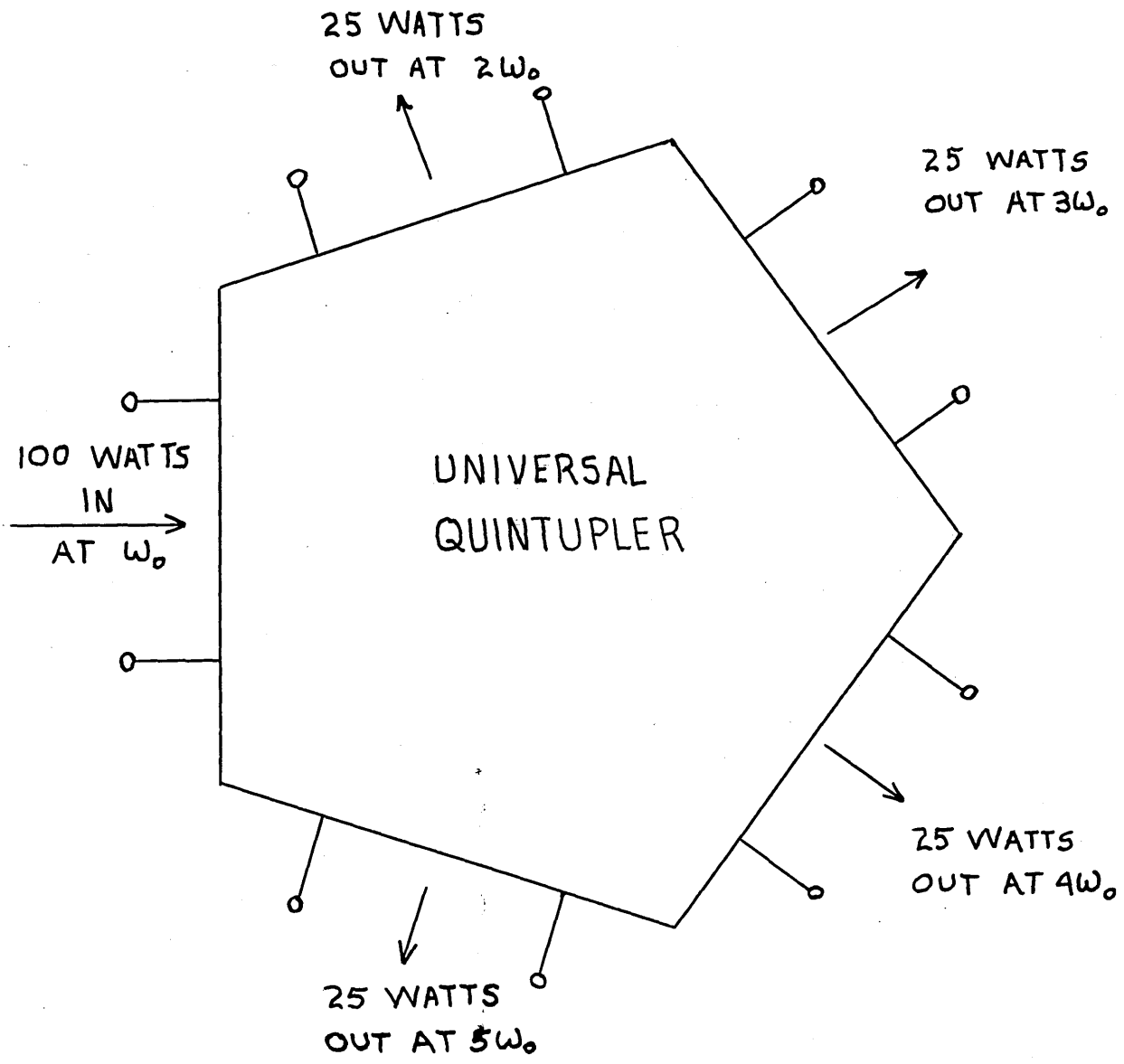

FIGURE 4.1

SCHEMATIC DIAGRAM OF A UNIVERSAL FREQUENCY QUINTUPLER UTILIZING SHORTED-STUB APPROACH.

inner conductor diameter and to the bending of the structure have not been taken into account (they were assumed negligible). Perhaps it could be determined if the discrepancies between the actual performance of the filter and the predicted performance is due to these discontinuities.

Also, it would be helpful to find some method to minimize the effect of these discontinuities.

Along with this filter, measurements can be made of the impedance versus frequency to see how closely they conform to the computer predicted values. (All that was of interest in the thesis was the reflection characteristics that yielded the attenuation versus frequency plot of Figure 2.7).

Chapter I described some of the measurements that were made to determine the diode parameters. These were made at 1 Mhz for the elastance characteristic and at 500 Mhz for the R_S characteristic. These measurements should be made at S-band or at least 1 Ghz to find out how much variation there is with frequency.

Also, much speculation has been made recently that R_S is not constant but does vary with the magnitude of the reverse bias voltage. This controversy should be resolved. The test jig used for the R_S measurement at 500 Mhz can easily be modified to allow for a variable bias to be placed on the diode.

Finally, a good theoretical problem is suggested by this reseach. Assuming that a multiplier is constructed using the shorted stub scheme, would it be possible to couple into each stub (which is resonant at each intermediate frequency) and obtain an output at that frequency? And, if this is possible, what conditions must be met to allow each stub to have the same power output? Figure 4.1 is a schematic representation of such a "universal" multiplier. If 100 watts were put in at ω_o then, in the example shown (a quintupler), 25 watts would be the output power at each of the other frequencies, $2\omega_o$, $3\omega_o$, $4\omega_o$, and $5\omega_o$. A "universal" multiplier would be valuable aid in communication systems as well as for laboratory test set-ups.

Thus, numerous possibilities certainly exist for extending the results established in this thesis.

BIBLIOGRAPHY

1) G. L. Matthaei, L. Young, and E. M. T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures, Mc Graw - Hill Book Co., Inc., New York (1964).

2) P. Penfield and R. P. Rafuse, Varactor Applications, The M. I. T. Press, Cambridge, Massachusetts (1962).

3) D. H. Steinbrecher, "Efficiency Limits for Tuned Harmonic Multipliers with Punch-Through Varactors", Department of Electrical Engineering and Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, Massachusetts (1967).