Energy Management Techniques for Ultra-Small Bio-Medical Implants

by

William R. Sanchez

M.Eng., Massachusetts Institute of Technology (2007)
B.S., Massachusetts Institute of Technology (2005)

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Author .....
Department of Electrical Engineering and Computer Science
May 23, 2012

Certified by .....
Joel L. Dawson
Associate Professor, Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Professor Leslie A. Kolodziejski
Chairman, Department Committee on Graduate Theses

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Abstract

Trends in the medical industry have created a growing demand for implantable medical devices. In particular, the need to provide medical professionals a means to continuously monitor bio-markers over long time scales with increased precision is paramount to efficient healthcare. To make medical implants more attractive, there is a need to reduce their size and power consumption. Small medical implants would allow for less invasive procedures and greater comfort for patients. The two primary limitations to the size of small medical implants are the batteries that provide energy to circuit and sensor components, and the antennas that enable wireless communication to terminals outside of the body.

In this work we present energy management and low-power techniques to help solve the engineering challenges posed by using ultracapacitors for energy storage. A major problem with using any capacitor as an energy source is the fact that its voltage drops rapidly with decreasing charge. This leaves the circuit to cope with a large supply variation and can lead to energy being left on the capacitor when its voltage gets too low to supply a sufficient supply voltage for operation. Rather than use a single ultracapacitor, we demonstrate higher energy utilization by splitting a single capacitor into an array of capacitors that are progressively reconfigured as energy is drawn out. An energy management IC fabricated in 180-nm CMOS implements a stacking procedure that allows for more than 98% of the initial energy stored in the ultracapacitors to be removed before the output voltage drops unsuitably low for circuit operation.

The second part of this work develops techniques for wide-input-range energy management. The first chip implementing stacking suffered an efficiency penalty by using a switched-capacitor voltage regulator with only a single conversion ratio. In a second implementation, we introduce a better solution that preserves efficiency performance by using a multiple conversion ratio switched-capacitor voltage regulator. At any given input voltage from an ultracapcitor array, the switched-capacitor voltage regulator is configured to maximize efficiency. Fabricated in a 180-nm CMOS process, the chip achieves a peak efficiency of 90% and the efficiency does not fall below 70% for input voltages between 1.25 and 3 V.

Thesis Supervisor: Joel L. Dawson
Title: Associate Professor, Electrical Engineering and Computer Science

Acknowledgments

"Do not be anxious about anything, but in every situation, by prayer and petition, with thanksgiving, present your requests to God. And the peace of God, which transcends all understanding, will guard your hearts and your minds in Christ Jesus.

- Phillipians 4:6

First and foremost, I thank God for His amazing grace.

Second, I thank my advisor, Professor Dawson. I am extremely grateful for Professor Dawson for giving me this opportunity, and for being a teacher, mentor, advisor, coach and friend. You believed in me based on pure potential and for than I am grateful. Thank you for giving me so much freedom to explore many areas beyond circuit design: from TA-ing over 20 times, to starting a salsa dance company and traveling around the world, to letting me explore the other side of campus, i.e., Sloan, which has shaped the next step in my career. I will miss your regular ability to pun - a true gift and talent.

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"The Lord hath given me a learned tongue, that I should know how to uphold by word him that is weary..."

- Isaiah 50:4

Thank you to the great MIT entrepreneurial ecosystem: the VMS, the 2010 and 2011 MIT Clean Energy Prize organizers, Leon and the Deshpande Center, and Bill Aulet. Bill thank you for pushing me, being a super-connector, backing me in the face of adversity and unfounded controversy, and for building the world-class, student-centered entrepreneurial community that exists at MIT today. You have made dreams possible and attainable for me and many of my peers by teaching us and establishing an amazing laboratory to test ideas.

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"Two are better than one, because they have a good return for their work; If one falls down, his friend can help him up. But pity the man who falls and has no one to help him up!"

- Ecclesiastes 4:9-10

Thank you to my friends. Thank you to the Boston and New York salsa dancing communities for giving me an outlet channel and great memories. You have kept me sane. Burcu from way back to our 18.02 days and random, existential conversations. Sonia, Bressica (Bressiper), Joselia, Licole - you are all really special to me. Very special thank you to Lino, Gleb, and Jose: Lino for hiring me as a UROP and teaching me salsa moves. Your sense of humor is uplifting and your ability to make me laugh is always refreshing; Gleb for your

patience during our late nights of 6.004 and salsa days all the way to our brainstorming about new ventures. You are a great role model and I am honored to know you. Your versatility, intellect, and ability to be so successful, efficient, and productive without sacrificing life's joys and adventures are inspirational. Jose for being such an exemplary role model as a researcher, entrepreneur, husband, brother, son, and father. I have learned many things from you and I thank you for blessing me with those lessons, least of which is not "When you know, you know." Thank you, B-family for sharing the precious lives of your children with my wife and me. Isa, Nina, and Lucas bring incredibly powerful joy to us.

"Honor your father and your mother, so that you may live long in the land the LORD your God is giving you."

- Exodus 20:12

Of course, thank you to my loving parents and siblings, Juan and Pierina. I am eternally grateful to my mother and father for their selflessness, iron-fist, dedication, and love. It is not easy to raise a family in inner-city New York. Thank you for never giving up on us, and for never putting down your guards. Your quintessential humility, discipline, and wisdom are a testament to God's grace and your service to Him. Thank you for the sacrifices you have made for us in raising us, for being tireless in providing and facilitating our upbringing, and being infinitely supportive of our dreams and ambitions. All along you have aligned what is good for us with what is best for us, and done so with incredible steadfastness.

Thank you Juan and Pierina for being so incredibly supportive always and being incredibly rich sources of inspiration. Your talents, achievements, and successes have made me proud. Juan - as kids, you were my partner-in-crime. You were my best friend. You still are. You were always faithful to me even when I tricked you into taking the blame for me. I always had your back. I still do and always will. I know I can trust in the same. Pierina - when I was 5 years old, I prayed for you. That year, we were blessed. You are so incredibly talented in so many ways, it is mind-boggling. Thank you for your strength, drive, and powerful sense of service. You are true to yourself and you constantly remind of the importance of self-loyalty and identity.

"...Love is patient, love is kind. It does not envy, it does not boast, it is not proud. It is not rude, it is not self-seeking, it is not easily angered, it keeps no record of wrongs. Love does not delight in evil but rejoices with the truth. It always protects, always trusts, always hopes, always perseveres..."

- 1 Corinthians

Lastly and certainly not least, I thank my beautiful wife, Shirley. Shirley - you are my world. The Heavens rejoiced the day we met because nearly 27 years of parallel living finally intersected. Thank you for saying "Yes!" when I asked you to marry me as you folded laundry. We will never forget how much I tried to get John Legend to help me express how much I love you, but alas. You teach me so much and I am so blessed to be able to share life with you. Thank you for continually, and very creatively, pushing me out of my comfort zones. You are the most beautiful person I know and I am grateful for how our lives have melded and influenced each other in most awesome and wondrous ways. I look forward to sharing a life with you full of purpose and love, bringing blessings to those whose lives we can touch, helping you sweat the small stuff so that others do not have to, and building a family to propagate a Godly heritage.

Most sincerely,

- Willie

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Chapter 1

Introduction and Background

Healthcare is important and, at the time of writing, reforms across many levels were necessary. Inefficiencies in the current U.S. system bring healthcare costs to $2-6T, which is upwards of 14% of GDP. This thesis seeks to explore three specific areas:

1. Microelectronics used in the medical space

2. Ways to facilitate using energy storage devices besides batteries for ultra-small implants

3. Impact the quality of life of patients with chronic conditions

This chapter motivates the use of a minimally invasive medical platform leveraging advances in energy storage technologies and microelectronics. Section 1.2 and Section 1.3 provide an overview of the burden of non-compliance on the U.S. health-care system and a survey of representative medical device solutions that partially mitigate the issue. Section 1.4 establishes the limitations to shrinking form factors of implants and how alternative energy storage solutions such as ultracapacitors can enable smaller form factors. Finally, Section 1.5 provides a description of a specific target application where a minimally invasive bio-implant solution might have a big impact on the effectiveness of diagnostics for patients with Parkinson's disease.

1.1 Healthcare and Non-compliance

Presently, continuous monitoring of patients is difficult and typically intrudes greatly on a patient's lifestyle and daily routines. Methods that rely on patients measuring themselves are unreliable and inconsistent. For example [7], consider a patient with a respiratory infection that does not complete the full course of antibiotics prescribed by a physician. When symptoms persist, the patient returns to her doctor but fails to report the non-compliance. The physician consequently believes that the original medication was somehow inadequate (e.g., the pathogen was resistant to the medication or not covered within the therapeutic range) and prescribes a different agent. In this scenario, non-compliance has resulted in (1) at least one unnecessary clinical visit, (2) two medications in a situation in which one might have sufficed, and (3) a deviation, based on misinformation, from the initial treatment plan which, by design, should have provided the optimal combination of safety, affordability, and effectiveness for that patient. Such cases occur every day throughout the health-care system.

As a second example, the evaluation and treatment of patients with a variety of movement disorders including Parkinson's disease, restless legs syndrome, and essential tremor demand medical electronics that can continuously record information between recharge cycles. Tremors are the number one diagnostic for Parkinson's disease which is a neurological disorder, but there are many different types of tremors including essential tremors and physiologic tremors. Patients with Parkinson's often get misdiagnosed as having an essential tremor which is actually more prevalent, but occurs at a different frequency and is not a neurological degenerative disease. The Parkinson tremor is used to monitor disease progression. In these cases, we can imagine a patient forgetting to record events, or altogether missing certain events, leading to poor diagnosis and treatment.

Non-compliance is as dangerous and costly as many illnesses, whether not complying with medical instructions such as following a dosage schedule, recording medically-relevant activity as requested, or attending scheduled medical visits. Non-compliance causes 300,000 deaths annually in the U.S., and leads to 10-25 percent of hospital and nursing home admissions, costing approximately $39.3 billion [8–10].

In these examples, one sees an opportunity for decades of advances in microelectronics to positively impact healthcare. Non-compliance is a larger issue and Parkinson's disease is a specific condition, both of which can be partially mitigated with engineering and technology solutions. To maximize patient compliance, a shift towards a long-term, implantable, minimally invasive platform is crucial. Fortunately, sophisticated devices have become ubiquitous and advances in micro-electro-mechanical systems (MEMS) and CMOS technology have opened possibilities for addressing non-compliance via electronic medical implants. While mobile devices are widespread, there remains an unmet need for minimally invasive implants to address non-compliance in a ways not possible today. Implants and wearable devices exist today but are typically constrained in size and form factor. We discuss trends and examples next in Section 1.2 and Section 1.3.

1.2 Trends in Medical Electronics

The challenges for all medical implants are essentially the same. They must be small, they must somehow communicate with the outside world, and they must be low-power. To prevent tissue damage due to heating and prolong battery lifetime, energy efficiency is important. Moreover, in order to be sustainable as long-term monitoring solutions, it is required that medical implants be wirelessly rechargeable, preferably without the need for additional surgery.

A wireless link enables easy collection of information from implanted sensors. Wireless communication is indispensable in a plethora of biomedical applications, including notifying a healthcare provider of abnormal cardiac events, assessing the effectiveness of drugs in diabetes patients, the communications between electrodes in deep brain stimulators, and monitoring the long-term fatigue of bio-mechanical joints following arthroplastic surgeries.

Finally, the miniaturization of medical implants has been observed in recent years. Riding the Moore's Law wave, aggressive scaling and deep sub-micron CMOS technology has placed less pressure on the need for circuitry to shrink. Correspondingly, sensors and actuators have benefited from advances in MEMS nanotechnology, which have likewise followed the scaling

trend seen in CMOS technology. By contrast, progress in battery technology is relatively slow.

1.3 Survey of Medical Electronics

With the commoditization of consumer electronics has come a surge in the number of electronic devices available at low price points and portable form factors. Many solutions addressing remote monitoring and patient non-compliance have been reported. A notable commercial option is the MedSmart system [11]. The automatic pill dispenser provides a robust means of reducing drug administration non-compliance. Other products are designed for alerting a monitoring station during medical emergencies. With the proliferation of heart rate, blood pressure, glucose, and temperature monitors, users are overwhelmed with data reporting devices that may be used to record long-term trends for medical diagnosis. A drawback of most commercial products, however, is that they are dependent on the initiative, responsibility, and compliance of the user. However, an increasing percentage of non-compliance problems stem from patients who deliberately discontinue administering prescribed medications or recording data because they deem it no longer necessary. This often leads to unauthorized deactivation.

There is ongoing research and development in many areas that target the deficiencies of commercial products. Several short-term monitoring integrated circuits are reported in [12–14]. These include intrahospital monitoring, glucose monitoring, and an actigraph platform for tremor monitoring for Parkinson's patients. Still, these suffer in size reduction due to the discrete/multi-component implementation and wearable form factors. [15–17] report telemetry-enabled implantable solutions. While these could serve as long-term monitoring devices, the miniaturization and lifetimes are limited in part by the battery and antenna. To circumvent the battery limitation an inductively coupled power transmission scheme may be used [4, 14, 18, 19]. Employing inductive coupling techniques, however, has several disadvantages. Inductive coupling requires power transmission from a fixed RF source. A rectifier front-end could be used to extract DC energy to power the electronics over a short-

term. In addition, poor inductive coupling efficiencies may compound with recalcitrant users required to position themselves near a base-station on a regular schedule with great precision.

A reasonable alternative to replace batteries without the need for inductive coupling is an energy harvester. Energy harvesting is a natural choice for resolving the need for a stand-alone energy source. The advent of advanced MEMS technology brings closer the possibility of a completely integrated solution. Piezo-electric and vibration-based harvesters have been reported [20–24]. The drawback of these harvesters rests on their dependence on continuous resonant vibration sources or the restrictive size geometries for implantable applications. Thermo-electric harvesters possess similar disadvantages, and the regulated temperature environment within the body hinders their feasibility in a medical implant.

1.4 Micro-scale Energy Storage and Power Management

Two considerations limit efforts to shrink the size of bio-implants. The first is reducing the size of the power and data link, or antenna, for in-body communications. Designing an antenna to be small compared to its operating wavelength is challenging. A higher carrier frequency is desirable and it has been demonstrated that an optimal frequency exists in the 2-3 GHz range for in-body communications [25]. However, the wavelength in this range (e.g., 2.4 GHz) is still very large for a minimally invasive device. Consider for instance an injectable device with a 15 gauge needle (1.8 mm ID) and 5 mm long (as shown in Fig. 1-3). These dimensions afford a tight squeeze into a needle and allow a perimeter of 12 mm. The perimeter is still $\sim 10\times$ smaller than the wavelength at 2.4 GHz. This would yield awful radiation efficiency. The Medical Body Area Network (MBAN) standard is under FCC review to provide allocation for exploiting this optimal point. However, the maximum transmit power is 1 mW EIRP. This a serious burden on antenna efficiency, especially as a power link.

The second area-consuming component is the energy source. For many bio-implant applications, on-chip energy storage requirements limit the smallest form factor permissible. At the time of writing, chemistry-based batteries could not be integrated. Providing an energy storage alternative to batteries is appealing because batteries:(1) scale poorly for bio-implant applications, (2) can be toxic, or present a host of other bio-incompatibility issues, and (3) offer long charging times, affecting patient lifestyle.

The increasing efficiency of energy harvesting technologies offer a solution that is amenable to micro-scale integration. However, power density levels remain a challenge [26] when sub-mW levels are required in micro-scale form factors. Advances in ultracapacitor technologies offer an attractive compromise between energy density and form factor. Ultracapacitors have several compelling advantages. Chief among them is the promise they hold of being integrated on chip [27]. In addition to the potential for an extremely small form factor,

ultracapacitors also feature: high *power* density, a practically unlimited number of recharge cycles, extremely rapid recharging, and a direct relationship between the terminal voltage and its state of charge. Section 1.4.1 presents a survey of electric double layer capacitor technologies as a passive energy storage alternative to battery chemistries.

1.4.1 Electric Double Layer Capacitor Technology - Ultracapacitors

Accidentally discovered by researchers at Standard Oil of Ohio in 1966 [1], ultracapacitors, or electric double-layer capacitors, can carry 5-10 percent the energy densities of conventional battery chemistries of comparable weight [2]. With over 10^5 recharge cycles possible, ultracapacitors are attractive, viable candidates for implantable applications employing efficient wireless recharging schemes. Moreover, recent advances in nanotechnology and the advent of carbon nanotubes have promised increased energy densities for ultracapacitors [1, 28].

Ultracapacitors have traditionally found their niche in the automotive and aviation industries, where their inherent, superior power densities come to the rescue in demanding environments, extending the lifetimes of the batteries they support. Work at MIT, RPI, and other research centers are getting closer to comparable energy densities of traditional battery chemistries. In the recent years, ARPA-E funds have focused a great deal in advancing this area of research and catalyzing commercialization. Already in use for military applications, commercial electric vehicles, and power generation plants, ultracapacitors are great candidates for spacecraft, medical, and other applications. For example, for space applications, tests on commercially-available ultracapacitors show no significant degradation effects to their charge/discharge profiles and electrical parameters due to gamma and proton radiation 60 MeV levels, making them excellent candidates for LEO and, possibly, interplanetary missions.

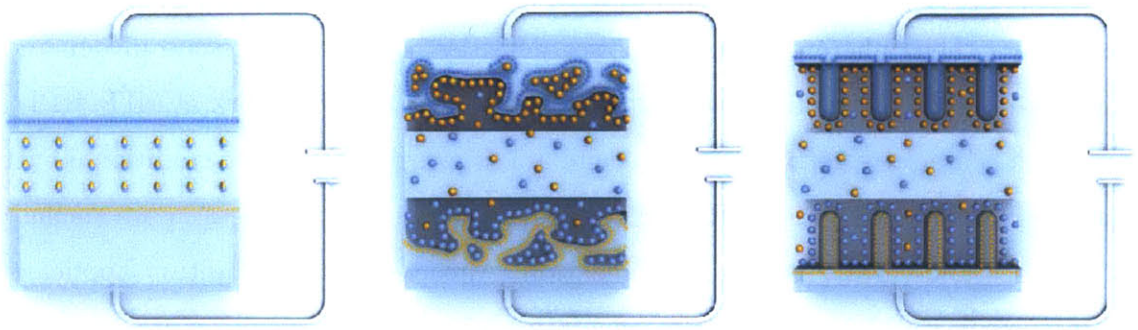
Traditional, parallel-plate capacitors store energy by creating a charge differential between two metal plates separated by a dielectric medium of permittivity ϵ. The resulting potential, V, is related to the dielectric material used, the amount of charge stored, Q, on

the plates, the separation distance, d, and surface area, A, of the plates as follows

$$V = \frac{Q}{C} = \frac{Q \cdot d}{\epsilon A} \tag{1.1}$$

where $C = \frac{\epsilon A}{d}$ is the capacitance in Farads.

Commercially available ultracapacitors obtain their increased capacitance and hence storage density through the use of activated carbon. In contrast with traditional capacitors, ultracapacitors do not make use of a conventional dielectric. Instead of separating two plates, ultracapacitors use two nanopourous substrates (e.g., activated carbon, polypyrrole, etc.) separated by very short distances. Fig. 1-1 highlights the differences between various capacitor structures. In essence, it is the sponge-like nature of activated materials increase their effective area per unit volume, augmenting their charge storage capacity by as much as 2,000% over a traditional material like aluminum.



(a) Traditional parallel-plate capacitor with capacitance determined by length and width of plates.

(b) Commercially available activated carbon ultracapacitors achieve their high energy densities by their porosity and sponge-like structure - achieving increases in surface area by as much as 2,000%.

(c) Carbon nanotube ultracapacitors gain additional surface area from the tube patterns formed.

Figure 1-1: Charge storage capacitor elements [1].

There are many advantages to replacing batteries with ultracapacitors. The number and speed of charge-discharge cycles afforded by ultracapacitors outperform rechargeable battery

chemistries by several orders of magnitude. The charge-discharge lifetime of ultracapacitors allow them to outlive the devices they provide energy for, making them environmentally friendly. Typical battery chemistries wear out in just a few years, leaving behind toxic waste that pose a serious disposal and safety hazard. Moreover, memory effects, loss of electrolyte, non-ideal charge cycles, leakage, and geometries pose challenges when using batteries.

In addition to safety and recharge lifetimes, ultracapacitors exhibit extremely low internal resistance (equivalent series resistance, ESR) as compared with rechargeable batteries. Consequently, ultracapacitors outperform batteries by two orders of magnitude in delivering quick power, when necessary. Fig. 1-2 shows the Ragone chart comparing various energy-power solutions and Table 1.1 compares the volumetric densities of various battery chemistries. High efficiency ($> 90\%$) , high output power, extremely low heating levels, and low leakage currents (0.1 - 4 μA) also make ultracapacitors immensely attractive substitutes for batteries [29–31]. These are all desirable attributes for an implantable medical device aiming for long-term operation with minimal heat dissipation.

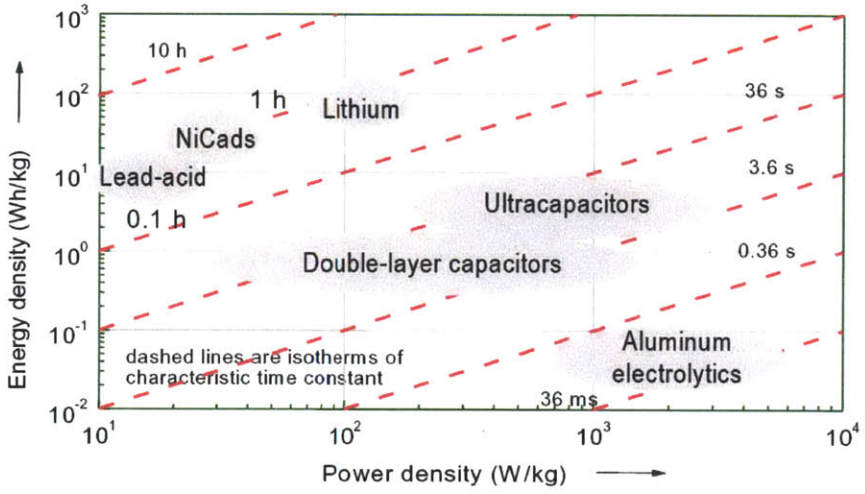


Figure 1-2: Gravimetric power density versus energy density for various energy storage devices [2]. Advances in carbon nanotube and manufacturing technology are enabling storage elements with capacities suitable for ultra-low power applications, such as bio-implant sensors.

Alongside modular and distributed design approaches, miniaturization continues the pur-

	Zinc-air	Alkaline-Manganese Dioxide	Nickel Metal Hydride	Poly-Carbon Monofluo-ride	Lithium Thionyl Chloride	$LiMgO_2$	Ultracapacitors
Voltage (V)	1.28	1.5	7.2	3	3.6	3	2-3
Energy Density ($W \cdot h/cm^3$)	1.3	0.039	0.175	0.427	0.69	0.83	.0027
Power Density (W/cm^3)	0.0003	0.0001	0.00005	0.00011	0.00019	0.00023	> 10
Shelf Life (years)	3	4	500 cycles	NA	NA	NA	$> 10^5$ cycles
Rechargeable	N	N	Y	N	N	N	Y

Table 1.1: Comparison of various battery chemistries showing typical operating voltages, shelf life, and rechargeability. Ultracapacitors are superior in power density and recharge cycles making them attractive energy storage alternatives for minimally invasive use models. Note that in addition to the large number of recharge cycles, a major advantage of ultracapacitors lies in the charging speeds which are inherently faster.

suit of modern technology. Increasing gravimetric/power-mass (W/kg) and power-volume (W/m^3) densities are figures of merit (FOM) that reflect the desire to miniaturize. Ultracapacitors lend themselves well to improving these FOMs. Reducing the size of energy storage components can be accomplished by 1) increasing the energy density per energy storage component, or 2) reducing the energy stored per cycle in the converter, as briefly discussed next.

Increasing Energy Density Considering a solenoidal inductor, it can be shown that the fundamental scaling between linear dimensions and flux- or current-carrying area causes inductor Q to decrease as α^2, where $\alpha < 1$ is a constant scaling each linear dimension. Similar relationships once limited capacitors due to material limitations of dielectrics, plate separation, and unacceptably low Q values. In today's CMOS technology the ratio of energy stored in a capacitor to the energy stored in an inductor for a given area easily exceed 3-5×. This ratio can exceed several order of magnitude for PCB-level, discrete applications [32].

Reducing Energy Stored Per Cycle Frequency-dependent losses in passive elements are limited almost exclusively to inductors and their magnetic materials. Most magnetic materials, used to increase inductance per unit volume, operate well at low frequency but have losses that rise rapidly otherwise. The basic trend is captured by the Steinmetz equation:

$$\overline{P_v(t)} = kf^{\alpha}B^{\beta} \tag{1.2}$$

where $\overline{P_v(t)}$ is the time-average loss per unit volume [kW/m^2], is the peak AC flux amplitude [Gauss], f is the frequency of sinusoidal excitation [Hz], and the constants k , α , and β are found by curve fitting. Typical values for α range from 1 - 3, indicating that losses rise steeply with frequency. Even worse, at higher frequencies cored inductors may actually increase in size since flux derating is necessary to avoid excessive heat buildup. The Steinmetz equation is a conservative measure for a limited number of situations. At high frequencies and under non-sinusoidal excitation typical of power converters, the losses become greater than predicted in the Steinmetz model.

1.5 Bio-Implant Platform for Monitoring Bio-markers for Parkinson's Disease and Essential Tremor

1.5.1 Background

The goal of this work is to contribute to the development of long-term, remote monitoring solutions that address patient non-compliance and provide access to preventive medical practices. This is accomplished by reducing the size of medical implants without sacrificing long-term, continuous monitoring. We achieve this by capitalizing on the increased energy storage capabilities of ultracapacitors and leveraging ultra-low power integrated circuit and small antenna techniques. Fig. 1-3 visually summarizes these goals.

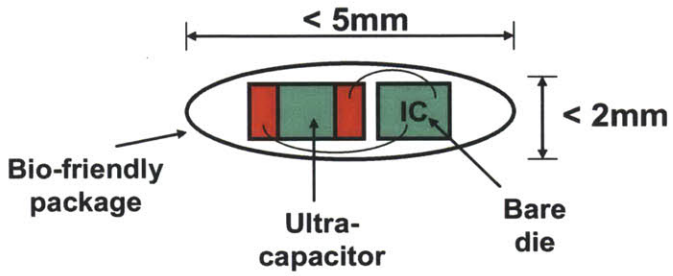


Figure 1-3: Target for minimally invasive medical implant. Minimizing the size of implants is limited by energy storage solutions and antennas. Maximizing the use of available energy is important because lifetime needs to be as long as possible. The model shown uses ultracapacitors instead of batteries as an energy storage alternative for ultra-small implants.

1.5.2 System Architecture and Description

The primary considerations for the design of an energy management integrated circuit are application-driven. In this thesis we consider identifying and applying techniques for powering sensor and data processing load electronics to diagnose and monitor the progression of Parkinson's disease (PD) and/or essential tremor (ET). Fig. 1-4 illustrates a block diagram representation of a bio-implant architecture. An accelerometer serves as the sensor to

transduce vibration signals into the electrical domain. The signal processing sub-blocks are responsible for amplifying and digitizing the signal, which is stored in a memory sub-block sized for storing 24-hours of data. The bio-implant adopts a use-model whereby it operates for a full day from a fully charged bank of ultracapacitors after which a patient wirelessly downloads the data to a central console for further processing and re-charging. This use-model highlights three key engineering challenges that constrain the implementation. First, the recorded data must be efficiently collected and compressed to minimize the size of the memory sub-block. Second, the power management and load electronics must minimize power dissipation in order to achieve the required operation duration desired, which in turn necessitates a highly efficient energy management sub-block as well as data processing, collection, and transmission circuitry with a very low *energy/bit* figure-of-merit. Lastly, minimally invasive packaging is desirable to minimize barriers to adoption. If implanted into the body with an RF link for data and power, then the requisite antenna must be as small and efficient as possible. Therefore, special design techniques must be employed towards this goal. For the system shown in Fig. 1-4, the major power consumers are 1) the accelerometer, 2) the analog-to-digital converter (ADC), and 3) specialized data acquisition circuitry leveraging compressive sensing techniques. The power management sub-block should be designed for $>250\ \mu$W.

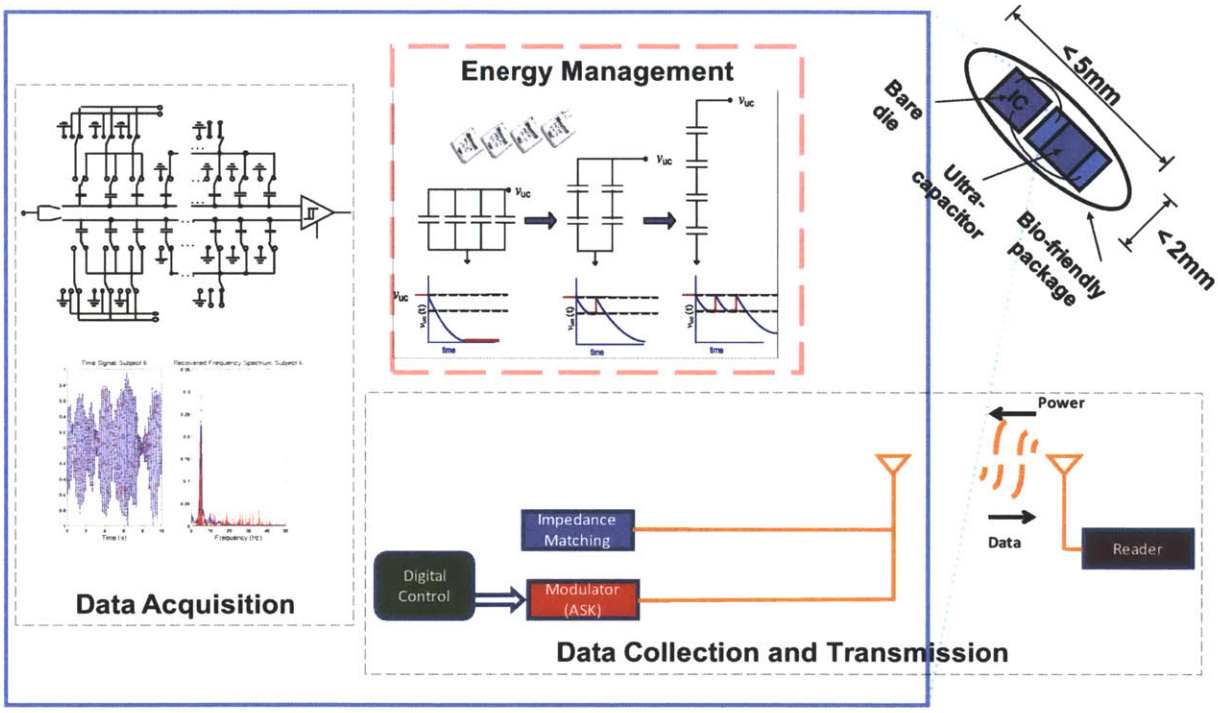


Figure 1-4: System diagram for bio-implant device for monitoring PD & ET.

1.6 Thesis Contributions and Organization

Minimizing the form factors of bio-implants while maximizing lifetimes is essential for minimally invasive solutions. Fast recharging, number of recharge cycles, and energy densities factor into energy storage solutions that are viable for such applications. The ability to provide power from the outside world for in-body communications requires good efficiency and smaller energy storage solutions.

DC-DC converters are an increasingly relevant block for energy constrained bio-implant and many applications. Chapter 2 provides an overview and tool-set useful for designing switched-capacitor DC-DC converters driven by application constraints and as viable alternatives to inductor-based DC-DC converters for on-chip applications. A brief treatment is provided on modeling switched-capacitor circuits along with analysis on the efficiency limiting mechanisms of on-chip switched capacitor DC-DC converters. The analysis is used for the implementation of a CMOS switched regulator described in Chapter 4. Special emphasis is placed on the design implications of accommodating wide-ranging input voltages and the implications on energy utilization since using ultracapacitors for energy storage inherently presents this situation.

Along with the antenna, a major limitation to reducing the size of bio-implants lies in energy storage. At the time of writing, chemistry-based batteries could not be integrated. A major problem with using any capacitor as an energy source is the fact that its voltage drops rapidly with decreasing charge. This leaves the circuit to cope with a large supply variation and can lead to energy being left on the capacitor when its voltage gets too low to supply a sufficient supply voltage for operation. Rather than use a single ultracapacitor, we will demonstrate higher energy utilization by splitting a single capacitor into an array of capacitors that are progressively reconfigured as energy is drawn out. In Chapter 3, we will present techniques to design an energy management integrated circuit combining RF energy harvesting and ultracapacitors to provide a long-term monitoring solution that maximizes energy utilization, thus prolonging bio-implant operational lifetime. Attention is placed on developing integrated circuit techniques to construct this alternative energy

storage solution. The shift to using ultracapacitors as energy storage elements circumvents the need for a battery and facilitates scaling down of bio-implants.

For an energy storage alternative using ultracapacitors to be practical and low complexity, we wish to store as much energy as possible. This corresponds to a higher initial voltage ($C \cdot V^2$). In addition, we wish to draw as much energy as possible from the ultracapacitors, which means drawing charge from the ultracapacitors in turn causing the voltage to drop. Therefore, we can expect to impose a wide-ranging input voltage to a power converter stage. In Chapter 4, we will explore the trade-offs encountered between switched-capacitor-based and inductor-based DC-DC converters when area is scarce, and we shall determine the best approach given wide-ranging input voltages that maintain good efficiency performance. We will introduce a switched-capacitor solution that preserves good efficiency performance by using a multiple conversion ratio switched-capacitor voltage regulator.

Chapter 5 provides a summary and conclusions for the work done as part of this thesis, and suggests open problems for future research related to this work.

Chapter 2

DC-DC Converters for Bio-Implants

While once seen as supporting circuitry, DC-DC converters are an increasingly relevant block for energy constrained bio-implant, [33] energy harvesting [34], and wireless sensor node [35] applications. There are many reasons to move beyond using a battery in these applications, despite the superior energy density of batteries. One great attribute of batteries, however, is their ability to hold a fairly constant output voltage over a wide range of states of charge. As these various fields have progressed into using energy storage elements that lack this key attribute, high-efficiency DC-DC converters become more important. Medical devices performing diagnostics and monitoring functions have lifetime requirements making energy storage a key specification; many such electronic systems today are designed to consume extremely low amounts of power ($<100\mu$W). In such contexts it becomes viable to use switched-capacitor DC-DC converters as the power delivery vehicles to integrated circuits. With the help of on-chip capacitors, switched-capacitor DC-DC converters provide higher efficiencies than possible with linear regulators and have the potential to accommodate a wide range of input voltage levels.

This chapter provides an overview and tool-set useful for designing switched-capacitor DC-DC converters driven by application constraints. Section 2.1 and Section 2.2 provide an overview of linear regulators and inductor-based switched-mode power converters, respectively. Section 2.3 is a brief treatment on modeling switched-capacitor circuits along

with detailed analysis on the efficiency limiting mechanisms of on-chip switched-capacitor DC-DC converters. Section 2.3.4 provides an analysis on the current handling capabilities of switched-capacitor DC-DC converters. Special emphasis will be placed on the design implications of accommodating a wide range of input voltages and the implications on energy utilization.

2.1 Linear Regulators

Both linear and switching regulators claim their segment in the marketplace with their specifications on power supply noise rejection, supply voltage required, efficiency, and accuracy. Low-dropout (LDO) linear regulators operate by modulating the conductance of a series pass switch connected between an input DC supply and a regulated output. Fig. 2-1 illustrates the traditional linear regulator; a bias voltage, v_{ref}, is cascaded with a non-inverting op-amp in shunt-feedback configuration. The main advantages of linear regulators are that they can be completely integrated on-chip, offer fast transient and good ripple performance, and can occupy little area [36]. However, the switch conductance modulation scheme for controlling output voltage constrains the flow of current directly from the battery to the load. This limits the maximum efficiency achievable to the ratio of the output and input voltages ($v_{\text{L}}/v_{\text{sup}}$) making accommodating wide-input ranges impractical unless we are willing to sacrifice efficiency.

2.2 Inductor-based DC-DC Converters

Inductor-based (off-chip) DC-DC converters have traditionally boasted the best efficiency performance. The switching converter alternately energizes inductors and/or capacitors from the supply and de-energizes them into a load, thereby transferring energy exclusively using ideally lossless devices. Accordingly, inductor-based topologies can theoretically achieve 100% efficiency independent of load voltage delivered. Fig. 2-2 shows the basic topology for an inductor-based boost converter stage as a representative example. The input/output

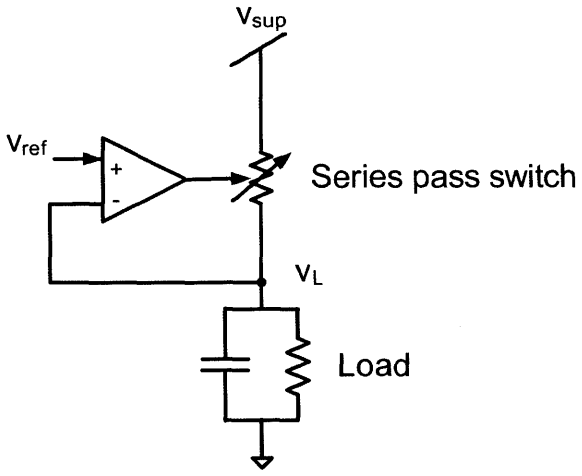


Figure 2-1: Basic linear regulator. The output, v_{L}, is regulated by the negative feedback of the op-amp. These regulators are easily integrated on-chip and offer fast transient performance.

voltage relationship is given by:

$$\frac{v(t)}{v_{\mathrm{sup}}} = \frac{1}{1-D}\frac{1}{\left(1+\frac{R_{\mathrm{L}}}{(1-D)^2R}\right)} \tag{2.1}$$

where D is the duty cycle and v_{sup} is the input supply voltage. In steady-state with ideal components, 100% efficient power transfer occurs with the average output regulated to the value given in Eq. 2.1. For transient load changes, the output settling speed is determined by the bandwidth of the feedback control loop (not shown in Fig. 2-2). A key observation is that if the switches are perfectly lossless, the efficiency of the voltage converter is independent of D and v_{sup} and therefore independent of the conversion ratio. If we just consider inductor losses, the instantaneous efficiency of an inductor-based boost converter is approximated by [37] as

$$\eta_{\mathrm{boost}} = \frac{1}{\left(1+\frac{R_{\mathrm{L}}}{(1-D)^2R}\right)} \tag{2.2}$$

where R_{L} is the inductor parasitic resistance and R models the load. For $R_L/R \ll 1$, high efficiency is preserved. A drawback of inductor-based approaches for integrated applications

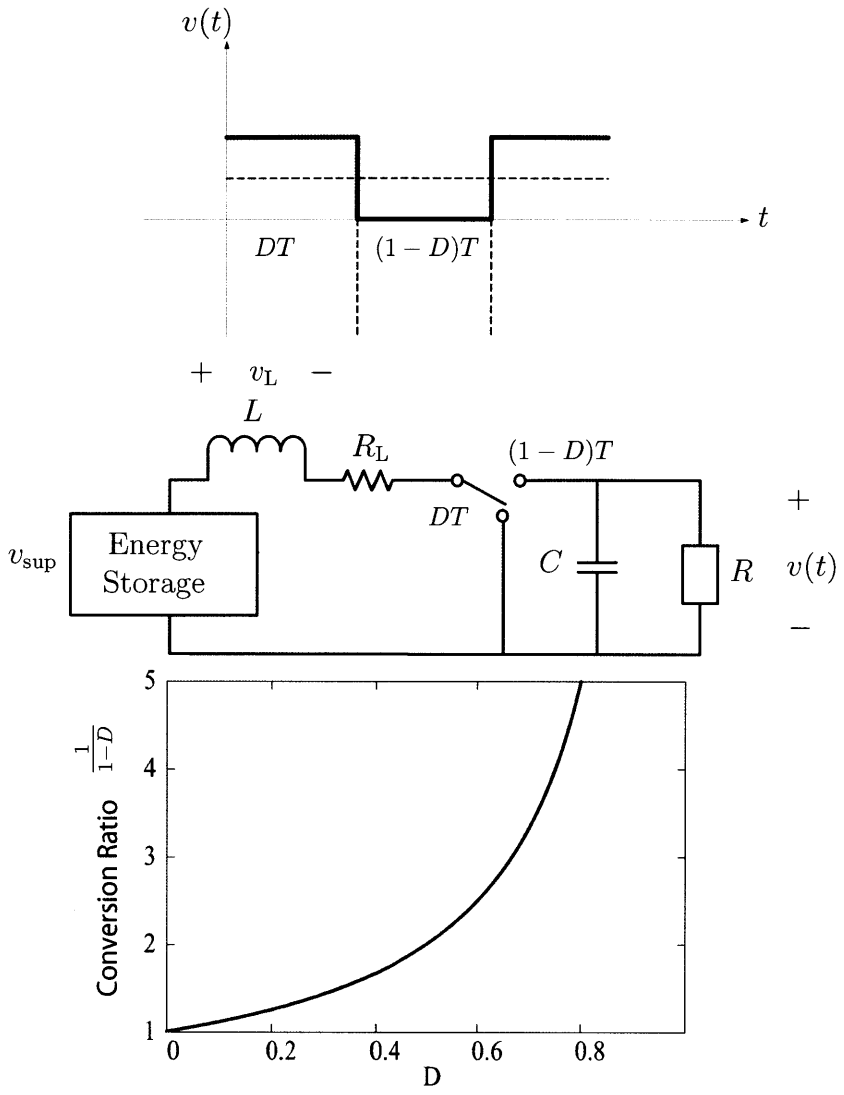


Figure 2-2: Typical boost converter circuit topology (top), duty cycle (middle), transfer characteristic (bottom).

is that magnetics are often large and expensive. In addition, the low achievable Q values (typically < 20) for on-chip inductors pose severe limitations on efficiency performance.

While boost and buck converters can achieve very high efficiencies (>85%) [38], the bulky magnetics required to do so make them and similar topologies undesirable for applications demanding ultra-small form factors. To a certain extent this tradeoff can be mitigated by running the converter at VHF frequencies ($>$ 100 MHz) [39], which makes the use of

on-chip inductors more feasible. However, the increased switching losses that come with running at such high frequencies, combined with the already augmented conduction losses in the on-chip inductors, makes achieving high efficiencies impossible. Techniques to mitigate high-frequency losses in VHF DC-DC converters are now becoming practical with nH sized inductors (e.g., zero-voltage switching, resonant gating) [40]. However, even at 110 MHz and excellent efficiency performance, the inductor box volume exceeds 183 mm^3.

2.3 Switched-Capacitor Converters

Switched-capacitor converters are a class of switched-mode converters that do not require magnetic storage elements used by inductor-based converters and can still achieve high efficiency by converting one voltage to another. While only capable of a finite number of conversion ratios, for a given conversion ratio and total rating of switches, switched-capacitor converters can support a higher power density compared with traditional converters [32]. The substantially superior energy and power density of capacitors with respect to inductors allow switched-capacitor networks to provide higher power density at equal or higher efficiency. To see this we must only compare the energy stored in a capacitor ($E_c = \frac{1}{2}Cv^2$) against that stored in an inductor ($E_L = \frac{1}{2}Li^2$) as shown in Fig. 2-3. For $C = 10$ nF in a 1.8-V process versus $L = 12$ nH at 1 A, $E_c/E_L > 2.7$. In practice, this ratio further favors switched-capacitor converters when we consider that there are significant losses associated with ripple current and ripple flux since full magnetization and de-magnetization is not possible.

Two major advantages of switched-capacitor converters is that they are small and amenable to integration. The drawback is that they are efficient at only one conversion ratio. This is acceptable for battery-powered applications since a battery can hold its output voltage steady over its lifetime, but is not acceptable for other energy storage elements where the output voltage varies over a wide range. In Chapter 4 we detail a proposal for dealing with a wide range of input voltages. In the following sections, however, we focus on the loss mechanisms that are specific to switched-capacitor converters.

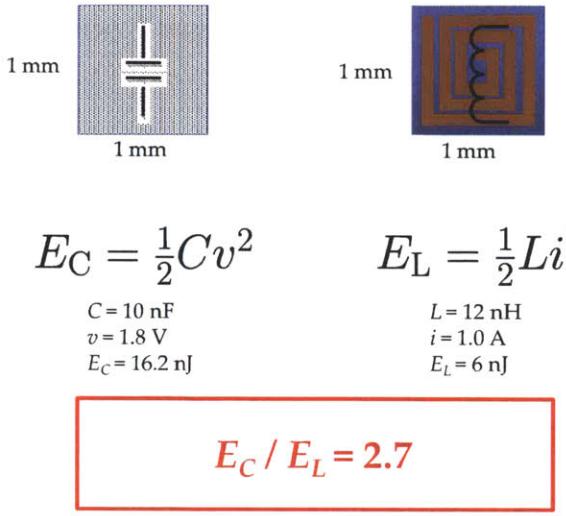


Figure 2-3: Energy density of capacitor versus inductor for today's CMOS process in 1 mm^2 area. The capacitor is implemented using gate oxide and the inductor using top layer metal (100 μm line width and 50 μm line spacing). The higher energy density of capacitor makes switched-capacitor-based converters more attractive for integrated applications.

2.3.1 The Energy Loss of Charging Capacitors

Switched-capacitor networks suffer from a fundamental deficiency that prevent capacitors from charging/discharging to a desired voltage with 100% efficiency. The power loss is due to ohmic dissipation in the connection between the voltage source and the capacitor being charged. Interestingly, the total energy lost is solely a function of the voltage change impressed on the capacitor, and *independent* of the resistance value [41]. The dual of this physical phenomenon is the case of an inductor that is charged by a current source. To illustrate this fundamental limitation, consider the circuit shown in Fig. 2-4. Assume the capacitor is initially discharged and $V > 0$; the current in the capacitor is given by $i(t) = C\frac{dV_c(t)}{dt}$. With a step function for the input, the capacitor voltage is given by

$$V_c(t) = V(1 - e^{-\frac{t}{RC}}). \tag{2.3}$$

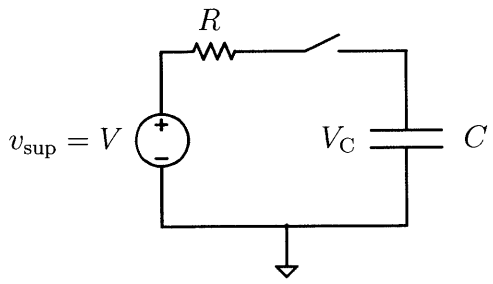


Figure 2-4: Example circuit to illustrate the fundamental efficiency limitation of switched-capacitor converters due to ohmic dissipation. The energy loss is independent of the value of the resistance value, R.

The energy drawn from the source in the charging process is given by

$$\begin{aligned} E_v &= \int_{0-}^{\infty} v_{\text{sup}} \cdot i_C(t)dt \\ &= \int_{0-}^{\infty} V \cdot i_C(t)dt = \int_{0-}^{\infty} \frac{V^2}{R} e^{-\frac{t}{RC}} dt \\ &= CV^2. \end{aligned} \tag{2.4}$$

In steady-state, the energy stored on the capacitor is $\frac{1}{2}CV^2$, resulting in an energy loss of $\frac{1}{2}CV^2$. Interestingly, we observe that the energy loss is indeed fixed and independent of R. This remains true even in the limit as R approaches zero.

The previous analysis assumed switched capacitors fully equilibrate so that capacitor currents can be modeled as impulsive, reaching nearly zero in a time that is small compared to the switching period. This is referred to as the Slow Switching Limit (SSL) [42]. In contrast, in Fast Switching Limit (FSL) operation, switched capacitors are not allowed to equilibrate (i.e., capacitors act like fixed voltage sources). The FSL case will be discussed next in Section 2.3.2. As an example, consider the 1:1 switched-capacitor circuit shown in Fig. 2-5. With the switching period much longer than the load time constant (slow-switching), the capacitor voltage is allowed to equilibrate. Fig. 2-6 illustrates the transient behavior of the circuit in Fig. 2-5 under SSL. For simplicity, rather than changing the switching speed, we change the size of the capacitor, C, from 100 μF for the SSL case to 500

mF for the FSL case.

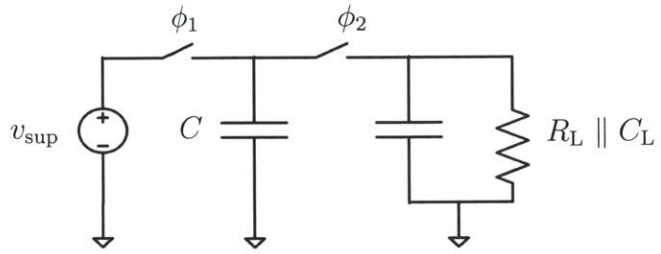


Figure 2-5: A 1:1 switched-capacitor circuit illustrates conduction loss mechanisms in switched-capacitor circuits due to switching speeds.

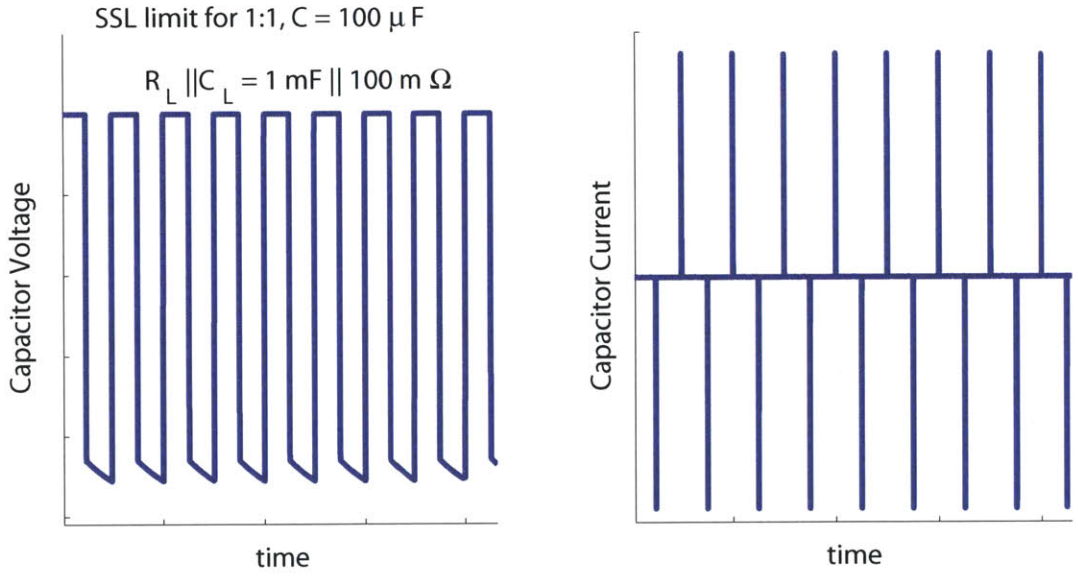


Figure 2-6: In the SSL, capacitor voltages equilibrate each half-cycle and currents are impulsive. The energy loss results in the familiar result of $\frac{1}{2}C(\Delta V_C^2)$.

Returning to Fig. 2-4, the energy lost through R is given by

$$E_{\text{tot}} = \int_{t=0}^{\infty} i_{\text{C}}(\tau)^2 R d\tau. \tag{2.5}$$

$V_C(t)$ is given by

$$V_C(t) = (V - V_C(0))(1 - e^{-t/RC}) + V_C(0), \tag{2.6}$$

and the capacitor current is $i_C = C\frac{dV_C(t)}{dt} = \frac{V-V_C(0)}{R}e^{-t/RC}$. This results in

$$\begin{aligned} E_{\text{tot}} &= -\frac{(V - V_C(0))^2}{2R} \cdot RC \left[e^{-2t/RC}\right]_0^{t_f} \\ &= \frac{(V - V_C(0))^2}{2} \cdot C \left[1 - e^{-2t_f/RC}\right] \end{aligned} \tag{2.7}$$

In SSL when the capacitors equilibrate, $t \gg RC$, and the exponential term in Eq. 2.7 falls out yielding a total energy loss of

$$E_{\text{tot,SSL}} = \frac{1}{2}(V - V_C(0))^2 C = \frac{1}{2}C(\Delta V_C)^2 \tag{2.8}$$

which is in agreement with Eq. 2.4.

2.3.2 Conduction Loss Associated with Fast Switched Capacitor Networks

In the fast-switching frequency regime, smaller packets of charge are shuttled from the source to the load and the charge-transfer capacitors maintain a nearly fixed voltage. In this case, switched-capacitor networks behave like resistors with a resistance equal to the switch resistances in each charge-transfer cycle. Switched capacitors operate in the fast-switching limit (FSL) when their voltages are not allowed to settle and they are switched at a fast rate compared to the load time constant such that there is negligible ripple on the capacitors (i.e., capacitors act like fixed voltage sources). Operating in FSL is appealing because, as we will see in Section 2.3.3, we can model a switched-capacitor network as an ideal transformer with an equivalent output resistance. Reducing the equivalent output resistance improves the efficiency performance of a switched-capacitor converter by limiting the ohmic losses incurred when charging/discharging capacitors. Fig. 2-7 illustrates the transient behavior

of the circuit in Fig. 2-5 under FSL. In the SSL case, we recall that the exponential term of

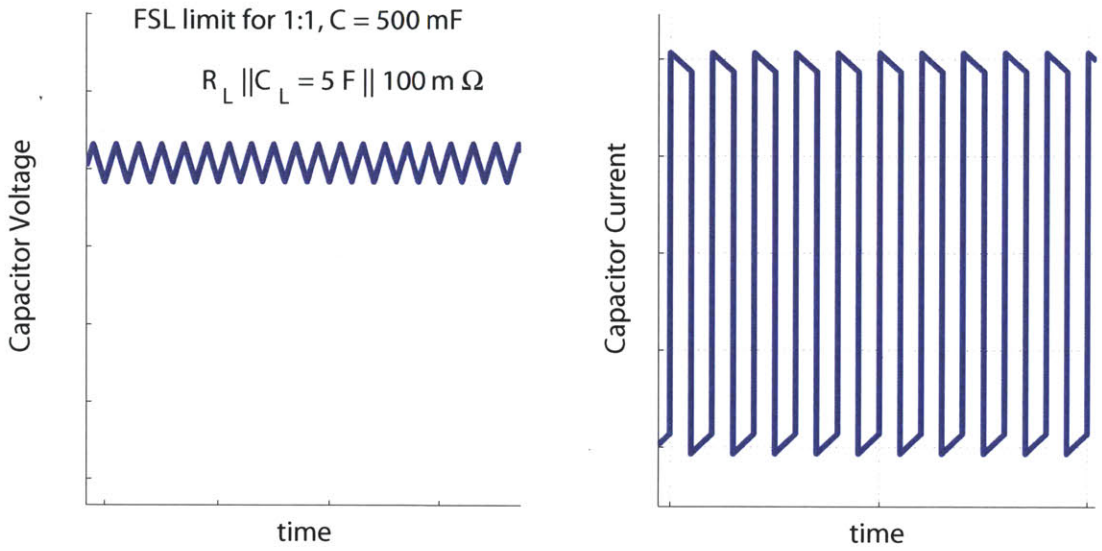


Figure 2-7: In the FSL, capacitor voltages are constant and capacitor currents are fixed during each half cycle. Higher switching frequencies reduce energy loss until the losses due to switch resistances dominate.

Eq. 2.7 vanishes. In the case of FSL, the total energy loss is given by

$$E_{\text{tot,FSL}} = \frac{1}{2}(V - V_C(0))^2 C \left[(1 - e^{-2t_f/RC}\right], \tag{2.9}$$

which has a dependency on R. Expanding into a Taylor series near $t = 0$, Eq. 2.9 assumes a form one would expect for two fixed voltages connected across a resistor:

$$E_{\text{tot,FSL}}(t) = \frac{1}{2}(V - V_{\text{C}}(0))^2 C(1 - (e^0 - \frac{2t}{RC}e^0 t)) = \frac{(V - V_{\text{C}}(0))^2 t}{R} \tag{2.10}$$

This observation suggests that switched-capacitor networks start to behave like resistors as the switching frequency is increased, which poses a limit to the efficiency and rapid transfer of smaller charge packets. In other words, the benefits from increasing the switching frequency are stymied when the charge transfer capacitors behave like ideal voltage sources and the

switch resistance dominate.

2.3.3 An Equivalent Model for Switched-Capacitor Converters

Switched-capacitor converters provide several advantages over inductor-based topologies including being more suited for integrated applications where area is scarce. For example, simple control techniques suffice to allow for light-load operation. A common technique for reducing total power losses during light load conditions is reducing the switching frequency [43]. However, the efficiency of switched-capacitor converters is inversely related to the output regulation capability for a given conversion ratio. To see this, we model a switched-capacitor converter stage using an ideal transformer with a conversion ratio $1{:}\alpha$ and output resistance, R_{eq}, as shown in Fig. 2-8 [44]. The output resistance, R_{eq}, is a function of the output current, switching frequency, and switched-capacitor topology. A method for determining R_{eq} using charge multiplier vectors is provided in [42]. The model of Fig.

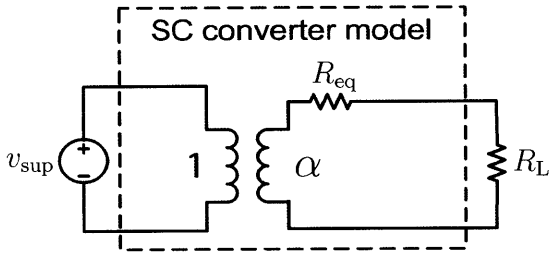


Figure 2-8: A model of a switched-capacitor converter model as an ideal transformer and equivalent output resistance. The conversion ratio, $1 : \alpha$, is determined by the topology. The equivalent output resistance is a function of switching frequency, charger transfer capacitors, and switch resistances.

2-8 provides a tractable construct for quickly analyzing and comparing different switched-capacitor networks using readily determined parameters once the topologies are known. For example, from the model in Fig. 2-8, we can determine that the upper limit for the efficiency of a switched-capacitor converter can be written as

$$\eta_{\text{max}} = \frac{1}{1 + R_{\text{L}}/R_{\text{eq}}} \tag{2.11}$$

To minimize losses through the switched-capacitor converter, the switching frequency, f_s, for a given topology is chosen to minimize R_{eq}. Consider the single-capacitor power transfer stage in Fig. 2-9. Modeling this 1:1 switched-capacitor converter stage as in Fig. 2-8, we write R_{eq}

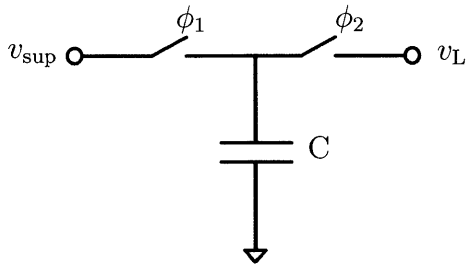


Figure 2-9: 1:1 switched-capacitor converter for illustrating effects of equivalent output resistance.

$$R_{eq} = \frac{1}{\kappa f_s C_{eff}}, \tag{2.12}$$

where κ is an exponential decay function that captures the slow-switching versus fast-switching limit behavior of the switched-capacitor converter stage [42] and can be modeled as a function of f_s, C, and R, the switch on-resistances as follows:

$$\kappa = \frac{1 - e^{-\frac{1}{4f_s RC}}}{1 + e^{-\frac{1}{4f_s RC}}} \tag{2.13}$$

As discussed in Section 2.3.1, in SSL the capacitor current can be modeled as impulsive, reaching nearly zero in a time that is very small compared $1/f_s$ ($\kappa \to 1$). Conversely, in FSL, the switched capacitors maintain nearly fixed voltages and the capacitor current during each switching state is nearly constant ($\kappa \to 0$). As f_s is increased, R_{eq} monotonically decreases, asymptotically approaching a lower bound of $2R$. This asymptotic behavior is illustrated for $C = 1$ nF and $R = 5\Omega$ in Fig. 2-10.

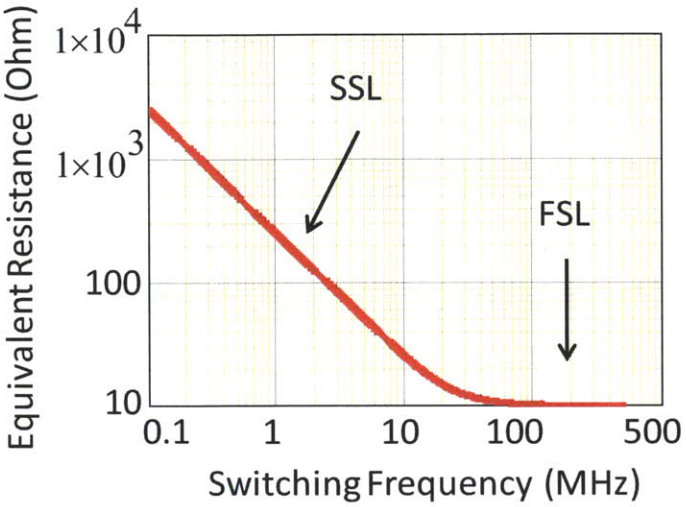
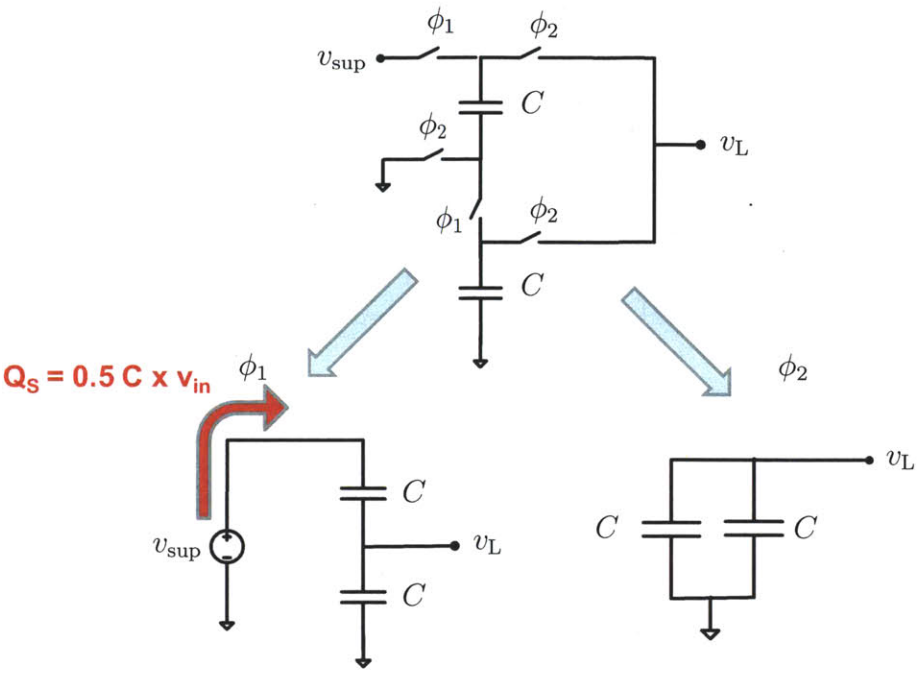


Figure 2-10: Equivalent output resistance, R_{eq}, of switched-capacitor circuit of Fig. 2-9 as a function of switching frequency showing the transition from SSL to FSL. As the switching frequency is increased, the equivalent output resistance asymptotically approaches $2R$, the switch resistances of Fig. 2-9.

2.3.4 Current Conversion and Current-Handling Capability of Switched-Capacitor Converters

From a physical basis, switched-capacitor networks are fundamentally current converters. In a first phase they split up charge across capacitors in one configuration. In a second phase, the capacitors are reconfigured to draw out the same charge in a different ratio. In periodic steady-state, the current conversion ratio of switched-capacitor converters is fixed because the average current into the topology capacitors is zero. This is the dual of inductor-based topologies where the voltage conversion ratio is fixed by volt-second balance (i.e., average voltage across inductor is zero). To see this, consider the simple example of a 2:1 switched-capacitor converter stage shown in Fig. 2-11. During phase-ϕ_1 the capacitors are connected in series and the source injects $Q_s = \frac{1}{2}C \times v_{\text{sup}}$ amount of charge across an electric potential of v_{sup}. During phase-ϕ_2, the capacitors are connected in parallel, the source is disconnected, and $2Q_s = C \times v_{\text{sup}}$ is delivered to the load through the node v_{L}. If this is done periodically at a switching frequency of f_{s}, then by conservation of energy



$$P_{in} = \tfrac{1}{2} f_s \cdot Q_s \cdot v_{sup} = \tfrac{1}{2} f_s \cdot \tfrac{v_{sup}}{2} C \cdot v_{sup} \qquad P_{out} = \tfrac{1}{2} f_s \cdot Q_{tot} \cdot v_L = \tfrac{1}{2} f_s \cdot v_{sup} C \cdot v_L$$

Figure 2-11: 2:1 switched-capacitor converter example illustrating current conversion function. During phase-ϕ_1 the capacitors are connected in series and the source injects $Q_s = \frac{1}{2} C \times v_{sup}$ amount of charge. During phase-ϕ_2, the capacitors are connected in parallel, the source is disconnected, and $2Q_s = C \times v_{sup}$ is delivered through the node v_L. If done at a switching frequency of f_s, then $i_{out} = 2 \cdot i_{in}$.

$(v_{in} \cdot i_{in} = v_{out} \cdot i_{out} \rightarrow v_{out} = \frac{1}{2} v_{in}, i_{out} = 2 \cdot i_{in})$ the expression for efficiency is given by

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{in}} \\ &= \frac{v_{out} i_{out}}{v_{in} i_{in}} \end{aligned} \tag{2.14}$$

Substituting $i_{out}/2 = i_{in}$ yields

$$\eta = \frac{v_L}{v_{in}/2} = \frac{v_L}{v_{NL}}, \tag{2.15}$$

where $v_{NL} = \frac{v_{in}}{2}$ and is the ideal no-load conversion ratio for the topology of Fig. 2-11. The no-load voltage transfer ratio, α, of a switched-capacitor converter is topology dependent

and is a function of the number of the charge transfer capacitors, the interconnection to the input and output terminals and among themselves. To capture the degradation in efficiency explicitly, we introduce the variable v_Δ to express the voltage drop below v_{NL} due to current flow to the load. We can re-write Eq. 2.14 as

$$\eta = \frac{P_{\mathrm{L}}}{P_{\mathrm{sup}}} = \frac{v_{\mathrm{NL}} - v_\Delta}{v_{\mathrm{NL}}} = 1 - \frac{v_\Delta}{v_{\mathrm{NL}}}. \tag{2.16}$$

From Fig. 2-8, we can express v_{L} as

$$\begin{aligned} v_{\mathrm{L}} &= \alpha \cdot v_{\mathrm{sup}} - R_{\mathrm{eq}} \cdot I_{\mathrm{L}} \\ &= v_{\mathrm{NL}} - v_\Delta. \end{aligned} \tag{2.17}$$

We can also derive the load current capability of the switched-capacitor network as

$$I_{\mathrm{L}} = v_\Delta \cdot \kappa f_{\mathrm{s}} C_{\mathrm{eff}}. \tag{2.18}$$

The voltage swing across the capacitors is proportional to v_Δ and results from non-zero loads. Note that the larger v_Δ is, i.e., the more v_{L} is below the no-load voltage, the more power the converter can deliver. Fig. 2-12 plots the load current versus frequency with varying switch resistance R_{sw} for a 5:3 switched-capacitor converter with v_{sup} =1.8 V. From Fig. 2-10 and Fig. 2-12, it would appear that increasing the switching frequency towards the asymptotes of both current-handling limits and R_{eq} would offer increased current-handling capability and reduced conduction losses. Missing from the analysis is consideration for loss mechanisms resulting from other phenomena. Section 2.3.6 will give insights as to how much the switching frequency can be increased before the efficiency degradation becomes significant due to additional loss mechanisms beyond conduction losses. Careful consideration of the significant loss mechanisms in tandem with desired current-handling capability informs how to select the region of operation to maximize efficiency.

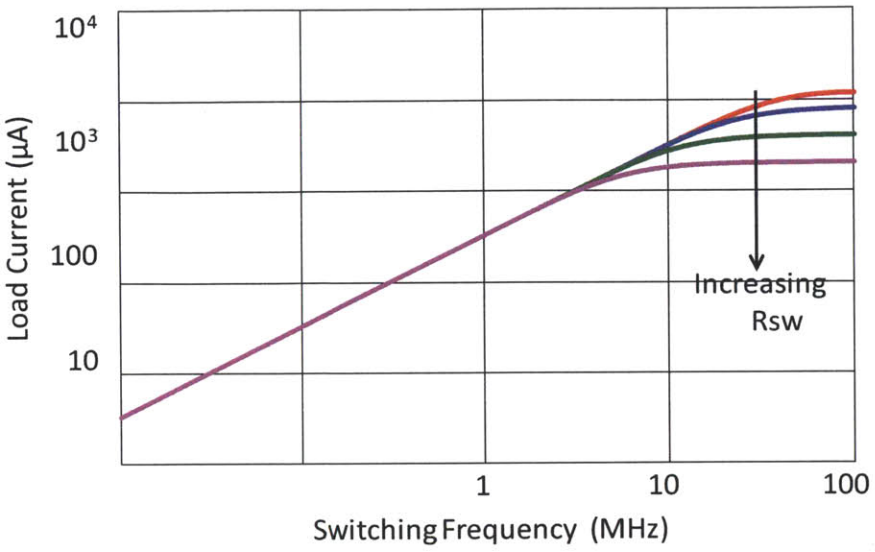


Figure 2-12: Load current versus switching frequency for increasing values of switch resistance for a 5:3 topology with a 1.8-V input voltage.

2.3.5 Wide Input Range Handling Capabilities of Switched-Capacitor Converters

Eq. 2.16 indicates that very high efficiency can be attained if the desired regulated output voltage, v_{L}, is given by v_{NL} (i.e., $v_{\Delta} \approx 0$). For wide input ranges, if no regulation control is implemented, the efficiency is fixed as given by Eq. 2.16. However, if regulation of the output is desired, the efficiency varies with the input as

$$\eta(v_{\mathrm{supply}}) = \frac{v_{\mathrm{L}}}{\alpha \cdot v_{\mathrm{supply}}} \tag{2.19}$$

where α is the conversion ratio. This implies that for non-zero loads, the efficiency degrades as the output voltage moves away from the ideal no-load value.

In order to increase the average efficiency, the conversion ratio, α, must be made variable with the input. This is analogous to inductor-based converters since the duty cycle is more accurately represented as $D(t) = D_o + \widetilde{d}(t)$, where D_o is the operating point duty cycle and $\widetilde{d}$ is the small-signal input duty cycle. Note that for an inductor-based topology the voltage

conversion ratio and efficiency are independent of the input and output voltages. This is the dual to the switched-capacitor converter where the efficiency is proportional to both the input and load voltages while the current conversion ratio remains fixed. For applications where high efficiency and a wide input voltage range is required and inductor-based topologies are not viable as in [45], using an switched-capacitor converter with multiple conversion ratios is necessary. Additional control enables selecting the conversion ratio that maximizes the average efficiency, over a certain input range (i.e., minimize $v_\Delta = |v_{\mathrm{NL}} - v_{\mathrm{L}}|$).

As another simple example, consider the circuit of Fig. 2-13. For an input provided by a capacitor bank modeled as C_{big} and assuming the switched-capacitor converter operates in the FSL, the input discharges linearly for a constant current draw at the load. This is because R_{eq} remains nearly constant despite the increases in f_{s} required to maintain a constant I_{out} at $v_{\mathrm{L,o}}$ using pulse frequency modulation. The input can be written as

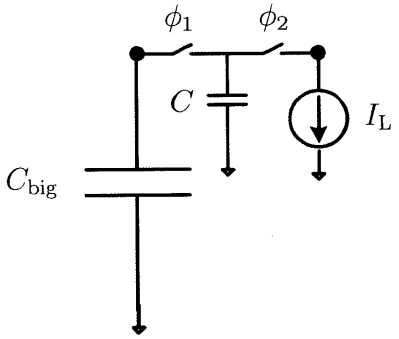


Figure 2-13: 1:1 switched-capacitor converter discharging capacitor C_{big} used to illustrate effect of wide-range input voltages on efficiency performance.

$$v_{\mathrm{in}}(t) = V_{\mathrm{init}} - \int_{-\infty}^{t} \frac{I_{\mathrm{L}}}{C_{\mathrm{big}}} dt \tag{2.20}$$

where V_{init} is the initial voltage stored on C_{big}. For the 1:1 converter of Fig. 2-9, the average efficiency over a discharge cycle is given by

$$\eta_{\mathrm{avg}} = \frac{1}{\alpha} \cdot \frac{\frac{v_{\mathrm{L}}}{V_{\mathrm{init}} - \int_{t_o}^{t} \frac{I_{\mathrm{L}}}{C_{\mathrm{big}}} dt}}{t - t_o} \tag{2.21}$$

Fig. 4-2 shows the voltage of C_{big} discharging from 3.5 V to 1 V and $v_{\text{L}} = 1\text{V}$, corresponding to the ideal efficiency rising from 28.5% to 100%. Using Eq. 4.2, we find $\eta_{\text{avg}} = 42.7\%$, which is clearly unacceptable for many applications. Thus, we see that the efficiency of charge

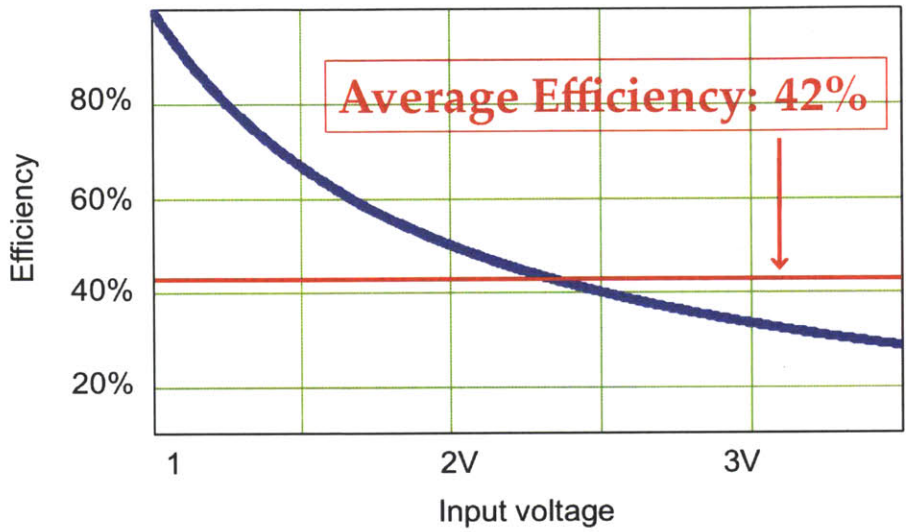


Figure 2-14: Efficiency versus input voltage corresponding to the 1:1 switched-capacitor converter of Fig. 2-13. The efficiency performance is analogous to a linear voltage regulator. High-efficiency is limited to a very limited range of input voltages.

transfer is in all cases linearly dependent on the load voltage v_{L}. This can be extended to any topology of a switched-capacitor converter all of which are fundamentally limited in efficiency to $v_{\text{L}}/v_{\text{NL}}$. This fundamental limitation in efficiency is because of conduction losses resulting from using switches. The efficiency may be further degraded due to the presence of other loss mechanisms, which will be discussed in the next section.

2.3.6 Additional Loss Mechanisms for Switched-Capacitor Converters

Energy-constrained applications render the efficiency of energy processing blocks paramount. In many instances refurnishing energy by battery replacement, recharging, or other methods is inconvenient, costly, or not possible. For example, it is desirable to subject a bio-implant

patient to the least number of surgical procedures for the purpose of recharging or battery replacement. For a system to achieve this, (1) the energy processing blocks must introduce little overhead and process energy efficiently, and (2) signal and data processing blocks must also operate efficiently and consume as low power as possible.

The overall efficiency of such a system can be expressed as the ratio between the total energy delivered to a load per cycle (E_{L}) to the sum of the energy extracted from the source (E_{sup}) and the sum of energy losses per cycle.

$$\eta = \frac{E_{\mathrm{L}}}{E_{\mathrm{sup}} + \Sigma E_{\mathrm{losses}}}. \tag{2.22}$$

The primary loss mechanisms in switched-capacitor converters are discussed in the following sections.

Conduction

Charging and discharging energy transfer capacitors through a switch is inherently lossy. The equivalent resistance, R_{eq}, discussed earlier models the effect of non-ideal switches. The power loss in the capacitor can be expressed as

$$P_{\mathrm{c}} = R_{\mathrm{eq}}(f_{\mathrm{s}}) \cdot I_{\mathrm{L}}. \tag{2.23}$$

For on-chip implementations, the capacitor switching losses can be estimated by finding the total parasitic capacitances at various nodes and the voltage swing across the capacitances.

Bottom-plate parasitic capacitors

For fully-integrated switched-capacitor converter designs, there are a number of options for constructing capacitors. Constructing metal-metal, double-poly, or MOS-based capacitor elements is straightforward. For capacitors implemented using two metal layers, parasitics arise due to the capacitance from the bottom-plate to the substrate. For gate-oxide capacitors implemented with the N-well as the bottom-plate, the parasitic is caused by the the reverse

biased diode capacitance of the N-well to P-substrate junction. Care must be taken to guard against bottom-plate effects, which are a second significant efficiency degradation mechanism in switched-capacitor converters due to charging and discharging the substrate-coupled parasitic capacitors. The bottom-plate capacitance can be expressed as

$$C_{\mathrm{BP}} = \alpha_{\mathrm{bp}} C, \tag{2.24}$$

where α_{bp} can be above 10% depending on process technology. Techniques to reduce bottom-plate losses and recover energy have been shown in [46]. Assuming a capacitor C_i is charged to v_i each cycle, the energy loss per cycle due to bottom-plate parasitics C_{BP} can be give by

$$E_{\mathrm{BP}} = \alpha_{\mathrm{bp}} \cdot \frac{C_i v_i}{2}. \tag{2.25}$$

Gate-drive loss

A third significant contributor to power loss and efficiency degradation is due to switching the gate capacitances of the charge-transfer switches. The energy expended in switching the gate capacitances of the charge-transfer switches every cycle can be given by

$$E_{\mathrm{sw}} = C_{\mathrm{ox}} W_{\mathrm{T}} L V_{\mathrm{sup}}^2 \tag{2.26}$$

where C_{ox} is the gate-oxide capacitance per unit area, W_{T} is the cumulative width of switches that are turned cycled, and L is the minimum channel length of the technology node in which the switched-capacitor converter is implemented.

Control circuitry

The inherent loss mechanisms of switched-capacitor converters and on-chip implementations motivates maintaining control circuitry overhead minimal to realize voltage regulation and desired operation. Control circuitry losses are comprised of two components: (1) dynamic, and (2) quiescent, which is dominantly due to leakage in all-digital control. Assuming no

quiescent power consumption for all-digital control, the losses per cycle can be decomposed and expressed as follows:

$$E_{\text{ctrl}} = C_{\text{ctrl}} v_{\text{sup}}^2 + \frac{1}{f_s} \left(I_{\text{leak}} v_{\text{sup}} \right) \tag{2.27}$$

where C_{ctrl} is the equivalent capacitance switched in the control circuit per cycle and I_{leak} is the total leakage current consumed by the control circuitry.

2.3.7 An Efficiency Analysis of a Switched-Capacitor Converter

In this section, we provide a treatment of efficiency analysis of switched-capacitor circuits using the results from the previous sections. This will provide guiding insights as to how to balance the competing mechanisms of efficiency performance, current-handling capability, and the the various loss mechanisms encountered.

A general expression for power efficiency can be expressed as

$$\eta = \frac{P_{\text{delivered}}}{P_{\text{sup}} + P_{\text{sw}} + P_{\text{bp}} + P_{\text{ctrl}}}. \tag{2.28}$$

First, we derive a relationship between energy delivered to a load and energy supplied from a source. To do this, we neglect operational and parasitic losses. It will be useful to recall that v_{L} and v_{NL} can be expressed as

$$v_{\text{L}} = v_{\text{NL}} - v_{\Delta} \tag{2.29}$$

$$v_{\text{NL}} = \alpha_i \cdot v_{\text{sup}} \tag{2.30}$$

In addition, recall from Eq. 2.16, repeated here for convenience, the fundamental efficiency limit due to conduction losses alone can be expressed as

$$\begin{aligned} \eta &= \frac{v_{\text{L}}}{v_{\text{NL}}} \\ &= 1 - \frac{v_{\Delta}}{v_{\text{NL}}} \end{aligned} \tag{2.31}$$

Since $\eta = \frac{E_L}{E_{sup}}$, we observe that the energy delivered to the load can be expressed as a linearly scaled version of the energy extracted from the source as follows

$$E_L = E_{sup} \cdot \frac{v_{NL} - v_\Delta}{v_{NL}}. \tag{2.32}$$

In the previous section, we provided analytical expression for energy losses per cycle due to bottom-plate effects, switching/gating losses, and control circuitry overhead. The power delivered to the load is determined by the topology and equivalent resistance and is expressed as

$$P_{delivered} = v_L \cdot I_L = (v_{NL} - v_\Delta) \cdot \frac{v_\Delta}{R_{eq}}. \tag{2.33}$$

Similarly, the power supplied from the source is given by

$$P_{sup} = v_{sup} \cdot \alpha_i \cdot I_L = v_{sup} \cdot \alpha_i \cdot \frac{v_\Delta}{R_{eq}}. \tag{2.34}$$

The power lost due to bottom-plate parasitics depends on the switched-capacitor topology and can be expressed as

$$P_{bp} = \alpha_{bp} C \cdot v(\alpha_i, v_{sup}, \ldots))^2 \cdot f_s = K_{bp} \cdot v_{sup}^2 \cdot f_s, \tag{2.35}$$

where the voltage value $v(\alpha_i, v_{sup}, \ldots)$ that the bottom-plate capacitor exhibits depends on the topology. For a 1:1 topology, no bottom-plate effects are present since the parasitic capacitor remains grounded in each cycle. On the other hand, for the 2:1 topology of Fig. 2-11, the top capacitor's bottom-plate parasitic is charged to $v_{sup}/2$ during ϕ_1 and discharged to ground during ϕ_2.

The gating loss can be estimated as

$$P_{sw} = n \cdot C_{ox} W L \cdot v_{sup}^2 \cdot f_s = K_{sw} \cdot v_{sup}^2 \cdot f_s, \tag{2.36}$$

where n is the number of switched devices (assuming identical switches).

Finally, losses due to control circuitry can be express as

$$P_{\text{ctrl}} = \left(K_c \cdot v_{\text{sup}}^2 + I_{\text{leak}} \cdot v_{\text{sup}} \cdot f_{\text{s}}^{-1}\right) \cdot f_{\text{s}}, \tag{2.37}$$

where dynamic and quiescent components are expressed separately.

We can now take the losses into account to arrive at an expression for the overall efficiency. after simplification, Eq. 2.28 becomes

$$\begin{aligned}\eta &= \left[1 - \tfrac{v_\Delta}{v_{\text{NL}}}\right] \cdot \left[1 + K_{\text{sw}} \cdot \frac{v_{\text{sup}}^2 \cdot f_{\text{s}}}{\alpha_i \cdot v_{\text{sup}} \frac{v_\Delta}{R_{\text{eq}}}} + K_{\text{bp}} \cdot \frac{v_{\text{sup}}^2 f_{\text{s}}}{\alpha_i \cdot v_{\text{sup}} \frac{v_\Delta}{R_{\text{eq}}}} + \right. \\ &\qquad \left. K_c \cdot \frac{v_{\text{sup}}^2 \cdot f_{\text{s}}}{\alpha_i \cdot v_{\text{sup}} \frac{v_\Delta}{R_{\text{eq}}}} + \frac{I_{\text{leak}} \cdot v_{\text{sup}} \cdot f_{\text{s}}^{-1}}{\alpha_i \cdot v_{\text{sup}} \frac{v_\Delta}{R_{\text{eq}}}} \cdot f_{\text{s}}\right]^{-1} \\ &= \left[1 - \tfrac{v_{\text{NL}} - v_{\text{NL}}}{v_{\text{NL}}}\right] \cdot \left[1 + \frac{v_{\text{sup}} \cdot f_{\text{s}}}{\alpha_i \cdot I_{\text{L}}} \cdot (K_{\text{sw}} + K_{\text{bp}} + K_c) + \frac{1}{\alpha_i} \cdot \frac{I_{\text{leak}}}{I_{\text{L}}}\right]^{-1}.\end{aligned} \tag{2.38}$$

The expression shows the degrading effect of the various loss mechanisms and introduces frequency dependence due to charging and discharging parasitic capacitors and switch gates. We can calculate the efficiency of the 1:1 switched-capacitor circuit of Fig. 2-9 assuming $I_{\text{L}} = 250\mu\text{A}$, a charge-transfer capacitor $C = 1\text{nF}$, $v_{\text{L}} = 1\text{V}$, $K_{\text{sw}} = 340\text{fF}$ ($W = 100\mu\text{m}$, $R_{\text{sw}} = 2\Omega$), $K_c = 100\text{fF}$, and $I_{\text{leak}} = 0.1\text{nA}$. Note that for the 1:1 case $K_{\text{bp}} = 0$. Fig. 2-15 plots the efficiency for v_{sup} =1.2 V (blue), 1.8 V (orange), 2.3 V (red), and 2.8 V (brown) and corresponding conversion ratios of $\alpha_i = 1$, 0.6, 0.5, and 0.4 respectively. The ideal efficiency (i.e., low switching frequency) is determined by Eq. 2.31 and only takes conduction losses into account. The switched-capacitor circuit used to generate the conversion ratios is discussed in Chapter 4 and is carefully designed to provide multiple conversion ratios by selectively activating switches (Table 4.2). It is interesting to note that both the rate of roll-off and where the frequency of roll-off occurs is expected to be different for different conversion ratios. The reason is simply due to the topology. Assuming operation in FSL and equal switch resistances, a topology with less active switches (i.e., lower total switch resistance)

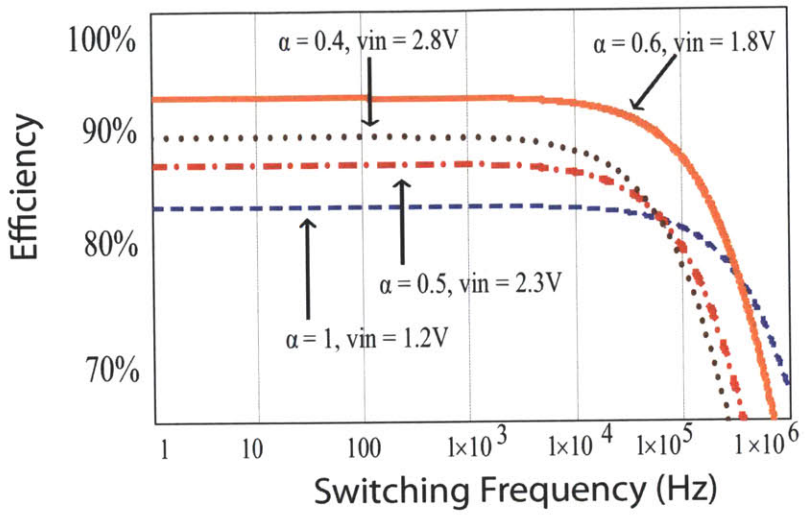


Figure 2-15: Efficiency versus switching frequency for four input voltages and switched-capacitor topologies (i.e., conversion ratios). Plots are shown for v_{sup} =1.2 V (blue), 1.8 V (orange), 2.3 V (red), and 2.8 V (brown) and corresponding conversion ratios of α_i = 1, 0.6, 0.5, and 0.4 respectively. The switched-capacitor circuit used to generate the conversion ratios plotted in Fig. 2-15 is discussed in Chapter 4 and is carefully designed to provide multiple conversion ratios by selectively activating switches (Table 4.2).

during charge transfer results in higher efficiency over a wider range of switching frequencies; however, from Eq. 2.13 we see that lower total switch resistance yields faster roll-off of the hyperbolic-like function. For v_{L} = 1V and v_{sup} = 1.2V, 1.8V, 2.3V, and 2.8V, Eq. 2.31 yields 83.3%, 92.6%, 87%, and 89.3%, respectively.

In Fig. 2-16 we set $K_{\text{bp}} = 0$, ignore losses due to leakage, and fix v_{sup} = 1.8 V and α_i = 0.6 to illustrate the effect of the switch resistance R_{sw} on efficiency. We substitute Eq. 2.18 into Eq. 4.10 to capture the dependence of switch resistance in the parameter κ ($\kappa \sim e^{R_{\text{sw}}}$) as well as in K_{sw} since $R_{\text{sw}} \propto W$. Clear trade-offs exist to guide the (1) sizing of the gate switches, (2) switching frequency, and (3) load current. One such tradeoff is area and switching frequency. If area needs to be minimized, small switch sizes are desired; however, this yields larger values for R_{sw} limiting the switching frequency range that yields high efficiency. The analytical models shown graphically in Fig. 2-12, Fig. 2-15, and Fig. 2-16 provide guidance for selecting the optimal operating conditions for a given technology,

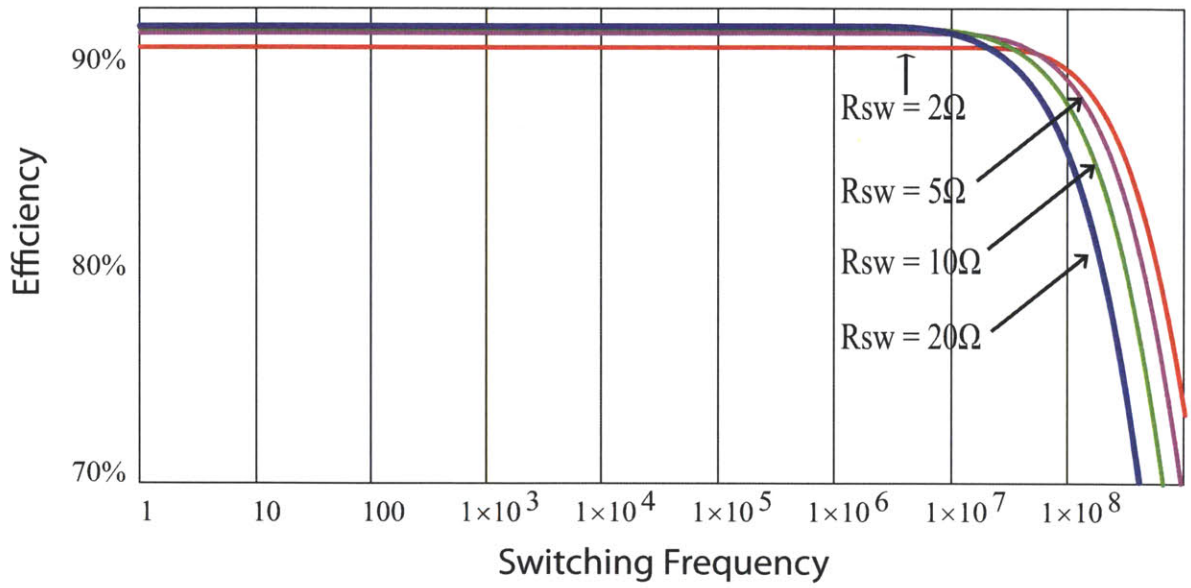


Figure 2-16: Efficiency versus switching frequency for various values of switch resistance on a fixed topology. Smaller switches yield higher efficiency for slow switching but drop off in efficiency faster due to κ. This affects load-handling as shown in Fig. 2-12 and it may be better to use larger switches with lower resistances.

load current, input range, and switched-capacitor topology. For example, from Fig. 2-12, it is noteworthy that operating above 10 MHz does not lead to any significant increase in the load current for various values of R_{sw}. However, as seen in Fig. 2-16, the efficiency begins degrade quickly depending on the switch resistance value.

2.4 Summary and Conclusions

Switched-capacitor converters provide several advantages over linear regulators and inductor-based topologies, and are suitable for integrated applications where area is scarce. This chapter provided a treatment on modeling switched-capacitor circuits. An overview of the fundamental efficiency limitations of switched-capacitor circuits and the inherent loss mechanisms were also provided to help guide design decisions for different applications. It was shown that in order to increase the cycle efficiency of a switched-capacitor converter accommodating a wide-input-range, the conversion ratio must be made variable with the input. This is the dual to varying the duty cycle of an inductor-based converter. Where high efficiency and wide-input-range is required and inductor-based topologies are not viable, a switched-capacitor converter with multiple conversion ratios can be implemented to maximize the cycle efficiency for a given number of capacitors and switches.

Chapter 3

Energy Management System for Bio-Implants Using Ultracapacitors in 180-nm CMOS

Trends in the medical industry have created a growing demand for implantable devices. While traditionally relying on batteries as energy storage elements, there is emerging interest in using high-density energy storage elements, such as ultracapacitors [27]. Ultracapacitors lack the energy density of batteries, at present falling short by approximately an order of magnitude. However, they have several compelling advantages. Chief among them is the promise they hold of being integrated on a chip as indicated in research in carbon nanotube based ultracapacitors in [1]. In addition to the potential for an extremely small form factor, ultracapacitors feature: high *power* density, a practically unlimited number of recharge cycles, extremely rapid recharging, and a direct relationship between the terminal voltage and its state of charge.

In this chapter we present energy management and low-power techniques to help solve the engineering challenges posed by using ultracapacitors for energy storage. We present an energy management integrated circuit (EMIC) example towards the end of the chapter [47]. A major problem with using any capacitor as an energy source is the fact that its voltage

drops rapidly with decreasing charge. This leaves the circuit to cope with a large supply variation and can lead to energy being left on the capacitor when its voltage gets too low to supply a sufficient supply voltage for operation [1]. The chip presented in this chapter has a switched-capacitor (S.C.) DC-DC converter to regulate the output voltage, which is referenced to a bandgap reference that draws less than 4 nW. In addition, rather than use a single ultracapacitor, we demonstrate higher energy efficiency by splitting a single capacitor into an array of capacitors that are progressively reconfigured as energy is drawn out. Finally, we take into account the "start-up" problem, or restoring charge to an ultracapacitor array that has completely lost charge after being implanted. The energy management IC described in this chapter is able to recharge from RF energy coupled into an antenna, even from the zero-charge state.

3.1 Mitigating Capacitor Voltage Discharge Characteristic

Ultracapacitors can serve as viable energy storage elements for diverse applications. Using an ultracapacitor to power portable electronics is not a new idea. In particular, ultracapacitors have been used as intermediate energy storage elements in audio and other applications [48, 49]. In general due to their high power densities, ultracapacitors have enjoyed a niche position in the automotive and aviation industries. For similar reasons, they have also served as secondary sources, surge-protectors, or high power density components [50–52].

From a circuit's point of view, the main advantage of using batteries lies in the constant voltage versus time characteristic. Fig. 3-1 shows typical voltage versus time characteristic for the $LiMgO_2$ (manganese dioxide lithium) coin cell battery in Table 1.1. From the Ragone plot of Fig. 1-2, current commercial ultracapacitors fail to match the energy densities of batteries. Therefore, the voltage drop across a capacitor starts sooner when compared to a similarly sized battery. In order to use capacitors to approximate a battery's voltage versus

[1] Note that 100 mV left on a 1 F ultracapacitor translates to 100 mJ, enough to power a 10 μW implant for almost 3 hours.

time characteristic, special care must be taken to mitigate the sagging voltage versus time characteristic.

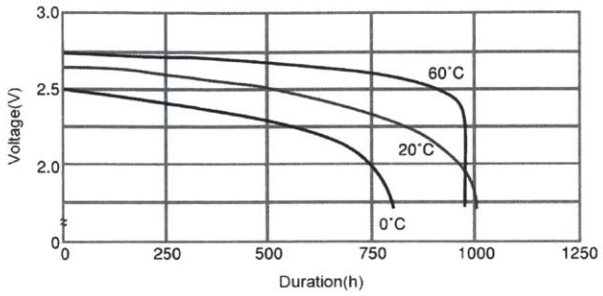


Figure 3-1: Voltage characteristics for manganese dioxide lithium coin cell battery illustrating the ability of the battery to maintain a steady voltage over its lifetime.

The issues that accompany employing ultracapacitors as power sources are a fundamental consequence of the linear voltage drop due to a constant current draw. The relatively low energy densities together with the linear characteristic pose barriers for the feasibility of ultracapacitors as power sources where a constant voltage level is important for performance. If instead of using a single component, however, a bank of ultracapacitors are used, stacking of individual capacitors legs allows a bank to maintain a voltage level even as the energy is drained. This in turn increases the operational time of circuits relying on a reference voltage range. Fig. 3-2 illustrates this idea. Initially, the four parallel capacitors are charged to v_{uc}. In this configuration, the most amount of energy is present and given by $E_{\text{init}} = 2Cv_{\text{uc}}^2$. Once $v_{\text{uc}}(t)$ drops below the lower threshold, the array stacks. For the example shown, stacking occurs in two steps. The number of stacking steps, capacitor legs, and the number of switches required depends on the acceptable energy utilization and output voltage variation. These are discussed in the next sections.

From Fig. 3-2, we can see it is possible to obtain arbitrarily small voltage variations in a bank with n elements. Practically speaking, this can result in prohibitively large banks (see Fig. 3-3). Yet, combining ultra-low power techniques with an appropriate stacking discipline enables moderate values for ultracapacitors (1-100mF) to approach feasible sizes. This was previously unimaginable for on-chip applications due to area limitations. The integration of

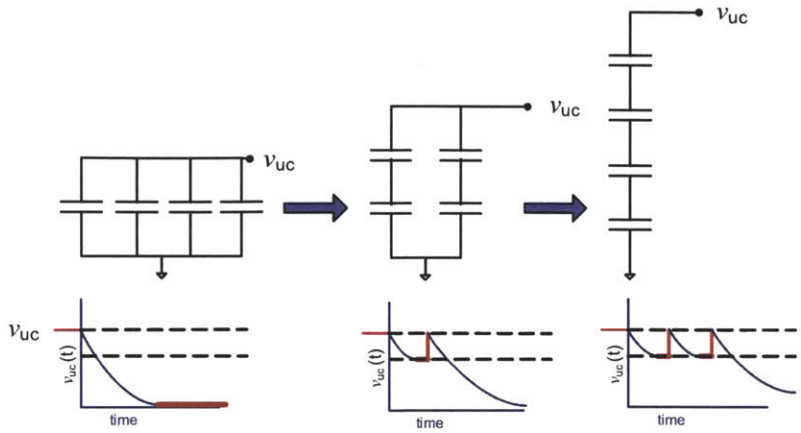


Figure 3-2: Illustration of stacking of capacitors for mitigating the voltage droop characteristic of capacitors as energy storage alternatives to batteries. Intelligently stacking the capacitor legs could allow prolonged operation for powered electronics as well as use more of the energy stored initially. The number of stacking steps, capacitor legs, and the number of switches required depends on the acceptable energy utilization and output voltage variation.

ultracapacitors for on-chip applications storing enough energy to power a medical implant between recharge cycles has been demonstrated [27].

Figure 3-3: Interconnection of commercial, discrete ultracapacitors to form banks in order to minimize voltage variation and/or maximize energy utilization.

3.1.1 Energy Utilization

Consider the commonly encountered architecture employing ultracapacitors of Fig. 3-4. The power converter regulates the output voltage level and compensates for variations on

the ultracapacitor bank voltage due to charging and discharging. If the maximum voltage of an ultracapacitor bank is v_{init} and the power converter operates down to v_{final} ($v_{\text{init}} > v_{\text{final}}$), then the energies remaining and used, respectively, on the ultracapacitor bank toward the end of the operating input range are given by

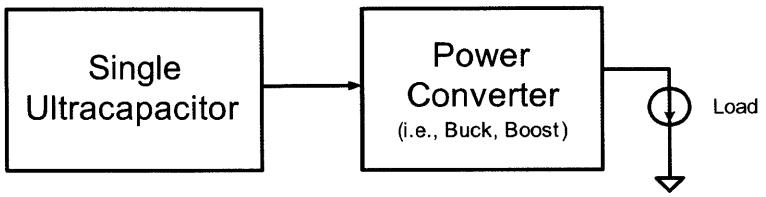


Figure 3-4: Common power converter architecture using static or single ultracapacitor. The power converter regulates the output voltage level and compensates for the voltage variation on the ultracapacitor bank voltage due to charging and discharging. The drawback of this approach is that once the voltage level of the single ultracapacitor drops below a certain level, subsequent electronics including the power converter, may no longer operate correctly.

$$E_{\text{final}} = \frac{1}{2}C \cdot v_{\text{final}}^2 \tag{3.1}$$

$$E_{\text{uc}} = \frac{1}{2}C \cdot (v_{\text{init}}^2 - v_{\text{final}}^2) \tag{3.2}$$

E_{final} can be substantial amount of energy.

For certain applications, the voltage drooping may be tolerable provided the power converter operating input range is large enough. In particular, in applications where area/weight considerations are immaterial, large ultracapacitor banks may be constructed to supply any load for a predetermined period. Resorting to larger banks, however, does not result in improved efficiency, which is an inherent problem of using a static ultracapacitor bank. By implementing a reconfigurable bank scheme as shown in Fig. 3-5, stacking mitigates these issues. Referring to Fig. 3-2, assuming all the ultracapacitors are equal in size and with $v_{\text{init}} = 2v_{\text{final}}$, stacking results in utilization of 98.4% of the total energy initially stored on the ultracapacitors. This is a 31% increase in energy utilization. In general, the energy utilization from stacking can be computed as

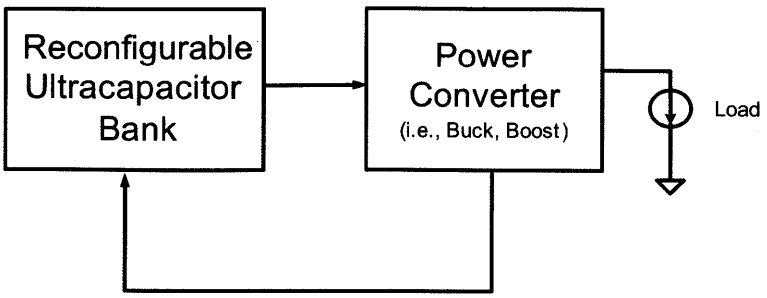


Figure 3-5: Energy management scheme adopting a reconfigurable ultracapacitor bank. A reconfigurable scheme mitigates the voltage droop resulting from draining energy out of the capacitors and can increase the energy utilization.

$$\eta_{\text{EU}} = \frac{E_{\text{delivered}}}{E_0} = 1 - \frac{1}{2^{2(N-1)}} \cdot \left(1 - \frac{v_{\text{uc,min}}}{v_{\text{uc,max}}}\right)^2 \tag{3.3}$$

where n is the number of capacitors in the array, and assuming the binary stack discipline as shown in Fig. 3-2. Eq. 3.3 shows that increasing n results in improved energy efficiency. Reducing v_{final} also yields greater energy efficiency; however, there is a lower limit of v_{final} set by the headroom requirements of the circuits powered by the capacitor array. The implications of the stacking discipline adopted are important and application-driven [6, 47]. Important considerations include number of switches, energy utilization, and permissible voltage variation at the output. The next section provides a discussion of these considerations.

From Eq. 3.3 it is clear that there is a trade-off between the capacitor array size and the maximum energy efficiency that is achievable when using reconfigurable ultracapacitor banks. In other words, to first order there is no tradeoff between efficiency and area if one keeps the total capacitance the same. For instance, in using a single 4F capacitor versus four 1F capacitors, the total area remains the same, but the energy efficiency of the four capacitor array is far superior. Therefore, for a fixed area, one might be tempted to increase the number of capacitors, n, in the array. First, this is the same as reducing the unit size, which may be limited by a particular process. Second, as n increases, stacking transitions occur more frequently as the capacitance decreases. Thus, a suitable array size with a manageable number of transitions that minimizes overhead in switches and control circuitry

might be four unit size capacitors.

Depending on the application and CMOS technology being used, a drawback of using ultracapacitors is that the substrates impose a maximum voltage of 2-3 V. In environments with loose supply requirements, the static configuration shown in Fig. 3-4 serves as a feasible solution. Current trends in integrated circuit design, however, aim toward aggressive reductions in the supply voltage. Unlike a high-voltage situation [50–52], typical sub-micron CMOS voltage supply levels ($v_{\mathrm{DD}} < 1.8$ V) do not afford power converter topologies large dynamic ranges. Moreover, lifetime is a critical specification. Assuming an average load current of I_{load}, and neglecting power converter and control losses, the time the ultracapacitor can power the load for is given by

$$t_{\mathrm{load}} = C \cdot \frac{(v_{\mathrm{init}} - v_{\mathrm{final}})}{I_{\mathrm{load}}}. \tag{3.4}$$

From Eq. 3.4, it is clear that t_{load} suffers significantly from the reduced dynamic range afforded by a static ultracapacitor bank. The meager operating time of the architecture in Fig. 3-4 drives the need for a larger bank. Alternatively, this motivates the design of higher energy density ultracapacitors or circuit solutions that maximize the amount of stored energy on the ultracapacitor(s). Finally, it is worthwhile to note that batteries too

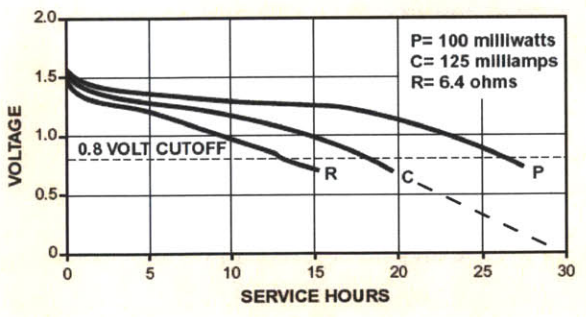


Figure 3-6: Duracell alkaline-manganese dioxide battery typical voltage profile under different modes of discharge. (R - constant resistance, C - constant current, P - constant power)

leave a substantial amount of energy unused. Fig. 3-6 shows the discharge characteristic for

a Duracell battery. Extrapolating from the constant current curve, one can see that nearly half of the energy goes unused due to the quick drop in voltage after a certain service period. This is a major advantage of shifting to reconfigurable capacitor banks.

3.1.2 Stacking Discipline Considerations

The implications of the stacking discipline implemented for maximum energy utilization is important and application-driven [6]. Table 3.1 tabulates the key tradeoffs encountered for various stacking discipline options. It can be seen that increasing the resolution and number of stacking steps increases energy utilization; however, this introduces more complexity (i.e., larger number of switches). For example, going from an 4-2-1 topology to a 8-4-2-1 topology increases the energy utilization from 98.44% to 99.61%. The corresponding increase in number of switches, however, more than doubles. The increased energy utilization may not be worthwhile unless it offsets the accompanying power consumption due to the increased complexity.

Table 3.1: Comparison of stacking discipline topologies [6]

Topology	**Number of switches**	**% Energy Utilization**	**Voltage variation**	**Number of leg capacitors**
2-1	3	93.75	1/2	1
4-2-1	9	98.44	1/2	1
8-4-2-1	21	99.61	1/2	1
3-2	5	80.25	1/3	2
4-3-2	12	88.89	1/3	3
6-4-3-2	22	95.06	1/3	2
4-3	7	68.36	1/4	3
5-4-3	16	79.75	1/4	12
6-5-4-3	27	85.94	1/4	10
8-6-5-4-3	41	92.09	1/4	15

Another important consideration is the voltage variation at the output of the capacitor array. This consideration influences the design of the subsequent power converter stage. The observation here is that for the same number of stacking steps, increasing the number of legs reduces the voltage variation at the expense of reduced energy utilization. For example,

consider the 4-2-1 and 4-3-2 topologies where both have two stacking steps. The 4-3-2 topology has a lower voltage variation of 33% compared to 50% in the 4-2-1 topology. However, the energy utilization of the 4-3-2 topology is 88.89% compared with 98.44% of the 4-2-1 topology. In general, complexity and area provides tighter voltage regulation and energy utilization.

3.2 Feasibility Analysis of Stacking Capacitors

Section 3.1.2 showed that energy utilization, voltage variation, and complexity are tightly coupled. We saw it possible to achieve upwards of 98% energy utilization with four capacitor legs and a moderate number of switches. An ideal energy management system consists of a series connection of a high energy utilization block as well as a high efficiency power converter. What is needed following a high energy utilization block is a way to process energy efficiently so as to present a steady voltage to load electronics. In other words, can voltage variation and energy utilization be isolated? As a sanity check, we can determine the minimum efficiency needed from the lossless converter to make stacking of an ultracapacitor array worthwhile.

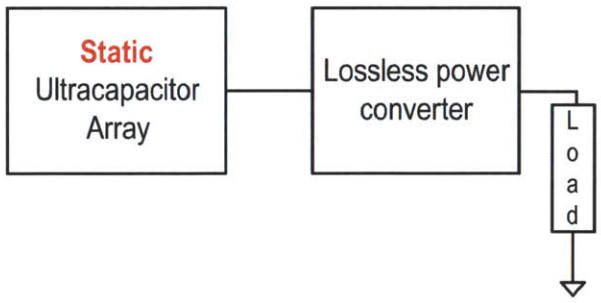


Figure 3-7: An energy utilization scheme using a static ultracapacitor array that achieves a maximum total efficiency of 75% ($v_{\text{final}} = 0.5v_{\text{init}}$).

Beginning with the static ultracapacitor setup shown in Fig. 3-7, we assume 100% power efficiency of the power converter with an initial voltage that is half the final voltage. In this case, 75% of the energy remains when the final voltage is reached. Therefore, this setup can

achieve a theoretical efficiency of 75%.

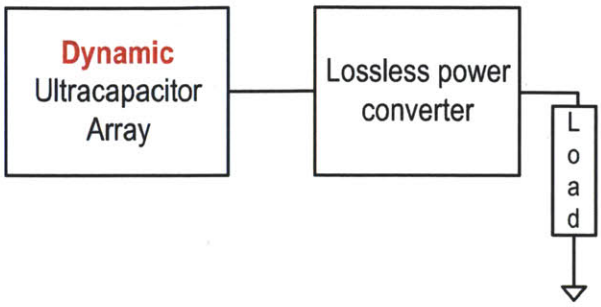


Figure 3-8: An energy utilization scheme using a dynamic ultracapacitor array that achieves a maximum total efficiency of 98% ($v_{\text{final}} = 0.5v_{\text{init}}$).

In the dynamic, or stacking, ultracapacitor case, it is possible to utilize 98% of the energy stored in the array. With a 100% efficient power converter this yields a theoretical total efficiency of 98%. Now, with the static ultracapacitor setup as a baseline, the relationship to the minimum efficiency required of the DC-DC power converter in the dynamic setup is given by

$$\textbf{Energy utilization efficiency} \times \min \textbf{(Average Efficiency of power converter)} > 75\%$$

Thus, for example, in order for the 4-2-1 topology of Table 3.1 with 98% energy utilization to be worthwhile, the minimum average efficiency of the DC-DC power converter is 76.5%.

3.3 System Architecture

The architecture for the energy management IC that implements the reconfigurable ultracapacitor bank and power converter is shown in Fig. 3-9. The general operation of the EMIC is illustrated in Fig. 3-10. During normal operation, the S.C. converters step down the ultracapacitor bank and reference voltages to α_1 and α_2, respectively. When discharging, once α_1 falls below the stepped down reference, α_2, the comparator trips and the digital logic reconfigures the switch matrix. A similar procedure follows during charging, in which case the

comparator trips once $\alpha_1 > \alpha_2$ resulting in unstacking. A 4-stage synchronous rectifier [4] is connected to the ultracapacitor bank during wireless recharging in the 900 MHz band. The circuit implementation of the various blocks are presented in the following sub-sections.

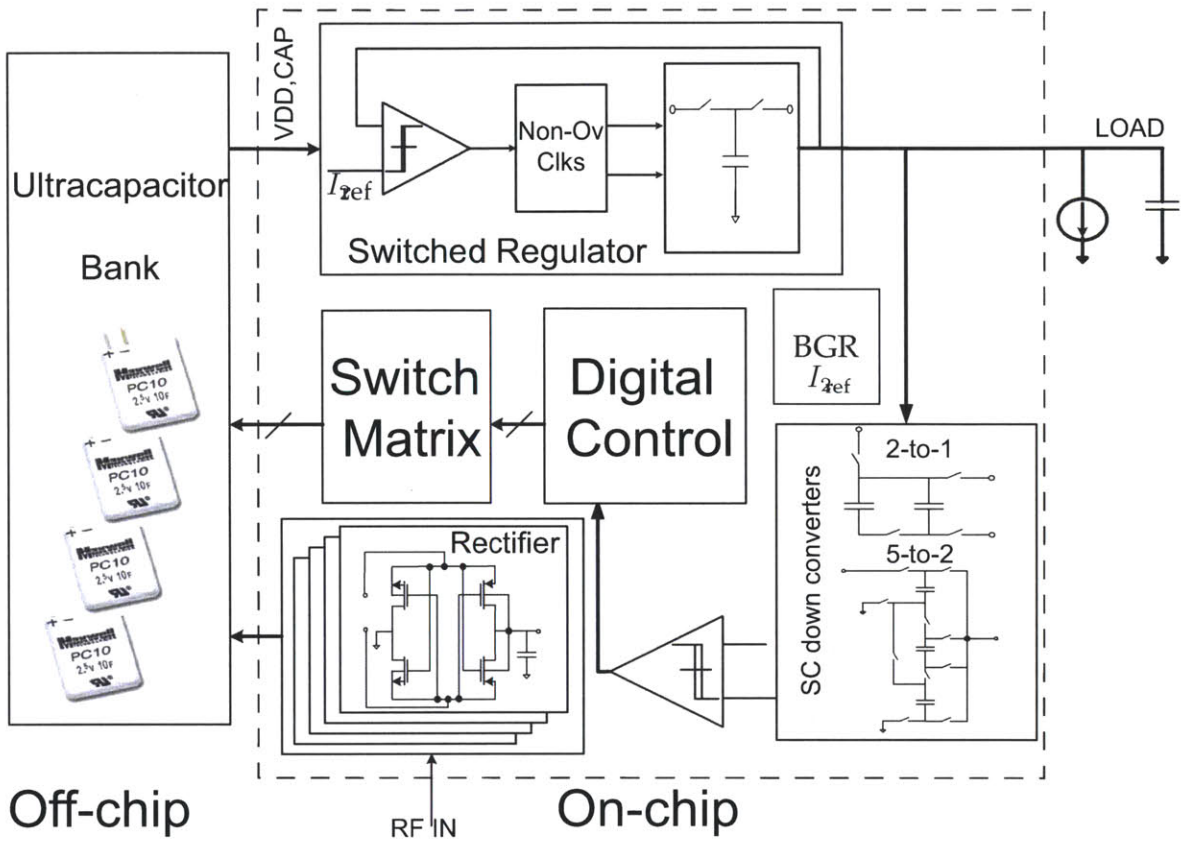


Figure 3-9: Energy management chip architecture that implements a reconfigurable ultracapacitor bank to demonstrate improved energy utilization.

The load is driven by the output of a 1.5-MHz switched-capacitor regulator whose level is controlled by a 1-V reference voltage generated by the bandgap reference (BGR). In a circuit environment such as this where the supply voltage varies significantly (the supply voltage here is the output of the ultracapacitor array), the BGR provides a stable reference useful for controlling the switch matrix of the reconfigurable capacitor bank. Since the BGR is the only static power draw in the entire architecture, we exploit the fact that the reference is only needed to drive transistor gates to allow us to operate the BGR at <4 nW for the

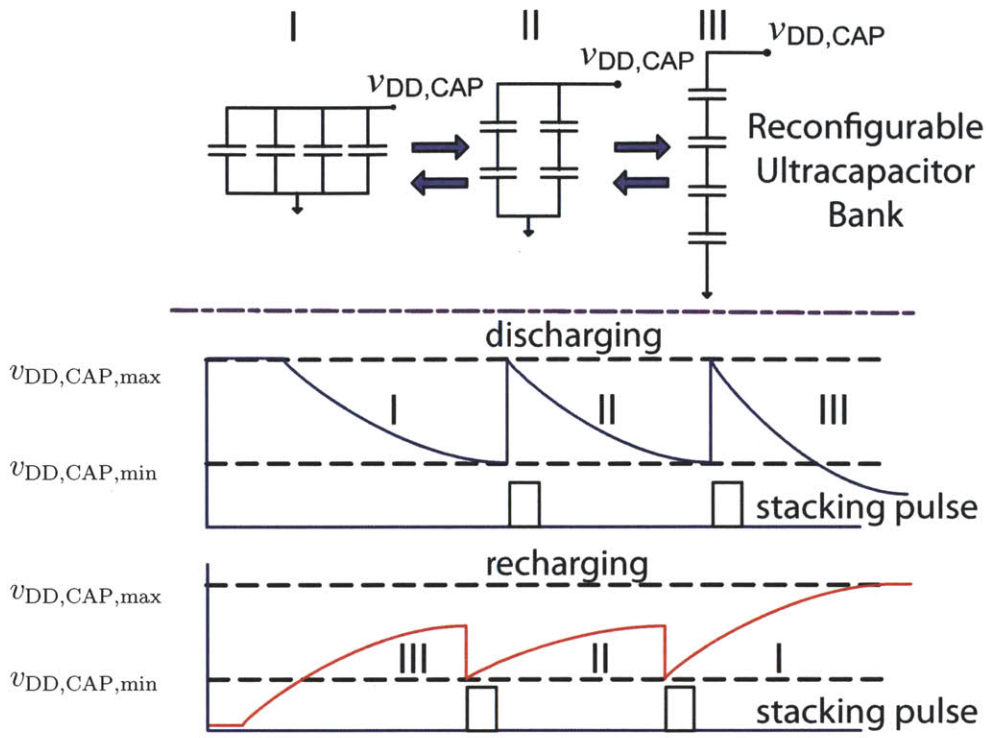


Figure 3-10: Operation of the energy management chip using stacking of capacitors to maximize utilization of the stored energy. For the energy management chip of Fig. 3-9, the thresholds $v_{DD,CAP,max}$ and $v_{DD,CAP,min}$ are 2.5 V and 1.25 V, respectively. The discharging and charging sequences are shown on the bottom figures. When the lower threshold, $v_{DD,CAP,max}$, is reached during discharging, the capacitors stack. Similarly, during charging a threshold is set between $v_{DD,CAP,max}$ and $v_{DD,CAP,min}$ to trigger unstacking.

highest ultracapacitor voltage of 2.5 V [2].

Referring to Fig. 3-10, assuming all the ultracapacitors are equal in size and with $v_{DD,CAP,max} = 2v_{DD,CAP,min}$, our stacking strategy results in utilization of 98.4% of the total energy initially stored on the ultracapacitors. In this stacking discipline, moving from one configuration to the other either halves or doubles the number of parallel branches, and is conveniently implemented when the total number of capacitors is a power of two. If this

[2]The ultracapacitors that we used (the Maxwell Technologies PC5 series) are rated for 2.5 V.

convention is followed, we may re-write from before the energy utilization that results as

$$\eta_{\mathrm{UC}} = \frac{E_{\mathrm{delivered}}}{E_0} = 1 - \frac{1}{2^{2(N-1)}} \cdot \left(1 - \frac{v_{\mathrm{DD,CAP,min}}}{v_{\mathrm{DD,CAP,max}}}\right)^2 \tag{3.5}$$

where N is the number of distinct stacking configurations and E_0 is the total stored energy. In practice, $v_{\mathrm{DD,CAP,max}}$ is set by dielectric breakdown in the ultracapacitors, and $v_{\mathrm{DD,CAP,min}}$ is set by the minimum input voltage of the S.C. regulator.

3.3.1 Circuit Implementation

Rectifier

The rectifier in Fig. 3-9 consists of a four-stage cascade of a four-transistor synchronous rectifier cell. Synchronous rectifiers are more efficient than their diode-based counterparts. Fig. 3-11 is a schematic the basic unit cell. Fig. 3-12 illustrates the basic operation of

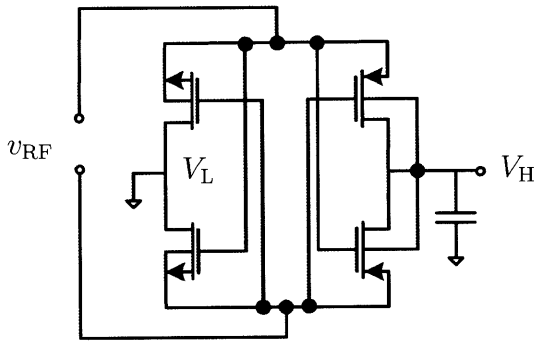
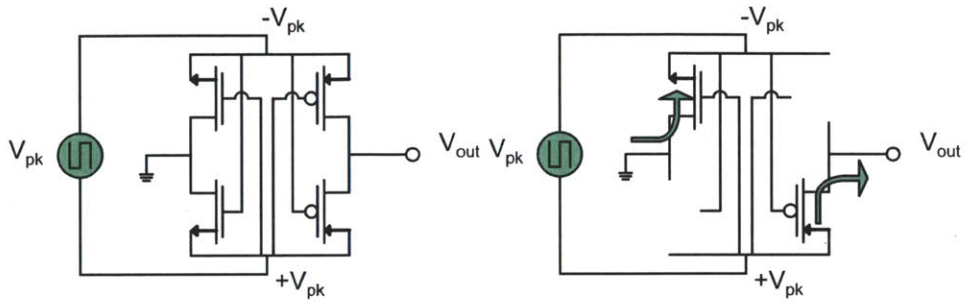


Figure 3-11: 4-transistor unit cell for synchronous rectifier topology. With a large enough input, the transistors operate as switches and only one pair of opposite devices conduct at a time.

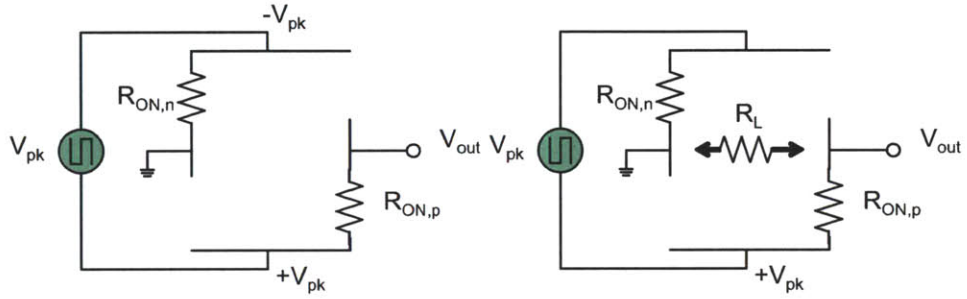
a unit cell with v_{RF} assumed to be a square-wave input. With a large enough input, the transistors operate as switches and only one pair of opposite devices conduct at a time. The key to achieving rectification is that current flows in the same direction during both half cycles, thus a DC voltage develops across a load connected between V_{H} and V_{L}. In general, $V_{\mathrm{out}} = (V_{\mathrm{H}} - V_{\mathrm{L}}) = (2v_{\mathrm{RF}} - V_{\mathrm{drop}})$. The quantity V_{drop} represents losses due to

switch resistance and reverse conduction. V_{drop} increases as the load current increases and v_{RF} decreases. The behavior with a sinusoidal input is similar, but the efficiency will be lower (i.e., output resistance will be higher) since the devices only turn on for part of the input cycle.



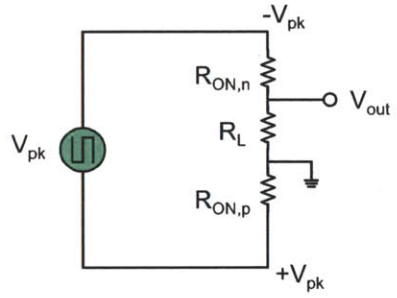
(a) Rectifier unit cell with large square-wave input.

(b) For each half cycle, only two conducting devices are turned on.



(c) Each device can be replaced by its on resistance, R_{on}.

(d) The current flows in the same direction through the load during both half cycles.



(e) The DC voltage can be expressed as $V_{\text{out,pk}} = 2V_{\text{pk}} \frac{R_{\text{L}}}{R_{\text{on,n}}+R_{\text{L}}+R_{\text{on,p}}}$.

Figure 3-12: Basic operation of rectifier unit cell.

In order to increase the DC voltage obtained at the output of the rectifier, we may cascade

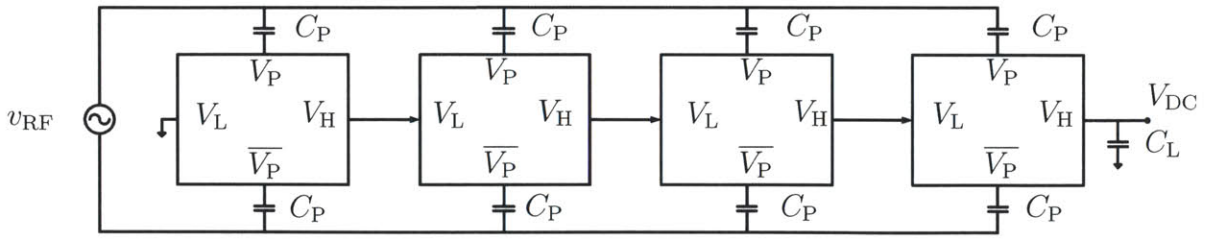


Figure 3-13: Cascading rectifier cells in order to increase the DC voltage obtained at the output of the rectifier. The circuit behaves as a charge pump voltage doubler. In practical implementations, body bias effects reduce increases in the output voltage.

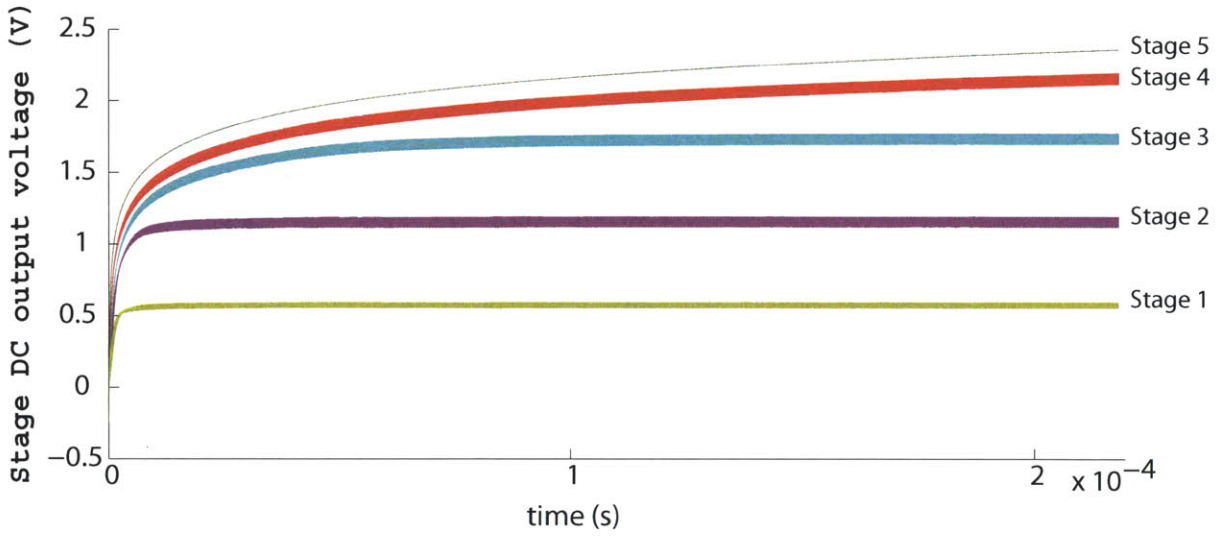


Figure 3-14: Simulation for $N = 5$ rectifier stages with $I_L = 100$ nA, $C_L = 1$pF, $P_{in} = 0$ dBm, and $v_{out,max} = 2.3$ V. The degradation due to body bias effects with each added stage is evident and increases in the output voltage are limited.

N cells in series as shown in Fig. 3-13. Thus the circuit behaves as a charge pump voltage doubler. Fig. 3-14 simulates a rectifier cascade with $N = 5$. For N stages, we expect the output DC voltage to be $V_{out} = N \cdot (2v_{RF} - V_{drop})$; however, in practical implementations, V_{out} is generally found to be lower. This is because V_{drop} is not constant and increases with subsequent cells due to body bias effects.

Dynamic Comparator

As seen in Fig. 3-9, the comparator's function is to provide coarse comparison (1-bit ADC) of the voltage levels at the output of the ultracapacitor bank and at load voltage. The topology of Fig. 3-15 works well for signal differences that are tens of millivolts. The outputs change on the rising edge of the clock signal. It should be noted that if the inputs become too large, the input devices move deep into triode operation. When this occurs, the small differences in their channel resistances adversely affect the quality of the comparator's decisions, resulting in comparison resolutions on the order of 100-200 mV. For the purposes of the EMIC, if we assume the energy consumption from the ultracapacitor bank is low enough, this is not a major concern since under normal operation comparisons happen infrequently. If the

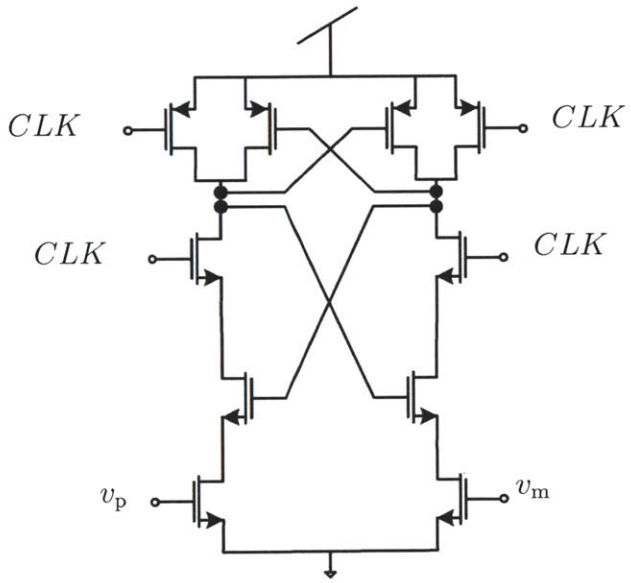


Figure 3-15: Clocked comparator used to provide coarse comparison of the voltage levels at the output of the ultracapacitor bank and the load voltage in order to determine when to stack/unstack.

comparison resolution is intolerable for a particular application, the topology in Fig. 3-16 may be used instead. The differential amplifiers function as pre-amplifiers and remove the need for the triode-susceptible input devices. Now, instead of steering voltage differences, the circuit steers currents from one side of the cross-coupled latch to the other. Fig. 3-17 shows

the operation of the comparator of Fig. 3-15. For high inputs the comparator demonstrates proper operation; however, as the inputs near the threshold voltage of the input transistors, the comparison decisions become inaccurate.

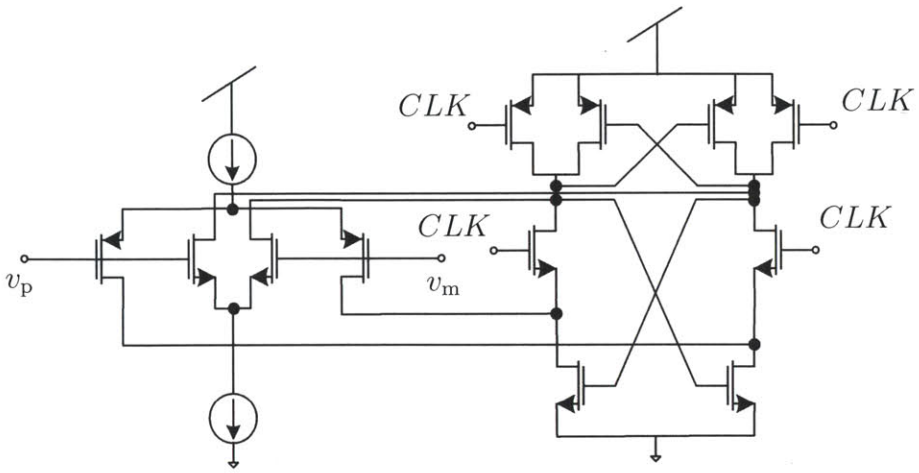


Figure 3-16: Improved wide-swing clocked current-mode comparator that provides finer resolution comparisons by using a pre-amplifier stage.

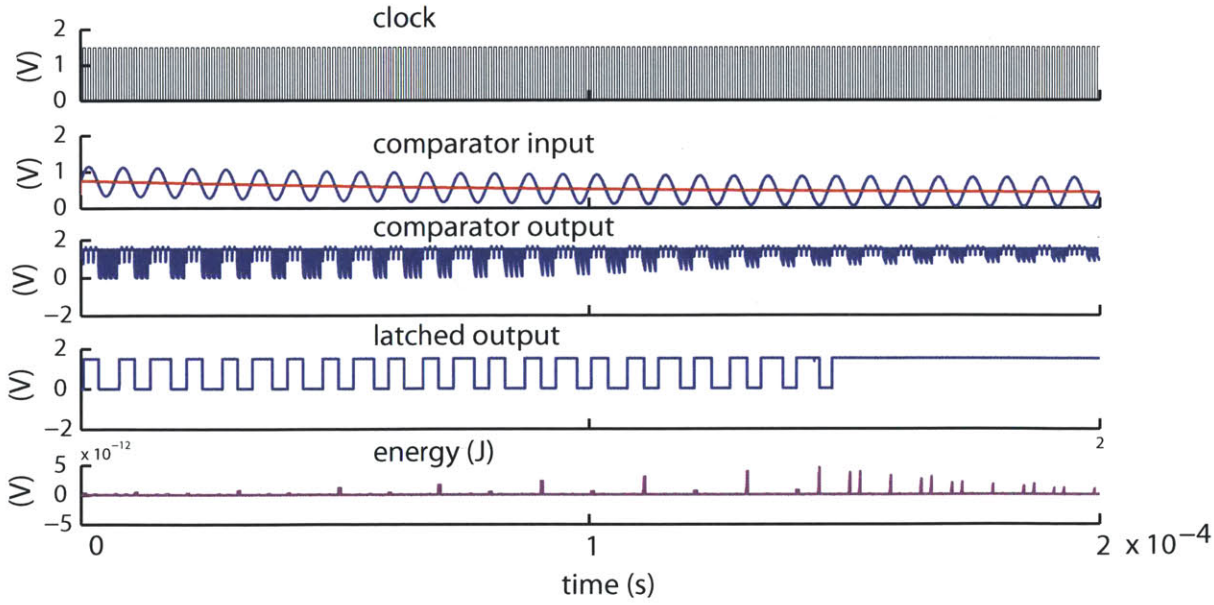


Figure 3-17: Simulation of dynamic comparator of Fig. 3-15.

Ultra-low Power Bandgap Reference

In an environment where the power supply can vary significantly, a bandgap reference (BGR) circuit provides a stable reference. This reference is useful for controlling the switch matrix of the reconfigurable capacitor bank and deriving a known voltage for supplying the load. The BGR v_{ref} generator must create a well-regulated supply voltage for any variations of voltage, process, and temperature, because other circuitry operate based on the reference voltage. Threshold-voltage V_{th}-referenced generators, and BGR generators are common. The V_{th}-referenced generators are easy to design but the output voltage has a large temperature coefficient and suffers from process fluctuation. Since the threshold-voltage of MOS transistors has a negative temperature coefficient around -2 mV/°C, the V_{th} shift is as large as 40 mV in a junction-temperature range from 20°C to 40°C. For many applications it is necessary to combine V_{th} with complementary circuitry to provide compensating (positive) temperature coefficient. The BGR utilizes the base-emitter voltages, V_{BE}, of a bipolar transistor (forward voltages of diodes). It features a small dependency on temperature or process fluctuation. Parasitic bipolar transistors fabricated with CMOS process, instead of a bipolar process, are usually used for process compatibility.

Fig. 3-18 shows the circuit implementation for a nano-power BGR using diode-connected NMOS devices to act as large resistors [53]. The cascode mirror devices ($M_5 - M_8$) keep the currents in Q_1 and Q_2 identical. The mirrored current in Q_3 is scaled-up increasing the channel width of M_{10} and M_{11} in order to minimize the effects of recombination-generation in the space charge regions. The PTAT current, i_1, is generated by the difference in emitter areas between Q_1 and Q_2, resulting in ΔV_{BE}. The ΔV_{BE} created counteracts the CTAT characteristic of Q_3's base-emitter voltage. The diode-connected MOS resistors, RM_1 and RM_2, serve to reduce the static power draw but also introduce a temperature dependence. Implementing the resistors with active elements introduces a deviation from the typical V_{BE} (CTAT) and ΔV_{BE} (PTAT) characteristics, shown in Fig. 3-19. This is because the NMOS devices, operating in the weak inversion regime introduce additional strong temperature dependence via their drain current, I_{D}.

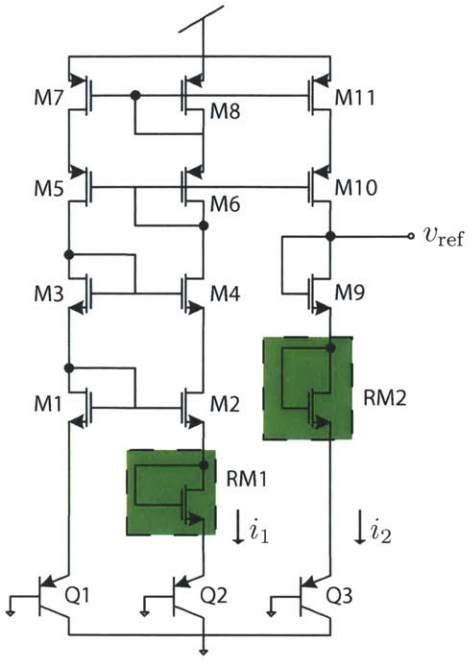


Figure 3-18: Bandgap reference circuit implementation. The highlighted devices act as large resistors that limit the quiescent power consumption.

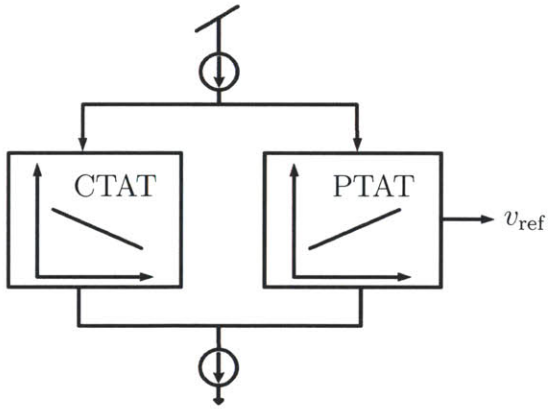


Figure 3-19: General bandgap reference block diagram. Ideally, the combination of CTAT and PTAT blocks are combined to generate a reference with zero temperature coefficient.

The strong temperature dependence poses trade-off challenges between the temperature coefficient, the PSRR, output resistance, and power consumption of the topology in Fig. 3-18. The devices in Fig. 3-18 are sized to minimize the degradation in the temperature

coefficient introduced by the additional NMOS devices. Fig. 3-20 shows the response of v_{ref} to sweeping v_{DD}. We observe that v_{ref} does not settle until v_{DD} exceeds $\approx$ 1.1 V. This is because since v_{ref} is inevitably close to the Si-bandgap voltage ($\approx$ 1.1 V at room temperature), therefore v_{DD} must be higher than 1.1 V for steady-state. Fig. 3-21 shows the start-up transient behavior of the BGR with a 1 pF load capacitance. Finally, Fig. 3-22 shows the temperature-dependence of v_{ref}. For the range of interest for most medical applications (20-40°C), the supply varies by 27 mV. Higher precision can be obtained at the expense of complexity and power [54].

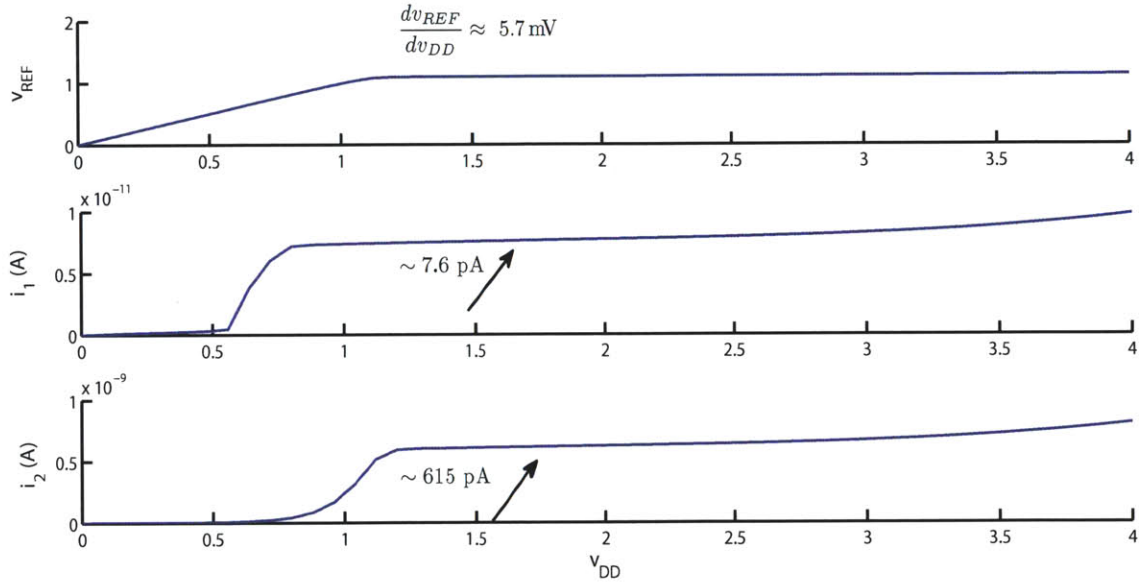


Figure 3-20: DC sweep of v_{DD} for ultra-low power bandgap reference. v_{ref} settles with $v_{\text{DD}} >$ 1.1 V. The power consumption is less than 4 nW at the highest v_{DD} level.

For further power reductions we may introduce power gating as shown in Fig. 3-23. By duty cycling the BGR in this way, the savings are proportional to the period of the power gating clock. Moreover, as discussed in Section 3.3.1, the BGR is only used to provide a reference input to a dynamic comparator, duty cycling is determined by the frequency of comparisons.

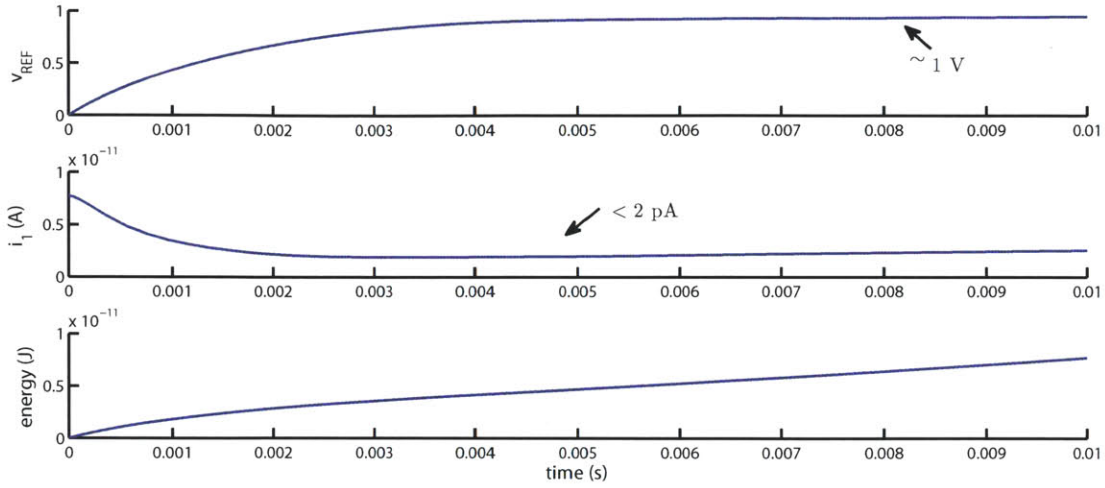


Figure 3-21: Bandgap reference transient simulation with $C_{\mathrm{L}} = 1$ pF illustrating the time for v_{ref} to settle.

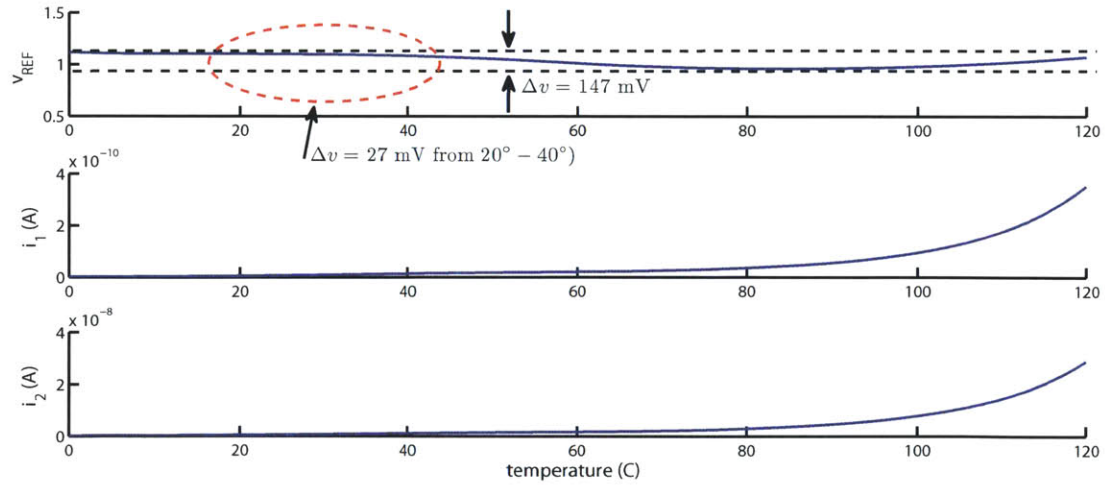


Figure 3-22: Bandgap reference temperature sweep. Over the temperature range of interest for in-body/near-body applications (20-40°C) the references varies less than $\Delta v = 27$ mV.

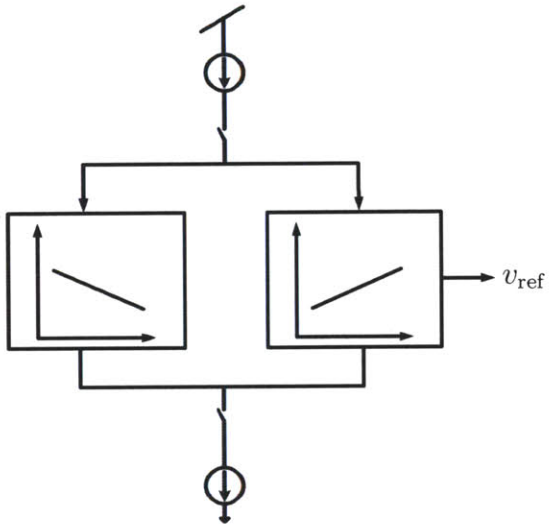
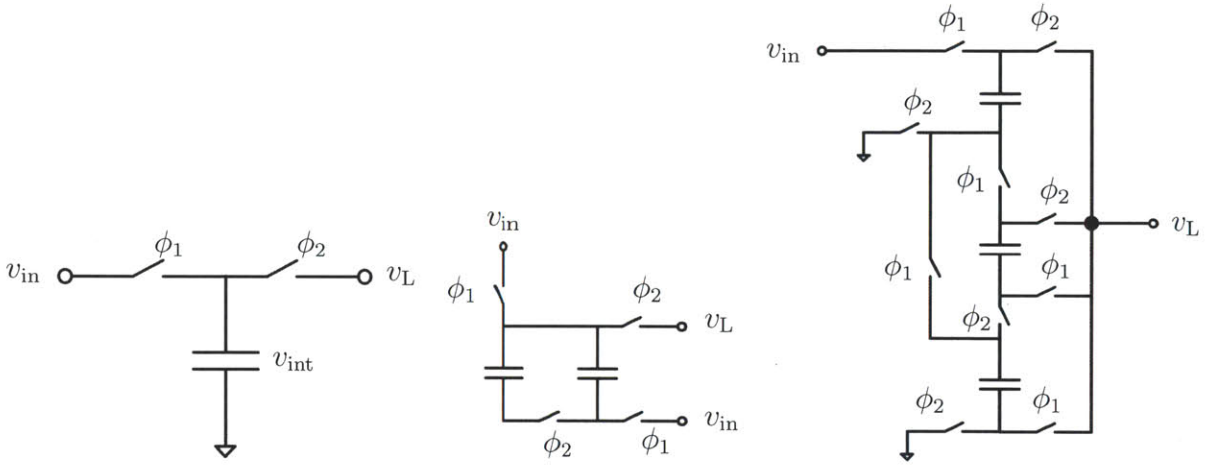


Figure 3-23: Block diagram illustrating how to duty cycle the BGR in Fig. 3-19 in order to further reduce the power consumption.

Switched-Capacitor DC-DC Converters

The switched capacitor converter circuits used in the switched regulator and at the input of the comparator are shown in Fig. 3-24. Switched capacitor converters offer improved efficiencies as compared to linear regulators [55]. Moreover, using integrated capacitors circumvents the need for large on-chip inductors, thus saves in area.



(a) 1:1 switched-capacitor converter used in switched regulator to maintain $v_L = v_{ref}$.

(b) 2:1 switched-capacitor converter used to compare the ultracapacitor voltage with $\frac{1}{2}v_L$ to determine when to stack/unstack.

(c) 5:2 switched-capacitor converter used to step down the ultracapacitor voltage for comparison against v_L to determine when to stack/unstack.

Figure 3-24: Switched-capacitor converters used in the EMIC test chip.

Fig. 3-25 is a block diagram implementing the switched regulator shown in Fig. 3-9. Fig. 3-26 show simulation results with $v_{ref} = 1$ V and $v_{uc} = 2$ V. The output load voltage is compared to the bandgap reference voltage. When the output voltage drops below v_{ref} the comparator trips and generates 50% duty-cycled, non-overlapping clock signals that drive the 1:1 switched-capacitor converter. Fig. 3-27 is the circuit implementation of the non-overlapping clock block.

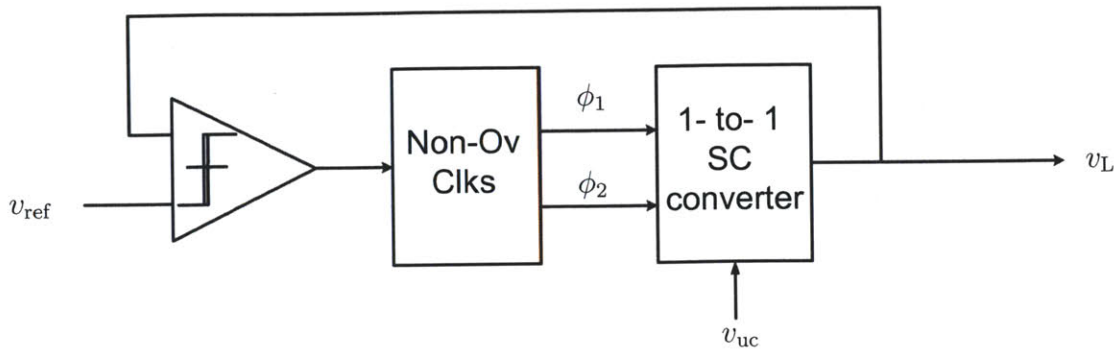


Figure 3-25: Switched regulator implementation using negative feedback to regulate output voltage. The output load voltage is compared to the bandgap reference voltage. When the output voltage drops below v_{ref} the comparator trips and generates 50% duty-cycled, non-overlapping clock signals that drive the 1:1 switched-capacitor converter.

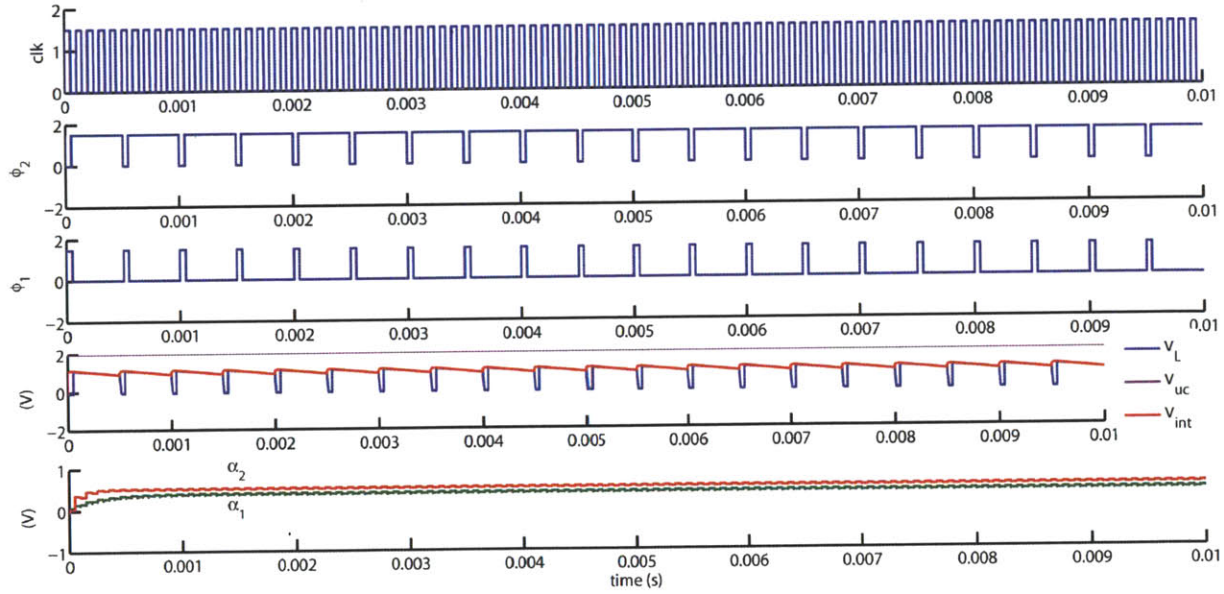


Figure 3-26: Simulation of switched regulator and S.C. converters of Fig. 3-24. α_1 and α_2 are the outputs of the 5:2 and 2:1 S.C. converters of Fig. 3-24, respectively.

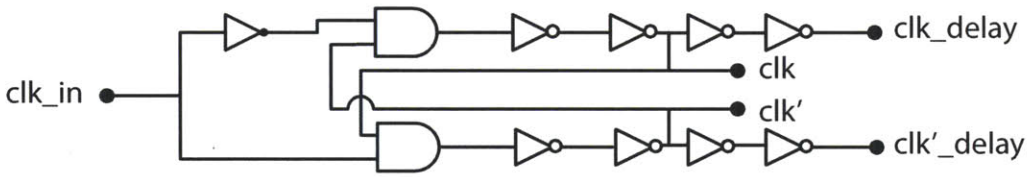


Figure 3-27: Non-overlapping circuit implementation used to generate the non-overlapping signals to drive the switches of the 1:1 switched-capacitor converter in the switched regulator of Fig. 3-25.

Digital Control

In order to provide the control signals for the switch matrix while minimizing power overhead, a digital state machine can be implemented. Fig. 3-28 shows a block diagram of the state machine to control the switch matrix. Asserting $\overline{\mathbf{clr}}$ low serves as a reset signal and configures the capacitor bank into an all-parallel configuration. The signal clk, fsm pulses to indicate when to stack/unstack by keeping track of the current state of the ultracapacitor bank switches as well monitoring the voltage level of the ultracapacitor bank.

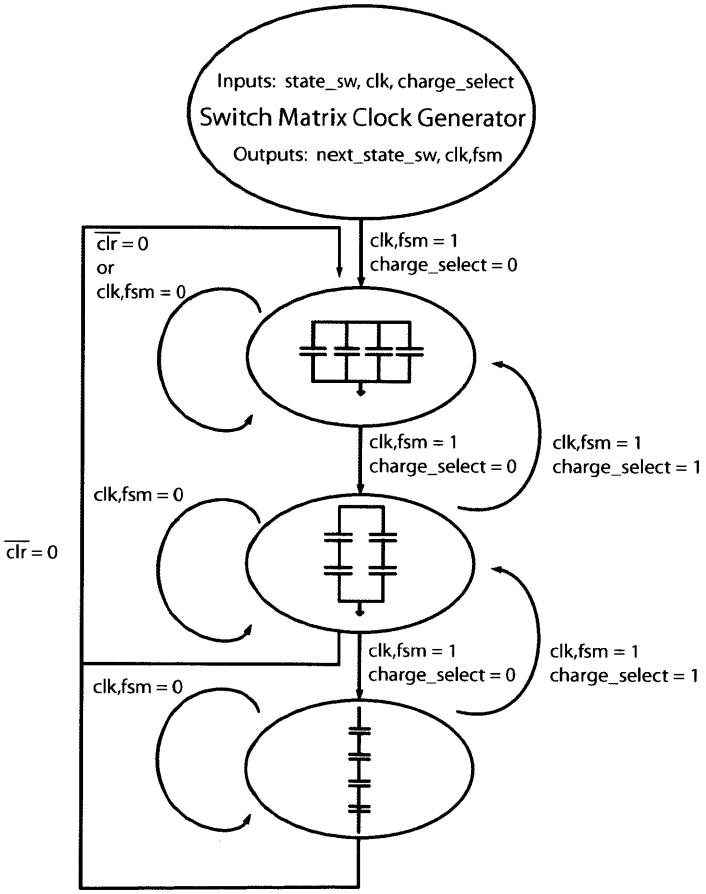
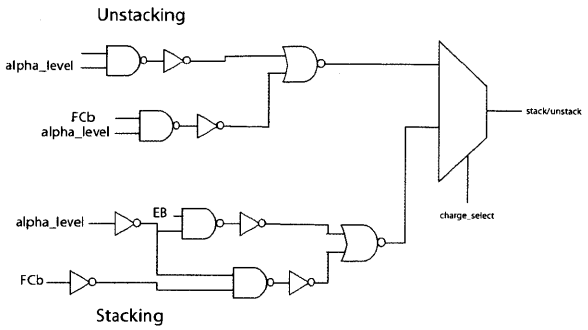


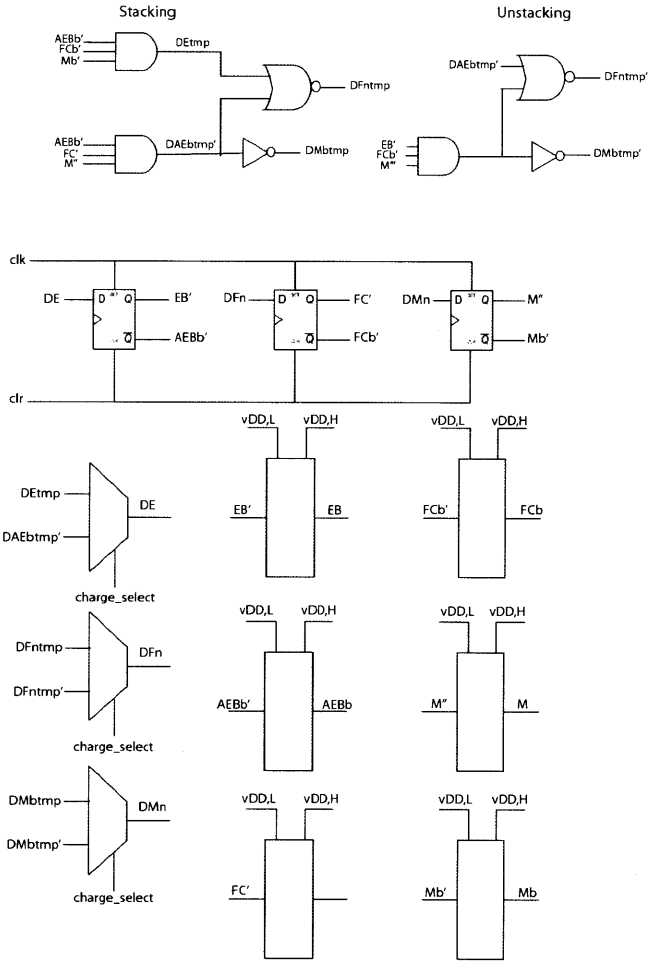
Figure 3-28: Block diagram of finite state machine to control switch matrix.

The state machine is implemented using the custom logic shown in Fig. 3-29. The logic used for stacking/unstacking are shown and the signal **charge_select** drives a multiplexer that selects the operating mode. Level-shifters are used to raise the voltage level to drive

ultracapacitor switches and switched-capacitor converter switches. To reduce the $C \cdot V^2$ energy, the digital logic operates on a lower supply, ($v_{\mathrm{DD,L}}$) derived from the ultracapacitor bank and the 2:1 switched-capacitor converter. Fig. 3-30 shows the simulated behavior of the digital control of the EMIC. The operation begins with **charge_select** asserting low. Following the FSM clock signal, it can be seen that two transitions occur as indicated by the state_1-EB and state_2-FCb signals. When **charge_select** asserts high, the unstacking sequence occurs. This is indicated by the two transitions in each of the corresponding digital signals.



(a) Custom logic to generate the state machine clock signal for stacking/unstacking (**clk, fsm**). The signal **charge_select** selects the operating mode.



(b) State machine logic that keeps track of the ultracapacitor bank switch configuration. The logic is run on a lower supply voltage, $v_{\mathrm{DD,L}}$, in order to minimize dissipation. The level-shifters provide the drive to the ultracapacitor switches.

Figure 3-29: Custom logic that implements the state machine to control stacking/unstacking of the ultracapacitor bank.

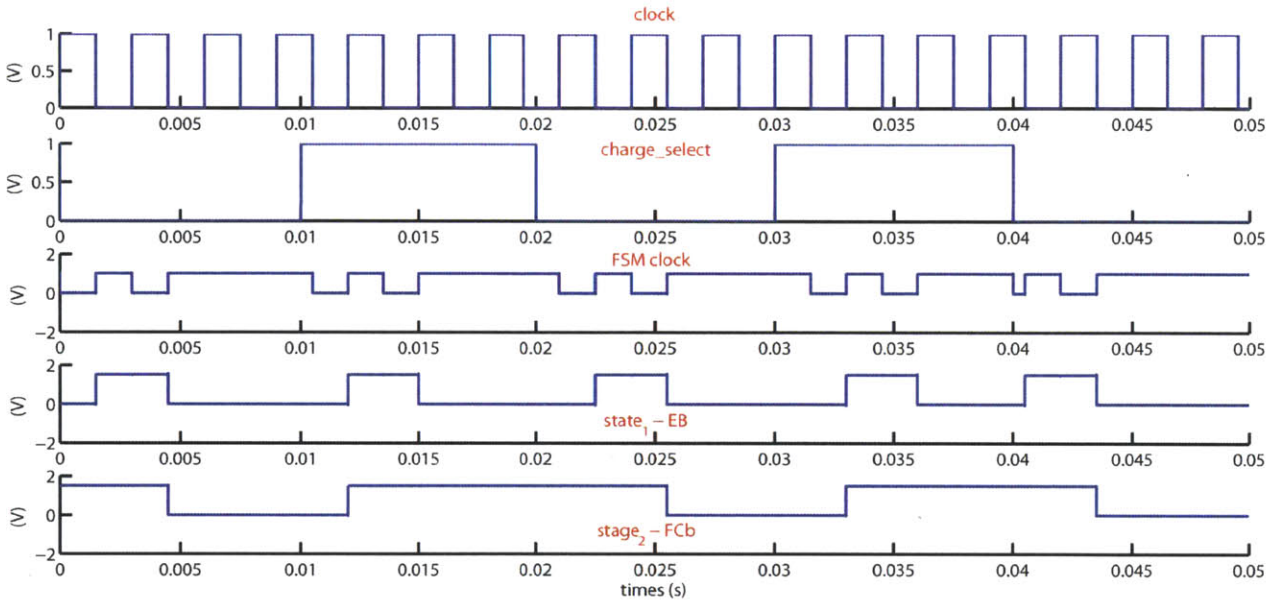


Figure 3-30: Operation of energy management chip and switch matrix state machine control. The state machine clock triggers configuration changes of switch matrix depending on the voltage, v_{uc}, of the ultracapacitor bank, a reset signal ($\overline{\mathbf{clr}}$), and the **charge_select** signal.

3.4 Measurement Results

Conversion efficiency measurements are shown Fig. 3-31 as a function of output load power for measured versus simulated data for a clock frequency of 1.5 MHz. A peak efficiency of 51% was measured with a load of 63 μA at 1 V$\pm$10 mV. This efficiency is comparable to the 56% achieved in [56] for 100-250 nW loads, which was designed for battery-powered (e.g., lithium based thin-film) biomedical implant applications. However, the architecture does not lend itself to wide-ranging input voltages. As will be discussed in Chapter 4, the efficiency of the test chip presented here is limited by the linear regulator characteristic of the switched regulator from using a single conversion ratio switched-capacitor converter.

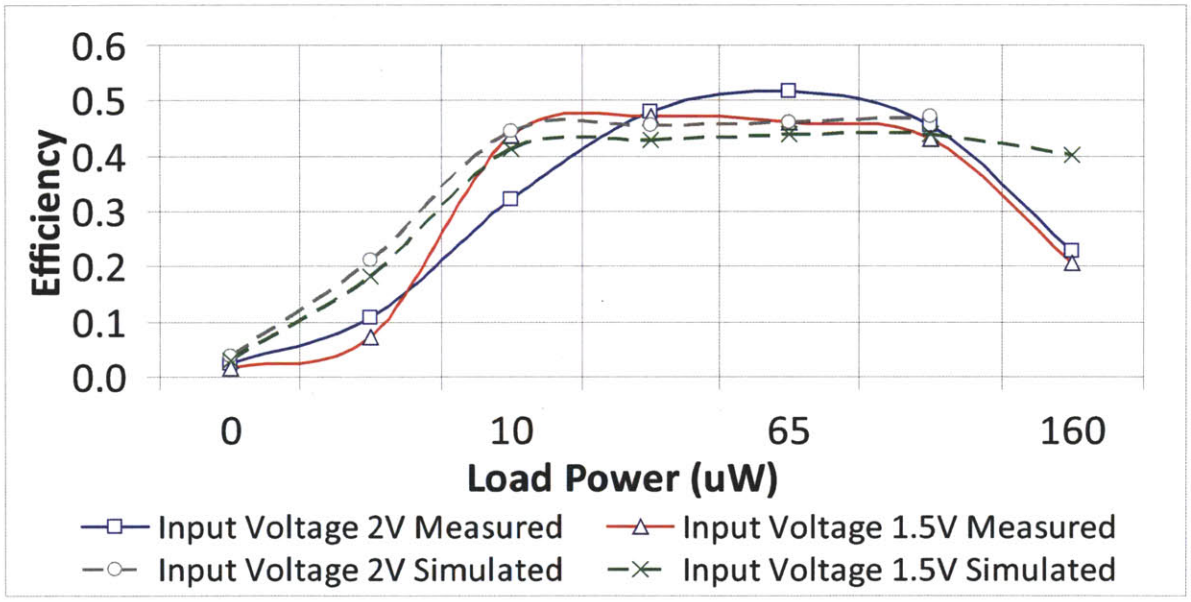


Figure 3-31: Conversion efficiency of measured versus simulation for $f_{\text{clk}} = 1.5$ MHz. A peak efficiency of 51% is measured.

Operation of the IC was confirmed using 5-F ultracapacitors from Maxwell Technologies. These capacitors have 0.18 Ω of series resistance, and 40 μA of leakage current. The voltage ripple at the output of the power converter depends on comparator clock rate as compared to the current draw and capacitance at the load. The higher the current demand and/or the smaller the capacitance, the higher the clock rate necessary for a given ripple. Fig. 3-32

illustrates this, where the clock has been greatly slowed to 50 kHz for illustration purposes. The current draw is 150-200 nA, and the capacitance is 200 pF±5%. Based on these numbers we expect a ripple on the order of 200 mV, which is what we observe from the measurements in Fig. 3-32.

The stacking and unstacking operations are shown in Fig. 3-33. Four 300-μF electrolytic capacitors are used for practical reasons and for purposes of illustration. Notice that the charging behavior starts successfully even when the ultracapacitor array is almost fully discharged (see Fig. 3-33 upper right). This is possible because the rectifier is connected directly to the output of the ultracapacitor array. Once the ultracapacitor output exceeds 1.2 V, the BGR and the switched regulator begin to function. The fabricated chip occupies a total area of 1.82 mm^2 (1.3 mm x 1.4 mm) with a 0.39 mm^2 active area. Fig. 3-34 shows the IC die photo.

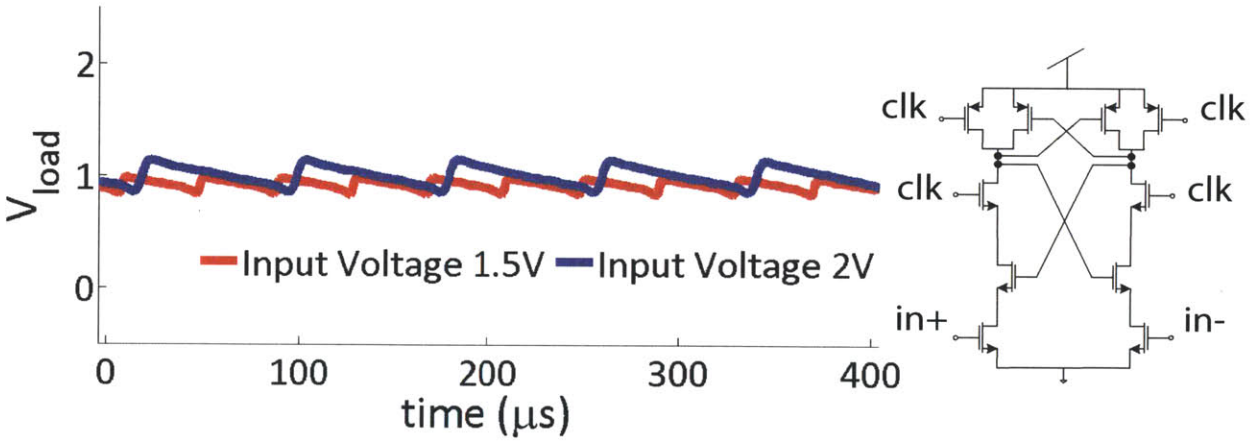


Figure 3-32: Illustrating the dependence of output ripple on clock frequency, current draw, and load capacitance on the power converter. The graphs show the load voltage output for 1.5 V and 2 V input. The topology for the comparator is shown on the right.

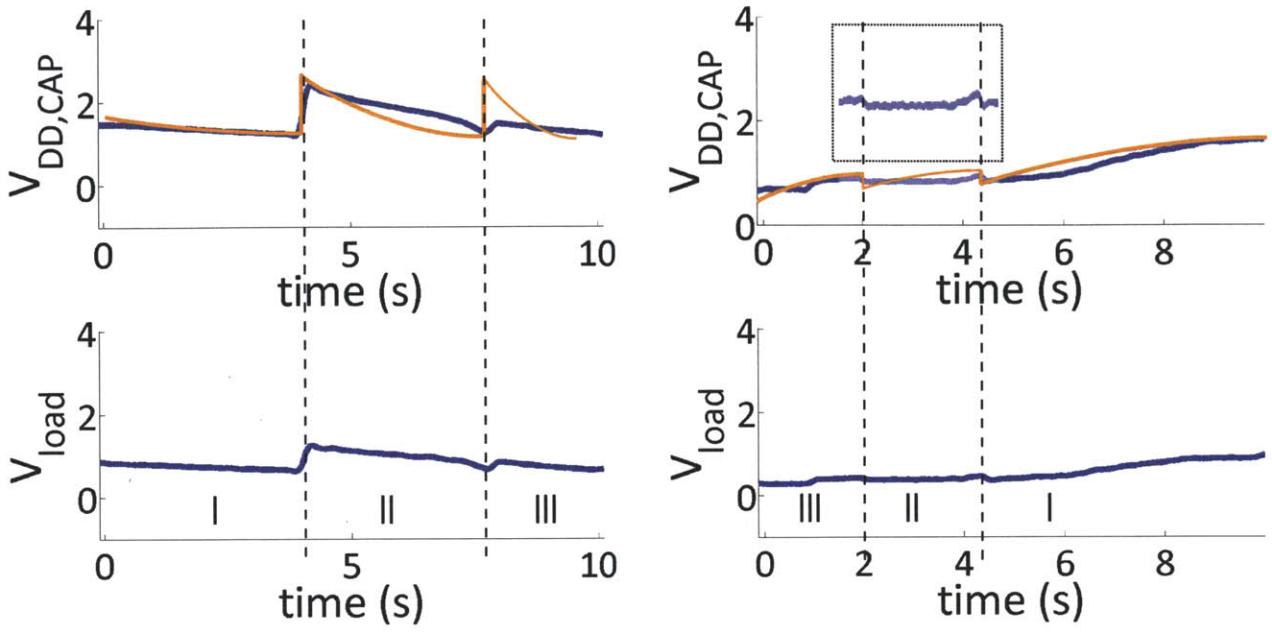


Figure 3-33: Stacking and unstacking operations during charging (right) and discharging (left). The yellow traces indicate simulated voltages. The top plots show the output of the ultracapacitor bank, the bottom plots show the regulated output (nominally 1 V).

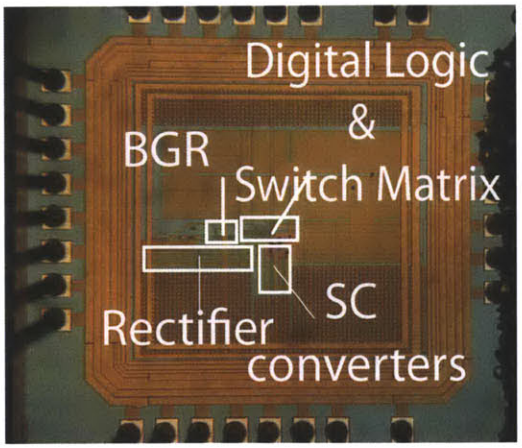


Figure 3-34: Die photograph of test chip in 180-nm, 5-V CMOS process.

3.5 Summary and Conclusions

This chapter presented an energy management integrated circuit (EMIC) to allow low-power systems, such as biomedical implants, to optimally use ultracapacitors instead of batteries as their chief energy storage elements. The chip, fabricated in a 180-nm CMOS process, consists of a switched-capacitor DC-DC converter, a 4-nW bandgap voltage reference, a high-efficiency rectifier to allow wireless recharging of the capacitor bank, a switch matrix, and digital control circuitry to govern the stacking and unstacking of the ultracapacitors. It is shown that the stacking procedure allows for more than 98% of the initial energy stored in the capacitors to be removed before the output voltage drops unsuitably low. The DC-DC converter implemented in this chapter is limited to a single conversion ratio and achieves a peak efficiency of 51%. For loads between 10 and 100 μW the chip operates for input voltages between 1.25 and 2.5 V. In the next chapter, techniques to increase the conversion efficiency of the switched-capacitor DC-DC converter stage are presented.

Chapter 4

Wide-input-range Switched-capacitor DC-DC Converters

This chapter discusses design considerations and techniques for wide-input-range energy management circuits and the implementation of a switched-capacitor converter with a peak efficiency of 90%. The fabricated IC allows low-power systems, such as biomedical implants, to optimally use ultracapacitors instead of batteries as their energy storage elements. Fabricated in a 180-nm CMOS process it consists of a switched-capacitor DC-DC converter with multiple conversion ratios, a switch matrix to control the configuration of an ultracapacitor array, and digital control to govern charging and discharging of the energy bank. A stacking procedure allows for more than 98% of the initial energy stored in the ultracapacitors to be removed before the output voltage drops unsuitably low for circuit operation. The DC-DC converter efficiency does not fall below 70% for loads between 20 and 250 μW and operates for input voltages between 1.25 and 3 V.

For bio-implantable devices that require the absolute smallest form factor, it is desirable to have on-chip energy storage capability. Recent advances in ultracapacitor research suggest that these devices may soon be suitable for on-chip implementation [27]. Indeed, ultracapacitors have several compelling advantages: a practically unlimited number of recharge cycles, extremely rapid charging, and a direct relationship between the terminal voltage and its

state of charge.

Ultracapacitors have one glaring drawback, which is that the terminal voltage drops off aggressively as the energy is drained ($V \sim \sqrt{E}$). This stands in unpleasant contrast to batteries, where the output voltage stays relatively steady over a useful range of the state of charge. To deal with the aggressive voltage droop of ultracapacitors, we introduced a stacking ultracapacitor bank concept in [47]. However, that implementation suffered an efficiency penalty by using a switched-capacitor (S.C.) voltage regulator with only a single conversion ratio. In this implementation, we introduce a better solution that preserves efficiency performance by using a multiple conversion ratio switched-capacitor voltage regulator. At any given input voltage from the ultracapcitor array, the switched-capacitor voltage regulator is configured to maximize efficiency [44].

4.1 System Architecture & Operation

Fig. 4-1 shows the architecture for the energy management IC. The load voltage, v_{L}, is compared to the output of a nano-power bandgap reference, v_{ref}. If v_{L} drops below the specified level, the comparator trips and generates 50% duty-cycled, non-overlapping clock signals ϕ_1 and ϕ_2. These signals are buffered through the tapered gate drivers in order to effectively drive the switches of the switched-capacitor converter.

In order to increase the efficiency, the conversion ratio of the switched-capacitor converter is selected such that the product of the conversion ratio and v_{uc} is as close to the desired v_{L} as possible. From there, burst-mode control is used to fine-tune the desired output voltage and reduce power consumption. A 5-bit SAR ADC digitizes v_{uc} and compares the digital word to pre-stored values in a look-up table (LUT) in order to select the most appropriate conversion ratio. The range of v_{uc} is kept below 2.5 V as a compromise between implementing the ultracapacitor bank switches using 5 V devices from a 180-nm process, and over-stressing the ultracapacitor dielectric material, which has a nominal 2.5 V breakdown voltage.

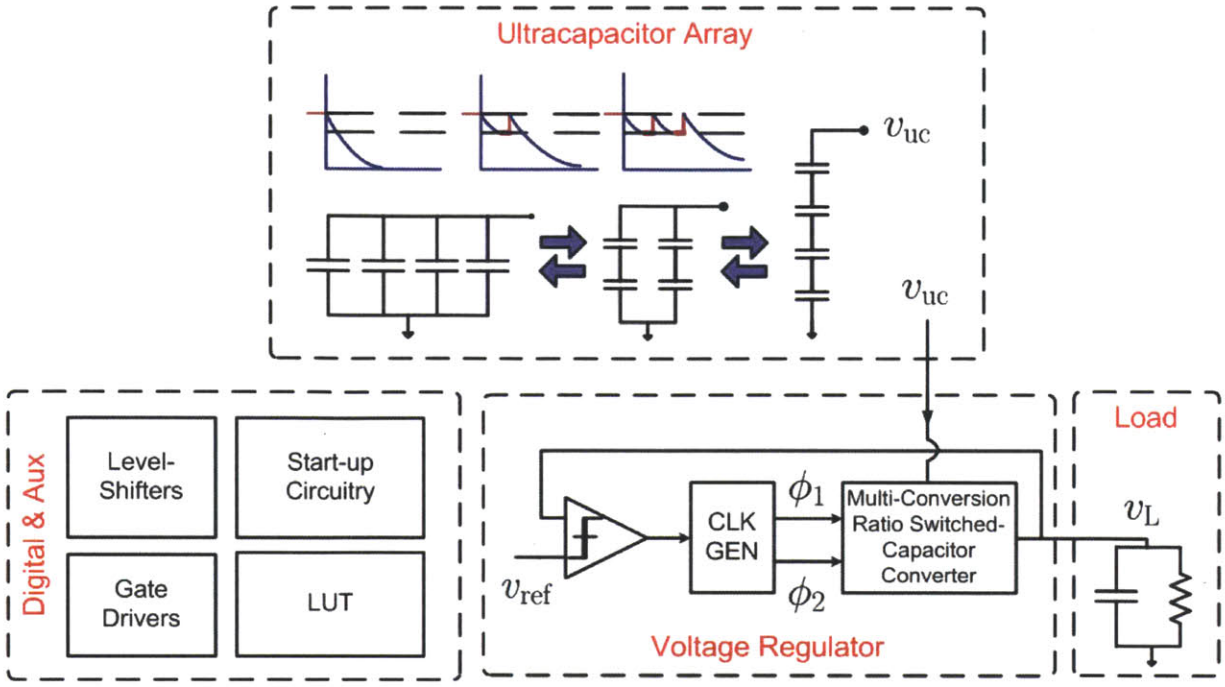


Figure 4-1: Architecture for energy management chip including a switched-capacitor converter capable of providing multiple conversion ratios. This helps improve the efficiency performance for wide-range input voltages.

4.1.1 Switched-Capacitor Converter Efficiency Considerations

By conservation of energy, the fundamental efficiency limit due to conduction losses is determined by the ratio of the loaded output voltage, v_{L}, and the ideal, no-load output voltage, v_{NL} This is discussed in Chapter 2 and Section 4.1.2. From a physical basis, S.C. converters are fundamentally current converters since they split up charges across capacitors by processing a current signal. Therefore, the efficiency of switched-capacitor converters is inversely related to the output regulation capability for a given conversion ratio.

S.C. converters are more challenging to implement than inductor-based converters because they have an ideal efficiency of 100% at only one conversion ratio. Different conversion ratios are possible using reconfigurable topology techniques [57], but the efficiency suffers according to $v_{\mathrm{L}}/v_{\mathrm{NL}}$, where v_{L} is the load voltage that is actively maintained, and v_{NL} is the output voltage at which the S.C. converter would be 100% efficient. Fig. 4-2 illustrates the

efficiency of a 1:1 S.C. converter whose output is actively maintained at 1 V. The efficiency is the highest for an input voltage of 1 V, and decreases monotonically as the input voltage increases. Section 4.1.2 provides more detailed efficiency analysis.

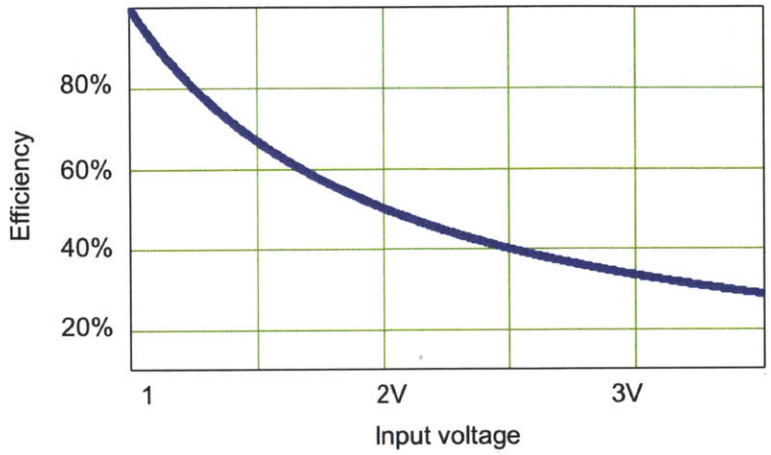


Figure 4-2: Efficiency verus input voltage for a 1:1 S.C. converter. The output voltage is assumed to be maintained at 1 V through some form of feedback control. The efficiency performance is analogous to a linear voltage regulator. High-efficiency is limited to a very limited range of input voltages.

4.1.2 Efficiency Analysis

Successful use of an ultracapacitor array is measured by how much of the energy from the array is actually delivered to the load circuit. As has been shown in [47], the stacking discipline employed results in 98% of the energy removed from the capacitor array. Between the capacitor array and the load circuit that consumes the energy, it is practical that there be a voltage regulator because most circuits consume constant current or, even worse, increase their current draw in response to an increase in the supply voltage. The result is a needless and wasteful increase in the rate of *energy* consumption. An ideal voltage regulator is the perfect solution: when v_{uc} increases, the current draw from the capacitor array decreases, keeping rate of energy consumption always constant.

The strategy of an ultracapacitor array followed by a voltage regulator can be undermined

if the voltage regulator has a low efficiency. This is a special concern when using S.C. regulators. For purposes of analysis, the best definition of efficiency for this system is

$$\eta_{\text{avg}} = \frac{E_{\text{delivered}}}{E_{\text{drawn}}}. \tag{4.1}$$

In the case of capacitive energy storage, this can be expressed as

$$\begin{aligned} \eta_{\text{avg}} &= \frac{\int_{\text{discharge cycle}} P_{\text{L}} dt}{E_{\text{init}} - E_{\text{final}}} \\ &= \frac{\int_{\text{discharge cycle}} \eta(t) \cdot P_{\text{supply}}(t) dt}{E_{\text{init}} - E_{\text{final}}} \end{aligned} \tag{4.2}$$

where $P_{\text{supply}}(t)$ is the instantaneous power drawn from the supply, and E_{final} and E_{init} refer to energy stored in the ultracapacitor array. The discharge case illustrated in Fig. 4-2 provides a dramatic illustration of the pitfalls of an S.C. converter with a single conversion ratio. Evaluating the integral results in an average efficiency of a mere 50.1%. This means that the energy usage from the ultracapacitor array would only have been 49.1% of the total energy stored. In comparison, not stacking at all and just letting the ultracapacitor drain to half of its voltage results in an energy usage of 75%. This implies that any energy management system using this stacking discipline must achieve an average efficiency greater than 75% to exhibit any improvement at all.

In order to increase the average efficiency of a switched-capacitor converter, the instantaneous conversion efficiency η must be made responsive to the input voltage. Inductor-based topologies do not suffer this difficulty. A buck converter, for example, can change its voltage conversion ratio by altering its switching duty cycle while remaining ideally 100% efficient. In biomedical applications where small form factor is important, however, a switched-capacitor converter is highly desirable. One way to break this size-efficiency tradeoff is to use a switched-capacitor converter with multiple conversion ratios. These ratios are then selected according to the current input voltage. The next section describes techniques to increase the efficiency.

4.1.3 Techniques to Improve Efficiency

Topology Selection

The selection of a specific topology for a switched-capacitor converter depends heavily on a number of considerations, including device selection and sizing, component working voltages (e.g., blocking and rated voltages), and cost-based metrics. For integrated circuit applications cost per unit area is typically paramount. For a capacitor, areal energy density for a rated voltage can serve as a useful criterion selection. For transistor switches, the ratio of switch conductance and/or blocking voltage with capacitive switching losses serves as a useful criterion. When choosing a device technology for each component, the device with the largest relevant metric, while having a sufficiently-high rated voltage, should be used for a given component in the topology. An analytical method and graphical tool for optimizing for cost, area, and performance criteria is presented in [58].

It should be evident that the technology used to implement a converter plays a significant role in overall performance. Five common topologies in the literature include:

- **Ladder** [59]. Based on two ladders of capacitors to achieve $m : n$ conversion ratios.

- **Dickson** [60]. Improvement upon ladder topology but primarily implements $1 : n$ conversion ratios.

- **Fibonacci** [44]. Performs the highest conversion ratio for a given number of capacitors of any 2-phase topology. A converter with k capacitors exhibits a conversion ratio of $n = F_{k+2}$ where F_{k+2} is the $k + 2^{\text{th}}$ Fibonacci number. A disadvantage of Fibonacci topologies is the unequal distribution of voltages across the charge-transfer capacitors, which unevenly stresses the dielectric structure(s) (e.g., gate-oxide capacitors unevenly driven).

- **Series-Parallel**. As the name suggests, this topology alternates between series and parallel configurations of the charge-transfer capacitors and achieves $m : n$ conversion ratios with an array of $(n - m) \times m$ capacitors $(m < n)$. The immediate disadvantage

of series-parallel topologies is the large number of switches needed to implement them: $(m+1)(n-m)$ in one phase and $m(n-m+1)$ in second phase.

- **Doubler**. The doubler topology consists of cascaded 1:2 stages in order to achieve $1{:}2^k$ conversion ratios using $2k-1$ capacitors.

In [58], these five topologies are compared for increasing conversion ratio values for SSL and FSL metrics (V-A products). It is shown that the converters each start at equal performance from the 2:1 conversion ratio since they all converge in topology at that conversion ratio. However, the performance diverges greatly for increasing conversion ratios. Notably, for SSL, the series-parallel topology performs best while the ladder topology performs worst. The reverse behavior is observed in the FSL regime. The ladder and Dickson converters achieve the best performance while the series-parallel performs worst. Therefore, it is clear that the topology selection must take into account the technology and converter performance metrics for the desired application. Together with the considerations of Chapter 2, load-handling capability, switching frequency, and optimal device selection and sizing trade off and are carefully balanced to identify the best converter topology for a given application.

Multiple Conversion Ratios

The previous section focused on the trade-offs governing the selection of a particular 2-phase switched-capacitor topology for a fixed conversion ratio. In this section, we discuss how to implement a multiple conversion ratio topology with the addition of minimal components. For a switched-capacitor converter with k capacitors, it is possible to obtain a finite, discrete set of conversion ratios determined by the k^{th} Fibonacci number [44]. The disadvantage with using Fibonacci topology is that the voltage distribution on the capacitors also follows a Fibonacci sequence. For a specified lower bound on the instantaneous conversion efficiency and a specified input voltage range, one can determine the minimum number of conversion ratios necessary and the corresponding minimum number of components. For a Fibonacci topology with a 3:1 input voltage range and $v_{\mathrm{L}} = 1$ V, $k = 3$ results in a worst-case instantaneous efficiency of 67%. For a Fibonacci topology with a 4:1 input voltage range, $k = 4$ results in

worst-case instantaneous efficiency of 75%. Fig. 4-3 shows the theoretical efficiency versus input voltage for a non-Fibonacci converter with $k = 3$ over an input voltage range of 4:1. It is possible to achieve further conversion ratios without increasing the number of capacitors by dithering between consecuitve conversion ratios [57]. A drawback of this approach is the increased output voltage ripple and harmonic distortion. For a switched-capacitor converter

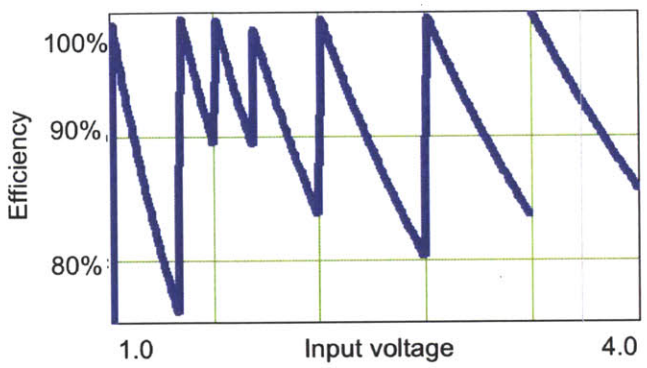


Figure 4-3: Ideal efficiency versus input voltage using a multiple conversion ratio switched-capacitor converter. The output voltage is assumed to be maintained at 1 V. The switched-capacitor circuit used to generate the conversion ratios is shown in Fig. 4-4 and is carefully designed to provide multiple conversion ratios by selectively activating switches (Table 4.2). Using multiple conversion ratios mitigate the linear regulation efficiency characteristic by limiting the voltage range over which any given conversion ratio is active.

topology allowing for n conversion ratios, the conversion efficiency can be expressed as

$$\eta(v_{\text{supply}}) = \frac{v_L}{\alpha_i \cdot v_{\text{supply}}} \tag{4.3}$$

for $i = 1, \ldots, n$ and α_i is selected to maximize $\eta(v_{\text{supply}})$. Fig. 4-3 shows the ultracapacitor bank input voltage and ideal efficiency for $v_{\text{L}} = 1$ V with seven conversion ratios ($\alpha_i \in \left[\frac{1}{3}, \frac{2}{5}, \frac{1}{2}, \frac{3}{5}, \frac{2}{3}, \frac{3}{4}, 1\right]$). Adapting Eq. 4.2 and Eq. 4.3, the average efficiency can be written as

$$= \frac{\int_{\text{discharge cycle}} \left(\frac{v_{\text{L}}}{\alpha(t) \cdot v_{\text{supply}}(t)}\right) \cdot P_{\text{supply}}(t) dt}{E_{\text{initial}} - E_{\text{final}}} \tag{4.4}$$

For an input voltage falling linearly from 4 V to 1 V, the additional three conversion ratios more than double the theoretically achievable average efficiency to greater than 90%.

Fig. 4-4 shows a switch implementation capable of achieving the desired conversion ratios with the minimal number of switches and charge-transfer capacitors. The charge-transfer

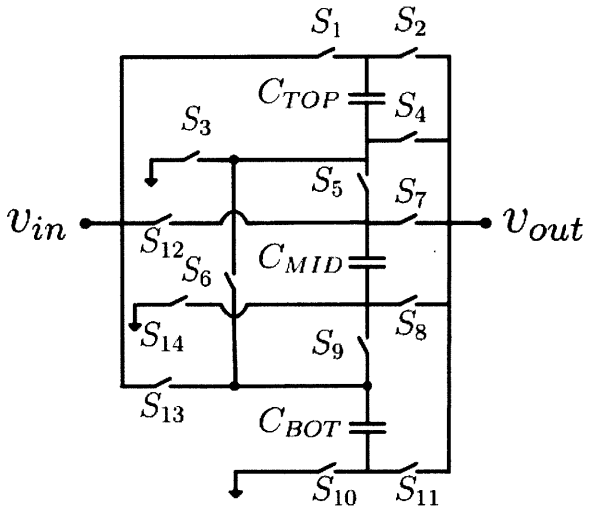


Figure 4-4: Multiple conversion ratio switch matrix for the switched regulator. The topology is capable of seven conversion ratios over a wide-input voltage range and delivers energy to the output during both charge-transfer phases. Table 4.2 maps active switches to each conversion ratio.

capacitors are equal in value and set to C_T. The switches and capacitors operate such that charge is transferred directly from the source to the load in both phases. This ensures that the load-handling capability is maximized for a given switching frequency and charge-transfer capacitors. Direct delivery of energy during both phases has the added benefit of reducing the output voltage ripple. Table 4.1 summarizes the energy handling capability of the various conversion ratios. Table 4.2 indicates which topology switches are active for the non-overlapping phases for each conversion ratios.

Table 4.1: Energy extracted from source every cycle for switched-capacitor topology of Fig. 4-4.

4 **Conversion Ratio**	**Energy Extracted from Source**
3:1	$2.25 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$
5:2	$1.67 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$
2:1	$6 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$
5:3	$2.5 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$
3:2	$4.5 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$
4:3	$4 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$
1:1	$2 \cdot C_{\mathrm{T}} \cdot v_{\mathrm{sup}} \cdot v_{\Delta}$

Table 4.2: Switch states for various conversion ratios of Fig. 4-4.

Conversion Ratio	ϕ_1	ϕ_2	**OFF**	**Active Capacitor(s)**
3:1	S_1, S_6, S_{11}	$S_2, S_3, S_8, S_9, S_{10}$	$S_4, S_5, S_7, S_{12}, S_{13}, S_{14}$	TOP, BOT
5:2	$S_1, S_5, S_6, S_8, S_{11}$	$S_2, S_3, S_7, S_9, S_{10}$	$S_4, S_{12}, S_{13}, S_{14}$	ALL
2:1	S_1, S_4, S_{11}, S_{13}	$S_2, S_3, S_8, S_9, S_{10}$	$S_5, S_6, S_7, S_{12}, S_{14}$	TOP, BOT
5:3	$S_1, S_5, S_8, S_{11}, S_{13}$	$S_2, S_6, S_7, S_9, S_{10}$	S_3, S_4, S_{12}, S_{14}	ALL
3:2	S_1, S_4, S_{11}, S_{13}	S_2, S_6, S_{10}	$S_3, S_5, S_7, S_8, S_9, S_{12}, S_{14}$	TOP, BOT
4:3	$S_1, S_4, S_8, S_{11}, S_{12}, S_{13}$	S_2, S_5, S_9, S_{10}	S_3, S_6, S_7, S_{14}	ALL
1:1	S_1, S_3, S_{10}, S_{13}	$S_2, S_3, S_8, S_9, S_{10}$	$S_4, S_5, S_6, S_7, S_{11}, S_{12}, S_{14}$	TOP, BOT

4.2 Practical Considerations for Integrated Switched-capacitor Circuits

In general the equivalent resistance of a switched-capacitor stage only takes into account conduction losses. Several additional loss mechanisms must be factored in the expression for $\eta(t)$ in order to more accurately predict actual behavior, including switching/gating losses, P_{sw}, bottom-plate losses if using integrated charge-transfer capacitors, P_{bp}, and control losses,

P_{ctrl}. These loss mechanisms are discussed in Chapter 2 and can be expressed as follows:

$$P_{\text{sw}} = n \cdot C_{ox} W L \cdot v_{\text{sup}}^2 \cdot f_{\text{s}} = K_{\text{sw}} \cdot v_{\text{sup}}^2 \cdot f_{\text{s}} \tag{4.5}$$

$$P_{\text{bp}} = \alpha_{\text{bp}} C \cdot \gamma_i(\alpha_i, v_{\text{sup}}, \ldots) \cdot v_{\text{sup}}^2 \cdot f_{\text{s}} = K_{\text{bp,i}} \cdot v_{\text{sup}}^2 \cdot f_{\text{s}} \tag{4.6}$$

$$P_{\text{ctrl}} = \left(K_{\text{c}} \cdot v_{\text{sup}}^2 + I_{\text{leak}} \cdot v_{\text{sup}} \cdot f_{\text{s}}^{-}1\right) \cdot f_{\text{s}} \tag{4.7}$$

with various parameters corresponding listed in Table 4.3.

Table 4.3:

n	Number of switches used; dependent on the conversion ratio
C_{ox}	Gate-oxide capacitance per unit area
W and L	Width and length of the switches
α_{bp}	Ratio of bottom-plate capacitance to actual capacitance C
I_{leak}	Total leakage current consumed by the control circuitry
K_{sw}, $K_{\text{bp,i}}$, K_{c}	Lumped loss parameters for P_{sw}, P_{bp}, and P_{ctrl}

The overall expression for efficiency is expanded as follows

$$\eta_{\text{total}} = \frac{P_{\text{delivered}}}{P_{\text{source}} + P_{\text{sw}} + P_{\text{bp}} + P_{\text{ctrl}}} \tag{4.8}$$

with

$$\begin{aligned} P_{\text{delivered}} &= v_{\text{L}} \cdot I_{\text{L}} = (v_{\text{NL}} - v_{\Delta}) \cdot \frac{v_{\Delta}}{R_{\text{eq}}} \\ P_{\text{source}} &= v_{\text{sup}} \cdot \alpha_i \cdot I_{\text{L}} = v_{\text{sup}} \cdot \alpha_i \cdot \frac{v_{\Delta}}{R_{\text{eq}}} \end{aligned} \tag{4.9}$$

Combining Eq. 4.5, Eq. 4.8, and Eq. 4.9 yields a complete expression for η as follows

$$\begin{aligned} \eta &= \left[1 - \tfrac{v_{\Delta}}{v_{\text{NL}}}\right] \cdot \left[1 + K_{\text{sw}} \cdot \frac{v_{\text{sup}}^2 \cdot f_{\text{s}}}{\alpha_i \cdot v_{\text{sup}} \frac{v_{\Delta}}{R_{\text{eq}}}} + K_{\text{bp,i}} \cdot \frac{v_{\text{sup}}^2 f_{\text{s}}}{\alpha_i \cdot v_{\text{sup}} \frac{v_{\Delta}}{R_{\text{eq}}}} + \right. \\ &\qquad \left. K_c \cdot \frac{v_{\text{sup}}^2 \cdot f_{\text{s}}}{\alpha_i \cdot v_{\text{sup}} \frac{v_{\Delta}}{R_{\text{eq}}}} + \frac{I_{\text{leak}} \cdot v_{\text{sup}} \cdot f_{\text{s}}^{-1}}{\alpha_i \cdot v_{\text{sup}} \frac{v_{\Delta}}{R_{\text{eq}}}} \cdot f_{\text{s}} \right]^{-1} \\ &= \left[1 - \tfrac{v_{\text{NL}} - v_{\text{NL}}}{v_{\text{NL}}}\right] \cdot \left[1 + \frac{v_{\text{sup}} \cdot f_{\text{s}}}{\alpha_i \cdot I_{\text{L}}} \cdot (K_{\text{sw}} + K_{\text{bp,i}} + K_c) + \frac{1}{\alpha_i} \cdot \frac{I_{\text{leak}}}{I_{\text{L}}}\right]^{-1} \end{aligned} \tag{4.10}$$

where $K_{\text{bp,i}}$ is the bottom-plate parasitic loss factor adjusted for the i^{th} conversion ratio, α_i.

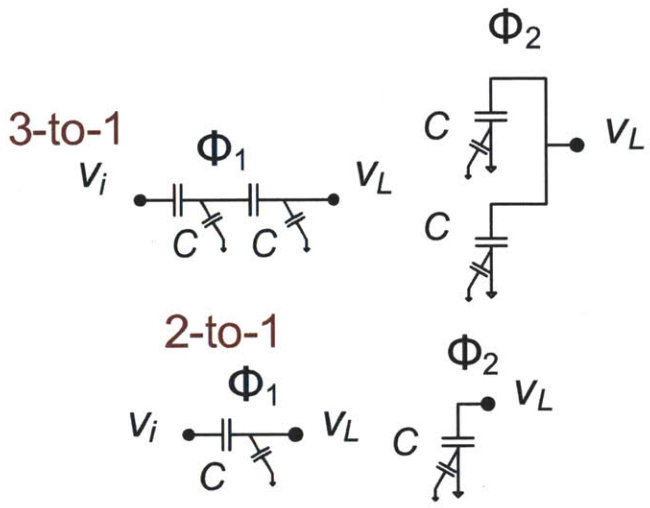


Figure 4-5: The effects of bottom-plate parasitics are dependent on the switched-capacitor topology. Different conversion ratios yield different K_{bp} factors. This is illustrated for the 3:1 and 2:1 topologies above.

For the 3:1 and 2:1 conversion ratio topologies shown in Fig. 4-5, charge-multiplier analysis is used to derive γ_i adjustment factors:

$$\begin{aligned}
K_{\text{bp,3:1}} &= \alpha_{\text{bp}} C \cdot \gamma_{3:1}(\alpha_{3:1}, v_{\text{sup}}, \ldots)^2 \\
&= \alpha_{\text{bp}} C \cdot \left[\frac{1}{2}\left(v_{\text{sup}} - \frac{1}{3} v_{\text{sup}}\right)\right]^2 \\
\gamma_{3:1} &= \frac{1}{9} \\
K_{\text{bp,2:1}} &= \alpha_{\text{bp}} C \cdot \gamma_{2:1}(\alpha_{2:1}, v_{\text{sup}}, \ldots)^2 \\
&= 3 \cdot \alpha_{\text{bp}} C \cdot \left[\frac{1}{2} \cdot v_{\text{sup}}\right]^2 \\
\gamma_{2:1} &= \frac{3}{4}
\end{aligned} \tag{4.11}$$

Similar calculations yield γ_i for the remaining conversion ratios as

For integrated switched-capacitor converters, bottom-plate capacitances are a major limitation on the maximum achievable efficiency. The factor α_{bp} can be as high as 10-20% for

Table 4.4: Adjustment factors for bottom-plate parameter for each conversion ratio

Bottom-plate Adjustment Factors	Scale Factor
$\gamma_{5:2}$	$\frac{6}{25}$
$\gamma_{5:3}$	$\frac{91}{225}$
$\gamma_{3:2}$	$\frac{5}{9}$
$\gamma_{4:3}$	$\frac{7}{8}$
$\gamma_{1:1}$	0

integrated capacitors and, typically, $K_{\mathrm{bp,i}} \gg \{K_{\mathrm{sw}}, K_{\mathrm{c}}\}$. Fig. 4-6 illustrates the degradation on efficiency due to various values of α_{bp}. Plots of efficiency due to conduction-only and all

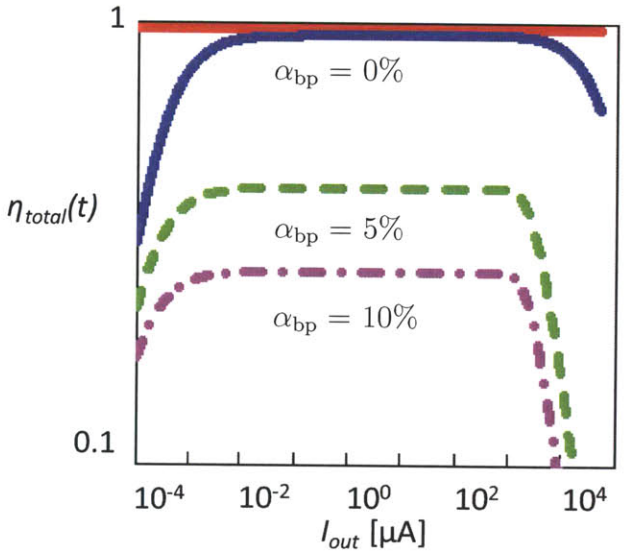


Figure 4-6: Bottom-plate parasitics degrade the efficiency performance of integrated switched-capacitor circuits. The effect of α_{bp} is shown for $\alpha_i = \frac{1}{3}$ and $f_{\mathrm{s}} = 10$ MHz for three values of α_{bp}.

additional loss mechanisms, $\eta_\Delta = 1 - \frac{v_\Delta}{v_{\mathrm{NL}}}$, and η, respectively, are shown in Fig. 4-7 for $K_{\mathrm{sw}} = 340$ fF, $K_{\mathrm{bp}} = 16.5$ pF, and $K_{\mathrm{c}} = 100$ fF ($W = 100$ μm, $L = 180$ nm, $m = 2$, $\alpha_{\mathrm{bp}} = 0.05$, $C = 1$ nF, $I_{\mathrm{leak}} = 1$ nA, $f_{\mathrm{s}} = 100$ kHz). For the range where the 1:1 configuration is active (1 - 1.33 V), η is approximately equal to η_Δ since both terminals of the bottom-plate

capacitance are grounded during both phases. The 2:1 configuration contributes the largest degradation to efficiency from bottom-plate losses, which is consistent with the significant drop in efficiency over the range (2 - 2.5 V). This can be seen from Eq. 4.10 and the $K_{\mathrm{bp,i}}/\alpha_i$ factor being largest for $\alpha_{2:1}$ and $K_{\mathrm{bp,2:1}}$.

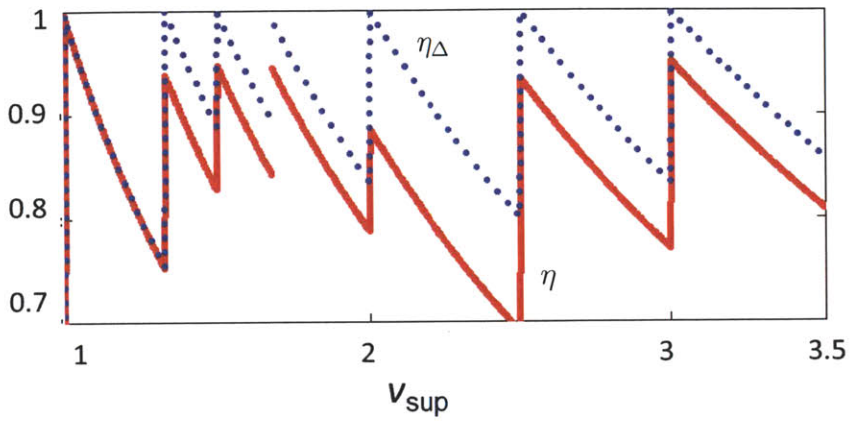


Figure 4-7: Effect of additional loss mechanisms on overall efficiency. (Blue) η_Δ is due to conduction-only losses and the (red) η includes additional loss mechanisms such as bottom-plate losses ($\alpha_{\mathrm{bp}} = 5\%$), leakage, and control losses.

4.2.1 Control Strategy

The two dominant control strategies used for switched-capacitor converters are pulse frequency modulation (PFM) [43] and burst-mode (on-off, "bang-bang") control [61, 62]. In both schemes, the idea is to adjust the instantaneous switching frequency to accommodate the load while maintaining the output within a ripple specification. Viewed another way, both schemes function by modulating the *average* switching frequency in order to deliver power to the load while minimizing switching losses.

A burst-mode control strategy is used here. An advantage of burst-mode control is that the converter incurs no losses when it is disabled, and operates at a fixed, high-efficiency switching frequency when it is enabled, resulting in higher efficiency at heavy loads and at light loads. Moreover, the simplicity of this control scheme overcomes the challenges limiting

traditional pulse-frequency modulation (PFM) schemes. For instance, continuous frequency modulation requires a static-draw VCO. Alternatively, a digitally-controlled oscillator may be implemented to limit digital power dissipation. However, this approach is limited to discrete switching frequencies across a range where the switched-capacitor converter might operate at a lower efficiency. To see this, recall that one would like to minimize the value of R_{eq}. There are two design parameters available for achieving the objective of operating near the "elbow" of the switched-capacitor converter output resistance since the charge multiplier vector is fixed by the topology. The first is appropriately selecting the unit capacitance, C, of the switched-capacitor converter stage. Arbitrarily increasing C is limited by area constraints. The other way is to use PFM. Analog PFM incurs a static power penalty while digital PFM (DPFM) fails to track the R_{eq} minimum point without overshoot unless high-resolution DPFM control is implemented costing in additional area and power dissipation.

Under burst-mode control, a *single* switching frequency is selected in conjunction with area constraints to minimize conduction losses (i.e., R_{eq}) for the conversion ratio that extracts the smallest amount of energy from the source for delivery to the load. This ensures the ability to maintain the desired output voltage within a ripple specification by delivering larger charge packets at the remaining conversion ratios. For example, the 5:2 topology extracts the least amount of charge ($6.66 \cdot C \cdot v_{\text{sup}}(t) \cdot v_{\Delta}$) from the source and sets the upper-bound on the switching frequency, $f_{\text{s,high}}$, while the 2:1 topology extracts the largest charge packets ($24 \cdot C \cdot v_{\text{sup}}(t) \cdot v_{\Delta}$), thereby requiring the lowest switching frequency, $f_{\text{s,low}}$, for a constant current source load [46]. It is then possible to obtain all average frequency values in the range $f_{\text{s,high}} - f_{\text{s,low}}$ according to the following relationship

$$f_{\text{avg}}(t) = \frac{\int f_{\text{s,high}} \cdot \Gamma(t) dt}{\Delta t} \tag{4.12}$$

where $\Gamma(t)$ functions as the digital frequency modulating signal. $\Gamma(t)$ is 0 when the output voltage is above the desired level and 1 when below. The average value of $\Gamma(t)$ over Δt sets the $f_{\text{avg}}(t)$.

4.2.2 Start-up

A careful start-up sequence is an important consideration for an energy processing system. One wishes to ensure that electronics are disabled and protected against power supply fluctuation for operational integrity. For the energy management IC presented here, two nodes in the system serve as power supplies: (1) v_{uc} serves as the energy storage buffer, and (2) v_{L} is designed to serve as a power supply to load electronics. Both power supplies must be supervised and dependent circuitry protected against steep drops and fluctuations. An under-voltage lockout circuit provides the desired supervision and ensures that critical functions (i.e., digital and energy processing) are protected and shut down while the power supplies stabilize [3]. In addition, it is desirable to implement hysteresis in order to detect when both upper and lower thresholds are crossed.

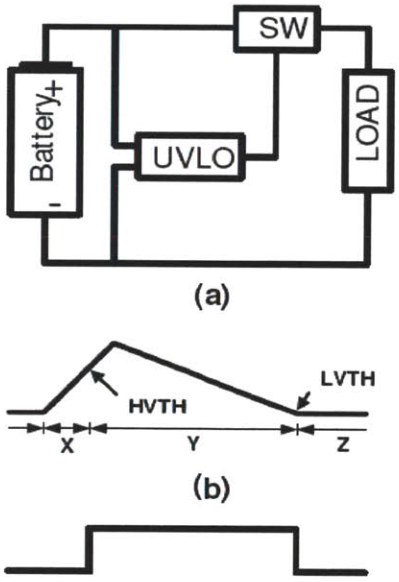


Figure 4-8: CMOS under-voltage lockout block diagram [3] to ensure that electronics are disabled and protected against power supply fluctuation. It is important to provide protection to ICs when the power-supply dips to levels that may cause undesired operation. The UVLO provides the simple function to ensure that SW is "OFF" below pre-determined thresholds

To ensure proper startup, two under-voltage lock-out (UVLO) blocks and a multiplexer block are implemented. Fig. 4-8 shows the block diagram of a UVLO circuit and the

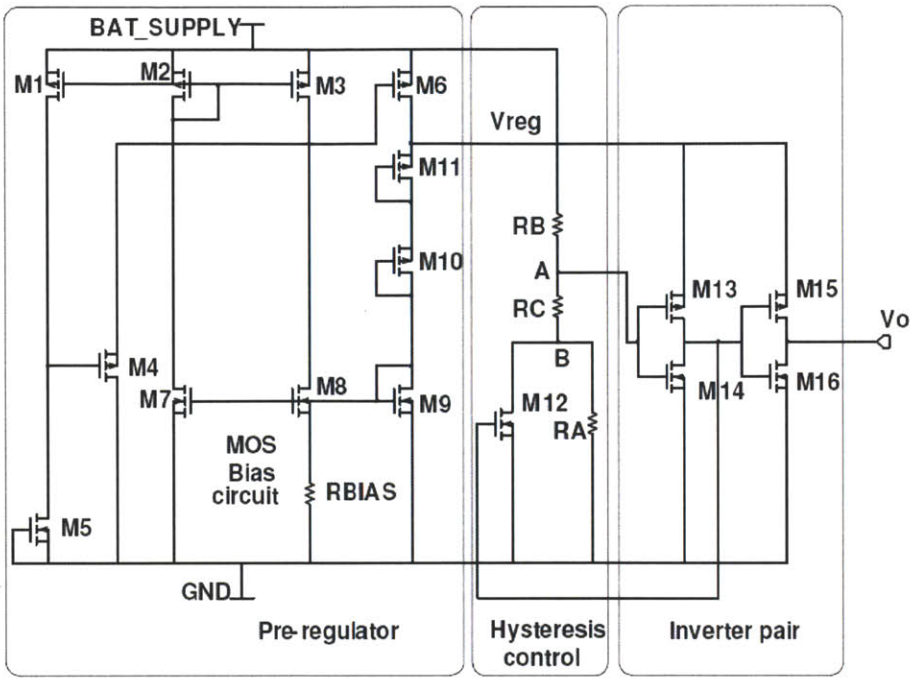


Figure 4-9: UVLO circuit implementation [3]. The resistor voltage divider controlled by M12 is the hysteresis controlling section which generates the input voltage to the first inverter of the inverter pair.

corresponding hysteretic waveforms. The circuit implementation is shown in Fig. 4-9. For our purposes during startup, a first UVLO drives a multiplexer that selects between v_{uc} or v_{L} to set the supply of digital and auxiliary blocks. While v_{L} ramps up to its steady-state value, v_{uc}, which is presumed to be in a charging phase, directly powers the chip. When v_{uc} exceeds 2.5 V, the first UVLO output is triggered and provides a reset for the digital section, beginning energy processing functions. The second UVLO supervises v_{L} and triggers when v_{L} exceeds 1.1 V. The second UVLO serves as a reset signal for load electronics.

Support Circuitry The addition of support circuitry blocks are included to help reduce power consumption, and drive both the ultracapacitor array switches and the switched-capacitor stage switches. Fig. 4-10, Fig. 4-11, and Fig. 4-12 show the circuit implementations for the level-shifters, tapered gate-drivers, and non-overlapping clock generation blocks,

respectively, of Fig. 4-1. Fig. 4-13 shows a power supply selector block used to minimize $C \cdot V^2$ power by using the switched regulator output voltage for powering much of the energy management circuitry rather than using the higher ultracapacitor bank voltage.

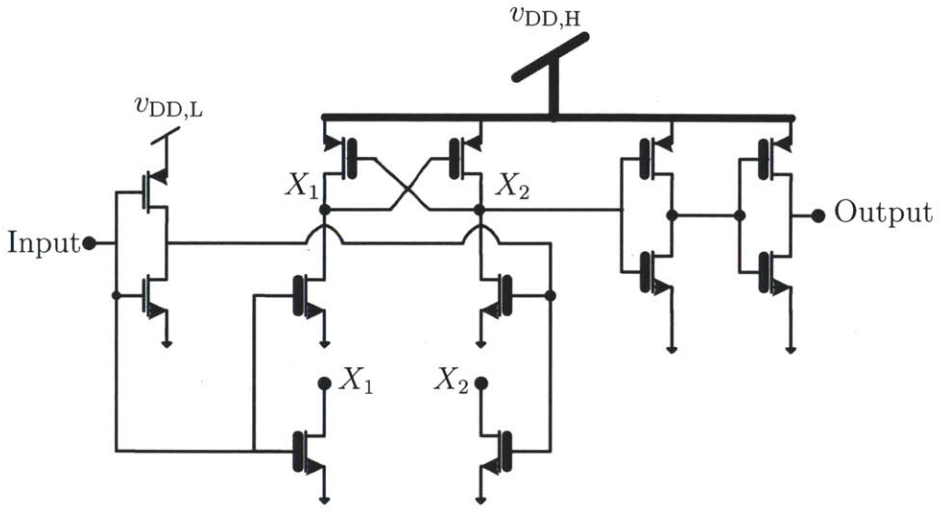


Figure 4-10: Level-shifters are used to raise the voltage levels up to the ultracapacitor bank voltage as necessary. To reduce the $C \cdot V^2$ energy, the digital section operates on the lower supply voltage of the switched-regulator output, $v_{DD,L} = v_L$.

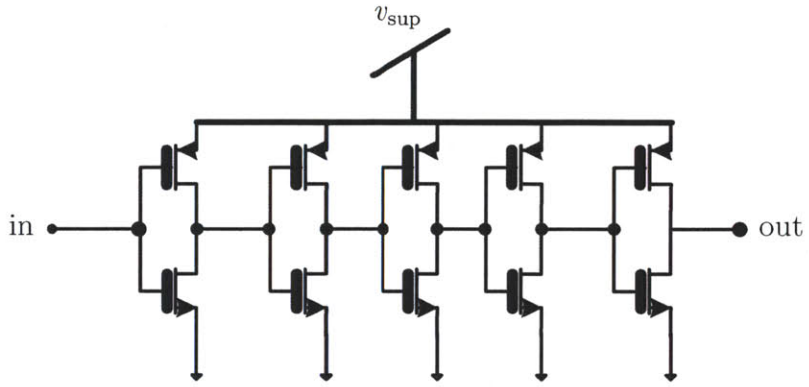


Figure 4-11: 5-V CMOS tapered driver circuit used to drive the ultracapacitor and switched-regulator switches.

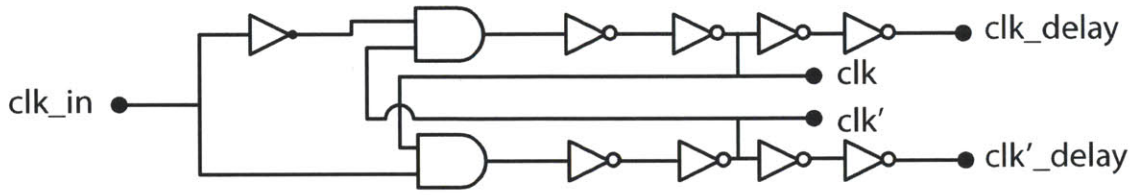


Figure 4-12: Non-overlapping clock generation circuit for generating ϕ_1 and ϕ_2 signals to drive charge-transfer phases of switched regulator.

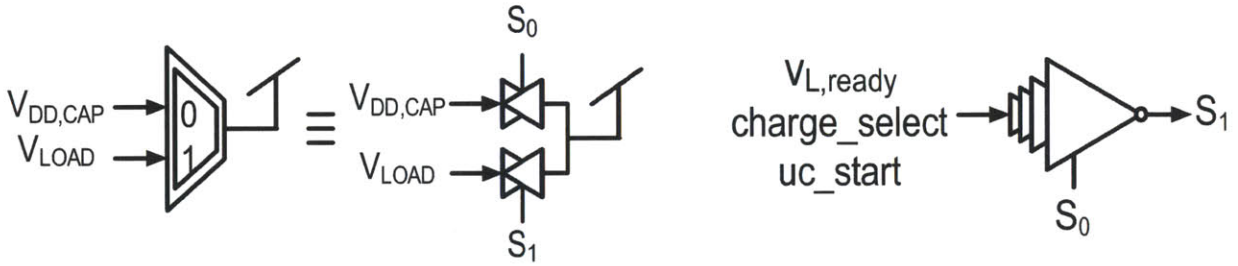


Figure 4-13: The power supply selector block switches to the switched regulator voltage, v_{L}, once the $v_{\mathrm{L,ready}}$, signal is HI. This reduces $C \cdot V^2$ power. The MUX-like block consists of large transmission gates that are driven by the buffered output of the switched regulator UVLO block, $v_{\mathrm{L,ready}}$. Other support signals including the UVLO output for the ultracapacitor bank, **uc_start**, and the charge-mode signal from the rectifier, **charge_select**, are buffered through gate drivers (Fig. 4-11).

4.3 Experimental Results

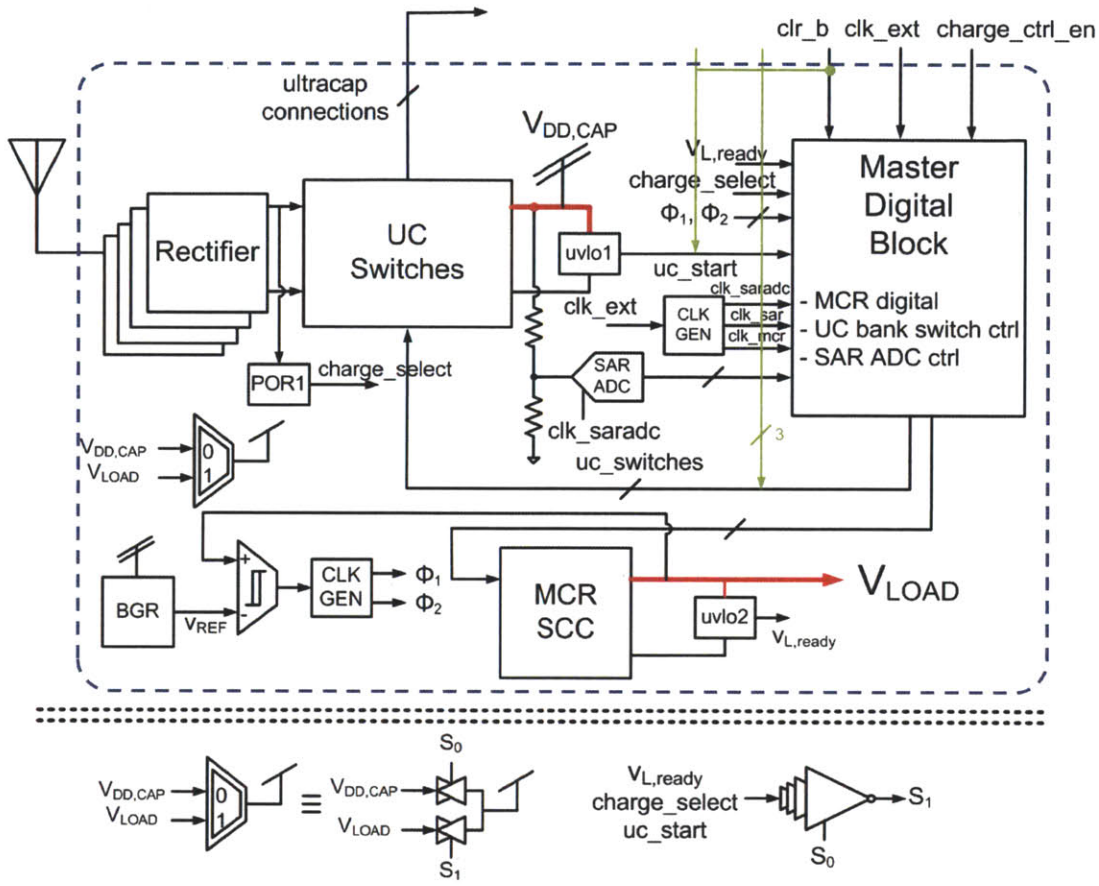


Figure 4-14: Chip-level implementation for energy management chip. The chip includes the energy utilization loop with the ultracapacitors switch matrix. The output load voltage is compared to the bandgap reference voltage. When the output voltage drops below v_{ref} the comparator trips and generates 50% duty-cycled, non-overlapping clock signals that drive the multiple conversion ratio switched-capacitor converter. The UVLO blocks to monitor our power supply voltages from the ultracapacitor bank and the output of the switched-regulator. The rectifier has two paths: (1) one for recharging the ultracapacitor bank, and (2) the second to drive a power-on reset block which signals the master digital block to operate in charging-mode.

Fig. 4-14 shows the architecture implemented for the energy management IC. In steady-state, the operation is discerned by focusing on the multiple conversion ratio switched-capacitor feedback loop. The load voltage, v_{L}, is compared to the output of a nano-power

bandgap reference, v_{ref}. If v_{L} drops below a specified level, the comparator trips and generates 50% duty-cycled, non-overlapping clock signals ϕ_1 and ϕ_2. These signals are buffered through the tapered gate drivers in order to effectively drive the switches of the switched-capacitor converter.

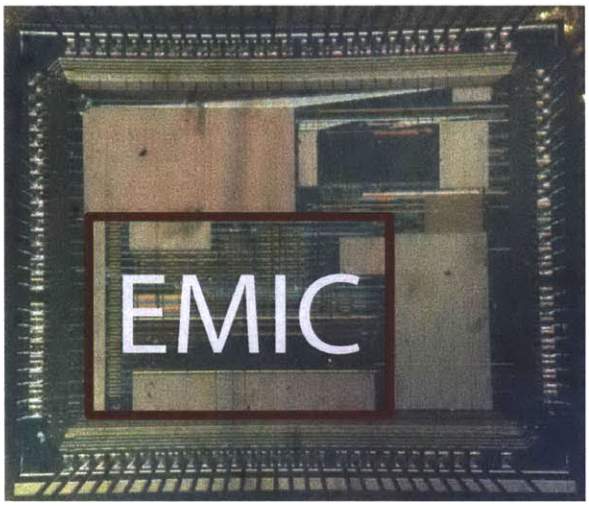


Figure 4-15: Micrograph of the chip fabricated in 180-nm, 5-V CMOS process. The active area occupies less than 1.7 mm^2 including 500 pF of integrated filtering poly-poly capacitors.

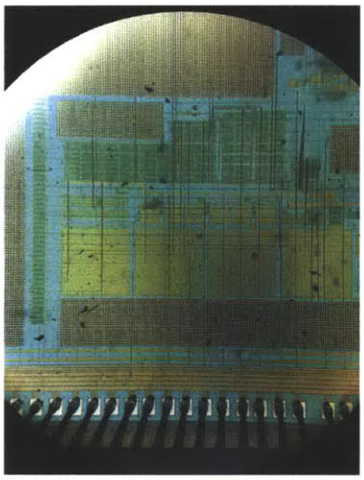


Figure 4-16: Micrograph of chip power management section.

Fig. 4-15 shows the micrograph of the test chip fabricated in a 180-nm CMOS process

with 5-V devices. Fig. 4-16 zooms into the energy management sections. The active area of the chip occupies 1.7 mm^2. To avoid bottom-plate losses of integrated capacitors, three off-chip, 1 μF charge-transfer capacitors are used in the embedded switched-capacitor converter. The ultracapacitors are also contained off-chip.

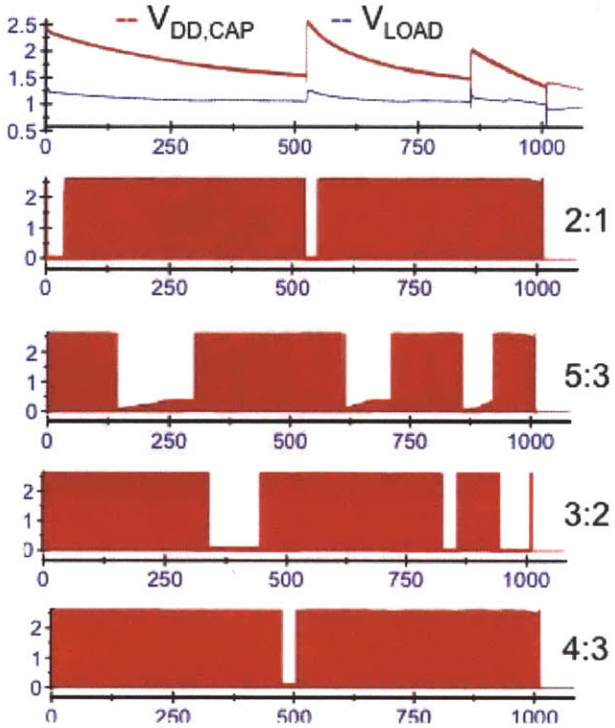


Figure 4-17: Transient operation of energy management IC over discharge cycle of ultracapacitor array. The stacking of the ultracapacitors occurs once the low threshold (1.4 V) is exceeded. The load voltage is tightly regulated to 1.1 V. Four conversion ratios are active for the input range shown as evidenced by the nulls in the four status signals.

Fig. 4-17 captures the transient operation over a full discharge cycle (i.e., 2.5 V $\geq v_{uc} \geq$ 1.3 V). One can observe the stepping up of v_{uc} once a low threshold ($\sim$1.4 V) is reached [47]. A bank of four CAP-XX ultracapacitors are used to allow for three stacking configurations (i.e., parallel, parallel-series, series). v_L is tightly regulated to 1.1 V $\pm$10% by the feedback control that generates the non-overlapping clock signals. For the range depicted in Fig. 4-17, four conversion ratios are active according to Table 4.5. We should note that the narrow windows where none of the conversion ratios are active are decision ranges outside

the range of a LUT in the master digital block. This is a hysteretic mechanism to help minimize unintended dithering between conversion ratios. During stacking transitions of the ultracapacitor array, a spike in v_L results due to the fact that the control logic does not anticipate the appropriate conversion ratio *a priori*. However, the spike is well within 20% of the nominal 1.1 V at all times.

Table 4.5: Conversion ratio mapping for wide range of v_{uc}

$\mathbf{v_{uc}}$	**Conversion Ratio**
$v_{uc} > 3.375$	3:1
$3.375 \geq v_{uc} > 2.750$	5:2
$2.750 \geq v_{uc} > 2.250$	2:1
$2.250 \geq v_{uc} > 2.000$	5:3
$2.000 \geq v_{uc} > 1.750$	3:2
$1.750 \geq v_{uc} > 1.375$	4:3
$v_{uc} \leq 1.375$	1:1

Fig. 4-18 plots efficiency with v_{uc} = 1.5 V, 1.8 V, and 2.3 V corresponding to the conversion ratio as shown in Table 4.5. The efficiency displays behavior expected from burst-mode operation and is maintained above 75% over a wide range of loads. As expected, the efficiency drops off on the low and high ends due to control and conduction losses, respectively.

Fig. 4-19 shows the static efficiency measurements as v_{uc} varies from 1.0-4.0 V with a 210 μW load. An external supply was used during these measurements since the ultracapacitors could not exceed 2.5 V. The seven conversion ratios for the corresponding ranges of v_{uc} are denoted. One can observe the shape of the waveform and note it is consistent with the theoretical efficiency waveform of Fig. 4-3.

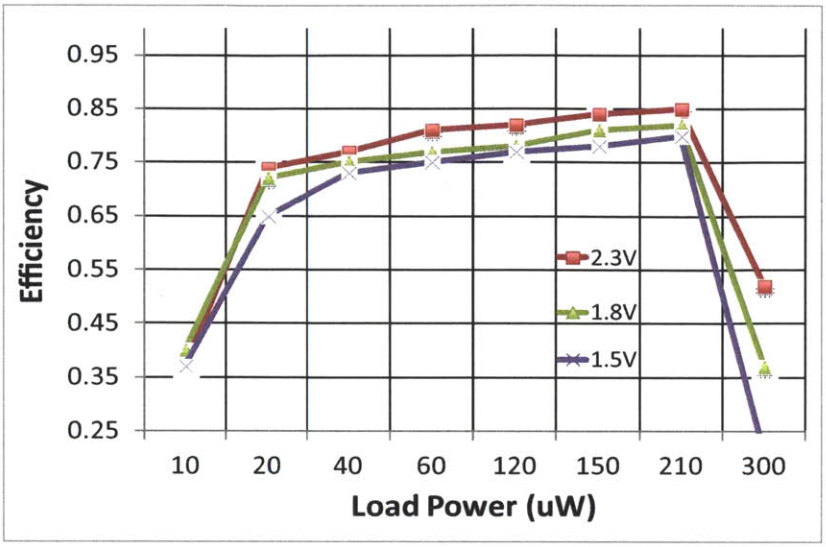


Figure 4-18: Efficiency versus load power for three levels of input voltage, $v_{\text{uc}} = 1.5$ V, 1.8 V, and 2.3 V. As expected, the efficiency drops off on the low and high ends due to control and conduction losses, respectively.

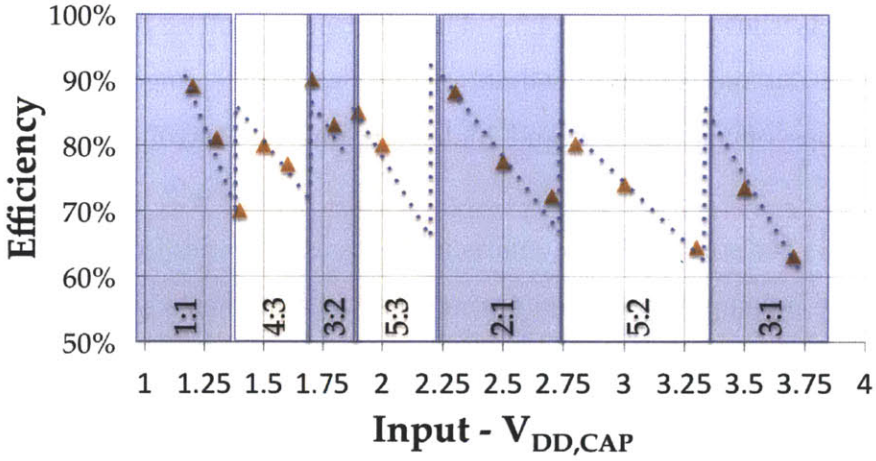


Figure 4-19: Efficiency versus input voltage. We observe the saw-tooth characteristic from changing conversion ratios according to the input voltage. The plot captures the seven conversion ratios of the switched-capacitor topology Fig. 4-4. The average efficiency is ~82%.

4.4 Summary and Conclusions

In this chapter, we presented a method for using multiple conversion efficiencies to make a switched-capacitor converter scheme worthwhile for wide-input-range supplies. The chip implementation achieves a peak efficiency of 90% with better than 70% efficiency for loads between 20 and 250 μW, and input voltages between 1.25 V and 3 V. The chip is designed to allow biomedical implants to optimally use ultracapacitors in place of batteries.

Chapter 5

Conclusions

The attractiveness of medical implants for minimally invasive monitoring is strongly tied to the size and lifetime of the devices. Proper energy management is paramount and necessitates high energy utilization for size constraints associated with energy storage solutions. For in-body applications, energy efficiency and ultra-low power operation are imperative to prevent tissue damage due to heating and prolonging operating lifetime. Moreover, in order to be sustainable as long-term monitoring solutions, it is required that medical implants be wirelessly rechargeable, preferably without the need for additional surgery. This thesis has focused on energy management techniques for using ultracapacitors as energy storage alternatives to batteries and maximizing the utilization of available energy. The specific contributions made are listed below.

5.1 Summary of Contributions

Switched-capacitor DC-DC Converters

- Analysis of the fundamental efficiency limitations of switched-capacitor circuits and the inherent loss mechanisms. It was shown that the conversion ratio must vary with the input in order to increase the average efficiency of a switched-capacitor converter accommodating a wide-input-range.

- Analysis of the current handling capability of switched-capacitor converters with design guidance and insights provided to maximize efficiency and load-handling.

Energy Utilization

- Identification of (1) efficiency challenges with wide-ranging input voltage energy supplies such as ultracapacitors, and (2) the advances in ultracapacitor technologies presenting a way to facilitate using these devices instead of batteries for ultra-small implants.

- Fast, wireless recharging circuit using a cascade of simple synchronous rectifier stages with a 900-MHz custom antenna.

- An ultra-low power, 4-nW bandgap reference circuit to provide a stable reference for two test chips for regulating an output voltage.

- A stacking procedure for a bank of ultracapacitors to use more than 98% of the initial energy stored before the output voltage drops unsuitably low.

- A complete energy management solution that accounts for the start-up of a test chip by restoring charge to an ultracapacitor array that has completely lost charge. The energy management IC is able to recharge from RF energy coupled into an antenna, even from the zero-charge state.

Multiple Conversion Ratio Switched-capacitor Converter

- Techniques for wide-input-range energy management and the implementation of a switched-capacitor converter capable of seven conversion ratios that achieves a peak efficiency of 90%, and maintains an average efficiency above 82% over a wide-input range.

- A complete solution in digital CMOS that allows low-power systems, such as biomedical implants, to optimally use ultracapacitors instead of batteries as their energy storage

elements. The solution consists of a switched-capacitor DC-DC converter with multiple conversion ratios, a switch matrix to control the configuration of an ultracapacitor array, and digital control to govern charging and discharging of the energy bank. The DC-DC converter efficiency does not fall below 70% for loads between 20 and 250 μW and operates for input voltages between 1.25 and 3 V.

5.2 Open Problems

There are several open problems and areas of interest related to this work. This thesis has demonstrated the feasibility of using ultracapacitors as an alternative energy storage solution to traditional batteries. Additional work can lead to improved total energy management solutions for minimally invasive bio-implant platforms. For example, one area of exploration is the on-chip integration of ultracapacitors with standard CMOS processes. Much work has been devoted to the research of increased energy density technologies but less efforts have gone into the study and feasibility of integrating the technologies with standard, on-chip CMOS processes. Similarly, the on-chip integration of efficient antennas for in-body data communications and power transfer is of interest. Lastly, the extension of the techniques developed in this thesis for higher power applications may be of interest. This is expanded further in the next for automotive waste heat recovery, space, and military applications.

5.2.1 Switched-Capacitor Converters for High-Power Applications

The contributions of this thesis may be extended to higher power applications. Power management technologies which are efficient, reliable, compact, and lightweight are needed to enable integration of advanced power sources and modern digital systems into commercial, space, and military platforms. Delivery of power to satellite subsystems, such as sensors, transceiver modules, and bus systems, requires efficient DC-DC converters that can support multiple loads at decreasingly low output voltages. Military architectures of ships, aircrafts, and vehicles employ traditional switched-mode power supplies (SMPS) which contain bulky

magnetics and conventional components.

The work presented in this thesis may be used to develop novel, high-efficiency, high-reliability energy management systems for high power applications based upon architectures incorporating switched-ultracapacitors, for example. Implementing the energy storage and power conversion ideas and techniques developed in this thesis might enable high efficiency performance to accommodate modern digital logic and analog processing electronics operating at low voltages (< 1.8 V), and high power density within a lightweight and modular unit. For space applications, ultracapacitors already lend themselves to total ionized dose hardness (> 100 krads), high single event latchup threshold, and single event functional interrupt of less than one event per fifty years. A system that conditions power across a wide range of diverse power source inputs and delivers a wide range of regulated outputs can be possible.

Automotive Waste Heat Recovery Applications

Energy efficiency of power electronics and management systems continues to be a major factor affecting size, weight, and cost of mobile products in which these electronics are used. Increasingly, sophisticated battery-operated electronic systems and self-powered systems - such as thermoelectric generators (TEG), thermo-photovoltaics, etc. – are being used in many environments, promising significant strides towards energy independence and emissions reductions. However, reliability remains a challenge, affecting customer perception of quality and maintenance costs. Likewise, managing product cost is also critical in achieving market penetration and customer accessibility. In particular, automotive TEGs pose unique challenges for conventional power conversion and necessitate special conditioning.

Increased electrical power demands for 2005+ production year vehicles has given rise to interest in energy recovery technologies - such as automotive TEG (a solid state energy harvester) – in order to reduce electrical load on the alternator, which is inherently inefficient. Furthermore, minimizing costs of vehicle electrical subsystems is paramount for commercial viability for automotive companies . Since 2002, the Department of Energy's (DOE) Vehicle

Technologies Program has provided over $272M in funding through the FreedomCAR and Fuel Partnership program, including automotive companies such as Chrysler Corporation, Ford Motor Company, and General Motors Corporation, to address the challenges of vehicle inefficiency.

Advanced power electronics funding in the DOE's Vehicle Technologies Program accounts for over 16% of the program's budget, however, relatively little emphasis has been placed on TEG power conditioning due to only recent advances in the TEG systems, which now look promising in affording attractive fuel efficiency benefits (~10%). Uniquely designed power management technologies which are efficient, reliable, compact, and lightweight are needed to enable integration of these energy harvesting platforms into vehicles. For combustion-based engine platforms, for example, delivery of power from TEG exhaust waste heat recovery in vehicles requires efficient DC-DC converters that can support multiple inputs/loads at various voltage regimes. Once developed, these technologies could easily translate into many additional mobile applications, including passenger, commercial and military vehicles as well as portable power generators, etc.

Conditioning thermoelectric generated power in automotive and industrial applications from waste heat sources is non-trivial due to many reasons, several presented here:

1. High currents and low voltages from TEGs are characteristic. In addition, the dynamic responses caused by engine operation are challenging to handle. Fig. 5-1 shows a narrow input range (0-4 V) for a TEG configuration, which is typically 0-25 V. This profile exemplifies the type of unique challenges for a TEG power conditioning system. The high amperage levels are fundamentally lossy due to copper and cable heating. Although a multi-phase architecture may seem like the perfect solution for this issue, the increased component count, size, etc. may not be ideal for such mobile applications.

2. As depicted in Fig. 5-1, peak power is only realized if the converter has maximum power point tracking (MPPT) [63, 64].

3. To avoid suboptimal TEG efficiency, generated power from different "zones" of the

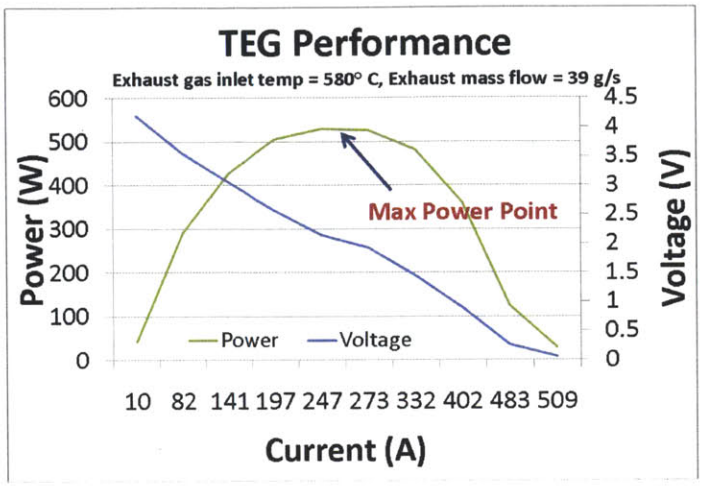


Figure 5-1: Typical power characteristic of TEG.

TEG system should be conditioned separately due to different power characteristics among the zones.

Large TEG system configurations (100s to 1000s of Watts) achieve suboptimal TEG-to-electrical power transfer efficiency because of lack of adequate power conditioning to meet the challenges listed in 1 - 3 as well as others. Similar issues plague photovoltaic and thermo-photovoltaic configurations. Low TEG-to-electrical power transfer efficiency, inconsistent output power due to temperature fluctuation, and high cost have impeded poor adoption of TEG technology.

The techniques presented in this thesis may give way to the design of DC-DC multiple-input, multiple-output (MIMO) two-stage power converter architectures based upon the integration of switched-ultracapacitor configurations and advanced control techniques. An appealing architecture is one enabling a relatively simple means of simultaneously achieving MIMO capability and very high efficiencies over a wide range of diverse and dynamic input voltages, characteristic of today's energy harvesters such as thermoelectric generation (TEG) from automotive exhaust waste heat. It may be possible to construct such a converter using commercial off-the-shelf (COTS) components with a scalable architecture, lending itself to high-volume commercialization.

Space and Military Applications

Finally, a paradigm shift in design has been underway for modular, distributed approaches to DC-DC power conversion for low-medium-high power ranges. For example, the low-power (< 100 W) tracking, telemetry, control and receiver subsystems on the Lockheed Martin A2100 use high-frequency, flyback converters since tightly regulated and isolated supply voltages are desirable. On the other hand, medium-to-high power (1 - 10 kW) solid-stage power amplifiers (SSPA) utilize high-efficiency resonant converters. The A2100's power regulation unit PRU provides a regulated 70 V at 1 - 14 kW, while numerous point-of-load guidance, navigation, control, and auxiliary on-ship power converters may run off of 3, 5, 12, 24, or 28 V. The techniques presented in this thesis may give way to point-of-load DC-DC converters based the high-efficiency techniques developed.

Appendix A

Small Antenna Techniques

A.1 Introduction

Chaos theory is rich with examples in nature offering elegant solutions to engineering problems. The fundamental principle of *self-similarity* offers an explanation for why building blocks mimic their own shape in the construction they comprise. An object or phenomenon that displays self-similarity is called a fractal. In 1904 a Swedish mathematician, Helge von Koch, took a triangle and added a similar, smaller triangle to each of the sides of the first one. He continued iterating in this way, thus creating the Koch curve, as shown in Fig. A-1. The Koch curve brings up an interesting paradox. Each time new triangles are added to the

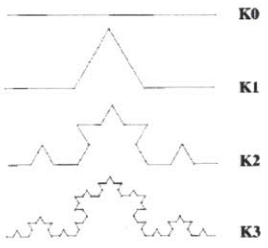


Figure A-1: Self-similarity and construction of the Koch fractal curve. Each iteration increases the length of the curve.

curve, the length increases. However, the inner area of the Koch curve remains less than the

area of a circle drawn around the original triangle. Essentially, it is a line of infinite length surrounding a finite area.

Much work has been devoted to exploiting self-similarity for the design of antennas. Fractal Antenna Systems, Inc. develops and manufactures fractal antennas for various military and commercial applications. The main benefits of fractal antennas is that they can alter the traditional relationships between bandwidth/multi-band, gain and size.

The purpose of this chapter is to begin an inquiry into the problem of designing efficient antennas within small form factors. One path is to consider going to extremely high carrier frequencies, because the wavelengths and therefore the antenna form factor shrinks. In [25] it is shown that the optimal frequency for bio-implant applications is in the 900 MHz - 2 GHz range. The great question is how can we minimize antenna size and still work in this spectral range? In this chapter, we propose exploiting fractal antenna patterns as a way of softening the tradeoff between small size and high radiation efficiencies. We discuss antenna design in the context of area constraints, a regime where fractal patterns thrive. The discussion proceeds as follows: Section A.2 and Section A.3 provide the context for the bio-implant application and the requisite brief overview of antenna theory. Challenges in building compact antennas, including fractal miniaturizing and input impedance matching are also discussed. Section A.4 presents experimental results for two fabricated loop antennas. Section A.5 presents an overview on fractal antenna theory and is followed by a comparison between two fractal patterns and microstrip antennas in Section A.6. We design a square-shape fractal shaped in the 2.4 GHz band to serve as a power and data link for a wireless ultracapacitor powered bio-implant chip.

A.2 Requirements for Bio-implant Antenna

Designing an antenna to be small compared to its operating wavelength is challenging. In Chapter 1 we described a medical implant whose largest dimension would be less than 1-2 cm. For the implanted use-model described, the major physical blocks hindering size reductions are the energy storage and data/power link. The whole implant package must therefore

be less than approximately $\frac{\lambda}{12}$. Furthermore, obtaining high efficiency and good matching simultaneously is difficult because of the additional real-estate required for a distributed matching network for coupling to a small output-resistance load to an efficient high input-resistance antenna. To solve the matching problem (at the expense of having low radiation resistance), we can integrate the impedance matching structures directly on the antenna structure for a conjugate match with the load impedance. While reducing antenna size comes at the expense of efficiency, it is possible to build a functional matched antenna for the application. The read-to-implant range need not be far, but for measurement convenience should be greater than the near-field power transfer methods (like using a transformer) alone could provide.

A.3 Basic Antenna Theory

As with any discussion concerning electromagnetic waves, we begin with the mentioning of Maxwell's equations. The important relations are given by

$$\nabla \times \mathbf{E} = -j\omega\mu\mathbf{H} \tag{A.1}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + j\omega\varepsilon\mathbf{E} \tag{A.2}$$

$$\nabla \bullet \mathbf{E} = \left(\frac{\rho}{\varepsilon}\right) \tag{A.3}$$

$$\nabla \bullet \mathbf{H} = 0 \tag{A.4}$$

Straightforward manipulations yield the well known wave-equation given by

$$\nabla^2\mathbf{E} + \omega^2\mu\varepsilon\mathbf{E} = j\omega\mu\mathbf{J} + \nabla\left(\frac{\rho}{\varepsilon}\right) \tag{A.5}$$

This equation links the radiated electric field directly to the source current density. Ignoring the $e^{j\omega t}$ factor and assuming an unbounded lossless medium, the solution to Eq. A.5 is given by

$$\mathbf{E}(\mathbf{r}) = -j\omega\mu \int_V \mathbf{J}(r') \frac{e^{-j\kappa\cdot|\mathbf{r}-\mathbf{r}'|}}{4\pi|\mathbf{r}-\mathbf{r}'|} dv' + \frac{1}{j\omega\varepsilon} \nabla \left(\nabla \bullet \int_V \mathbf{J}(r') \frac{e^{-j\kappa\cdot|\mathbf{r}-\mathbf{r}'|}}{4\pi|\mathbf{r}-\mathbf{r}'|} dv' \right) \tag{A.6}$$

where $\mathbf{r}$ is the distance vector from the origin to an observation point $\mathbf{r}'$, $\kappa = \frac{2\pi}{\lambda}$, and λ is the wavelength. κ is referred to as the wave number.

The result of Eq. A.6 succinctly summarizes antenna theory. However, except for some simple cases, Eq. A.6 is unwieldy and difficult to solve in order to obtain an analytical expression for the radiated electric field. Fortunately, there are two simple cases of great practical value. These two cases are the near-field and far-fields situations whereby, approximating the current density as $\mathbf{J} = \hat{z} I \Delta l$ such that $\Delta l \ll \lambda$, the radiated field can be simplified as

$$\begin{aligned} E_r &= 2\frac{I\Delta l}{4\pi}\eta\kappa^2 \cos\theta \left(\frac{1}{\kappa^2 r^2} - \frac{j}{\kappa^3 r^3} \right) e^{-j\kappa r} \\ E_\theta &= \frac{I\Delta l}{4\pi}\eta\kappa^2 \sin\theta \left(\frac{j}{\kappa r} + \frac{1}{\kappa^2 r} - \frac{j}{\kappa^3 r^3} \right) e^{-j\kappa r} \\ E_\phi &= 0 \end{aligned} \tag{A.7}$$

Evidently, $\kappa r = 1$, is an important point. For example, for $\kappa r > 1$, the ratio of $|\mathbf{E}/\mathbf{H}| = \eta$ is about 377 Ω (120π Ω) in free space. This and the trends $\mathbf{E}$ and $\mathbf{H}$ follow as functions of κ (fixed r) and κr are useful conclusions for RFID and electromagnetic compatibility.

A.3.1 Small Antennas

For RF and antenna engineers, the far-field ($r > 3\lambda$ for electrically small antennas [1]) is of most interest. In this region, $\kappa r \gg 1$, simplifying Eq. A.7 to

[1]The far-field condition ensures that the field is similar to that of a plane wave with the exception of the $1/r$ term. The far-field condition for an electrically large antenna ($D > \lambda$, where D is the maximum dimension) is given by

$$r > \frac{2D^2}{\lambda} \tag{A.8}$$

In general, an antenna is considered electrically small if its largest dimension is at or under $\lambda/10$. Thus, the condition $r > 3\lambda$ ensures that r is large enough to be considered far-field.

$$
\begin{aligned}
E_\theta &= \frac{jI\Delta l}{4\pi r}\eta\kappa \sin\theta e^{-j\kappa r} \\
E_r &\approx 0; \qquad E_\phi = 0
\end{aligned} \tag{A.9}
$$

(A.10)

and from Eq. A.1, the magnetic field becomes

$$
\begin{aligned}
H_\phi &= \frac{jI\Delta l}{4\pi r}\kappa \sin\theta e^{-j\kappa r} \\
H_r &= 0; \qquad H_\theta = 0
\end{aligned} \tag{A.11}
$$

A.3.2 Power Transmission

To compute the power flow density, or Poynting vector, we can take the cross product of the electric and magnetic fields. For better physical insight we consider a single point charge accelerating in a nonrelativistic point of reference. A fundamental consequence of Maxwell's equations, an accelerated charge leads to electromagnetic radiation which travels through space at the speed of light ($c = 1/\sqrt{\varepsilon\mu}$). Thus, applying an alternating current to a metal structure will give rise to radiating fields. Choosing the geometry of this structure for efficient and desirable radiation characteristics is the fundamental problem of antenna engineering. Following the exposition given in [65], we derive the electric field from an infinitesimal *Hertzian* dipole. The magnetic field can be obtained readily, as the quantity $\mathbf{E} \times \mathbf{B}$ is in the direction of propagation of the wave. Eq. A.12 expresses the electric field as given from an accelerating charge along the positive z-axis. The acceleration is the perpendicular component to the direction of viewing. That is, maximum radiation is detected in the x-y plane.

$$
E(r,t) = -\frac{qa(t')\sin\theta}{4\pi\varepsilon_o r c^2} \tag{A.12}
$$

If we imagine a small element of current on the z-axis, we find it is related to the product of charge and acceleration above simply as:

$$\dot{I}(t')\Delta l = qa(t') \tag{A.13}$$

In the *far-field*, the Poynting vector is in the direction of propagation, perpendicular to **E** and **B**. Therefore, we can apply the Larmor formula to calculate the total power radiated:

$$P(t) = \frac{q^2 a^2(t')}{6\pi\varepsilon_o c^3} \tag{A.14}$$

Upon solving for $a(t')$ from Eq. A.13 and plugging in (assuming a form $I = I_o e^{j\omega t'}$), Eq. A.14 becomes:

$$P(t) = \frac{\dot{I}(t')^2 \Delta l^2}{6\pi\varepsilon_o c^3} = \frac{(\omega\Delta l)^2 I_o^2 \sin^2\omega t'}{6\pi\varepsilon_o c^3} \tag{A.15}$$

Taking the time average and rearranging, noting that $\frac{\omega}{c} = \frac{2\pi}{\lambda}$ yields:

$$P_{\text{avg}}(t) = \frac{1}{2} I_o^2 \overbrace{\left[80\pi^2 (\frac{\Delta l}{\lambda})^2\right]}^{\text{Radiation Resistance}} = \frac{1}{2} I_o^2 R_{\text{rad}} \tag{A.16}$$

Eq. A.16 provides an interesting insight. The radiated power can be viewed as being directly proportional to the square of the input current by the parameter R_{rad}, the *radiation resistance*. It represents how much radiation can be dissipated (or "lost") into space for a given input current. This quantity is an essential link between the properties of an antenna as a circuit element and a radiating element. One sees that if the length is much smaller than a wavelength, the radiation resistance is very small. This fundamental insight means electrically small antennas are necessarily inefficient radiators and is driver for seeking geometries that maximize physical length within a fixed area.

Other important antenna parameters include the gain and the directivity. Directivity in a given direction is defined as:

$$D = 4\pi \frac{P(\theta,\phi)}{P_{\text{total}}}, \tag{A.17}$$

where P_{total} is the total integral over a sphere of the power per solid angle:

$$P_{\text{total}} = \int_0^{4\pi} P(\theta, \phi) \; d\Omega \tag{A.18}$$

Gain is defined as the product of directivity and an efficiency factor. Thus the maximum possible gain is equal to the directivity:

$$G = \eta_{\text{eff}} \cdot D \tag{A.19}$$

A.3.3 Circuit Model for Antennas

The function of the antenna is to transition radio waves from electromagnetic media to voltage/current on a transmission line. Adopting this definition allows us to model the antenna, using lumped elements, as a load to a transmission line. Such a model is shown in Fig. A-2 [66]. Here R_{rad} models the power radiated away in a transmitted wave as described

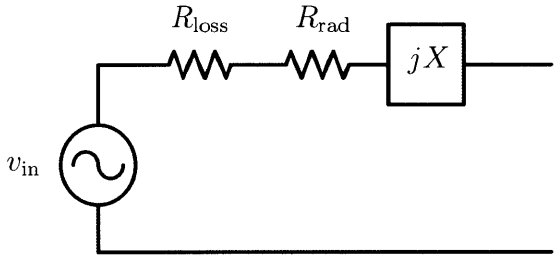


Figure A-2: Equivalent circuit model for an antenna. R_{loss} captures the power dissipated as heat, jX represents the reactive component, and the radiation resistance, R_{rad}, captures the effectiveness of the antenna and power transmitted into space.

in the previous section, R_{loss} models the power loss to heat in the antenna conductors, and jX models the energy stored in the antenna's near field (i.e., capacitor or inductor).

Since what we desire is to maximize the amount useful radiated power and minimize the power loss to heat dissipation, the antenna radiation efficiency is defined as

$$\eta_r = \frac{P_{\text{t}}}{P_{\text{in}}} = \frac{R_{\text{rad}}}{R_{\text{rad}} + R_{\text{loss}}} \tag{A.20}$$

From the matching point of view, we need to match R_{rad} with the impedance of the line and, ideally, $R_{\text{loss}} = 0$. The matching efficiency can be defined as

$$\eta_m = \frac{P_{\text{in}}}{P_{\text{s}}} = 1 - |\Gamma|^2 \tag{A.21}$$

where P_{s} is the source power and Γ is given by

$$\Gamma = \frac{Z_{\text{A}} - Z_o}{Z_{\text{A}} + Z_o}. \tag{A.22}$$

In Eq. A.22 Z_{A} is the antenna impedance and Z_o is the characteristic impedance of the transmission line. Multiplying these two expressions gives some idea of the total efficiency which is defined as the power radiated into space divided by the power output by source:

$$\begin{aligned} \eta_{\text{tot}} = \frac{P_{\text{t}}}{P_{\text{s}}} &= \eta_{\text{m}} \cdot \eta_{\text{r}} \\ &= (1 - |\Gamma|^2) \frac{R_{\text{rad}}}{R_{\text{rad}} + R_{\text{loss}}} \end{aligned} \tag{A.23}$$

For simplicity, consider the case where both Z_{A} and Z_o are purely real, and assume $Z_{\text{A}} = R_{\text{rad}} + R_{\text{loss}}$. With this simplification, a plot of Eq. A.23 is shown in Fig. A-3 for different values of the characteristic impedance. The plot shows efficiency versus a sweep of radiation resistance. We can see from this figure that matching efficiency is essential for efficient power transfer. The ideal radiation resistance for maximum efficiency is only slightly higher than the characteristic impedance of the the transmission line.

Finally, an alternative parameter to characterize antenna radiation efficiency is the quality factor, Q, defined as

$$Q = \frac{X}{R_{\text{rad}} + R_{\text{loss}}} \tag{A.24}$$

Poor efficiency results from low radiation resistance and high Q. The role of Q is discussed further in Section A.5

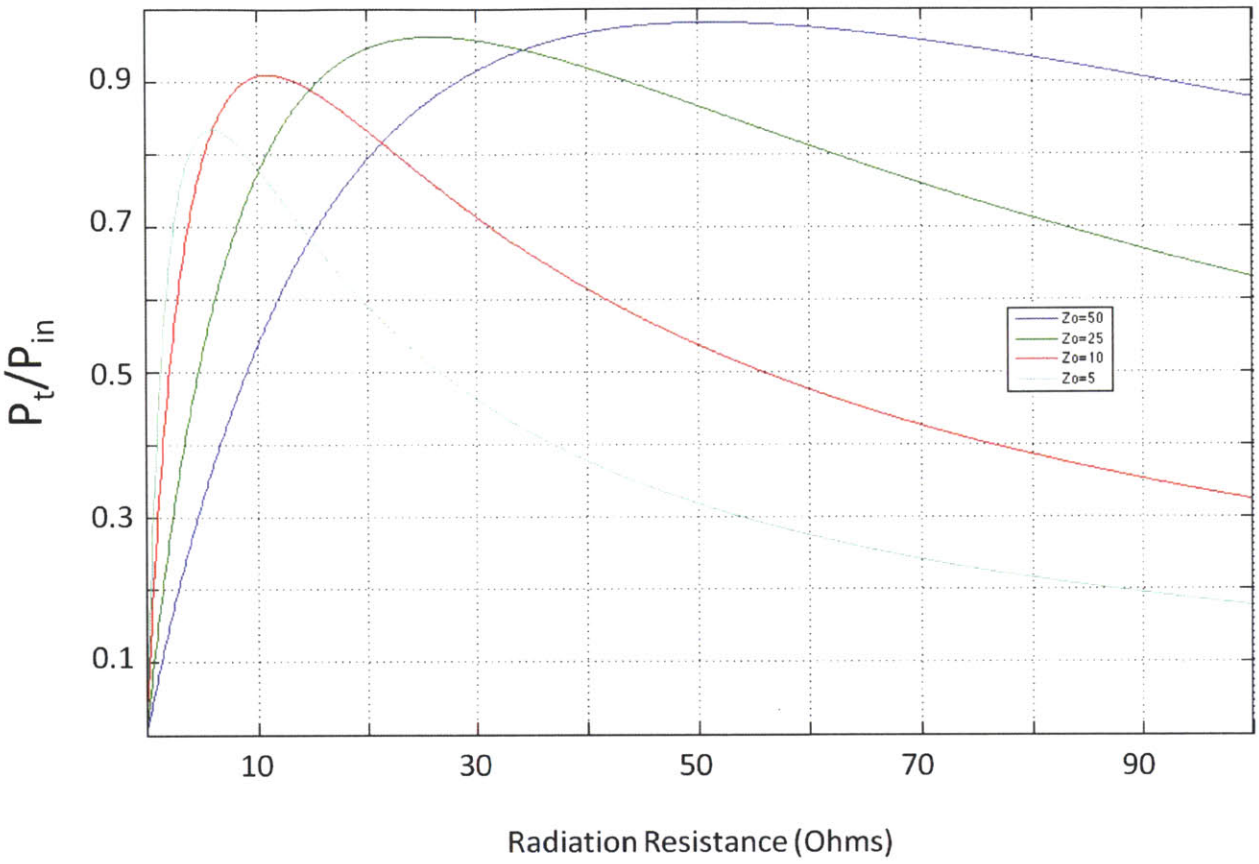


Figure A-3: Antenna efficiency ($\eta_{\text{tot}} = \frac{P_t}{P_s}$) as a function of radiation resistance for several values of characteristic impedance Z_o. For simplicity, Z_A and Z_o are assumed real.

A.3.4 Matching Networks

As discussed in Section A.3.3, we can view an antenna as a reactance in series with a resistor. For maximum power transfer, the impedance of this structure should be equal to the complex conjugate of the load. However, a perfect match can only occur at one frequency. To tolerate environmental changes, we would like to maintain a match over a range of bandwidths [67]. What is the maximum bandwidth achievable? An analysis of this problem is provided in [65, 67]. The Bode-Fano criterion can be written as:

$$\int_0^\infty \ln\left(\frac{1}{|\Gamma(\omega)|}\right) d\omega \leq \frac{\pi\omega_o}{Q_L} \tag{A.25}$$

We assume narrowband operation where Q_L is almost constant over the bandwidth of interest, a reasonable assumption. Eq. A.25 expresses the fundamental gain-bandwidth-like constraint of the antenna-matching problem. For a given load, if a "high gain" matching network is desired (one that realizes a very low Γ), it can only be realized over a narrow bandwidth.

A.4 Prototype Measurement Results

A.4.1 PCB Loop Antenna

Fig. A-4 shows a loop antenna used to benchmark measurements against basic fractal patterns. The size is 20 mm on a side, and the thickness of the wire is 0.3 mm. The board is FR4, and the antenna is built on a layer embedded in the board for improved matching to a 50 Ω source. The radiation pattern of this structure at 2.4 GHz, in roughly the same orientation

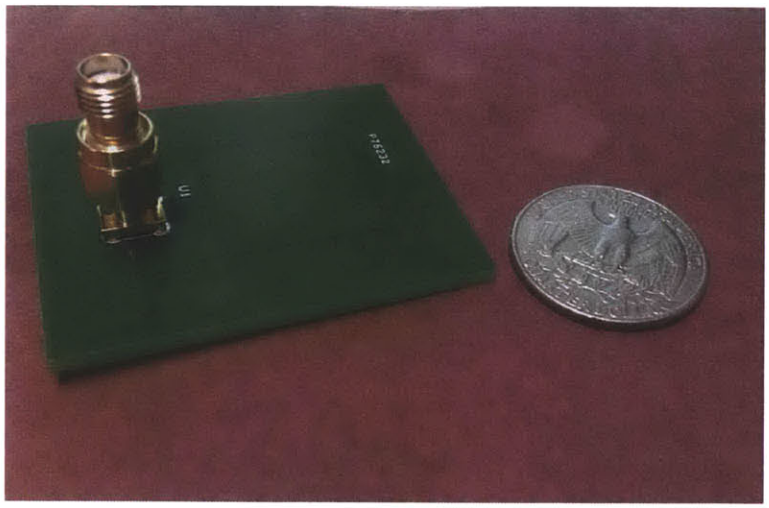


Figure A-4: Simple PCB loop antenna used for benchmarking.

as the image above is shown in Fig. A-5. A comparison of simulated and measured S_{11} are shown in Fig. A-6. The S_{11} reflection coefficient is used to characterize a match with a 50 Ω source. We observe that the loop antenna matches well at approximately 2.55 GHz, and that

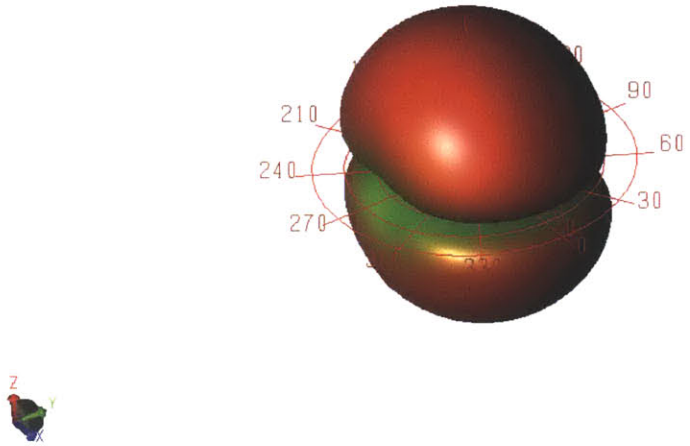


Figure A-5: Simulated far-field radiation pattern of PCB loop antenna of Fig. A-4 at 2.4 GHz.

the overall measured S_{11} is right-shifted by approximately 100 MHz. Keeping in mind that an integrated chip (load) would appear as a small resistor in series with some capacitance this antenna will require a matching network.

In order to measure input impedance, the reflection coefficient was measured with both magnitude and phase components. Shown in Fig. A-8 is a measurement of S_{11} in the complex plane. The antenna was simulated with the through-holes on the PCB board. The effect of the SMA connector was not included. Additional parasitics were also omitted. The network analyzer was set to zero electrical delay because the SMA fixture was approximately the length of the calibration connector, which is the default calibration plane. The reflection coefficient directly relates to the input antenna impedance as shown in Fig. A-9 and Fig. A-10.

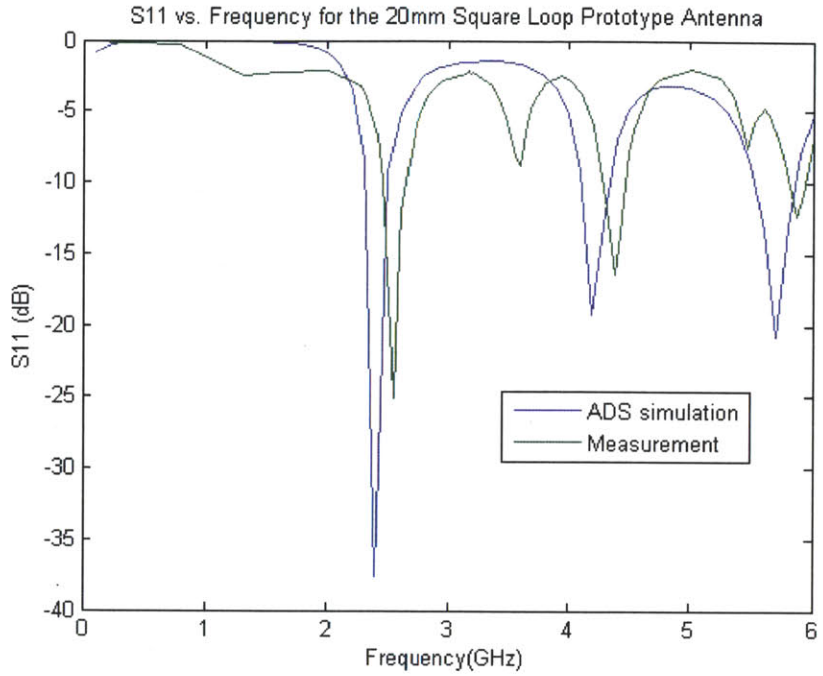


Figure A-6: PCB loop antenna simulation versus measurement of reflection coefficient (S_{11}) magnitude. S_{11} is used to characterize a match with a 50 Ω source.

A.4.2 Load Input Impedance

A setup for measuring the input impedance of a 5-stage, four-transistor synchronous rectifier test chip discussed in Chapter 5 is shown in Fig. A-11. An electrical delay of approximately -200 ps was used to subtract the length of the SMA cable from the calibration plane. In this case, the SMA connector is not as long as the antenna fixture-SMA connector to justify 0 ps electrical delay as used before. It should be noted that these measurements are approximate because of the 1 cm distance between chip and SMA connector. This could be de-embeded using simulation-based techniques as in [4]. This is particularly important when a load chip is directly connected to an antenna.

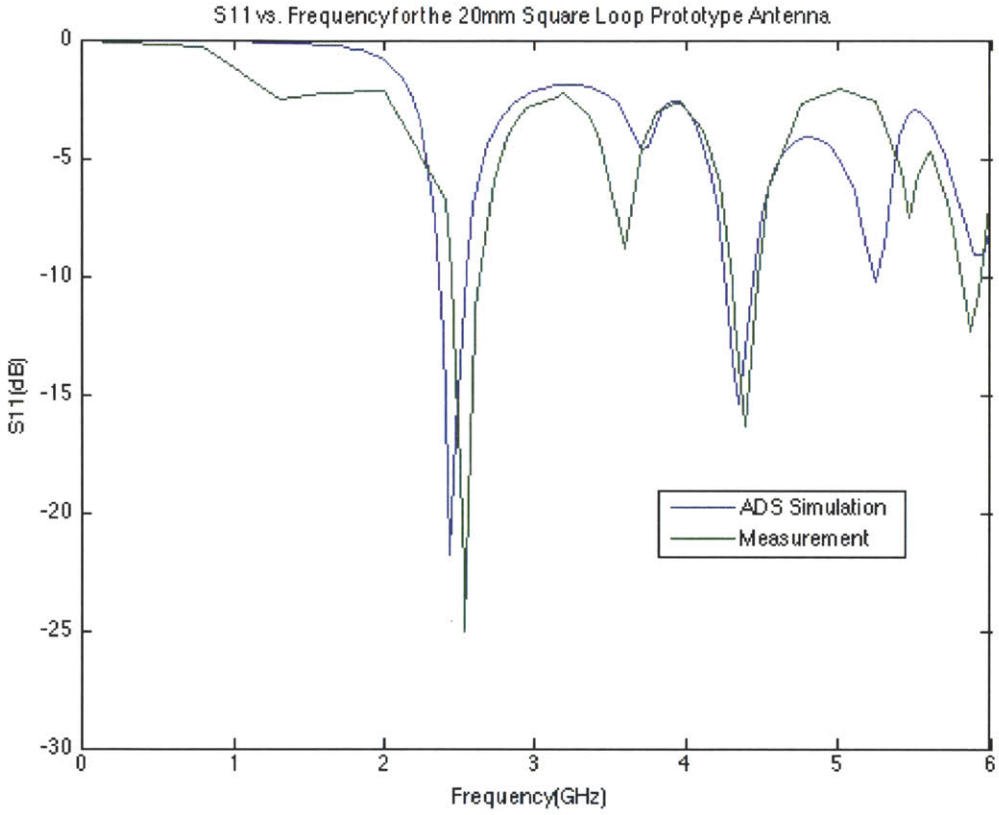


Figure A-7: PCB loop antenna simulation versus measurement of reflection coefficient (S_{11}) magnitude including PCB-via effects

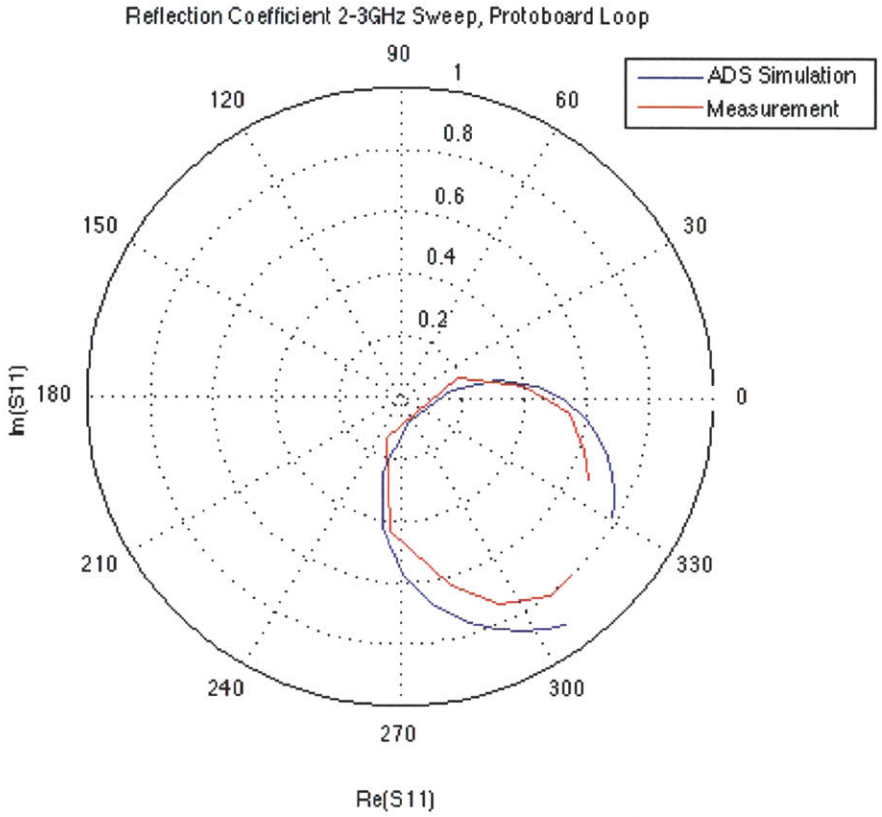


Figure A-8: The complex plane S_{11} plot over a 2-3 GHz sweep used to measure the input impedance.

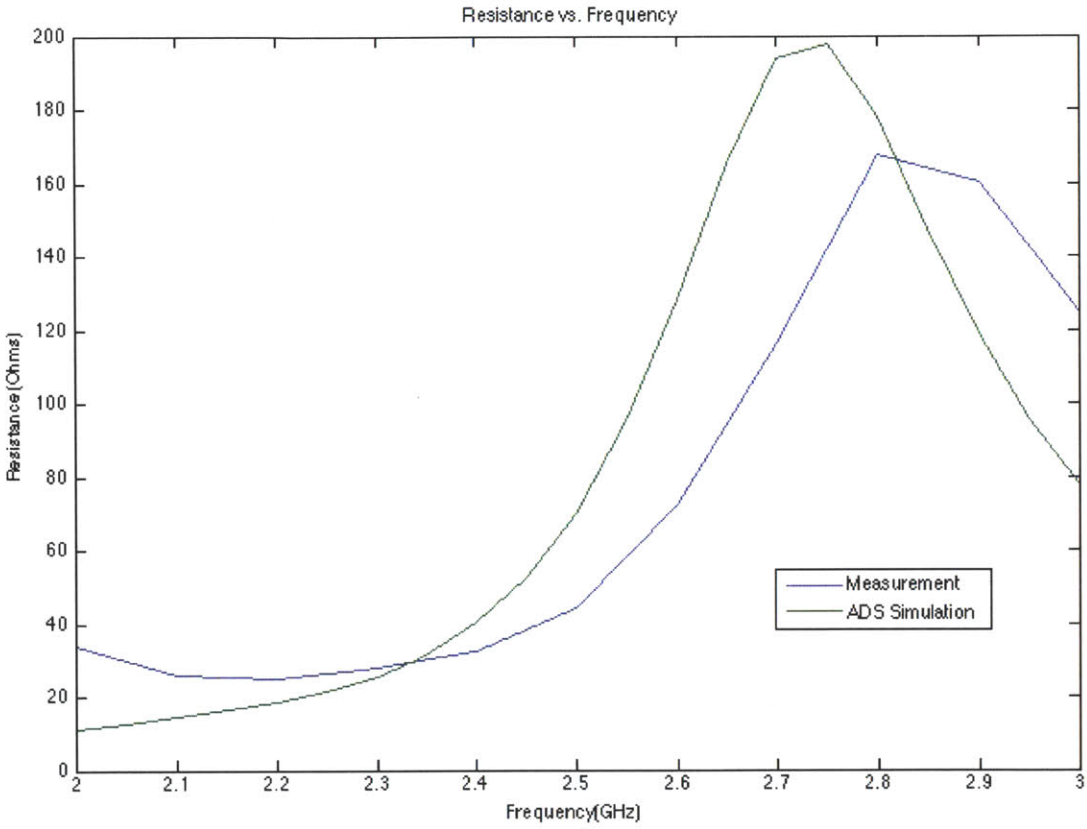


Figure A-9: PCB loop input resistance versus frequency.

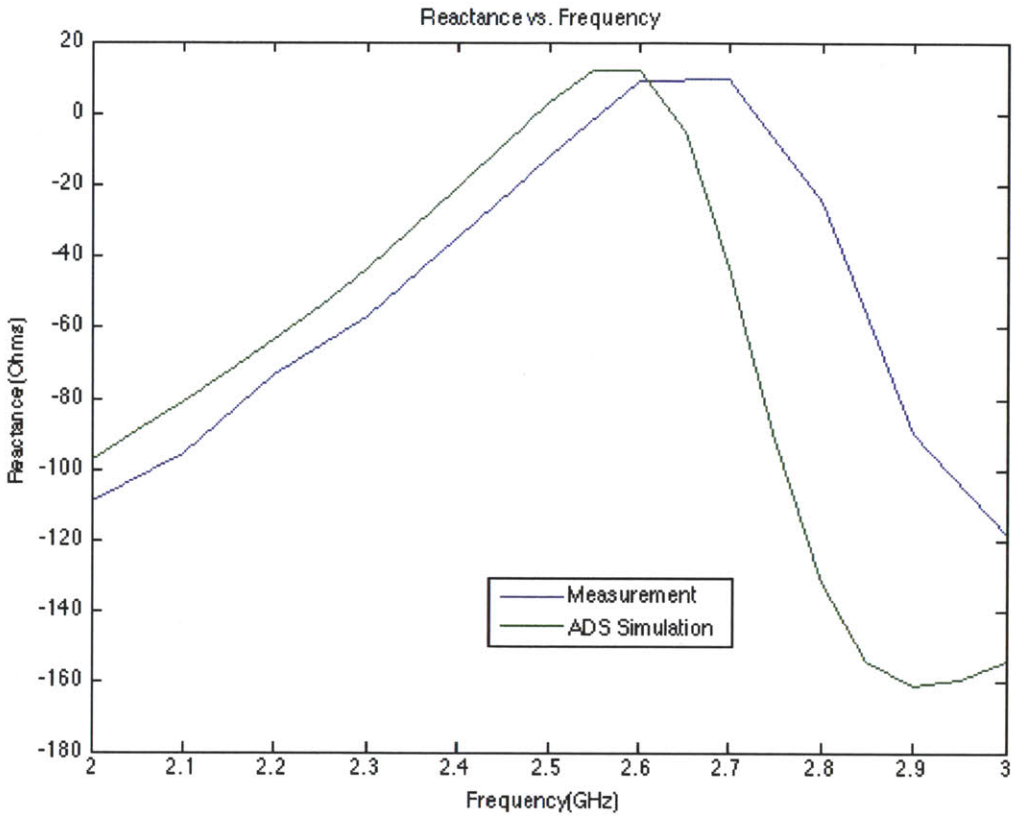


Figure A-10: PCB loop reactance versus frequency.

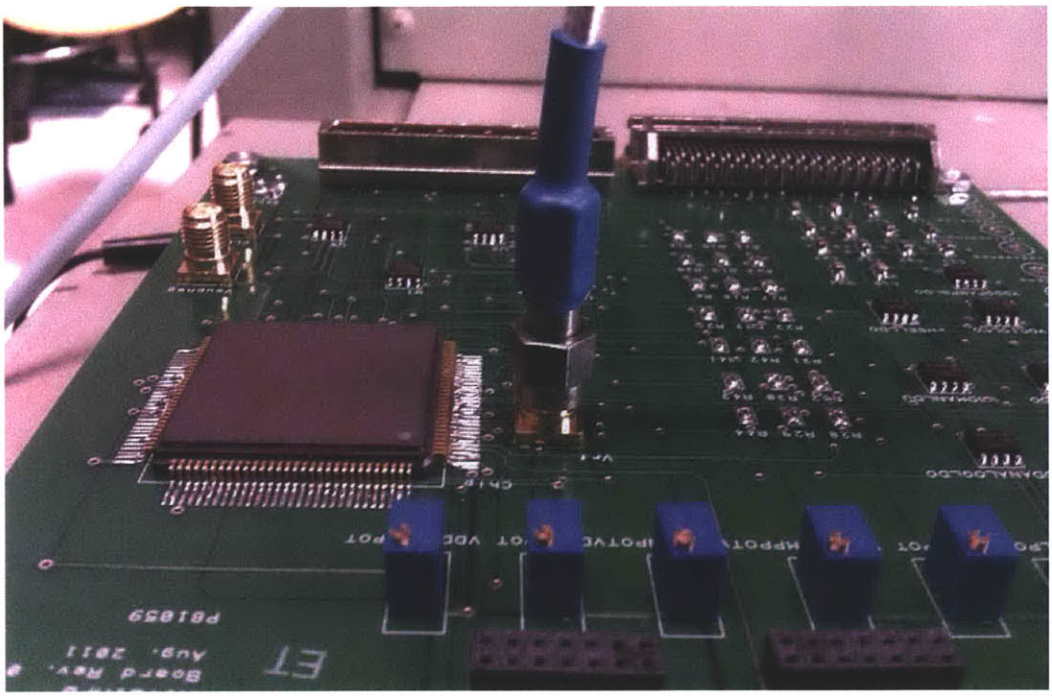


Figure A-11: Chip test-board and impedance measurement set-up. The SMA connector is located approximately 1 cm away from the chip input to minimize PCB trace parasitics. The measurement is calibrated to account for the length of the SMA cable. Additional de-embedding techniques are discussed in [4].

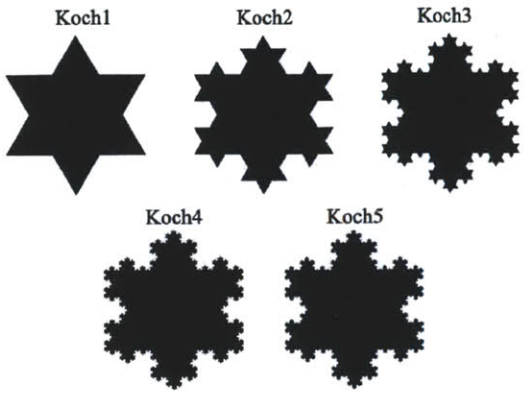
A.5 Fractal Antennas

A fractal consists of a geometric shape possessing the property of self-similarity. In other words, zooming at any level reproduces the geometry of the whole shape. The implication is that the perimeter of such a shape is theoretically infinite. The self-similarity property of fractal antennas allow for the compact design of multiband or wideband antennas. To gain physical insight, consider optical frequencies where the angular resolving power of a lens or mirror system increases with the size of the aperture. Apertures much smaller than a wavelength necessarily have poor resolving power. The analogy is directly applicable to microwave antennas, and a limit for the maximum gain exists for a given antenna size. Thus, the problem of antenna scaling is an engineering trade-off between gain and size, and benefits fractal geometries may offer cannot surmount natural limits.

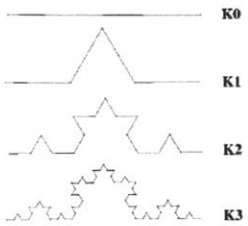
The benefits of fractal geometry as applied to loop and wire-type antennas are based on the observation that one can lengthen an antenna without increasing its overall dimensions. This could be useful in applications where the available space is limited, such as in bio-implants. After several iterations, small kinks and turns characteristic of fractal geometries are very small compared with the wavelength, and thus do not affect the antenna resonant frequency and performance. However, since extending beyond three iterations is impractical, these antennas have been shown to have similar characteristics with meander lines.

A nice feature about fractal geometries is that, albeit complex, they can be analytically described. A set of simple rules when applied iteratively can lead to complicated shapes. Since computational tools have proven to be extremely useful for electromagnetic simulations, the fractal definition would be interesting for optimization work. For example, we could modify a simple generator function with only a few lines of code to create many different geometries [5].

Fractal antennas' predecessor, the log-periodic antenna, has been around since the 1950s. The log-periodic antenna is similar in configuration to the Yagi-Uda antenna, but the log-periodic antenna offers a wider bandwidth due to its self-similarity attribute. Fig. A-12 show a patch and dipole renditions of Koch-based fractal antennas.



(a) Fractal patch antenna obtained by replacing each side of an equilateral triangle by a Koch curve iteratively [68].



(b) Various iterations of a Koch curve. Each additional iteration physically increases the length of the curve.

Figure A-12: Patch-based and dipole Koch-based fractal antennas geometries.

A fundamental limitation of antenna design is the resulting inefficiency in the small antenna limit (i.e., when the antenna is several times smaller than the operating wavelength). As discussed in Section A.3.3, this translates to a decrease in radiation resistance and an increase in reactive energy storage in the near-field region. These physical phenomena make small antennas difficult to match all the while displaying high Q [5]. In 1948, Chu's research at M.I.T. and expression of radiated fields in spherical modes yielded a lower bound for the achievable Q [69] expressed as

$$\min(Q) = \frac{1}{k^3 a^3} + \frac{1}{ka} \tag{A.26}$$

where $a = \lambda/2\pi$ and relates to the smallest antenna that fits within a sphere of radius a, and k is the wave number. Eq. A.26 is a theoretical fundamental limit, but in practice, $Q = 1.5 \cdot Q_{\min}$ is among the lowest reported.

Much of the appeal for turning to fractal geometries is that numerical and experimental data suggest that as the number of iterations increase (i.e., the shape approaches an ideal fractal), the Q of the antenna approaches the fundamental limit established by Chu. It is easy to see that for the Koch curve in Fig. A-12(a), the physical perimeter increases

geometrically as follows [68]

$$l_k = 3a \cdot \left(\frac{4}{3}\right)^k \tag{A.27}$$

since the physical length of each side (Fig. A-12(b)) increases as $(4/3)^k$ at each iteration. In [68], a 44% decrease in area is achieved for the Koch patch compared to the smallest circular patch that circumscribes it [2]. That is, with each iteration the Koch patch fundamental mode resonance is at longer wavelengths than the equivalent Euclidean patches. The reduction in resonant frequency may be attributed to the longer distance the electrical current must propagate through. This property suggests resonance below the small antenna limit for fractal antennas.

A limit to the gains afforded by Eq. A.27 does exist. This can be seen from Fig. A-13.

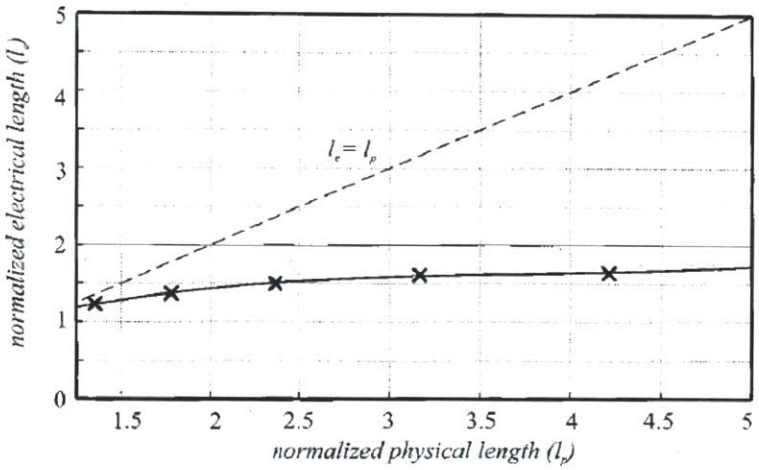


Figure A-13: Experimentally, [5] finds that a limit to the electrical length of a fractal exists and poses a limit to the marginal gains after a few iterations.

[2]The drawback is a degradation in Q by 17%. Clearly, a trade-off between bandwidth and area will exist for a particular application

A.6 Comparison Between Geometries

The previous sections discussed the tradeoffs between bandwidth, center frequency, and physical geometry. Section A.3.2 showed that the radiation resistance presents a fundamental limit on power transmission due to the physical length of a geometry. Section A.5 showed that it is possible to obtain additional gains physical length within an area budget in order to increase the equivalent electrical length of an antenna. In this section we provide comparisons between two common geometries and two fractal shapes. For ease of comparison, we restrict the dimensions to 6-9 mm per side for each of the geometries.

A.6.1 Loop and patch antenna examples

Loops are a simple and versatile wire-type antenna. Fig. A-14 shows a 6 mm x 6 mm square loop. For an electrically small loop, the voltage is small and the current is large. This

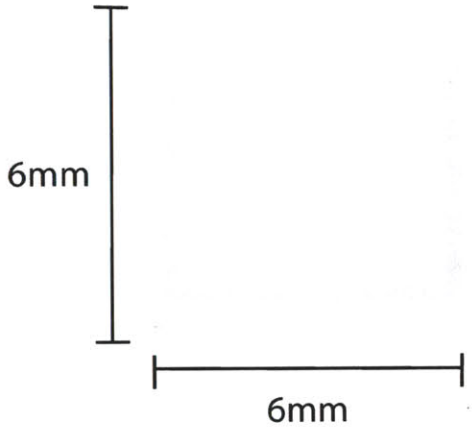


Figure A-14: Small loop antenna for comparison against fractal geometry in Section A.6.2.

results in a small input impedance. Generally, speaking loops are low profile and present a well-controlled radiation pattern [70]. The first resonance for the loop of diameter D is given approximately as

$$f_o = \frac{0.98c}{2\pi D} \tag{A.28}$$

For the loop of Fig. A-14 this yields $f_o = 7.8$ GHz, lying comfortably in the small antenna regime ($C = \pi D < \frac{\lambda}{3}$). Fig. A-15 shows the S_{11} plot for the loop antenna of Fig. A-14. The performance would not be adequate for many applications where higher efficiency is

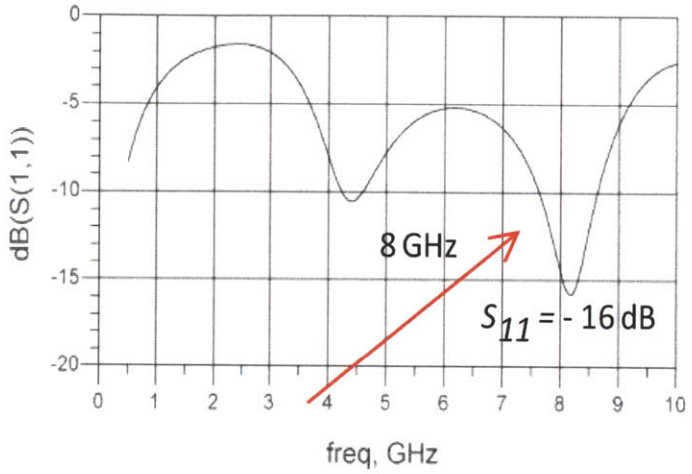


Figure A-15: Simulated S_{11} for small loop antenna of Fig. A-14. The poor radiation efficiency would not be adequate for many applications.

necessary, and a resonance better than -20 dB at a standard FCC frequency is desirable.

For purposes of comparison, Fig. A-16 shows a 6 mm x 6 mm patch (microstrip) antenna. A patch antenna consists of a metal patch on a substrate on a ground plane. This type of antenna is low-profile, simple and cheap to manufacture using modern printed-circuit technology. It is versatile in terms of resonant frequency, input impedance, radiation pattern, and polarization. However, as can be seen from the corresponding S_{11} plot shown in Fig. A-17, the major disadvantages of this type of antenna includes low efficiency (conducting, dielectric and surface wave losses), low power-handling capability, and relatively narrow bandwidth [70]. Despite the shortcomings, patch antennas are the most popular type of printed antenna for their simplicity and robustness. The radiation impedance of a patch at the edge can be approximated as

$$Z_{\text{rad}} \approx 90\frac{\varepsilon_r^2}{\varepsilon_r - 1}\left(\frac{L}{W}\right)^2 \Omega \tag{A.29}$$

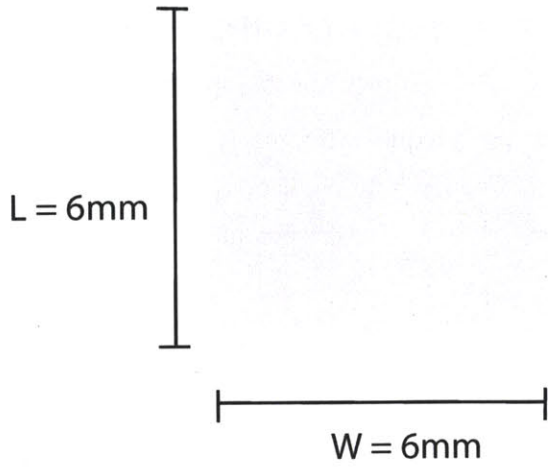


Figure A-16: Small patch antenna for comparison against fractal geometry in Section A.6.2.

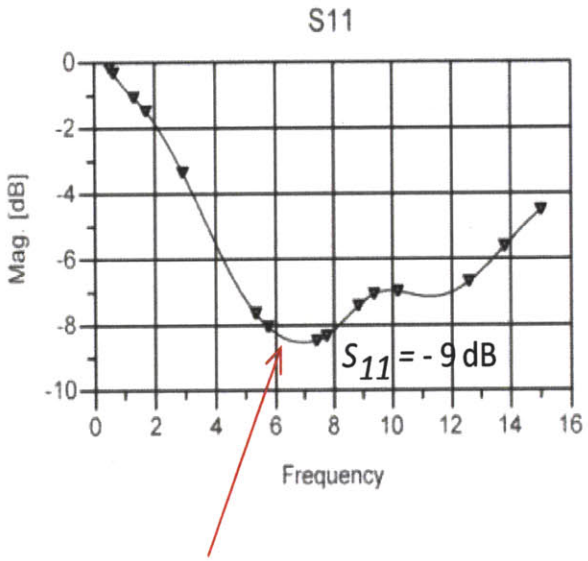


Figure A-17: Simulated S_{11} for small patch antenna of Fig. A-16. The patch has worse radiation efficiency but exhibits resonance of a larger structure resulting from fringing effects.

Interestingly, because of fringing effects the patch antenna behaves like a larger structure electrically. This affords the patch structure a slightly lower resonant frequency than its loop

counterpart, which can be given as follows [70]

$$f_o = \frac{1}{2L_{eff}\sqrt{\varepsilon_{eff}}\sqrt{\varepsilon_0\mu_0}} \tag{A.30}$$

L_{eff} is the effective length of the patch and ε_{eff} is the effective (relative) permittivity and given as follows

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{1 + 12d/W}} \tag{A.31}$$

where d is the thickness of the substrate. Larger d/W ratios yield higher bandwidth but at the expense of higher resonant frequency.

A.6.2 Fractal pattern examples

In this section we investigate the effects of fractal patterns for the same physical dimensions presented in Section A.6.1. Fig. A-18 is $k = 2$ fractal pattern on each side of the loop antenna of Fig. A-14 where the repeated shape is a square. The fractal shape is drawn within the containing box of 6 mm x 6 mm. Fig. A-19 plots the S_{11} and shows a narrowband resonance at 2.4 GHz. According to Eq. A.27, the resulting physical length increases by $(3 \cdot \frac{D}{2}\frac{4}{3}^k) = 2.65 \cdot D$. There is no simple mathematical expression for the radiated field from the fractal shape shown, and computer simulations are really the best choice if a 3D radiation pattern is desired. Compared to the simple loop, we can make a few observations. First, the bandwidth achieved by the fractal pattern versus the loop antenna, which clearly demonstrates the Bode-Fano tradeoff between gain and bandwidth. Second, the first resonance of the fractal shape occurs at 2.4 GHz compared to 4.4 GHz, or a frequency that is 2.3× lower than the first resonance of the loop. This is approximately consistent with the increased physical length. In practice, the asymptotic limit for the electrical length shown Fig. A-13 would dominate. However, the existence of such an asymptotic limit does not have a formal proof and even numerical or empirical determination is difficult. The exponential growth of the number of segments as the fractal iteration increases leads to a numerical problem for a even relatively

small number of iterations. Moreover, manufacturing limitations pose limitations to the realizable number of iterations.

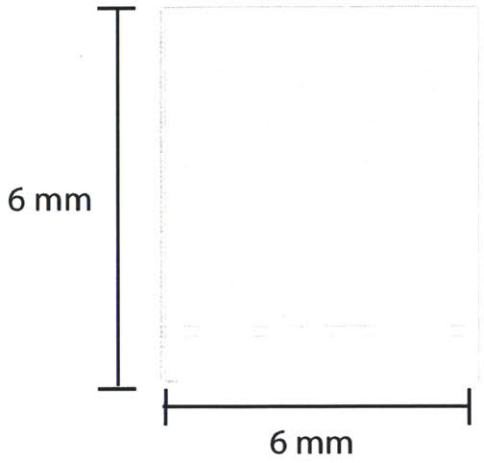


Figure A-18: A $k = 2$ fractal loop pattern with the same dimensions as Fig. A-14. The fractal pattern increases the physical length by 2.65×.

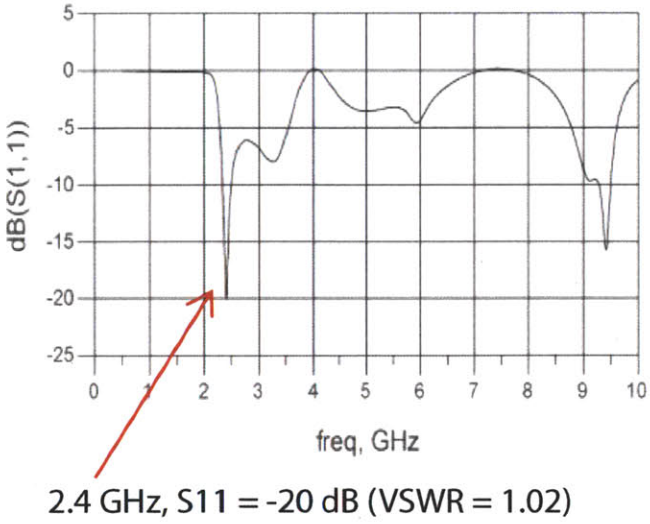


Figure A-19: Simulated S_{11} for fractal pattern of Fig. A-18. Compared to the simple loop geometry, the fractal pattern exhibits better radiation efficiency at a lower resonance that is consistent with an increased physical length.

A final observation can be made by studying Fig. A-20 and the corresponding multi-

bandedness plotted in Fig. A-21. We can see that the fractal pattern of Fig. A-20 is identical to Fig. A-18 except that the shape is inside-out. Hence, the footprint of the inside-out fractal pattern is larger, but more interestingly we observe four resonance frequencies. This is characteristic of fractal patterns and can be understood by modeling the geometry as an ideal distributed network with complex fringing effects governing the dynamics between the fractal features. This has the effect of making fractal patterns higher order than their loop or patch counterpart. The effect of high-order localized modes in fractal boundaries is described by the physics of disordered materials and a study of the effects on current distribution due to added irregularity is discussed in [68]. It is shown that the current is highly localized in more regions, which has the effect of improving directivity.

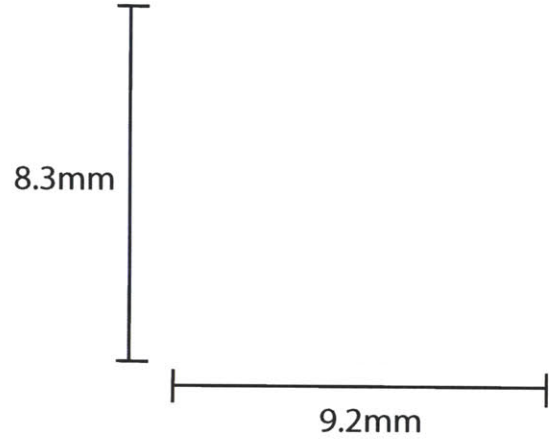


Figure A-20: Variation of fractal pattern of Fig. A-18 where the pattern is made on the outer perimeter.

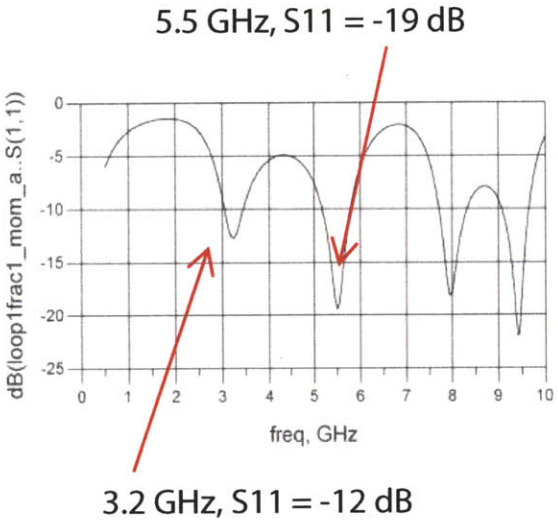


Figure A-21: Simulated S_{11} for inside-out fractal pattern of Fig. A-20. This pattern exhibits four resonance frequencies, which is characteristic of fractal antennas due to high-order localized modes in fractal boundaries.

A.7 Summary

In this Appendix chapter we provided basic relations for antenna design. We provided a simple circuit model for representing antennas for purposes of designing a matching network and presented the tradeoffs between bandwidth, gain, and efficiency, and how the physical geometry presents fundamental limits to the smallest antenna size. We saw that simultaneously obtaining high efficiency and good matching is difficult because of the additional real-estate required for a distributed matching network. The Bode-Fano criterion provides the fundamental gain-bandwidth constraint of the antenna-matching problem. The fundamental principle of self-similarity was introduced that gave rise to the study of fractal antenna patterns. We observed that we can exploit geometric properties of fractals to design and develop a PCB prototype fractal antenna to demonstrate size reductions as compared to Euclidean geometries. The self-similarity property of fractal antennas allow for the compact design of multi-band or wide-band antennas as was demonstrated with the design and performance of two fractal antenna patterns presented. We have shown that the benefits of fractal geometries are based on the observation that one can lengthen an antenna without increasing its overall encompassing areas. This could be useful in many applications such as bio-implants.

Bibliography

[1] J. Schindall, "The charge of the ultra - capacitors," *IEEE Spectrum*, Nov. 2007.

[2] NESSCAP. (2008) Nesscap ultracapacitor technical guide. [Online]. Available: http://www.nesscap.com/

[3] R. M. Hoque and S. S. Ang, "A cmos under-voltage lockout circuit," in *Proc. of WCECS*, Oct. 2008.

[4] S. Mandal and R. Sarpeshkar, "Low-power cmos rectifier design for rfid applications," *Circuits and Systems I, IEEE Trans. on*, 2007.

[5] C. P. Baliarda, J. Romeu, and A. Cardama, "The koch monopole: a small fractal antenna," *Antennas and Propagation, IEEE Transactions on*, vol. 48; 48, no. 11, pp. 1773–1781, 2000, iD: 1.

[6] X. Fang, N. Kutkut, J. Shen, and I. Batarseh, "Ultracapacitor shift topologies with high energy utilization and low voltage ripple," in *Telecommunications Energy Conference (INTELEC), 32nd International*, june 2010, pp. 1 –7.

[7] Medsmart. [Online]. Available: http://www.alignmap.com/noncompliance-fact-fiction/costs.com

[8] Thomson and Reuters. (2009) Medication non-compliance estimated to result in more than 300,000 deaths each year. [Online]. Available: http://www.reuters.com.

[9] S. R. IX, "The forgetful patient: The high cost of improper patient compliance," 1987.

[10] "A study of long-term care in oregon with emphasis on the elderly," Oregon Department of Human Resources, March, 1981.

[11] Medsmart. [Online]. Available: http://www.healthyagingsolutions.com

[12] Y.-H. Lin, I.-C. Jan, P.-I. Ko, Y.-Y. Chen, J.-M. Wong, and G.-J. Jan, "A wireless pda-based physiological monitoring system for patient transport," *Information Technology in Biomedicine, IEEE Transactions on*, vol. 8, no. 4, pp. 439–447, Dec. 2004.

[13] E. Van Someren, B. Vonk, W. Thijssen, J. Speelman, P. Schuurman, M. Mirmiran, and D. Swaab, "A new actigraph for long-term registration of the duration and intensity of tremor and movement," *Biomedical Engineering, IEEE Transactions on*, vol. 45, no. 3, pp. 386–395, March 1998.

[14] M. Ahmadi and G. Jullien, "A wireless-implantable microsystem for continuous blood glucose monitoring," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 3, no. 3, pp. 169–180, June 2009.

[15] J. Bohorquez, A. Chandrakasan, and J. Dawson, "A 350 *mu* w cmos msk transmitter and 400 *mu*w ook super-regenerative receiver for medical implant communications," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 4, pp. 1248–1259, April 2009.

[16] M. Roham, D. Daberkow, E. Ramsson, D. Covey, S. Pakdeeronachit, P. Garris, and P. Mohseni, "A wireless ic for wide-range neurochemical monitoring using amperometry and fast-scan cyclic voltammetry," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, no. 1, pp. 3–9, March 2008.

[17] L. Wong, S. Hossain, A. Ta, J. Edvinsson, D. Rivas, and H. Naas, "A very low-power cmos mixed-signal ic for implantable pacemaker applications," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 12, pp. 2446–2456, Dec. 2004.

[18] S. Mandal and R. Sarpeshkar, "Power-efficient impedance-modulation wireless data links for biomedical implants," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, no. 4, pp. 301–315, Dec. 2008.

[19] S. O'Driscoll, A. Poon, and T. Meng, "A mm-sized implantable power receiver with adaptive link compensation," in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, Feb. 2009, pp. 294–295,295a.

[20] N. Lajnef, N. Elvin, and S. Chakrabartty, "A piezo-powered floating-gate sensor array for long-term fatigue monitoring in biomechanical implants," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 2, no. 3, pp. 164–172, Sept. 2008.

[21] S. Meninger, T. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J. Lang, "Vibration-to-electric energy conversion," in *Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on*, 1999, pp. 48–53.

[22] R. Amirtharajah, J. Wenck, J. Collier, J. Siebert, and B. Zhou, "Circuits for energy harvesting sensor signal processing," in *Design Automation Conference, 2006 43rd ACM/IEEE*, 0-0 2006, pp. 639–644.

[23] X. Cao and Y.-K. Lee, "Design and fabrication of mini vibration power generator system for micro sensor networks," in *Information Acquisition, 2006 IEEE International Conference on*, Aug. 2006, pp. 91–95.

[24] U. Bartsch, A. Trautmann, P. Ruther, J. Gaspar, and O. Paul, "Electrostatic transducers for micro energy harvesting based on soi technology," in *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, June 2007, pp. 141–144.

[25] A. Poon, S. O'Driscoll, and T. Meng, "Optimal frequency for wireless power transmission into dispersive tissue," *Antennas and Propagation, IEEE Transactions on*, vol. 58, no. 5, pp. 1739 –1750, may 2010.

[26] D. Pimentel and P. Musilek, "Power management with energy harvesting devices," in *Electrical and Computer Engineering (CCECE), 2010 23rd Canadian Conference on*, may 2010.

[27] V. Karam, P. H. R. Popplewell, A. Shamim, J. Rogers, and C. Plett, "A 6.3 GHz BFSK Transmitter with On-Chip Antenna for Self-Powered Medical Sensor Applications," *RFIC 2007.*

[28] V. L. Pushparaj, M. M. Shaijumon, A. Kumar, S. Murugesan, L. Ci, R. Vajtai, R. J. Linhardt, O. Nalamasu, and P. M. Ajayan, "Flexible energy storage devices based on nanocomposite paper," *PNAS*, pp. 0 706 508 104+, August 2007. [Online]. Available: http://dx.doi.org/10.1073/pnas.0706508104

[29] M. Marei, S. Samborsky, S. Lambert, and M. Salama, "On the characterization of ultracapacitor banks used for hevs," in *Vehicle Power and Propulsion Conference, 2006. VPPC '06. IEEE*, Sept. 2006, pp. 1–6.

[30] R. Spyker and R. Nelms, "Evaluation of double layer capacitor technologies for high power and high energy storage applications," in *Industrial Electronics, Control and Instrumentation, 1997. IECON 97. 23rd International Conference on*, vol. 3, Nov 1997, pp. 1086–1091 vol.3.

[31] Y. Yao, D. Zhang, and D. Xu, "A study of supercapacitor parameters and characteri stics," in *Power System Technology, 2006. PowerCon 2006. International Conference on*, Oct. 2006, pp. 1–4.

[32] M. Seeman, V. Ng, H.-P. Le, M. John, E. Alon, and S. Sanders, "A comparative analysis of switched-capacitor and inductor-based dc-dc conversion technologies," in *Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*, june 2010, pp. 1 –7.

[33] M. Wieckowski, G. K. Chen, M. Seok, D. Blaauw, and D. Sylvester, "A hybrid dc-dc converter for sub-microwatt sub-1v implantable applications," in *VLSI Circuits, 2009 Symposium on*, june 2009, pp. 166 –167.

[34] E. Carlson, K. Strunz, and B. Otis, "20mv input boost converter for thermoelectric energy harvesting," in *VLSI Circuits, 2009 Symposium on*, june 2009, pp. 162 –163.

[35] M. Seeman, S. Sanders, and J. Rabaey, "An ultra-low-power power management ic for energy-scavenged wireless sensor nodes," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, june 2008, pp. 925 –931.

[36] ——, "An ultra-low-power power management ic for energy-scavenged wireless sensor nodes," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, june 2008, pp. 925 –931.

[37] R. Erickson, "Dc-dc power converters," in *Wiley Encyclopedia of Electrical and Elctronics Engineering.*, vol. 5, 1999, pp. 53–63.

[38] J. Xiao, A. Peterchev, J. Zhang, and S. Sanders, "A 4 mu;a-quiescent-current dual-mode buck converter ic for cellular phone applications," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, 2004, pp. 280 –528 Vol.1.

[39] P. Hazucha, G. Schrom, J. Hahn, B. Bloechel, P. Hack, G. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-mhz 80-87 percent efficient four-phase dc-dc converter utilizing air-core inductors on package," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 4, pp. 838 – 845, april 2005.

[40] D. Perreault, J. Hu, J. Rivas, Y. Han, O. Leitermann, R. Pilawa-Podgurski, A. Sagneri, and C. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, feb. 2009, pp. 1 –14.

[41] C. Tse, S. Wong, and M. Chow, "On lossless switched-capacitor power converters," *Power Electronics, IEEE Transactions on*, vol. 10, no. 3, pp. 286 –291, may 1995.

[42] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," in *Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on*, 2006, pp. 216 –224.

[43] Y. Ramadass and A. Chandrakasan, "Voltage scalable switched capacitor dc-dc converter for ultra-low-power on-chip applications," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 2353 –2359.

[44] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 2, Jun. 1995, pp. 1215 –1221 vol.2.

[45] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," in *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, sept. 2011, pp. 479 –482.

[46] Y. Ramadass, "Energy processing circuits for low-power applications," in *Ph.D Thesis. MIT*, 2009.

[47] W. Sanchez, C. Sodini, and J. Dawson, "An energy management ic for bio-implants using ultracapacitors for energy storage," in *VLSI Circuits (VLSIC), 2010 IEEE Symposium on*, 2010, pp. 63 –64.

[48] E. Dowgiallo and J. Hardin, "Perspective on ultracapacitors for electric vehicles," in *Battery Conference on Applications and Advances, 1995., Proceedings of the Tenth Annual*, Jan 1995, pp. 153–157.

[49] A. Belousov, "Single capacitor powers audio mixer," *EDN*, March 1997. [Online]. Available: http://www.edn.com

[50] E. Cegnar, H. Hess, and B. Johnson, "A purely ultracapacitor energy storage system hybrid electric vehicles utilizing a based dc-dc boost converter," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 2, 2004, pp. 1160–1164 vol.2.

[51] D. Cheng and M. Wismer, "Active control of power sharing in a battery/ultracapacitor hybrid source," in *Industrial Electronics and Applications, 2007. ICIEA 2007. 2nd IEEE Conference on*, May 2007, pp. 2913–2918.

[52] M. Kazimierczuk and R. Cravens, "Application of super capacitors for voltage regulation in aircraft distributed power systems," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, vol. 1, Jun 1996, pp. 835–841 vol.1.

[53] F. Gozzini, G. Ferrari, and M. Sampietro, "Linear transconductor with rail-to-rail input swing for very large time constant applications," *Electronics Letters*, 2006.

[54] R.-M. Weng, X.-R. Hsu, and Y.-F. Kuo, "A 1.8- v high-precision compensated cmos bandgap reference," in *Electron Devices and Solid-State Circuits, 2005 IEEE Conference on*, dec. 2005, pp. 271 – 273.

[55] P. Favrat, P. Deval, and M. Declercq, "A high-efficiency cmos voltage doubler," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 3, pp. 410–416, Mar 1998.

[56] M. Wieckowski, G. K. Chen, M. Seok, D. Blaauw, D. Sylvester, and A. Arbor, "A Hybrid DC-DC Converter for Sub-Microwatt Sub-1V Implantable Applications," *VLSI Symposium 2009.*

[57] S. Ben-Yaakov and A. Kushnerov, "Algebraic foundation of self adjusting switched capacitors converters," in *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, 2009, pp. 1582 –1589.

[58] M. Seeman, "A design methodology for switched-capacitor dc-dc converters," in *Ph.D Thesis. U.C. Berkeley*, 2009.

[59] P. Lin and L. Chua, "Topological generation and analysis of voltage multiplier circuits," *Circuits and Systems, IEEE Transactions on*, vol. 24, no. 10, pp. 517 – 530, oct 1977.

[60] J. Dickson, "On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique," *Solid-State Circuits, IEEE Journal of*, vol. 11, no. 3, pp. 374 – 378, jun 1976.

[61] Y. Lee and Y. Cheng, "A 580 khz switching regulator using on-off control," *Electronic and Radio Engineers, Journal of the Institution of*, vol. 57, no. 5, pp. 221 –226, 1987.

[62] J. Rivas, D. Jackson, O. Leitermann, A. Sagneri, Y. Han, and D. Perreault, "Design considerations for very high frequency dc-dc converters," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 2006, pp. 1 –11.

[63] R.-Y. Kim, J.-S. Lai, B. York, and A. Koran, "Analysis and design of maximum power point tracking scheme for thermoelectric battery energy storage system," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 9, pp. 3709 –3716, sept. 2009.

[64] R.-Y. Kim and J.-S. Lai, "A seamless mode transfer maximum power point tracking controller for thermoelectric generator applications," *Power Electronics, IEEE Transactions on*, vol. 23, no. 5, pp. 2310 –2318, sept. 2008.

[65] G. Bekefi and A. H. Barrett, *Electromagnetic Vibrations, Waves, and Radiation.* MIT Press, 1977.

[66] D. B. Miron, *Small antenna design by Douglas B. Miron*, ser. Communications engineering series. Burlington, MA: Newnes/Elsevier, 2006, 019: 1 40037609; : ill. ; 24 cm. + 1 CD-ROM (4 3/4 in.; Includes bibliographical references and index. [Online]. Available: http://www.loc.gov/catdir/toc/ecip064/2005033797.html

[67] R. Sarpeshkar, *Ultra Low Power Bioelectronics.* Cambridge University Press, 2010.

[68] C. Borja and J. Romeu, "On the behavior of koch island fractal boundary microstrip patch antenna," *Antennas and Propagation, IEEE Transactions on*, vol. 51, no. 6, pp. 1281–1291, 2003, iD: 1.

[69] L. J. Chu, "Physical limitations of omni-directional antennas," *Journal of Applied Physics*, vol. 19, no. 12, pp. 1163–1175, 1948. [Online]. Available: http://link.aip.org/link/?JAP/19/1163/1

[70] Y. Huang and K. Boyle, *Antennas : from theory to practice.* Chichester, UK: John Wiley and Sons Ltd., 2008, iD: 214285896.