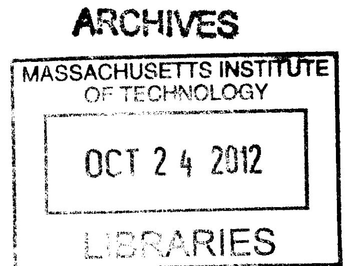
Efficiency Enhancement Techniques for RF and Millimeter Wave Power Amplifiers

by

Olumuyiwa Temitope Ogunnika

B.E., Electrical Engineering
The City College of New York (2001)
S.M., Electrical Engineering and Computer Science
Massachusetts Institute of Technology (2004)



Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2012

© Massachusetts Institute of Technology 2012. All rights reserved.

Author ....
Department of Electrical Engineering and Computer Science
August 31, 2012

Certified by ....
Joel L. Dawson
Associate Professor
Thesis Supervisor

Accepted by ....
Leslie A. Kolodziejski
Chairman, Department Committee on Graduate Theses

Efficiency Enhancement Techniques for RF and Millimeter Wave Power Amplifiers

by

Olumuyiwa Temitope Ogunnika

Submitted to the Department of Electrical Engineering and Computer Science
on August 31, 2012 in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

Power amplifiers are the circuit blocks in wireless transceivers that require the largest power budget because of their relatively low efficiencies. RF designers cannot depend solely on the development better semiconductor devices in advanced deeply scaled process technologies to obtain improved power amplifier performance. The development of new and better circuits, architectures and design methodologies to maximally exploit the available semiconductor devices is very important as well. This thesis investigates a number of techniques that can be used to improve the efficiency of power amplifiers and break the power-frequency tradeoff in power amplifier design. The first technique emphasizes the use of a class E tuned output network as an efficiency enhancement tool for power amplifiers regardless of their bias conditions. A Class E tuned CMOS power amplifier (PA) operating in the 60 GHz band was designed. Design, layout, and parasitic modeling considerations to attain high-efficiency millimeter-wave PA operation are discussed. Both single-ended and differential versions of the single-stage PA were implemented in a 32 nm SOI CMOS process. Peak power added efficiency of 27% (30%), power gain of 8.8 dB (10 dB), and saturated output power > 9 dBm (12.5 dBm) were measured at 60 GHz from the single-ended (differential) PA with 0.9 V supply. The second technique investigated the efficacy of resistance compression networks in an energy recycling network operating at multi-gigahertz frequencies. The resistance compression network reduces the variation in resonant rectifier input impedance seen at the isolation port of an isolating power combiner. The system was operated at 2.14 GHz and was built around Schottky barrier diodes custom fabricated in a 0.13 μm CMOS process. It is the first experimental demonstration that resistance compression networks can be used for energy recycling in multi-gigahertz applications.

Thesis Supervisor: Joel L. Dawson
Title: Associate Professor

Acknowledgements

First and foremost, I would like to thank my research advisor, Professor Joel Dawson, for his support and guidance throughout the course of my doctoral work. He has been an extraordinary mentor and it has been a great privilege working with him. I have learnt a great deal from Professor Dawson about all aspects of RF and communication circuits design and techniques for good problem solving. He has been a great example to me of professionalism and hard work; important traits which I will seek to emulate as I embark on my career. I would certainly not be where I am today without his dedication to my progress and success. I would like to thank Dr. Alberto Valdes-Garcia who was my mentor during my summer internship at IBM T.J. Watson Research Center. I learnt a lot about millimeter wave PA design from working with Dr. Valdes-Garcia because of his vast experience and understanding of the subject matter. His guidance enabled me to complete the class E tuned PA design and obtain record PAE performance from a single tape out. He also designed the measurement setup required to test the PA. I would also like to express my sincere gratitude to Professor Charlie Sodini and Professor Jim Roberge for serving on my thesis committee. Their comments and insight have been invaluable for improving my thesis. Dr. Mihai Sanduleanu and the entire millimeter wave design team at IBM T.J. Watson research center were invaluable in the completion of the first half of this work. I would like to thank Professor David Perreault for useful technical discussions about resistance compression networks and resonant rectifiers.

Several past and present members of the Dawson research group have been important in my journey. Dr. Philip Godoy implemented the first OPERA prototype at 48 MHz that demonstrated the efficacy of resistance compression networks for energy recovery. His suggestions were invaluable for my initial foray into employing energy recovery at multi-

gigahertz frequencies. Sungwon Chung was a great person to discuss ideas and issues with because of his vast experience and understanding of many areas in wireless communications. It has been a pleasure working in the same lab with Tania Khanna, Willie Sanchez, Taylor Barton, Gilad Yahalom and Zhen Li. They have helpful in so many ways from prepping for my thesis defense talk to working together on test setups in the lab. My office mates Laura Popa, Radhika Marathe, and Wentao Wang have been great friends to chat with and always made working at my desk more fun. I would like to thank our research group administrator, Coleen Kinsella, for helping with timely orders of parts and components I needed for my measurements.

I have had a great support network during my years in graduate school. Professor Terry Orlando and Dr. Ann Orlando who are the Housemasters at Ashdown House have been an immense source of support and encouragement in my journey. I got to know Ann and Terry when I served on the Ashdown House Execute Council and shared some of my best experiences in graduate school with them. Denise Lanfanchi, who is the House Manager at Ashdown House, has been an amazing friend and someone who I could always talk to. Debroah Hodges-Pabón has also been a great source of encouragement always checking on my well-being and progress. Several friends have been immense sources of support and encouragement throughout my time at MIT. They include Dr. David Chan, Chris Lee, Chris Sutherland, Daniel Grivakis, Dr. Tyler VanderWeele, Po-Ru Loh and Kunle Adeyemo. Dr. Gordon Hugenberger who is the Senior Minister at Part Street Church which I attended during my time in Boston always had great words of wisdom through his sermons and personal discussions with me.

I would like to thank my brothers Babatunde and Femi and my sisters Toyin and Seun for their unwavering love and encouragement.

Words cannot express my deepest gratitude to my loving parents Professor Zacchaeus Ogunnika and Olabisi Ogunnika for all they've done in my life. They inspired me at a young age to pursue knowledge and a good education which culminated in my decision to go to graduate school. They have been the foundation of my support and the wellspring I could always draw from whenever I needed encouragement. They never ceased loving me and praying for me.

And finally, I am grateful to God for giving me the strength to complete graduate school and reach the culmination of my doctoral research work.. Nothing I could hope to do is now or in the future is possible without faith in the Lord Jesus Christ. One of my favorite verses of scripture is Proverbs 3:5-6; "Trust in the Lord with all your heart, and lean not on your own understanding. In all your ways acknowledge Him, and he shall direct your paths." To God be the Glory!

Contents

1 Introduction **17**

1.1 Motivation 18

1.2 Research Contributions 20

1.3 Thesis Organization 22

2 PA theory, design methodology and simulation results **25**

2.1 Common PA Architectures 25

2.2 Theoretical Analysis of the Class E PA 30

2.2.1 Design Equations for Ideal Class E PA 34

2.3 Implementation of 60-GHz Class E tuned PA 38

2.3.1 Transistor Size 39

2.3.2 Input Matching Network 43

2.3.3 Drain Load 45

2.3.4 Output Network 47

2.3.5 FET Layout Methodology 52

2.4 Simulation Results 53

2.5 Design Insights and Discussion 56

2.5.1 Class E Tuned Output Network as an efficiency enhancement technique for classical power amplifiers 57

2.6 Summary 59

3 PA Measurement and Characterization 61

3.1 Measurement Setup 61

3.2 Measurement Results 64

3.3 Summary 71

4 Theoretical Development of Energy Recovery at RF and Multi-gigahertz Frequencies 74

4.1 Schottky Barrier Diode Design Considerations 76

4.1.1 Schottky Barrier Diode Model 76

4.1.2 Schottky Barrier Diode size selection 79

4.2 Resonant rectifier design 87

4.3 Resistance Compression Network 89

4.4 Theoretical Efficiency of Outphasing PA employing energy recovery 92

4.5 Summary 93

5 Practical System Implementation and Measurement of the Energy Recovery Network 95

5.1 Energy Recovery Network Design 95

5.2 Prototype Implementation 107

5.3 Measurements and Results 111

5.4 Summary 118

6 Conclusions and Future Work 120

6.1 Summary of Contributions 120

6.2 Future Work 121

List of Figures

1-1: System Diagram of Asymmetric Multilevel Outphasing PA. The rectification and energy storage block can be implemented by means of an energy recovery network which uses a resistance compression network to reduce the variation in impedance at the power combiner's difference port. 19

1-2: Class E power amplifier 21

2-1: Concept diagram and current waveforms of Class A PA [10] 26

2-2: Concept diagram of Class B power amplifier [10] 27

2-3: Concept diagram of Class F power amplifier [10] 29

2-4: Diagram of ideal class E power amplifier 31

2-5: Non-overlapping voltage and current waveforms at the drain of the active device. 32

2-6: Diagram of ideal class E power amplifier 35

2-7: Design methodology 38

2-8: Family of I_{DS} vs. V_{GS} plots used for transistor size selection 42

2-8b: Peak power gain variation with gate bias in 10-GHz class E PA 43

2-9: Concept diagram of design of input network 44

2-10: Input matching network with drain load for single ended PA. 45

2-11: AC simulation from input pad to NFET gate showing peaking at 60 GHz 45

2-12: Estimating transmission line drain load using Z-parameter simulation 46

2-13: Class E tuned PA with output network implemented using ideal passives 47

2-14: (a) PAE and (b) Output power from a PSS simulation of Fig. 2-13 with load R swept form 10 Ω to 100 Ω 48

2-15: (a) PAE and (b) Output power from a PSS simulation of Fig. 2-13 with load R = 20 Ω and series inductance L_S swept from 100 pH to 550 pH 49

2-16: Smith Chart depicting the S parameters of alternative implementations of the output network. S_{11}: output network implemented ideal components; S_{33}: final transmission line output network; S_{55} and S_{77}: alternative network topologies that did not possess the desired low-pass characteristics. 50

2-17: Conversion of ideal output network to transmission line equivalent. Their input reflection coefficients are matched by setting $S_{33} = S_{11}$. 50

2-18: Schematic of 60-GHz class E PA (a) single-ended; (b) differential 51

2-19: FET Layout; (a) Gate ring contact with multiple metals; (b) Staircase-like drain/source metallization [14] 52

2-20: Measured f_{MAX} on 6 dies across a wafer. FET test structure includes all metals. 53

2-21: S-parameter plots of the 60-GHz class E PA 54

2-22: Voltage and Current waveforms at drain of active device simulated at 57 GHz, 61 GHz and 65 GHz. 54

2-23: Simulated PAE, saturated output power and power gain of the 60-GHz class E tuned PA 56

2-24: Schematic of a standard 10-GHz class A/AB PA compared to version with load replaced by a class E tuned output network. 58

2-25: PAE of a standard 10-GHz class A/AB PA compared to version with load replaced by a class E tuned output network 58

3-1: PA chip micrographs; (a) Single-ended (550 μm X 650 μm)

(b) Differential (550 μm X 1.1 mm) 61

3-2: Single-ended PA measurement setup. 63

3-3: Differential PA measurement setup 63

3-4: Drain current vs. gate bias voltage. 64

3-5: S-parameters of 60-GHz class E tuned PA 66

3-6: S parameters variation with gate bias voltage at 60 GHz 67

3-7: Measured PAE and power gain vs. output power at 60 GHz for the single-ended implementation of the PA 68

3-8: Measured peak PAE, Psat and power gain vs. frequency 68

3-9: Measured 60-GHz peak PAE and Psat vs. drain voltage. 69

3-10: Measured process variation of PAE, Psat and power gain for 7 different dies at 60 GHz 69

3-11: Measured peak PAE, Psat and power gain vs. temperature at 60 GHz 70

3-12: Measured PAE and power gain vs. output power at 60 GHz for the differential implementation of the Class-E PA. 70

4-1: Outphasing power amplifier with power recycling network. 75

4-2: Schematic cross section of an integrated SBD [15] 77

4-3: Circuit schematic model of SBD; (a) General model (b) Small signal model 77

4-4: I-V characteristics of Schottky diode with and without series resistance, R_S 79

4-5: Simulation testbench for the halfwave rectifier 80

4-6: Efficiency and input power of halfwave rectifier using SBD with length = 4 μm, width = 5 μm and number of fingers = 2 81

4-7: Efficiency and input power of halfwave rectifier using SBD with length = 20 μm, width = 5 μm and number of fingers = 4 82

4-8: Halfwave rectifier with parasitic diode capacitance 87

4-9: Outphasing power amplifier with resistance compression network in energy recovery network. 90

4-10. Resistance compression network with matched load resistances. 90

4-11: Variation of the resistance of a resistance compression network with 10:1 change in matched load resistance. 91

4-12: Variation of the outphasing PA efficiency with energy recovery network efficiency. 93

5-1: Testbench to determine input current drive and resistance of the resonant rectifiers. 96

5-2: Efficiency and Input and Output power of resonant rectifier testbench in Fig. 5-1. 98

5-3: Resonant rectifier input resistance from testbench in Fig. 5-1. 98

5-4: Testbench for outphasing system with resistance compressed energy recovery network. 99

5-5: Lumped element Wilkinson power combiner designed for 2.5 GHz. 100

5-6: Compressed resistance of the resistance compressed rectifier (i.e. resonant rectifier combined with a resistance compression network) 101

5-7: Resistance of the entire energy recovery network (including the matching network) 101

5-8: Efficiency of energy recovery network 102

5-9a: Total outphasing system efficiency vs. outphasing angle for two systems one of which employs a resistance compressed ERN. PAs modeled as ideal current sources 104

5-9b: Total outphasing system efficiency vs. output power back off for two systems one of which employs a resistance compressed ERN. 105

5-10: Recovered power normalized to available power from the individual PAs. 105

5-11: Total available power from outphasing system normalized to available power from the individual PAs........ 106

5-12: Chip micrograph showing integrated Schottky barrier diodes........ 107

5-13: Schematic of energy recovery network........ 109

5-14. Measurement setup for the energy recovery network prototype........ 110

5-15: S_{11} of energy recycling network vs. input power........ 115

5-16: Efficiency of energy recycling network vs. Input power........ 116

List of Tables

3.1: Summary of Current State of the Art in High-Efficiency Silicon-Based Millimeter Wave PAs 72

5.1: Range of R_{ERN} for the values of S_{11} measured in Fig. 5-15b 113

Chapter 1

Introduction

RF systems show the challenge of efficiently operating simultaneously at high frequency and high power. The typical limitation observed is degradation in the ability to deliver high output power as the RF systems' operating frequency is increased. Power amplifiers are a good example of transceiver blocks that provide much evidence to support this power—frequency tradeoff. The engineer has basically two approaches to improving this tradeoff. The first approach is to simply fabricate and take advantage of better semiconductor devices. The staggering success of this approach can be seen in the revolution ushered in by Moore's Law scaling in CMOS: so much of the improvement in the last couple of decades can indeed be traced to better, faster devices. Outside of silicon, the improvements are less dramatic but still substantial. GaAs, GaN, and many other technologies get better and better as time goes on. The other, often underappreciated, approach that the engineer has is to develop new and better circuits, architectures, and design methodologies to maximally exploit the amazing properties of new devices. The development of techniques which can break this power—frequency tradeoff is very important because it will provide access to higher frequency bands which are currently underutilized for wireless communication.

1.1 Motivation

With the availability of 7 GHz of unlicensed bandwidth centered at 60GHz, this space has emerged as an active area of research. A number of challenges are typically faced when designing transceivers at millimeter wave frequencies. Strong atmospheric absorption at 60 GHz lowers the signal-to-noise ratio (SNR) available at the receiver [29]. This limits the complexity of the signal constellations that can be used and thus reduces the number of bits per symbol that can be encoded with typical modulation strategies. For high data rates, this will require more symbols per second forcing the use of extremely fast baseband modulators. The well understood challenges of obtaining good linearity, high output power and high efficiency in power amplifiers is further exacerbated at this carrier frequency complicating transceiver design. Delivering significant power at 60 GHz requires very fast devices with high f_{max} and f_{T}. This technological hurdle has been lowered with recent advances in SiGe, III-V semiconductor technology and deeply scaled CMOS with $f_{\text{max}} > 250$ GHz. The implementation of wireless transceivers at millimeter wave frequencies is particularly attractive because of several useful applications which include:

- Uncompressed high-definition video streaming
- Wireless Gigabit Ethernet
- Rapid transfer of large files
- Wireless Personal Area Networks (WPAN)
- Wireless docking station and desktop point to multipoint connections

Energy recovery, which has enjoyed sporadic attention over the last couple of decades, is newly enabled by custom Schottky barrier diodes (SBDs) and resistance compression networks. A particularly useful application of energy recovery is in further improving the efficiency of

outphasing power amplifier architectures. Over the last few years, there has been newfound interest in outphasing because of recent results of the Asymmetric Multilevel Outphasing (AMO) power amplifier architecture [28], [31], and [32]. This architecture (see Fig. 1-1) combines the best properties of polar transmitters and outphasing (LINC) transmitters [30]. The power amplifier's efficiency is improved without significantly degrading its linearity by using the combination of drain voltage modulation and rapid outphasing. A key motivation of this project will be the investigation of energy recovery as a means of further improving the AMO transmitter's efficiency. The inclusion of a resistance compression network [23] as a means of reducing the impedance variation of the energy recovery network is very important because the PA outputs (PA_1 and PA_2 in Fig. 1-1) need to be isolated from each other if they are implemented with high-efficiency switching topologies such as class E.

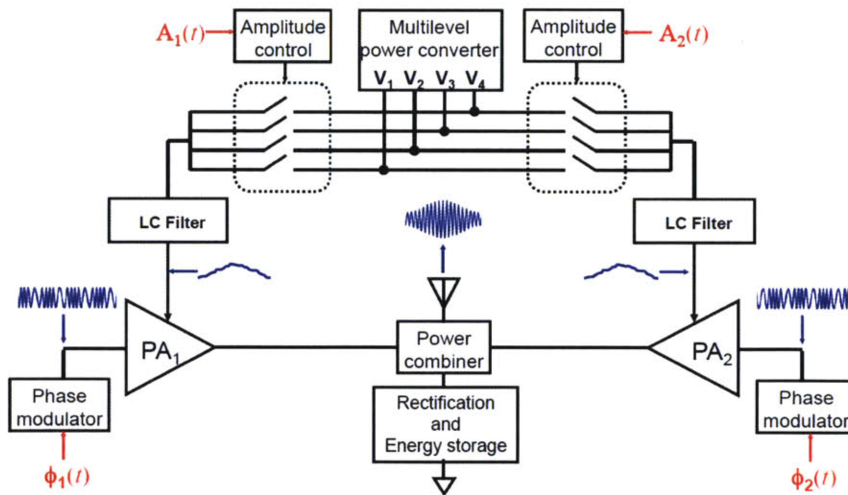


Figure 1-1: System Diagram of Asymmetric Multilevel Outphasing PA. The rectification and energy storage block can be implemented by means of an energy recovery network which uses a resistance compression network to reduce the variation in impedance at the power combiner's difference port.

An important question to consider is the justification to use energy recovery rather than lossless combining in an outphasing PAs. After all, it is inefficient to throw energy away (at the isolating combiner's difference port) and then try to recover it. Typical lossless combiners such as Chireix provide isolation between its ports at a very narrow range of outphasing angles (or output power). Such restrictions are detrimental in modern wireless communication systems which use modulation schemes such as Orthogonal Frequency Division Multiplexing (OFDM) and 256-QAM (Quadrature Amplitude Modulation) that have high PAPRs. Significant power backoff at large outphasing angles is necessary to produce the required signal constellations. But good isolation between the PAs is essential for reliable operation of high-efficiency switching PAs such as Class-E. Using classical PA topologies which are less sensitive to load modulation (such as class A/AB) is undesirable because the benefit of an outphasing system can only be harnessed if high-efficiency but nonlinear PAs are used. It is necessary to use the high efficiency of the switching mode PAs to ameliorate or compensate for the losses in the power combiner. Moreover, there is additional circuit complexity and DSP overhead in the signal component separation operation necessary to generate the input signals for the PAs. Such additional complexity can only be justified with the use of high-efficiency switching PAs in outphasing systems.

1.2 Research Contributions

The initially proposed solution to the problems enumerated in the previous section was the implementation of an outphasing PA system that employs millimeter wave class E tuned PAs and a resistance compressed energy recovery network. Subsequent chapters in this thesis will show that a high-efficiency millimeter wave PA was successfully designed but energy recovery at millimeter wave frequencies was not feasible in the CMOS process available. Subsequently,

the project goal was modified to demonstrate the efficacy of resistance compression networks at frequencies on the order of 2 GHz.

The first contribution of this work is employing the class E tuned output network as an efficiency enhancement technique for classical PA topologies. The standard class E PA presented in Fig. 1-2 employs a tuned output network to produce non-overlapping voltage and current waveforms at the drain of the active device. Since voltage and current are not simultaneously non-zero, there is no power dissipation in the active device and a 100% theoretical efficiency is possible. A 60-GHz class E tuned power amplifier designed in 32 nm CMOS SOI is presented which employs a transmission line class E tuned network to obtain 30% peak PAE for the differential version. The PA was designed employing class E techniques but the active device was biased in the sub-threshold or weak inversion region so that a larger output power could be obtained. Even though the active device was not operated as an ideal switch as required for a classical class E PA, its efficiency was still improved because of the output signal shaping properties of the class E tuned network.

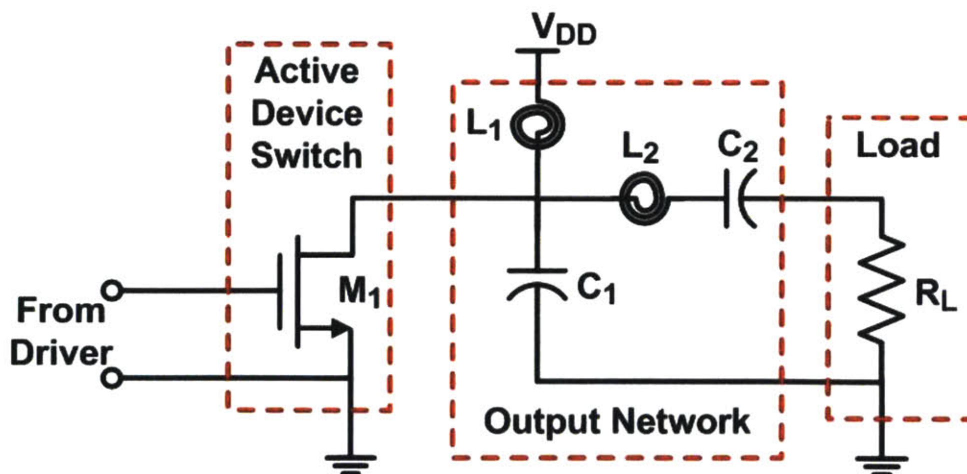


Figure 1-2: Class E power amplifier

The second contribution is the use of a formalized iterative approach to the design of the millimeter wave power amplifier. The PA design was compartmentalized into distinct sections which were implemented separately but have a strong influence on each other. Employing the iterative design approach made possible the convergence to a final solution in an efficient manner. This approach also emphasizes the interaction between each major section of the PA and the tradeoffs that need to be made for good performance.

The third contribution is the use of resistance compression networks (RCN) for energy recovery at multi-gigahertz frequencies. The use of an outphasing PA topology with an isolating power combiner becomes more attractive when the energy typically lost at the difference port of the power combiner can be recycled back to the power supply. The inclusion of an RCN along with the resonant rectifiers at the difference port of the power combiner helps to maintain good isolation between the switching mode PAs. This enables high efficiency and good linearity to be achievable in outphasing PA architectures such as AMO. Although Godoy et al. [22] has presented a successful demonstration of the principle at a 48-MHz operating frequency, it was not clear that a RCN will be effective when the operating frequency is increased. An energy recycling network that operates at 2.14 GHz is presented to show that RCNs can be used at multi-gigahertz frequencies.

1.3 Thesis Organization

Chapter 2 briefly reviews a number of classical PA architectures and justifies the use of the class E topology for the purposes of this work. The theory of operation of the class E PA will be discussed emphasizing the properties that give this architecture high theoretical efficiency. Next,

the design and implementation of a 60-GHz class E tuned PA will be presented along with simulation results and useful design insights.

Chapter 3 presents the measurement setup and results of the 60-GHz PA implemented in an IBM 32μm CMOS SOI process. Comparison of the PA's performance to other state-of-the-art millimeter PAs will also be included.

Chapter 4 delves into the theory of energy recovery at RF and multi-gigahertz frequencies. Important considerations for the Schottky diode size selection and resonant rectifier design will be discussed. The theory of operation of a resistance compression network will also be analyzed.

Chapter 5 discusses the design of an energy recovery network that operates at a frequency of 2.5 GHz. A prototype of the energy recovery network which uses Schottky barrier diodes fabricated in a 0.13-μm CMOS process will be presented along with some measurement results.

Finally, Chapter 6 summarizes the contributions of this work and proposes future projects that can improve upon the results presented in this thesis.

Chapter 2

PA theory, design methodology and simulation results

This chapter covers the theory and design of the 60-GHz Class E PA. A brief overview of a number of alternative PA architectures will be discussed with reference to advantages and disadvantages of their implementation at millimeter wave frequencies.

2.1 Common PA Architectures

There are several power amplifier topologies commonly used at millimeter wave frequencies. A common feature is simplicity and the use of as few active devices as possible because of the loss introduced by device parasitics. This section describes, in broad terms, the features and characteristics of class A, B, C, D, E, and F PAs. Ultimately, for the millimeter wave PA work in this thesis, the methods and theory of the class E proved to be the best choice.

The class A power amplifier exhibits a linear relationship between the input and output signals. Typically, the transfer function shows a low pass characteristic with attenuation at higher frequencies. Highly linear PAs are essential for complex modulation schemes and constellations making the class A architecture good for 64 QAM and OFDM. The class A PA represents the ultimate sacrifice of efficiency for the sake of linearity. That is because it achieves its high linearity by using a 360° conduction angle. This implies the active device conducts

current continuously and dissipates static DC power regardless of the power being delivered to the load. Thus, the efficiency of class A PAs are very poor at large power backoffs. Since complex modulation schemes have high PAPR which can exceed 6.5 dB, class A PA implementations lead to very poor system efficiencies. In practical PAs at millimeter wave frequencies, the power gain is further reduced from the peak theoretical efficiency (50% for class A) because of the limited power gain attainable from the active device. The effect of device parasitics is more significant at millimeter wave frequencies making PA efficiencies significantly below 50%.

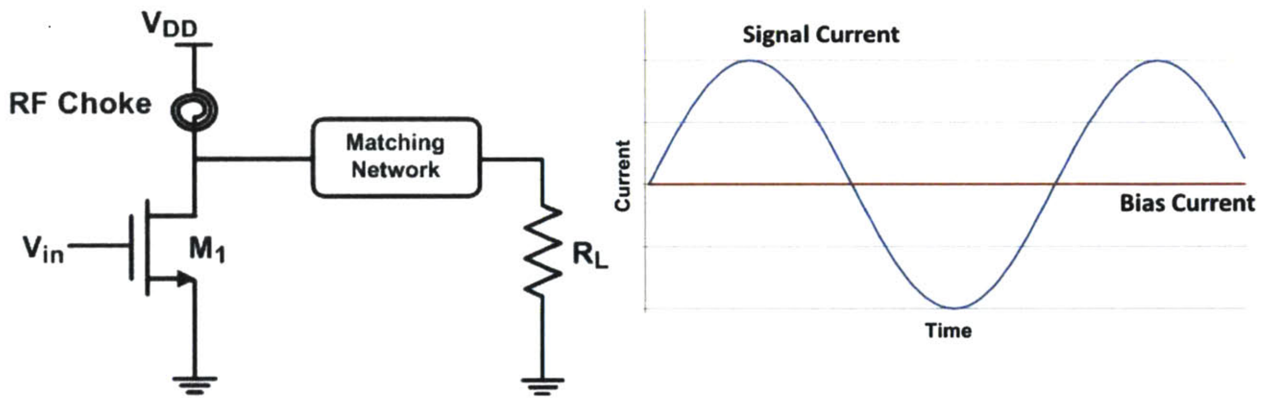


Figure 2-1: Concept diagram and current waveforms of Class A PA [10]

Class B achieves higher efficiency than class A by setting the active device bias so that it conducts for 180° of the cycle. The DC power dissipation in the device is reduced by a factor of $\pi/2$ when compared to a class A PA designed to deliver the same output power to a given load. Thus theoretical maximum efficiency of the class B PA increases to a value of $\pi/4 \cong 79\%$. An example is the push-pull topology shown in Fig. 2-2. Note that technically, the class B PA is actually one of the active device stages that conducts for 180° of the cycle. Since the two devices are driven differentially, the supply current always flows through the load. A drawback of this topology is the need for a low loss balun to combine the outputs of the two active devices.

At millimeter wave frequencies, the non-idealities and parasitics of the balun will degrade efficiency.

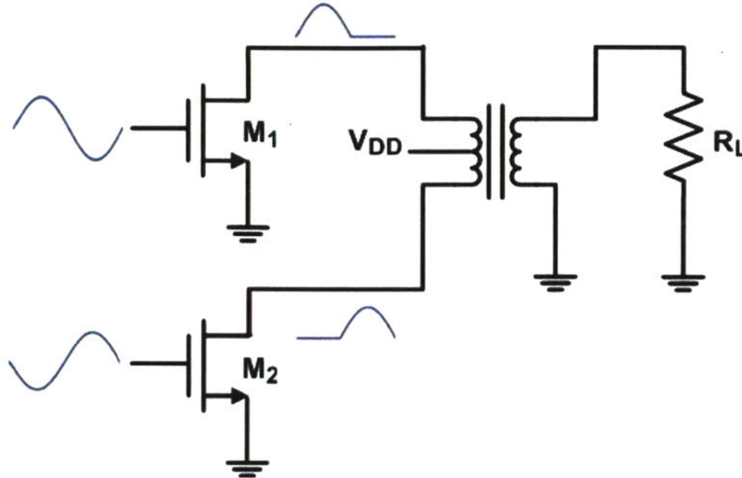


Figure 2-2: Concept diagram of Class B power amplifier [10]

The conduction angle in the class C PA topology is less than 180° and can be implemented by biasing the gate in the class A topology in Fig. 2-1 with a negative voltage. This introduces significant nonlinearity making it essential to use this PA in a system that employs envelope elimination and restoration (EER) or outphasing (LINC). Because the load current is now a section of a sinusoid, the class C topology dissipates less power in the transistor but also delivers lower output power. When this drawback is combined with the dearth of power gain at millimeter frequencies, the class C topology is not suitable for use.

The class D PA topology achieves high efficiency by operating the active devices as switches. The voltage drop across the transistor is made as small as possible while there is a current flowing through it. Similarly, the current through the transistor is small or zero while there is a voltage across it. The other mechanism of power loss in a switching transistor is the unavoidable power dissipation when there is a transition from the "on" state to the "off" state during which

appreciable voltage and current are simultaneously present in the active device. Researchers have sought to reduce this power loss by reducing the switching time. But the faster transistors which are available in deeply scaled CMOS processes come with adverse properties such as lower supply voltages, smaller breakdown voltages, increased sensitivity to transistor parasitics, etc.

The class F PA topology shown in Fig. 2-3 achieves high efficiency by output load harmonic tuning. The voltage is a square wave while the current is a half sine wave. The shaping of the voltage at the active device's drain is obtained by setting the load network to provide high impedance at twice or three times the fundamental frequency. The high impedance is created by including parallel resonant L-C sections in the output load network leading to sharper transitions in the drain voltage waveform. The major idea of the class F PA is to reduce power dissipation in the device by reducing the length of the drain voltage transition time. When the voltage waveform has a sharp transition similar to that in a square wave, the time during which the current and voltage are simultaneously high is reduced thus improving PA efficiency. In theory, better performance can be obtained by creating resonances at more harmonics of the fundamental. But we encounter diminishing returns in practical circuits because of the increased complexity and large number of components required. The difficulty in using this topology at millimeter wave frequencies is the requirement for high Q passive components to construct the harmonically tuned load. Such high Q components are difficult to obtain at high frequencies. Another drawback of this topology is the relatively low output power available when the PA is operating under optimum efficiency conditions.

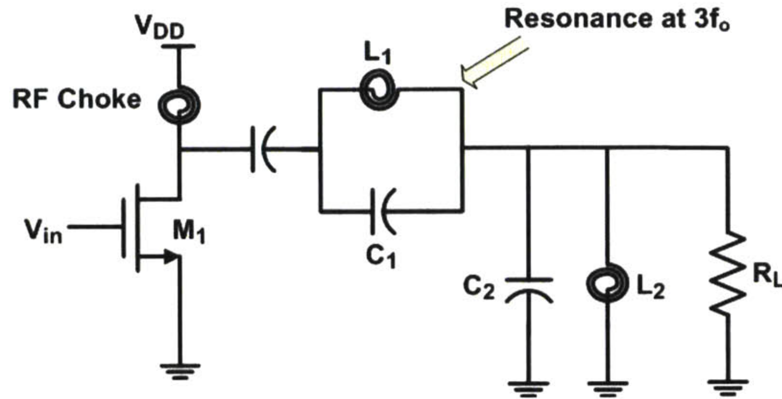


Figure 2-3: Concept diagram of Class F power amplifier [10]

The class E PA (introduced by Alan and Nathan Sokal [8]) achieves high efficiency by means of zero voltage switching (ZVS) and zero voltage-derivative switching (ZVDS) conditions. When the transistor or active device is turned on and carrying a current, the voltage across the active device is zero or a very small value. Similarly, when the transistor is turned off, it develops some voltage across the drain – source terminals while no current flows through it. In other words, the non-overlapping characteristic of the voltage and current waveforms ensures that the peak voltage across the device occurs when the magnitude of current flowing through it is minimum and vice versa. As a result, there is very little power dissipation in the active device and a theoretical efficiency of 100% is possible under ideal conditions. Class E operation requires that the PA satisfies the following three properties:

(1) During the turn-off transient, the voltage remains zero until the current through the active device drops to zero; then is rises.

(2) During the turn-on transient, the current remains at zero until the voltage drops to zero; then it rises.

(3) During the turn-on transient, the voltage drops to zero with zero slope. This ensures that the region where there is simultaneous appreciable value of voltage across and current through the active device is small ensuring high efficiency operation of the class E PA.

The class E PA is able to satisfy these conditions because of the transient response behavior of the output network. At transistor turn-off when the current drops to zero, the output network behaves like a critically damped 2nd order system with initial conditions determined by the current through L_2 and the voltage across C_1 and C_2 in Fig. 2-4. Thus the operation of the circuit is governed by the transistor when it is on, and by the transient response of the load (output) network when the transistor is off.

A drawback of the Class-E PA is excessive voltage and current stress on the active device. The peak voltage across the active device is $3.56V_{DD}$ where V_{DD} is the supply voltage. The class E topology was selected for this project because of its relative simplicity when compared to other high efficiency topologies such as the class F. Although it requires the active device to operate as a switch, the abruptness of the transitions in the current and voltage waveforms are not as stark as those for other topologies, such as the class D, which is an important consideration especially at very high frequencies. Almost as important, over the decades the class E PA has earned a reputation for robustness and good behavior when implemented in the lab.

2.2 Theoretical Analysis of the Class E PA

A standard class E PA (presented in Fig. 2-4 and adapted from [8]) consists of a transistor connected to an output network and bias inductor. The output network is designed to have a transient response that enables the PA to achieve a theoretical 100% efficiency. This high efficiency can still be obtained even though the transistor's switching time is a significant portion

of the input signal's period. At millimeter wave frequencies, the operating frequency is typically a significant fraction of the f_{MAX} obtainable in the CMOS process leading to switching times which are a significant fraction of the period of the PA's input. Thus, class E tuned designs can be used at millimeter wave frequencies since they can still provide high efficiency. The output network of a class E PA consists of a shunt capacitor, C_1, a series resonator, L_2 — C_2 and a load, R. The DC supply voltage V_{DD} is transformed by the on-off switching actions of the transistor into an RF voltage which is composed of components at the switching frequency and several harmonics. The unwanted harmonic frequencies are filtered out by the series resonator L_2 — C_2. The magnitude of the residual harmonics in the output voltage at the load will be small if the quality factor of the series resonator is high. The output network of the class E PA is designed so that its transient response leads to voltage and current waveforms that satisfy the three conditions enumerated in section 1.1. It also transforms the load impedance at the drain of the active device into the correct impedance required for class E operation.

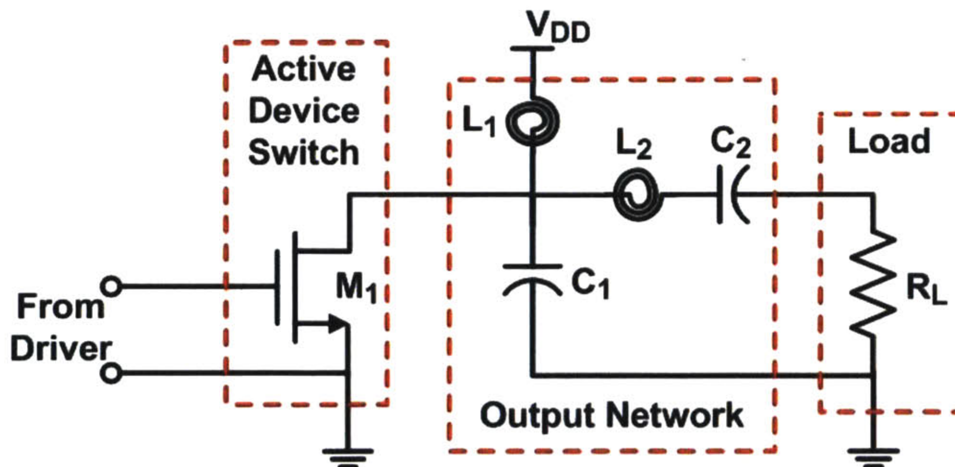


Figure 2-4: Diagram of ideal class E power amplifier

The active device is modeled as a single-pole, single-throw switch that can have a small non-zero resistance in the "on" position; a large non-infinite resistance in the "off" position, and turn on

and turn off switching times that could be non-zero. As the switch is driven at the desired operating frequency, DC energy from the power supply is converted to RF energy at the operating frequency and several harmonics. A series resonant circuit is usually included in the output network to suppress or filter out these harmonics from the signal going to the load. In addition, the output network is used to transform the load impedance into a value which is required for the zero voltage switching (ZVS) and zero voltage-derivative switching (ZVDS) voltage waveforms that will be described later. In order to obtain maximum efficiency, the switch is operated at approximately 50% duty cycle. This is called the "optimum" operating mode of the class E PA. There is some incentive to employ non-50% duty cycle "sub-optimal" operation as well, such as reduced maximum drain voltage stress and reduced maximum drain current.

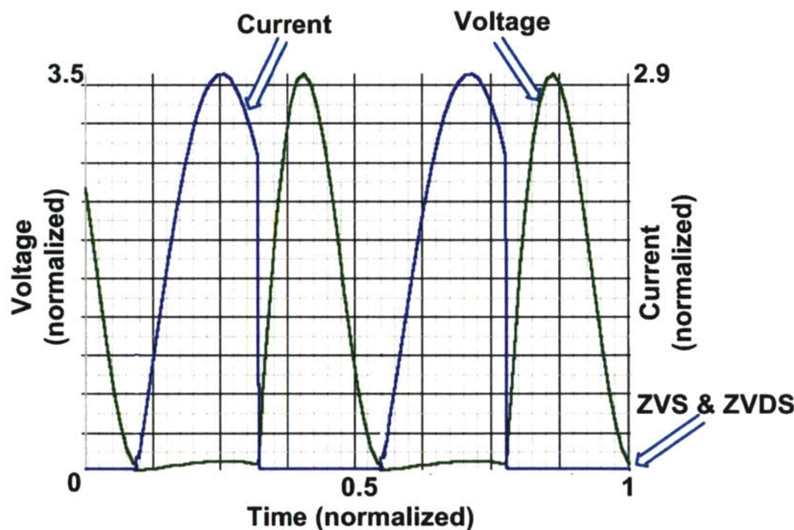


Figure 2-5: Non-overlapping voltage and current waveforms at the drain of the active device.

To minimize the dissipation in the active device, the class E PA is designed so that the voltage and current waveforms which are shown in Fig. 2-5 satisfy a number of conditions.

- The voltage across the active device when current flows through it is minimized. A transistor with a low on voltage (small channel resistance) can satisfy this requirement.

- The current through the active device when a voltage exists across it is also minimized. The minimization of leakage current in the transistor will satisfy this requirement.
- The active device's switching time should be minimized. This reduces the time during which appreciable current and voltage exist simultaneously and power is lost. Fulfilling this condition is achieved by appropriate driver design, transistor selection and the design of the output network. The goal is to have the driver provide an input signal large enough to drive the transistor into strong inversion within a small fraction of the driving input signal's period.
- A voltage delay should be introduced during switch turn off. During the turn off transition, the voltage across the active device should remain close to zero until the current has reduced to its minimum value (which should be close to zero). Then the voltage across the switch or active device can increase. This condition ensures that the voltage across the switch does not rise to a significant value while there is current flowing which will lead to substantial losses and degrade the PA's efficiency.
- The voltage returns to zero before the start of the turn on transition. The transient response of the output network ensures that during the period when the active device is turned off, the voltage rises up to a maximum value which is designed not to exceed the maximum voltage stress that can be tolerated by the active device. The voltage then falls back down to zero. It is essential that the voltage reaches zero prior to the active device or switch turning on. This will prevent substantial losses that would occur from a simultaneous occurrence of voltage across and current flowing through the switch.
- The slope of the voltage transition at switch turn on should be zero. This makes it possible for the PA efficiency to be robust to modest mistuning of the output network. A zero slope of the voltage transition during turn on ensures that there is some leeway in the time interval

during which the switch can turn on and still satisfy the requirement of zero voltage switching (ZVS). Thus, the region where there is simultaneous appreciable value of voltage across and current through the active device is small ensuring high efficiency operation of the class E PA. This condition is called zero voltage-derivative switching (ZVDS). Another positive effect of ZVDS is a slow switch turn on will not lead to substantial power losses because the voltage is not changing rapidly during the turn on transition as long as the voltage is already close to its minimum value.

2.2.1 Design Equations for Ideal Class E PA

A practical implementation of the class E PA is shown in Fig. 2-4 which is redrawn in Fig. 2-6 for convenience and adapted from [8]. The active device switch is implemented with a NMOS transistor, M_1. The inductor, L_1 is an RF choke which is used to bias M_1. The inductance of L_1 is large enough that it can be assumed it provides a relatively constant DC current. C_1 is the net capacitance at the drain of transistor M_1. R is the load to which the PA will deliver power and might also be the input port resistance of a bandpass or lowpass filter used to remove the extra harmonic content from the output signal. Any load reactance is absorbed into L_2 and/or C_2. When transistor M_1 is turned off, the output network (composed of C_1, C_2, and L_2) produces a transient response similar to that of a damped second-order system with initial conditions depending on the energies stored in the passive components. During the turn off transition, C_1 keeps V_{DS}, the voltage across M_1, low until the current flowing through the transistor has dropped to zero. This delays the voltage rise and ensures that there is little power dissipated in the active device. The values of C_1, C_2, and L_2 are selected to satisfy the conditions of ZVS and

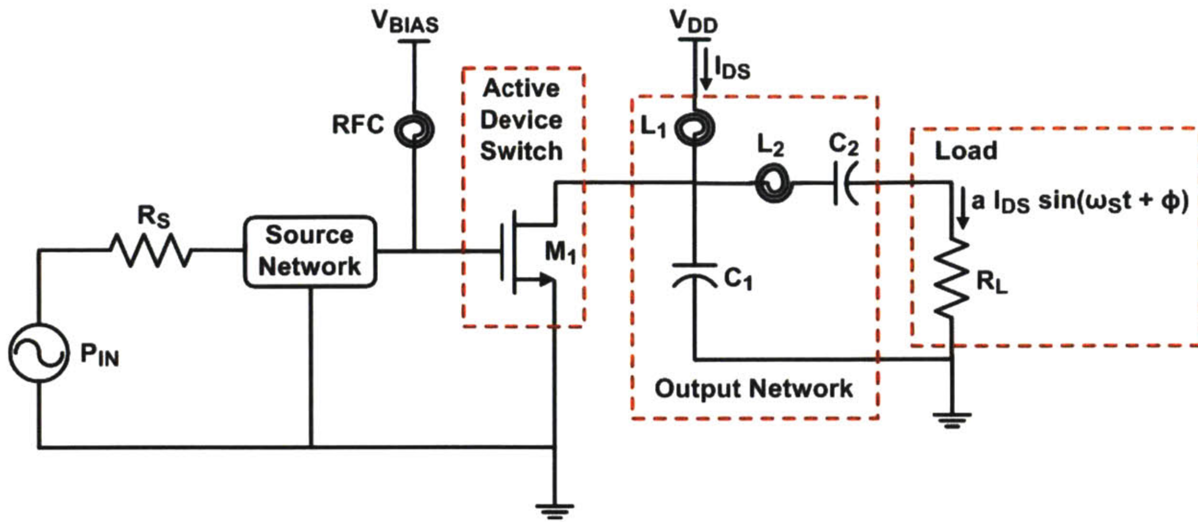


Figure 2-6: Diagram of ideal class E power amplifier

ZVDS enumerated in the previous section. With a 50% duty cycle and switching frequency, f, the values these components are designed to satisfy the following three mathematical relations simultaneously:

1. At the turn off transition, $v_s = 0$ at $t = T_s/2$ where T_s is the period of the input driving signal and v_s is the voltage across the active device. For optimum operation, the duty cycle = 50%. This is the ZVS condition.
2. At the turn off transition, $dv_s/dt = 0$ at $t = T_s/2$. This is the ZVDS condition.
3. The loaded quality factor, Q_L of the output network can be chosen to be any practical value. The selection of Q_L is a tradeoff between low harmonic content in the output signal (high Q_L) and higher efficiency (low Q_L). In practical integrated systems, Q_L is limited by the poor quality factors of integrated inductors.

Assuming the output network has a high quality factor, Q_L, the output current is essentially sinusoidal and of the form

$$i_{\text{out}} = a\, I_{DS} sin(\omega t + \phi) \tag{2.1}$$

Since the RF choke only allows a DC current to flow through it, the difference between the output current and the RF choke DC current will flow through the switch—capacitor combination. When the switch is open, the current will flow through and charge capacitor, C_1, producing a voltage across it given by [11]

$$v_s(t) = \frac{1}{C_s}\int_0^t I_{DS}\left(1 - A\, sin(\omega t' + \phi)\right) dt' \tag{2.2}$$

If we assume that the ZVS condition occurs at t=0 (switch turn on), the integral above evaluates to

$$v_s(t) = \frac{I_{DS}}{\omega C_s}\left(\omega t + A(cos(\omega t + \phi) - cos\, \phi)\right) \tag{2.3}$$

Using the ZVS and ZVDS conditions at $t = T_s/2$ with (1.3), the values of a and ϕ can be uniquely determined:

$$a = \sqrt{1 + \frac{\Pi^2}{4}} \cong 1.862 \tag{2.4}$$

$$\phi = -\arctan\frac{2}{\pi} \cong -32.48 \tag{2.5}$$

Employing Fourier series expansions, the fundamental component of the load voltage at the transistor's drain is determined as [11]:

$$v_{s1} = a_1 I_{DS} \sin(\omega t + \phi_1) \tag{2.6}$$

where the constants $a_1$and ϕ_1 are given by

$$a_1 = \frac{1}{\omega C_s}\sqrt{\frac{\pi^2}{16} + \frac{4}{\pi^2} - \frac{3}{4}} \tag{2.7}$$

$$\phi_1 = \frac{\pi}{2}\sqrt{arctan\left(\frac{2\pi}{8-\pi^2}\right)} \tag{2.8}$$

The phasor of the impedance presented to the transistor's drain at the fundamental by the output network can now be determined from load current in (1.1) and load voltage in (1.6)

$$Z_{net1} = \frac{v_{s1}}{i_{\text{out}}} = \frac{a_1}{a} e^{\phi_1 - \phi} \cong \frac{0.28015}{\omega C_s} e^{49.0524^{\text{o}}} \tag{2.9}$$

This is the required phase angle that needs to be provided by the output network for the PA to operate in class E mode. The drain voltage, V_{DS} and the resistance, R presented by the output network at the drain of the active device are constrained by the desired output power, P, to be delivered to the load. Since the maximum value of V_{DS} is also constrained by the breakdown voltage of the process and the largest possible supply voltage V_{DD} should be selected for highest efficiency, the desired output power, P essentially specifies the load resistance at the active device's drain. This resistance is given by [8]:

$$R = \frac{V_{DD}^2}{P} \left(\frac{2}{\frac{\pi^2}{4}+1} \right) = 0.577 \frac{V_{DD}^2}{P} \tag{2.10}$$

The inductor L_2 is calculated using the selected value of the output network loaded quality factor, Q_L,

$$L_2 = \frac{Q_L R}{2\pi f} \tag{2.11}$$

Where f is the frequency of the input driving signal. The value of Q_L is chosen as a tradeoff between low output voltage harmonic content (high Q_L) and high efficiency (low Q_L).

To satisfy the ZVS and ZVDS conditions at the switch turn on transition in Fig. 2-5, C_1 and C_2 are calculated as [8],[12]

$$C_1 = \frac{1}{2\pi f R\left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right)} \tag{2.12}$$

$$C_2 \cong \left(\frac{1}{(2\pi f)^2 L_2}\right)\left(1 + \frac{1.42}{Q_L - 2.08}\right) \tag{2.13}$$

It should be noted that L_2 is not necessarily resonant with C_1 and C_2 at the operating frequency, f.

2.3 Implementation of 60-GHz Class E tuned PA

The design of the 60-GHz class E tuned PA was carried out in the order of steps shown in Fig. 2-7. An iterative design methodology was necessary because of the feedback created by the gate to drain capacitance, C_{gd}. Any changes made to a particular section affects the other sections which will all need to be updated. The iteration continues until an acceptable level of performance is obtained. Each section is first implemented with ideal passive components. Then the ideal passive components are replaced by transmission line equivalents as successive sections are implemented.

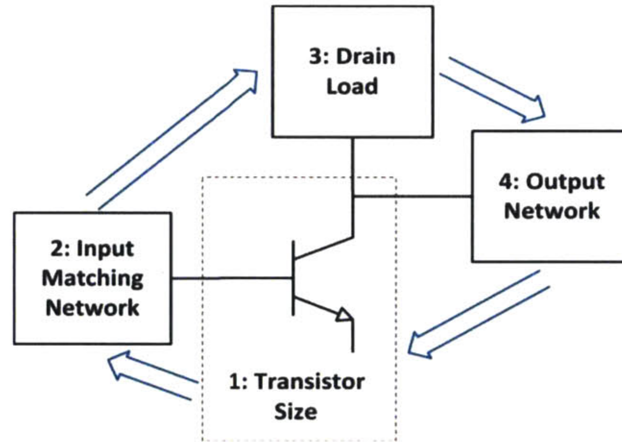


Figure 2-7: Design methodology

A starting point for the PA design was to calculate the component values R, C_1, C_2, and L_2 using the ideal class E PA design equations presented by Sokal et al. [8] and Raab [12]. The load resistance, R was computed from Eq. 2.10 using a supply voltage $V_{DD} = 0.9V$

$$R = 0.577 \times \frac{0.9^2}{10^{-2}} = 46.737\ \Omega \tag{2.14}$$

Using the value of R, $C_1$is calculated from Eq. 2.12

$$C_1 = \frac{1}{2\pi \times 60 \times 10^9 \times 46.737 \left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right)} = 10.42\ \text{fF} \tag{2.15}$$

The value computed for C_1 is significantly smaller than the transistor's drain-source capacitance and will be difficult to realize on chip. Thus, a smaller value of $R = 10\ \Omega$ was selected in order to increase the size of the shunt resistance C_1 calculated previously and hence make its realization on chip easier. The calculated value of the RF power to be delivered to the load will increase to 16.7 dBm as seen from Eq. 2.10 but practical constraints of the PA's implementation ensures that the actual delivered power will be less. Moreover, we seek to deliver a much power as possible to the load from a given supply so this increase in calculated output power is advantageous.

Using Eqs. 1.11, 1.12 and 1.13, the other components in the output network as calculated as

$$C_1 = 48.7\text{ fF};\ \ C_2 = 41.1\text{ fF};\ \ L_2 = 212\text{ pH} \tag{2.16}$$

The peak current target for the PA was $I_{pk} = 30$ mA calculated using the 3V breakdown voltage of the process, the equivalent DC resistance offered by the class E PA to the power supply and equations in [8] and [12]. The load resistance, R, will eventually be transformed to 50 Ω by the transmission line equivalent of the output network.

2.3.1 Transistor Size

It is necessary for the transistor to be large enough to rapidly discharge the shunt capacitance at the transistor's drain at turn on in a small fraction (10%) of the input signal's period. At turn on, a class E PA implemented using an ideal switch should have no voltage across the shunt capacitor (C_1 in Fig. 2-6) in accordance with the ZVS condition. But a practical implementation of the class E will always have some drain-source voltage across C_1 because of the non-ideal transient response of the output network (due to losses and tolerance in the values of passive components) and the switching speed of the active device. Hence, it is necessary for the designer

to cater for the inevitability of discharging the residual charge on C_1 to ground through the active device, M_1 in Fig 2-6. Note that for a linear PA, increase in transistor size increases the transconductance, g_m, of the device and available output power. In contrast, increasing the transistor size for the class E PA is done so that the device is large enough to sink the current required to discharge the drain shunt capacitance quickly. Output power delivered to the load is increased by using a larger power supply voltage.

A family of I_{DS} vs V_{GS} (shown in Fig. 2-8) curves at $V_{DS} = 3$ V with a range of transistor width from 20 μm to 100 μm was plotted. The optimum transistor size was chosen that will carry the maximum drain current ($I_{pk} = 30$ mA) as determined by the class E equations in [8] and [12] for a reasonable change in input voltage of 175 mV while biased close to its threshold voltage. This maximum drain current is limited by the 3V AC breakdown voltage of the 32 nm CMOS SOI process technology and the fact that the voltage at the drain of a class E PA is greater than the supply voltage by a factor of 3.56. The plots were done using $V_{DS} = 3$ V so that the worst case scenario at transistor turn on can be catered for in the design. This worst case scenario is when the transient response of the output network is such that the voltage across the shunt capacitor C_1 is still at the peak value when the active device M_1 is turned on. The transistor was biased close to its threshold voltage of 360 mV so that an input signal with relatively small amplitude from 100 mV—200 mV is sufficient to drive the transistor hard enough to turn it on and carry a drain current $I_{DS} = I_{pk}$. It is worth noting that the active device operation would be closer to a switch if the gate is not biased and it is driven by a large sinusoid or square wave signal. The drawback of this approach is lower PAE from excessive input drive power and lower output power delivered to the load. Thus a compromise was reached to bias the active device close to its threshold voltage so that the goal of enabling the active device to carry

the peak drain current at the peak of the input signal can be achieved. In addition, increasing the gate bias of the transistor increases the power gain of the PA. When the active device bias is increased so that its starting operating point moves from the subthreshold region to the weak inversion region, the power gain available will increase as well. This was demonstrated with a 10-GHz version of the class E PA realized with ideal passive components. Fig. 2-8b shows that the peak power gain of the 10-GHz version of the class E PA increases from 13.3 dB to 17 dB when the gate bias is increased from 170 mV to 300 mV. It is necessary for the PA to have sufficient power gain so that excessive input RF energy is not needed to drive the active device defeating the purpose of the PA in the first place. The plots in Fig 2-8b also show the expected gain expansion as the input power increases when the active device is biased at 170 mV because the active device is in the subthreshold region for a larger fraction of the driving signal period.

As the transistor width is increased, the drain current rises to its peak value more quickly until the drain-source capacitance C_{gs} gets large enough to slow the down the operation of the active device. It is important optimize this switching speed – peak drain current tradeoff obtain a transistor width large enough to fulfill two conditions; (1) support the peak current, I_{pk}, required for class E operation with our target output power of 10 dBm and (2) reach the peak current in 10% of the input driving signal period [12]. If the width selected is too small, the transistor's drain current will never reach the required peak current because with a worst case scenario at transistor turn on of $V_{DS} = 3V$ and the active device in saturation,

$$I_{DS} = \mu_o C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 < I_{pk} \tag{2.17}$$

A transistor with a width of 49.5 μm and 60 fingers (875 μm finger width) was found to be satisfy the previously enumerated conditions. Caution must be used in the selection of the finger

width because excessively long fingers introduce more parasitic gate resistance and inductance and degrades the f_{max} of the transistor. A transistor finger width value chosen to be less than 1mm is found to be a good compromise for the f_{max} – output power tradeoff [13]. Transient simulations where carried out with this selected transistor size and ideal passive component values calculated for the output network in Fig. 2-6 (see Eq. 2.16) to ensure the peak current is reached in 10% of the input signal period. In the ensuing design steps, the ideal passives will be replaced by transmission line equivalents.

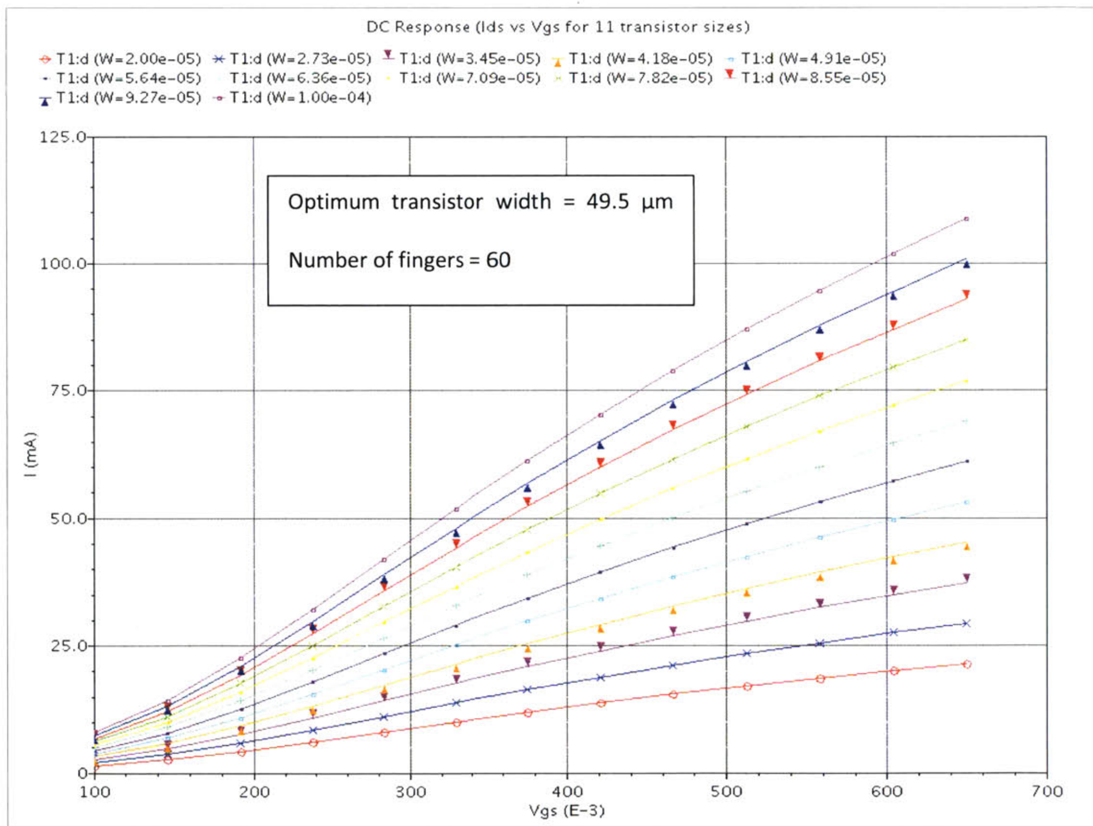


Figure 2-8: Family of I_{DS} vs. V_{GS} plots used for transistor size selection

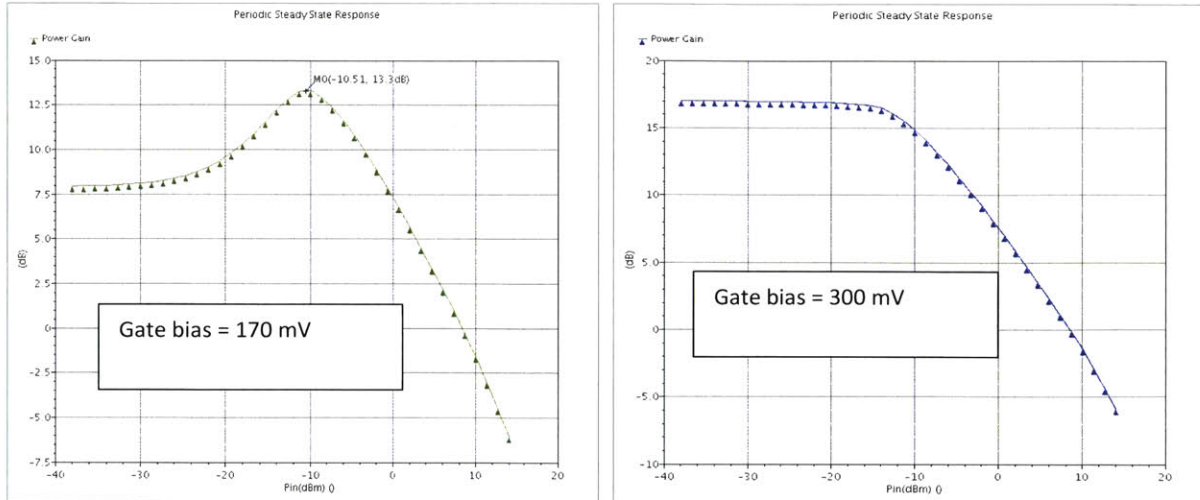


Figure 2-8b: Peak power gain variation with gate bias in 10-GHz class E PA

2.3.2 Input Matching Network

The input matching network was designed as a low-pass network with peaking at 60 GHz. Thus, limited input power can be transformed into a relatively large voltage amplitude for stronger drive of the active device. It was first necessary to determine the input impedance of the intrinsic active device. A 50 Ω load was connected to the drain of the transistor which was biased by two large ideal inductances serving as an RF chokes as shown in Fig. 2-9. The drain voltage was 0.9 V while the gate-source voltage, V_{GS} was 360 mV. Then a 50 Ω port was connected to the gate of the transistor and the S_{11} parameter determined from simulation in Cadence and plotted on a $R + jX$ Smith Chart. The input matching network shown in Fig. 2-10 was used to transform impedance at the gate of the transistor to match the 50 Ω source resistance of the PA driver. The input matching network is composed of t-line2 (105 μm transmission line), t-line1 (100 μm shunt stub) and the capacitance of the input pad.

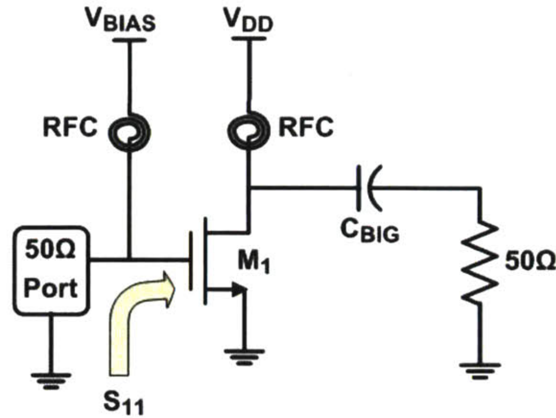


Figure 2-9: Concept diagram of design of input network

The 100 μm shunt stub is used to resonate out the input pad capacitance. The combination of the t-line 2 and C_{gs} of the NFET provides the low-pass frequency response with peaking at 60 GHz. The capacitance C_2 at the end of the shunt stub, t-line1, was implemented with two vertical natural capacitors (vncap) with a self-resonant frequency of ~70 GHz. The differential PA (Fig. 2-18b) features a virtual ground at the center of t-line6 avoiding the use of a shunt capacitance. This results into an input network with a higher quality factor and improved PA power gain. When the drain load and output networks were replaced with their transmission line equivalents, it became necessary to retune the input matching network. This was done with a combination of large signal transient simulations and small signal AC simulation to verify that the peaking in the frequency response of the input matching network remained at 60 GHz (see Fig. 2-11).

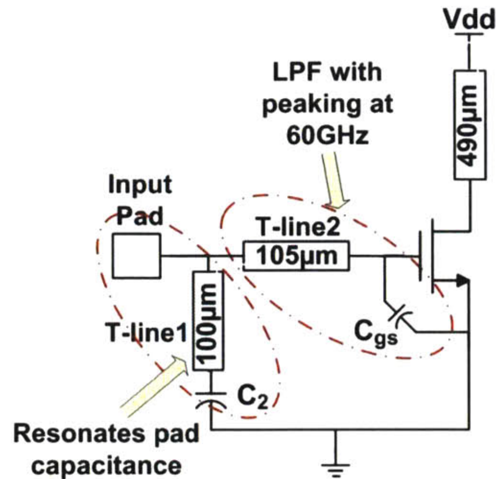


Figure 2-10: Input matching network with drain load for single ended PA.

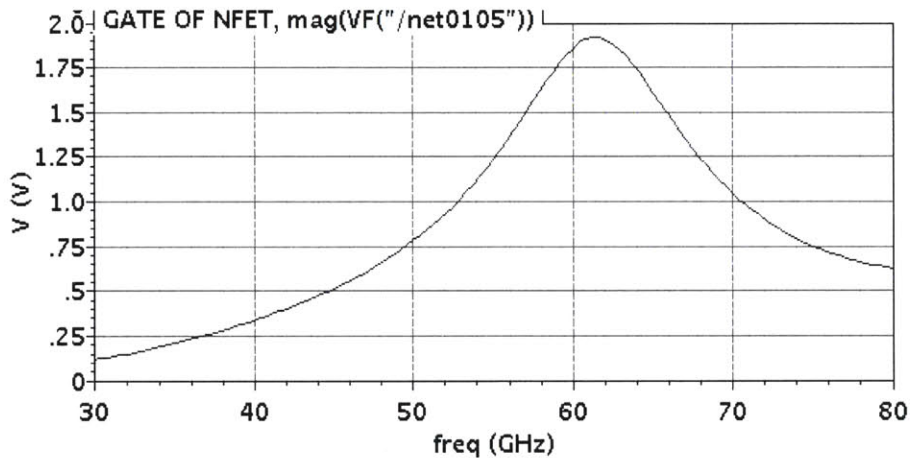


Figure 2-11: AC simulation from input pad to NFET gate showing peaking at 60 GHz

2.3.3 Drain Load

The voltage at turn-off across the transistor is determined by the net shunt capacitance, C_1 in Fig. 2-6. The value of this shunt capacitance is 48.7 fF (see Eq. 2.16) and was computed using ideal class E design equations in [8] and [12]. An initial estimate of transistor's drain capacitance was obtained by means of Z-parameter simulations of a modified version of the setup in Fig. 2-9. The input port was replaced by the transmission line version of the input matching network. The 50 Ω load at the drain was replaced with a 50 Ω port and the drain load remains as an ideal RF

choke. The results of the Z-parameter simulations indicated that the drain-source capacitance was larger than the required 48.7 fF. The RF choke used for the drain load was now replaced by an ideal inductor of smaller value which introduces the inductance necessary to resonate out enough of the device drain capacitance to obtain a net shunt capacitance equal to 48.7 fF at the drain of the active device. An inductance of 220 pH for the ideal inductor drain load was obtained from more Z-parameter simulations.

Finally, the drain load inductor was replaced by a high characteristic impedance (85 Ω) transmission line. The required length of the transmission line was estimated by matching its inductance when grounded on one end (essentially a shunt stub) to the drain load inductance of 220 pH determined previously. See Fig. 2-12 below:

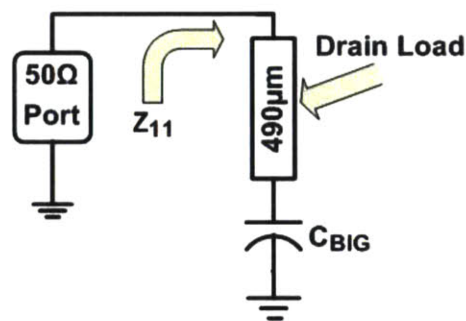


Figure 2-12: Estimating transmission line drain load using Z-parameter simulation

The ideal output network was now reintroduced and the schematic in Fig. 2-13 was obtained. At this point, the input matching network and drain load have been implemented with transmission lines. Large signal transient simulations were then used to modify the length of the drain load transmission line length until PAE > 35% with maximum saturated output power were obtained for operating frequencies from 58 GHz – 62 GHz. A transmission line of length 490 μm and characteristic impedance 85 Ω was obtained. The power supply end of the transmission line was properly decoupled to provide a good AC ground so its impedance looks like that of a

shunt inductor. The supply bypass capacitors, C_1 and C_2, were implemented using vertical natural capacitors (vncap) with self-resonant frequencies of ~70 GHz.

2.3.4 Output Network

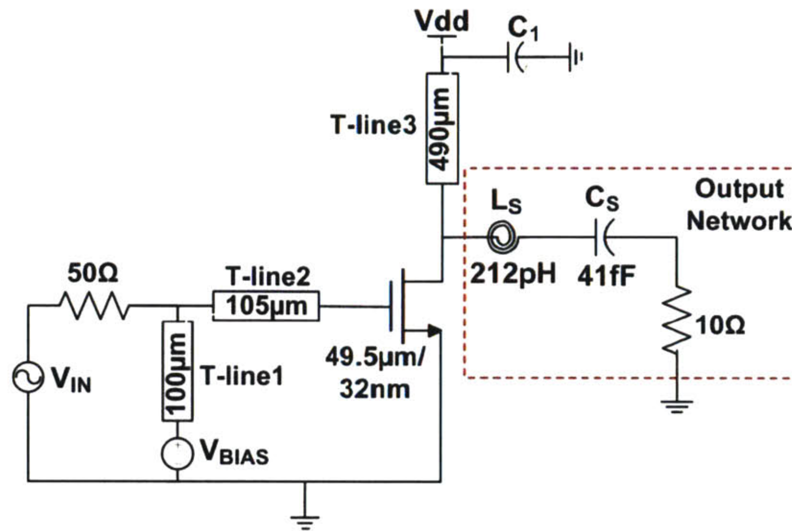
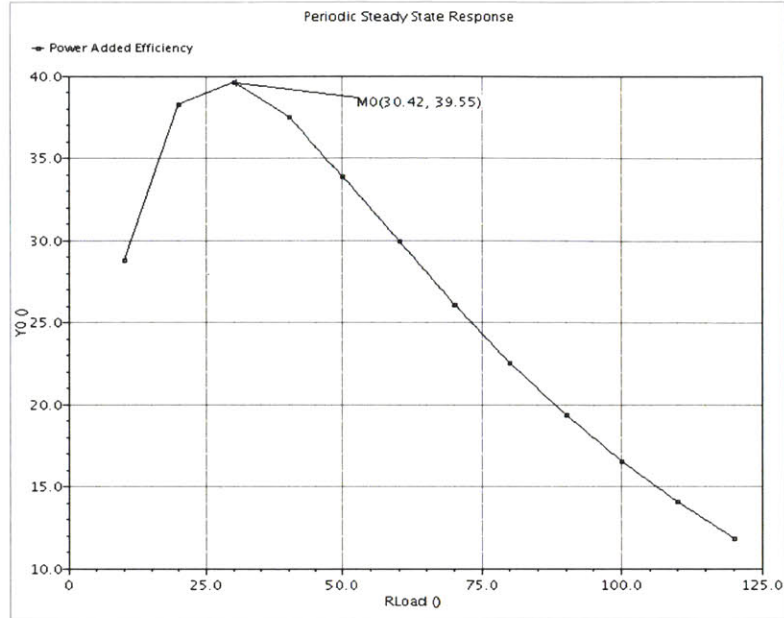


Figure 2-13: Class E tuned PA with output network implemented using ideal passives

Periodic steady state (PSS) simulations of the schematic in Fig. 2-13 were used to optimize the output network implemented with ideal passive components. PSS simulations were used instead of transient simulations because of their shorter execution time. Comparison was made between PSS and transient simulations at a single parametric point and it was confirmed that the results of both methods were very similar. Note that the input matching network was not re-tuned until the output network had been converted into its transmission line equivalent. In addition, the PSS simulations in this section did not include bondpad capacitance. The final PA design in which all networks are implemented with transmission lines will include the bondpad capacitance.

The load resistance, R, was swept from 10 Ω to 100 Ω to find the optimum resistance which results in the highest possible value of power gain and saturated output power while keeping the PAE > 30% This is essentially an acceptable value for load resistance taking into consideration



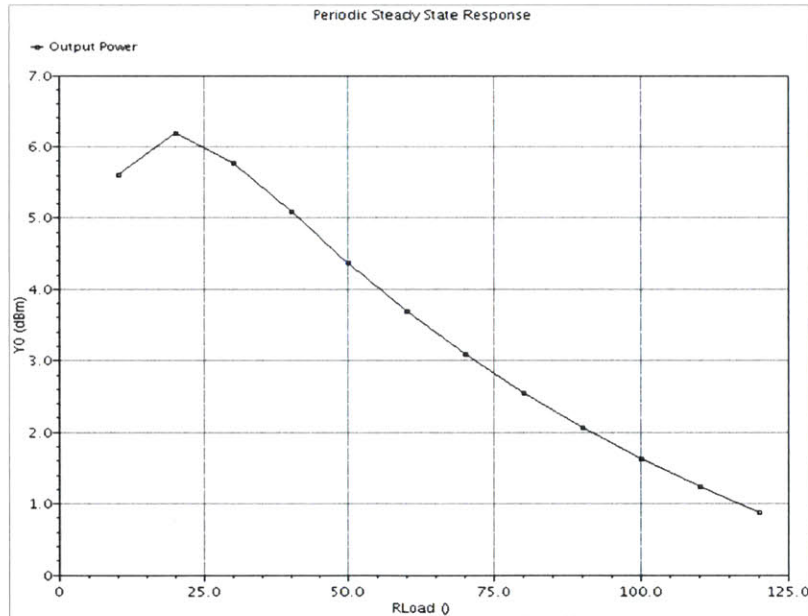


Figure 2-14: (a) PAE and (b) Output power from a PSS simulation of Fig. 2-13 with load R swept form 10 Ω to 100 Ω

the tradeoff between efficiency and output power. A value of $R = 20\ \Omega$ was selected with PAE greater than 35% while output power = 6.1 dBm (see Fig. 2-14). The input power for these PSS simulations was set to 0 dBm because the power gain of the starting point class E PA design at this input power was a reasonable value of 4 dB.

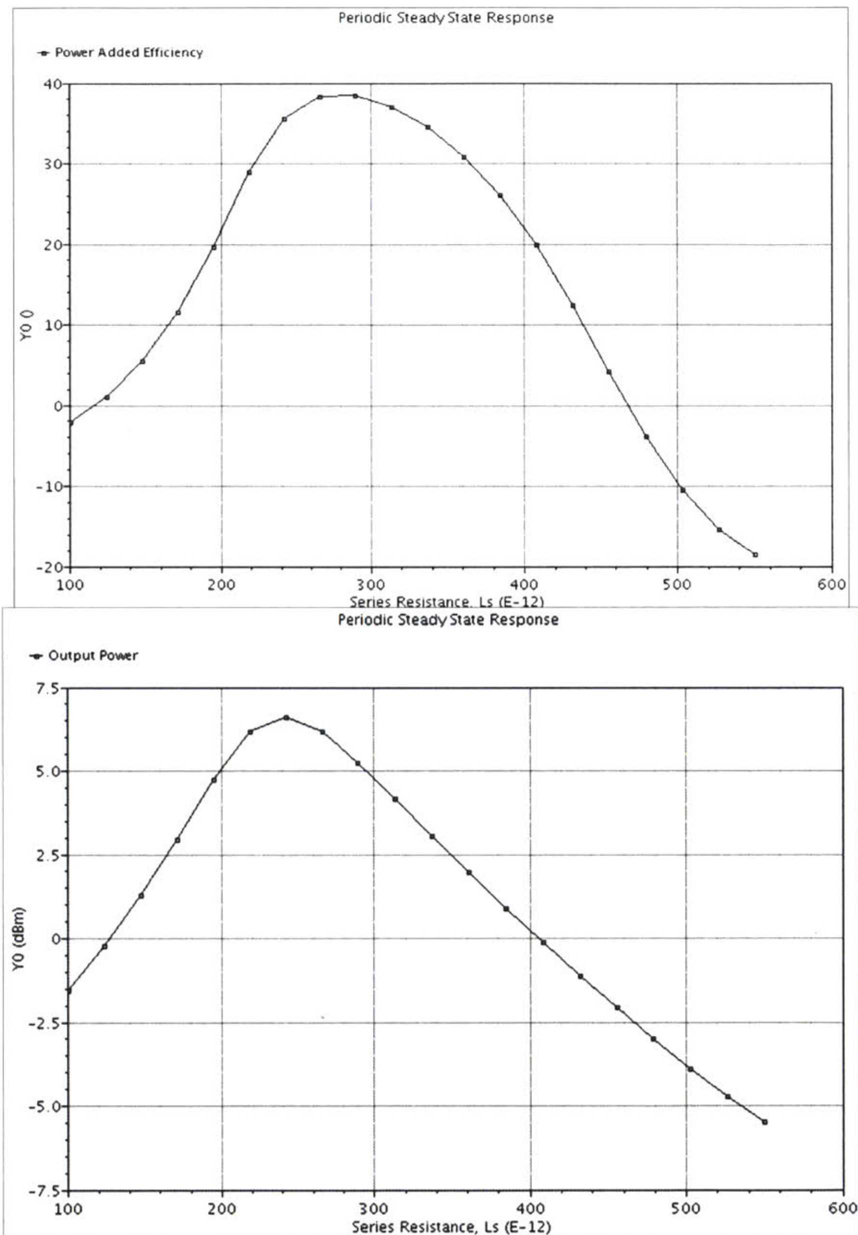


Figure 2-15: (a) PAE and (b) Output power from a PSS simulation of Fig. 2-13 with load R = 20 Ω and series inductance L_S swept from 100 pH to 550 pH.

The exercise was repeated by sweeping the series inductance L_S while keeping the other components of the output network constant. A value of L_S = 242 pH was selected as a good compromise for the tradeoff between PAE and output power. At this value of series inductance, PAE is greater than 35% and output power = 6.5 dBm (see Fig. 2-15).

The output network was then converted to a transmission line equivalent with a 50 Ohm load. The conversion was done by matching the input reflection coefficient, S_{33} at the input port of the transmission line version of the output network to the input reflection coefficient, S_{11} at the input port (NFET drain end) of the ideal output network on a Smith Chart (see Fig. 2-16 and Fig. 2-17).

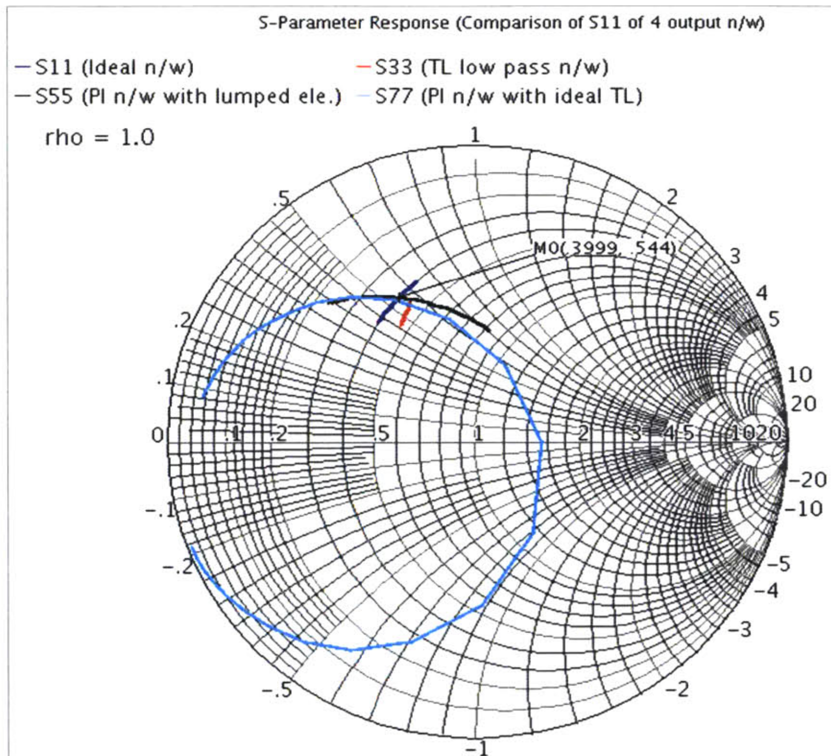


Figure 2-16: Smith Chart depicting the S parameters of alternative implementations of the output network. S_{11}: output network implemented ideal components; S_{33}: final transmission line output network; S_{55} and S_{77}: alternative network topologies that did not possess the desired low-pass characteristics.

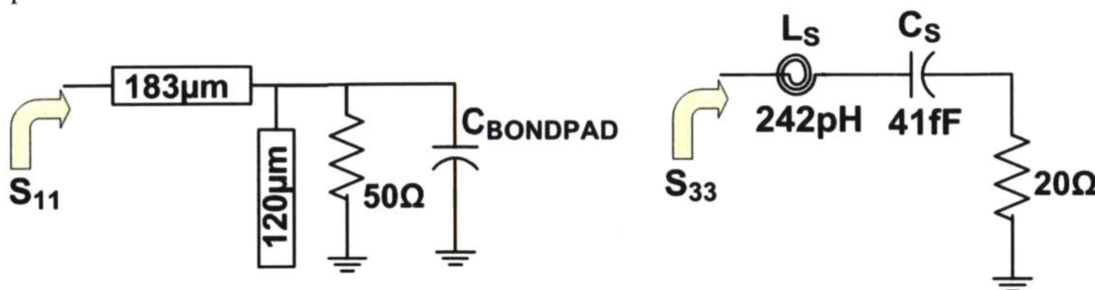


Figure 2-17: Conversion of ideal output network to transmission line equivalent. Their input reflection coefficients are matched by setting $S_{33} = S_{11}$.

The schematic of the final class E PA is presented in Fig 2-18. The output network is composed of a 183 μm transmission line, a 120 μm open stub and the bondpad capacitance. The 50 Ω load along with the bondpad capacitance is transformed by the output network into impedance required for class E operation. The parasitic via inductances L_1, L_2, resistance R_P, and parasitic capacitances C_{gs}, C_{gd} at the gate and drain of the active device were included in the PA design and are absorbed into the input matching and output networks.

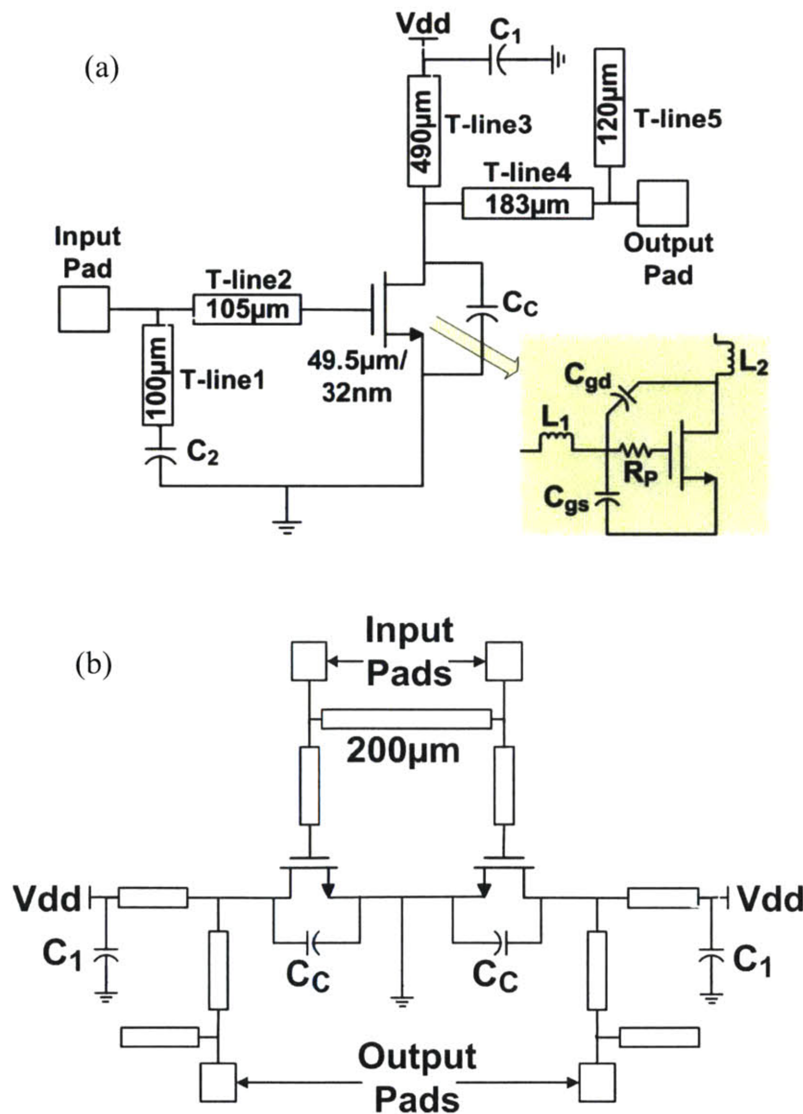


Figure 2-18: Schematic of 60-GHz class E PA (a) single-ended; (b) differential

2.3.5 FET Layout Methodology

A field-effect transistor (FET) that must handle large signals at high frequencies faces the dual challenges of electromigration compliance for high DC and AC currents, and attaining the highest possible f_T and f_{MAX}. Thus, the FET layout must minimize the relevant capacitive and resistive parasitics without compromising electromigration reliability. The FET layout uses a metal-poly ring gate terminal contacted on both sides of the device, relaxed gate pitch, and a staircase-like multiple level metallization for source and drain terminals [14]. The resulting terminal (gate, source, drain) configuration enables an easy, non-overlapping connection of transmission lines for high frequency input and output signals. Post-layout simulation results with distributed R-C parasitic extraction indicate that this layout methodology offers ~40% f_{MAX} improvement as compared to that achievable using a conventional layout.

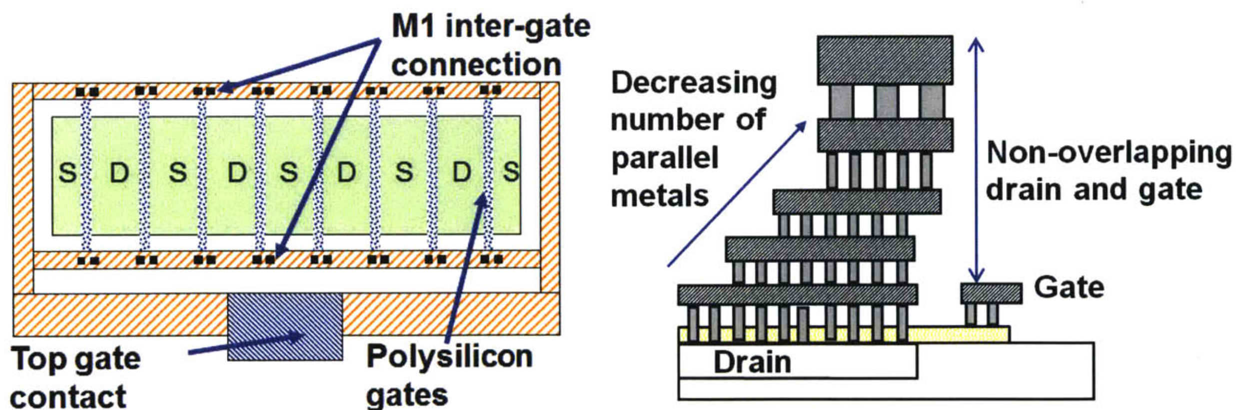


Figure 2-19: FET Layout; (a) Gate ring contact with multiple metals; (b) Staircase-like drain/source metallization [14]

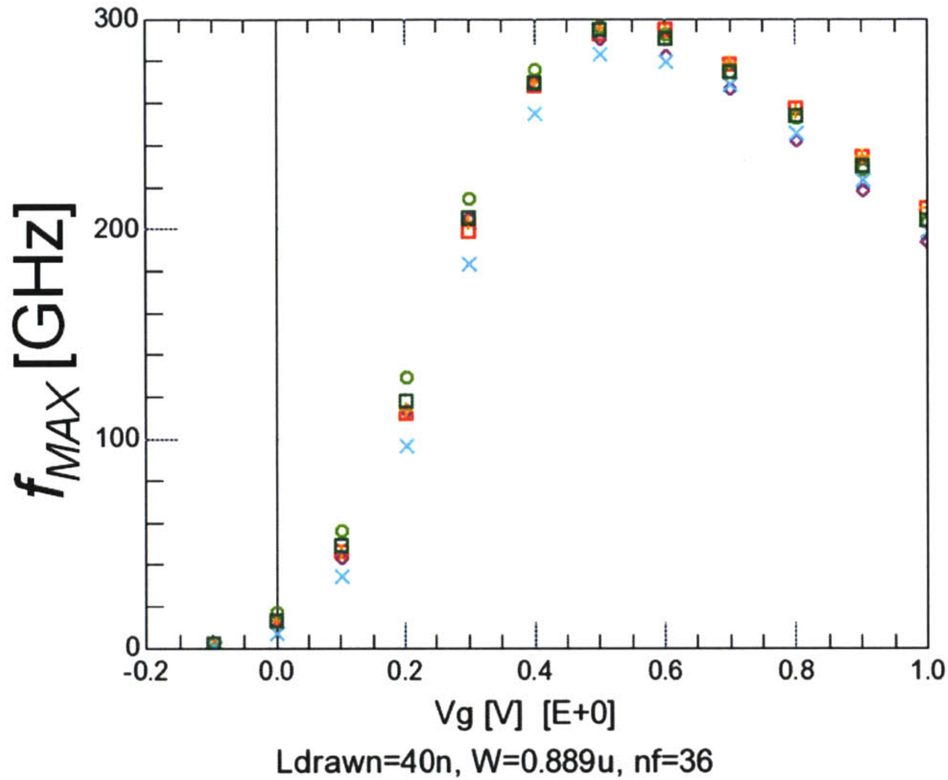


Figure 2-20: Measured f_{MAX} on 6 dies across a wafer. FET test structure includes all metals.

2.4 Simulation Results

Figure 2-21 presents the S parameter plots of the 60-GHz class E PA. The S_{11} plot indicates good input match to 50 Ω. The utility of S parameter plots is limited because the operation of the PA is essentially large signal. Fig. 2-22 presents the voltage and current waveforms at the drain of the FET simulated at 60 GHz. The plots show that the maxima and minima of the voltage and current waveforms coincide. The reduction in the overlap between the drain voltage and drain current waveforms enables the PA to achieve higher efficiency.

The simulated drain voltage and drain current waveforms depart from the ideal waveforms presented in Fig. 2-5. For instance, there is some overlap between the voltage and current waveforms leading to power loss in the active device.

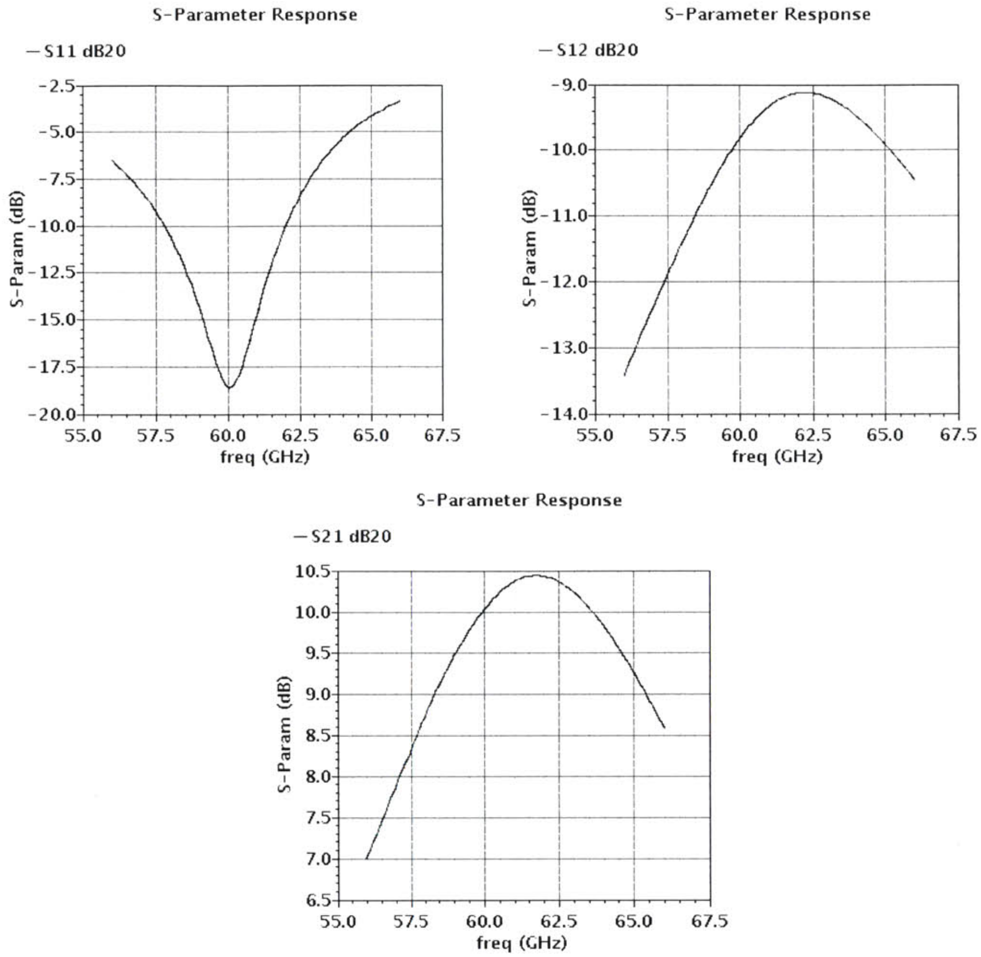


Figure 2-21: S-parameter plots of the 60-GHz class E PA

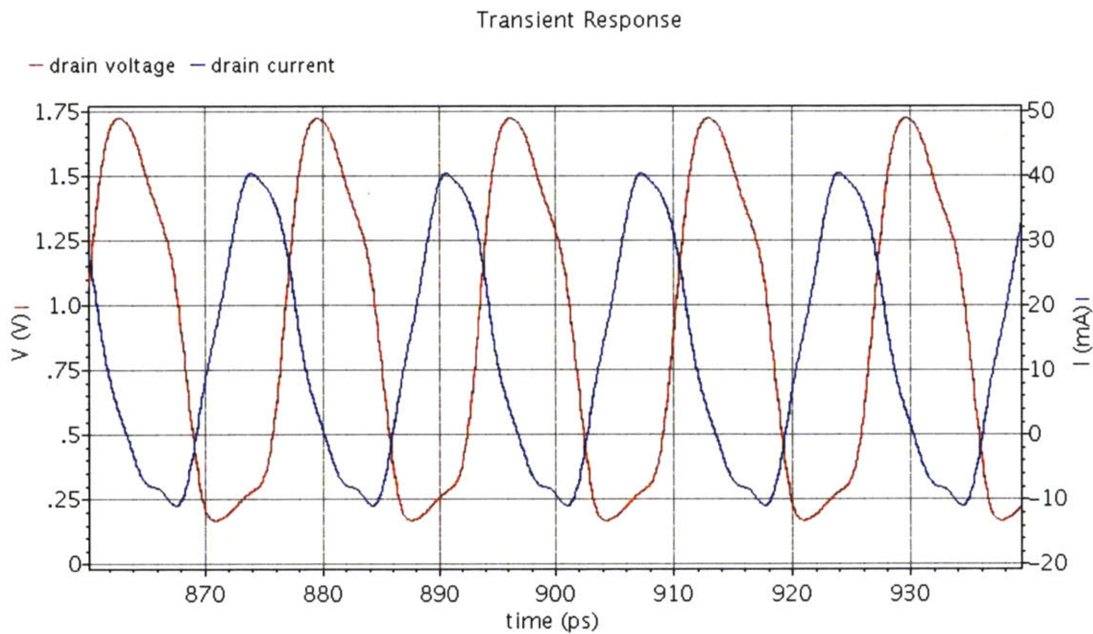
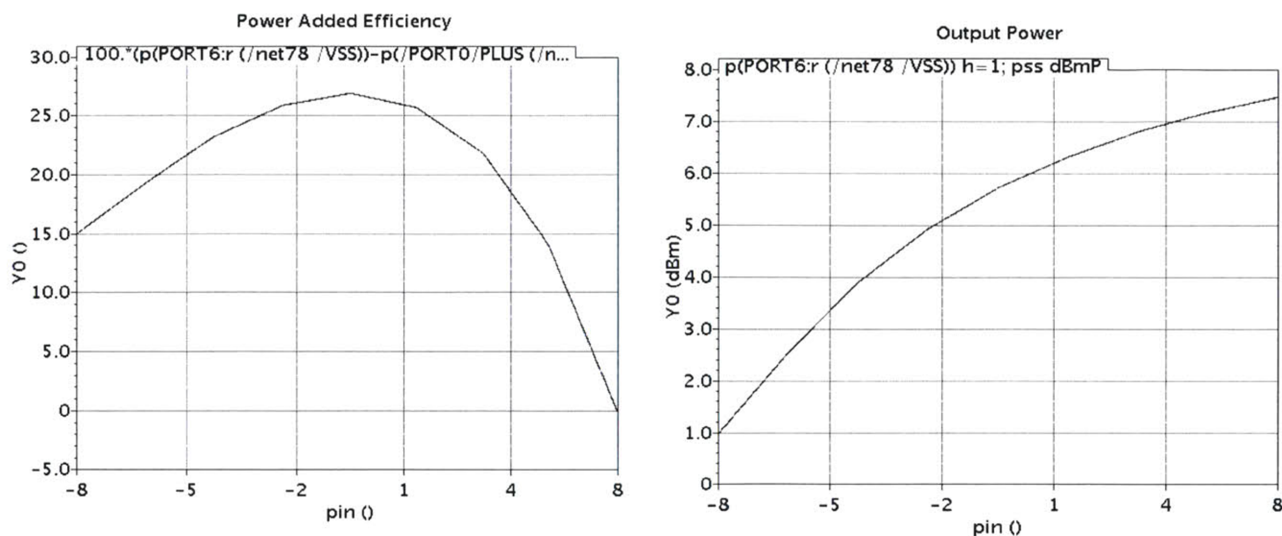


Figure 2-22: Voltage and Current waveforms at drain of active device simulated at 60 GHz.

This observation is due to a number of reasons. The f_t/f_{MAX} of the FET is 270 GHz / 300 GHz. This is just 6x the frequency of operation of the class E PA. As a result, the active device cannot switch fast enough causing its operation to deviate from that of the ideal switch useful for class E operation. The gate of the active device is biased at 360 mV which is close to its threshold. This prevents the device from operating as a true switch as it is never completely turned off. Higher efficiency could have been obtained if the gate was not biased but at it would have been at the expense of lower output power. Thus, it was decided to trade-off efficiency for higher output power. The gate bias also explains why the PA did not show the expected gain expansion as the input power is increased. Fig. 2-22 indicates that the 60-GHz PA can be said to exhibit "sub-optimal operation" [10]. The use of class E design techniques and minimization of the overlap between voltage and current at the drain provides some efficiency enhancement benefit.

Fig. 2-23 presents the PAE, saturated output power and power gain of the 60-GHz class E tuned PA. A peak PAE of 27% and power gain of 9 dB was obtained. The simulated saturated output power has a strong dependence on gate bias voltage and is not believed to be accurate because of simulator and model limitations.



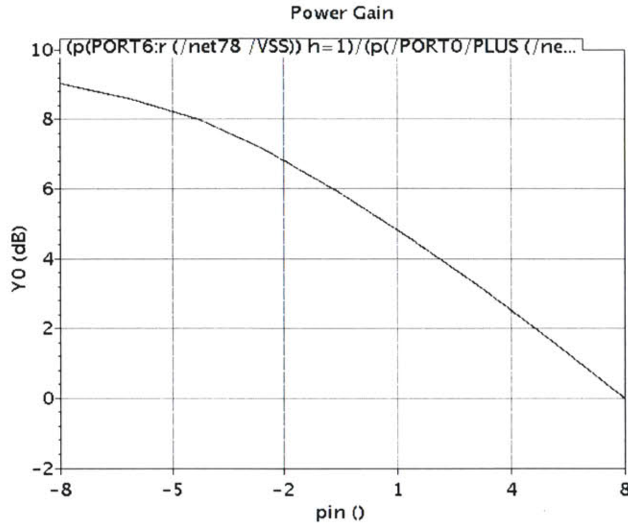


Figure 2-23: Simulated PAE, saturated output power and power gain of the 60-GHz class E tuned PA

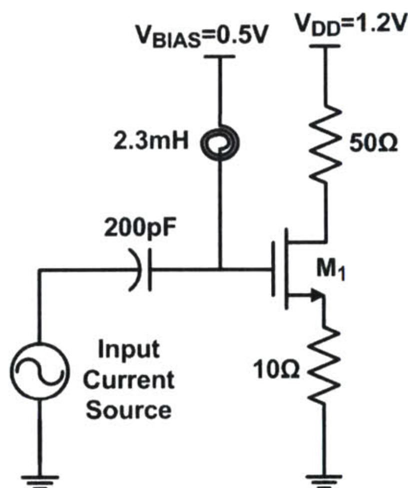
2.5 Design Insights and Discussion

Section 2.4 describes a PA that falls outside the space of what is normally considered "class E" in two important ways. First, we observe that the carrier frequency of 60 GHz far exceeds the transistor's ability to function as a convincing switch, even in this extremely aggressive process. Second, in order to achieve higher output power it was found that the transistors functioned better with nonzero bias current, further undermining the claim to being a switching, class E amplifier. In consideration of the high level of performance that the prototype ultimately achieved, however, it is a major outcome of this work that for extremely high carrier frequencies, the design methodologies foundational to traditional switching PAs can be used as efficiency enhancement techniques regardless of the choice of bias current. In this section we detail this observation, and also review the iterative design approach that made the achieved performance possible.

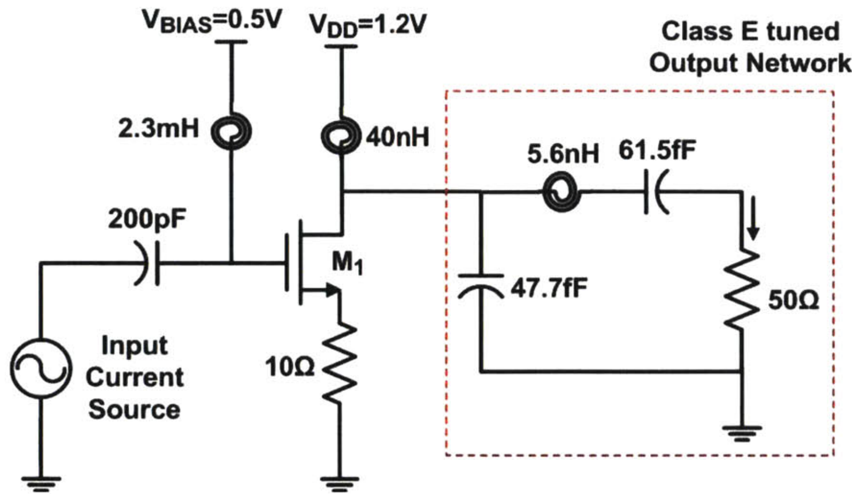
2.5.1 Class E Tuned Output Network as an efficiency enhancement technique for classical power amplifiers

The work presented in this chapter has shown that in conditions which preclude ideal class E operation, good efficiency can still be obtained. A useful insight that can be obtained from this fact is that the class E output network itself can be viewed as an efficiency enhancement technique for a more pedestrian but realizable power amplifier architectures such as class A/AB. The signal shaping produced by the class E tuned output network is sufficient to reduce the power dissipation in the active device by reducing the region of overlap of non-zero drain voltage and current.

In order to demonstrate the PAE enhancement provided by the class E tuned output network, a class A/AB amplifier was designed at 10 GHz driving a 50 Ω load in the IBM CMOS8RF 0.13 μm process (see Fig. 2-24). This operating frequency is about $1/10$ of the f_{MAX} of the process. The same schematic was modified by replacing the 50 Ω load with a class E tuned output network designed for the same operating frequency and driving the same 50 Ω load. The power added efficiencies of both PAs were compared. The results presented in Fig. 2-25 show that by just replacing the 50 Ω load in the standard class A/AB PA with a class E tuned output network, the peak PAE increased from 30% to 48%.



(a) 10-GHz class A/AB PA



(b) 10-GHz class A/AB PA with class E tuned output network

Figure 2-24: Schematic of a standard 10-GHz class A/AB PA compared to version with load replaced by a class E tuned output network.

The phase introduced in the load by the class E tuned output network (as shown in Eq. 2.9) and the output network's transient response produces enough output voltage waveform shaping and phase shift between the voltage and current at the drain of the active device to produce improvement in the PA's power added efficiency.

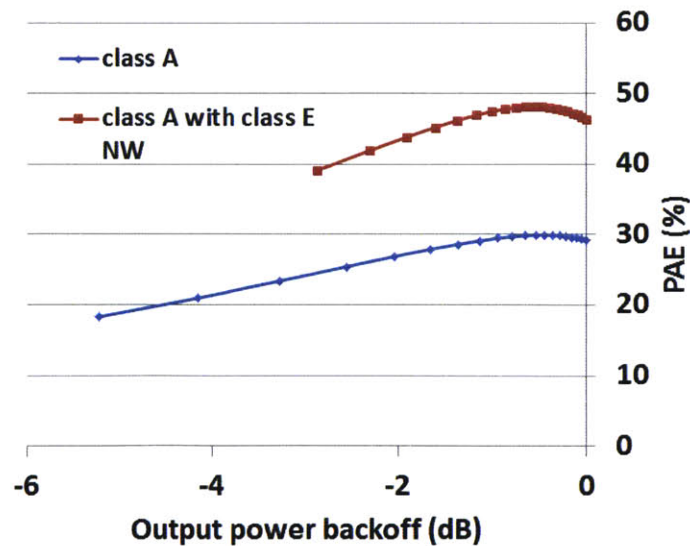


Figure 2-25: PAE of a standard 10-GHz class A/AB PA compared to version with load replaced by a class E tuned output network

The formalized iterative design approach discussed in section 2.3 was also important in achieving good PAE performance. The PA design was compartmentalized into distinct sections which were implemented separately but have a strong influence on each other. Employing the iterative design approach made possible the convergence to a final solution in an efficient manner. This approach also emphasizes the interaction between each major section of the PA and the tradeoffs that need to be made for good PA performance.

2.6 Summary

This chapter presented the design of a 60-GHz class E tuned PA. Although the operating frequency was a factor of $1/6$ of the f_{MAX} of the 32 nm SOI process, good simulated peak PAE of 27% was obtained for the single ended version of the PA. The efficiency enhancement was still obtained despite the fact the active device could not operate as an ideal switch because the region of overlap of high voltage across and high current through the FET was minimized. An iterative design approach which helps to simplify the design of the class E tuned PA was implemented. The use of an FET layout that minimizes the overlap between drain and gate transmission lines at the active device increased the f_{MAX} by as much as 40%. The availability of higher f_{MAX} provided the extra needed frequency headroom to design a class E PA that has good efficiency at millimeter wave frequencies. The intuition here is the closer the active device can operate as a switch, the higher the PA's efficiency will become.

Chapter 3

PA Measurement and Characterization

This chapter presents the measurement setup and results of the 60-GHz class E tuned PA. Important requirements needed for reliable millimeter wave measurements will be discussed. Reconciling the measurement results with suboptimal class E operation at millimeter wave frequencies will also be investigated.

3.1 Measurement Setup

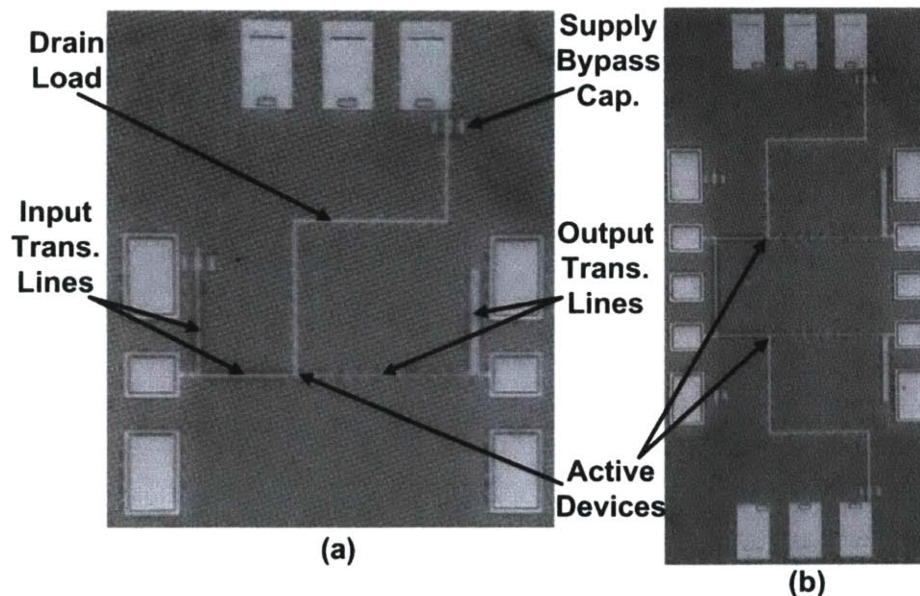


Figure 3-1: PA chip micrographs;(a) Single-ended (550 μm X 650 μm) (b) Differential (550 μm X 1.1 mm)

The PA was fabricated in IBM 32 nm CMOS SOI technology. The chip micrographs are shown in Fig. 3.1. Ground-signal-ground (GSG) bondpads were used to conduct the millimeter

wave signal on to and off the chip. The area of the single-ended PA was 550 μm X 650 μm while that of the differential PA was 550 μm X 1.1 mm. Two different setups were required to measure the single-ended (see Fig. 3-2) and differential (see Fig. 3-3) versions of the class E tuned PA. In the single-ended PA measurement setup, the 60-GHz CW signal was generated by an Anritsu MG3696A signal generator capable of producing signals up to 65 GHz. An SMA to waveguide adapter was necessary to connect the SMA cable to the waveguide that drives the probe station. A bias tee was used to bias the gate of the PA while also delivering the 60-GHz millimeter wave input signal. Power was delivered to and taken from the die by means of probe pins capable of handling signals > 70 GHz. The temperature of the probe station chuck was controlled by a Temptronic thermal power sensor. The PA output power was measured by an Anritsu ML243A power meter. The differential PA measurement setup was similar to that of the single-ended PA. The SMA cable – waveguide section in Fig. 3-2 was replaced by the structure in Fig. 3-3 so that the PA can be driven differentially. The 60-GHz CW signal from the Anritsu MG3696A signal generator is first amplified by a Spacek Labs PA driver before is it split into two signals which are 180° out of phase. The 180° phase shift is achieved by a hybrid coupler realized in waveguide called a magic tee. It has very similar properties to a rat-race coupler which in contrast is realized in microstrip. A phase shifter was included in each signal path after the magic tee to compensate for any mismatch in total path length. Because of the small wavelengths at millimeter wave frequencies, a small mismatch in the length of the differential signals path will lead to phase mismatch at the input of the PA. Swept power gain, compression and efficiency measurements were taken at room temperature (25 °C), 65 °C and 85 °C. The calibration procedure was performed at each power level and frequency to remove any nonlinear

and/or frequency dependent effects of the test equipment. The losses introduced by the SMA cables and adapters, waveguides and bias tee were also carefully calibrated out.

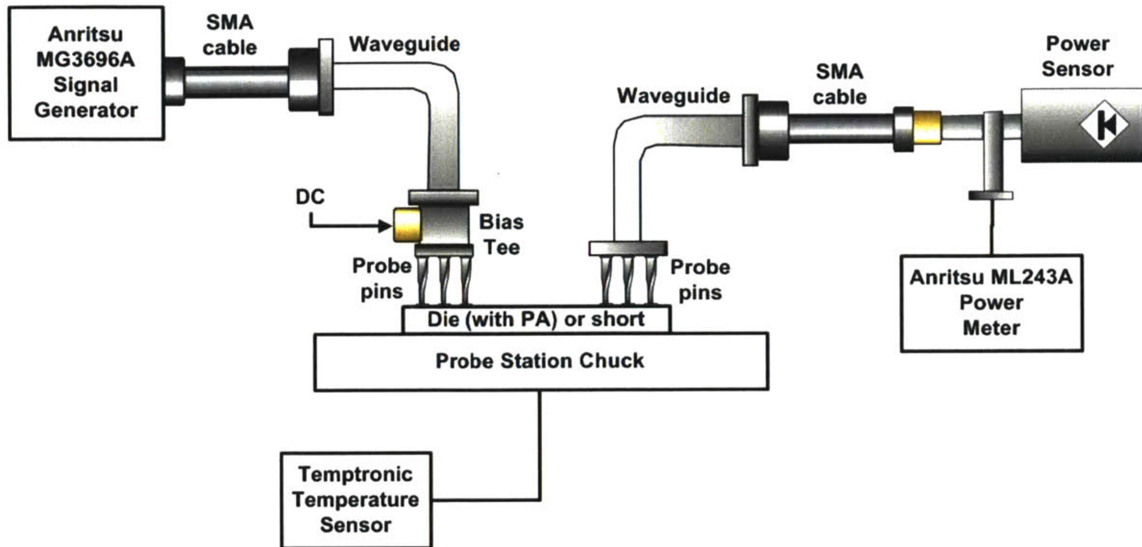


Figure 3-2: Single-ended PA measurement setup.

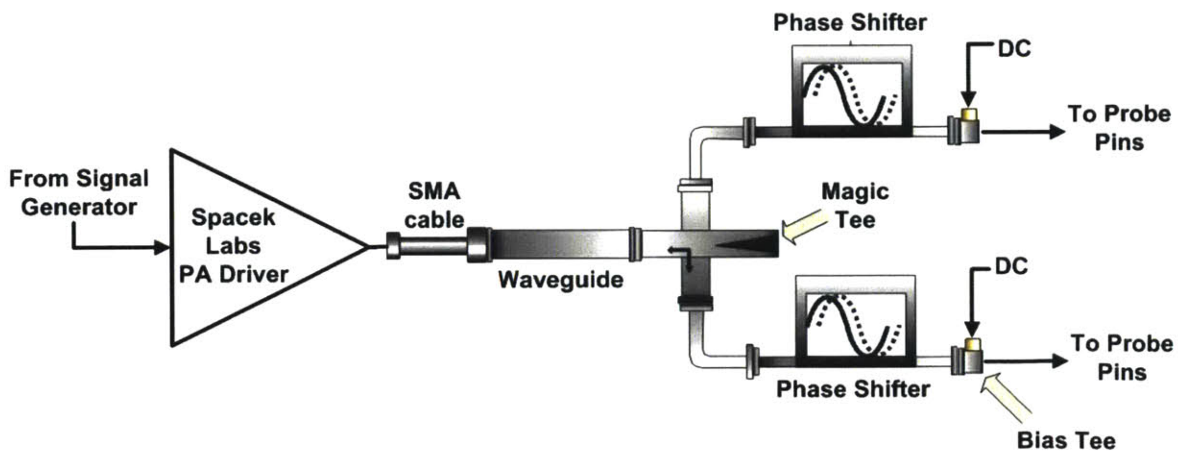


Figure 3-3: Differential PA measurement setup.

3.2 Measurement Results

As mentioned in the previous chapter 2, the gate of the active device was biased close to its threshold in order to increase the output power. This reduced the PA efficiency because of the increased static power dissipation owing to the active device not being operated as a true switch. But the efficiency – output power tradeoff was thought to be acceptable. Fig. 3-4 shows the transistor drain current versus bias voltage.

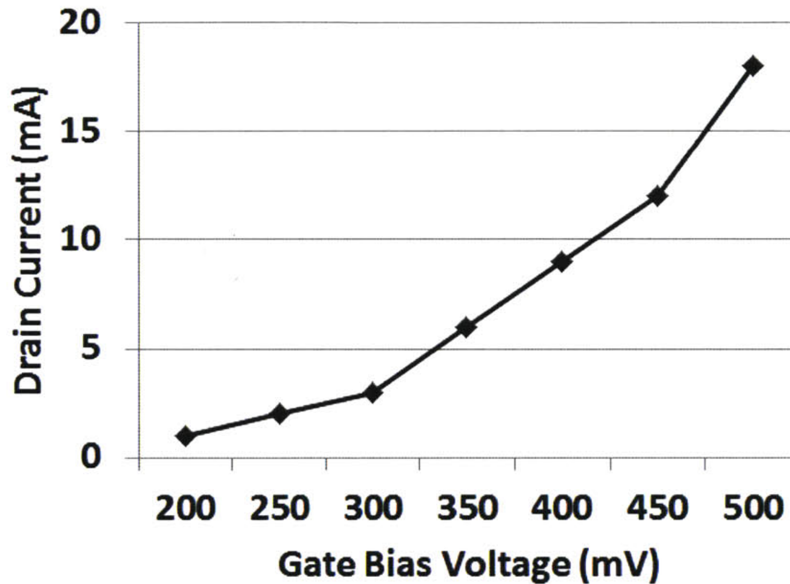
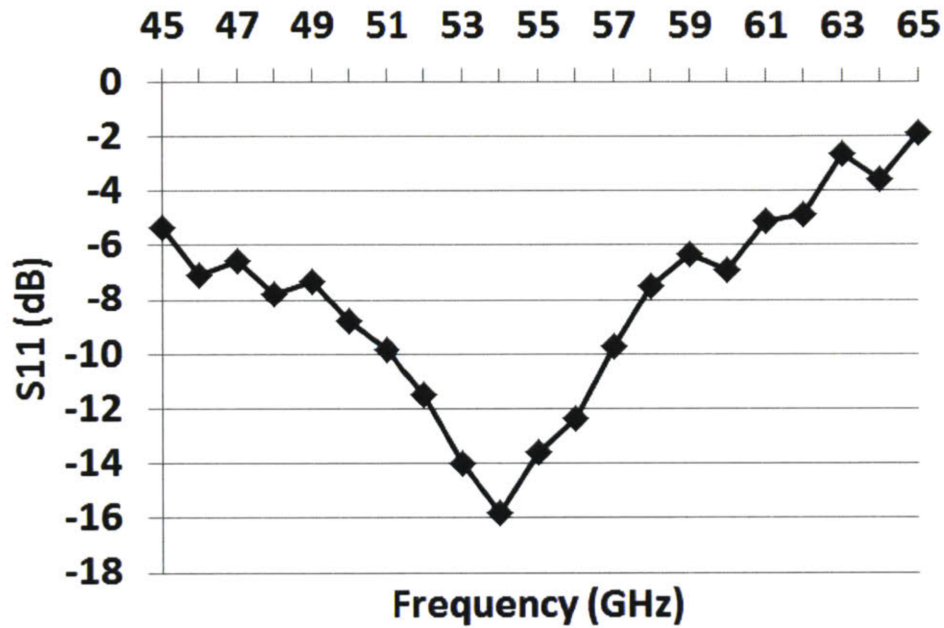


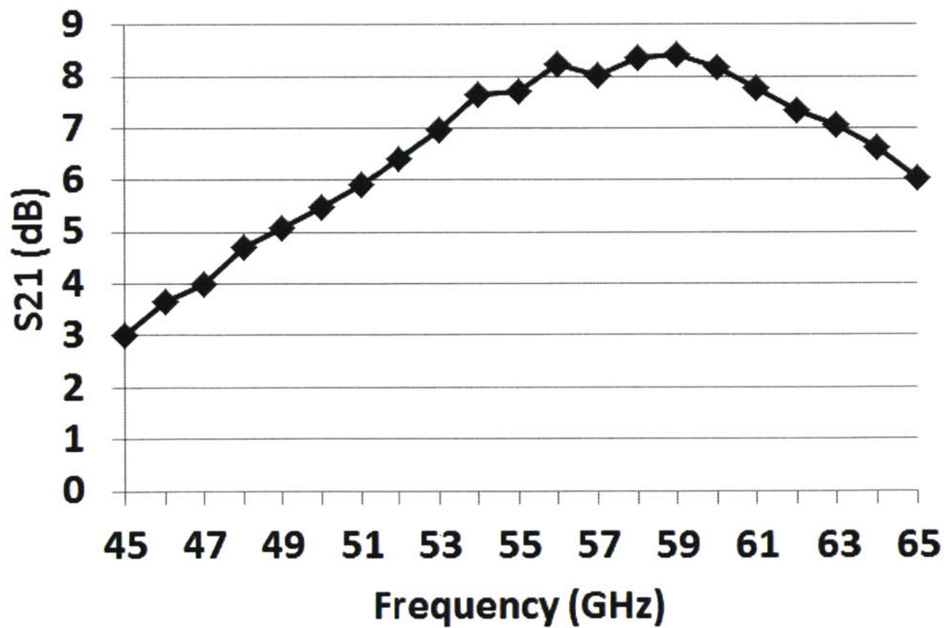
Figure 3-4: Drain current vs. gate bias voltage.

Figure 3-5 presents the measured S-parameters of the 60-GHz class E tuned PA. The measured S-parameters at 60 GHz are; $S_{11} = -6.9$ dB, $S_{21} = 8.2$ dB, $S_{12} = -10.4$ dB, and $S_{22} = -6.7$ dB. Fig. 3-6 shows that the S_{11} and S_{21} show strong variation with gate bias voltage. When the gate bias voltage of the active device is increased, it becomes easier to turn on with a small input signal. This fact is reflected in the increase of S_{21} (forward transmission coefficient or gain) with gate bias voltage. The variation of S_{11} with gate bias voltage is probably because

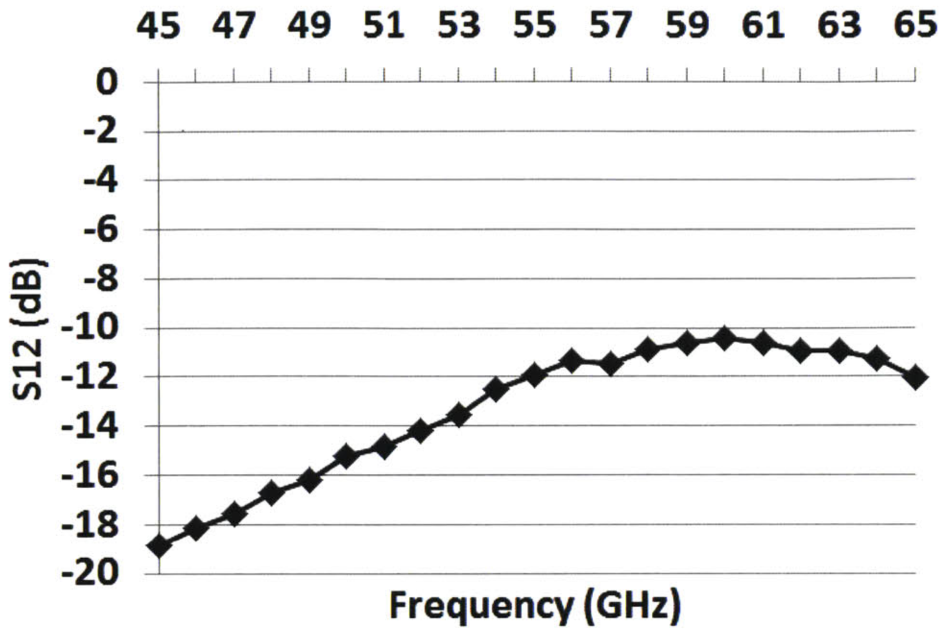
of the change in FET parasitic capacitors. In addition, the threshold voltages of the taped out FETs were different from what was used in the simulation models making it necessary to change the gate bias of the active device. As a result, the S-parameter plots are different from simulation.



(a) Input reflection coefficient vs. frequency

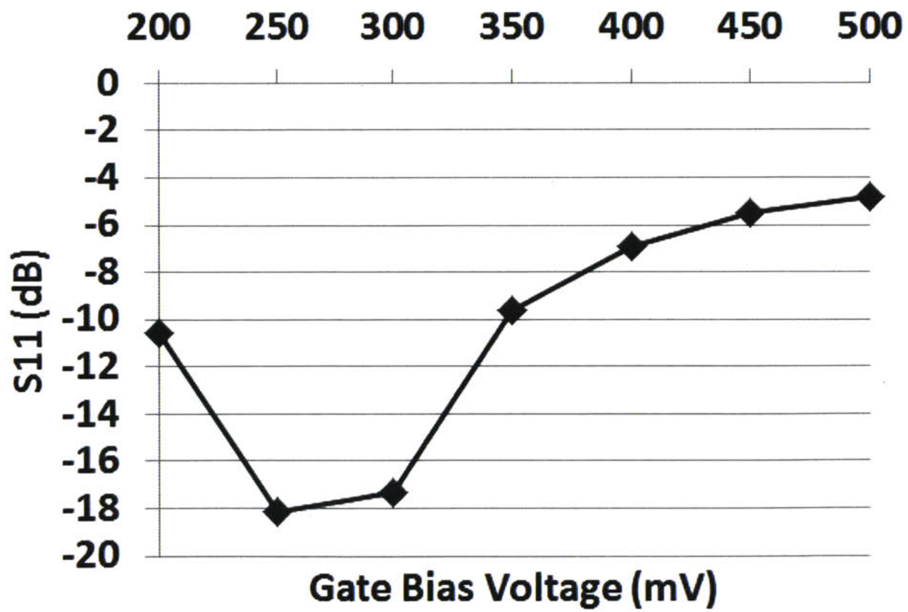


(b) Forward transmission reflection coefficient vs. frequency

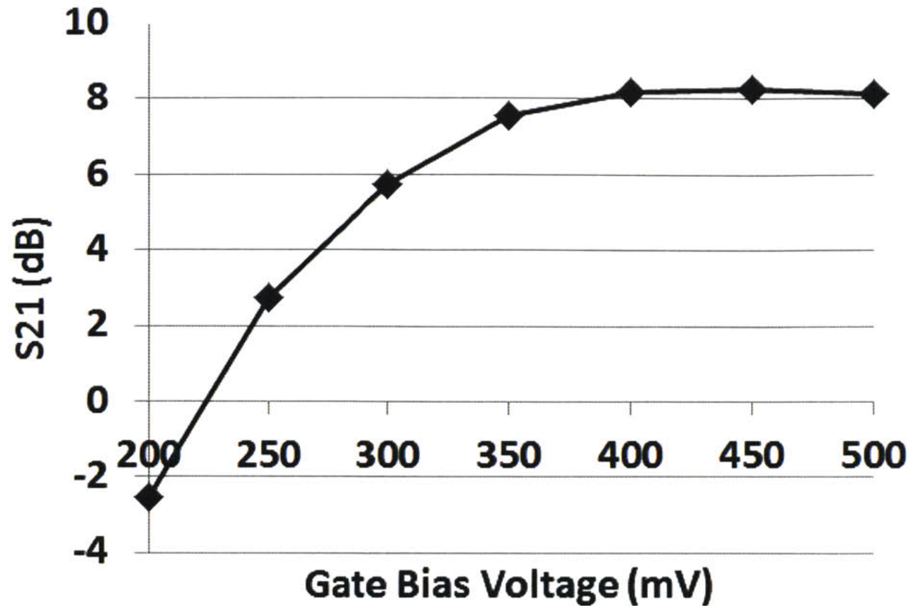


(c) Reverse transmission coefficient

Figure 3-5: S-parameters of 60-GHz class E tuned PA.



(a) Input reflection coefficient vs. gate bias voltage



(b) Forward transmission reflection coefficient vs. gate bias voltage

Figure 3-6: S parameters variation with gate bias voltage at 60 GHz

All of the measurements were performed on-wafer. Swept power gain, compression and efficiency measurements were taken with a thermal power sensor. Unless otherwise indicated, all measurements presented in Fig. 3-7 to Fig. 3-12 were taken at 60 GHz with a temperature of 25 °C, a gate bias voltage of 0.4 V and a supply voltage of 0.9 V. The measured results for the single-ended PA are presented in Figs. 3-7 to 3-11. Fig. 3-7 shows the measured PAE and power gain vs. output power at 60 GHz. A peak PAE of 27% and power gain of 8.8 dB were obtained. Fig. 3-8 presents the peak PAE, Psat and power gain at five frequencies between 56 GHz and 64 GHz. The peak PAE is greater than 21% for all frequencies. Fig. 3-9 illustrates the variation of peak PAE and Psat with drain voltage. Fig. 3-10 shows the variation in the measured peak PAE, Psat and power gain across 7 different locations on a 300 mm wafer. The peak PAE is consistently greater than 23% in all dies. This measurement was performed at a constant gate bias voltage (400 mV) and even better uniformity can be expected with constant-current biasing.

Fig. 3-11 illustrates the measured dependence of the PA performance on temperature. The PAE at 60 GHz remains above 20% up to 85 ºC.

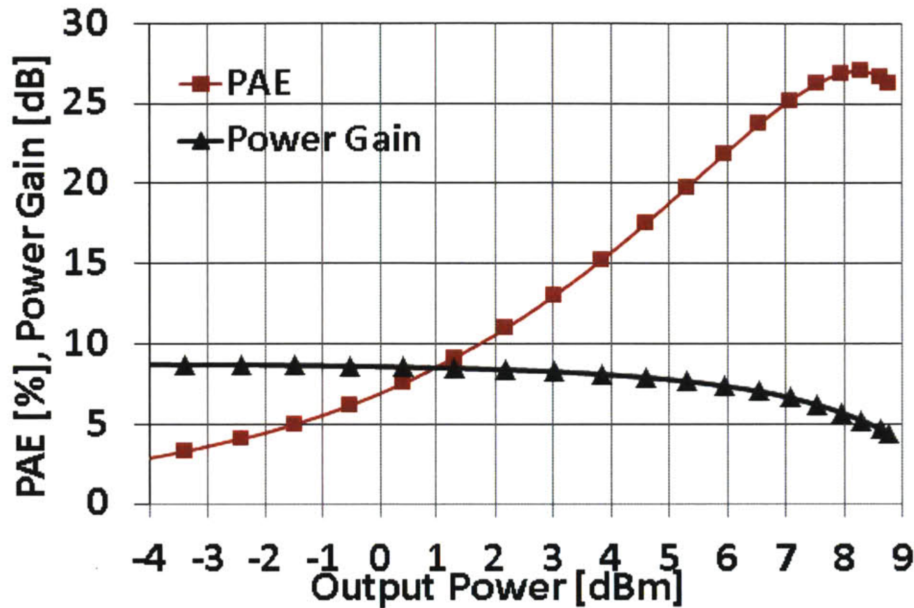


Figure 3-7: Measured PAE and power gain vs. output power at 60 GHz for the single-ended implementation of the PA

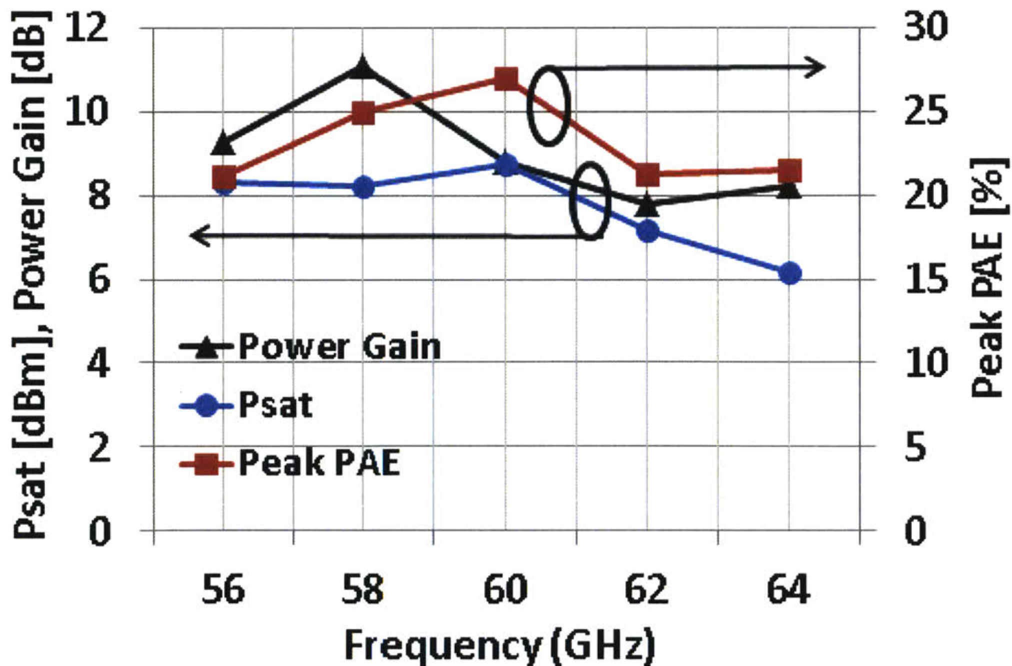


Figure 3-8: Measured peak PAE, Psat and power gain vs. frequency

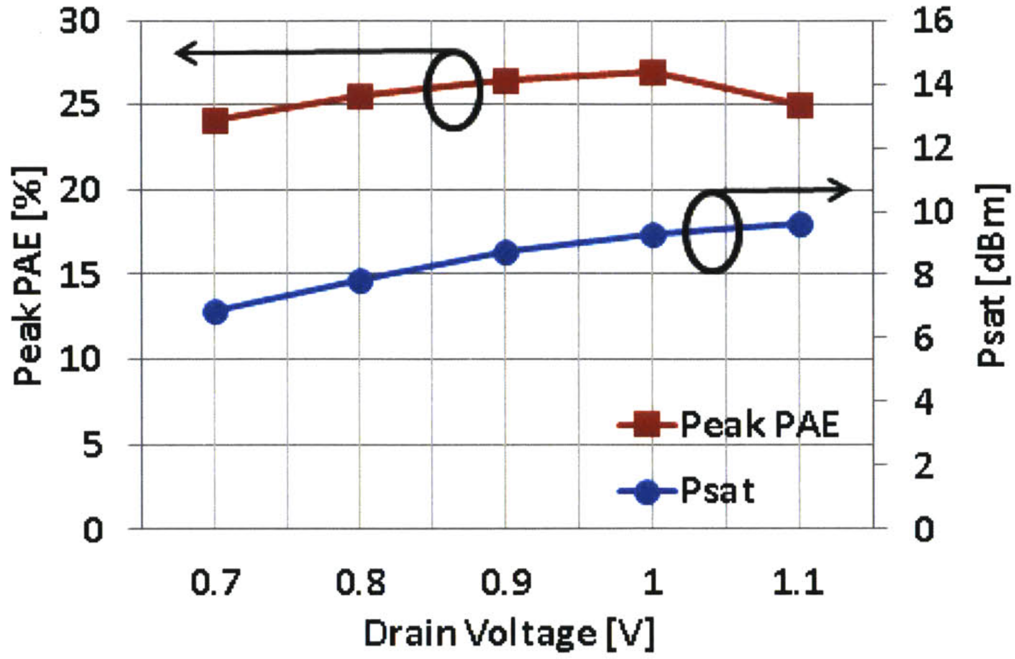


Figure 3-9: Measured 60-GHz peak PAE and Psat vs. drain voltage.

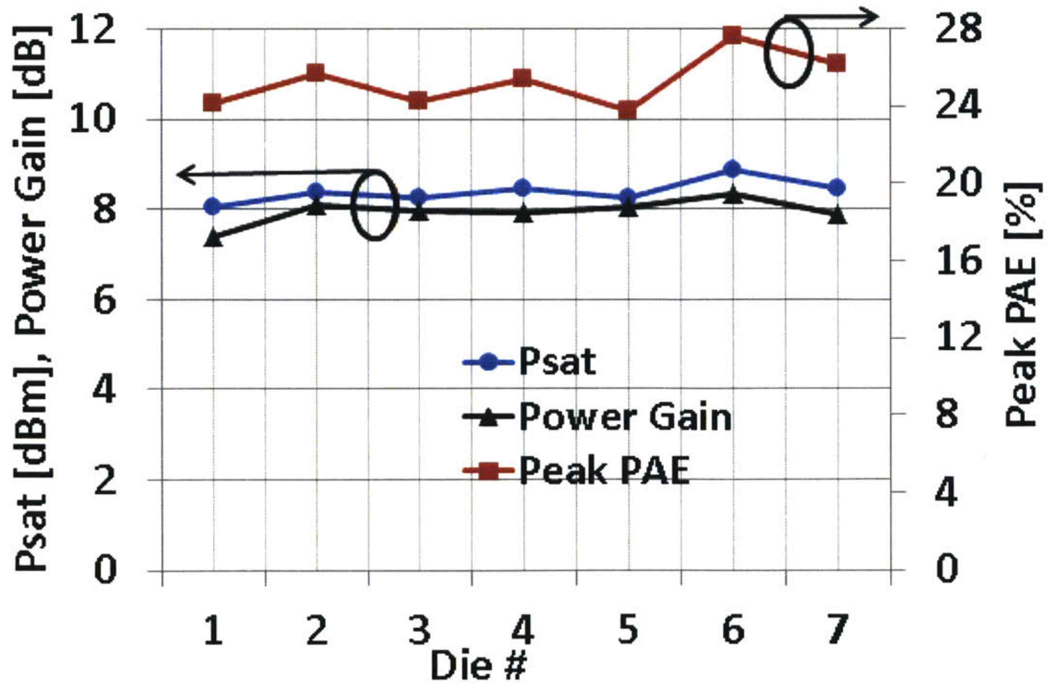


Figure 3-10: Measured process variation of PAE, Psat and power gain for 7 different dies at 60 GHz

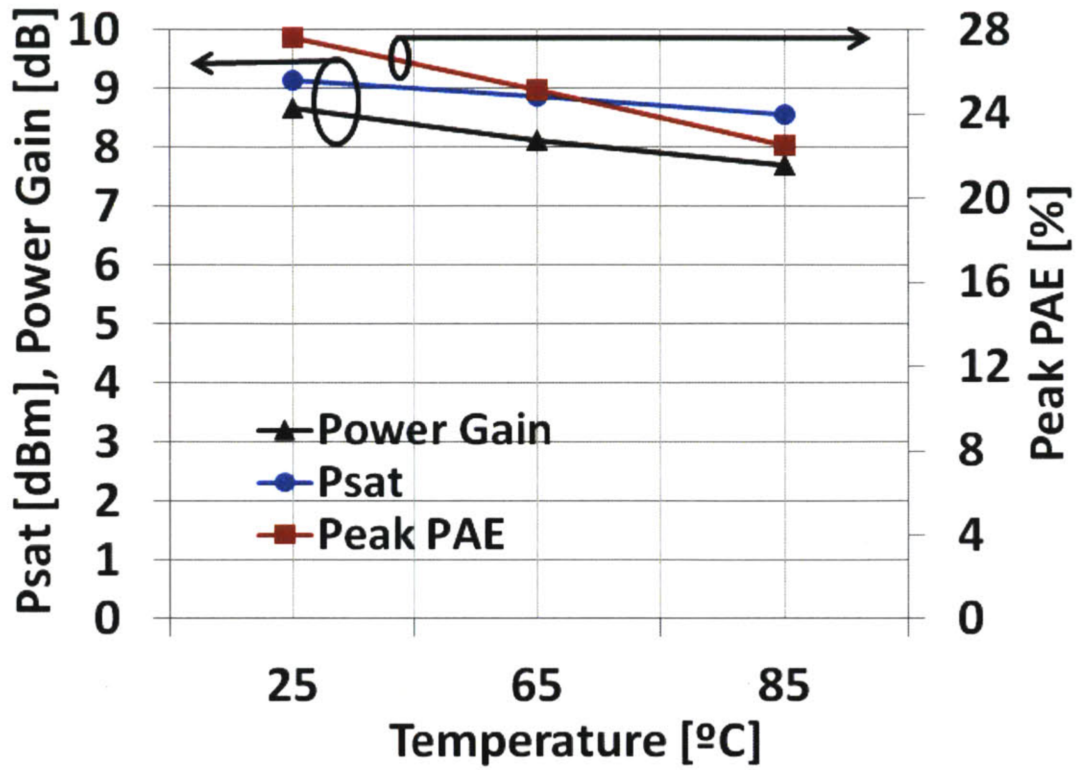


Figure 3-11: Measured peak PAE, Psat and power gain vs. temperature at 60 GHz

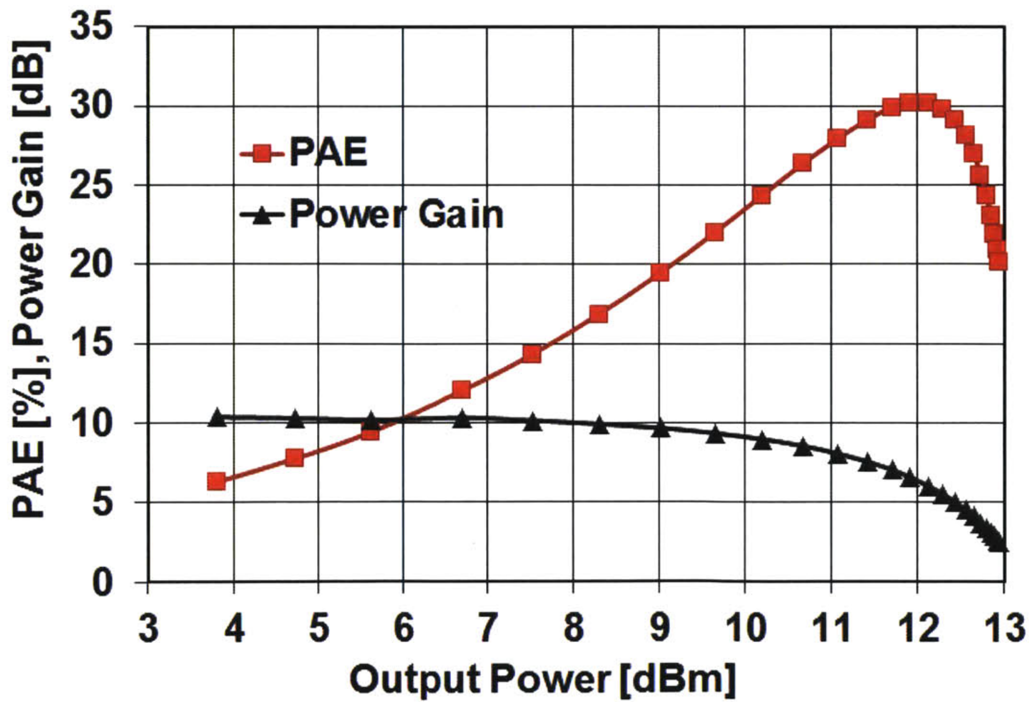


Figure: 3-12 Measured PAE and power gain vs. output power at 60 GHz for the differential implementation of the Class-E PA.

The measurement results for the differential version of the PA are presented in Fig. 3-12. This PA delivers higher output power to a 100 Ω load and, as expected from having lower losses in the input network, features ~1.2 dB higher power gain with respect to the single-ended design.

3.3 Summary

In this chapter, the measurement results of the class-E tuned PA operating at 60 GHz which has been successfully demonstrated in a CMOS SOI process was presented. The transmission line based design assures non-overlapping current and voltage waveforms at the drain of the power device while taking into account the device parasitics. Table 3.1 summarizes the measurement results along with those from other recent millimeter wave PAs [1-7]. To the best of the author's knowledge at the time of writing, this design attains the highest reported PAE for any silicon-based 60-GHz PA. The use of a smaller 32 nm process node with its higher f_{MAX} when compared to the other reported millimeter wave PAs also helped in achieving the superior PAE.

There are a few reasons which can be used to explain or justify the fact that the measurement results show good efficiency even though the active device does not operate as an ideal switch, The use of the class E output network as an efficiency enhancement technique ensures that the region of overlap of high voltage across and high current through the FET was minimized. What this implies is the signal shaping and phase shift introduced in the drain voltage waveform by the class E tuned output network is sufficient to reduce the power dissipation in the active device regardless of whether is operates as a switch or current source. The use of an FET layout that minimizes the overlap between drain and gate transmission lines at the active device increased the f_{MAX} by as much as 40%. The availability of higher f_{MAX} provided the extra needed frequency headroom to enable the active device to switch faster than it would ordinarily. It is

expected that the PAE of the power amplifier will increase if the active device can operate as close to a switch as possible.

Table 3.1: Summary of Current State of the Art in High-Efficiency Silicon-Based Millimeter Wave PAs

Reference	Frequency [GHz]	Supply[V]	Psat [dBm]	Peak PAE [%]	Remarks	Technology
This work	60	0.9	9[1]	27	Class-E, single-ended	CMOS 32nm SOI
			12.5[1]	30	Class-E, differential	
[1]	60	1.2	10.5	20.3	Two-stage, Cascode	CMOS 65 nm SOI
		1.8	14.5	25.7		
[2]	60	1	18.6	15.1	Transformer combiner	CMOS 65nm
[3]	60	1	14.85	16.2	Differential, transformer-coupled	CMOS 65nm
[4]	60	1.8	20.5	19.4	Differential, transformer-coupled	SiGe 0.13μm
[5]	45	4	18	23	Stacked FET	CMOS 45nm
[6]	58	1.2	11.5	20.9	Class-E, single-ended	SiGe 0.13μm
[7]	42	2.4	19.4	14.4	Class-E, two parallel stages	SiGe 0.12μm
	45	1.2	11.3	18		

[1]Measured at a power gain of approximately 4 dB.

Chapter 4

Theoretical Development of Energy Recovery at RF and Multi-gigahertz Frequencies

Transceivers used in modern communication systems typically have the power amplifier as the dominant component of the power budget. Several PA architectures have been employed and researched over the years including polar[16], Doherty[16], and outphasing (LINC)[17]. The outphasing PA architecture has seen renewed research interest with the advent of good power combining techniques and deeply scaled CMOS technologies that can be used to implement efficient switching PAs and complicated DSP for signal component separation and decomposition. Power amplifiers achieve best performance when their load resistance is relatively constant. This is especially important for high-efficiency switching PAs such as Class-E. The use of isolating combiners serves to satisfy the PA's constant load resistance requirement. A significant problem with the use of isolating combiners is the energy wasted in the isolation resistor when the PA is delivering low output power [18]. Outphasing PAs employing Chireix non-isolating combiners have been proposed [16], [18], [19] but have the disadvantage of being tuned for only a narrow range of outphasing angles. A power recycling technique was proposed in [20] and [21] which replaces the isolation resistor in an isolating

combiner with a rectifier so that some of the energy is recovered and returned to the PA power supply as shown in Fig. 4-1.

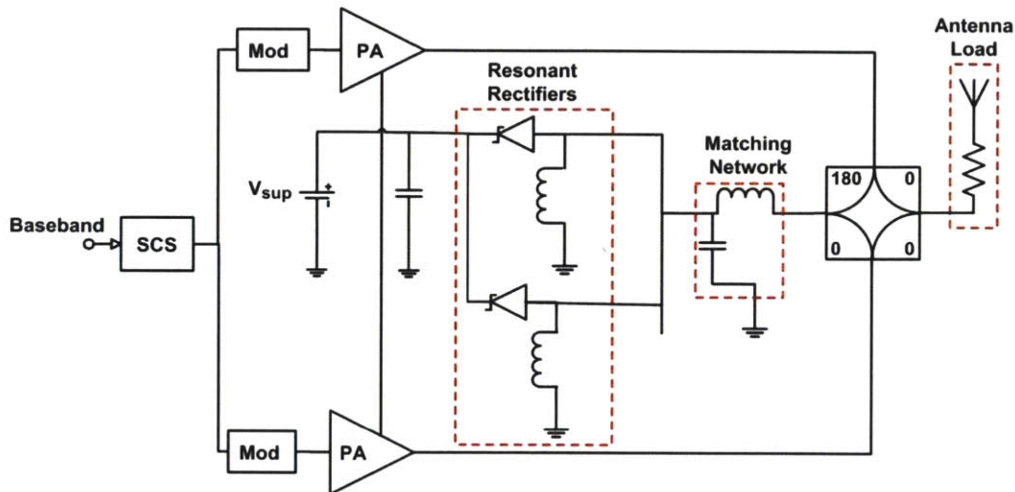


Figure 4-1: Outphasing power amplifier with power recycling network.

A drawback of this technique is the significant variation in rectifier impedance with input power. This variation will degrade the isolation between the PAs and increase the impedance variation at their outputs leading to reduced efficiency. An isolator could be placed between the rectifier and isolation port of the power combiner but this increases the cost and complexity of the final system. Moreover, the isolator will introduce some insertion loss which reduces the efficiency of the energy recycling network. Godoy et al. [22] proposed the use of resistance compression networks [23] to significantly reduce the variation in the rectifier input impedance seen at the isolation port of the power combiner. That demonstration was carried out at a 48-MHz center frequency and 20.8 W peak power.

The challenge of employing the technique of energy recovery to increase the efficiency of RF and multi-gigahertz power amplifiers will be investigated in this chapter. The use of Schottky barrier diodes (SBD) for passive rectification of the signal whose energy would be ordinarily lost

will be discussed. The limitations and necessary tradeoffs in Schottky barrier diode device size selection will be analyzed. In addition, the use of resistance compression networks in energy recovery networks at multi-gigahertz frequencies will be investigated.

4.1 Schottky Barrier Diode Design Considerations

Schottky Barrier Diodes (SBDs) are preferred for passive rectification when compared to regular PN junction diodes because of their lower forward voltage drop. SBDs typically have forward drop voltages in the range of 0.2V – 0.4V compared to 0.6V for PN diodes. The lower forward voltage drop ensures less power is lost in the diode and more can be delivered to the load or voltage regulator. In addition, SBDs are primarily a majority carrier device with signal being transmitted through majority electrons. This is in contrast to PN diodes which are minority carrier devices that utilize both electrons and holes for signal transmission and can have large diffusion capacitances in addition to the junction capacitance. As a result, SBDs can operate at higher frequencies than PN diodes making them more useful for passive rectification at RF frequencies. A drawback of SBDs is higher leakage current in reverse bias because of their smaller barrier height (Φ_{BI}) and smaller built in potential ($q\Phi_{BI}$) when compared to PN diodes.

4.1.1 Schottky Barrier Diode Model

Fig. 4-2 shows the cross sectional schematic of a SBD fabricated in a p-type substrate. The Schottky barrier junction is formed between a metal contact and the lightly doped semiconductor body quasi-neutral region (QNR). A second contact is made to the QNR through a highly doped n+ region and an ohmic metal contact.

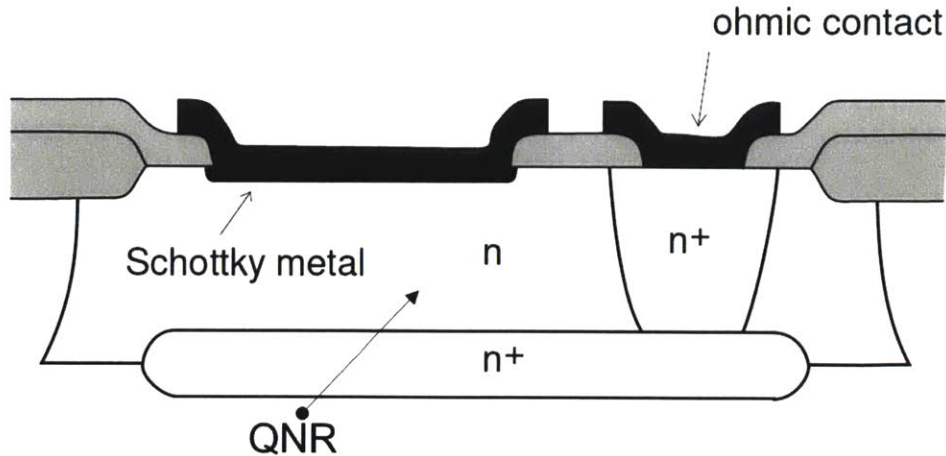


Figure 4-2: Schematic cross section of an integrated SBD [15]

A simplified circuit model of the Schottky diode which is used for circuit analysis is shown in Fig. 4-3. The general model shown in Fig. 4-3a includes an ideal diode, D_1 in parallel with a charge storage element which for a practical SBD is the junction capacitance, C_j. Both components are connected to a series resistance R_S which models the overall series resistance of the SBD. This resistance is composed of the ohmic contact resistance (between the metal contact and n+ doped region) and the resistance of the quasi-neutral region (QNR).

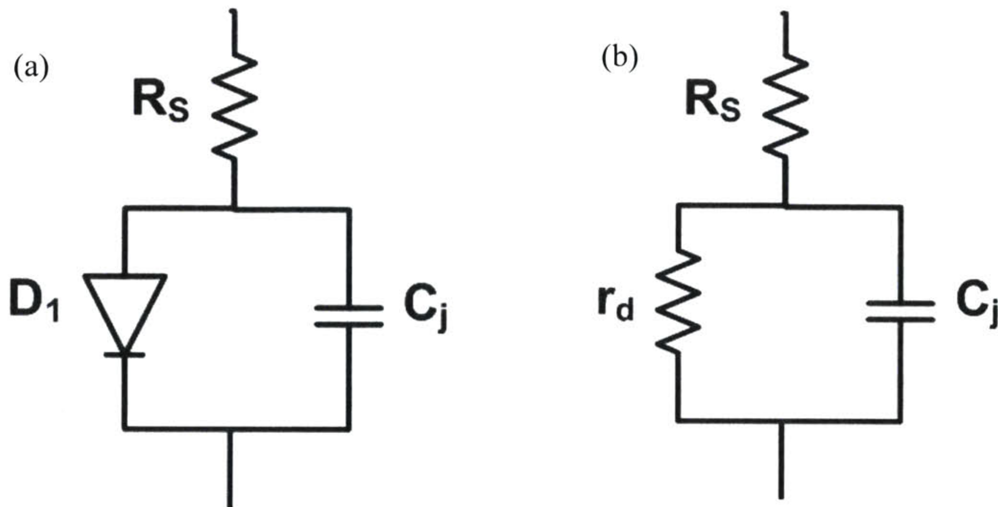


Figure 4-3: Circuit schematic model of SBD; (a) General model (b) Small signal model

The ideal diode D_1 has an exponential relationship between the current flowing through it and the bias voltage across it. If the voltage across the entire SBD is V, the actual voltage, V_j across the Schottky junction in D_1 is reduced by the ohmic drop across the series resistance R_S which leads to the expression for diode current given in Eq. 4.1.

$$I = I_S\left[exp\frac{q(V-IR_S)}{kT} - 1\right] = I_S\left[exp\frac{qV_j}{kT} - 1\right] \quad (4.1)$$

Where I_S is the saturation current, T is the temperature and k is the Boltzmann's constant.

The small signal model of a SBD is presented in Fig 4-3b. The ideal diode, D_1 in Fig. 4-3a is replaced a dynamic resistance, r_d which is modeled by linearizing the SBD I-V characteristics about a given operating point such as 'a' or 'b' in Fig. 4-4. The expression for the dynamic resistance shown in Eq. 4.2 indicates its inverse relationship with the diode current.

$$r_\mathrm{d} = \frac{kT}{q(I+I_S)} \quad (4.2)$$

The capacitance C_j in parallel with r_d is dependent on the Schottky junction voltage and area and is given by the expression in Eq. 4.3

$$C = A\frac{C_{j0}}{\left(1-\frac{V_j}{V_{j0}}\right)^M} \quad (4.3)$$

where C_{j0} is the junction capacitance at zero bias, V_{j0} is the junction built in potential, V_j is the voltage applied to the junction and A is the area of the junction.

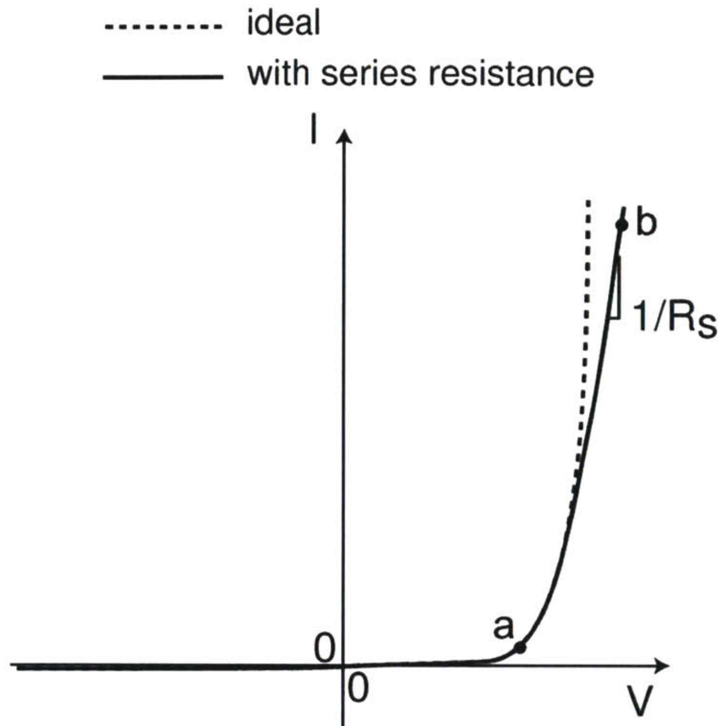


Figure 4-4: I-V characteristics of Schottky diode with and without series resistance, R_S

The model shown in Fig. 4-3 is a small signal model, and accordingly for sufficiently small excitations it can be regarded as a linear, time-invariant model useful for analysis. However, rectification necessarily implies large-signal excitation. Under these circumstances, and for purposes of analysis, it remains helpful to use the model of Fig. 4-3, but to see the parasitic components as time varying instead of time-invariant. It is possible, as we shall show, to get great deal of design insight from such a framework.

4.1.2 Schottky Barrier Diode size selection

In order to investigate the criteria necessary to determine the optimum diode size, a simulation testbench was setup in Cadence SpectreRF using a halfwave rectifier driven by an ideal current source with an ideal 2 V voltage source load as shown in Fig 4-5. The small 100pΩ resistance

was included at the input of the halfwave rectifier so that it can provide a node to be probed in the determination of the input power to the rectifier. Periodic steady state simulations of the test bench in Fig. 4-5 were carried out with two diode sizes which differ in effective area by a factor of 10. The dimension of the smallest diode was close to the minimum dimensions allowed in the IBM CMOS8RF process. Plots of efficiency and input power versus frequency for the smaller diode (henceforth called diode_4μm) are presented in Fig. 4-6 while that for the larger diode (henceforth called diode_20μm) are presented in Fig. 4-7. The efficiency of the halfwave rectifier in Fig. 4-5 is defined as DC power output /RF power input.

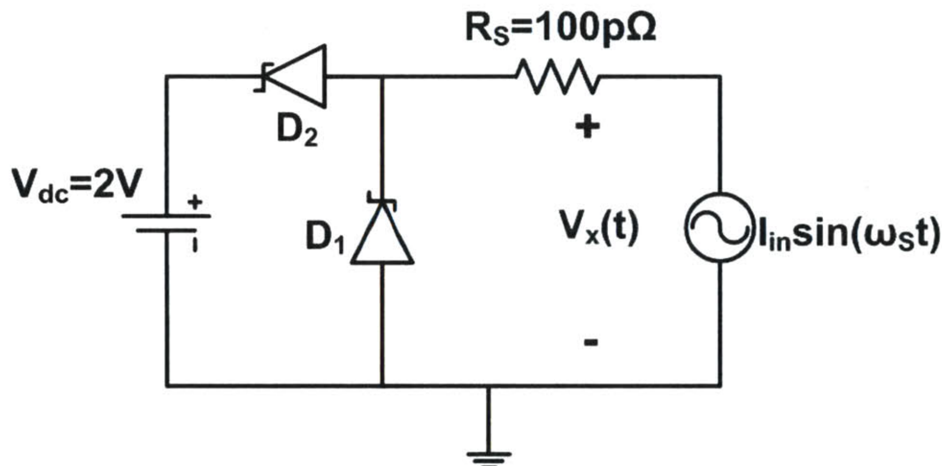
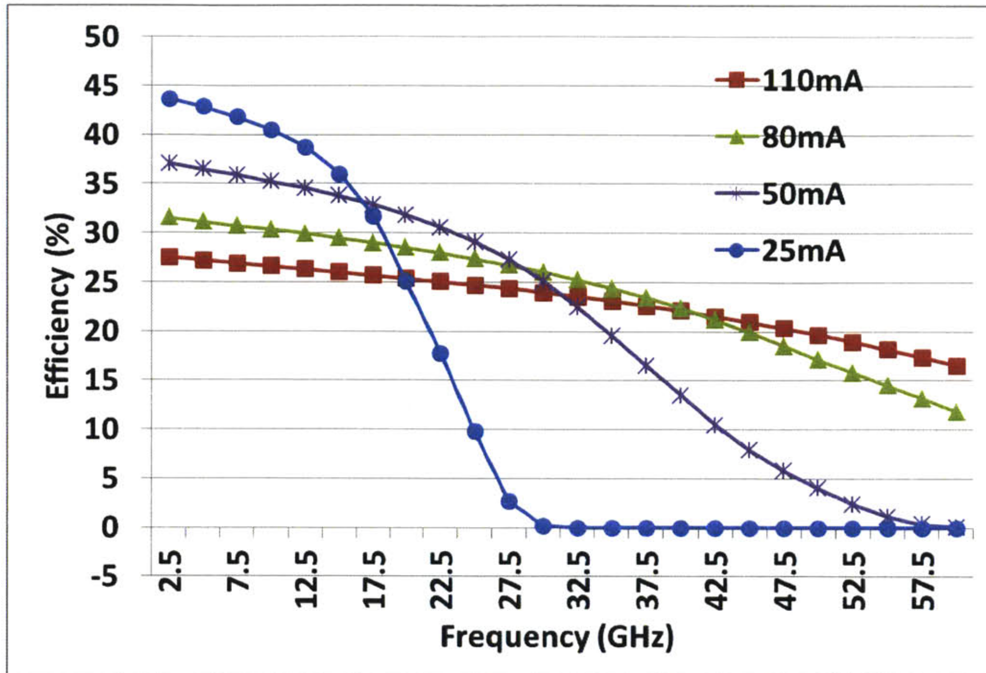


Figure 4-5: Simulation testbench for the halfwave rectifier

The efficiency plots (in both Fig 4-6 and 4-7) are parameterized for a number of input current drives with the maximum current drive selected to be 110 mA for diode_4μm and 320 mA for diode_320μm. These are the input current drives that ensure the maximum allowable current density in the diodes are not exceeded. Looking at Fig. 4-6, it can be seen that the efficiency of the halfwave rectifier decreases as the frequency is swept from 2.5 GHz to 60 GHz. But the high frequency performance of the rectifier can be improved by increasing the input current drive.



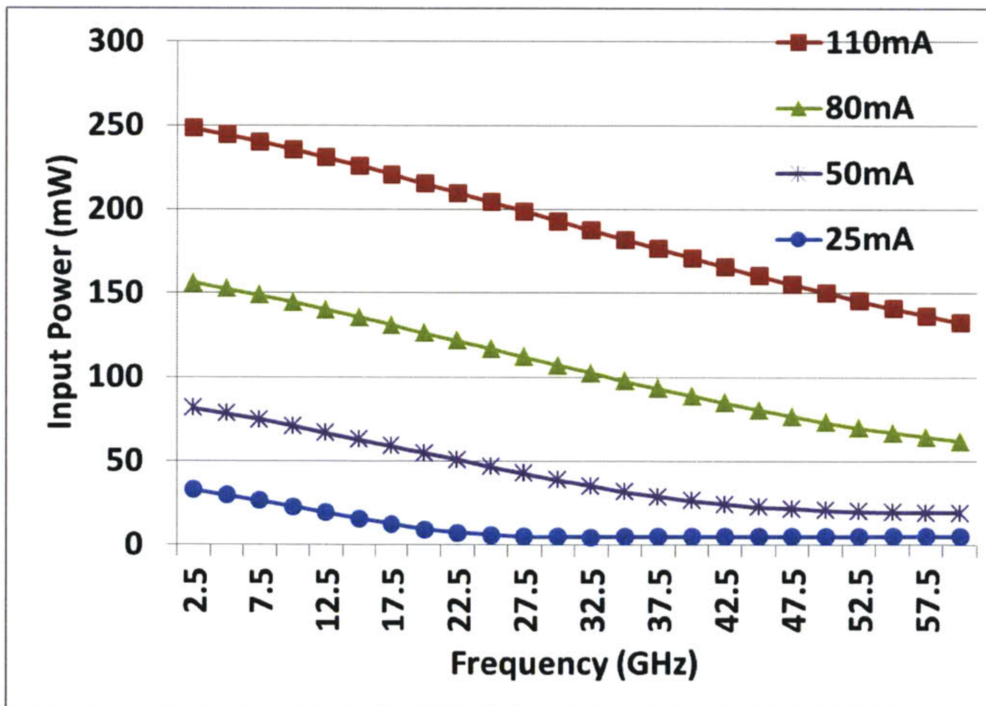
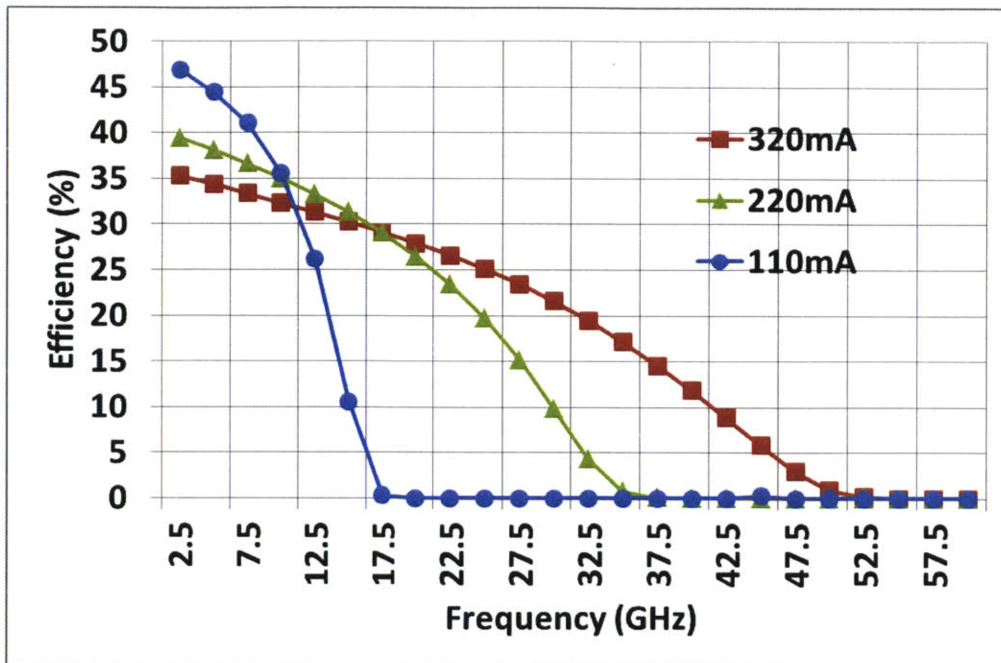


Figure 4-6: Efficiency and input power of halfwave rectifier using SBD with length = 4 μm, width = 5 μm and number of fingers = 2



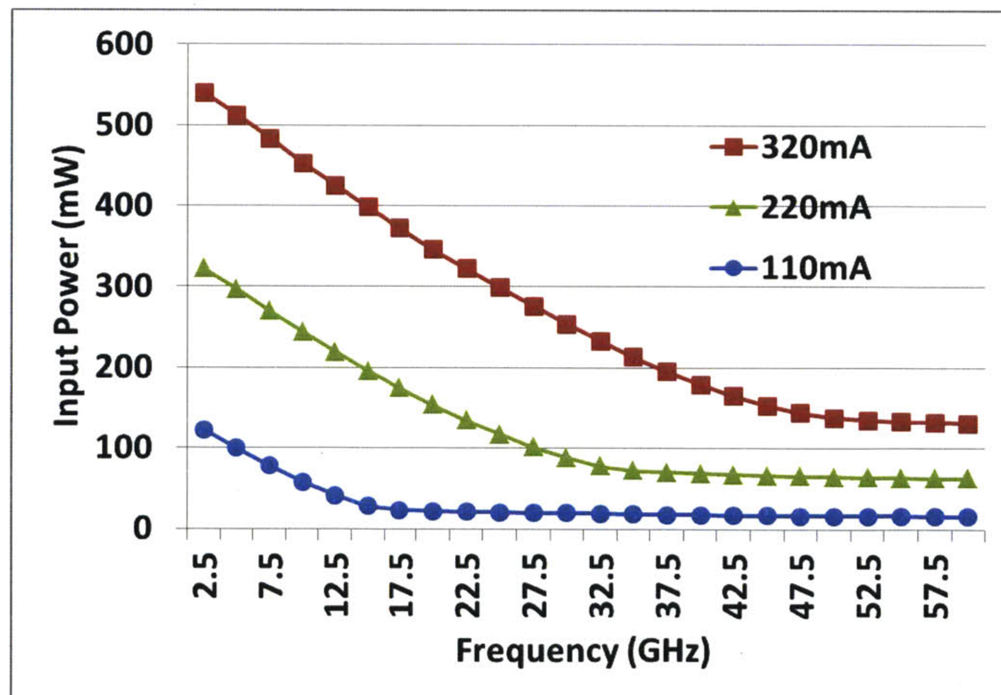


Figure 4-7: Efficiency and input power of halfwave rectifier using SBD with length = 20 μm, width = 5 μm and number of fingers = 4

When the input current drive is increased from 25 mA to 50 mA, the efficiency at 32.5 GHz increases from 0% to 25% while the efficiency at 2.5 GHz decreases from 44% to 37%. This trend is more pronounced as we increase the input current drive up to 110 mA with improved higher frequency operation being traded off with poorer efficiency at lower frequencies. The halfwave rectifier implemented with the larger diodes (diode width = 20μm) exhibits the same efficiency – high frequency operation tradeoff as shown in Fig. 4-7.

Using smaller diodes ensures that the parasitic juncition capacitance is small providing faster operation with good efficiency at high frequencies. The draw-back is lower power handling capabilities. When a diode size is selected so that the maximum expected power from the PA (or input current drive) to the halfwave rectifier is close to the maximum power that can be handled by the diode, the device will spend more time operating in the linear region of its I-V characteristic (such as point 'b' in Fig. 4-4). There will be significant ohmic losses in the diode's series resistance leading to lower efficiency. This fact can be seen in Fig. 4-6 where the efficiency at 2.5 GHz decreases as the input current drive is increased. Conversely, if a large diode size is selected, more power will be required to turn on the device the first place. A larger current is needed to charge the larger junction capacitance to a voltage that brings the diode into the beginning of the exponential region of it's I-V characteristic. If a situation is envisaged in which the input drive current is large enough to turn on the diode such that it is in the exponential region of its I-V curve, higher efficiency can be obtained. Such a scenario can be investigated by comparing the efficiency and input power plots in Fig. 4-6 and 4-7 at 2.5 GHz with a 110 mA input current drive. This approximates the case where the PAs in a hypothetical outphsing system employing an isolationg power combiner has a fixed available output power. For the halfwave rectifier implemented with the 4μm diode, the efficiency at 2.5 GHz is 27.5%

but the output power delivered to the 2 V load is 0.27 * 250 mW (input power at 2.5 GHz). Similarly, for the 20 μm diode, the efficiency is higher at 46.9% and the power delivered to the output load is 0.469 * 122.5 mW. The output power in both cases is comparable. Thus, at the low frequency of 2.5 GHz the larger diode is preferable because it can provide similar levels of output power with higher efficiency.

When higher frequency operation is desired, the halfwave rectifier implemted with the 4u diode significantly outperforms that implemented with the 20 μm diode. This result can be explained by referring to the SBD model discussed in Section 4.1.1 and presented in Fig. 4-3. When current is initially applied to the SBD, all the current is used to charge up the parasitic junction capacitor. As the capacitor charges, its voltage increases until appreciable current can start flowing through the diode, D_1. This siphons some of the current coming from the input current source. The fraction of the current which flows through D_1 depends on the Schottky barrier junction dynamic resistance, r_d at that instant in time. This implies that some part of the current will still continue to flow through the capacitor and increase the voltage across both capacitor and the Schottky junction. As a result of the Schottky diode exponential I-V characteristic, its current will continue to rise rapidly making its effective resistance smaller. D_1 will continue to siphon more of the current from the input current source. Note that we now have a current divider between the Schottky barrier junction diode, D_1 and the junciton capacitor, C_j. The process of positive feedback which increases diode current continues until the sinusoidal waveform of the current from the input source reaches its peak. Then as the current from the current source decreases, the current through the combination of D_1 and C_j decreases as well. This changes the operating point and hence the dynamic resistance of the SBD. The junction

capacitor starts to discharge reducing the voltage across the Schottky junction. The current through the diode decreases exponentially which increases its effective dyanmic resistance.

When a larger diode is used, more power is wasted charging up the parasitic capacitor up to a voltage that will set the SBD at an operating point which can carry appreciable current. Thus, for a given input current at a particular frequency, a smaller diode will provide more rectified output power than a larger one because it turns on faster and its parasitic capacitor can be charged up to a higher voltage so that the diode is at an operating point on it's IV curve that gives larger output current. The larger current for the smaller diode means that it has a smaller dynamic resistance and thus presents a lower impedance path for the input current. It can siphon more current from the parasitic capacitor in parallel leading to more rectified output.

At higher frequencies, the junction capacitor impedance reduces causing it to provide a lower impedance path to the output node when compared to the resistance of the Schottky barrier junction. With a smaller fraction of the input current flowing through the actual Schottky barrier junction, a smaller rectified current will be obtained. This problem is exacerbated for the larger diode which has a larger junction capacitance that creates an even smaller impedance in parallel with the Schottky barrier junction. This leads to a significant decrease in efficiency because the signal which should have been rectified is simply passed to the output through the junction capacitance and filtered. Thus, large diodes perform poorly at higher frequencies. The problem can only be mitigated by using larger input current or power source. The larger current ensures that the parasitic capacitor will charge up to a larger voltage during the positive half of the input signal cycle. The larger voltage across the SBD leads to a larger current through the Schottky junction thus reducing its effective dynamic resistance r_d (see Eq. 4.2) so that it can siphon more of the input current from the junction capacitor, C_j. As a result, more power is routed through the

Schottky barrier junction leading to the rectification of a larger precentage of the input signal and improved efficiency. Note that this analysis depends on the approximation proposed in section 4.1.1. in which to first order, the large signal variation in dynamic resistance of the SBD can be approximated by a series of small signal dynamic resistances whose values change in time during each instant in the input signal period.

A few conclusions can be made from the preceding disucssion. When energy recovery is to be implemented at relatively lower frequencies employing a large diode size is preferable. The input power must be large enough to turn on the diode strongly enough so that it operates within the exponential region of the I-V characteristic. The linear region of the I-V characteristic with its resultant ohmic losses in the series resistance must be avoided. For higher frequency operation, smaller diodes are preferable because a larger percentage of the input signal is routed through the Schottky barrier junction since the smaller junction capacitance siphons a smaller fraction of the input current. A method of implementing this diode size section optimization in simulation is to setup the outphasing PA system using simplified models of the individual switching PA. The rectifier is now connected to the difference port of the outphasing PA's power combiner. A series of PSS simulations in which the diodes size is swept is performed so that a plot of rectifier efficiency vs diodes size at the given operating frequency can be plotted. An optimum point which gives the highest efficiency for sufficient rectified output power can be determined.

In order for energy recovery to be worthwhile, the efficiency of the energy recovery network which includes the rectifier should be high. The efficiency plots in Fig. 4-6 and Fig. 4-7 indicate low efficiency of the halfwave rectifier at frequencies > 10 GHz regardless of diode size. Energy recovery at millimieter wave frequencies is therefore not feasible using Scottky barrier diodes in

the IBM CMOS8RF process. Thus, the rest of this chapter will discuss the design of an energy recovery network operating at a lower frequency of 2.14 GHz.

4.2 Resonant rectifier design

The major impediment to efficient rectification at multi-gigahertz frequencies is diode parasitic capacitance. Godoy et al. [22] analyzed the effect of parasitic diode capacitance on the input impedance of a half wave rectifier. First we consider the input impedance of the halfwave rectifier without parasitic capacitance which from [22] is given by:

$$R_{\text{rect}} = \frac{k_{\text{rect}} V_{\text{dc}}}{2 P_{\text{in}}} \tag{4.4}$$

where k_{rect} is a constant determined from simulation, P_{in} is the input power to the rectifier and V_{dc} is the voltage at the output of the rectifier. When diode parasitic capacitance is included in the analysis (see Fig. 4-8), the fundamental component of the voltage is no longer in phase with the current leading to an input impedance that is no longer purely resistive. This leads to poor isolation between the PAs of an outphasing system if the half wave rectifier is connected to the power combiner's isolation port.

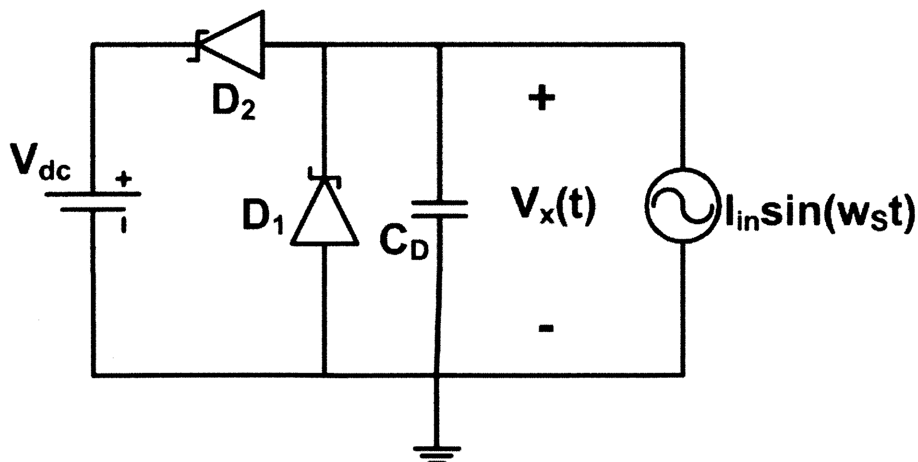


Figure 4-8: Halfwave rectifier with parasitic diode capacitance

The analysis in [22] shows that the diode D_2 turns on at time $u = \omega_s t$ which is computed in radians by the equation,

$$\cos(u) = 1 - \frac{\omega_s C_D V_{dc}}{I_{in}} = 1 - \frac{V_{dc}}{X_C I_{in}} \tag{4.5}$$

where ω_s is the frequency of the input current source, X_C is the reactance of C_D at ω_s. Furthermore, the rectifier impedance, Z_{rect} is given by,

$$|Z_{rect}| = \frac{1}{I_{in}}\sqrt{a_{x1}^2 + b_{x1}^2} \tag{4.6}$$

$$\angle(Z_{rect}) = -\tan^{-1}\frac{b_{x1}^2}{a_{x1}^2} - \frac{\pi}{2} \tag{4.7}$$

where,

$$a_{x1} = \frac{2}{\pi}V_{dc}\left[-\frac{u}{2\alpha} + \left(\frac{1}{\alpha} - 1\right)\sin(u) - \frac{1}{4\alpha}\sin(2u)\right] \tag{4.8}$$

$$b_{x1} = \frac{2}{\pi}V_{dc}\left[\frac{3}{4\alpha} + \left(1 - \frac{1}{\alpha}\right)\cos(u) + \frac{1}{4\alpha}\cos(2u)\right] \tag{4.9}$$

with $\alpha = V_{dc}/X_C I_{in}$ and a_{x1} and b_{x1} representing the real and imaginary components of the Fourier transform of the half wave rectifier input voltage at the fundamental frequency, V_{x1} (see Figure 4-8). The parameter, α, is similar to the "reactance factor" defined for low frequency rectifiers [25]. When α is substituted into Eq. 4.5, we see that the diode stops conducting when $\alpha > 2$ and the rectifier impedance is purely capacitive. Thus, it can be concluded that a small value of α is necessary to keep the half wave rectifier input impedance mostly resistive. Examining the expression for α, we see that its value can be minimized by minimizing the rectifier output voltage, V_{dc}, the operating frequency, ω_s, and the diode parasitic capacitance, C_D and by increasing the input current I_D. Three of the parameters, I_D, ω_s and V_{dc} are typically fixed by the desired application. For instance, use of the halfwave rectifier at multi-gigahertz frequencies ensures that ω_s will be large thus increasing the value of α.

One way to mitigate the effect of diode capacitance is the use of resonant rectifiers [22], [23], [24], [25], [26]. The diode D_1 in Fig. 4-8 is replaced by an inductor which cuts the total parasitic diode capacitance by a factor of 0.5. In addition, the inductor resonates out the parasitic capacitance associated with diode D_2 (making the rectifier impedance resistive) and provides a DC path to ground. Another issue to consider is sizing of the diodes to improve their power handing capacity. Larger diodes can handle more power but have larger parasitic capacitances which will require even smaller inductors to tune out. Excessively large diodes will result in the need for inductors whose small values are difficult to fabricate on chip or realize with high-Q discrete components.

4.3 Resistance Compression Network

The energy recycling scheme shown in Fig. 4-1 exhibits the drawback of poor PA isolation because of excessive variation in the input impedance of the rectifiers with input power. This problem can be ameliorated by the introduction of a resistance compression network (RCN) between the rectifier and the isolation port of the power combiner (see Fig. 4-9 and [22]). A RCN can be combined with a pair of resonant rectifiers to form an RF to DC converter which exhibits a relatively narrow range of impedance variation in response to the variation of the rectifiers' impedance [23]. The resistance compression network (RCN) consists of a pair of complex conjugate matched impedances in series with a pair of matched resistances, R_L as shown in Fig. 4-10. The matched resistances can be used to model the input resistance of resonant rectifiers which vary with input power according to Eq. 4.4.

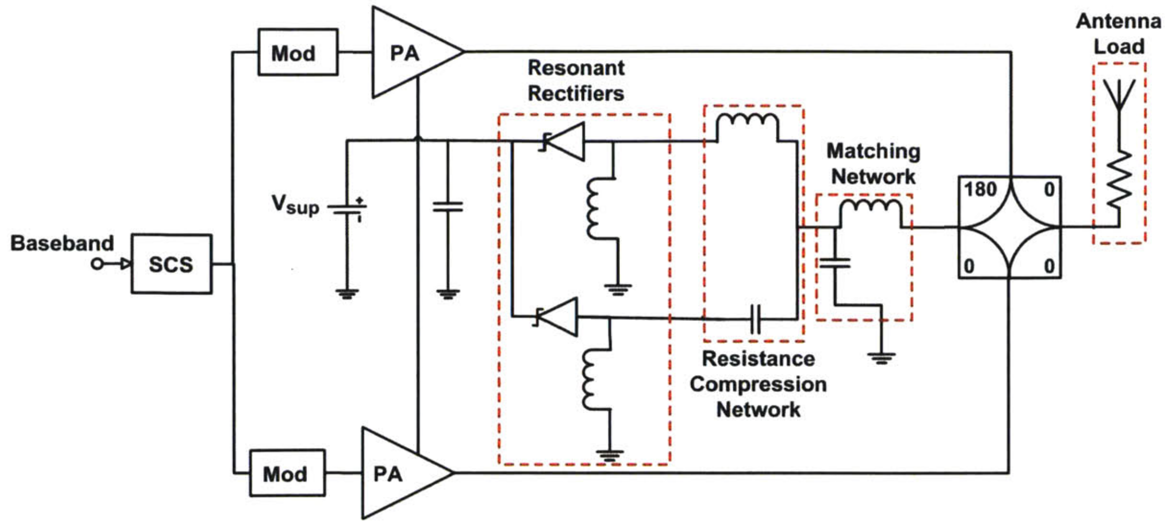


Figure 4-9: Outphasing power amplifier with resistance compression network in energy recovery network.

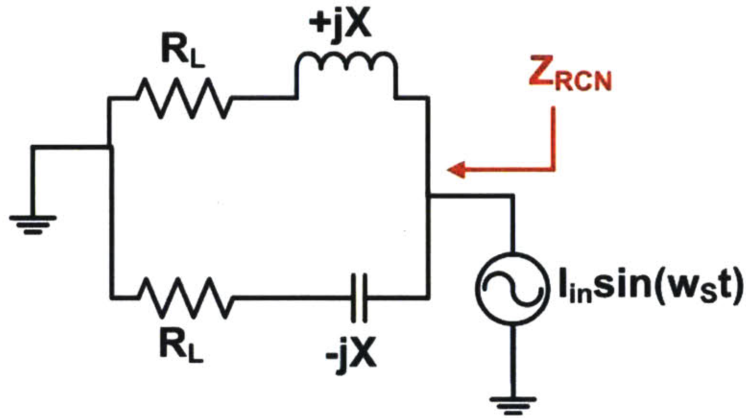


Figure 4-10. Resistance compression network with matched load resistances.

The RCN consists of two complex conjugate reactances $+/-jX$ whose magnitude at the operating frequency is set to be the geometric mean of the minimum and maximum values of the matched resistances, R_{L}. This means that $R_{\mathrm{rect}} \in \left[X/\sqrt{c_{\mathrm{rect},}}\ X\sqrt{c_{\mathrm{rect}}}\,\right]$ where c_{rect} is the ratio of the maximum to minimum resistance in the R_{rect} range. As shown in [22], the resistance R_{RCN} of the RCN is calculated to be,

$$R_{\mathrm{RCN}} = \frac{X^2}{2R_{\mathrm{rect}}}\left[1 + \left(\frac{R_{\mathrm{rect}}}{X}\right)^2\right] \tag{4.10}$$

where R_{rect} is the impedance of the rectifier. Thus the RCN provides compression of the rectifier resistance, R_{rect}, about the value of reactance, X. The compressed range of R_{RCN} can be shown to be [22]

$$c_{\mathrm{RCN}} = \frac{1+c_{\mathrm{rect}}}{2\sqrt{c_{\mathrm{rect}}}} \tag{4.11}$$

Fig. 4-11 shows a plot of the RCN resistance, R_{RCN} against the corresponding rectifier resistance, R_{rect}. We can see that a 10:1 variation in rectifier resistance (from 2Ω to 20Ω) results in a modest 1.74:1 change in R_{RCN}. This reduction in rectifier resistance variation at the isolation or difference port of the power combiner will result in better isolation and the maintenance of higher efficiency in the switching PAs.

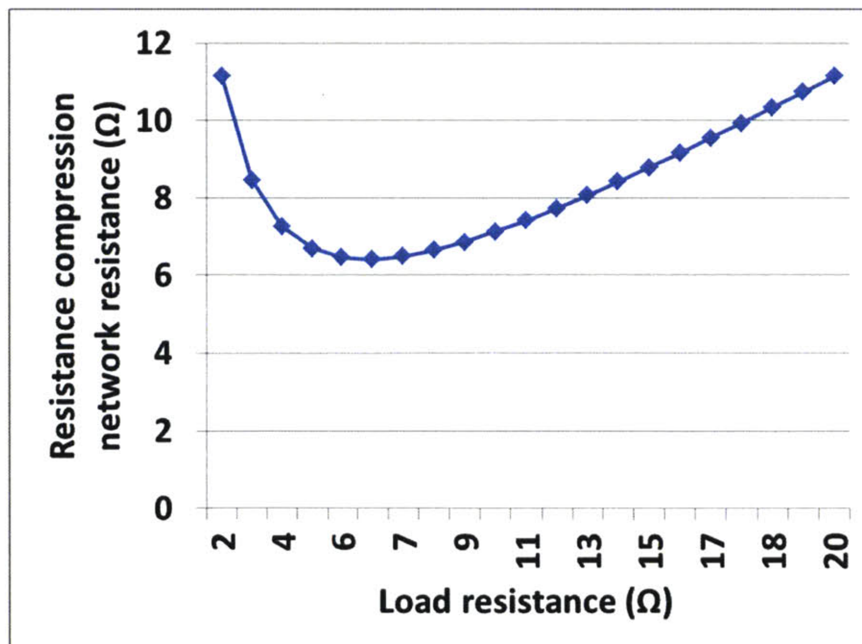


Figure 4-11: Variation of the resistance of a resistance compression network with 10:1 change in matched load resistance.

4.4 Theoretical Efficiency of Outphasing PA employing energy recovery

The energy recovery network which is shown in Fig. 4-9 is composed of a matching network, a resistance compression network and a pair of resonant rectifiers. The signal at the difference port of the power combiner is rectified by the energy recovery network with the DC energy fed back into the power supply. The efficiency of the outphasing PA is given by the expression derived in [22]

$$\eta_{\text{total}} = \frac{P_{\text{out}}}{P_{\text{dc}} - P_{\text{rec}}} \tag{4.12}$$

where P_{out} is the total output power of the outphasing PA, P_{dc} is the power drawn from the supply by the individual PAs and P_{rec} is the dc power obtained from the energy recovery network by means of rectifying the signal at the difference port of the power combiner. The total power available at the output of the outphasing PA is given by

$$P_{\text{avail}} = \eta_{\text{PA}} \eta_{\text{comb}} P_{\text{dc}} \tag{4.13}$$

where η_{PA} is the PA efficiency and η_{comb} is the power combiner efficiency. The rectified power which is fed back to the power supply, P_{rec} is given by

$$P_{\text{rec}} = \eta_{\text{rec}}(P_{\text{avail}} - P_{\text{out}}) = \eta_{\text{rec}}(\eta_{\text{PA}} \eta_{\text{comb}} P_{\text{dc}} - P_{\text{out}}) \tag{4.14}$$

where η_{rec} is the efficiency of the energy recovery network. Substituting Eq. 4.14 back into Eq. 4.12, the expression for the efficiency of the outphasing PA with energy recovery is given by

$$\eta_{\text{total}} = \frac{P_{\text{out}}}{P_{\text{dc}} - \eta_{\text{rec}}(\eta_{\text{PA}} \eta_{\text{comb}} P_{\text{dc}} - P_{\text{out}})} = \frac{p}{\frac{1}{\eta_{\text{PA}} \eta_{\text{comb}}} - \eta_{\text{rec}}(1-p)} \tag{4.15}$$

where $p = P_{\text{out}}/P_{\text{avail}}$ is the normalized output power. Fig 4-12 presents a plot of η_{total} versus output power backoff = $dB(p)$ for an outphasing PA using practical values of $\eta_{\text{PA}} = 70\%$, $\eta_{\text{comb}} = 0.95$ and a few values of energy recovery network (ERN) efficiency, η_{rec}

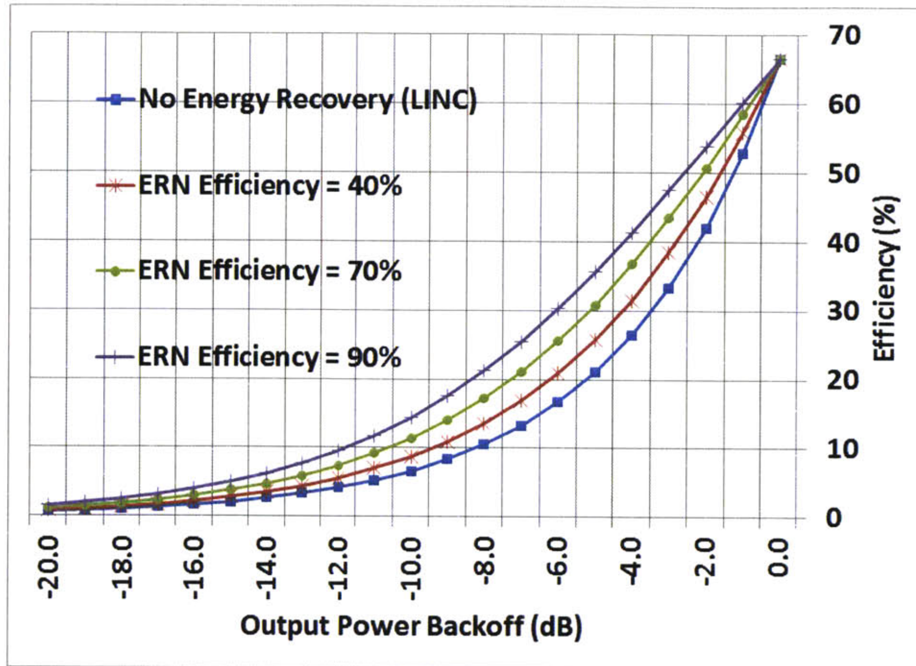


Figure 4-12: Variation of the outphasing PA efficiency with energy recovery network efficiency.

The outphasing PA efficiency shows a strong dependence on the energy recovery network efficiency. At 6 dB backoff, the outphasing PA efficiency increases from 16.7% for the LINC implementation to 30.2% with an ERN efficiency = 90%. The plots in Fig. 4-12 leads to the conclusion that an ERN efficiency which is greater than 40% is required for the use of an energy recovery network to be worthwhile.

4.5 Summary

In this chapter, the theory of employing an energy recovery network to increase the efficiency of an outphasing power amplifier was discussed. The tradeoffs which need to be addressed in the Schottky diode size selection for the halfwave or resonant rectifier was investigated. The design of a resonant rectifier for use in RF – DC conversion in the energy recovery network was also discussed.

Chapter 5

Practical System Implementation and Measurement of the Energy Recovery Network

In this chapter, an energy recovery network (ERN) operating at 2.5 GHz was designed employing some of the theory developed in chapter 4. Simulation results will be analyzed to determine the feasibility of energy recovery utilizing resistance compression networks at multi-gigahertz frequencies. A prototype of the energy recovery network which operates at a frequency of 2.14 GHz will be implemented and measurement results discussed.

5.1 Energy Recovery Network Design

The first step in the process is the selection of the Schottky diode size required for the resonant rectifier. The goal of this implementation is to evaluate the feasibility of resistance compression in an energy recovery network (ERN) operating at 2.5 GHz. Thus, a specific output power target for the ERN was not required. Fig. 4-12 indicated that the ERN needs to have an efficiency greater than 40% for energy recovery to be worthwhile. The strategy employed to satisfy this condition was to first select a relatively large diode size for the rectifier. The dimensions used were: diode length = 25μm, diode width = 5μm, and number of fingers = 4. Employing the more rigorous diode size selection process described in chapter 4 could be the subject of future work.

But for the requirements of this stage of the project, selecting a relatively large diode was sufficient. The use of a large size gives the assurance that appreciable rectified output power can be obtained while the diodes still operate within the exponential region of their I-V characteristics as discussed in section 4.1.2. A resonant rectifier topology (see Fig. 5-1) was used instead of the halfwave rectifier because the use of a single diode reduces the net capacitance of the rectifier by a factor of 0.5. The inductor which replaces one of the diodes in the halfwave rectifier has a value that is chosen so that it resonates with the diode junction capacitance at the frequency of operation. This makes the input impedance of the resonant rectifier to be dominated by its real component. The resonant rectifier can be designed via periodic steady state (PSS) and transient simulations in which the inductance value is swept until the voltage and current waveforms at the resonant rectifier's input are in phase.

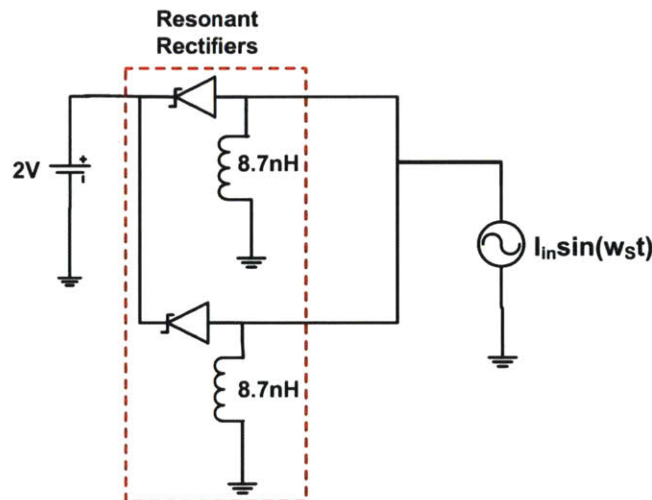
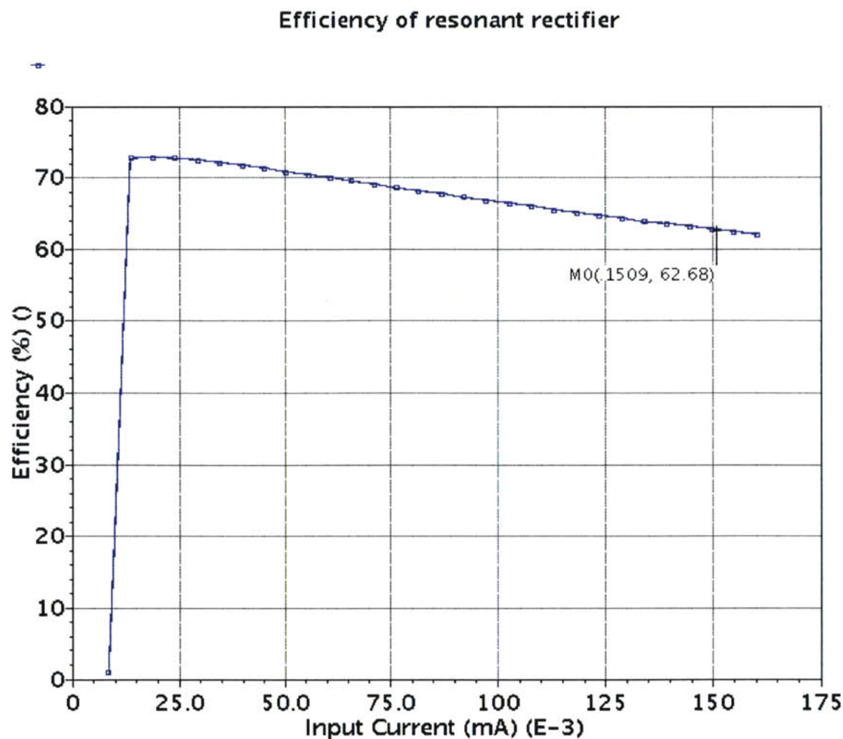


Figure 5-1: Testbench to determine input current drive and resistance of the resonant rectifiers.

The next step was selecting the input power that will ensure the resonant rectifier's efficiency is greater than 50%. This step was carried out using periodic steady state and transient simulations of the schematic in Fig. 5-1. The input current drive was swept to obtain the current range that keeps the efficiency greater than 60% and rectified output power greater 200 mW for a

360 mW input power. These numbers were chosen as reasonable output power levels for PA used in cellular and other wireless communication applications. With these power levels, the diodes operate mostly in the exponential region of their I-V characteristics as exemplified by the good efficiency performance of the resonant rectifier. Considering the outphasing PA depicted in Fig. 4-1, the maximum power of 360 mW will be delivered to the resonant rectifiers at the maximum outphasing angle of 180°. In addition, the testbench of Fig 5-1 was used to determine the range of input resistance of the resonant rectifier as the input power is varied from 10 mW up to the 360 mW. The results of the simulation are presented in Fig. 5-2.

Fig. 5-3 presents the classic inverse relationship between the resonant rectifier input resistance and the power (input current drive). The range of input resistance to be compressed is from 71 Ω to 483 Ω which corresponds to a 10:1 variation in input current drive. Employing the discussion in section 4.3, the reactance of the conjugate matched passive components in the resistance compression network is set to the geometric mean of this resistance range.



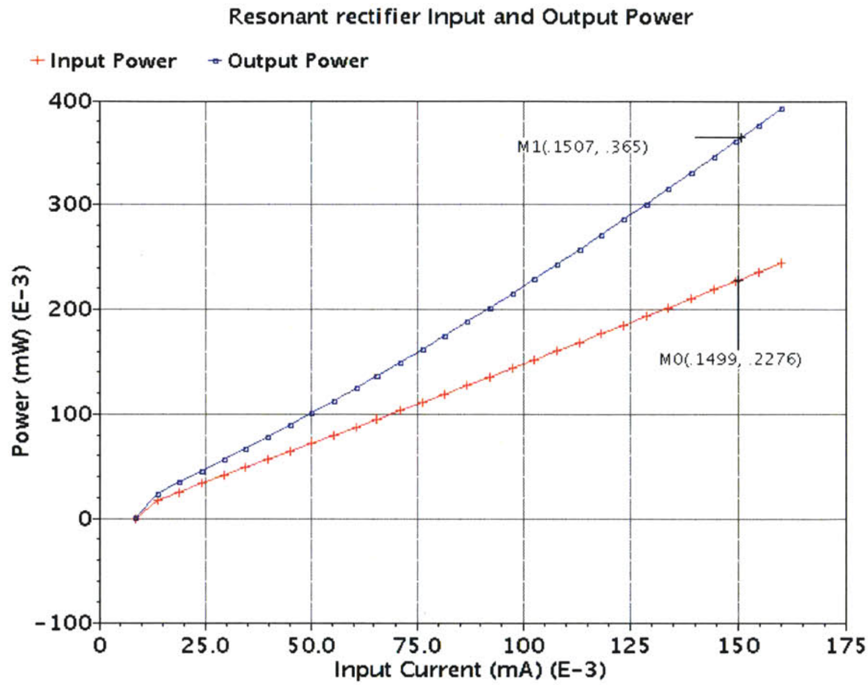


Figure 5-2: Efficiency and Input and Output power of resonant rectifier testbench in Fig. 5-1.

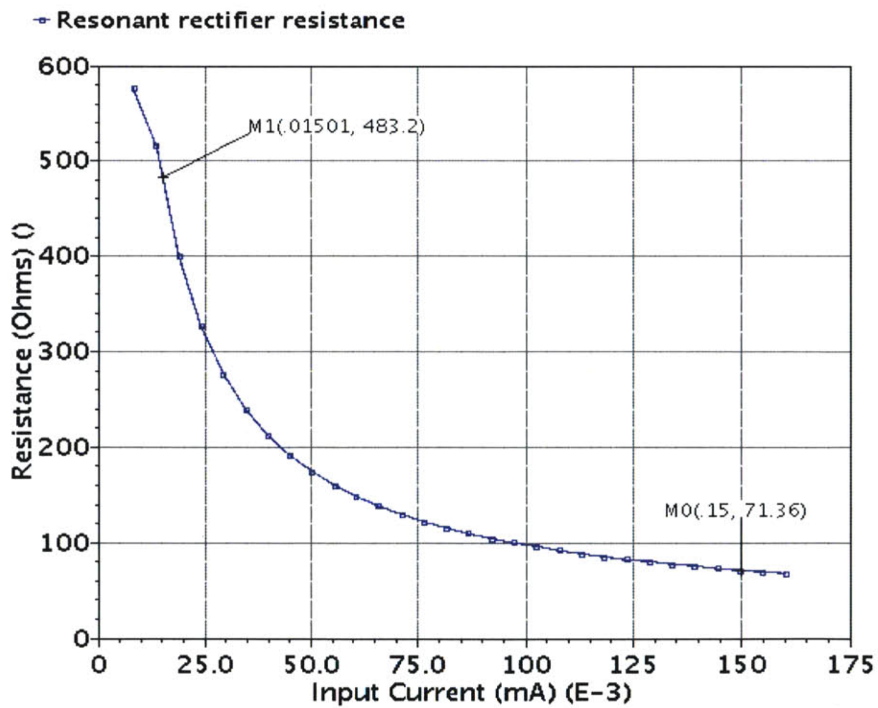


Figure 5-3: Resonant rectifier input resistance from testbench in Fig. 5-1.

Thus, the inductor and capacitor of the resistance compression network should have an impedance of 185 Ω at 2.5 GHz.

The resistance compression network along with the resonant rectifiers form the energy recovery network which is now included in the outphasing PA model presented in Fig. 5-4. The PAs are modeled as ideal current sources with the output of the outphasing PA driving a 50 Ω load. A 7.4Ω resistor was put across the 2 V supply to mimic the steady current draw by the PA from the supply. In practice, the energy recovery network "returns power to the supply" by reducing the current draw by the PA from the supply. Some of the bias current required by the PA for operation is provided by the energy recovery network. Thus, the current which the supply needs to provide is reduced and a net increase in overall system efficiency is achieved. A lumped element implementation of a Wilkinson combiner shown in Fig. 5-5 was used to combine the signals from the two ideal current sources. Note that the isolation resistor of 100 Ω which is required for the Wilkinson combiner is replaced by the energy recovery network.

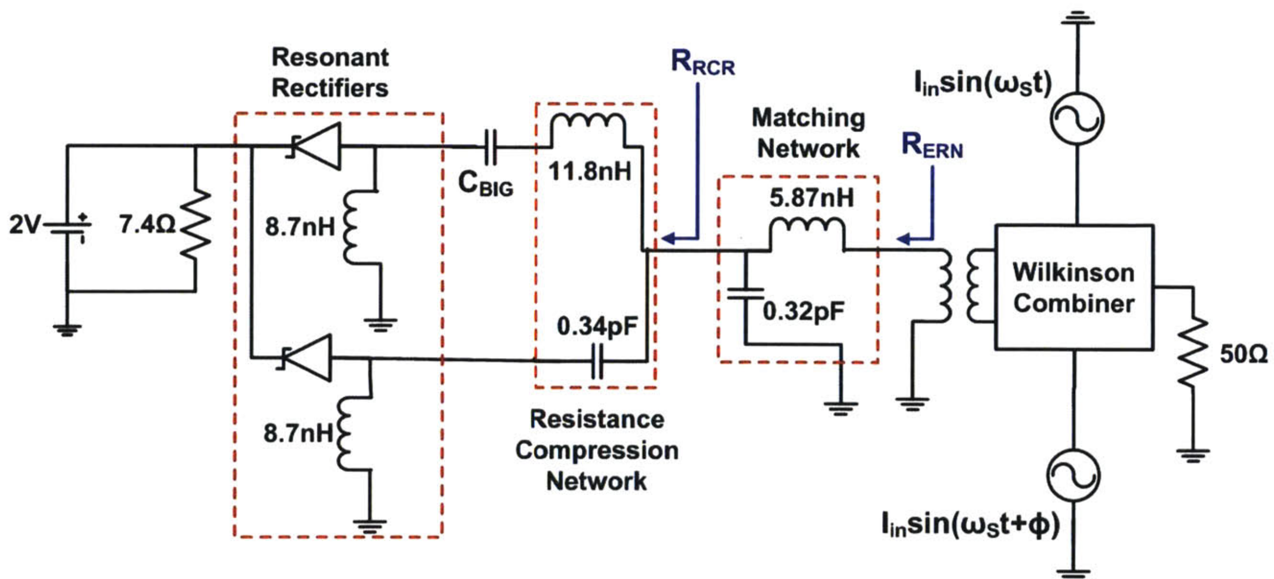


Figure 5-4: Testbench for outphasing system with resistance compressed energy recovery network.

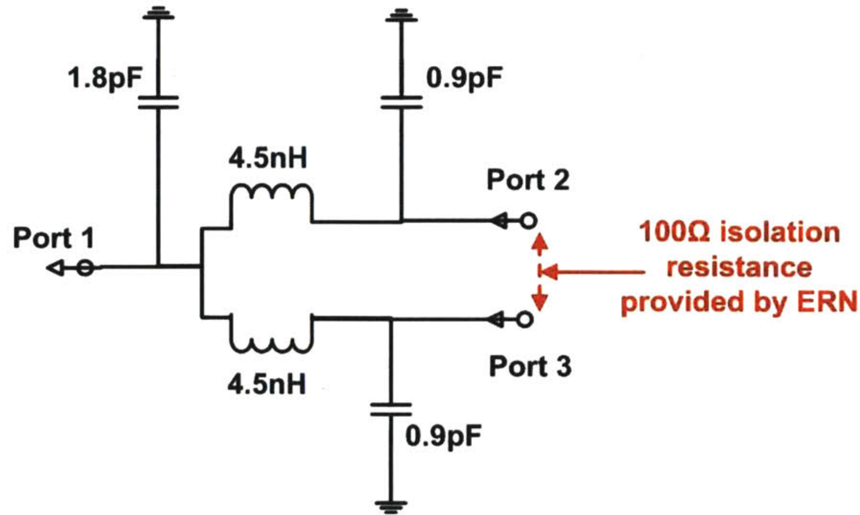


Figure 5-5: Lumped element Wilkinson power combiner designed for 2.5 GHz.

A matching network is placed between the energy recovery network and the Wilkinson combiner so that the compressed resonant rectifier impedance (R_{RCR} in Fig. 5-4) can be transformed to a value close to 100 Ω

The current drive of the ideal current sources (which serve as simple PA models) is selected so that the same maximum input power of 360 mW as determined in Fig. 5-2 is delivered to the energy recovery network when the outphasing angle is 180°. This ensures that the resonant rectifier will have a similar input resistance range to that shown in Fig. 5-3 and the resistance compression network will function properly. Fig. 5-6 shows that the variation in resonant rectifier resistance is compressed when combined with a resistance compression network. The compressed resistance is designed by R_{RCR}. The ratio of maximum to minimum resistance of the resistance compressed rectifier is 1.65 which is significantly less than the original ratio of 6.8. Using Eq. 4.11 with $c_{\text{rect}} = 6.8$, the theoretical range of compressed rectifier resistance, $c_{\text{RCN}} = 1.5$ which is close to the simulation results. The resultant smaller variation in the effective resistance of the entire energy recovery network (designated by R_{ERN} in Fig. 5-4) will lead to

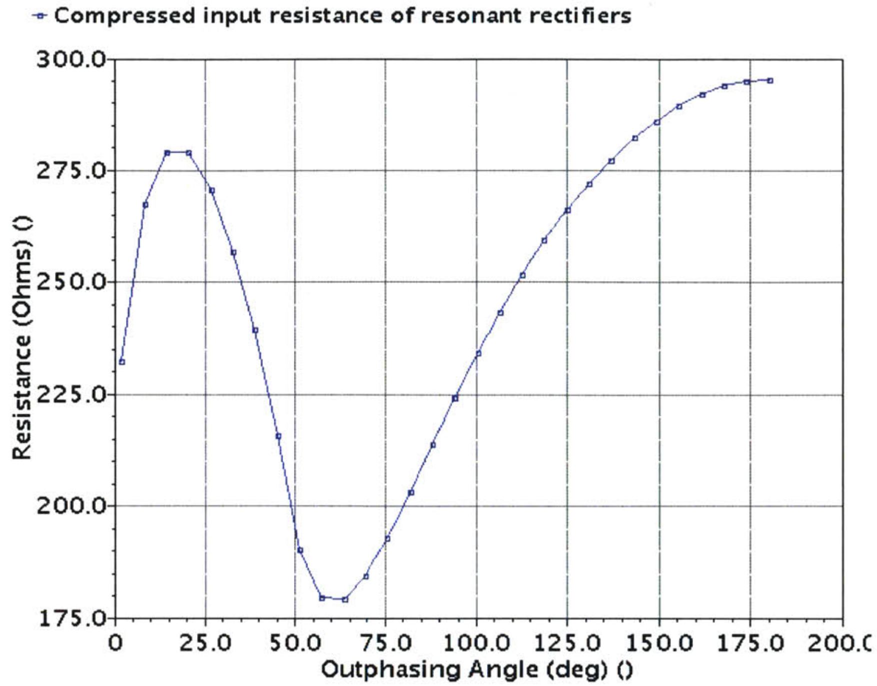


Figure 5-6: Compressed resistance of the resistance compressed rectifier (i.e. resonant rectifier combined with a resistance compression network)

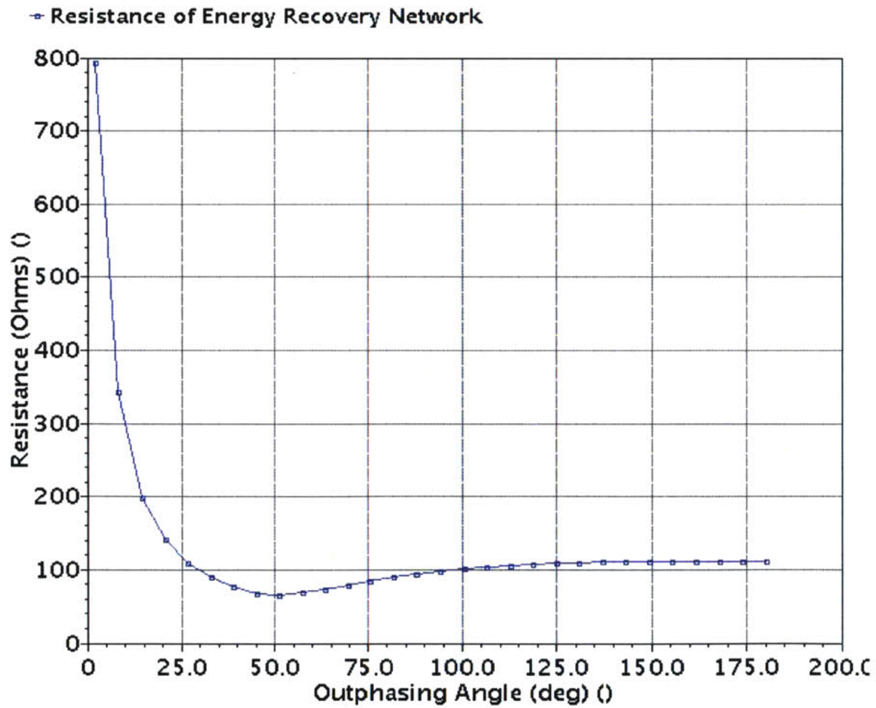


Figure 5-7: Resistance of the entire energy recovery network (including the matching network)

better isolation between the PAs. A plot of R_{ERN} versus outphasing angle is presented in Fig. 5-7. It should be noted that R_{ERN} becomes large and R_{RCR} exhibits a steep drop off for outphasing angles less than 15°. This fact does not lead to any significant degradation in performance because the diodes are either turned off or weakly turned on. Most of the PA's output power is being delivered to the load anyway making PA isolation less critical. Moreover there is very little power to be rectified making energy recovery unnecessary for small outphasing angles.

Fig. 5-8 depicts the efficiency of the energy recovery network. It can be seen that the efficiency is greater than 70% for outphasing angles between 20° and 80°. This is because the input power to the resonant rectifiers is small enough that the Schottky barrier diodes (SBD) are operating well within the exponential region of their I-V characteristics. The ERN efficiency remains above 65% until an outphasing angle of 130° before it drops to about 62% for an outphasing angle of 180°.

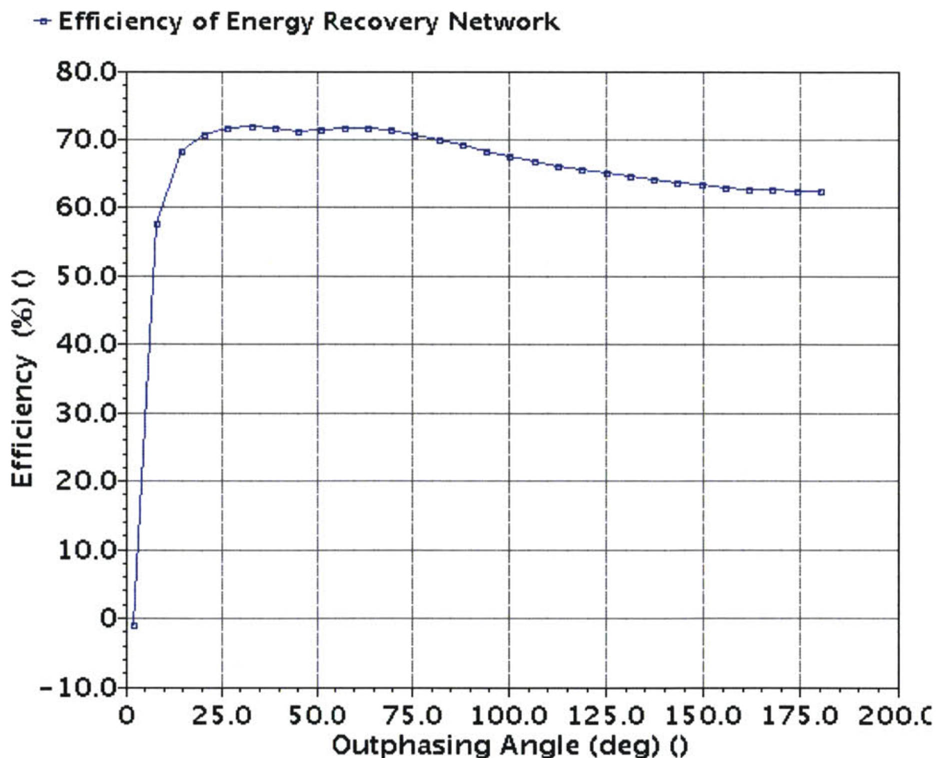


Figure 5-8: Efficiency of energy recovery network

At this point the SBDs have begun to enter the linear region of their I-V characteristics hence the lower efficiency. As discussed in chapter 4, the diodes can handle more power and cover a larger range of resistance values but at the expense of larger ohmic losses. The following equations were used to compute the quantities plotted in Fig. 5-9, Fig. 5-10 and Fig. 5-11 from simulation results.

$$\text{Total System Efficiency} = \frac{\text{Output Power}}{\text{Net Input Power}} = \frac{P_{out}(wilkinson\ combiner)}{P_{out}(PA) - P_{out}(ERN)} \quad (5.1)$$

$$\text{Normalized Recovered Power} = \frac{P_{out}(ERN)}{P_{out}(PA)} \quad (5.2)$$

$$\text{Normalized Total Available Power} = \frac{P_{out}(wilkinson\ combiner) + P_{out}(ERN)}{P_{out}(PA)} \quad (5.3)$$

Fig. 5-9a presents the efficiency of the outphasing system. It can be seen that the use of energy recovery significantly increases the efficiency of the outphasing PA. The efficiency enhancement is most dramatic between outphasing angles of 50° and 130°. This is because the efficiency of the energy recovery network is highest within this range of outphasing angles as can be seen in Fig. 5-8. The plot in Fig. 5.9a indicates that the system has a maximum efficiency of 100% at a 0° outphasing angle because the PAs were modeled with ideal current sources. The efficiency enhancement introduced by energy recovery as shown in Fig. 5.9a and Fig 5.9b is somewhat exaggerated because of the unrealistic value of PA efficiency. Cellular and Wi-Fi applications have power amplifiers with efficiencies typically less than 70%. Using a PA with 70% efficiency will show more modest but significant improvements in efficiency as seen in Fig. 4-12. It is useful to plot the outphasing system efficiency versus output power backoff. Typical cellular modulation schemes have PAPR = 6.5 dB making improvement in PA efficiency at these power back off levels important. Fig 5-9b shows that the efficiency increases from 22% to 45%

when energy recovery is introduced into the standard LINC architecture. This is a significant result in favor of employing energy recovery at frequencies greater than 2 GHz.

Fig. 5-10 presents the power recovered by the energy recovery network normalized by the total available power from the PAs. The plot indicates that at the maximum outphasing angle of 180°, 62% of the power delivered to the energy recovery network can be returned to the power supply. This is very significant because in a standard outphasing PA architecture such as LINC, all this power would be lost or dissipated in the isolation resistor of the Wilkinson or similar isolating combiner. This power loss is one of the major reasons the LINC architecture is very inefficient at large outphasing angles or output power back offs.

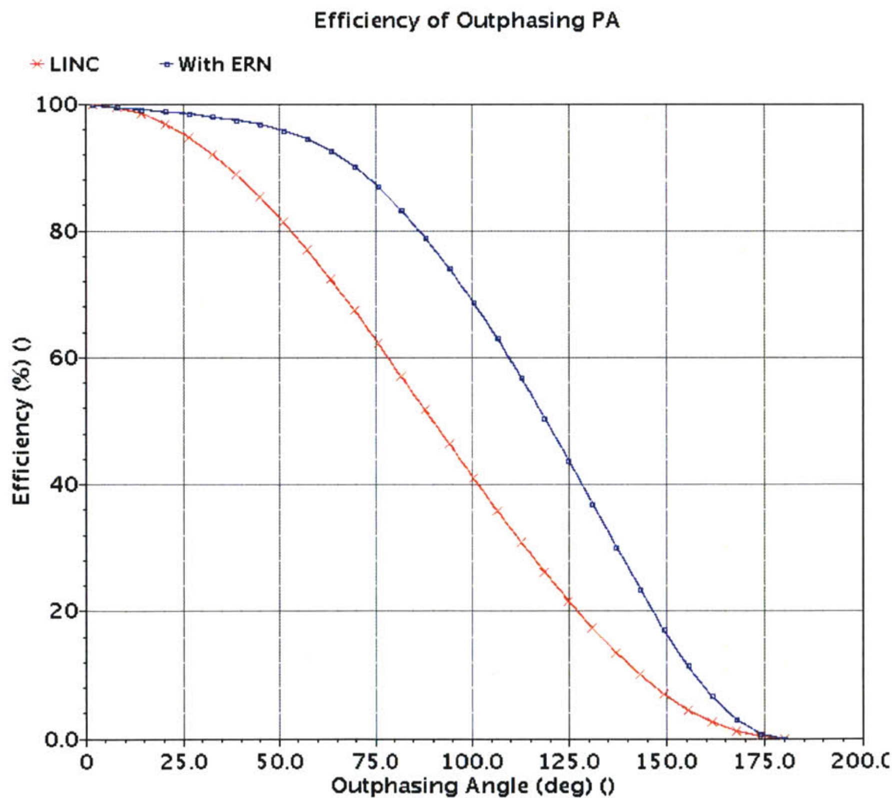


Figure 5-9a: Total outphasing system efficiency vs. outphasing angle for two systems one of which employs a resistance compressed ERN. PAs modeled as ideal current sources

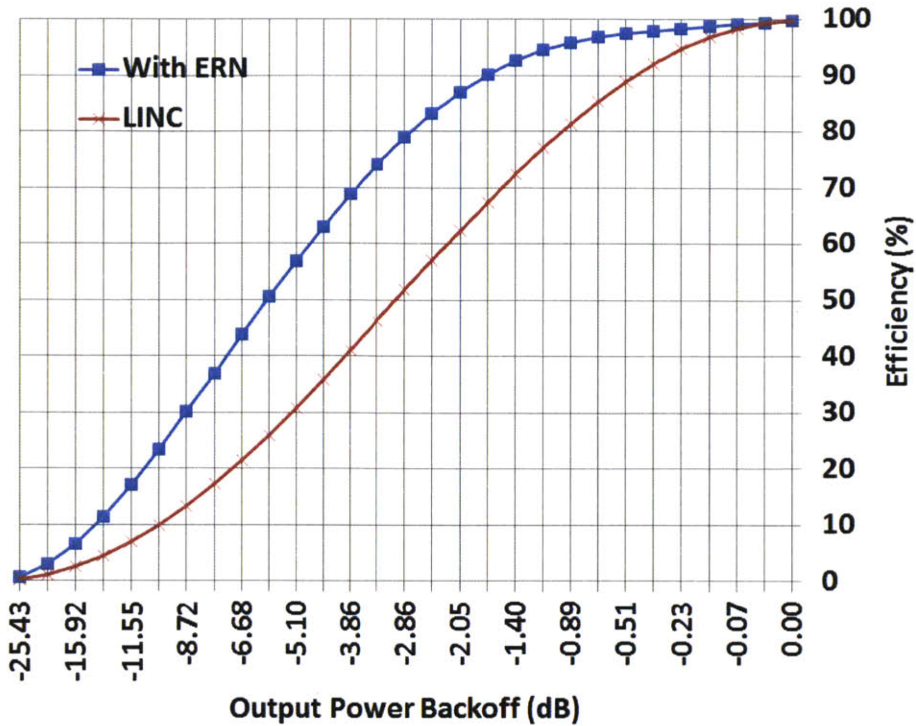


Figure 5-9b: Total outphasing system efficiency vs. output power back off for two systems one of which employs a resistance compressed ERN.

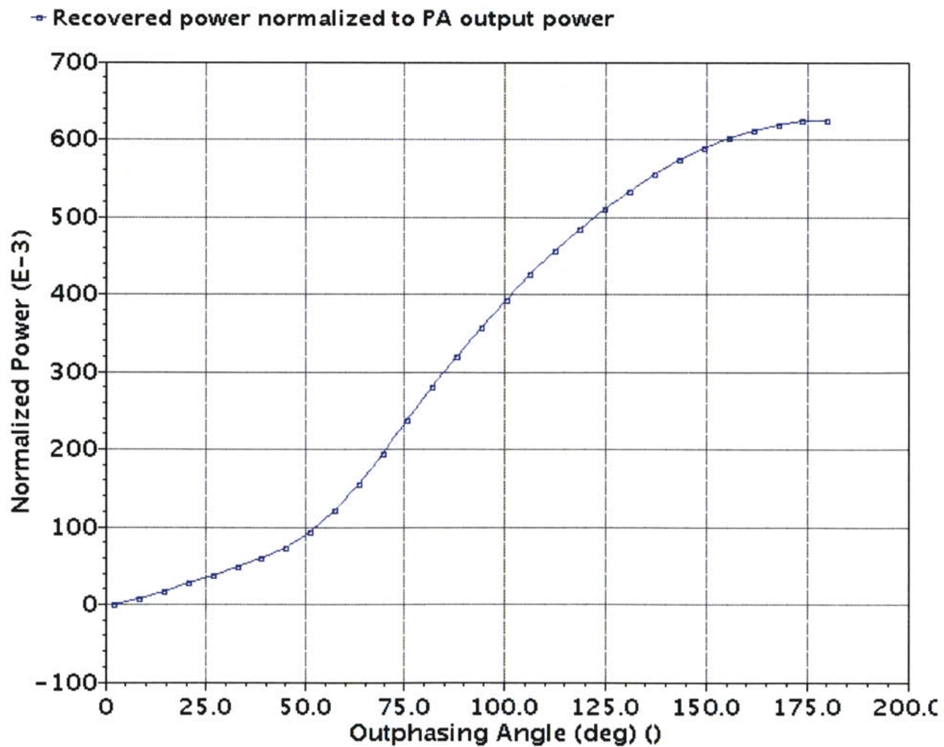


Figure 5-10: Recovered power normalized to available power from the individual PAs.

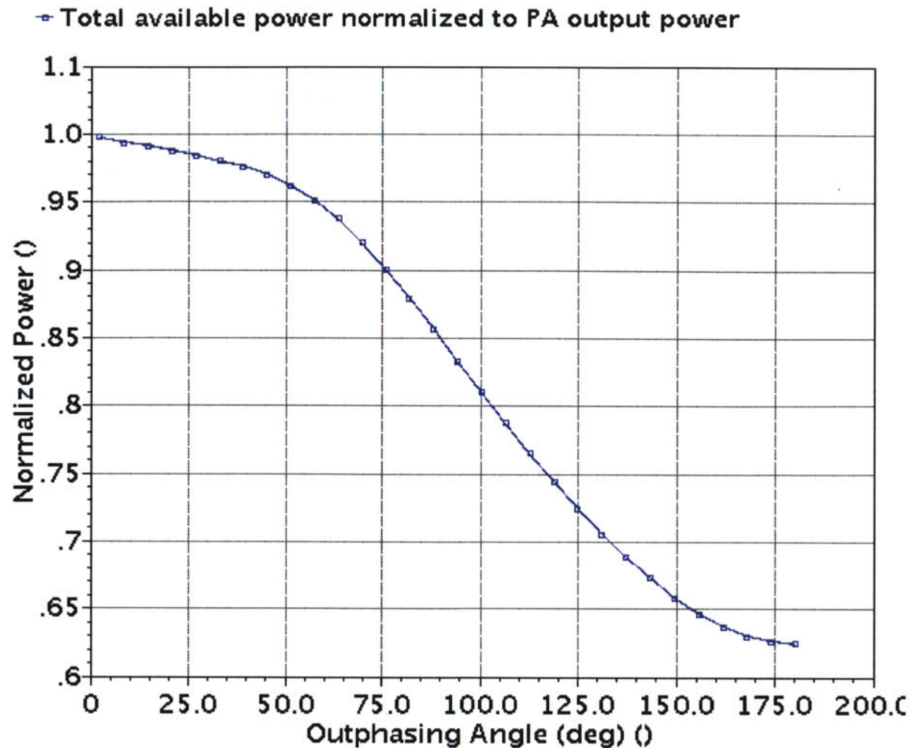


Figure 5-11: Total available power from outphasing system normalized to available power from the individual PAs.

With the use of energy recovery, the designer can take advantage of the high efficiency available from nonlinear switching PAs such as Class E but still have the capability of linear amplification. The use of the LINC architecture combined with energy recovery is a good technique to break the high-efficiency – linearity trade off in multi-gigahertz power amplifier design.

Fig. 5-11 is another way of viewing or analyzing the simulation results. Obviously with very low outphasing angles most of the power is delivered to the load making the normalized total available power = 1. What is useful to realize is that the normalized total available power is still 0.62 at the maximum outphasing angle of 180° emphasizing that a significant percentage of the power is not wasted but recycled.

5.2 Prototype Implementation

A prototype was built to test the efficacy of resistance compression networks for a resonant rectifier operating at 2.14 GHz. Note that the prototype to be tested was the energy recovery network (excluding the PA) whose components are highlighted with red dotted rectangles in Fig. 5-13. The constituent sections of the energy recovery network are the matching network, resistance compression network and the resonant rectifiers. Schottky barrier diodes (SBD) were fabricated in a 0.13-µm CMOS process. A chip-on-board test structure in which the input and output pads of the SBD structures were wirebonded to landpads on an FR4 PCB was employed.

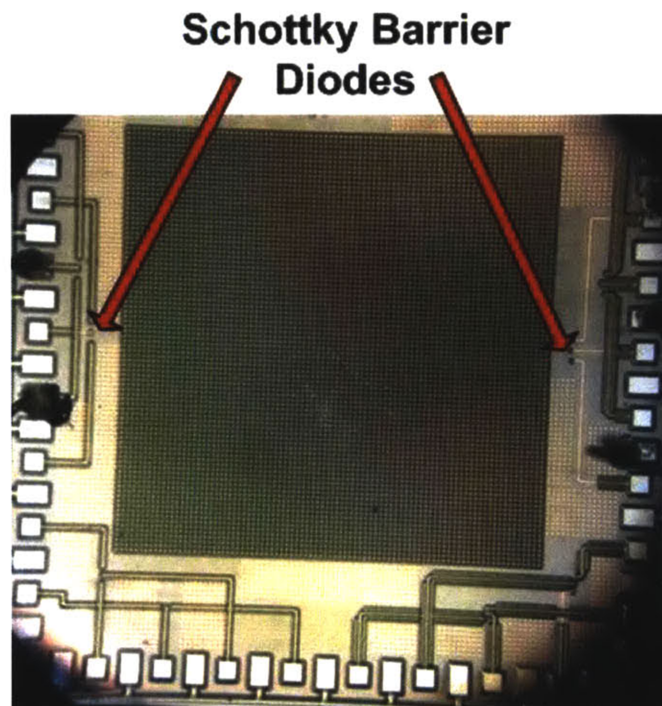


Figure 5-12: Chip micrograph showing integrated Schottky barrier diodes.

The SBDs consist of a metal-silicide junction surrounded by a p+ guard ring. These guard rings are included because the leakage current in reverse bias is especially high at the perimeter of the Schottky diode. The p+ guard ring helps to reduce this leakage. A chip micrograph of the SBD integrated on the silicon die is presented in Fig. 5-12. SBDs of several sizes were

fabricated so that the diode area power handing – switching speed tradeoff could be studied with measurements in the laboratory. It was found that the largest diodes fabricated (with a total of 400 μm^2 anode area) provided the best compromise for power and switching speed. The diode size used for the prototype implementation had a diode length = 20μm, diode width = 5μm and number of fingers = 4. For reasons similar to those stated in section 5.1, these relatively large diodes provide sufficient performance for our application. Future work could include using the more rigorous diode size selection process discussed in chapter 4.

A schematic of the energy recovery network which is essentially a resistance compressed RF-DC converter [23] is presented in Fig. 5-13. The system was designed to operate within an input power range of 28 mW to 140 mW. This power range was selected because the SBDs will operate within the exponential region of their I-V characteristics thus providing good efficiency. The resonant rectifier was constructed from integrated on-chip Schottky barrier diodes and an off- chip shunt 12 nH inductor. This inductance value was chosen with the aid of periodic steady state and transient simulations so that the fundamental component of the input voltage and current of the resonant rectifier are in phase. When this condition is satisfied, the input impedance of the resonant rectifier appears resistive at the fundamental frequency. The resistance compression network was fabricated on an FR4 substrate PCB with 0402 passive components to reduce package parasitics. Using the same design process described in section 5.1, the geometric mean of the input resistance range of the resonant rectifier was found to be 269 Ω. The 20nH inductor and 0.276 pF capacitor which were selected for the resistance compression network have a reactance approximately equal to 269 Ω at the operating frequency of 2.14 GHz. The resistance of the resonant rectifiers will be compressed around this reactance value. The output of the resonant rectifier was connected back to a 3.3 V power supply. It is

important to select the power supply voltage as high as possible to increase the efficiency of the resonant rectifier. The bigger the ratio of power supply voltage to Schottky diode forward voltage, the higher the resonant rectifier efficiency.

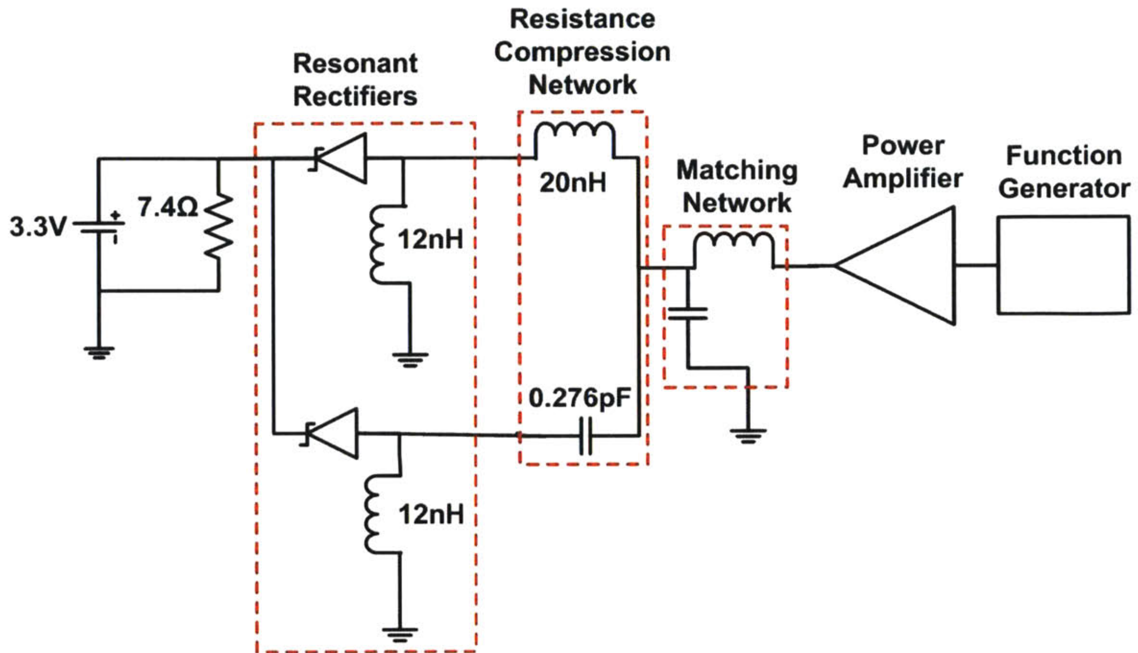
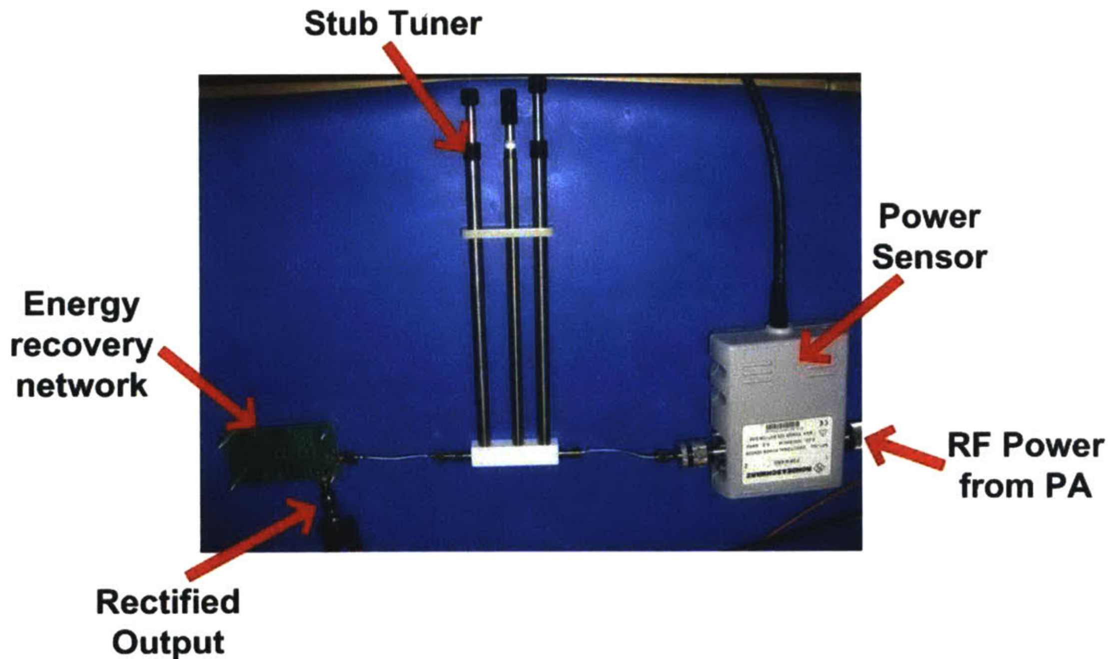
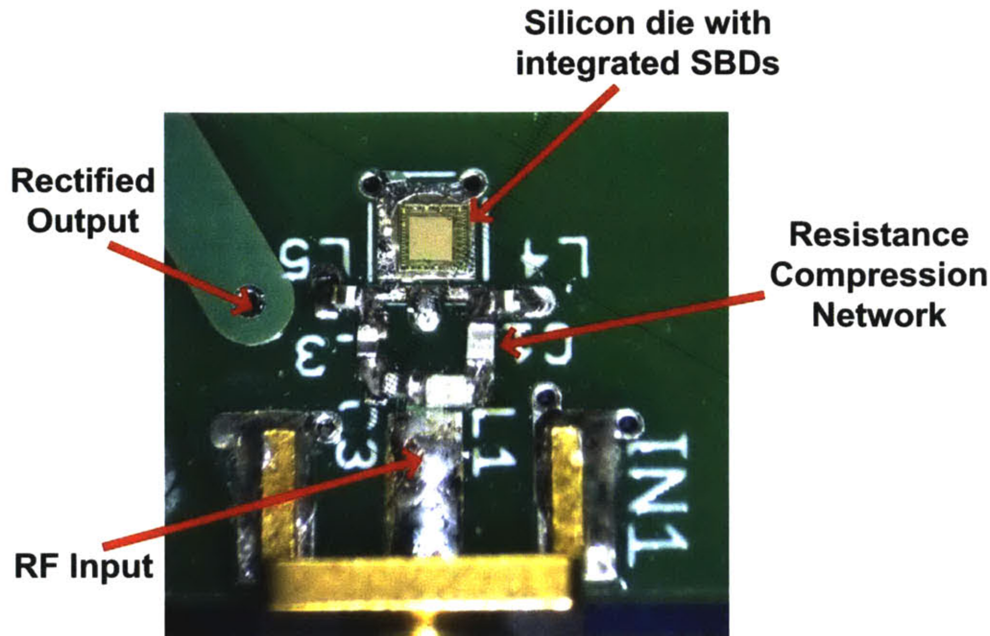


Figure 5-13: Schematic of energy recovery network.



(a) A section of the energy recovery network prototype measurement setup.



(b) Energy recovery network showing resistance compression network and silicon die with integrated Schottky barrier diodes

Figure 5-14. Measurement setup for the energy recovery network prototype.

A 7.4Ω resistor was put across the 3.3 V supply to mimic the steady current draw by the PA from the supply. In practice, the energy recovery network "returns power to the supply" by reducing the current draw by the PA from the supply. Some of the bias current required by the PA for operation is provided by the energy recovery network. Thus, the current which the supply needs to provide is reduced and a net increase in overall system efficiency is achieved. A mechanical stub tuner was used to match the input impedance of the energy recycling network (composed of the resonant rectifiers and resistance compression network) to the 50 Ω output resistance of a bench top Amplifier Research power amplifier. A Rhode&Schwarz through power meter which was placed between the bench top power amplifier and energy recovery network was used to measure the input reflection coefficient, S_{11}, at the input of the energy recycling network. Fig. 5-14 shows a picture of a section of the measurement setup.

5.3 Measurements and Results

Two incident power ranges with at a 10:1 ratio of maximum to minimum power were used in the testing of the energy recovery network (ERN) prototype presented in section 5.2. The ERN was matched to the 50Ω output of the bench top power amplifier at 65 mW and 140 mW incident power. In addition, the incident power range was selected such that the geometric mean of the maximum and minimum power coincided with the incident power at which the ERN was matched to the PA. The methodology for selection of the incident power level at which the ERN is matched ensures we can take advantage of resistance compression around the ERN resistance at that power level as indicated in Eq. 4.10 and Eq. 4.11. The inverse relationship between rectifier input resistance and incident power was presented in Eq. 4-4 and Eq. 4.6. Thus sweeping the incident power will change the match between the PA and energy recovery network and be reflected in a variation in the S_{11} of the ERN. The maximum incident power for all measurements was selected to be 400 mW. This value was chosen based on the simulation results presented in Fig. 5-2 and Fig. 5-8 for the similarly sized Schottky diode of length = 25μm. It was desired to keep the Schottky diodes operating mostly in the exponential region of their I-V characteristics so that the resonant rectifier and ERN efficiency remains relatively high for good system performance. It is also important to note that the selection of the incident power at which the ERN is matched depends on the modulation scheme used for the wireless transceiver the outphasing PA is a part of. The ERN should be matched to the isolation port of the power combiner at the most frequently occurring incident power levels. In addition, the resonant rectifier should be designed so that its input impedance is mostly resistive at this incident power. For instance, if a modulation scheme has a PAPR of 6 dB, the ERN should be matched for an incident power level that is 75% of the maximum PA output power. Thus, the

best average efficiency of the ERN will be obtained since the geometric mean of the energy recovery network's input impedance range is located at the most frequently occurring incident power.

The measurement results from testing the energy recovery prototype is presented in Fig. 5-15 and Fig. 5-16. Both figures feature a comparison between the performance of the energy recovery network (ERN) with and without the resistance compression network (RCN). Fig. 5-15 and Fig. 5-16 show the S_{11} and efficiency of the energy recovery network respectively. In Fig. 5-15a, the S_{11} values for incident powers less than 30 mW are not relevant because the Schottky diodes are either very weakly turned on or turned off. It can be seen that for an input power range of 30 mW to 240 mW, the S_{11} varies over a range of -23 dB to -8.5 dB for the energy recovery network without a resistance compression network. On the other hand, the S_{11} varies from -22.2 dB to -12.9 dB for the ERN with a RCN. The variation in S_{11} and hence, input resistance of the ERN is significantly compressed when a resistance compression network is added to the energy recovery network. Similarly, in Fig 5-15b, S_{11} varies from -22.2 dB to -9.1 dB for the energy recovery network without a resistance compression network while the setup which includes a RCN shows a S_{11} variation at the ERN's input of -25.2 dB to -15 dB. Although the S_{11} value does not contain any phase information, we can employ its definition to obtain an estimate of the range over which the ERN's resistance varies. Consider Eq. 5.4 below for an ERN matched to 50 Ω:

$$S_{11} \approx \Gamma = \frac{R_{\mathrm{ERN}} - R_{\mathrm{PA}}}{R_{\mathrm{ERN}} + R_{\mathrm{PA}}} \tag{5.4}$$

where R_{ERN} is the ERN input resistance, R_{PA} is the 50-Ω resistance at the output of the power sensor (see Fig. 14) and Γ is the reflection coefficient. From Eq. 5.4, the estimate of the ERN resistance is given by

$$R_{\text{ERN}} = \frac{1+\Gamma}{1-\Gamma} \quad (5.5)$$

Table 5.1 below shows the computed values of R_{ERN} using Eq. 5.5 and the S_{11} values measured in Fig. 5-15b:

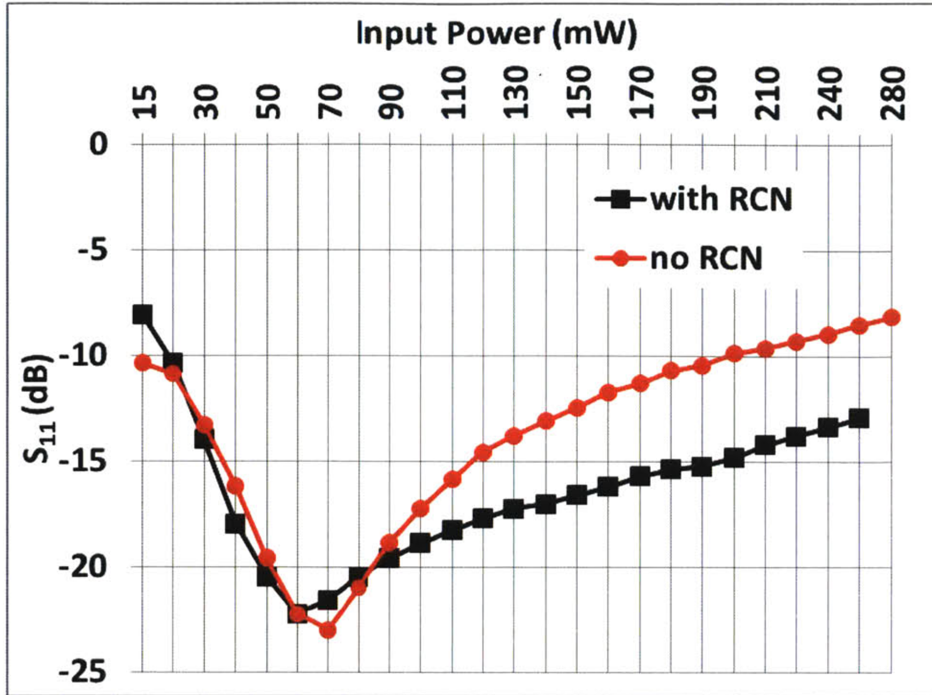
Table 5.1: Range of R_{ERN} for the values of S_{11} measured in Fig. 5-15b

	S_{11}(dB)	Γ	R_{ERN}
With RCN	-25.2	0.003	50.3
	-15	0.032	53.3
No RCN	-22.2	0.006	50.6
	-9.1	0.123	64.0

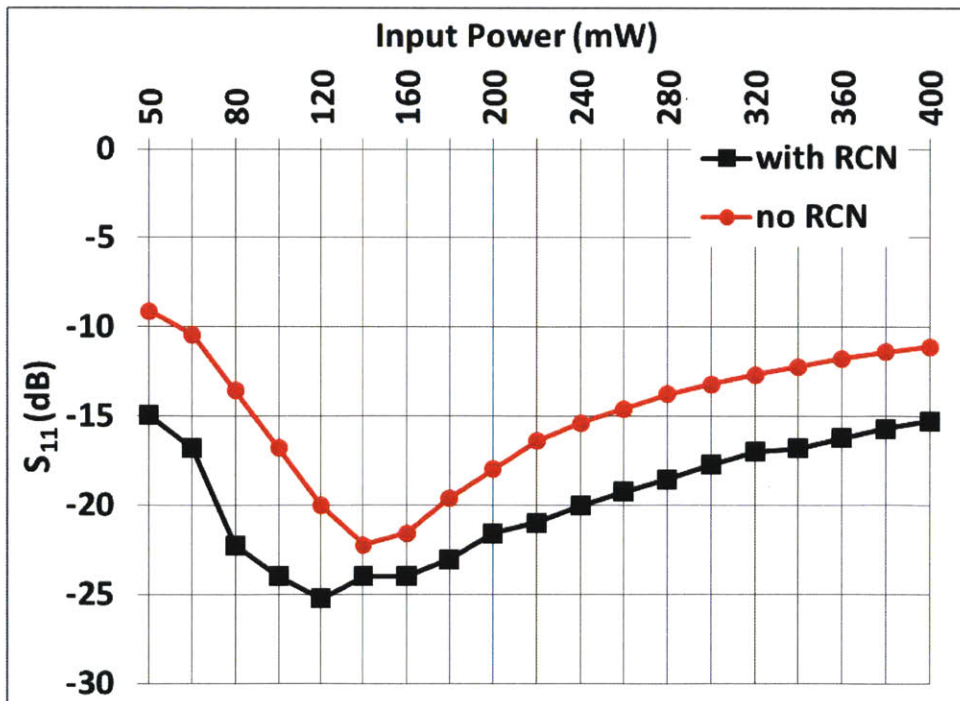
The results in table 5.1 indicate that the ERN without the RCN has an input resistance range, R_{ERN} of 50.6 Ω to 64 Ω. This resistance is compressed by the RCN to the smaller range of 50.3 Ω to 53.3 Ω. The smaller variation in R_{ERN} ensures there will be good isolation between the PAs when the ERN is included in an outphasing PA architecture such as AMO [31]. Note that for the calculation in table 5.1 to be accurate, we need to know the phase of the reflection coefficient, Γ which is not available from the power sensor's reading.

Fig. 5-16a presents a plot of the efficiency of the ERN when it is matched to the PA at 63 mW input power. The power range used is the same as in Fig. 5-15a. The peak efficiency of the ERN without an RCN is 39.6% while including an RCN shows a peak efficiency of 40.7%. Both numbers are comparable as expected because when the ERN is matched to the power source, most of the input power gets delivered to the resonant rectifier regardless of the presence of the RCN. The significant difference occurs when a change in input power causes the ERN to be no longer matched due to a change in the resonant rectifier input resistance with incident power.

The effect is exacerbated at lower incident power levels. For instance, at an incident power of 50 mW, the efficiency of the ERN without the RCN is just 20% while the version which contains an RCN is 40%. The smaller value of S_{11} in the latter case ensures that more power is incident on the resonant rectifier which will give the ERN that includes an RCN better efficiency. Moreover, at these relatively low input power levels, the Schottky diodes are very weakly turned on and operate within the exponential region of their I-V characteristics. Thus, the extra input power which gets delivered to the resonant rectifiers when a RCN is included with the ERN will exponentially increase the resonant rectifier's output current further increasing its efficiency. At higher input power levels, this effect is less pronounced because the Schottky diodes are now approaching the linear region of their I-V characteristics. But the ERN which includes a RCN still outperforms the version without the RCN because of the lower S_{11} means less power is wasted due to reflection. This fact can be seen at an incident power of 240 mW where the efficiency increases from 33% for the ERN without RCN to 39.5% for the version which includes a RCN. An important observation from the efficiency plot in Fig. 5-16a is the efficiency remains above 35% for most of the input power range because the compressed input resistance of the ERN keeps it closely matched to the input power source's (from the power sensor) 50-Ω resistance. A very similar state of affairs is observed in Fig 5-16b where the ERN is initially matched to the input power source at 140 mW incident power. The efficiency remains above 35% for the entire range of incident power for the energy recovery network which employs a resistance compression network. On the other hand, the version of the ERN without a RCN has an efficiency which drops to 20% when the incident power is 50 mW.

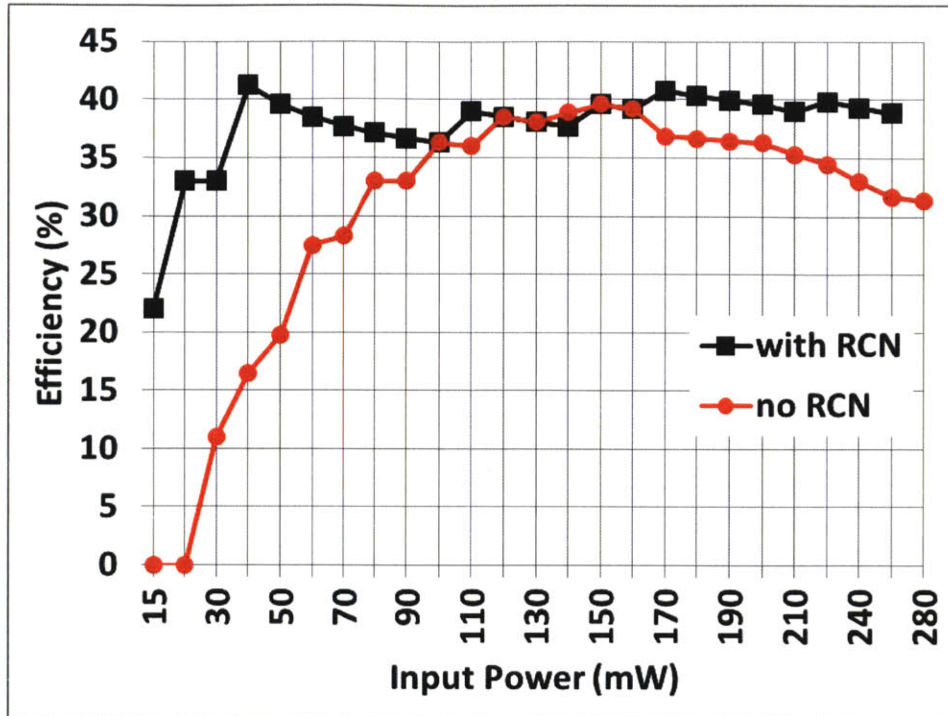


(a) S_{11} vs. input power for ERN matched at 65mW to PA

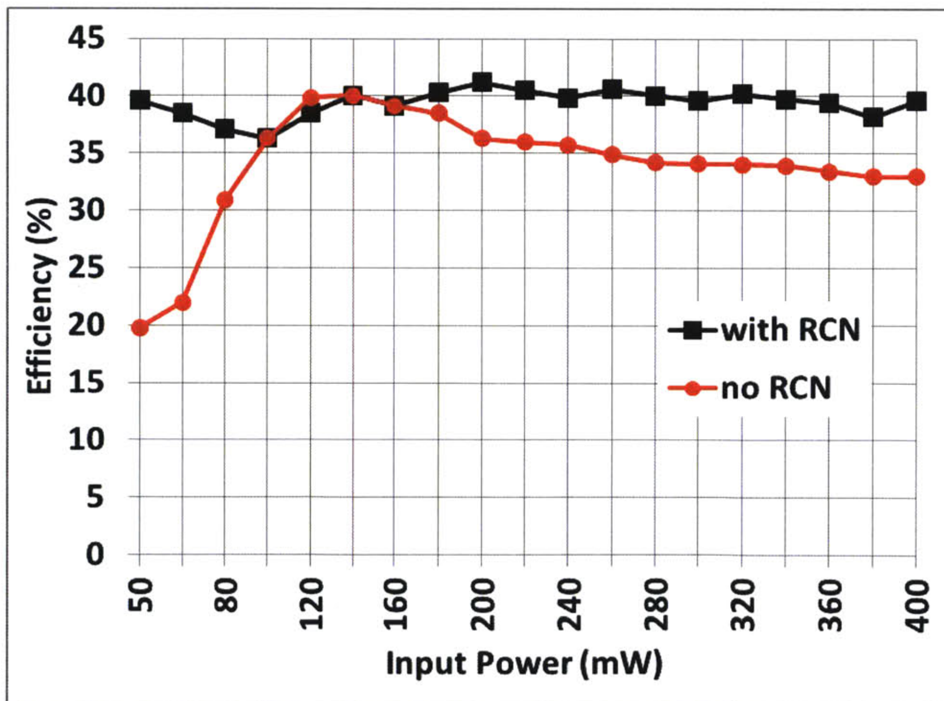


(b) S_{11} vs. input power for ERN matched at 140mW to PA

Figure 5-15: S_{11} of energy recycling network vs. input power.



(a) Efficiency vs. input power for ERN matched at 65mW to PA



(b) Efficiency vs. input power for ERN matched at 140 mW to PA

Figure 5-16: Efficiency of energy recycling network vs. Input power.

The performance of the energy recovery network with a RCN must be compared to a system with no RCN but with a circulator. When high-efficiency switching PAs such as class E are used in the outphasing PA which employs an energy recovery network without resistance compression, a circulator must be used. It is essential to ensure a fixed resistance is connected to isolation port of the power combiner to preserve the isolation between the PAs. The circulator approach has a few disadvantages. The use of a circulator will increase the complexity and cost of an outphasing amplifier and is not practical for mobile wireless applications. Moreover, a circulator or isolator can typically have as much as 1 dB of insertion loss which will decrease the efficiency of energy recovery network. In addition, the use of ordinary, surface-mount components makes the RCN a much more compact, much less expensive implementation of the energy recycling concept than with a circulator.

The measurement results presented in Fig. 5-15 and Fig 5-16 above clearly indicate the effectiveness of the resistance compression network at an operating frequency of 2.14 GHz. Although Godoy et al. in [22] successfully demonstrated an energy recovery network (ERN) which employs a resistance compression network linked with resonant rectifiers at 48 MHz, it was not certain that this approach would be feasible at multi-gigahertz frequencies. One difficulty with the use of an ERN is the interaction between the parasitic capacitance of the Schottky barrier diodes and the passive components in the ERN. This interaction makes the effective value of the reactance in each branch of the ERN to be no longer conjugate matched (see section 4.3 and Fig. 4-10). Moreover, the input impedance of each branch of the resonant rectifier – RCN cascade is also unequal. Thus, unequal power is delivered to each resonant rectifier and the resistances of the two resonant rectifiers are no longer matched because of the dependence of rectifier input resistance on incident power (see Eq. 4.4 and Eq. 4.6). As a result

of these conditions, the ERN performance was expected to degrade at multi-gigahertz frequencies where the adverse effects of the interaction between diode capacitance and the passive components in the ERN are exacerbated. Tuning or modification of the RCN inductor and capacitor calculated values are necessary to compensate for the diode capacitance – ERN interaction.

5.4 Summary

In this chapter, an energy recycling network which employs a resistance compression network to significantly reduce the variation in the input impedance of a resonant rectifier at 2.14 GHz has been demonstrated. The prototype system achieves 41% conversion efficiency for 200 mW of incident power, and maintains a reflected power of less than 3% for almost a 10:1 range of incident power. This energy recycling network will find application in outphasing power amplifier architectures that use isolating combiners and require a relatively constant resistance at the isolation port for efficient operation. To the authors' knowledge, this is the first experimental demonstration of resistance compression networks for energy recycling at multi-gigahertz frequencies.

Chapter 6

Conclusions and Future Work

6.1 Summary of Contributions

This work has provided contributions in two major categories. The first is conceptualizing and employing the class E tuned output network itself as an efficiency enhancement technique. The efficiency of classical power amplifier architecture (such as class A/AB) can be enhanced by replacing its load with a class E tuned output network. The transient response of the class E tuned output network reduces the region of overlap of non-zero drain voltage and drain current. This is sufficient to reduce the power dissipation in the active device and improve the PA's efficiency. The advantage of this approach is simpler classical PA architectures are more feasible at multi-gigahertz frequencies. The use of the class E tuned output network can enable the designer to take advantage of these PA architectures while minimizing the efficiency degradation. A robust iterative design approach was conceived and implemented which simplifies class E PA design. The matching of the input reflection coefficient, S_{11} of a lumped element implementation of the class E tuned output network to its transmission line equivalent was used to provide an efficient methodology for output network design.

The second area of contribution was the implementation of a resistance compression network in an energy recovery network to improve the efficiency of outphasing power amplifiers at multi-gigahertz frequencies. Previous work by Godoy et al. [22] had confirmed the feasibility of this approach at 48 MHz but it was not clear that energy recovery was possible at multi-gigahertz

frequencies. A resistance compression network which compresses the variation in the input resistance of an energy recovery network was implemented at 2.14 GHz. The successful implementation of this technique will find application in current wireless standards that can take advantage of the high efficiency of switching amplifiers in outphasing PA topologies while retaining the high linearity required for complex modulation schemes such as OFDM and 256-QAM.

6.2 Future Work

The energy recovery network along with a class E power amplifier and isolating combiner can be integrated on chip. The resultant removal of the bondwire inductance from the inputs of the resonant rectifiers should reduce the mismatch between the two branches of the energy recovery network and enhance the system's performance. The efficiency of the Asymmetric Multilevel Outphasing power amplifier architecture [28] can be further improved by employing an energy recovery network to recycle the energy from the difference port of the power combiner. The entire AMO power amplifier along with a resistance compressed energy recovery network can be implemented in a deeply scaled CMOS process for better overall system performance. This will make the technique relevant for current wireless applications.

Bibliography

[1] A. Siligaris, et. al, “A 60 GHz Power Amplifier With 14.5 dBm Saturation Power and 25% Peak PAE in CMOS 65 nm SOI”, *IEEE JSSC,* vol.45, pp. 1286-1294, June 2010.

[2] J. Chen and A.M. Niknejad, “A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS”, *IEEE ISSCC, pp. 432-433,* February 2011.

[3] J. Y.-C. Liu, et. al. “A V-band Self-Healing Power Amplifier with Adaptive Feedback Bias Control in 65 nm CMOS”, *IEEE RFIC*, pp. 1-4, June 2011.

[4] Y. Zhao, J. R. Long, and M. Spirito “A 60GHz-band 20dBm Power Amplifier with 20% Peak PAE”, *IEEE RFIC*, pp. 1-4, June 2011.

[5] S. Pornpromlikit, et. al “A Q-Band Amplifier Implemented with Stacked 45-nm CMOS FETs”, *IEEE CSICS,* pp. 1-4, October 2011.

[6] A. Valdes-Garcia, S. Reynolds, and U. R. Pfeiffer, “A 60 GHz class-E power amplifier in SiGe,” *IEEE A-SSCC*, pp. 199–202, November 2006.

[7] N. Kalantari and J.F. Buckwalter, “A 19.4 dBm, Q-Band Class-E Power Amplifier in a 0.12um SiGe BiCMOS Process”, *IEEE MWCL,* vol. 20, pp. 283-285, May 2010.

[8] N. O. Sokal and A. D. Sokal, “Class E – A New Class of High Efficiency Tuned Single-Ended Switching Power Amplifiers”, *IEEE JSSC*, vol. 10, pp. 168-176, June 1975.

[9] T. Mury and V. Fusco, "Exploring figures of merit associated with the suboptimum operation of class-E power amplifiers", *IET Circuits Devices Syst.*, vol. 1, pp. 401–407, December 2007.

[10] B. Razavi, "RF Microelectronics", *Prentice Hall Ptr,* 1998

[11] T.B. Mader, E.W. Bryerton, M. Markovic, M. Forman, Z. Popovic, "Switched-Mode High Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array", *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 10, October 1998.

[12] F.H. Raab, "Idealized Operation of the Class E Tuned Power Amplifer", *IEEE Transactions on Circuits and Systems*, vol. CAS-24, no 12, December 1977.

[13] M.Y. Bohsali, *"Millimeter – Wave CmOS Power Amplifers Design",* Ph.D. Dissertation, Electrical Engineering and Computer Sciences, University of California at Berkeley, February 2009.

[14] D.R. Greenberg, J-O. Plouchart, A. Valdes-Garcia, *"Electromigration-Compliant High Performance FET Layout"*, Patent Pub. No.: US 2012/0112819 A1, May 10, 2012

[15] Integrated Microelectronic Devices – Spring 2007 OCW Lecture 19, http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-720j integrated-microelectronic-devices-spring-2007/lecture- notes/lecture19.pdf

[16] S.C. Cripps, RF Power Amplifiers for Wireless Communications, 2nd ed., Artech House Microwave Library

[17] H. Chireix, "High-power outphasing modulation," Proc. IRE, vol. 23,pp. 1370–1392, Nov. 1935.

[18] Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto, "A 2.14-GHz Chireix outphasing transmitter," IEEE Trans. Microw. Theory Tech., vol. 53, no. 6, pp. 2129–2138, Jun. 2005.

[19] F. H. Raab, "Efficiency of outphasing RF power-amplifier systems,"IEEE Trans. Commun., vol. 33, no. 9, pp. 1094–1099, Sep. 1994.

[20] R. Langridge, T. Thornton, P. M. Asbeck, and L. E. Larson, "A power re-use technique for improved efficiency of outphasing microwave pp. power amplifiers," IEEE Trans. Microw. Theory Tech., vol. 47, no. 8, 1467–1470, Aug. 1999.

[21] X. Zhang, L. E. Larson, P. M. Asbeck, and R. A. Langridge, "Analysis of power recycling techniques for RF and microwave outphasing power amplifiers," IEEE Trans. Circuits Syst. II, vol. 49, no. 5, pp. 312–320,May 2002.

[22] P.A. Godoy, D.J. Perreault, J.L. Dawson, "Outphasing Energy Recovery Amplifier With Resistance Compression for Improved Efficiency," IEEE Trans. Microw. Theory Tech., vol. 57, no. 12, pp. 2895–2906, Dec. 2009.

[23] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas, and D. J. Perreault, "Resistance compression networks for radio-frequency power conversion,"IEEE Trans. Power Electron., vol. 22, no. 1, pp. 41–53, Jan. 2007.

[24] R. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," in Proc. 37th IEEE Power Electron. Spec. Conf., Jun. 2006,pp. 2287–2297.

[25] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, Principles of Power Electronics. Reading, MA: Addison-Wesley, 1992, ch. 3.

[26] R. Gutmann and J. Borrego, "Power combining in an array of microwave power rectifiers," IEEE Trans. Microw Theory Tech., vol. MTT-27, no. 12, pp. 958–968, Dec. 1979.

[27] W. A. Nitz, W. C. Bowman, F. T. Dickens, F. M. Magalhaes, W. Strauss, W. B. Suiter, and N. G. Ziesse, "A new family of resonant rectifier circuits for high frequency dc-dc converter applications," in Proc. Applied Power Electron. Conf., Feb. 1988, pp. 12–22.

[28] P.A. Godoy, S. Chung, T.W. Barton, D.J. Perreault, and J.L. Dawson, "A 2.5-GHz, Asymmetric Multilevel Outphasing Power Amplifier in 65-nm CMOS," 2011 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications, pp. 57–60, 2011.

[29] C. H. Doan, S. Emami, D. Sobel, A. M. Niknejad, and R.W. Brodersen, "60 GHz CMOS radio for Gb/s wireless LAN," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, , pp. 225-228, June 2004.

[30] D. C. Cox, "Linear Amplification with Nonlinear Components," IEEE Transactions on Communications, vol. 22, No. 12, pp. 1942-1945, Dec. 2004.

[31] S. Chung, P.A. Godoy, T.W. Barton, D.J. Perreault, and J.L. Dawson, "Asymmetric multilevel outphasing transmitter using class-E PAs with discrete pulse width modulation," 2010 IEEE MTT-S International Microwave Symposium Digest, pp. 264-267, May 2010.

[32] P.A. Godoy, S. Chung, T.W. Barton, D.J. Perreault, and J.L. Dawson,"A highly efficient 1.95-GHz, 18-W asymmetric multilevel outphasing transmitter for wideband applications," 2011 IEEE MTT-S International Microwave Symposium Digest, pp. 1-4, June 2011.